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MT6735 LTE Smartphone Application Processor Functional Specification

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Document Revision History

Revision	Date	Author	Description
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Preface

Acronyms for register types

R/W	For both read and write access
RO	Read only
RC	Read only. After the register bank is read, every bit that is HIGH(1) will be cleared to LOW(0) automatically.
WO	Write only
W1S	Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be set to 1. Data bits that are LOW(0) have no effects on the corresponding bit.
W1C	Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be cleared to 0. Data bits that are LOW(0) have no effects on the corresponding bit.

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1 System Overview

The MT6735 device (see Figure 1-1), with integrated Bluetooth, FM, WLAN and GPS modules, is a highly integrated baseband platform incorporating both modem and application processing subsystems to enable LTE smart phone applications,. The chip integrates Quad-core ARM® Cortex-A53 operating up to 1.3GHz, an ARM® Cortex-R4 MCU and powerful multi-standard video codec. In addition, an extensive set of interfaces and connectivity peripherals are included to interface to cameras, touch-screen displays and MMC/SD cards.

The application processor, an Quad-core ARM® Cortex-A53 MPCore™ equipped with NEON engine offers processing power necessary to support the latest OpenOS along with its demanding applications such as web browsing, email, GPS navigation and games.
All are viewed on a high resolution touch screen display with graphics enhanced by the 2D and 3D graphics acceleration.

The multi-standard video accelerator and an advanced audio subsystem are also integrated to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders.

An ARM® Cortex-R4, DSP, and 2G and 3G coprocessors combined provide a powerful modem subsystem capable of supporting LTE Cat 4, Category 24 HSDPA downlink and Category 7 HSUPA uplink data rates, Category 14 TD-HSDPA downlink and Category 6 TD-HSUPA uplink, as well as Class 12 GPRS, EDGE. Supports cdma2000 HRPD/1xEV-DO Revision 0 and A (3.1Mbps for forward link and 1.8Mbps for reverse link).

MT6735 also embodies wireless communication device, including WLAN, Bluetooth and GPS. With four advanced radio technologies integrated into one single chip, MT6735 provides the best and most convenient connectivity solution in the industry.

The enhanced overall quality is achieved for simultaneous voice, data and audio/video transmission on mobile phones and Media Tablets. The small footprint with low-power consumption greatly reduces the PCB layout resource.

1.1 Highlighted Features Integrated in MT6735

- Quad-core ARM® Cortex-A53 MPCore™ operating at 1.3GHz
- LPDDR3 up to 3GB, 640MHz
- LTE Cat 4 (150Mnps)
- CDMA200 HEPD/ 1xEV-DO Revision 0 and A.
- Embedded connectivity system including WLAN/BT/FM/GPS
- Resolution up to HD (1,280*720)
- OpenGL ES 3.0 3D graphic accelerator
- ISP supports 13MP@30fps.
- H.264 1080p @ 30fps encoder
- Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)

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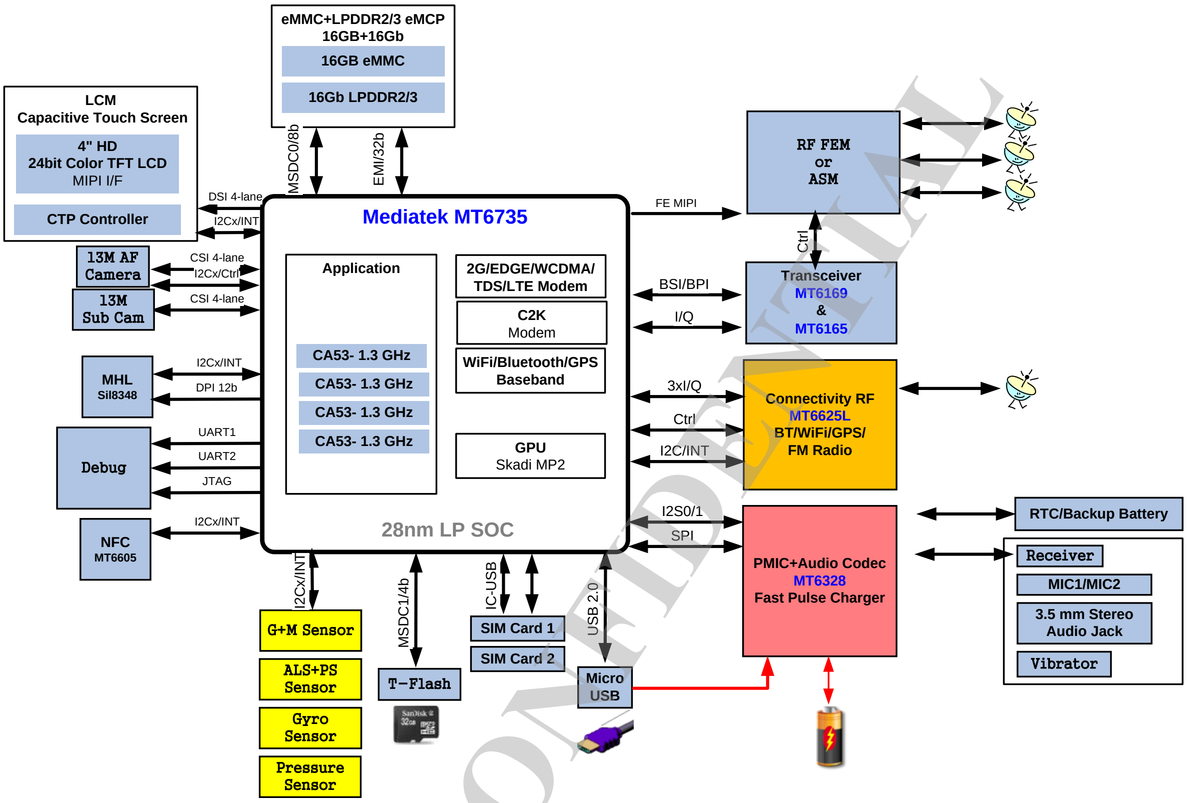

Figure 1-1. High-level MT6735 functional block diagram

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1.2 Platform Features

- **General**
  - Smartphone, two MCU subsystems architecture
  - eMMC boot support
  - Supports LPDDR-2/LPDDR-3

- **AP MCU subsystem**
  - Quad-core ARM® 1.3Ghz Cortex-A53 MPCore™
  - NEON multimedia processing engine with SIMDv2/VFPv4 ISA support
  - 32KB L1 I-cache and 32KB L1 D-cache
  - 512KB unified L2 cache
  - DVFS technology with adaptive operating voltage from 0.85V to 1.25V

- **MD MCU subsystem**
  - ARM® Cortex-R4 processor with max. 600MHz operation frequency
  - 64KB I-cache, 64KB D-cache
  - 512KB TCM (tightly-coupled memory)
  - Coresonic DSP for running LTE modem tasks, with max. 240MHz operation frequency
  - FD216 DSP for running modem/voice tasks, with max. 250MHz operation frequency
  - High-performance AXI and AHB bus
  - General DMA engine and dedicated DMA channels for peripheral data transfer
  - Watchdog timer for system error recovery
  - Power management for clock gating control

- **MD external interfaces**
  - Dual SIM/USIM interface
  - Interface pins with RF and radio-related peripherals (antenna tuner, PA, etc.)

- **Security**
  - ARM® TrustZone® Security

- **External memory interface**
  - LPDDR2/3 up to 3GB
  - Single channel with 32-bit data bus width
  - Memory clock up to 640MHz
  - Self-refresh/partial self-refresh mode
  - Low-power operation
  - Programmable slew rate for memory controller's IO pads
  - Dual rank memory device
  - Advanced bandwidth arbitration control

- **Peripherals**
  - USB2.0 HS/FS support
  - eMMC5.1
  - 4 UART for debugging and applications
  - SPI master for external device
  - 4 I2C to control peripheral devices, e.g. CMOS image sensor, LCM or FM receiver module
  - Max. 5 PWM channels (depending on system configuration/IO usage)
  - I2S for connection with optional external hi-end audio codec
  - GPIOs
  - 3 sets of memory card controllers supporting SD/SDHC/MS/MSPRO/MMC and SDIO2.0/3.0 protocols

- **Operating conditions**
  - Core voltage: 1.15V
  - I/O voltage: 1.8V/2.8V/3.3V
  - Memory: 1.2V
  - LCM interface: 1.8V
  - Clock source: 26MHz, 32.768kHz

- **Package**
  - Type: VFBGA
  - 12.6mm*12.6mm

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- Height: Max. 0.9mm
- Ball count: 641 balls
- Ball pitch: 0.4mm

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1.3 MODEM Features

- **LTE**
  - FDD: Up to 150Mbps downlink, 50Mbps uplink
  - TDD: Up to 150Mbps downlink, 50Mbps uplink
  - 1.4 to 20MHz RF bandwidth
  - 2*2 downlink SU-MIMO; 4*2 downlink SU-MIMO
  - IPv6, QoS
  - Inter-RAT capabilities with HSPA+, EDGE and applicable backward-compatible modes
  - SNOW3G/ZUC cipher offload engine
- **3G UMTS FDD supported features**
  - 3G modem supports most main features in 3GPP Release 7 and Release 8
  - CPC (DTX in CELL_DCH, UL DRX DL DRX), HS-SCCH-less, HS-DSCH
  - Dual cell operation
  - MAC-ehs
  - 2 DRX (receiver diversity) schemes in URA_PCH and CELL_PCH
  - Uplink Cat. 7 (16QAM), throughput up to 11.5Mbps
  - Downlink Cat. 24 (64QAM, dual-cell HSDPA), throughput up to 42.2Mbps
  - Fast dormancy
  - ETWS
  - Network selection enhancements
- **TD-SCDMA**
  - CDMA/HSDPA/HSUPA baseband
  - TD-SCDMA Bands 34, 39 & 40 and Quad band GSM/EDGE
  - Circuit-switched voice and data; packet-switched data
  - 384/384Kbps class in UL/DL for TD-SCDMA
  - TD-HSDPA: 2.8Mbps DL (Cat.14)
  - TD-HSUPA: 2.2Mbps UL (Cat.6)
  - F8/F9 ciphering/integrity protection
- **Radio interface and baseband front-end**
  - High dynamic range delta-sigma ADC converts the downlink analog I and Q signals to digital baseband.
  - 10-bit D/A converter for Automatic Power Control (APC)
  - Programmable radio Rx filter with adaptive gain control
  - Dedicated Rx filter for FB acquisition
  - Baseband Parallel Interface (BPI) with programmable driving strength
  - Supports multi-band
- **GSM modem and voice CODEC**
  - Dial tone generation
  - Noise reduction
  - Echo suppression
  - Advanced side-tone oscillation reduction
  - Digital side-tone generator with programmable gain
  - 2 programmable acoustic compensation filters
  - GSM quad vocoders for adaptive multi-rate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
  - GSM channel coding, equalization and A5/1, A5/2 and A5/3 ciphering
  - GPRS GEA1, GEA2 and GEA3 ciphering
  - Programmable GSM/GPRS/EDGE modem
  - Packet switched data with CS1/CS2/CS3/CS4 coding schemes
  - GSM circuit switch data
  - GPRS/EDGE Class 12
  - Supports SAIC (Single Antenna Interference Cancellation) technology
  - VAMOS (Voice services over Adaptive Multi-user channels on One Slot) technology in R9 spec

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- **CDMA2000**
  - Supports cmda2000 1xRTT (release 1 and Advanced) and cdma2000 HRPD/1xEV-DO Revision 1 and A.
  - Hybrid operation between 1x and HEPD
  - Simultaneous hybrid dual receiver (SHDR) support.
  - Supports maximum 1x data rates of 153.6kbps for forward and reverse links and DO data rates of 3.1Mbps for forward link and 1.8Mbps for reverse link.
  - Supports 1x Diversity.

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1.4 Connectivity Features

MT6735 includes four wireless connectivity functions:

- WLAN
- Bluetooth
- GPS
- FM Receiver

The RF parts of those four blocks are placed on chip MT6625. With four advanced radio technologies integrated on one chip, MT6735/MT6625 is the best and most convenient connectivity solution in the industry,MT6735 implementing advanced and sophisticated Radio Coexistence algorithms and hardware mechanisms. It supports single antenna sharing among 2.4 GHz Bluetooth, 2.4GHz/5GHz WLAN and 1.575 GHz for GPS. The enhanced overall quality is achieved for simultaneous voice, data and audio/video transmission on mobile phones and Media Tablets. The small footprint with low-power consumption greatly reduces PCB layout resource. MT6735 also supports 802.11ac WLAN in advanced assorted with MT6630.

- **Supports integrated WIFI/BlueTooth/GPS**
  - Single antenna for Bluetooth and WLAN/GPS/Bluetooth
  - Self calibration
  - Single TCXO and TMS for GPS, BT and WLAN
  - Best-in-class current consumption performance
  - Intelligent BT/WLAN coexistence scheme that goes beyond PTA signaling (e.g. transmit window and duration that take into account protocol exchange sequence, frequency, etc.)
- **Wi-Fi**
  - Dual-band (2.4GHz/5Ghz) single stream 802.11 a/b/g/n MAC/BB/RF
  - 802.11 d/h/k compliant
  - Security: WFA WPA/WPA2 personal, WPS2.0, WAPI (hardware)
  - QoS: WFA WMM, WMM PS
  - 802.11n optional features: STBC, A-MPDU, Blk-Ack, RIFS, MCS Feedback, 20/40MHz coexistence (PCO), unscheduled PSMP
  - Supports 802.11w protected managed frames
  - Supports Wi-Fi Direct (WFA P-2-P standard) and Wi-Fi Miracast (Wi-Fi Display)
  - Supports Wi-Fi HotSpot 2.0
  - Integrated 2.4GHz PA with max. 19dBm CCK output power and 5GHz PA with max. 17dBm OFDM 54Mbps output power
  - Typical Rx sensitivity with companion chip modem: -75dBm at 11g 54Mbps mode and -75.5dBm at 11a 54Mbps mode
  - Per packet TX power control
- **BlueTooth**
  - Bluetooth specification v2.1+EDR
  - Bluetooth specification 3.0+HS compliance
  - Bluetooth v4.0 Low Energy (LE)
  - Integrated PA with 6dBm (class 1) transmit power
  - Typical Rx sensitivity with companion chip modem: GFSK -92.5dBm, DQPSK -91.5dBm, 8-DPSK -86dBm
  - Best-in-class BT/Wi-Fi coexistence performance
  - Up to 4 piconets simultaneously with background inquiry/page scan
  - Supports Scatternet

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- Packet Loss Concealment (PLC) function for better voice quality
- Low-power scan function to reduce power consumption in scan modes

- **GPS**
  - GPS/Glonass/Beidou/Galileo/ QZSS tri-band reception concurrently
  - Supports SBAS (Satellite-Based Augmentation Systems): WAAS/MSAS/EGNOS/GAGAN
  - Best-in-class sensitivity performance
    - -165 dBm tracking sensitivity
    - -163 dBm hot start sensitivity
    - -148 dBm cold start sensitivity
    - -151 dBm warm start sensitivity
  - AGPS sensitivity is 6dB design margin over 3GPP
  - Full A-GPS capability (E911/SUPL/EPO/HotStill)
  - Active interference cancellation for up to 12 in-band tones
  - Supports both TCXO and TMS (Thermister Crystal) clock source
  - 5Hz update rate

- **FM**
  - 65-108MHz with 50kHz step
  - RDS/RBDS
  - Digital stereo demodulator
  - Simplified digital audio interface (I2S)
  - Stereo noise reduction
  - Audio sensitivity 2dBµVemf (SINAD=26dB)
  - Audio SINAD 60dB
  - Anti-jamming
  - Integrated short antenna

- **WBT IPD**
  - Integrated matching network, balance band-pass filter, GPS-WBT diplexer
  - Fully integrated in one IPD die
  - Single and dual antenna operation

- **GPS IPD**
  - Integrated high-pass type matching network and 5th-order ellipse low-pass filter
  - Fully integrated in one IPD die
  - Single and dual antenna operation

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1.5 Multimedia Features

- **Display**
  - Portrait panel resolution up to HD (1,280*720)
  - MIPI DSI interface (4 data lanes)
  - MiraVision™ for picture quality enhancement
  - ClearMotionTM for DTV-class video quality
  - Embedded LCD gamma correction
  - True colors
  - 4 overlay layers with per-pixel alpha channel and gamma table
  - Single and dual antenna operation, spatial and temporal dithering
  - Side-by-side format output to stereo 3D panel in both portrait and landscape modes
  - Color enhancement
  - Adaptive contrast enhancement
  - Image/video/graphic sharpness enhancement
  - Dynamic backlight scaling
  - Wide gamut

- **Graphics**
  - 3D graphic accelerator capable of processing 100M tri/sec and 900M pixel/sec @ 450 MHz
  - Support API standards OpenGL ES 1.1/2.0/3.0, OpenCL 1.0/1.1/1.2 and DirectX9

- **Image**
  - Integrated image signal processor supports 13MP@30fps.
  - Electronic image stabilization
  - Video stabilization
  - Preference color adjustment
  - Noise reduction
  - Multiple frame noise reduction for image capture
  - Temporal noise reduction for video recording
  - Lens shading correction
  - Auto sensor defect pixel correction
  - Supports AE/AWB/AF
  - Edge enhancement (sharpness)
  - Face detection and visual tracking
  - Video face beautification
  - Zero shutter delay image capture
  - Captures full size image when recording video (up to 13M sensors)
  - 2 MIPI CSI-2 high-speed camera serial interfaces; both are 4 data lane
  - PIP (picture in picture), [13MP + 5MP]@15fps
  - Hardware JPEG encoder: Baseline encoding with 130M pixel/sec. Continuous shot with 96M pixel/sec
  - Supports YUV422/YUV420 color format and EXIF/JFIF format

- **Video**
  - H.264 decoder: Baseline 1080p @ 30fps/40Mbps
  - H.264 decoder: Main/high profile 1080p @30fps/40Mbps
  - Sorenson H.263/H.263 decoder: 1080p @ 30fps/40Mbps
  - MPEG-4 SP/ASP decoder: 1080p @ 30fps/40Mbps
  - DIVX4/DIVX5/DIVX6/DIVX HD/XVID decoder: 1080p @ 30fps/40Mbps
  - H.264 encoder: High profile 1080p @ 30fps

- **Audio**
  - Audio content sampling rates supported: 8kHz to 192kHz
  - Audio content sample formats supported: 8-bit/16-bit/24-bit, Mono/Stereo
  - Interfaces supported: I2S, PCM

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- External CODEC I2S interface supports 16-bit/24-bit, Mono/Stereo, 8kHz to 192kHz.
- 4-band IIR compensation filter to enhance loudspeaker responses
- Proprietary audio post-processing technologies: BesLoudness(MB-DRC), BesSurround, Android built-in post processing
- Audio encoding: AMR-NB, AMR-WB, AAC, OGG, ADPCM
- Audio decoding: WAV, MP3, MP2, AAC, AMR-NB, AMR-WB, MIDI, Vorbis, APE, AAC-plus v1, AAC-plus v2, FLAC, WMA, ADPCM

- **Speech**
  - Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)
  - CTM
  - Noise reduction
  - Noise suppression
  - Noise cancellation
  - Dual-MIC noise cancellation
  - Echo cancellation
  - Echo suppression
  - Dual-MIC voice tracking
  - Dual-MIC sound recording w/o Wind Noise Rejection
  - MagiLoudness (enhances the voice clarity based on near end environment noise)
  - MagiClarity (maximizes loudness while controlling the maximum receiver output power; feed-forward receiver protection)
  - Compensation filter and digital gain for both uplink and downlink paths

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1.6 General Description

MediaTek's MT6735 is a highly integrated LTE System-on-Chip (SoC) which incorporates advanced features, e.g. LTE cat.4, Octa HMP core operating at 1.3GHz, 3D graphics (OpenGL|ES 3.0), 13M camera ISP, LPDDR3-640 Mbps, HD display and 1080p video codec. MT6735 helps phone manufacturers build high-performance LTE smart phones with PC-like browser, 3D gaming and cinema class home entertainment experiences.

The World-leading Technology!

Based on MediaTek's world-leading mobile chip SoC architecture with advanced 28nm process, MT6735 is the brand-new generation smart phone SoC integrating MediaTek LTE modem, Quad-core ARM® Cortex-A53 MPCore™, 3D graphics and high-definition 1080p video decoder.

Rich in Features, High-value Product!

To enrich camera features, MT6735 equips a 13M camera ISP with advanced features, e.g. auto focus, electrical stabilization, auto sensor defect pixel correction, continuous video AF, face detection, face beautify, burst shot, optical zoom, panorama view, picture in picture, video in video and video face beautication.

Incredible Browser Experience!

The powerful CPU architecture with NEON multimedia processing engine brings PC-like browser experiences while keeping low standby power. GPU supporting OpenGL|ES 3.0 also provides you with excellent multimedia experiences.

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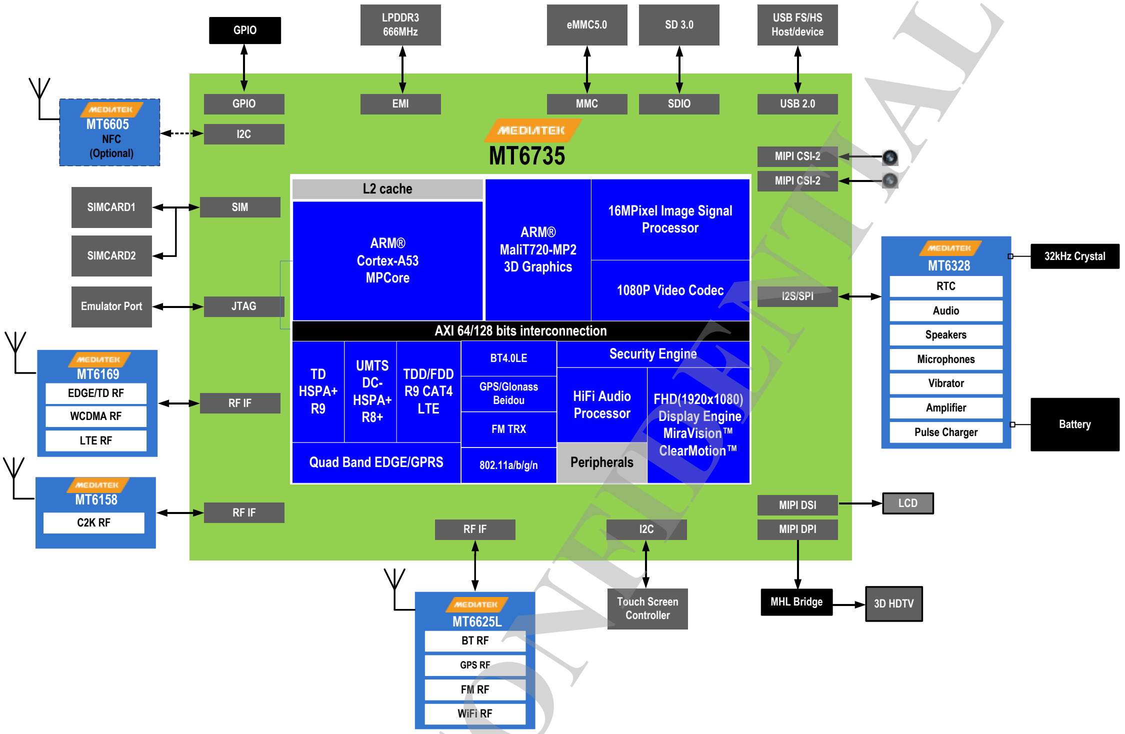

Figure 1-2. Block diagram of MT6735

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2 Product Description

2.1 Pin Description

2.1.1 Ball Map View

641	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
A	NC	NC	RA2		RA4	RA3		RDQ17	RDQ16		RDQ22	RDQ0		RDQ6	RDQ7		RDQ14	RDQ15		RDQ27	RDQ31		MSDC0_DAT	MSDC0_DAT		MSDC0_DAT	DVSS		WB_SEN	NC	NC	A
B	NC	RA8	RCS1_B	RCS_B	DVSS	RA1	DVSS	RDQ18	DVSS	RDQ20	RDQ19	RDQ2	RDQ4	DVSS	RDQ8	RDQ9	RDQ11	DVSS	RDQ25	RDQ28	RDQ30	RDQ29	DVSS	MSDC0_CM	MSDC0_DAT	MSDC0_DAT	WB_SCLK	WB_SDATA	WB_RSTB	AVDD18_W	NC	B
C		RA7	RA6			DVSS	RDQ21			RDQ1	RDQ3			RDQM1	DVSS			RDQ13	RDQM3			DVSS	MSDC0_CLK			DVSS	DVDD18_M	DVDD18_CO	AVSS18_WB	GPS_RXQP	GPS_RXQN	C
D	RA9	RA5	DVSS	RCKE	DVSS	RA0	RDQM2	DVSS	RDQ23	DVSS	DVSS	RDQ5		RDQM0	RDQ10		RDQ12	DVSS		RDQ24	RDQ26		MSDC0_DAT		MSDC0_DAT	MSDC0_RST	F2W_DATA	F2W_CLK	AVSS18_WB	GPS_RXIN		D
E	AVDD18_M	REXTDN	AVSS18_ME						RCLK0_B			RDQS2			RDQS0		RDQS1			RDQS3_B			MSDC0_DAT	DVSS	MSDC0_DSL		XIN_WBG	AVSS18_WB		GPS_RXIP	AVSS18_WB	E
F		MSDC1_CM	DVDD18_M						RCLK0			RDQS2_B			RDQS0_B	VREF	RDQS1_B			RDQS3							AVSS18_WB	AVSS18_WB	WB_CTRL0	WB_TXQP	WB_TXQN	F
G	DVDD28_M	MSDC1_DAT		MSDC1_DAT					DVDD12_E	DVSS		DVDD12_E	DVSS	DVDD12_E	DVSS	DVDD12_E	DVSS	DVDD12_E										WB_CTRL2	WB_CTRL1	WB_TXIN		G
H	DVDD28_SI	MSDC1_DAT	MSDC1_CLK	MSDC1_DAT					DVDD12_E	DVSS		DVDD12_E	DVSS	DVDD12_E	DVSS	DVDD12_E	DVSS	DVDD12_E										WB_CTRL4	WB_CTRL3	WB_TXIP	WB_RXQN	H
J		SIM1_SIO		SIM1_SRST																								ANT_SEL0	WB_CTRL5	WB_RXIN	WB_RXQP	J
K	SIM2_SIO	SIM2_SRST		SIM1_SCLK			DVSS	DVDD CORE	DVSS																		DVDD18_IOL	MSDC2_CM		WB_RXIP		K
L		DVDD28_SI	AVSS18_MIP	SIM2_SCLK			DVDD CORE	DVDD CORE	DVDD CORE	DVDD CORE	DVDD CORE	DVDD CORE	DVSS	DVDD SRA	DVDD CORE	DVDD CORE	DVSS	DVSS	DVDD CORE	DVDD CORE	DVDD CORE	DVDD CORE	DVSS				MSDC2_DAT	ANT_SEL2	MSDC2_CLK	AVSS18_WB	DVDD28_M	L
M	TDP3	TDN3	TDN2				DVSS	DVDD CORE	DVSS	DVDD CORE	DVSS	DVDD CPU	DVDD CPU		DVDD CPU	DVDD CPU	DVDD CPU	DVDD CPU	DVDD CPU	DVDD CPU	DVSS	DVDD CORE	DVSS				MSDC2_DAT	ANT_SEL1		MSDC2_DAT	MSDC2_DAT	M
N	TCN	TCP	TDP2				DVSS	DVDD CORE	DVSS	DVDD CORE	DVSS	DVDD CPU	DVDD CPU	DVDD CPU	DVDD CPU	DVDD CPU	DVDD CPU	DVDD CPU	DVDD CPU	DVDD CPU	DVSS	DVDD CORE	DVSS				AVSS18_MIP	RCN	RDP0	AVDD18_MI		N
P		TDN0	TDN1				DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS							RCP	RDN0	RDP1	RDN1	P
R	VRT	TDP0	TDP1				DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS							RCN_A	RDN0_A	RDN2		R
T	AVDD18_MI	AVDD33_US	CHD_DP	CHD_DM			DVSS	DVDD CORE	DVSS	DVDD CORE	DVSS	DVDD CPU	DVDD CPU	DVDD CPU	DVDD CPU	DVDD CPU	DVDD CPU	DVDD CPU	DVDD CPU	DVDD CPU	DVSS	DVDD CORE	DVSS					RCP_A	RDP0_A	RDP2	RDP3	T
U		USB_DP		WATCHDOG			DVDD CORE	DVDD CORE	DVDD CORE	DVDD CORE	DVDD CORE	DVDD CPU	DVDD CPU	DVDD CPU	DVDD CPU	DVDD CPU	DVDD CPU	DVDD CPU	DVDD CPU	DVDD CPU	DVSS	DVDD CORE	DVDD CORE					RDN3_A	RDN2_A	RDN1_A	RDN3	U
V	USB_VRT	USB_DM		SRCLKENA0			DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVDD CPU	DVSS	DVSS	DVSS	DVSS	DVDD SRA	DVDD SRA	DVSS	DVSS	DVSS					RDP3_A	RDP2_A	RDP1_A		V
W	AVDD18_US	AVSS33_USB	AUD_DAT_	LCM_RST			DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVDD CPU	DVSS	DVDD LTE	DVDD LTE	DVDD LTE	DVDD LTE	DVDD LTE	DVDD LTE	DVDD LTE	DVDD LTE	DVDD LTE				CMDAT1	CMDAT0	FSOURCE_P	AVDD18_MI	W
Y	AUD_CLK_	AUD_DAT_	PWRAP_SPI0	PWRAP_SPI0			DVDD CORE	DVDD CORE	DVDD CORE	DVDD CORE	DVDD CORE	DVDD CORE	DVSS	DVDD CPU	DVSS	DVDD LTE	DVDD LTE	DVDD LTE	DVDD LTE	DVDD LTE	DVDD LTE	DVDD LTE	DVDD LTE	DVDD LTE			CMMCLK	CMMCLK1		SDA0	CMPCLK	Y
AA		PWRAP_INT			DSI_TE		DVSS	DVDD CORE	DVSS	DVDD CORE	DVSS	DVDD CORE	DVSS	DVDD CPU	DVSS	DVDD LTE	DVSS	DVDD LTE	DVSS	DVDD LTE	DVSS	DVDD LTE	DVSS	DVDD LTE				SCL2	DVDD18_IOL	SCL0		AA
AB	PWRAP_SPI0	PWRAP_SPI0		RFIC_MIPI1	RFIC_MIPI0		DVSS	DVDD CORE	DVSS	DVDD CORE	DVSS	DVDD CORE	DVSS	DVDD CPU	DVSS	DVDD LTE	DVSS	DVDD LTE	DVSS	DVDD LTE	DVSS	DVDD LTE	DVSS	DVDD LTE			SCL3	SDA2	DVDD18_EF	SDA1	SCL1	AB
AC	RTC32K_CK	SYSRSTB	RFIC_MIPI1	LTE_PAVM1			DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVDD CPU	DVSS	VLTE_SRAM	DVSS	DVSS	DVSS	VLTE_SRAM	DVSS	DVSS	DVSS	VLTE_SRAM			SDA3			SRCLKENA1	SRCLKENAI	AC
AD		RFIC_MIPI0	DVDD18_IO	LTE_PAVM0	BPI_BUS27																						PCM_RX	PCM_TX	PCM_SYNC	UTXD2		AD
AE	BPI_BUS1	BPI_BUS3			BPI_BUS24					LTEX26M_IN	AVSS18_MD		C2KX26M_IN	AVSS18_PLL													PCM_CLK	EINT1	URXD2	UTXD3	URXD3	AE
AF	BPI_BUS4	BPI_BUS21			BPI_BUS23															BPI_BUS16	BPI_BUS14	BPI_BUS12					EINT2	EINT0		EINT3	EINT4	AF
AG		BPI_BUS2	BPI_BUS26	BPI_BUS25	BPI_BUS22	AVSS18_MD	AVSS18_MD	AVSS18_MD	AVSS18_MD		AUXIN0	AUXIN1	C2K_RX1_BB	C2K_RX1_BB	AVSS18_PLL	AVDD18_PLL	RFIC0_BSI_E	RFIC0_BSI_CK	C2K_TXBPI	BPI_BUS15	BPI_BUS13	BPI_BUS9	KPROW2	KPCOL2	EINT11	EINT9	UTXD1			SPI_MO		AG
AH	LTE_TXBPI	BPI_BUS0	AVSS18_MD	RFIC_ET_N	RFIC_ET_P	AVSS18_MD	LTE_RX1_BBI	LTE_RX2_BB	AVSS18_MD	APC1	AUXIN2		C2K_RX1_BBI	C2K_RX2_BB	AVSS18_PLL			RFIC1_BSI_E	BPI_BUS19		BPI_BUS11	BPI_BUS8	KPROW0		EINT10	EINT8	URXD1	SPI_CS	SPI_CK	SPI_MI	DISP_PWM	AH
AJ	AVSS18_MD	AVSS18_MD	AVSS18_MD	AVSS18_MD	AVSS18_MD	AVSS18_MD	LTE_RX1_BBI	LTE_RX2_BB	AVSS18_MD	APC2			C2K_RX1_BBI	C2K_RX2_BB	AVSS18_PLL			RFIC1_TX_BSI	RFIC1_BSI_CK			BPI_BUS7	KPROW1			EINT7	URXD0	UTXD0	JTDI	JTCK	JTMS	AJ
AK	NC	LTE_TX_BBI	LTE_TX_BBI	LTE_TX_BBQ	AVSS18_MD	LTE_RX1_BB	LTE_RX2_BBI	LTE_RX2_BBI	AVSS18_MD	AVSS_REFN	AVDD18_AP	C2K_TX_BBQ	C2K_TX_BBI	C2K_TX_BBIP	AVSS18_PLL	RFIC0_BSI_D	RFIC0_BSI_D	RFIC1_TX_BSI	RFIC1_TX_BSI	BPI_BUS20	BPI_BUS18	BPI_BUS10	BPI_BUS6	KPCOL1	EINT12	I2S_BCK	I2S_DATA_I	JTDO	EINT6	TESTMODE		AK
AL	NC	NC	LTE_TX_BBQ	AVDD18_M	AVSS18_MD	LTE_RX1_BB		AVSS18_MD	AVDD28_DA	REFP		C2K_TX_BBQ		C2K_RX2_BBI	C2K_RX2_BBI		RFIC0_BSI_D	RFIC1_BSI_D		DVDD18_IOL	BPI_BUS17		BPI_BUS5	KPCOL0		DVDD18_IOL	I2S_LRCK		EINT5	NC	NC	AL
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	

Figure 2-1. Ball map view for LPDDR3

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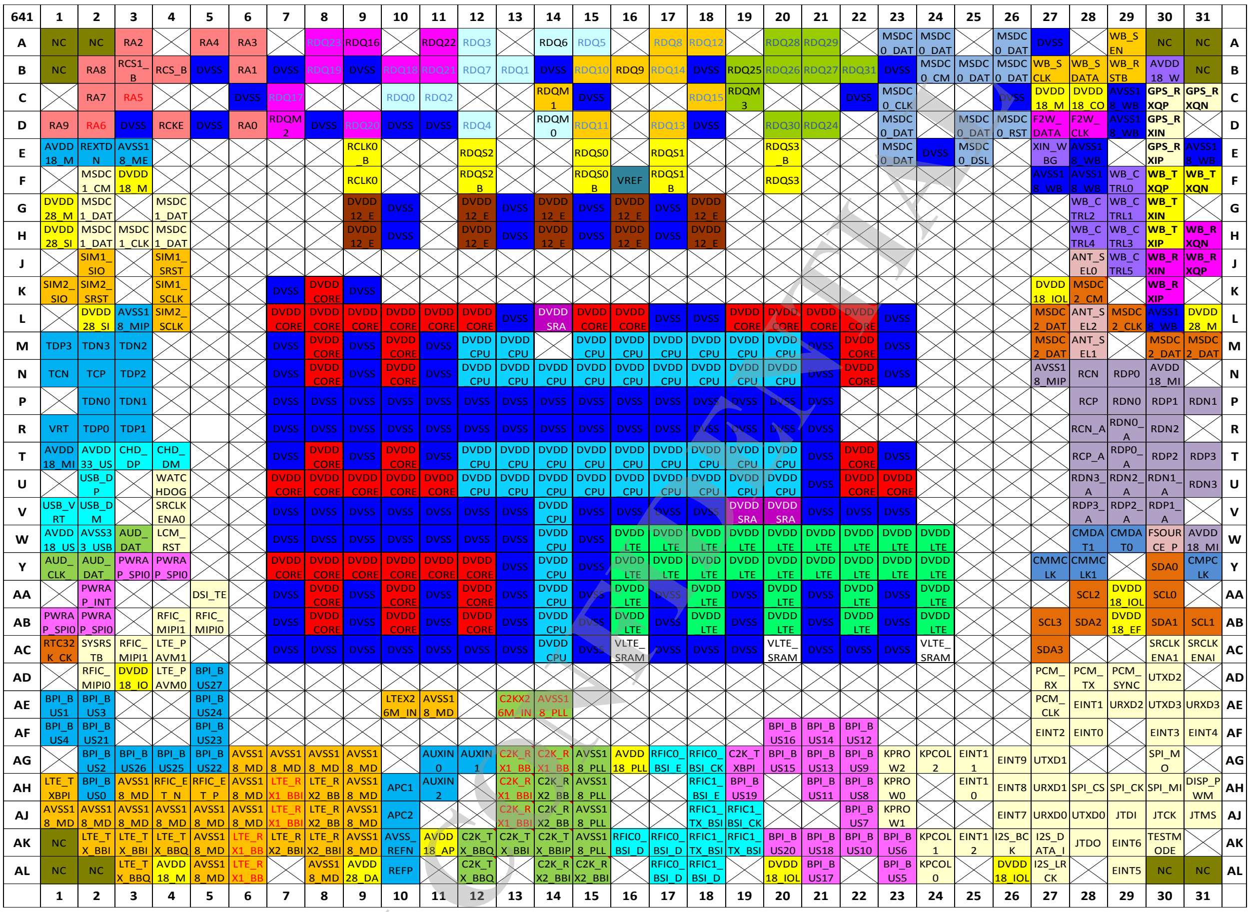

Figure 2-2. Ball map view for LPDDR2

2.1.2 Pin Coordinate

Table 2-1. Pin coordinate (using LPDDR3)

Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A1	NC	M23	DVSS	AA28	SCL2
A2	NC	M27	MSDC2_DAT0	AA29	DVDD18_IOLB
A3	RA2	M28	ANT_SEL1	AA30	SCL0
A5	RA4	M30	MSDC2_DAT3	AB1	PWRAP_SPI0_MI
A6	RA3	M31	MSDC2_DAT2	AB2	PWRAP_SPI0_MO
A8	RDQ17	N1	TCN	AB4	RFIC_MIPI1_SDATA
A9	RDQ16	N2	TCP	AB5	RFIC_MIPI0_SDATA
A11	RDQ22	N3	TDP2	AB7	DVSS
A12	RDQ0	N7	DVSS	AB8	DVDD_CORE

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A14	RDQ6	N8	DVDD_CORE	AB9	DVSS
A15	RDQ7	N9	DVSS	AB10	DVDD_CORE
A17	RDQ14	N10	DVDD_CORE	AB11	DVSS
A18	RDQ15	N11	DVSS	AB12	DVDD_CORE
A20	RDQ27	N12	DVDD_CPU	AB13	DVSS
A21	RDQ31	N13	DVDD_CPU	AB14	DVDD_CPU
A23	MSDC0_DAT4	N14	DVDD_CPU	AB15	DVSS
A24	MSDC0_DAT5	N15	DVDD_CPU	AB16	DVDD_LTE
A26	MSDC0_DAT0	N16	DVDD_CPU	AB17	DVSS
A27	DVSS	N17	DVDD_CPU	AB18	DVDD_LTE
A29	WB_SEN	N18	DVDD_CPU	AB19	DVSS
A30	NC	N19	DVDD_CPU	AB20	DVDD_LTE
A31	NC	N20	DVDD_CPU	AB21	DVSS
B1	NC	N21	DVSS	AB22	DVDD_LTE
B2	RA8	N22	DVDD_CORE	AB23	DVSS
B3	RCS1_B	N23	DVSS	AB24	DVDD_LTE
B4	RCS_B	N27	AVSS18_MIPIRX0	AB27	SCL3
B5	DVSS	N28	RCN	AB28	SDA2
B6	RA1	N29	RDP0	AB29	DVDD18_EFUSE
B7	DVSS	N30	AVDD18_MIPIRX0	AB30	SDA1
B8	RDQ18	P2	TDN0	AB31	SCL1
B9	DVSS	P3	TDN1	AC1	RTC32K_CK
B10	RDQ20	P7	DVSS	AC2	SYSRSTB
B11	RDQ19	P8	DVSS	AC3	RFIC_MIPI1_SCLK
B12	RDQ2	P9	DVSS	AC4	LTE_PAVM1
B13	RDQ4	P10	DVSS	AC7	DVSS
B14	DVSS	P11	DVSS	AC8	DVSS
B15	RDQ8	P12	DVSS	AC9	DVSS
B16	RDQ9	P13	DVSS	AC10	DVSS
B17	RDQ11	P14	DVSS	AC11	DVSS
B18	DVSS	P15	DVSS	AC12	DVSS
B19	RDQ25	P16	DVSS	AC13	DVSS
B20	RDQ28	P17	DVSS	AC14	DVDD_CPU
B21	RDQ30	P18	DVSS	AC15	DVSS
B22	RDQ29	P19	DVSS	AC16	VLTE_SRAM
B23	DVSS	P20	DVSS	AC17	DVSS

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
B24	MSDC0_CMD	P21	DVSS	AC18	DVSS
B25	MSDC0_DAT2	P28	RCP	AC19	DVSS
B26	MSDC0_DAT1	P29	RDN0	AC20	VLTE_SRAM
B27	WB_SCLK	P30	RDP1	AC21	DVSS
B28	WB_SDATA	P31	RDN1	AC22	DVSS
B29	WB_RSTB	R1	VRT	AC23	DVSS
B30	AVDD18_WBG	R2	TDP0	AC24	VLTE_SRAM
B31	NC	R3	TDP1	AC27	SDA3
C2	RA7	R7	DVSS	AC30	SRCLKENA1
C3	RA6	R8	DVSS	AC31	SRCLKENAI
C6	DVSS	R9	DVSS	AD2	RFIC_MIPI0_SCLK
C7	RDQ21	R10	DVSS	AD3	DVDD18_IORB
C10	RDQ1	R11	DVSS	AD4	LTE_PAVM0
C11	RDQ3	R12	DVSS	AD5	BPI_BUS27
C14	RDQM1	R13	DVSS	AD27	PCM_RX
C15	DVSS	R14	DVSS	AD28	PCM_TX
C18	RDQ13	R15	DVSS	AD29	PCM_SYNC
C19	RDQM3	R16	DVSS	AD30	UTXD2
C22	DVSS	R17	DVSS	AE1	BPI_BUS1
C23	MSDC0_CLK	R18	DVSS	AE2	BPI_BUS3
C26	DVSS	R19	DVSS	AE5	BPI_BUS24
C27	DVDD18_MC0	R20	DVSS	AE10	LTEX26M_IN
C28	DVDD18_CONN	R21	DVSS	AE11	AVSS18_MD
C29	AVSS18_WBG	R28	RCN_A	AE13	C2KX26M_IN
C30	GPS_RXQP	R29	RDN0_A	AE14	AVSS18_PLLGP
C31	GPS_RXQN	R30	RDN2	AE27	PCM_CLK
D1	RA9	T1	AVDD18_MIPITX	AE28	EINT1
D2	RA5	T2	AVDD33_USB	AE29	URXD2
D3	DVSS	T3	CHD_DP	AE30	UTXD3
D4	RCKE	T4	CHD_DM	AE31	URXD3
D5	DVSS	T7	DVSS	AF1	BPI_BUS4
D6	RA0	T8	DVDD_CORE	AF2	BPI_BUS21
D7	RDQM2	T9	DVSS	AF5	BPI_BUS23
D8	DVSS	T10	DVDD_CORE	AF20	BPI_BUS16
D9	RDQ23	T11	DVSS	AF21	BPI_BUS14
D10	DVSS	T12	DVDD_CPU	AF22	BPI_BUS12

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
D11	DVSS	T13	DVDD_CPU	AF27	EINT2
D12	RDQ5	T14	DVDD_CPU	AF28	EINT0
D14	RDQM0	T15	DVDD_CPU	AF30	EINT3
D15	RDQ10	T16	DVDD_CPU	AF31	EINT4
D17	RDQ12	T17	DVDD_CPU	AG2	BPI_BUS2
D18	DVSS	T18	DVDD_CPU	AG3	BPI_BUS26
D20	RDQ24	T19	DVDD_CPU	AG4	BPI_BUS25
D21	RDQ26	T20	DVDD_CPU	AG5	BPI_BUS22
D23	MSDC0_DAT6	T21	DVSS	AG6	AVSS18_MD
D25	MSDC0_DAT7	T22	DVDD_CORE	AG7	AVSS18_MD
D26	MSDC0_RSTB	T23	DVSS	AG8	AVSS18_MD
D27	F2W_DATA	T28	RCP_A	AG9	AVSS18_MD
D28	F2W_CLK	T29	RDP0_A	AG11	AUXIN0
D29	AVSS18_WBG	T30	RDP2	AG12	AUXIN1
D30	GPS_RXIN	T31	RDP3	AG13	C2K_RX1_BBQP
E1	AVDD18_MEMPL L	U2	USB_DP	AG14	C2K_RX1_BBQN
E2	REXTDN	U4	WATCHDOG	AG15	AVSS18_PLLGP
E3	AVSS18_MEMPLL	U7	DVDD_CORE	AG16	AVDD18_PLLGP
E9	RCLK0_B	U8	DVDD_CORE	AG17	RFIC0_BSI_EN
E12	RDQS2	U9	DVDD_CORE	AG18	RFIC0_BSI_CK
E15	RDQS0	U10	DVDD_CORE	AG19	C2K_TXBPI
E17	RDQS1	U11	DVDD_CORE	AG20	BPI_BUS15
E20	RDQS3_B	U12	DVDD_CPU	AG21	BPI_BUS13
E23	MSDC0_DAT3	U13	DVDD_CPU	AG22	BPI_BUS9
E24	DVSS	U14	DVDD_CPU	AG23	KPROW2
E25	MSDC0_DSL	U15	DVDD_CPU	AG24	KPCOL2
E27	XIN_WBG	U16	DVDD_CPU	AG25	EINT11
E28	AVSS18_WBG	U17	DVDD_CPU	AG26	EINT9
E30	GPS_RXIP	U18	DVDD_CPU	AG27	UTXD1
E31	AVSS18_WBG	U19	DVDD_CPU	AG30	SPI_MO
F2	MSDC1_CMD	U20	DVDD_CPU	AH1	LTE_TXBPI
F3	DVDD18_MC1	U21	DVSS	AH2	BPI_BUS0
F9	RCLK0	U22	DVDD_CORE	AH3	AVSS18_MD
F12	RDQS2_B	U23	DVDD_CORE	AH4	RFIC_ET_N
F15	RDQS0_B	U28	RDN3_A	AH5	RFIC_ET_P
F16	VREF	U29	RDN2_A	AH6	AVSS18_MD

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
F17	RDQS1_B	U30	RDN1_A	AH7	LTE_RX1_BBIP
F20	RDQS3	U31	RDN3	AH8	LTE_RX2_BBQN
F27	AVSS18_WBG	V1	USB_VRT	AH9	AVSS18_MD
F28	AVSS18_WBG	V2	USB_DM	AH10	APC1
F29	WB_CTRL0	V4	SRCLKENA0	AH11	AUXIN2
F30	WB_TXQP	V7	DVSS	AH13	C2K_RX1_BBIN
F31	WB_TXQN	V8	DVSS	AH14	C2K_RX2_BBQP
G1	DVDD28_MC1	V9	DVSS	AH15	AVSS18_PLLGP
G2	MSDC1_DAT3	V10	DVSS	AH18	RFIC1_BSI_EN
G4	MSDC1_DAT0	V11	DVSS	AH19	BPI_BUS19
G9	DVDD12_EMI	V12	DVSS	AH21	BPI_BUS11
G10	DVSS	V13	DVSS	AH22	BPI_BUS8
G12	DVDD12_EMI	V14	DVDD_CPU	AH23	KPROW0
G13	DVSS	V15	DVSS	AH25	EINT10
G14	DVDD12_EMI	V16	DVSS	AH26	EINT8
G15	DVSS	V17	DVSS	AH27	URXD1
G16	DVDD12_EMI	V18	DVSS	AH28	SPI_CS
G17	DVSS	V19	DVDD_SRAM	AH29	SPI_CK
G18	DVDD12_EMI	V20	DVDD_SRAM	AH30	SPI_MI
G28	WB_CTRL2	V21	DVSS	AH31	DISP_PWM
G29	WB_CTRL1	V22	DVSS	AJ1	AVSS18_MD
G30	WB_TXIN	V23	DVSS	AJ2	AVSS18_MD
H1	DVDD28_SIM1	V28	RDP3_A	AJ3	AVSS18_MD
H2	MSDC1_DAT2	V29	RDP2_A	AJ4	AVSS18_MD
H3	MSDC1_CLK	V30	RDP1_A	AJ5	AVSS18_MD
H4	MSDC1_DAT1	W1	AVDD18_USB	AJ6	AVSS18_MD
H9	DVDD12_EMI	W2	AVSS33_USB	AJ7	LTE_RX1_BBIN
H10	DVSS	W3	AUD_DAT_MISO	AJ8	LTE_RX2_BBQP
H12	DVDD12_EMI	W4	LCM_RST	AJ9	AVSS18_MD
H13	DVSS	W7	DVSS	AJ10	APC2
H14	DVDD12_EMI	W8	DVSS	AJ13	C2K_RX1_BBIP
H15	DVSS	W9	DVSS	AJ14	C2K_RX2_BBQN
H16	DVDD12_EMI	W10	DVSS	AJ15	AVSS18_PLLGP
H17	DVSS	W11	DVSS	AJ18	RFIC1_TX_BSI_D0
H18	DVDD12_EMI	W12	DVSS	AJ19	RFIC1_BSI_CK
H28	WB_CTRL4	W13	DVSS	AJ22	BPI_BUS7

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
H29	WB_CTRL3	W14	DVDD_CPU	AJ23	KPROW1
H30	WB_TXIP	W15	DVSS	AJ26	EINT7
H31	WB_RXQN	W16	DVDD_LTE	AJ27	URXD0
J2	SIM1_SIO	W17	DVDD_LTE	AJ28	UTXD0
J4	SIM1_SRST	W18	DVDD_LTE	AJ29	JTDI
J28	ANT_SEL0	W19	DVDD_LTE	AJ30	JTCK
J29	WB_CTRL5	W20	DVDD_LTE	AJ31	JTMS
J30	WB_RXIN	W21	DVDD_LTE	AK1	NC
J31	WB_RXQP	W22	DVDD_LTE	AK2	LTE_TX_BBIP
K1	SIM2_SIO	W23	DVDD_LTE	AK3	LTE_TX_BBIN
K2	SIM2_SRST	W24	DVDD_LTE	AK4	LTE_TX_BBQN
K4	SIM1_SCLK	W28	CMDAT1	AK5	AVSS18_MD
K7	DVSS	W29	CMDAT0	AK6	LTE_RX1_BBQP
K8	DVDD_CORE	W30	FSOURCE_P	AK7	LTE_RX2_BBIP
K9	DVSS	W31	AVDD18_MIPIRX1	AK8	LTE_RX2_BBIN
K27	DVDD18_IOLT	Y1	AUD_CLK_MOSI	AK9	AVSS18_MD
K28	MSDC2_CMD	Y2	AUD_DAT_MOSI	AK10	AVSS_REFN
K30	WB_RXIP	Y3	PWRAP_SPI0_CK	AK11	AVDD18_AP
L2	DVDD28_SIM2	Y4	PWRAP_SPI0_CSN	AK12	C2K_TX_BBQN
L3	AVSS18_MIPITX	Y7	DVDD_CORE	AK13	C2K_TX_BBIN
L4	SIM2_SCLK	Y8	DVDD_CORE	AK14	C2K_TX_BBIP
L7	DVDD_CORE	Y9	DVDD_CORE	AK15	AVSS18_PLLGP
L8	DVDD_CORE	Y10	DVDD_CORE	AK16	RFIC0_BSI_D2
L9	DVDD_CORE	Y11	DVDD_CORE	AK17	RFIC0_BSI_D0
L10	DVDD_CORE	Y12	DVDD_CORE	AK18	RFIC1_TX_BSI_CK
L11	DVDD_CORE	Y13	DVSS	AK19	RFIC1_TX_BSI_EN
L12	DVDD_CORE	Y14	DVDD_CPU	AK20	BPI_BUS20
L13	DVSS	Y15	DVSS	AK21	BPI_BUS18
L14	DVDD_SRAM	Y16	DVDD_LTE	AK22	BPI_BUS10
L15	DVDD_CORE	Y17	DVDD_LTE	AK23	BPI_BUS6
L16	DVDD_CORE	Y18	DVDD_LTE	AK24	KPCOL1
L17	DVSS	Y19	DVDD_LTE	AK25	EINT12
L18	DVSS	Y20	DVDD_LTE	AK26	I2S_BCK
L19	DVDD_CORE	Y21	DVDD_LTE	AK27	I2S_DATA_IN
L20	DVDD_CORE	Y22	DVDD_LTE	AK28	JTDO
L21	DVDD_CORE	Y23	DVDD_LTE	AK29	EINT6

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
L22	DVDD_CORE	Y24	DVDD_LTE	AK30	TESTMODE
L23	DVSS	Y27	CMMCLK	AL1	NC
L27	MSDC2_DAT1	Y28	CMMCLK1	AL2	NC
L28	ANT_SEL2	Y30	SDA0	AL3	LTE_TX_BBQP
L29	MSDC2_CLK	Y31	CMPCLK	AL4	AVDD18_MD
L30	AVSS18_WBG	AA2	PWRAP_INT	AL5	AVSS18_MD
L31	DVDD28_MC2	AA5	DSI_TE	AL6	LTE_RX1_BBQN
M1	TDP3	AA7	DVSS	AL8	AVSS18_MD
M2	TDN3	AA8	DVDD_CORE	AL9	AVDD28_DAC
M3	TDN2	AA9	DVSS	AL10	REFP
M7	DVSS	AA10	DVDD_CORE	AL12	C2K_TX_BBQP
M8	DVDD_CORE	AA11	DVSS	AL14	C2K_RX2_BBIN
M9	DVSS	AA12	DVDD_CORE	AL15	C2K_RX2_BBIP
M10	DVDD_CORE	AA13	DVSS	AL17	RFIC0_BSI_D1
M11	DVSS	AA14	DVDD_CPU	AL18	RFIC1_BSI_D0
M12	DVDD_CPU	AA15	DVSS	AL20	DVDD18_IOLB
M13	DVDD_CPU	AA16	DVDD_LTE	AL21	BPI_BUS17
M15	DVDD_CPU	AA17	DVSS	AL23	BPI_BUS5
M16	DVDD_CPU	AA18	DVDD_LTE	AL24	KPCOL0
M17	DVDD_CPU	AA19	DVSS	AL26	DVDD18_IOLB
M18	DVDD_CPU	AA20	DVDD_LTE	AL27	I2S_LRCK
M19	DVDD_CPU	AA21	DVSS	AL29	EINT5
M20	DVDD_CPU	AA22	DVDD_LTE	AL30	NC
M21	DVSS	AA23	DVSS	AL31	NC
M22	DVDD_CORE	AA24	DVDD_LTE		

2.1.3 Detailed Pin Description

Table 2-2. Acronym for pin type

Abbreviation	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-direction
DI	Digital input
DO	Digital output
DIO	Digital bi-direction
P	Power
G	Ground

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Table 2-3. Detailed pin description (using LPDDR3)

Pin name	Type	Description	Power domain
SYSTEM			
SYSRSTB	DI	System reset input	DVDD18_IORB
WATCHDOG	DO	Watchdog reset output	DVDD18_IORB
TESTMODE	DIO	Test mode	DVDD18_IOLB
RTC32K_CK	DIO	32K clock input	DVDD18_IORB
SRCLKENAI	DIO	26MHz co-clock enable input	DVDD18_IOLB
SRCLKENA0	DIO	26MHz co-clock enable output	DVDD18_IORB
SRCLKENA1	DIO	26MHz co-clock enable output	DVDD18_IOLB
PMIC			
PWRAP_SPI0_MO	DIO	PMIC SPI control interface	DVDD18_IORB
PWRAP_SPI0_MI	DIO	PMIC SPI control interface	DVDD18_IORB
PWRAP_SPI0_CSN	DIO	PMIC SPI control interface	DVDD18_IORB
PWRAP_SPI0_CK	DIO	PMIC SPI control interface	DVDD18_IORB
PWRAP_INT	DIO	PMIC SPI control interface	DVDD18_IORB
AUD_CLK_MOSI	DIO	PMIC audio input interface	DVDD18_IORB
AUD_DAT_MOSI	DIO	PMIC audio input interface	DVDD18_IORB
AUD_DAT_MISO	DIO	PMIC audio input interface	DVDD18_IORB
SIM			
SIM1_SIO	DIO	SIM1 data, PMIC interface	DVDD18_MC1
SIM1_SRST	DIO	SIM1 reset, PMIC interface	DVDD18_MC1
SIM1_SCLK	DIO	SIM1 clock, PMIC interface	DVDD18_MC1
SIM2_SIO	DIO	SIM2 data, PMIC interface	DVDD18_MC1
SIM2_SRST	DIO	SIM2 reset, PMIC interface	DVDD18_MC1
SIM2_SCLK	DIO	SIM2 clock, PMIC interface	DVDD18_MC1
JTAG			
JTCK	DIO	JTCK	DVDD18_IOLB
JTDO	DIO	JTDO	DVDD18_IOLB
JTDI	DIO	JTDI	DVDD18_IOLB
JTMS	DIO	JTMS	DVDD18_IOLB
LCD			
DISP_PWM	DIO	Display PWM output	DVDD18_IOLB
DSI_TE	DIO	Parallel display interface tearing effect	DVDD18_IORB
LCM_RST	DIO	Parallel display interface reset signal	DVDD18_IORB
I2S			
I2S_DATA_IN	DIO	I2S data input pin	DVDD18_IOLB
I2S_BCK	DIO	I2S clock	DVDD18_IOLB
I2S_LRCK	DIO	I2S word select	DVDD18_IOLB
PCM/I2S merge interface			
PCM_TX	DIO	PCM audio interface	DVDD18_IOLB
PCM_CLK	DIO	PCM audio interface	DVDD18_IOLB

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Pin name	Type	Description	Power domain
PCM_RX	DIO	PCM audio interface	DVDD18_IOLB
PCM_SYNC	DIO	PCM audio interface	DVDD18_IOLB
EINT			
EINT0	DIO	External interrupt 0	DVDD18_IOLB
EINT1	DIO	External interrupt 1	DVDD18_IOLB
EINT2	DIO	External interrupt 2	DVDD18_IOLB
EINT3	DIO	External interrupt 3	DVDD18_IOLB
EINT4	DIO	External interrupt 4	DVDD18_IOLB
EINT5	DIO	External interrupt 5	DVDD18_IOLB
EINT6	DIO	External interrupt 6	DVDD18_IOLB
EINT7	DIO	External interrupt 7	DVDD18_IOLB
EINT8	DIO	External interrupt 8	DVDD18_IOLB
EINT9	DIO	External interrupt 9	DVDD18_IOLB
EINT10	DIO	External interrupt 10	DVDD18_IOLB
EINT11	DIO	External interrupt 11	DVDD18_IOLB
EINT12	DIO	External interrupt 12	DVDD18_IOLB
UART			
URXD0	DIO	UART0 RX	DVDD18_IOLB
UTXD0	DIO	UART0 TX	DVDD18_IOLB
URXD1	DIO	UART1 RX	DVDD18_IOLB
UTXD1	DIO	UART1 TX	DVDD18_IOLB
URXD2	DIO	UART2 RX	DVDD18_IOLB
UTXD2	DIO	UART2 TX	DVDD18_IOLB
URXD3	DIO	UART3 RX	DVDD18_IOLB
UTXD3	DIO	UART3 TX	DVDD18_IOLB
SPI			
SPI_CS	DIO	SPI chip select	DVDD18_IOLB
SPI_MI	DIO	SPI data in	DVDD18_IOLB
SPI_MO	DIO	SPI data out	DVDD18_IOLB
SPI_CK	DIO	SPI clock	DVDD18_IOLB
BPI			
BPI_BUS0	DIO	BPI1 BUS0	DVDD18_IORB
BPI_BUS1	DIO	BPI1 BUS1	DVDD18_IORB
BPI_BUS2	DIO	BPI1 BUS2	DVDD18_IORB
BPI_BUS3	DIO	BPI1 BUS3	DVDD18_IORB
BPI_BUS4	DIO	BPI1 BUS4	DVDD18_IORB
BPI_BUS5	DIO	BPI1 BUS5	DVDD18_IOLB
BPI_BUS6	DIO	BPI1 BUS6	DVDD18_IOLB
BPI_BUS7	DIO	BPI1 BUS7	DVDD18_IOLB
BPI_BUS8	DIO	BPI1 BUS8	DVDD18_IOLB
BPI_BUS9	DIO	BPI1 BUS9	DVDD18_IOLB
BPI_BUS10	DIO	BPI1 BUS10	DVDD18_IOLB
BPI_BUS11	DIO	BPI1 BUS11	DVDD18_IOLB

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Pin name	Type	Description	Power domain
BPI_BUS12	DIO	BPI1 BUS12	DVDD18_IOLB
BPI_BUS13	DIO	BPI1 BUS13	DVDD18_IOLB
BPI_BUS14	DIO	BPI1 BUS14	DVDD18_IOLB
BPI_BUS15	DIO	BPI1 BUS15	DVDD18_IOLB
BPI_BUS16	DIO	BPI1 BUS16	DVDD18_IOLB
BPI_BUS17	DIO	BPI1 BUS17	DVDD18_IOLB
BPI_BUS18	DIO	BPI1 BUS18	DVDD18_IOLB
BPI_BUS19	DIO	BPI1 BUS19	DVDD18_IOLB
BPI_BUS20	DIO	BPI1 BUS20	DVDD18_IOLB
BPI_BUS21	DIO	BPI1 BUS21	DVDD18_IORB
BPI_BUS22	DIO	BPI1 BUS22	DVDD18_IORB
BPI_BUS23	DIO	BPI1 BUS23	DVDD18_IORB
BPI_BUS24	DIO	BPI1 BUS24	DVDD18_IORB
BPI_BUS25	DIO	BPI1 BUS25	DVDD18_IORB
BPI_BUS26	DIO	BPI1 BUS26	DVDD18_IORB
BPI_BUS27	DIO	BPI1 BUS27	DVDD18_IORB
ANT_SEL0	DIO	Antenna select 0	DVDD18_IOLT
ANT_SEL1	DIO	Antenna select 1	DVDD18_IOLT
ANT_SEL2	DIO	Antenna select 2	DVDD18_IOLT
VM			
LTE_PAVM1	DIO	PA mode selection	DVDD18_IORB
LTE_PAVM0	DIO	PA mode selection	DVDD18_IORB
BSI			
RFIC1_BSI_EN	DIO	RFIC1 BSI enable	DVDD18_IOLB
RFIC1_BSI_CK	DIO	RFIC1 BSI clock	DVDD18_IOLB
RFIC1_BSI_D0	DIO	RFIC1 BSI Data0	DVDD18_IOLB
RFIC1_TX_BSI_EN	DIO	RFIC1 TX BSI enable	DVDD18_IOLB
RFIC1_TX_BSI_CK	DIO	RFIC1 TX BSI clock	DVDD18_IOLB
RFIC1_TX_BSI_D0	DIO	RFIC1 TX BSI Data0	DVDD18_IOLB
RFIC0_BSI_EN	DIO	RFIC0 BSI enable	DVDD18_IOLB
RFIC0_BSI_CK	DIO	RFIC0 BSI clock	DVDD18_IOLB
RFIC0_BSI_D2	DIO	RFIC0 BSI Data2	DVDD18_IOLB
RFIC0_BSI_D1	DIO	RFIC0 BSI Data1	DVDD18_IOLB
RFIC0_BSI_D0	DIO	RFIC0 BSI Data0	DVDD18_IOLB
RFIC_MIPI1_SCLK	DIO	RFIC MIPI1 SCLK	DVDD18_IORB
RFIC_MIPI1_SDATA	DIO	RFIC MIPI1 SDATA	DVDD18_IORB
RFIC_MIPI0_SCLK	DIO	RFIC MIPI0 SCLK	DVDD18_IORB
RFIC_MIPI0_SDATA	DIO	RFIC MIPI0 SDATA	DVDD18_IORB
C2K_TXBPI	DIO	C2K TXBPI	DVDD18_IOLB
LTE_TXBPI	DIO	LTE TXBPI	DVDD18_IORB
MSDC0			

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Pin name	Type	Description	Power domain
MSDC0_DAT7	DIO	MSDC0 data7 pin	DVDD18_MC0
MSDC0_DAT6	DIO	MSDC0 data6 pin	DVDD18_MC0
MSDC0_DAT5	DIO	MSDC0 data5 pin	DVDD18_MC0
MSDC0_RSTB	DIO	MSDC0 reset output	DVDD18_MC0
MSDC0_DAT4	DIO	MSDC0 data4 pin	DVDD18_MC0
MSDC0_DAT2	DIO	MSDC0 data2 pin	DVDD18_MC0
MSDC0_DAT3	DIO	MSDC0 data3 pin	DVDD18_MC0
MSDC0_CMD	DIO	MSDC0 command pin	DVDD18_MC0
MSDC0_CLK	DIO	MSDC0 clock output	DVDD18_MC0
MSDC0_DAT1	DIO	MSDC0 data1 pin	DVDD18_MC0
MSDC0_DAT0	DIO	MSDC0 data0 pin	DVDD18_MC0
MSDC1			
MSDC1_CLK	DIO	MSDC1 clock output	DVDD28_MC1/DVDD18_MC1
MSDC1_CMD	DIO	MSDC1 command pin	DVDD28_MC1/DVDD18_MC1
MSDC1_DAT0	DIO	MSDC1 data0 pin	DVDD28_MC1/DVDD18_MC1
MSDC1_DAT1	DIO	MSDC1 data1 pin	DVDD28_MC1/DVDD18_MC1
MSDC1_DAT2	DIO	MSDC1 data2 pin	DVDD28_MC1/DVDD18_MC1
MSDC1_DAT3	DIO	MSDC1 data3 pin	DVDD28_MC1/DVDD18_MC1
MSDC2			
MSDC2_CLK	DIO	MSDC2 clock output	DVDD28_MC2/DVDD18_IOLT
MSDC2_CMD	DIO	MSDC2 command pin	DVDD28_MC2/DVDD18_IOLT
MSDC2_DAT0	DIO	MSDC2 data0 pin	DVDD28_MC2/DVDD18_IOLT
MSDC2_DAT1	DIO	MSDC2 data1 pin	DVDD28_MC2/DVDD18_IOLT
MSDC2_DAT2	DIO	MSDC2 data2 pin	DVDD28_MC2/DVDD18_IOLT
MSDC2_DAT3	DIO	MSDC2 data3 pin	DVDD28_MC2/DVDD18_IOLT
WiFi/BT/GPS			
WB_SDATA	DIO	WiFi/BT SPI control data	DVDD18_CONN
WB_SCLK	DIO	WiFi/BT SPI control clock	DVDD18_CONN
WB_SEN	DIO	WiFi/BT SPI control enable	DVDD18_CONN
WB_RSTB	DIO	WiFi/BT SPI control reset	DVDD18_CONN
F2W_CLK	DIO	FM clock	DVDD18_CONN
F2W_DATA	DIO	FM data	DVDD18_CONN
WB_CTRL0	DIO	Data bus 0	DVDD18_IOLT
WB_CTRL1	DIO	Data bus 1	DVDD18_IOLT
WB_CTRL2	DIO	Data bus 2	DVDD18_IOLT
WB_CTRL3	DIO	Data bus 3	DVDD18_IOLT
WB_CTRL4	DIO	Data bus 4	DVDD18_IOLT
WB_CTRL5	DIO	Data bus 5	DVDD18_IOLT
EFUSE			
FSOURCE_P	DIO	E-FUSE blowing power control	FSOURCE_P
EMI			
RCLK0	DIO	DRAM clock 0 output	DVDD12_EMI
RCLK0_B	DIO	DRAM clock 0 output #	DVDD12_EMI

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Pin name	Type	Description	Power domain
RCKE	DIO	DRAM command output CKE	DVDD12_EMI
RCS_B	DIO	DRAM chip select 0 #	DVDD12_EMI
RCS1_B	DIO	DRAM chip select 1 #	DVDD12_EMI
RA0	DIO	DRAM address output 0	DVDD12_EMI
RA1	DIO	DRAM address output 1	DVDD12_EMI
RA2	DIO	DRAM address output 2	DVDD12_EMI
RA3	DIO	DRAM address output 3	DVDD12_EMI
RA4	DIO	DRAM address output 4	DVDD12_EMI
RA5	DIO	DRAM address output 5	DVDD12_EMI
RA6	DIO	DRAM address output 6	DVDD12_EMI
RA7	DIO	DRAM address output 7	DVDD12_EMI
RA8	DIO	DRAM address output 8	DVDD12_EMI
RA9	DIO	DRAM address output 9	DVDD12_EMI
RDQM0	DIO	DRAM DQM 0	DVDD12_EMI
RDQM1	DIO	DRAM DQM 1	DVDD12_EMI
RDQM2	DIO	DRAM DQM 2	DVDD12_EMI
RDQM3	DIO	DRAM DQM 3	DVDD12_EMI
RDQS0	DIO	DRAM DQS 0	DVDD12_EMI
RDQS0_B	DIO	DRAM DQS 0 #	DVDD12_EMI
RDQS1	DIO	DRAM DQS 1	DVDD12_EMI
RDQS1_B	DIO	DRAM DQS 1 #	DVDD12_EMI
RDQS2	DIO	DRAM DQS 2	DVDD12_EMI
RDQS2_B	DIO	DRAM DQS 2 #	DVDD12_EMI
RDQS3	DIO	DRAM DQS 3	DVDD12_EMI
RDQS3_B	DIO	DRAM DQS 3 #	DVDD12_EMI
RDQ0	DIO	DRAM data pin 0	DVDD12_EMI
RDQ1	DIO	DRAM data pin 1	DVDD12_EMI
RDQ2	DIO	DRAM data pin 2	DVDD12_EMI
RDQ3	DIO	DRAM data pin 3	DVDD12_EMI
RDQ4	DIO	DRAM data pin 4	DVDD12_EMI
RDQ5	DIO	DRAM data pin 5	DVDD12_EMI
RDQ6	DIO	DRAM data pin 6	DVDD12_EMI
RDQ7	DIO	DRAM data pin 7	DVDD12_EMI
RDQ8	DIO	DRAM data pin 8	DVDD12_EMI
RDQ9	DIO	DRAM data pin 9	DVDD12_EMI
RDQ10	DIO	DRAM data pin 10	DVDD12_EMI
RDQ11	DIO	DRAM data pin 11	DVDD12_EMI
RDQ12	DIO	DRAM data pin 12	DVDD12_EMI
RDQ13	DIO	DRAM data pin 13	DVDD12_EMI
RDQ14	DIO	DRAM data pin 14	DVDD12_EMI
RDQ15	DIO	DRAM data pin 15	DVDD12_EMI
RDQ16	DIO	DRAM data pin 16	DVDD12_EMI
RDQ17	DIO	DRAM data pin 17	DVDD12_EMI

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Pin name	Type	Description	Power domain
RDQ18	DIO	DRAM data pin 18	DVDD12_EMI
RDQ19	DIO	DRAM data pin 19	DVDD12_EMI
RDQ20	DIO	DRAM data pin 20	DVDD12_EMI
RDQ21	DIO	DRAM data pin 21	DVDD12_EMI
RDQ22	DIO	DRAM data pin 22	DVDD12_EMI
RDQ23	DIO	DRAM data pin 23	DVDD12_EMI
RDQ24	DIO	DRAM data pin 24	DVDD12_EMI
RDQ25	DIO	DRAM data pin 25	DVDD12_EMI
RDQ26	DIO	DRAM data pin 26	DVDD12_EMI
RDQ27	DIO	DRAM data pin 27	DVDD12_EMI
RDQ28	DIO	DRAM data pin 28	DVDD12_EMI
RDQ29	DIO	DRAM data pin 29	DVDD12_EMI
RDQ30	DIO	DRAM data pin 30	DVDD12_EMI
RDQ31	DIO	DRAM data pin 31	DVDD12_EMI
REXTDN	DIO	DRAM REXTDN pin	DVDD12_EMI
VREF	DIO		DVDD12_EMI
CAM			
CMPCLK	DIO	Pixel clock from sensor	DVDD18_IOLB
CMMCLK	DIO	Master clock to sensor	DVDD18_IOLB
CMMCLK1	DIO	Master clock1 to sensor	DVDD18_IOLB
CMDAT0	DIO	CAM sensor Data0	DVDD18_IOLB
CMDAT1	DIO	CAM sensor Data1	DVDD18_IOLB
I2C0			
SCL0	DIO	I2C0 clock	DVDD18_IOLB
SDA0	DIO	I2C0 data	DVDD18_IOLB
I2C1			
SCL1	DIO	I2C1 clock	DVDD18_IOLB
SDA1	DIO	I2C1 data	DVDD18_IOLB
I2C2			
SCL2	DIO	I2C2 clock	DVDD18_IOLB
SDA2	DIO	I2C2 data	DVDD18_IOLB
I2C3			
SCL3	DIO	I2C3 clock	DVDD18_IOLB
SDA3	DIO	I2C3 data	DVDD18_IOLB
ABB			
C2K_RX2_BBQP	AIO	C2K downlink QP for diversity path	AVDD18_MD
C2K_RX2_BBQN	AIO	C2K downlink QN for diversity path	AVDD18_MD
C2K_RX2_BBIN	AIO	C2K downlink IN for diversity path	AVDD18_MD
C2K_RX2_BBIP	AIO	C2K downlink IPP for diversity path	AVDD18_MD
C2K_RX1_BBQP	AIO	C2K downlink QP for main path	AVDD18_MD
C2K_RX1_BBQN	AIO	C2K downlink QN for main path	AVDD18_MD
C2K_RX1_BBIN	AIO	C2K downlink IN for main path	AVDD18_MD
C2K_RX1_BBIP	AIO	C2K downlink IPP for main path	AVDD18_MD

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Pin name	Type	Description	Power domain
C2K_TX_BBQP	AIO	C2K uplink QP	AVDD18_MD
C2K_TX_BBQN	AIO	C2K uplink QN	AVDD18_MD
C2K_TX_BBIN	AIO	C2K uplink IN	AVDD18_MD
C2K_TX_BBIP	AIO	C2K uplink IP	AVDD18_MD
C2KX26M_IN	AIO	26MHz clock input for 2nd modem	AVDD18_MD
AUXIN0	AIO	AuxADC external input channel 0	AVDD18_AP
AUXIN1	AIO	AuxADC external input channel 1	AVDD18_AP
AUXIN2	AIO	AuxADC external input channel 2	AVDD18_AP
REFP	AIO	Positive reference port for internal circuit	AVDD18_AP
APC1	AIO	Automatic power control for MD1	AVDD28_DAC
APC2	AIO	Automatic power control for MD2	AVDD28_DAC
LTEX26M_IN	AIO	26MHz clock input for AP & 1st modem	AVDD18_MD
LTE_RX2_BBQP	AIO	LTE downlink QP for diversity path	AVDD18_MD
LTE_RX2_BBQN	AIO	LTE downlink QN for diversity path	AVDD18_MD
LTE_RX2_BBIN	AIO	LTE downlink IN for diversity path	AVDD18_MD
LTE_RX2_BBIP	AIO	LTE downlink IPP for diversity path	AVDD18_MD
LTE_RX1_BBQP	AIO	LTE downlink QP for main path	AVDD18_MD
LTE_RX1_BBQN	AIO	LTE downlink QN for main path	AVDD18_MD
LTE_RX1_BBIN	AIO	LTE downlink IN for main path	AVDD18_MD
LTE_RX1_BBIP	AIO	LTE downlink IP for main path	AVDD18_MD
LTE_TX_BBQP	AIO	LTE uplink QP	AVDD18_MD
LTE_TX_BBQN	AIO	LTE uplink QN	AVDD18_MD
LTE_TX_BBIN	AIO	LTE uplink IN	AVDD18_MD
LTE_TX_BBIP	AIO	LTE uplink IP	AVDD18_MD
RFIC_ET_N	AIO	Envelop Tracking DAC output N	AVDD18_MD
RFIC_ET_P	AIO	Envelop Tracking DAC output P	AVDD18_MD
WBG			
XIN_WBG	AIO	WIFI/BT clock source	AVDD18_WBG
GPS_RXQN	AIO	RXQN for GPS RX	AVDD18_WBG
GPS_RXQP	AIO	RXQP for GPS RX	AVDD18_WBG
GPS_RXIN	AIO	RXIN for GPS RX	AVDD18_WBG
GPS_RXIP	AIO	RXIP for GPS RX	AVDD18_WBG
WB_TXQN	AIO	TXQN for WIFI/BT TX	AVDD18_WBG
WB_TXQP	AIO	TXQP for WIFI/BT TX	AVDD18_WBG
WB_TXIN	AIO	TXIN for WIFI/BT TX	AVDD18_WBG
WB_TXIP	AIO	TXIP for WIFI/BT TX	AVDD18_WBG
WB_RXQN	AIO	RXQN for WIFI/BT RX	AVDD18_WBG
WB_RXQP	AIO	RXQP for WIFI/BT RX	AVDD18_WBG
WB_RXIN	AIO	RXIN for WIFI/BT RX	AVDD18_WBG
WB_RXIP	AIO	RXIP for WIFI/BT RX	AVDD18_WBG
MIPI			

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Pin name	Type	Description	Power domain
TDN3	AIO	DSI0 lane3 N	DVDD18_MIPITX
TDP3	AIO	DSI0 lane3 P	DVDD18_MIPITX
TDN2	AIO	DSI0 lane2 N	DVDD18_MIPITX
TDP2	AIO	DSI0 lane2 P	DVDD18_MIPITX
TCN	AIO	DSI0 CK lane N	DVDD18_MIPITX
TCP	AIO	DSI0 CK lane P	DVDD18_MIPITX
TDN1	AIO	DSI0 lane1 N	DVDD18_MIPITX
TDP1	AIO	DSI0 lane1 P	DVDD18_MIPITX
TDN0	AIO	DSI0 lane0 N	DVDD18_MIPITX
TDP0	AIO	DSI0 lane0 P	DVDD18_MIPITX
VRT	AO	External resistor for DSI bias Connect 1.5K ohm 1% resistor to ground	DVDD18_MIPITX
RDN3	AIO	CSI0 lane3 N	DVDD18_MIPIRX0
RDP3	AIO	CSI0 lane3 P	DVDD18_MIPIRX0
RDN2	AIO	CSI0 lane2 N	DVDD18_MIPIRX0
RDP2	AIO	CSI0 lane2 P	DVDD18_MIPIRX0
RCN	AIO	CSI0 CK lane N	DVDD18_MIPIRX0
RCP	AIO	CSI0 CK lane P	DVDD18_MIPIRX0
RDN1	AIO	CSI0 lane1 N	DVDD18_MIPIRX0
RDP1	AIO	CSI0 lane1 P	DVDD18_MIPIRX0
RDN0	AIO	CSI0 lane0 N	DVDD18_MIPIRX0
RDP0	AIO	CSI0 lane0 P	DVDD18_MIPIRX0
RDN1_A	AIO	CSI1 lane1 N	DVDD18_MIPIRX1
RDP1_A	AIO	CSI1 lane1 P	DVDD18_MIPIRX1
RCN_A	AIO	CSI1 CK lane N	DVDD18_MIPIRX1
RCP_A	AIO	CSI1 CK lane P	DVDD18_MIPIRX1
RDN0_A	AIO	CSI1 lane0 N	DVDD18_MIPIRX1
RDP0_A	AIO	CSI1 lane0 P	DVDD18_MIPIRX1
RDN2_A	AIO	CSI1 lane 2 N	DVDD18_MIPIRX1
RDP2_A	AIO	CSI1 lane 2 P	DVDD18_MIPIRX1
RDN3_A	AIO	CSI1 lane 3 N	DVDD18_MIPIRX1
RDP3_A	AIO	CSI1 lane 3 P	DVDD18_MIPIRX1
USB			
USB_DP	AIO	USB porto D+ differential data line	AVDD33_USB
USB_DM	AIO	USB porto D- differential data line	AVDD33_USB
CHD_DP	AIO	BC1.1 Charger DP	AVDD33_USB
CHD_DM	AIO	BC1.1 Charger DM	AVDD33_USB
USB_VRT	AO	USB output for bias current; connect with 5.11K 1% Ohm to GND	AVDD18_USB
Keypad			
KPROW0	AIO	Keypad row 0	DVDD18_IOLB
KPROW1	AIO	Keypad row 1	DVDD18_IOLB
KPROW2	AIO	Keypad row 2	DVDD18_IOLB

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Pin name	Type	Description	Power domain
KPCOL0	AIO	Keypad column 0	DVDD18_IOLB
KPCOL1	AIO	Keypad column 1	DVDD18_IOLB
KPCOL2	AIO	Keypad column 2	DVDD18_IOLB
Analog power			
DVDD18_PLLGP	P	Analog power input 1.8V for PLL	
AVDD18_AP	P	Analog power input 1.8V for AuxADC, TSENSE	
AVDD18_MD	P	Analog power input 1.8V for BBTX, BBRX, 2GBBTX	
AVDD18_MEMPLL	P	Analog power for MEMPLL	
AVDD18_USB	P	Analog power 1.8V for USB	
AVDD18_WBG	P	Analog power 1.8V for WiFi/BT/GPS	
DVDD18_MIPITX	P	Analog power for MIPI DSI	
DVDD18_MIPIRX0	P	Analog power for MIPI CSI	
DVDD18_MIPIRX1	P	Analog power for MIPI CSI	
AVDD28_DAC	P	Analog power input 2.8V for APC	
AVDD33_USB	P	Analog power 3.3V for USB port 1	
Digital power			
DVDD18_IOLT	P	Digital power input for IO	-
DVDD18_IOLB	P	Digital power input for IO	-
DVDD18_IORB	P	Digital power input for IO	-
DVDD18_CONN	P	Digital power input for IO	-
EVDD18_EFUSE	P	Digital power input for efuse IO	-
DVDD18_MC0	P	Digital power input for MSDC0 IO	-
DVDD18_MC1	P	Digital power input for MSDC1 IO	-
DVDD18_MC2	P	Digital power input for MSDC2 IO	-
DVDD28_MC1	P	Digital power input for 1.8/3.3V MSDC IO	-
DVDD28_MC2	P	Digital power input for 1.8/3.3V MSDC IO	-
DVDD12_EMI	P	Digital power input for 1.2V EMI	-
DVDD_TOP	P	Digital power input for core	-
DVDD_LTE	P	Digital power input for LTE	-
VLTE_SRAM	P	Digital power input for LTE SRAM	-
DVDD_CPU	P	Digital power input for processor	-
DVDD_SRAM	P	Digital power input for processor SRAM	-
Analog ground			
AVSS18_AP	G	Analog ground	
AVSS18_MD	G	Analog ground	
AVSS18_MEMPLL	G	Analog ground	
AVSS18_WBG	G	Analog ground	
AVSS_REFN	G	Analog ground	
AVSS33_USB	G	Analog ground	
DVSS18_MIPITX	G	Analog ground	

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Pin name	Type	Description	Power domain
DVSS18_MIPIRX0	G	Analog ground	
DVSS18_MIPIRX1	G	Analog ground	
AVSS33_USB	G	Analog ground	
Digital ground			
DVSS	G	Digital ground	-

Table 2-4. Acronym for the table of state of pins

Abbreviation	Description
I	Input
LO	Low output
HO	High output
XO	Low or high output
PU	Pull-up
PD	Pull-dowm
-	No PU/PD
0~N	Aux. function number
X	Delicate function pin

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Table 2-5. State of pins

Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
eMMC Interface						
MSDC0_CLK	LO	1	-	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_CMD	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DAT0	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DAT1	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DAT2	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DAT3	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DAT4	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DAT5	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DAT6	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DAT7	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_RSTB	HO	1	-	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DSL	I	1	PD	DIOH4,DIOL4	No Need	IO Type 4
SD Card Interface						
MSDC1_CLK	LO	1	-	DIOH6,DIOL6	No Need	IO Type 6
MSDC1_CMD	I	1	PU	DIOH6,DIOL6	No Need	IO Type 6
MSDC1_DAT0	I	1	PU	DIOH6,DIOL6	No Need	IO Type 6
MSDC1_DAT1	I	1	PU	DIOH6,DIOL6	No Need	IO Type 6
MSDC1_DAT2	I	1	PU	DIOH6,DIOL6	No Need	IO Type 6
MSDC1_DAT3	I	1	PU	DIOH6,DIOL6	No Need	IO Type 6
SIM Interface						
SIM1_SCLK	I	0	PD	DIOH7,DIOL7	No Need	IO Type 7
SIM1_SRST	I	0	PD	DIOH7,DIOL7	No Need	IO Type 7
SIM1_SIO	I	0	PD	DIOH7,DIOL7	No Need	IO Type 7
SIM2_SCLK	I	0	PD	DIOH7,DIOL7	No Need	IO Type 7
SIM2_SRST	I	0	PD	DIOH7,DIOL7	No Need	IO Type 7
SIM2_SIO	I	0	PD	DIOH7,DIOL7	No Need	IO Type 7
Audio Interface						
AUD_CLK_MOSI	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
AUD_DAT_MISO	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
AUD_DAT_MOSI	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
LCD Control						
DISP_PWM	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
LCM_RST	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
DSI_TE	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
CAM Interface						
CMPCLK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
CMMCLK	I	0	PD	DIOH4,DIOL4	No Need	IO Type 4
CMMCLK1	I	0	PD	DIOH4,DIOL4	No Need	IO Type 4
CMPDAT0	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
CMPDAT1	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1

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[1] The column "State" of "Reset" shows the pin state during reset (Input, High Output, Low Output, etc).
[2] The column "Aux" for "Reset" means the default aux. funtion number shown in Table "Pin Multiplexing, Capability and Settings".
[3] The column "PU/PD" for "Reset" means if there is internal pull-up or pull-down when the pin is input in the reset state.

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Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
PMIC SPI Interface						
PWRAP_SPI0_CK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
PWRAP_SPI0_CSN	I	0	PU	DIOH1,DIOL1	No Need	IO Type 1
PWRAP_SPI0_MI	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
PWRAP_SPI0_MO	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2C Interface						
SCL0	I	1	-	DIOH3,DIOL3	No Need	IO Type 3
SCL1	I	1	-	DIOH3,DIOL3	No Need	IO Type 3
SCL2	I	1	-	DIOH3,DIOL3	No Need	IO Type 3
SCL3	I	1	-	DIOH3,DIOL3	No Need	IO Type 3
SDA0	I	1	-	DIOH3,DIOL3	No Need	IO Type 3
SDA1	I	1	-	DIOH3,DIOL3	No Need	IO Type 3
SDA2	I	1	-	DIOH1,DIOL1	No Need	IO Type 1
SDA3	I	1	-	DIOH3,DIOL3	No Need	IO Type 3
RFIC Interface						
RFIC0_BSI_EN	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC0_BSI_CK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC0_BSI_D0	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC0_BSI_D1	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC0_BSI_D2	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC1_BSI_EN	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC1_BSI_CK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC1_BSI_D0	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC1_TX_BSI_EN	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC1_TX_BSI_CK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC1_TX_BSI_D0	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC_MIPI1_SCLK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC_MIPI1_SDATA	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC_MIPI0_SCLK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC_MIPI0_SDATA	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI Interface						
BPI_BUS0	I	0	PD	DIOH6,DIOL6	No Need	IO Type 6
BPI_BUS1	I	0	PD	DIOH6,DIOL6	No Need	IO Type 6
BPI_BUS2	I	0	PD	DIOH6,DIOL6	No Need	IO Type 6
BPI_BUS3	I	0	PD	DIOH6,DIOL6	No Need	IO Type 6
BPI_BUS4	I	0	PD	DIOH6,DIOL6	No Need	IO Type 6
BPI_BUS5	I	0	PD	DIOH6,DIOL6	No Need	IO Type 6
BPI_BUS6	I	0	PD	DIOH5,DIOL5	No Need	IO Type 5
BPI_BUS7	I	0	PD	DIOH5,DIOL5	No Need	IO Type 5
BPI_BUS8	I	0	PD	DIOH5,DIOL5	No Need	IO Type 5
BPI_BUS9	I	0	PD	DIOH5,DIOL5	No Need	IO Type 5
BPI_BUS10	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS11	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS12	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS13	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS14	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS15	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS16	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS17	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS18	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1

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Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
BPI_BUS19	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS20	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS21	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS22	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS23	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS24	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS25	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS26	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS27	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
LTE_TXBPI	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
C2K_TXBPI	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
Connectivity RF Interface						
WB_CTRL0	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
WB_CTRL1	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
WB_CTRL2	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
WB_CTRL3	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
WB_CTRL4	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
WB_CTRL5	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
F2W_DATA	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
F2W_CLK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
WB_SCLK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
WB_SDATA	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
WB_SEN	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
WB_RSTB	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
Keypad						
KPCOL0	I	1	PU	DIOH1,DIOL1	No Need	IO Type 1
KPCOL1	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
KPCOL2	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
KPROW0	LO	1	PD	DIOH1,DIOL1	No Need	IO Type 1
KPROW1	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
KPROW2	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
DPI Interface						
DPI_D0	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D1	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D2	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D3	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D4	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D5	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D6	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D7	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D8	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D9	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D10	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D11	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_DE	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_CK	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_HSYNC	I	0	PU	DIOH2,DIOL2	No Need	IO Type 2
DPI_VSYNC	I	0	PU	DIOH2,DIOL2	No Need	IO Type 2
I2S Interface						

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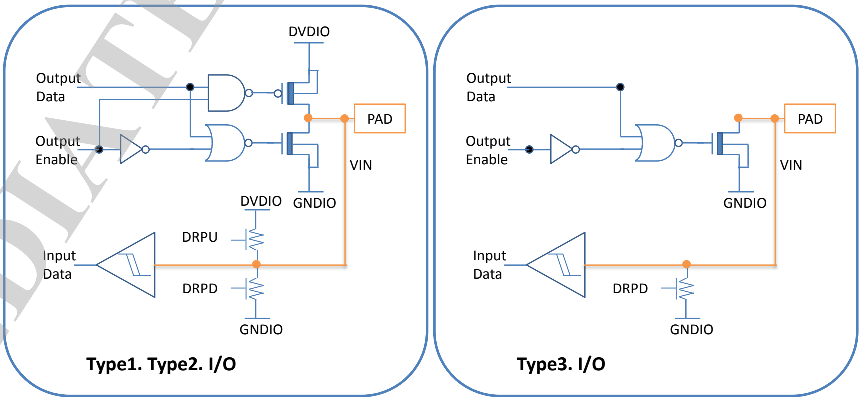
Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
I2S0_MCK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S0_BCK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S0_LRCK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S0_DI	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S1_MCK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S1_BCK	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
I2S1_LRCK	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
I2S1_DO	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
I2S2_MCK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S2_BCK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S2_LRCK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S2_DI	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S3_MCK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S3_BCK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S3_LRCK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S3_DO	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
SPI Interface						
SPI_CSB	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
SPI_CLK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
SPI_MO	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
SPI_MI	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
System /Reset Clock Enable						
WATCHDOG	HO	1	-	DIOH1,DIOL1	No Need	IO Type 1
SRCLKENA0	HO	1	-	DIOH1,DIOL1	No Need	IO Type 1
SRCLKENA1	LO	1	-	DIOH1,DIOL1	No Need	IO Type 1
SRCLKENAI	I	1	PD	DIOH1,DIOL1	No Need	IO Type 1
IDDIG	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
USB_DRVBUS	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1



Type1. Type2. I/O

Type3. I/O

Type1. GPIO 28 type
(2mA, 4mA, 6mA, 8mA)
Type2. GPIO 4G type
(4mA, 8mA, 12mA, 16mA)

Type 3. Open-drain IO

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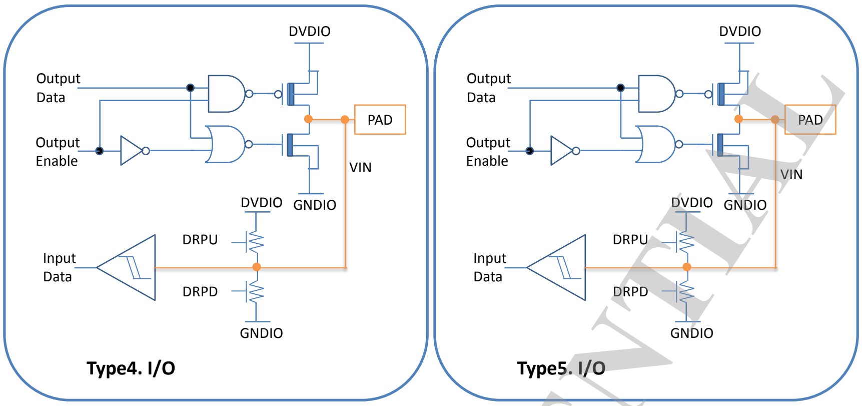
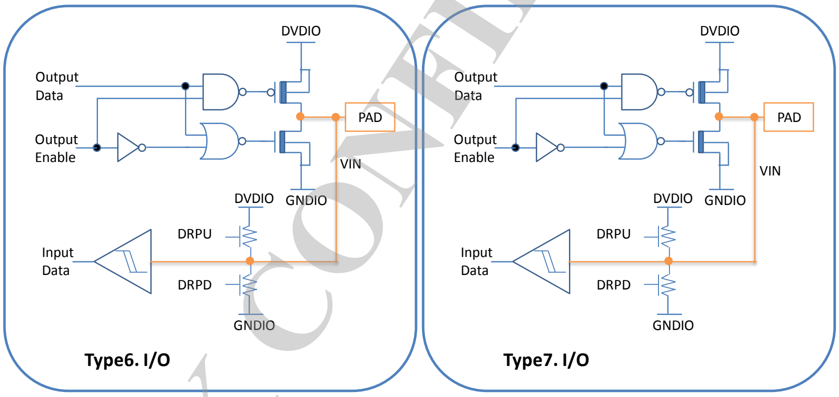


Type4. MSDC 1.8V I/O
(2mA, 4mA, 6mA, 8mA,
10mA, 12mA, 14mA, 16mA)

Type5. 3.3v GPIO
(4mA, 8mA, 12mA, 16mA)



Type6. MSDC 3.3V I/O
(2mA, 4mA, 6mA, 8mA,
10mA, 12mA, 14mA, 16mA)

Type7. 3.3v SIM I/O
(4mA, 8mA, 12mA, 16mA)

Figure 2-3. IO types in state of pins

2.1.4 Pin Multiplexing, Capability and Settings

Table 2-6. Acronym for pull-up and pull-down type

Abbreviation	Description
PU	Pull-up, not controllable
PD	Pull-down, not controllable
CU	Pull-up, controllable
CD	Pull-down, controllable
X	Cannot pull-up or pull-dowm

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Table 2-7. Pin multiplexing, capability and settings

Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
MSDC0_CLK	0	GPIO174	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_CLK	O	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_CMD	0	GPIO172	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_CMD	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DAT0	0	GPIO175	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DAT0	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DAT1	0	GPIO176	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DAT1	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DAT2	0	GPIO177	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DAT2	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DAT3	0	GPIO178	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DAT3	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DAT4	0	GPIO179	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DAT4	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DAT5	0	GPIO180	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DAT5	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DAT6	0	GPIO181	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DAT6	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DAT7	0	GPIO182	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DAT7	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_RSTB	0	GPIO183	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_RSTB	O	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DSL	0	GPIO173	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DSL	I	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC1_CLK	0	GPIO167	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC1_CLK	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	2	LTE_MD32_JTAG_TCK	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	3	C2K_TCK	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	4	TDD_TCK	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	5	CONN_DSP_JCK	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	6	JTCK	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	CONN_MCU_AICE_TCKC	I	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC1_CMD	0	GPIO166	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC1_CMD	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	2	LTE_MD32_JTAG_TMS	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	3	C2K_TMS	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	4	TDD_TMS	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	5	CONN_DSP_JMS	I	CU, CD	2/4/6/8/10/12/14/16mA	0

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Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
	6	JTMS	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	CONN_MCU_AICE_TMSC	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC1_DAT0	0	GPIO168	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC1_DAT0	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	2	LTE_MD32_JTAG_TDI	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	3	C2K_TDI	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	4	TDD_TDI	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	5	CONN_DSP_JDI	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	6	JTDI	I	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC1_DAT1	0	GPIO169	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC1_DAT1	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	2	LTE_MD32_JTAG_TDO	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	3	C2K_TDO	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	4	TDD_TDO	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	5	CONN_DSP_JDO	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	6	JTDO	O	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC1_DAT2	0	GPIO170	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC1_DAT2	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	2	LTE_MD32_JTAG_TRST	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	3	C2K_NTRST	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	4	TDD_TRSTN	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	5	CONN_DSP_JINTP	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	6	DM_JTINTP	O	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC1_DAT3	0	GPIO171	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC1_DAT3	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	3	C2K_RTCK	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	6	TDD_TXD	O	CU, CD	2/4/6/8/10/12/14/16mA	0
SIM1_SCLK	0	GPIO18	IO	CU, CD	4/8/12/16mA	0
	1	MD1_SIM1_SCLK	O	CU, CD	4/8/12/16mA	0
	2	MD2_SIM1_SCLK	O	CU, CD	4/8/12/16mA	0
	3	MD1_SIM2_SCLK	O	CU, CD	4/8/12/16mA	0
	4	MD2_SIM2_SCLK	O	CU, CD	4/8/12/16mA	0
SIM1_SRST	0	GPIO164	IO	CU, CD	4/8/12/16mA	0
	1	MD_SIM1_SRST	O	CU, CD	4/8/12/16mA	0
	2	MD_SIM2_SRST	O	CU, CD	4/8/12/16mA	0
	3	UIM1_RST	O	CU, CD	4/8/12/16mA	0
	4	UIM0_RST	O	CU, CD	4/8/12/16mA	0
SIM1_SIO	0	GPIO165	IO	CU, CD	4/8/12/16mA	0
	1	MD_SIM1_SDAT	IO	CU, CD	4/8/12/16mA	0

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Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
	2	MD_SIM2_SDAT	IO	CU, CD	4/8/12/16mA	0
	3	UIM1_IO	IO	CU, CD	4/8/12/16mA	0
	4	UIM0_IO	IO	CU, CD	4/8/12/16mA	0
SIM2_SCLK	0	GPIO160	IO	CU, CD	4/8/12/16mA	0
	1	MD_SIM2_SCLK	O	CU, CD	4/8/12/16mA	0
	2	MD_SIM1_SCLK	O	CU, CD	4/8/12/16mA	0
	3	UIM0_CLK	O	CU, CD	4/8/12/16mA	0
	4	UIM1_CLK	O	CU, CD	4/8/12/16mA	0
SIM2_SRST	0	GPIO161	IO	CU, CD	4/8/12/16mA	0
	1	MD_SIM2_SRST	O	CU, CD	4/8/12/16mA	0
	2	MD_SIM1_SRST	O	CU, CD	4/8/12/16mA	0
	3	UIM0_RST	O	CU, CD	4/8/12/16mA	0
	4	UIM1_RST	O	CU, CD	4/8/12/16mA	0
SIM2_SIO	0	GPIO162	IO	CU, CD	4/8/12/16mA	0
	1	MD_SIM2_SDAT	IO	CU, CD	4/8/12/16mA	0
	2	MD_SIM1_SDAT	IO	CU, CD	4/8/12/16mA	0
	3	UIM0_IO	IO	CU, CD	4/8/12/16mA	0
	4	UIM1_IO	IO	CU, CD	4/8/12/16mA	0
AUD_CLK_MOSI	0	GPIO143	IO	CU, CD	2/4/6/8mA	0
	1	AUD_CLK_MOSI	O	CU, CD	2/4/6/8mA	0
AUD_DAT_MISO	0	GPIO144	IO	CU, CD	2/4/6/8mA	0
	1	AUD_DAT_MISO	I	CU, CD	2/4/6/8mA	0
	3	AUD_DAT_MOSI	O	CU, CD	2/4/6/8mA	0
AUD_DAT_MOSI	0	GPIO145	IO	CU, CD	2/4/6/8mA	0
	1	AUD_DAT_MOSI	O	CU, CD	2/4/6/8mA	0
	3	AUD_DAT_MISO	I	CU, CD	2/4/6/8mA	0
DISP_PWM	0	GPIO69	IO	CU, CD	2/4/6/8mA	0
	1	DISP_PWM	O	CU, CD	2/4/6/8mA	0
	2	PWM1	O	CU, CD	2/4/6/8mA	0
	3	LTE_MD32_JTAG_TRST	I	CU, CD	2/4/6/8mA	0
	4	TDD_TRSTN	I	CU, CD	2/4/6/8mA	0
	5	ANT_SEL7	O	CU, CD	2/4/6/8mA	0
	6	DM_JTINTP	O	CU, CD	2/4/6/8mA	0
LCM_RST	0	GPIO146	IO	CU, CD	2/4/6/8mA	0
	1	LCM_RST	O	CU, CD	2/4/6/8mA	0
DSI_TE	0	GPIO147	IO	CU, CD	2/4/6/8mA	0
	1	DSI_TE	I	CU, CD	2/4/6/8mA	0
CMDAT0	0	GPIO42	IO	CU, CD	2/4/6/8mA	0
	1	CMDAT0	I	CU, CD	2/4/6/8mA	0

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Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
	2	CMCSD0	I	CU, CD	2/4/6/8mA	0
	3	CMMCLK1	O	CU, CD	2/4/6/8mA	0
	6	ANT_SEL5	O	CU, CD	2/4/6/8mA	0
	7	CLKM5	O	CU, CD	2/4/6/8mA	0
CMDAT1	0	GPIO43	IO	CU, CD	2/4/6/8mA	0
	1	CMDAT1	I	CU, CD	2/4/6/8mA	0
	2	CMCSD1	I	CU, CD	2/4/6/8mA	0
	3	CMFLASH	O	CU, CD	2/4/6/8mA	0
	4	MD_EINT0	I	CU, CD	2/4/6/8mA	0
	5	CMMCLK1	O	CU, CD	2/4/6/8mA	0
	6	CLKM4	O	CU, CD	2/4/6/8mA	0
	7	DBG_MON_A10	IO	CU, CD	2/4/6/8mA	0
CMPCLK	0	GPIO44	IO	CU, CD	2/4/6/8mA	0
	1	CMPCLK	I	CU, CD	2/4/6/8mA	0
	2	CMCSK	I	CU, CD	2/4/6/8mA	0
	3	CMCSD2	I	CU, CD	2/4/6/8mA	0
	4	KCOL3	IO	CU, CD	2/4/6/8mA	0
	5	SRCLKENAI2	I	CU, CD	2/4/6/8mA	0
	6	PWM0	O	CU, CD	2/4/6/8mA	0
	7	DBG_MON_A11	IO	CU, CD	2/4/6/8mA	0
CMMCLK	0	GPIO45	IO	CU, CD	2/4/6/8mA	0
	1	CMMCLK0	O	CU, CD	2/4/6/8mA	0
	7	DBG_MON_A12	IO	CU, CD	2/4/6/8mA	0
CMMCLK1	0	GPIO46	IO	CU, CD	2/4/6/8mA	0
	1	CMMCLK1	O	CU, CD	2/4/6/8mA	0
	2	IDDIG	I	CU, CD	2/4/6/8mA	0
	3	LTE_MD32_JTAG_TRST	I	CU, CD	2/4/6/8mA	0
	4	TDD_TRSTN	I	CU, CD	2/4/6/8mA	0
	5	DM_JTINTP	O	CU, CD	2/4/6/8mA	0
	6	KCOL6	IO	CU, CD	2/4/6/8mA	0
	7	DBG_MON_A13	IO	CU, CD	2/4/6/8mA	0
PWRAP_SPI0_CK	0	GPIO141	IO	CU, CD	2/4/6/8mA	0
	1	PWRAP_SPICK_I	O	CU, CD	2/4/6/8mA	0
PWRAP_SPI0_CSN	0	GPIO142	IO	CU, CD	2/4/6/8mA	0
	1	PWRAP_SPICS_B_I	O	CU, CD	2/4/6/8mA	0
PWRAP_SPI0_MI	0	GPIO138	IO	CU, CD	2/4/6/8mA	0
	1	PWRAP_SPIDO	IO	CU, CD	2/4/6/8mA	0
	2	PWRAP_SPIDI	IO	CU, CD	2/4/6/8mA	0
PWRAP_SPI0_	0	GPIO139	IO	CU, CD	2/4/6/8mA	0

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Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
MO						
	1	PWRAP_SPIDI	IO	CU, CD	2/4/6/8mA	0
	2	PWRAP_SPIDO	IO	CU, CD	2/4/6/8mA	0
WATCHDOG	0	GPIO149	IO	CU, CD	2/4/6/8mA	0
	1	WATCHDOG	O	CU, CD	2/4/6/8mA	0
SRCLKENA0	0	GPIO148	IO	CU, CD	2/4/6/8mA	0
	1	SRCLKENA0	O	CU, CD	2/4/6/8mA	0
SRCLKENA1	0	GPIO56	IO	CU, CD	2/4/6/8mA	0
	1	SRCLKENA1	O	CU, CD	2/4/6/8mA	0
SCL0	0	GPIO48	IO	CD		0
	1	SCL0_0	IO	CD		0
SCL1	0	GPIO50	IO	CD		0
	1	SCL1_0	IO	CD		0
SCL2	0	GPIO52	IO	CD		0
	1	SCL2_0	IO	CD		0
SCL3	0	GPIO54	IO	CD		0
	1	SCL3_0	IO	CD		0
	3	IDDIG	I	CD		0
SDA0	0	GPIO47	IO	CD		0
	1	SDA0_0	IO	CD		0
SDA1	0	GPIO49	IO	CD		0
	1	SDA1_0	IO	CD		0
SDA2	0	GPIO51	IO	CD		0
	1	SDA2_0	IO	CD		0
SDA3	0	GPIO53	IO	CD		0
	1	SDA3_0	IO	CD		0
	3	IDDIG	I	CD		0
RFIC0_BSI_EN	0	GPIO110	IO	CU, CD	2/4/6/8mA	0
	1	RFIC0_BSI_EN	O	CU, CD	2/4/6/8mA	0
	4	SPM_BSI_EN	O	CU, CD	2/4/6/8mA	0
RFIC0_BSI_CK	0	GPIO111	IO	CU, CD	2/4/6/8mA	0
	1	RFIC0_BSI_CK	O	CU, CD	2/4/6/8mA	0
	4	SPM_BSI_CLK	O	CU, CD	2/4/6/8mA	0
RFIC0_BSI_D0	0	GPIO112	IO	CU, CD	2/4/6/8mA	0
	1	RFIC0_BSI_D0	IO	CU, CD	2/4/6/8mA	0
	4	SPM_BSI_D2	IO	CU, CD	2/4/6/8mA	0
RFIC0_BSI_D1	0	GPIO113	IO	CU, CD	2/4/6/8mA	0
	1	RFIC0_BSI_D1	IO	CU, CD	2/4/6/8mA	0
	4	SPM_BSI_D1	IO	CU, CD	2/4/6/8mA	0
RFIC0_BSI_D2	0	GPIO114	IO	CU, CD	2/4/6/8mA	0
	1	RFIC0_BSI_D2	IO	CU, CD	2/4/6/8mA	0
	4	SPM_BSI_D0	IO	CU, CD	2/4/6/8mA	0

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RFIC1_BSI_EN	0	GPIO104	IO	CU, CD	2/4/6/8mA	0
	1	RFIC1_BSI_EN	O	CU, CD	2/4/6/8mA	0
	5	C2K_RX_BSI_EN	O	CU, CD	2/4/6/8mA	0
RFIC1_BSI_CK	0	GPIO105	IO	CU, CD	2/4/6/8mA	0
	1	RFIC1_BSI_CK	O	CU, CD	2/4/6/8mA	0
	2	PCM1_SYNC	IO	CU, CD	2/4/6/8mA	0
	5	C2K_RX_BSI_CLK	O	CU, CD	2/4/6/8mA	0
RFIC1_BSI_D0	0	GPIO106	IO	CU, CD	2/4/6/8mA	0
	1	RFIC1_BSI_D0	IO	CU, CD	2/4/6/8mA	0
	5	C2K_RX_BSI_DATA	IO	CU, CD	2/4/6/8mA	0
RFIC1_TX_BSI_EN	0	GPIO107	IO	CU, CD	2/4/6/8mA	0
	1	RFIC1_BSI_D1	IO	CU, CD	2/4/6/8mA	0
	5	C2K_TX_BSI_EN	O	CU, CD	2/4/6/8mA	0
RFIC1_TX_BSI_CK	0	GPIO108	IO	CU, CD	2/4/6/8mA	0
	1	RFIC1_BSI_D2	IO	CU, CD	2/4/6/8mA	0
	5	C2K_TX_BSI_CLK	O	CU, CD	2/4/6/8mA	0
RFIC1_TX_BSI_D0	0	GPIO109	IO	CU, CD	2/4/6/8mA	0
	5	C2K_TX_BSI_DATA	IO	CU, CD	2/4/6/8mA	0
PAD_RFIC_MIPI1_SCLK	0	GPIO133	IO	CU, CD	2/4/6/8mA	0
	1	MIPI1_SCLK	O	CU, CD	2/4/6/8mA	0
PAD_RFIC_MIPI1_SDATA	0	GPIO134	IO	CU, CD	2/4/6/8mA	0
	1	MIPI1_SDATA	IO	CU, CD	2/4/6/8mA	0
PAD_RFIC_MIPI0_SCLK	0	GPIO135	IO	CU, CD	2/4/6/8mA	0
	1	MIPI0_SCLK	O	CU, CD	2/4/6/8mA	0
PAD_RFIC_MIPI0_SDATA B	0	GPIO136	IO	CU, CD	2/4/6/8mA	0
	1	MIPI0_SDATA	IO	CU, CD	2/4/6/8mA	0
BPI_BUS0	0	GPIO119	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	BPI_BUS0	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_B28	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
BPI_BUS1	0	GPIO120	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	BPI_BUS1	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_B29	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
BPI_BUS2	0	GPIO121	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	BPI_BUS2	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_B30	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
BPI_BUS3	0	GPIO122	IO	CU, CD	2/4/6/8/10/12/14/16mA	0

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	1	BPI_BUS3	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_B31	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
BPI_BUS4	0	GPIO123	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	BPI_BUS4	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_B32	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
BPI_BUS5	0	GPIO87	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	BPI_BUS5	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	2	LTE_C2K_BPI_BUS5	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	5	C2K_BPI_BUS5	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_B0	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
BPI_BUS6	0	GPIO88	IO	CU, CD	4/8/12/16mA	0
	1	BPI_BUS6	O	CU, CD	4/8/12/16mA	0
	2	LTE_C2K_BPI_BUS6	O	CU, CD	4/8/12/16mA	0
	3	Reserved	-	CU, CD	4/8/12/16mA	0
	4	Reserved	-	CU, CD	4/8/12/16mA	0
	5	C2K_BPI_BUS6	O	CU, CD	4/8/12/16mA	0
	6	Reserved	-	CU, CD	4/8/12/16mA	0
	7	DBG_MON_B1	IO	CU, CD	4/8/12/16mA	0
BPI_BUS7	0	GPIO89	IO	CU, CD	4/8/12/16mA	0
	1	BPI_BUS7	O	CU, CD	4/8/12/16mA	0
	2	LTE_C2K_BPI_BUS7	O	CU, CD	4/8/12/16mA	0
	3	CLKM0	O	CU, CD	4/8/12/16mA	0
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS7	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B2	IO	CU, CD	4/8/12/16mA	-
BPI_BUS8	-	GPIO9-	IO	CU, CD	4/8/12/16mA	-
	1	BPI_BUS8	O	CU, CD	4/8/12/16mA	-
	2	LTE_C2K_BPI_BUS8	O	CU, CD	4/8/12/16mA	-
	3	CLKM1	O	CU, CD	4/8/12/16mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS8	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B3	IO	CU, CD	4/8/12/16mA	-
BPI_BUS9	-	GPIO91	IO	CU, CD	4/8/12/16mA	-
	1	BPI_BUS9	O	CU, CD	4/8/12/16mA	-
	2	LTE_C2K_BPI_BUS9	O	CU, CD	2/4/6/8mA	-
	3	CLKM2	O	CU, CD	4/8/12/16mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS9	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B4	IO	CU, CD	4/8/12/16mA	-

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BPI_BUS1-	-	GPIO92	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS1-	O	CU, CD	2/4/6/8mA	-
	2	LTE_C2K_BPI_BUS1-	O	CU, CD	2/4/6/8mA	-
	3	CLKM3	O	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS1-	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B5	IO	CU, CD	4/8/12/16mA	-
BPI_BUS11	-	GPIO93	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS11	O	CU, CD	2/4/6/8mA	-
	2	LTE_C2K_BPI_BUS11	O	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS11	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B6	IO	CU, CD	4/8/12/16mA	-
BPI_BUS12	-	GPIO94	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS12	O	CU, CD	2/4/6/8mA	-
	2	LTE_C2K_BPI_BUS12	O	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS12	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B7	IO	CU, CD	4/8/12/16mA	-
BPI_BUS13	-	GPIO95	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS13	O	CU, CD	2/4/6/8mA	-
	2	LTE_C2K_BPI_BUS13	O	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS13	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B8	IO	CU, CD	4/8/12/16mA	-
BPI_BUS14	-	GPIO96	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS14	O	CU, CD	2/4/6/8mA	-
	2	LTE_C2K_BPI_BUS14	O	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS14	O	CU, CD	4/8/12/16mA	-

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	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B9	IO	CU, CD	4/8/12/16mA	-
BPI_BUS15	-	GPIO97	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS15	O	CU, CD	2/4/6/8mA	-
	2	LTE_C2K_BPI_BUS15	O	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS15	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B1-	IO	CU, CD	4/8/12/16mA	-
BPI_BUS16	-	GPIO98	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS16	O	CU, CD	2/4/6/8mA	-
	2	LTE_C2K_BPI_BUS16	O	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS16	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B11	IO	CU, CD	4/8/12/16mA	-
BPI_BUS17	-	GPIO99	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS17	O	CU, CD	2/4/6/8mA	-
	2	LTE_C2K_BPI_BUS17	O	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS17	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B12	IO	CU, CD	4/8/12/16mA	-
BPI_BUS18	-	GPIO1--	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS18	O	CU, CD	2/4/6/8mA	-
	2	LTE_C2K_BPI_BUS18	O	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS18	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B13	IO	CU, CD	4/8/12/16mA	-
BPI_BUS19	-	GPIO1-1	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS19	O	CU, CD	2/4/6/8mA	-
	2	LTE_C2K_BPI_BUS19	O	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-

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	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS19	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B14	IO	CU, CD	4/8/12/16mA	-
BPI_BUS2-	-	GPIO1-2	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS2-	O	CU, CD	2/4/6/8mA	-
	2	LTE_C2K_BPI_BUS2-	O	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS2-	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B15	IO	CU, CD	4/8/12/16mA	-
BPI_BUS21	-	GPIO124	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS21	O	CU, CD	2/4/6/8mA	-
	2	Reserved	-	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	DPI_HSYNC1	O	CU, CD	4/8/12/16mA	-
	6	KCOL2	IO	CU, CD	4/8/12/16mA	-
	7	TDD_TXD	O	CU, CD	4/8/12/16mA	-
BPI_BUS22	-	GPIO125	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS22	O	CU, CD	2/4/6/8mA	-
	2	Reserved	-	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	DPI_VSYNC1	O	CU, CD	4/8/12/16mA	-
	6	KROW2	IO	CU, CD	4/8/12/16mA	-
	7	MD_URXD	I	CU, CD	4/8/12/16mA	-
BPI_BUS23	-	GPIO126	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS23	O	CU, CD	2/4/6/8mA	-
	2	Reserved	-	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	DPI_CK1	O	CU, CD	4/8/12/16mA	-
	6	I2S2_MCK	O	CU, CD	4/8/12/16mA	-
	7	MD_UTXD	O	CU, CD	4/8/12/16mA	-
BPI_BUS24	-	GPIO127	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS24	O	CU, CD	2/4/6/8mA	-
	2	Reserved	-	CU, CD	2/4/6/8mA	-
	3	CONN_MCU_DBGI_N	I	CU, CD	2/4/6/8mA	-

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Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
	4	EXT_FRAME_SYNC	I	CU, CD	4/8/12/16mA	-
	5	DPI_DE1	O	CU, CD	4/8/12/16mA	-
	6	SRCLKENAI1	I	CU, CD	4/8/12/16mA	-
	7	URXD-	I	CU, CD	4/8/12/16mA	-
BPI_BUS25	-	GPIO128	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS25	O	CU, CD	2/4/6/8mA	-
	2	Reserved	-	CU, CD	2/4/6/8mA	-
	3	GPS_FRAME_SYNC	O	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	I2S2_DI	I	CU, CD	4/8/12/16mA	-
	6	PTA_RXD	I	CU, CD	4/8/12/16mA	-
	7	UTXD-	O	CU, CD	4/8/12/16mA	-
BPI_BUS26	-	GPIO129	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS26	O	CU, CD	2/4/6/8mA	-
	2	DISP_PWM	O	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	I2S2_LRCK	O	CU, CD	4/8/12/16mA	-
	6	PTA_TXD	O	CU, CD	4/8/12/16mA	-
	7	LTE_URXD	I	CU, CD	4/8/12/16mA	-
BPI_BUS27	-	GPIO13-	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS27	O	CU, CD	2/4/6/8mA	-
	2	Reserved	-	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	I2S2_BCK	O	CU, CD	4/8/12/16mA	-
	6	IRTX_OUT	O	CU, CD	4/8/12/16mA	-
	7	LTE_UTXD	O	CU, CD	4/8/12/16mA	-
LTE_TXBPI	-	GPIO118	IO	CU, CD	2/4/6/8mA	-
	1	TXBPI	I	CU, CD	2/4/6/8mA	-
C2K_TXBPI	-	GPIO1-3	IO	CU, CD	2/4/6/8mA	-
	1	C2K_TXBPI	I	CU, CD	2/4/6/8mA	-
WB_CTRL-	-	GPIO13	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	1	WB_CTRL-	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	3	C2K_ARM_EINT-	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	7	DBG_MON_A-	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
WB_CTRL1	-	GPIO14	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	1	WB_CTRL1	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	3	C2K_ARM_EINT1	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	7	DBG_MON_A1	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
WB_CTRL2	-	GPIO15	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	1	WB_CTRL2	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-

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Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
	3	C2K_ARM_EINT2	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	7	DBG_MON_A2	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
WB_CTRL3	-	GPIO16	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	1	WB_CTRL3	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	3	C2K_ARM_EINT3	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	7	DBG_MON_A3	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
WB_CTRL4	-	GPIO17	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	1	WB_CTRL4	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	3	C2K_DM_EINT-	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	4	WATCHDOG	O	CU, CD	2/4/6/8/1-/12/14/16mA	-
	7	DBG_MON_A4	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
WB_CTRL5	-	GPIO18	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	1	WB_CTRL5	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	2	C2K_DM_EINT1	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	7	DBG_MON_A5	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
F2W_DATA	-	GPIO184	IO	CU, CD	2/4/6/8mA	-
	1	F2W_DATA	I	CU, CD	2/4/6/8mA	-
	2	MRG_CLK	O	CU, CD	2/4/6/8mA	-
	3	C2K_DM_EINT2	IO	CU, CD	2/4/6/8mA	-
	4	PCM-_CLK	O	CU, CD	2/4/6/8mA	-
F2W_CLK	-	GPIO185	IO	CU, CD	2/4/6/8mA	-
	1	F2W_CK	I	CU, CD	2/4/6/8mA	-
	2	MRG_DI	I	CU, CD	2/4/6/8mA	-
	3	C2K_DM_EINT3	IO	CU, CD	2/4/6/8mA	-
	4	PCM-_DI	I	CU, CD	2/4/6/8mA	-
WB_SCLK	-	GPIO187	IO	CU, CD	2/4/6/8mA	-
	1	WB_SCLK	O	CU, CD	2/4/6/8mA	-
	2	MRG_DO	O	CU, CD	2/4/6/8mA	-
	4	PCM-_DO	O	CU, CD	2/4/6/8mA	-
WB_SDATA	-	GPIO188	IO	CU, CD	2/4/6/8mA	-
	1	WB_SDATA	IO	CU, CD	2/4/6/8mA	-
	2	MRG_SYNC	O	CU, CD	2/4/6/8mA	-
	4	PCM-_SYNC	O	CU, CD	2/4/6/8mA	-
WB_SEN	-	GPIO189	IO	CU, CD	2/4/6/8mA	-
	1	WB_SEN	O	CU, CD	2/4/6/8mA	-
	4	UTXD3	O	CU, CD	2/4/6/8mA	-
	5	URXD3	I	CU, CD	2/4/6/8mA	-
WB_RSTB	-	GPIO186	IO	CU, CD	2/4/6/8mA	-
	1	WB_RSTB	O	CU, CD	2/4/6/8mA	-
	4	URXD3	I	CU, CD	2/4/6/8mA	-
	5	UTXD3	O	CU, CD	2/4/6/8mA	-
KPCOL-	-	GPIO84	IO	CU, CD	2/4/6/8mA	-

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Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
	1	KCOL-	IO	CU, CD	2/4/6/8mA	-
	2	URTS-	O	CU, CD	2/4/6/8mA	-
	3	CONN_MCU_DBGACK_N	O	CU, CD	2/4/6/8mA	-
	4	SCL2	IO	CU, CD	2/4/6/8mA	-
	5	C2K_TDO	IO	CU, CD	2/4/6/8mA	-
	6	AUXIF_CLK	O	CU, CD	2/4/6/8mA	-
	7	Reserved	-	CU, CD	2/4/6/8mA	-
KPCOL1	-	GPIO85	IO	CU, CD	2/4/6/8mA	-
	1	KCOL1	IO	CU, CD	2/4/6/8mA	-
	2	UCTS-	I	CU, CD	2/4/6/8mA	-
	3	UCTS1	I	CU, CD	2/4/6/8mA	-
	4	SDA2	IO	CU, CD	2/4/6/8mA	-
	5	C2K_TMS	I	CU, CD	2/4/6/8mA	-
	6	AUXIF_ST	O	CU, CD	2/4/6/8mA	-
	7	DBG_MON_A31	IO	CU, CD	2/4/6/8mA	-
KPCOL2	-	GPIO86	IO	CU, CD	2/4/6/8mA	-
	1	KCOL2	IO	CU, CD	2/4/6/8mA	-
	2	Reserved	-	CU, CD	2/4/6/8mA	-
	3	URTS1	O	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	2/4/6/8mA	-
	5	C2K_RTCK	O	CU, CD	2/4/6/8mA	-
	6	Reserved	-	CU, CD	2/4/6/8mA	-
	7	DBG_MON_A32	IO	CU, CD	2/4/6/8mA	-
KPROW-	-	GPIO81	IO	CU, CD	2/4/6/8mA	-
	1	KROW-	IO	CU, CD	2/4/6/8mA	-
	2	Reserved	-	CU, CD	2/4/6/8mA	-
	3	CONN_MCU_DBGI_N	I	CU, CD	2/4/6/8mA	-
	4	CORESONIC_SWCK	I	CU, CD	2/4/6/8mA	-
	5	C2K_TCK	I	CU, CD	2/4/6/8mA	-
	6	Reserved	-	CU, CD	2/4/6/8mA	-
	7	C2K_DM_EINT1	IO	CU, CD	2/4/6/8mA	-
KPROW1	-	GPIO82	IO	CU, CD	2/4/6/8mA	-
	1	KROW1	IO	CU, CD	2/4/6/8mA	-
	2	Reserved	-	CU, CD	2/4/6/8mA	-
	3	CONN_MCU_TRST_B	I	CU, CD	2/4/6/8mA	-
	4	CORESONIC_SWD	IO	CU, CD	2/4/6/8mA	-
	5	C2K_NTRST	I	CU, CD	2/4/6/8mA	-
	6	USB_DRVVBUS	O	CU, CD	2/4/6/8mA	-
	7	C2K_DM_EINT2	IO	CU, CD	2/4/6/8mA	-

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Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
KPROW2	-	GPIO83	IO	CU, CD	2/4/6/8mA	-
	1	KROW2	IO	CU, CD	2/4/6/8mA	-
	2	USB_DRVVBUS	O	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	2/4/6/8mA	-
	5	C2K_TDI	I	CU, CD	2/4/6/8mA	-
	6	Reserved	-	CU, CD	2/4/6/8mA	-
	7	C2K_DM_EINT3	IO	CU, CD	2/4/6/8mA	-
SRCLKENAI	-	GPIO55	IO	CU, CD	2/4/6/8mA	-
	1	SRCLKENAI-	I	CU, CD	2/4/6/8mA	-
	2	PWM2	O	CU, CD	2/4/6/8mA	-
	3	CLKM5	O	CU, CD	2/4/6/8mA	-
	4	CORESONIC_SWD	IO	CU, CD	2/4/6/8mA	-
	5	ANT_SEL6	O	CU, CD	2/4/6/8mA	-
	6	KROW5	IO	CU, CD	2/4/6/8mA	-
	7	DISP_PWM	O	CU, CD	2/4/6/8mA	-
SPI_CSB	-	GPIO65	IO	CU, CD	2/4/6/8mA	-
	1	SPI_CSA	O	CU, CD	2/4/6/8mA	-
	2	EXT_FRAME_SYNC	I	CU, CD	2/4/6/8mA	-
	3	I2S3_MCK	O	CU, CD	2/4/6/8mA	-
	4	KROW2	IO	CU, CD	2/4/6/8mA	-
	5	GPS_FRAME_SYNC	O	CU, CD	2/4/6/8mA	-
	6	PTA_RXD	I	CU, CD	2/4/6/8mA	-
	7	DBG_MON_A22	IO	CU, CD	2/4/6/8mA	-
SPI_CLK	-	GPIO66	IO	CU, CD	2/4/6/8mA	-
	1	SPI_CKA	O	CU, CD	2/4/6/8mA	-
	2	USB_DRVVBUS	O	CU, CD	2/4/6/8mA	-
	3	I2S3_BCK	O	CU, CD	2/4/6/8mA	-
	4	KCOL2	IO	CU, CD	2/4/6/8mA	-
	5	Reserved	-	CU, CD	2/4/6/8mA	-
	6	PTA_TXD	O	CU, CD	2/4/6/8mA	-
	7	DBG_MON_A23	IO	CU, CD	2/4/6/8mA	-
SPI_MO	-	GPIO68	IO	CU, CD	2/4/6/8mA	-
	1	SPI_MOA	O	CU, CD	2/4/6/8mA	-
	2	SPI_MIA	I	CU, CD	2/4/6/8mA	-
	3	I2S3_LRCK	O	CU, CD	2/4/6/8mA	-
	4	PTA_TXD	O	CU, CD	2/4/6/8mA	-
	5	ANT_SEL4	O	CU, CD	2/4/6/8mA	-
	6	URTS1	O	CU, CD	2/4/6/8mA	-
	7	DBG_MON_A25	IO	CU, CD	2/4/6/8mA	-
SPI_MI	-	GPIO67	IO	CU, CD	2/4/6/8mA	-
	1	SPI_MIA	I	CU, CD	2/4/6/8mA	-

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Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
	2	SPI_MOA	O	CU, CD	2/4/6/8mA	-
	3	I2S3_DO	O	CU, CD	2/4/6/8mA	-
	4	PTA_RXD	I	CU, CD	2/4/6/8mA	-
	5	IDDIG	I	CU, CD	2/4/6/8mA	-
	6	UCTS1	I	CU, CD	2/4/6/8mA	-
	7	DBG_MON_A24	IO	CU, CD	2/4/6/8mA	-

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2.2 Electrical Characteristic

2.2.1 Absolute Maximum Ratings

Table 2-8. Absolute maximum ratings for power supply

Symbol or pin name	Description	Min.	Max.	Unit
AVDD18_PLLGP AVDD18_MEMPLL AVDD18_MDPLLGP	Analog power input 1.8V for PLL	1.7	1.9	V
AVDD18_AP	Analog power input 1.8V for AuxADC, TSENSE	1.7	1.9	V
AVDD18_MD	Analog power input 1.8V for BBTX, BBRX	1.7	1.9	V
AVDD28_DAC	Analog power input 2.8V for APC	2.66	2.94	V
DVDD18_MIPITX1	Analog power for MIPI DSI	1.7	1.9	V
DVDD18_MIPIRX- DVDD18_MIPIRX1	Analog power for MIPI CSI- & CSI1	1.7	1.9	V
AVDD33_USB_P- AVDD33_USB_P1	Analog power 3.3V for USB	3.135	3.465	V
AVDD18_USB	Analog power 1.8V for USB	1.7	1.9	V
AVDD18_WBG	Analog power 1.8V for connectivity ABB	1.7	1.9	V
DVDD18_IO! DVDD18_IO2 DVDD18_IO3 DVDD18_BIAS1 DVDD18_BIAS2 DVDD18_BIAS3	Digital power input for 1.8V IO	1.62	1.98	V
DVDD28_BPI1 DVDD28_BPI2	Digital power input for BPI	1.7	3.6	V
DVDD18_MSDC-	Digital power input for MSDC-	1.62	1.98	V
DVDD28_MSDC1	Digital power input for MSDC1	1.7	3.6	V
DVDD28_SIM1	Digital power input for SIM1	1.7	3.6	V
DVDD28_SIM2	Digital power input for SIM2	1.7	3.6	V
DDRV DDRV_CLK DDRV_VREF	Digital power input for DRAM	1.14	1.3	V
DVDD_DVFS	Digital power input for DVFS	-.72	1.131	V
DVDD_GPU	Digital power input for GPU	-.93	1.125	V
DVDD_LTE	Digital power input for LTE	-.9	1.1	V
DVDD_SRAM	Digital power input for SRAM	-.93	1.131	V
DVDD_TOP	Digital power input for TOP	-.63	1.125	V

Warning: *Stressing the device beyond the absolute maximum ratings may cause permanent damage. These are stress ratings only.*

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2.2.2 Recommended Operating Conditions

Table 2-9. Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
AVDD18_PLLGP AVDD18_MEMPLL AVDD18_MDPLLGP	Analog power input 1.8V for PLL	1.7	1.8	1.89	V
AVDD18_AP	Analog power input 1.8V for AuxADC, TSENSE	1.71	1.8	1.89	V
AVDD18_MD	Analog power input 1.8V for BBTX, BBRX	1.71	1.8	1.89	V
AVDD28_DAC	Analog power input 2.8V for APC	2.66	2.8	2.94	V
DVDD18_MIPITX1	Analog power for MIPI DSI	1.71	1.8	1.89	V
AVDD33_USB_P- AVDD33_USB_P1	Analog power for MIPI CSI- & CSI1	1.71	1.8	1.89	V
AVDD33_USB	Analog power 3.3V for USB	3.135	3.3	3.465	V
AVDD18_USB	Analog power 1.8V for USB	1.71	1.8	1.89	V
AVDD18_WBG	Analog power 1.8V for connectivity ABB	1.71	1.8	1.89	V
DVDD28_BPI1 DVDD28_BPI2	Digital power input for BPI	1.7	1.8	1.95	V
		2.66	2.8	2.94	
DVDD18_IO! DVDD18_IO2 DVDD18_IO3 DVDD18_BIAS1 DVDD18_BIAS2 DVDD18_BIAS3	Digital power input for 1.8V IO	1.62	1.8	1.98	V
DVDD18_MSDC-	Digital power input for MSDC-	1.62	1.8	1.98	V
DVDD28_MSDC1	Digital power input for MSDC1	1.7	1.8	1.95	V
		2.7	3.3	3.6	
DVDD28_SIM1 DVDD28_SIM2	Digital power input for SIM1/SIM2	2.7	3.3	3.6	V
		1.7	1.8	1.9	
DDRV DDRV_CLK DDRV_VREF	Digital power input for EMI (LPDDR2/3)	1.14	1.2	1.3	V
DVDD_DVFS	Digital power input for DVFS	-.72	1.-	1.131	V
DVDD_GPU	Digital power input for GPU	-.93	1.-	1.125	V
DVDD_LTE	Digital power input for LTE	-.9	1.-	1.1	V
DVDD_SRAM	Digital power input for SRAM	-.93	1.-	1.131	V
DVDD_TOP	Digital power input for TOP	-.63	1.-	1.125	V

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2.2.3 Storage Condition

1. Shelf life in sealed bag: 12 months at < 40°C and < 90% relative humidity (RH).
2. After the bag is opened, devices subjected to infrared reflow, vapor-phase reflow or equivalent processing must be:
   - Mounted within 168 hours in factory condition of 30°C/60% RH, or
   - Stored at 20% RH

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3. Devices require baking before being mounted, if they are placed
   - For 192 hours at 40°C +5°C/-0°C and < 5% RH in low temperature device containers, or
   - For 24 hours at 125°C +5°C/-0°C in high temperature device containers.

2.2.4 AC Electrical Characteristics and Timing Diagram

2.2.4.1.1 External Memory Interface for LPDDR3

The external memory interface, shown in Figure 2-4. Basic timing parameter for LPDDR3 commands, Figure 2-5 and Figure 2-6, is used to connect LPDDR3 device for MT6735. It includes pins CLK_T, CLK_C, CKE[1:0], CS[1:0], DQS[3:0], DQS#[3:0], CA[9:0] and DQ[31:0]. Table 2-10 summarizes the symbol definition and the related timing specifications.

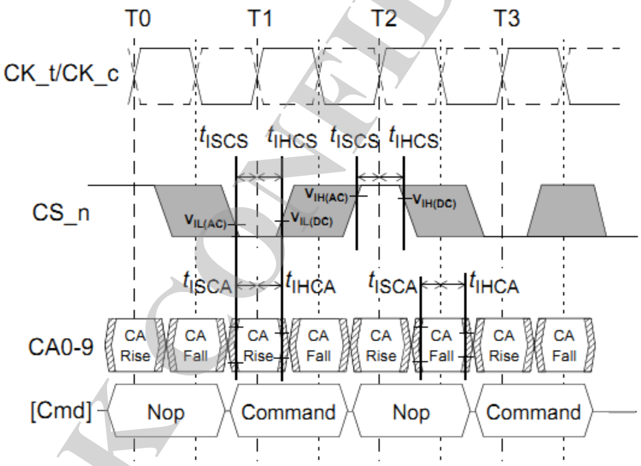

Figure 2-4. Basic timing parameter for LPDDR3 commands

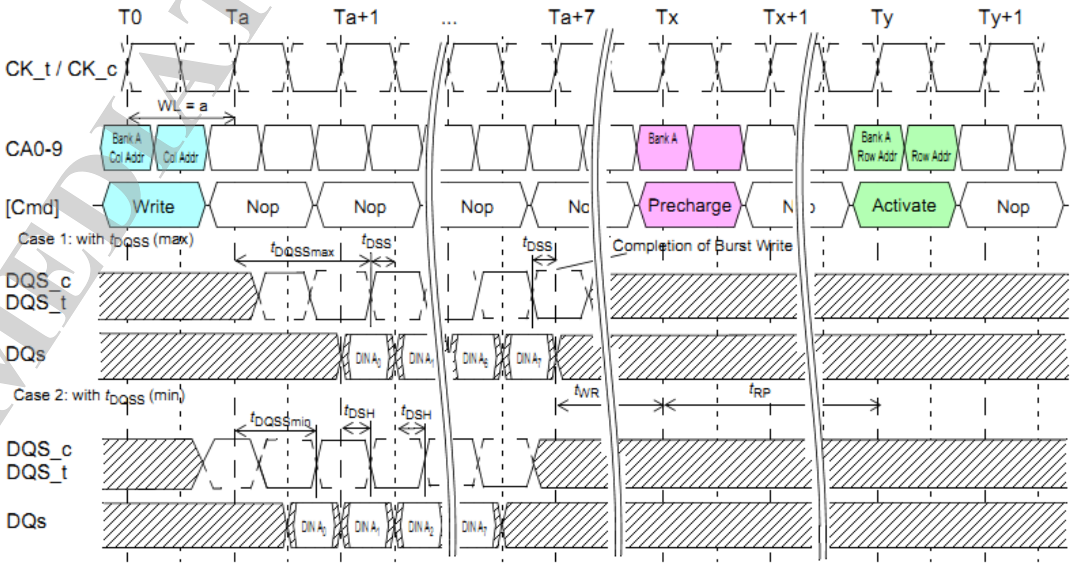

Figure 2-5. Basic timing parameter for LPDDR3 write

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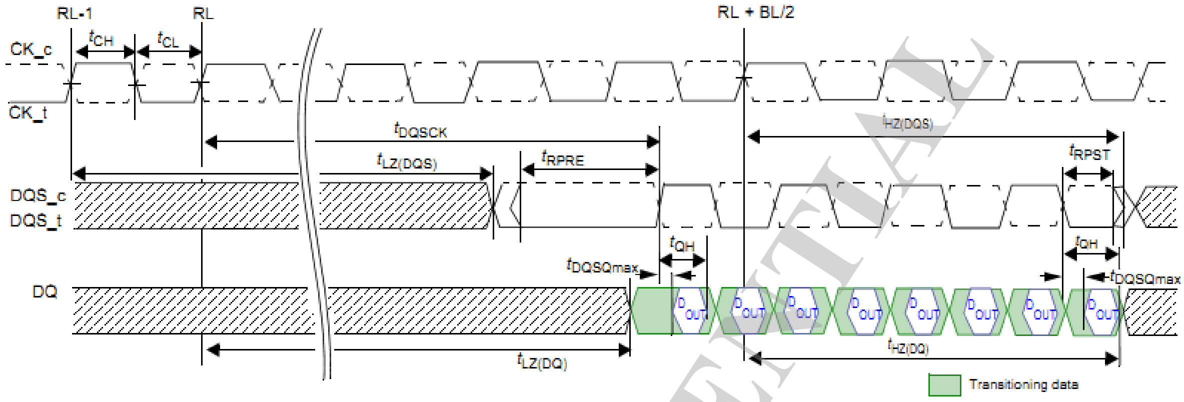

Figure 2-6. Basic LPDDR3 read timing parameter

Table 2-10. LPDDR3 AC timing parameter table of external memory interface

Symbol	Description	Min.	Typ.	Max.	Unit
tCK	Clock cycle time	1.071		100	ns
tDQSCK	DQS output access time from CK/CK'	2.5		5.5	ns
tCH	Clock high level width	0.45		0.55	tCK
tCL	Clock low level width	0.45		0.55	tCK
tDS	DQ & DM input setup time	0.13			ns
tDH	DQ & DM input hold time	0.13			ns
tDIPW	DQ and DM input pulse width	0.35			tCK
tDQSS	Write command to 1st DQS latching transition	0.75		1.25	tCK
tDSS	DQS falling edge to CK setup time	0.2			tCK
tDSH	DQS falling edge hold time from CK	0.2			tCK
tWPST	Write postamble	0.4			tCK
tWPRE	Write preamble	0.8			tCK
tISCA	Address & control input setup time	0.13			ns
tIHCA	Address & control input hold time	0.13			ns
tISCS	CS_ input setup time	0.23			ns
tIHCS	CS_ input hold time	0.23			ns
tIPWCA	Address and control input pulse width	0.35			tCK
tIPWCS	CS_ input pulse width	0.7			tCK
tCKE	CKE minimum pulse width (HIGH and LOW pulse width)	Max. (7.5ns, 3tCK)			ns
tISCKE	CKE input setup time	0.25			tCK
tIHCKE	CKE input hold time	0.25			tCK
tCPDED	Command path disable delay	2			tCK
tLZ(DQS)	DQS low-impedance time from CK/CK'	tDQSCK (MIN) - 0.3			ns
tHZ(DQS)	DQS high-impedance time from CK/CK'			tDQSCK (MAX) –	ns

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Symbol	Description	Min.	Typ.	Max.	Unit
				0.1	
tLZ(DQ)	DQ low-impedance time from CK/CK'	tDQSCK (MIN) - 0.3			ns
tHZ(DQ)	DQ high-impedance time from CK/CK'			tDQSCK (MAX) + [1.4*tDQSQ (MAX)]	ns
tDQSQ	DQS-DQ skew			0.115	ns
tDQSH	DQS input high-level width	0.4			tCK
tDQSL	DQS input low-level width	0.4			tCK
tQSH	DQS output high pulse width	tCH - 0.05			tCK
tQSL	DQS output low pulse width	tCL - 0.05			tCK
tQH	DQ/DQS output hold time from DQS	Min. (tQSH, tQSL)			ns
tMRW	MODE register Write command period	Max. (10tCK, 15)			ns
tMRR	MODE register Read command period	4			tCK
tMRD	Mode register set command delay	Max. (10tCK, 14)			ns
tRPRE	Read preamble	0.9			tCK
tRPST	Read postamble	0.3			tCK
tRAS	ACTIVE to PRECHARGE command period	Max. (42ns, 3tCK)		70000	ns
tRC	ACTIVE to ACTIVE command period	tRAS + tRPab (with all-bank pre-charge) tRAS + tRPpb (with per-bank pre-charge)			ns
tRFC	AUTO REFRESH to ACTIVE/AUTO REFRESH command period	56			ns
tRCD	ACTIVE to READ or WRITE delay	Max. (18ns, 3tCK)			ns
tRPpb	Row PRECHARGE Time (single bank)	Max. (18ns, 3tCK)			ns
tRPab	Row PRECHARGE Time (all banks)	Max. (21ns, 3tCK)			ns
tRRD	ACTIVE bank A to ACTIVE bank B delay	Max. (10ns, 2tCK)			ns
tWR	WRITE recovery time	Max. (15ns, 4tCK)			ns
tWTR	Internal write to READ command time	Max. (7.5ns, 4tCK)			ns
tXSR	SELF REFRESH exit to next valid command	Max. (tRFCab + 10ns, 2tCK)			ns
tXP	EXIT power down to next valid command delay	Max. (7.5ns, 3tCK)			ns
tREFW	Refresh period			32	ms

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Symbol	Description	Min.	Typ.	Max.	Unit
tRFCab	Refresh cycle time	130			ns
tRFCpb	Per bank refresh cycle time	60			ns
tRTP	Internal READ to PRECHARGE command delay	Max. (7.5ns, 4tCK)			ns
tCCD	CAS-to-CAS delay	4			tCK

2.2.4.2 External Memory Interface for LPDDR2

The external memory interface, shown in Figure 2-4. Basic timing parameter for LPDDR3 commands, Figure 2-59 and Figure 2-610, is used to connect LPDDR2 device for MT6735. It includes pins ED_CLK, ED_CLK_B, ECKE, ECS#, EBA[2:0], EDQS[3:0], EDQS#[3:0], EA[9:0] and ED[31:0]. Table 2-10 summarizes the symbol definition and the related timing specifications.

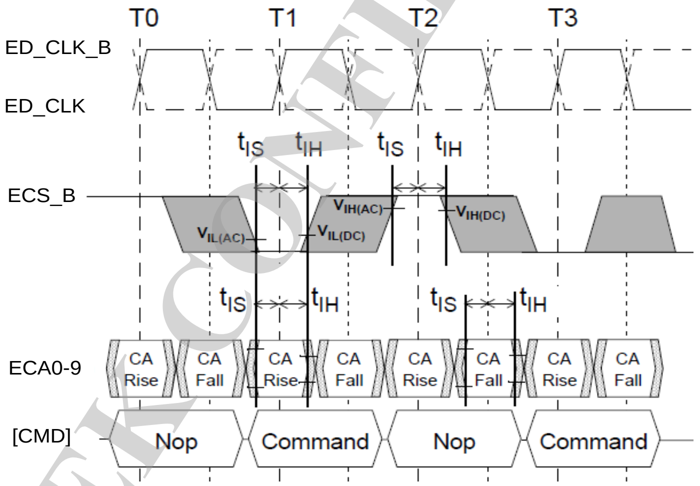

Figure 2-7. Basic timing parameter for LPDDR2 commands

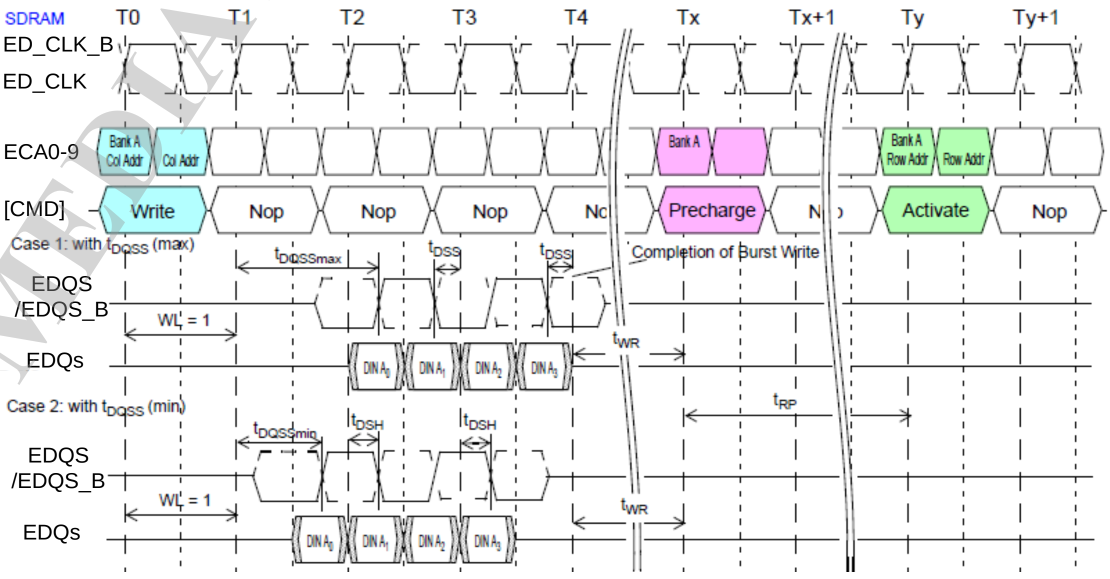

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Figure 2-8. Basic timing parameter for LPDDR2 write

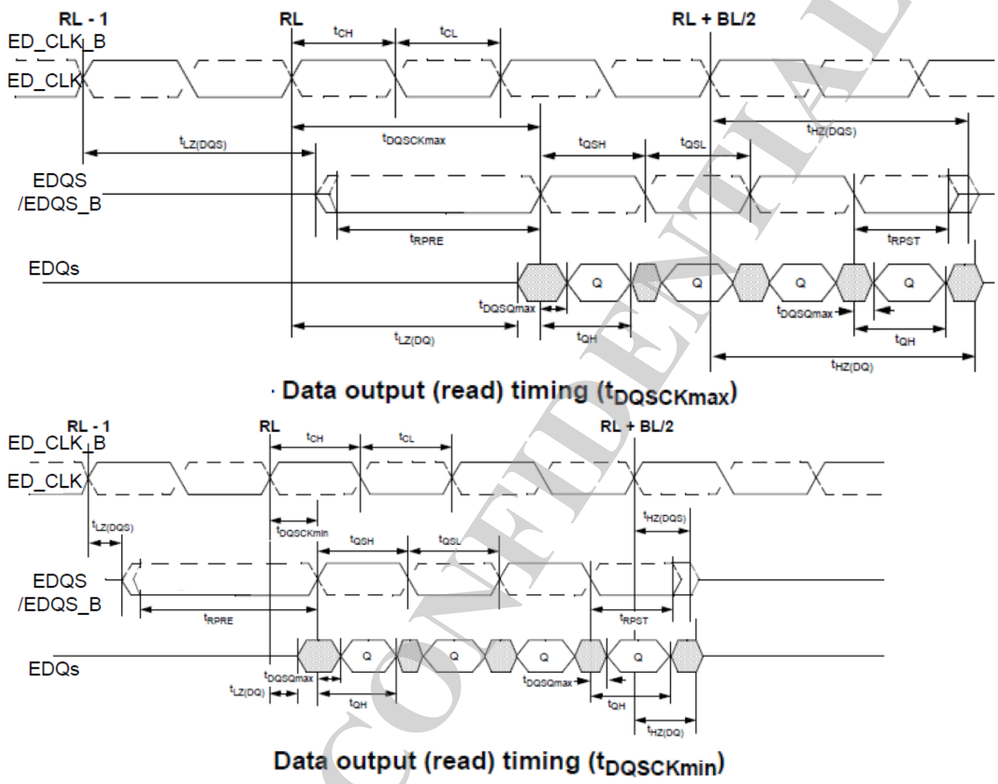

Figure 2-9. Basic timing parameter for LPDDR2 read

Table 2-11. LPDDR2 AC timing parameter table of external memory interface

Symbol	Description	Min.	Typ.	Max.	Unit
tCK	Clock cycle time	3.75		8	ns
tDQSCK	DQS output access time from CK/CK'	2.5		5.5	ns
tCH	Clock high level width	0.45		0.55	tCK
tCL	Clock low level width	0.45		0.55	tCK
tHP	Clock half period	0.45		0.55	tCK
tDS	DQ & DM input setup time	0.43			ns
tDH	DQ & DM input hold time	0.43			ns
tDQSS	Write command to 1st DQS latching transition	0.75		1.25	tCK
tDSS	DQS falling edge to CK setup time	0.2			tCK
tDSH	DQS falling edge hold time from CK	0.2			tCK
tIS	Address & control input setup time	0.46			ns
tIH	Address & control input hold time	0.46			ns
tLZ(DQS)	DQS low-impedance time from CK/CK'	tDQSCK (Min.) – 300			ns
tHZ(DQS)	DQS high-impedance time from CK/CK'	tDQSCK (Max.) –			ns

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Symbol	Description	Min.	Typ.	Max.	Unit
		100			
tLZ(DQ)	DQ low-impedance time from CK/CK'	tDQSCK (Min.) – [1.4*tQHS (Max.)]			ns
tHZ(DQ)	DQ high-impedance time from CK/CK'	tDQSCK (Max.) + [1.4*tDQSQ (Max.)]			ns
tDQSQ	DQS-DQ skew	0.34			ns
tQHP	Data half period	Min. (tQSH, tQSL)			tCK
tQHS	Data hold skew factor	0.4			ns
tQH	DQ/DQS output hold time from DQS	tQHP – tQHS			ns
tDQSH	DQS input high-level width	0.4			tCK
tDQSL	DQS input low-level width	0.4			tCK
tQSH	DQS output high pulse width	tCH – 0.05			tCK
tQSL	DQS output low pulse width	tCL – 0.05			tCK
tMRW	MODE register Write command period	5			tCK
tMRR	MODE register Read command period	2			tCK
tRPRE	Read preamble	0.9		1.1	tCK
tRPST	Read postamble	tCL – 0.05			tCK
tRAS	ACTIVE to PRECHARGE command period	3			tCK
tRC	ACTIVE to ACTIVE command period	6			tCK
tRFC	AUTO REFRESH to ACTIVE/AUTO REFRESH command period	56			tCK
tRCD	ACTIVE to READ or WRITE delay	3			tCK
tRP	PRECHARGE command period	3			tCK
tRRD	ACTIVE bank A to ACTIVE bank B delay	2			tCK
tWR	WRITE recovery time	3			tCK
tWTR	Internal write to READ command time	2			tCK
tXSR	SELF REFRESH exit to the next valid command	40			tCK
tXP	EXIT power-down to the next valid command delay	2			tCK
tCKE	CKE min. pulse width (high & low pulse width)	2			tCK

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2.3 System Configuration

2.3.1 Mode Selection

Table 2-12. Mode selection

Pin name	Description
KCOL0	0: Force USB download mode in bootrom 1: NA (default)

2.3.2 Constant Tie Pins

Table 2-13. Constant tied pins

Pin name	Description
TESTMODE	Test mode (tied to GND)

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2.4 Power-on Sequence

The power-on/off sequence with XTAL is shown in the following figure:

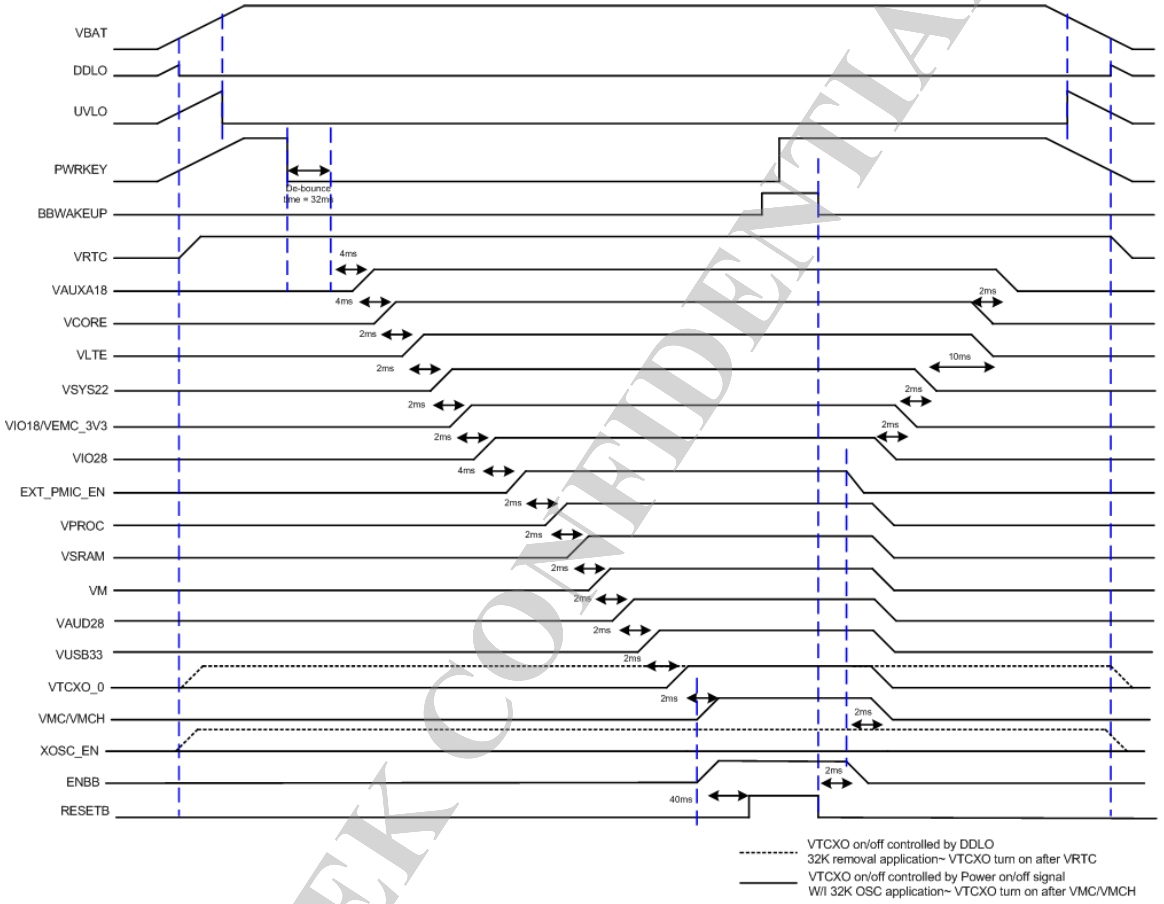

Figure 2-10. Power on/off Sequence by pressing PWRKEY

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2.5 Analog Baseband

2.5.1 Introduction

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are some dedicated interfaces for data transfer. The common control interface translates the APB bus write and read cycle for specific addresses related to analog front-end control. In the write or read of any of these control registers, there is a latency associated with the transfer of data to or from the analog front-end. Dedicated data interface of each analog block is implemented in the corresponding digital block. An analog block includes the following analog functions for the complete GSM/GPRS/WCDMA/LTE/C2K base-band signal processing:

- Base-band Rx: For I/Q channels base-band A/D conversion
- Base-band Tx: For I/Q channels base-band D/A conversion and smoothing filtering
- ETDAC: A DAC output to control buck-converter for envelop tracking technique.
- RF control: Two DACs for automatic power control (APC) is included.The outputs are provided to external RF power amplifiers respectively.
- Auxiliary ADC: Provides an ADC for the battery and other auxiliary analog functions monitoring.
- Clock generation: One clock-squarer for shaping the input sinwave clock and 20 PLLs providing clock signals to base-band TRx, DSP, MCU, USB, MSDC units.

2.5.2 Features

The analog blocks include the following analog functions for complete GSM/GPRS/WCDMA/LTE/C2K base-band signal processing:

- LTE_BBRX
- C2K_BBRX
- LTE_BBTX
- C2K_BBTX
- ETDAC
- APC-DAC
- AUXADC
- Phase locked loop
- Temperature sensor

2.5.3 Block Diagram

2.5.3.1 LTE_BBRX

2.5.3.1.1 Block Descriptions

The receiver (Rx) performs baseband I/Q channels downlink analog-to-digital conversion:

1. Analog input multiplexer: For each channel, a 2-input multiplexer is included.

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2. A/D converter: 4 high performance sigma-delta ADCs perform I/Q digitization for further digital signal processing.

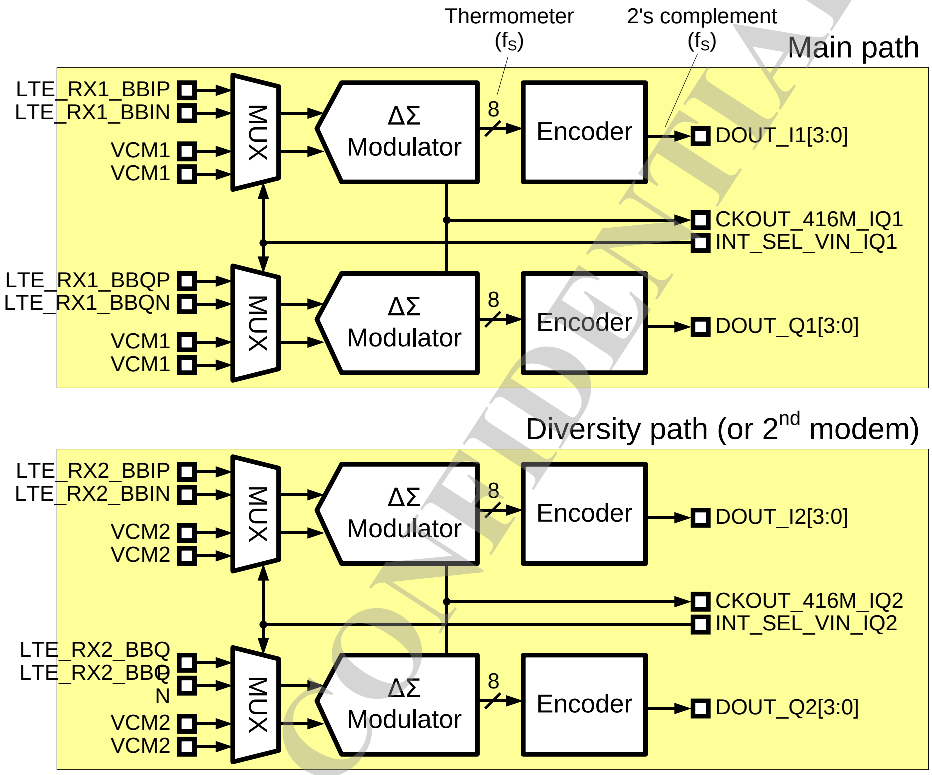

Figure 2-11. Block diagram of LTE_BBRX-ADC

2.5.3.1.2 Functional Specifications

See the table below for the functional specifications of the base-band downlink receiver.

Table 2-14. Baseband downlink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Differential analog input voltage (peak-to-peak)			2.4	V
ICM	Common mode input current magnitude			1	uA
VCM	Common mode input voltage	0.65	0.7	0.75	V
FC	Input clock frequency – Clock rate (LTE HB mode) – Clock rate (LTE LB mode) – Clock rate (DC mode) – Clock rate (SC mode & GSM mode)		416 208 416 208		MHz
	Input clock duty cycle	49.5	50	50.5	%
	Input clock period jitter, DC mode			0.14	% (rms)

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	Input clock period jitter, SC mode & GSM mode			0.61	% (rms)
RIN	Differential input resistance – LTE HB mode – LTE LB mode – DC mode – SC mode & GSM mode	2.8 5.6 5.6 11.2	4 8 8 16	5.2 10.4 10.4 20.8	kΩ
FS	Output sampling rate		416/208		MSPS
VOS	Differential input referred offset			10	mV
SIN	Signal to in-band noise – LTE HB mode, 2.4Vpp (10.2MHz) sinewave, 1kHz ~ 9MHz band – LTE LB mode, 2.4Vpp (5.2MHz) sinewave, 1kHz ~ 4.5MHz band – DC mode, 2.4Vpp (5.2MHz) sinewave, 400kHz ~ 4.6MHz band – SC mode, 2.4Vpp (2.7MHz) sinewave, 1kHz ~ 2.1MHz band – GSM mode: 2.4Vpp(570kHz) sinewave, 70kHz ~ 270kHz band	70 70 72 72 83	73 73 75 75 86		dB dB dB
DVDD18	Digital power supply	1.7	1.8	1.9	V
AVDD18	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption (per channel, 1 ADC) – Power-up – Power-down			4.5 1	mA uA

2.5.3.2 C2K_BBRX

2.5.3.2.1 Block Descriptions

The receiver (Rx) performs baseband I/Q channels downlink analog-to-digital conversion:

1. Analog input multiplexer: For each channel, a 2-input multiplexer is included.
2. A/D converter: 4 high performance sigma-delta ADCs perform I/Q digitization for further digital signal processing.

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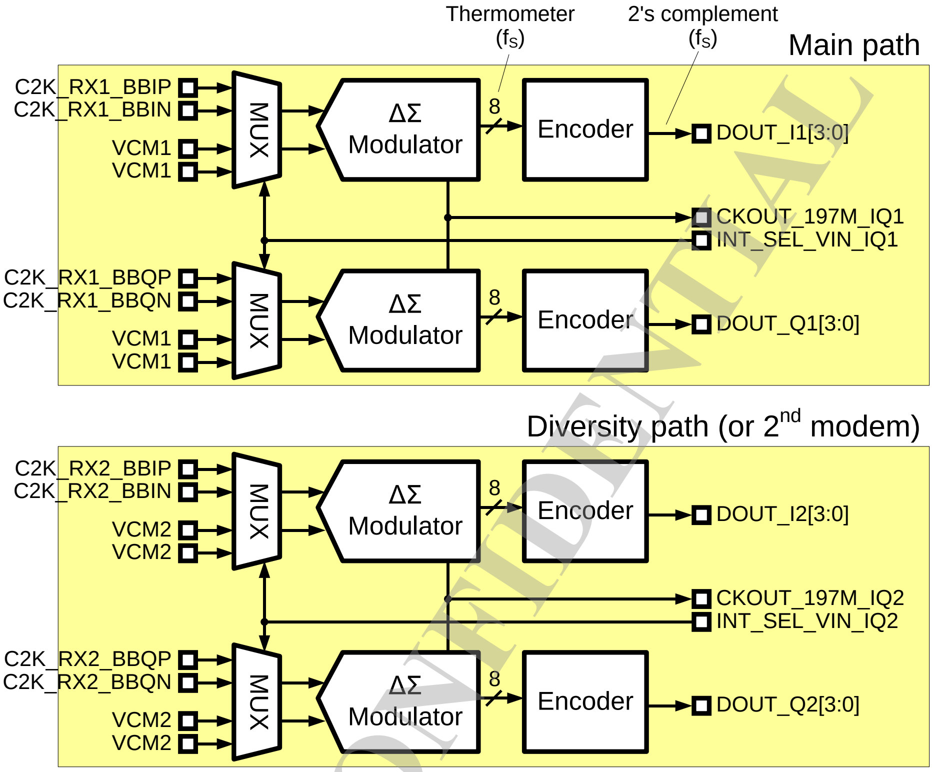

Figure 2-12. Block diagram of C2K_BBRX-ADC

2.5.3.3 Functional Specifications

See the table below for the functional specifications of the base-band downlink receiver.

Table 2-15. Baseband downlink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Differential analog input voltage (peak-to-peak)			2.4	V
ICM	Common mode input current magnitude			1	uA
VCM	Common mode input voltage	0.65	0.70	0.75	V
FC	Clock rate		196.608		MHz
	Input clock duty cycle	49.5	50	50.5	%
	Input clock period jitter			0.61	% (rms)
RIN	Differential input resistance	11.2	16	20.8	kΩ
FS	Output sampling rate		196.608		MSPS
VOS	Differential input referred offset			10	mV
SIN	Signal to in-band noise – 2.4Vpp (1.6MHz) sinewave, 1kKHz ~ 640kHz band	79	82		dB
DVDD18	Digital power supply	1.7	1.8	1.9	V
AVDD18	Analog power supply	1.7	1.8	1.9	V

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Symbol	Parameter	Min.	Typ.	Max.	Unit
T	Operating temperature	−20		80	°C
	Current consumption (per channel, 1 ADC) – Power-up – Power-down			 2 1	 mA uA

2.5.3.4 LTE_BBTX

2.5.3.4.1 Block Descriptions

BBTX includes two channel DACs with the 1st order low pass filter. The DACs are PMOS current-steering topology with NMOS constant sinking current and the active RC filter performs current to voltage buffer.

The bitwidth of DACs is 11-bit which is encoded into 7 bits of thermometer code and 8 binary code by digital hard macro inside BBTX layout. The encoded bits are timing synchronized by D-type flip-flop which is toggled by the analog local clock. The MD-PLL delivers 832MHz differential clock to BBTX. A clock divider translates the 832MHz to 416MHz for DACs and AFIFO inside mixedsys.

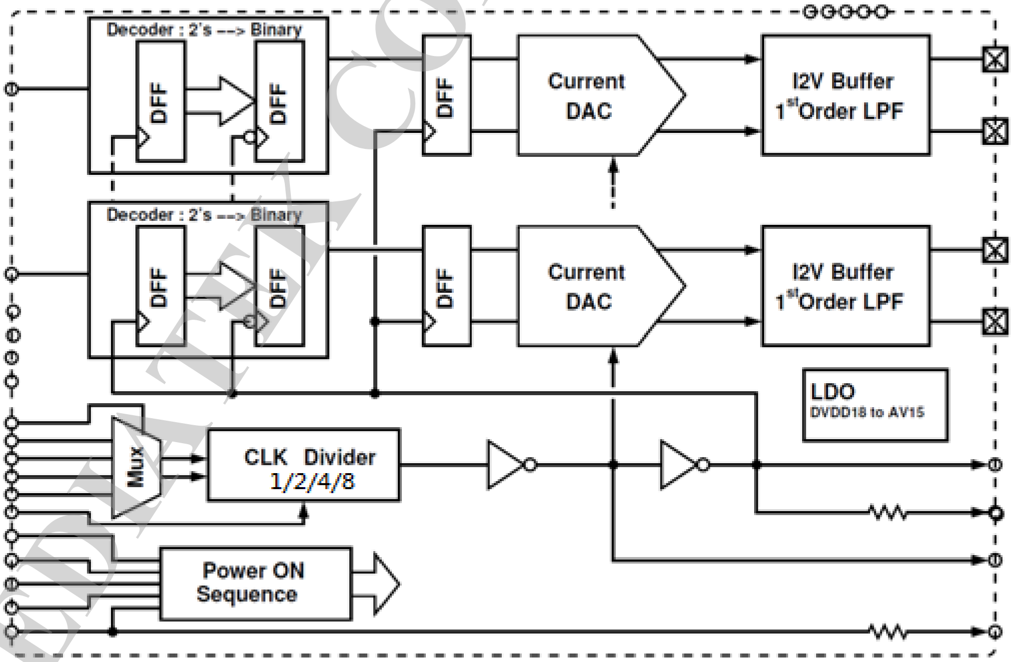

Figure 2-13. Block diagram of LTE_BBTX

2.5.3.4.2 Functional Specifications

Table 2-16. LTE_BBTX specifications

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Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{ocm}	DC output common mode voltage	0.615	0.65	0.685	V
I_K	HF leakage current @ supply, Irms @416*2 = 832MHz			3.5	uA
V_{fs}	DAC output swing		2100		mV
N	DAC resolution		11.0		bit
F_s	Sampling clock		416		MHz
I_{mis}	1-sgma DAC unit cell mismatch			1	%
G_{mis}	3-sigma I/Q gain mismatch	-0.2		0.2	dB
V_{os}	3-sigma output differential DC offset			20	mV
F_{3dB}	3dB corner freq.		20/40		MHz
N_{OOB}	Output noise level @25MHz		40		nVrms/sqrt(Hz)
Dinb	Inband Droop		0.1		dB
DNL			1		LSB
INL			2		LSB
IM3	In-band two-tone test swing V1=V2=290/sqrt(2) mV		-58	-55	dBc
T	Operating temperature	-20		80	°C
	Current consumption – Power-up – Power-down		 6.5 10		 mA uA

2.5.3.5 C2K_BBTX

2.5.3.5.1 Block Descriptions

BBTX includes two channels of DACs with the first order low pass filter. The DACs are PMOS current-steering topology with NMOS constant sinking current, and the active RC filter performs current to the voltage buffer.

The bitwidth of DACs is 10-bit which is encoded into 7 bits of thermometer code and 7 binary code by mixedsys hardware. The encoded bits are timing synchronized by D-type flip-flop which is toggled by the analog local clock. MD-PLL2 deliver 393.216MHz differential clock to BBTX. A clock divider buffered the 393.216MHz to AFIFO inside the mixedsys.

The IO power, DVDD18_MD, is regulated to a voltage around 1.55V to supply analog component, and the required bias currents are generated by BBRX.

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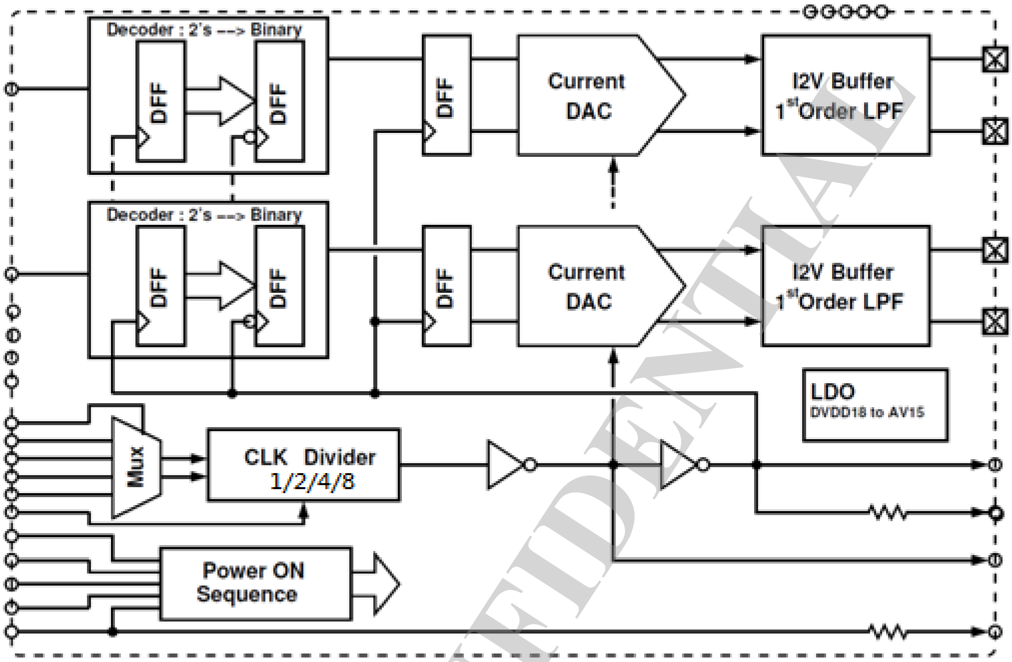

Figure 2-14. Block diagram of C2K_BBTX

2.5.3.5.2 Functional Specifications

Table 2-17. C2K_BBTX specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit.
V_{ocm}	DC output common mode voltage	0.615	0.65	0.685	V
I_K	HF Leakage current @ supply, Irms @416*2=832MHz			3.5	uA
V_{fs}	DAC output swing		2100		mV
N	DAC resolution		10.0		bit
F_s	Sampling clock		393.216		MHz
I_{mis}	1-sgma DAC unit cell mismatch			1	%
G_{mis}	3-sigma I/Q gain mismatch	-0.2		0.2	dB
V_{os_T}	3-sigma output differential DC offset over temp.			4	mV
V_{os}	3-sigma output differential DC offset			10	mV
F_{3dB}	3dB corner freq.	20	25	30	MHz
S_{LPF}	LPF selectivity @832MHz	28			dB
N_{OOB}	Output noise level @45MHz		15.1	30.1.	nVrms/sqrt(Hz)
CN	Signal to noise ratio@45MHz		-146	-140	dBc/Hz
IM3	In-band two-tone test swing V1=V2=290/sqrt(2) mV		-60	-56	dBc
T	Operating temperature	-20		80	°C
	Current consumption				

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Symbol	Parameter	Min.	Typ.	Max.	Unit.
	Power-up Power-down		6.5 10		mA uA

2.5.3.6 ETDAC

2.5.3.6.1 Block Descriptions

The ETDAC (Envelope Tracking DAC) provides analog envelope signal to external ET modulator. It includes:

1. 11-bit D/A converter: Converts digital modulated signals to analog domain. The input to the DAC is sampled at 416MHz rate with the 11-bit resolution.
2. Smoothing filter: The low-pass filter performs smoothing function for DAC output signals with a 20/40MHz 1st-order Butterworth frequency response.

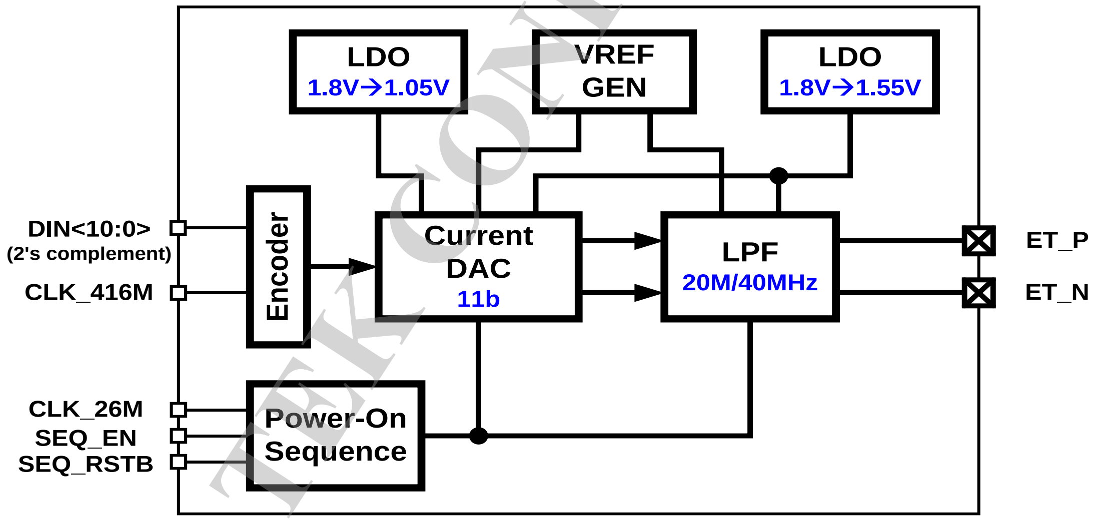

Figure 2-15. Block diagram of ETDAC

2.5.3.6.2 Functional Specfications

Table 2-18. ETDAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		11		Bit
FS	Sampling rate		416		MSPS
IM3	3rd order Intermodulation distortion		-60	-50	dB
	Output swing (full swing)		2		Vppd
VOCM	Output CM voltage	0.6		0.85	V
	Output capacitance (single-ended)			10	PF

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	Output resistance (differential)		100		KΩ
DNL	Differential nonlinearity	-1		+1	LSB
INL	Integral nonlinearity	-2		+2	LSB
FCUT	Filter -3dB cutoff frequency (calibrated)		20/40		MHz
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption – Power-up – Power-down		 4.5 10		 mA uA

2.5.3.7 APC-DAC

2.5.3.7.1 Block Descriptions

See the figure below. APC-DAC is designed to produce a single-ended output signal at APC pin. Two APC-DACs provide two separate output signals (APC1 and APC2).

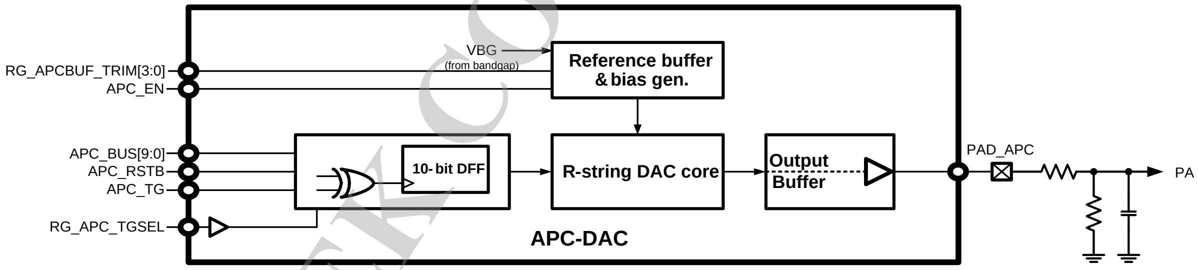

Figure 2-16. Block diagram of APC-DAC (same architecture for two APC-DACs)

2.5.3.7.2 Functional Specifications

See the table below for the functional specifications of the APC-DAC (apply to both APC-DACs).

Table 2-19. APC-DAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
F_S	Clock rate	1.0833		2.1666	MS/s
SNDR	Signal-to-noise-and-distortion ratio (10kHz sine wave with 1.0V swing)		50		dB
T_S	Settling time (99% full-swing settling)			5	us
$V_{O,max}$	Maximum output			AVDD – 0.2	V
C_L	Output loading capacitance		220	2200	pF

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Symbol	Parameter	Min.	Typ.	Max.	Unit
DNL	Differential nonlinearity (code 30 ~ 970)		±1.0		LSB
INL	Integral nonlinearity (code 30 ~ 970)		±2.0		LSB
DVDD	Digital power supply	0.81	1.0	1.1	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	–20		85	°C
I_{ON}	Current consumption (power-on state)		450		uA
I_{OFF}	Current consumption (power-down state)			20	uA

2.5.3.8 AUXADC

2.5.3.8.1 Block Descriptions

The auxiliary ADC includes the following functional blocks:

1. Analog multiplexer: Selects signal from one of the auxiliary input channels. There are 16 input channels of AUXADC. Some are for internal voltage measurement and some for external voltage measurement. Environmental messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
2. 12-bit A/D converter: Converts the multiplexed input signal to 12-bit digital data.

See Table 2-20 for brief descriptions of AUXADC input channels.

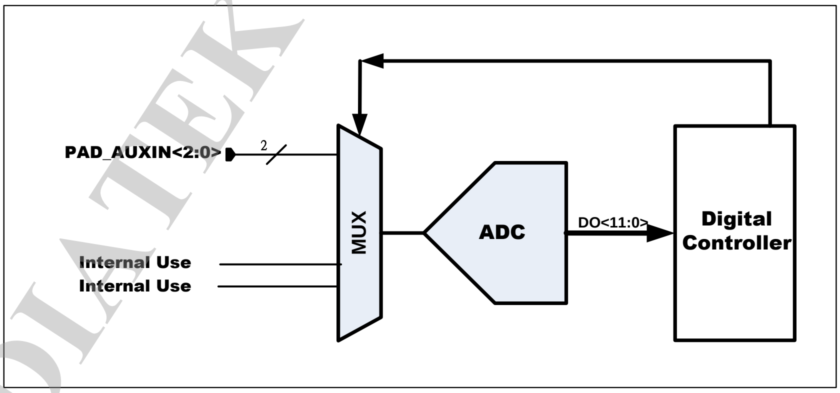

Figure 2-17. Block diagram of AUXADC

Table 2-20. Definitions of AUXADC channels

AUXADC channel ID	Description
Channel 0	External use (AUX_IN0)
Channel 1	External use (AUX_IN1)
Channel 2	NA

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AUXADC channel ID	Description
Channel 3	NA
Channel 4	NA
Channel 5	NA
Channel 6	NA
Channel 7	NA
Channel 8	NA
Channel 9	NA
Channel 10	Internal use
Channel 11	Internal use
Channel 12	External use (AUX_IN2)
Channel 13	NA
Channel 14	NA
Channel 15	NA

2.5.3.8.2 Functional Specifications

See the table below for the functional specifications of auxiliary ADC.

Table 2-21. AUXADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		12		Bit
FC	Clock rate		4		MHz
FS	Sampling rate @ N-Bit		4/(N+4)		MSPS
	Input swing	0.05		1.45	V
CIN	Input capacitance Unselected channel Selected channel		 50 4		 fF pF
RIN	Input resistance Unselected channel	 20			 MΩ
	Clock latency		N+4		1/FC
DNL	Differential nonlinearity		+1.0/-1.0		LSB
INL	Integral nonlinearity		+2.0/-2.0		LSB
SINAD	Signal to noise and distortion ratio (1kHz full swing input & 1.0833MHz clock rate)	62	68		dB
DVDD	Digital power supply	0.81	1.0	1.1	V
AVDD	Analog power supply	1.75	1.8	1.85	V
T	Operating temperature	-20		80	°C
	Current consumption Power-up Power-down		 600 1		 uA uA

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2.5.3.9 Clock Squarer

2.5.3.9.1 Block Descriptions

For most VCXO, the output clock waveform is sinusoidal with too small amplitude (about several hundred mV) to make digital circuits function well. The clock squarer is designed to convert such a small signal to a rail-to-rail clock signal with excellent duty-cycle.

2.5.3.9.2 Functional Specifications

See the table below for the functional specifications of clock squarer.

Table 2-22. Clock squarer specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency	13	26		MHz
Fout	Output clock frequency	13	26		MHz
Vin	Input signal amplitude	350	500	1,000	mVpp
DcycIN	Input signal duty cycle		50		%
DcycOUT	Output signal duty cycle	DcycIN-5		DcycIN+5	%
TR	Rise time on pin CLKSQOUT			5	ns/pF
TF	Fall time on pin CLKSQOUT			5	ns/pF
DVDD	Digital power supply	0.81	1.0	1.1	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		500		uA

2.5.3.10 Phase Locked Loop

2.5.3.10.1 Block Descriptions

There are total 17 PLLs in PLL macro separated into 2 groups, providing several clocks for CPU, BUS, modem, analog modem, MSDC and image-sensor.

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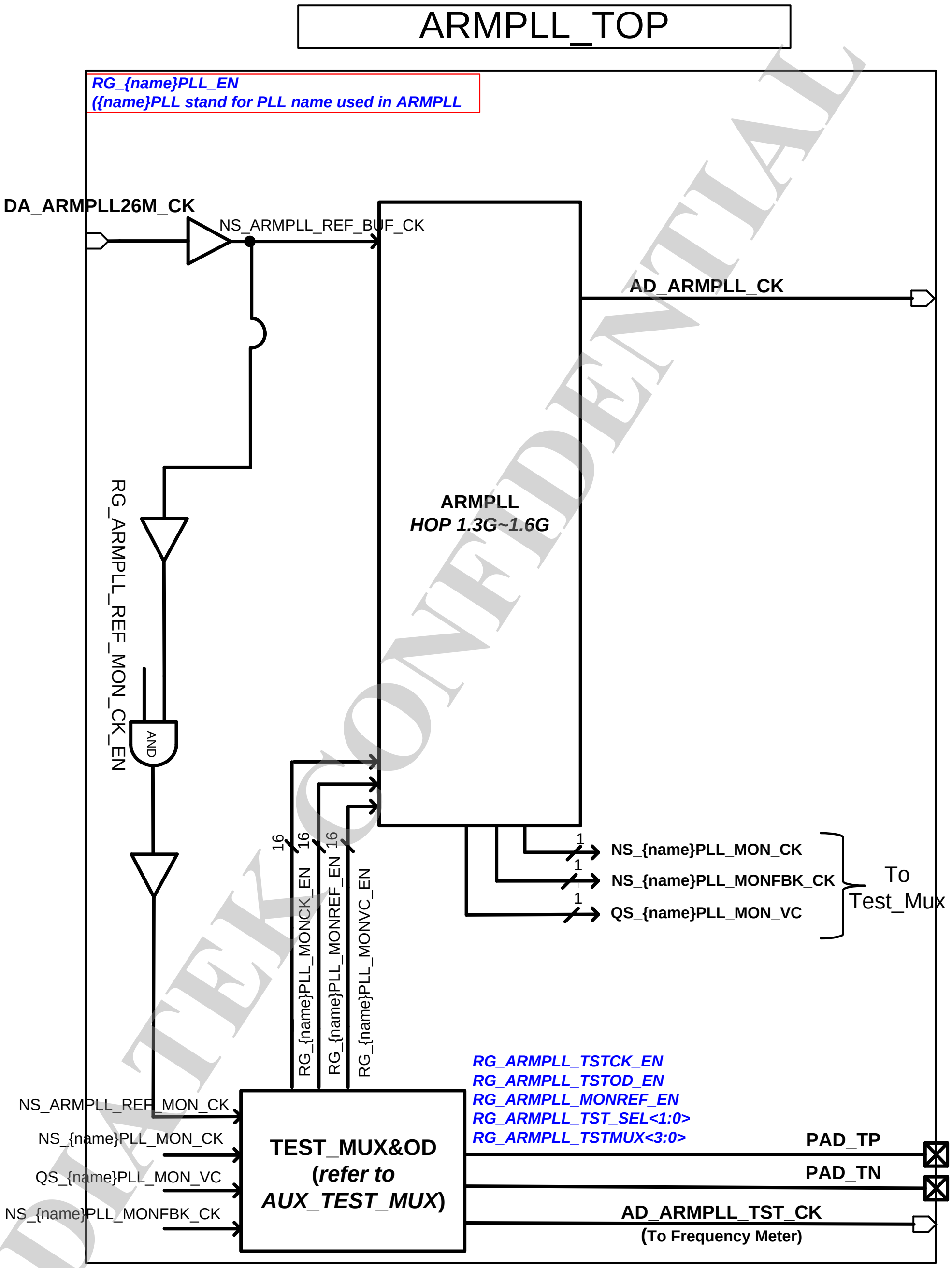

Figure 2-18. Block diagram of ARMPLL

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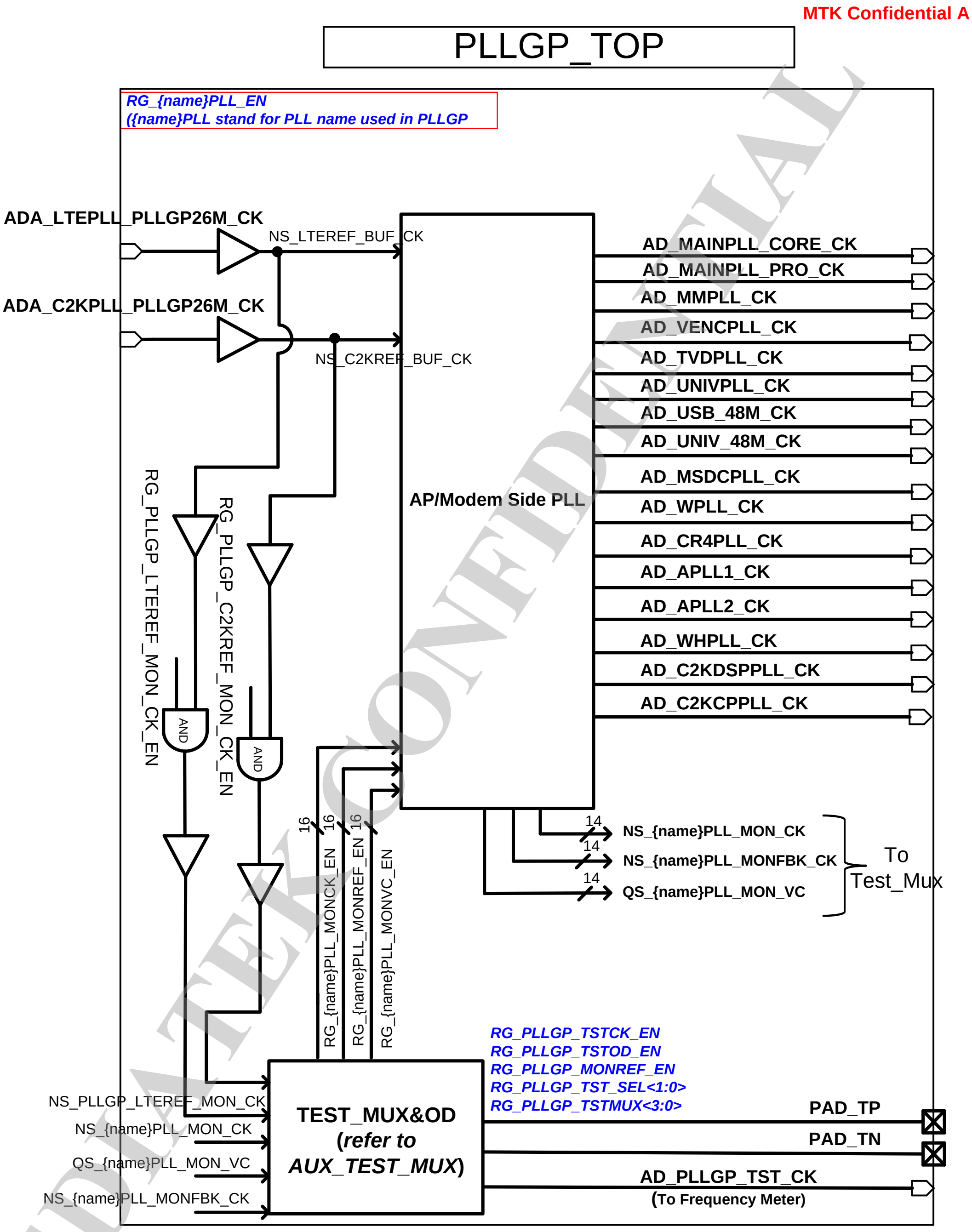

Figure 2-19. Block diagram of PLLGP

2.5.3.10.2 Functional Specifications

See the table below for the functional specifications of PLL.

Table 2-23. ARMPLL specifications

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Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		1300		MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		30		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			1	uA

Table 2-24. MAINPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		1092		MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		30		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			1	uA

Table 2-25. MMPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		450		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-26. UNIVPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz

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Symbol	Parameter	Min.	Typ.	Max.	Unit
Fout	Output clock frequency	N/A	1248	N/A	MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		30		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	℃
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-27. MSDCPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		800		MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	℃
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-28. WPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	491.52	N/A	MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (rms period jitter)		60		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	℃
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-29. WHPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz

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Symbol	Parameter	Min.	Typ.	Max.	Unit
Fout	Output clock frequency	N/A	500.5	N/A	MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (rms period jitter)		60		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-30. C2KCPPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	780	N/A	MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-31. C2KDSPPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		340		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-32. CR4PLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		1196		MHz

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		30		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-33. VENCPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		295.75		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-34. TVDPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		148.5		MHz
	Settling time		20		Us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-35. LTEDSPPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		320		MHz
	Settling time		20		Us

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-36. APLL1 specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		98.304		MHz
	Settling time		20		Us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

2.5.3.11 Temperature Sensor

2.5.3.11.1 Block Descriptions

In order to monitor the temperature of CPUs, several temperature sensors are provided. The temperature sensor is made of substrate BJT in the CMOS process. The voltage output of temperature sensor is measured by AUXADC.

2.5.3.11.2 Functional Specifications

See the table below for the functional specifications of temperature sensor.

Table 2-37. Temperature sensor specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Resolution		0.15		°C
	Temperature range	0		85	°C
	Accuracy	-5		5	°C
	Active current		60		uA

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	Quiescent current		12		uA

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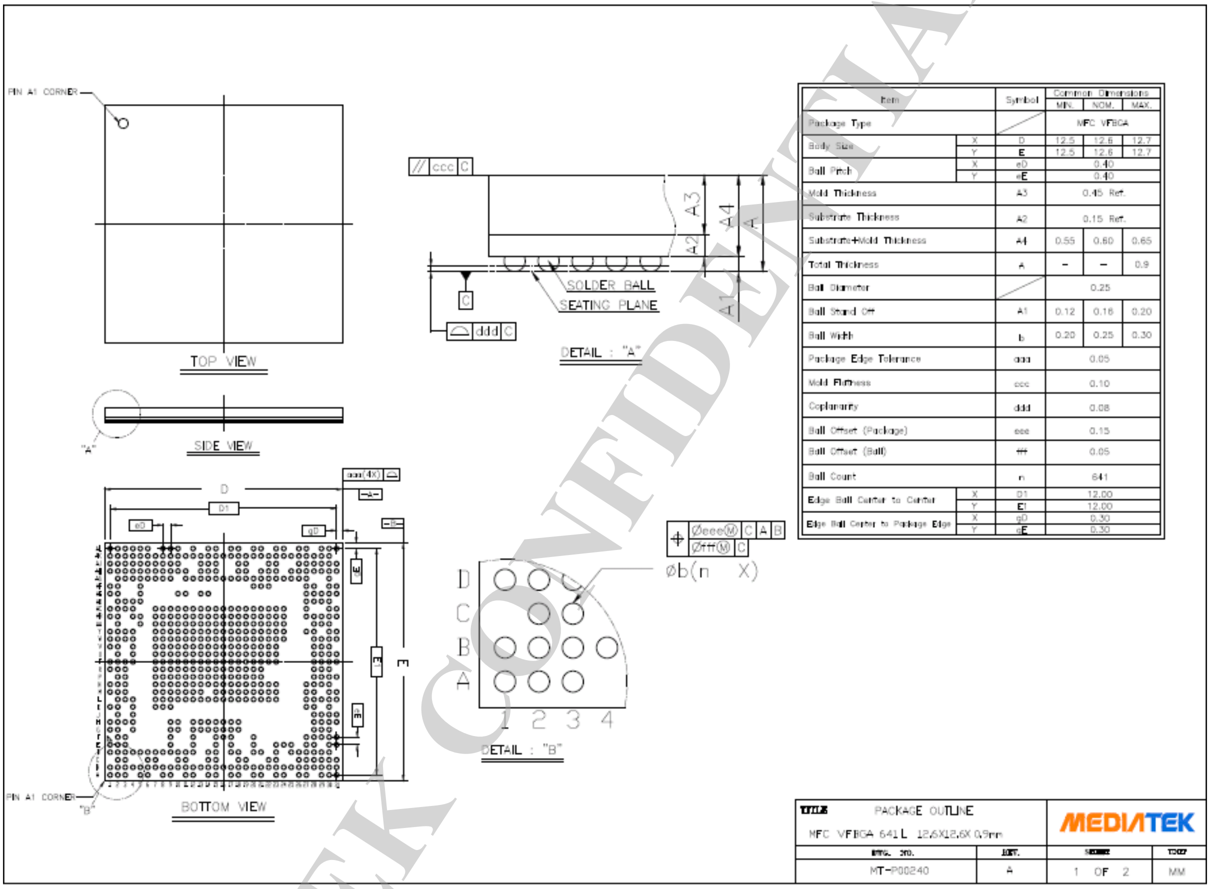
2.6 Package Information

2.6.1 Package Outlines



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type			MFC VFBGA		
Body Size	X	D	12.5	12.6	12.7
	Y	E	12.5	12.6	12.7
Ball Pitch	X	eD	0.40		
	Y	eE	0.40		
Mold Thickness		A3	0.45 Ref.		
Substrate Thickness		A2	0.15 Ref.		
Substrate+Mold Thickness		A4	0.55	0.60	0.65
Total Thickness		A	–	–	0.9
Ball Diameter			0.25		
Ball Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa	0.05		
Mold Flatness		ccc	0.10		
Coplanarity		ddd	0.08		
Ball Offset (Package)		eee	0.15		
Ball Offset (Ball)		fff	0.05		
Ball Count		n	641		
Edge Ball Center to Center	X	D1	12.00		
	Y	E1	12.00		
Edge Ball Center to Package Edge	X	gD	0.30		
	Y	gE	0.30		

Figure 2-20. Outlines and dimensions of VFBGA 12.6mm*12.6mm, 641 balls, 0.4mm pitch package

2.6.2 Thermal Operating Specifications

Table 2-38. Thermal operating specifications

Symbol	Description	Value	Unit	Note
	Max. operating junction temperature	125	°C	
	Package thermal resistances in nature convection	25.46	°C/Watt	

2.6.3 Lead-free Packaging

The chip is provided in a lead-free package and meets RoHS requirements.

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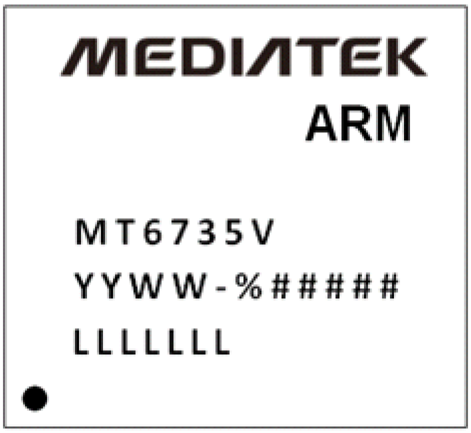
2.7 Ordering Information

2.7.1 Top Marking Definition



- YYWW: Date code
- %: Functional code
- #####: Subcontractor code
- LLLLLLL: Die lot No.

Figure 2-21. Top mark of MT6735

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3 MCU and BUS Fabric

3.1 MCU System

3.1.1 Introduction

MCUSYS is a subsystem responsible for running operating system and application programs in MT6735. It comprises with four Cortex-A53 cores into 1 cluster, and Generic Interrupt Controller (GIC). A 333MHz 128-bit AXI bus is directly connected to External Memory Interface (EMI) to minimize the access latency to DRAM and provide sufficient memory bandwidth. The peripheral system and on-chip storage are bridged through a 273MHz/64-bit AXI bus, and the outstanding capability of AXI protocol allows the system to exploit its maximum throughput from eight CPU cores.

MCUSYS supports DVFS technology which allows CPU to run at different frequency/voltage configurations for different application requirements. When in standby mode, MCUSYS can be completely shut down to further save power consumption and optimize the battery usage on mobile devices.

3.1.2 Features

3.1.2.1 Cluster 0, Cortex-A53 Specifications

- Four-core ARM® Cortex-A53 MPCore™ operating at 1.3GHz
- Supports ARMv8-A architecture for both 32 and 64-bit execution state
- Supports NEON multimedia processing engine with SIMDv2/VFPv4 ISA
- Optionally supports ARMv8 Cryptographic extension
- 32KB L1 I-cache and 32KB L1 D-cache
- 512KB unified L2 cache for CPU cluster
- DVFS technology with adaptive operating voltage from 0.95V to 1.25V
- Supports ARM Jazelle technology

3.1.2.2 Clock Modes Between Clusters and AXI Bus Fabric

The CPU and AXI bus fabric is synchronous and with integer clock ratio for example 1:1/1:2/1:4 for the best system performance. CPU and AXI bus fabric also support Dynamic Clock Management (DCM) mechanism to dynamically turn off the clock when no transactions are on the bus interface. CPU, cluster and AXI bus fabric can also support DVFS technology to lower power consumption.

3.1.3 Interrupt Controller

MT6735 uses ARM GIC400 interrupt controller for interrupt management. GIC400 is embedded inside MCUSYS alongside CCI to minimize the interrupt handling latency. For the interrupt connected

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to GIC400, see the table below for details. The GIC interrupts are separated into 2 categories, the Private Peripheral Interrupts (PPI) and Shared Peripheral Interrupts (SPI). PPI occupies the first 32 interrupt slots in GIC and are banked for each CPU core. SPI begins from the 33rd interrupt and is shared by all CPU cores.

Table 3-1. Interrupt request list for Cortex-A53

GIC ID	Interrupt source/name	Polarity	Trigger type
0	Software generated interrupt 0	H	Edge
1	Software generated interrupt 1	H	Edge
2	Software generated interrupt 2	H	Edge
3	Software generated interrupt 3	H	Edge
4	Software generated interrupt 4	H	Edge
5	Software generated interrupt 5	H	Edge
6	Software generated interrupt 6	H	Edge
7	Software generated interrupt 7	H	Edge
8	Software generated interrupt 8	H	Edge
9	Software generated interrupt 9	H	Edge
10	Software generated interrupt 10	H	Edge
11	Software generated interrupt 11	H	Edge
12	Software generated interrupt 12	H	Edge
13	Software generated interrupt 13	H	Edge
14	Software generated interrupt 14	H	Edge
15	Software generated interrupt 15	H	Edge
16	(Reserved)	-	-
17	(Reserved)	-	-
18	(Reserved)	-	-
19	(Reserved)	-	-
20	(Reserved)	-	-
21	(Reserved)	-	-
22	(Reserved)	-	-
23	(Reserved)	-	-
24	(Reserved)	-	-
25	Virtual maintenance interrupt	L	Level
26	Hypervisor timer event	L	Level
27	Virtual timer event	L	Level
28	Legacy nFIQ	L	Level
29	Secure physical timer event	L	Level
30	Non-secure physical timer event	L	Level
31	Legacy nIRQ	L	Level
32	nIRQOUT[0]	L	Level
33	nIRQOUT[1]	L	Level

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GIC ID	Interrupt source/name	Polarity	Trigger type
34	nIRQOUT[2]	L	Level
35	nIRQOUT[3]	L	Level
40	nPMUIRQ[0]	L	Level
41	nPMUIRQ[1]	L	Level
42	nPMUIRQ[2]	L	Level
43	nPMUIRQ[3]	L	Level
48	nCNTHPIRQ[0]	L	Level
49	nCNTHPIRQ[1]	L	Level
50	nCNTHPIRQ[2]	L	Level
51	nCNTHPIRQ[3]	L	Level
56	nCNTVIRQ[0]	L	Level
57	nCNTVIRQ[1]	L	Level
58	nCNTVIRQ[2]	L	Level
59	nCNTVIRQ[3]	L	Level
64	CNTPSIRQ[0]	H	Level
65	CNTPSIRQ[1]	H	Level
66	CNTPSIRQ[2]	H	Level
67	CNTPSIRQ[3]	H	Level
72	CNTPNSIRQ[0]	H	Level
73	CNTPNSIRQ[1]	H	Level
74	CNTPNSIRQ[2]	H	Level
75	CNTPNSIRQ[3]	H	Level
80	EXTERRIRQ	H	Level
82	mpo_CTIIRQ_sync[0]	H	Level
83	mpo_CTIIRQ_sync[1]	H	Level
84	mpo_CTIIRQ_sync[2]	H	Level
85	mpo_CTIIRQ_sync[3]	H	Level
90	CCI_EVNTCNTOVFL[0]	H	Level
91	CCI_EVNTCNTOVFL[1]	H	Level
92	CCI_EVNTCNTOVFL[2]	H	Level
93	CCI_EVNTCNTOVFL[3]	H	Level
94	CCI_EVNTCNTOVFL[4]	H	Level
95	CCI_ERRORIRQ	H	Level
96	mcu_xgpt_irq[0]	H	Level
97	mcu_xgpt_irq[1]	H	Level
98	mcu_xgpt_irq[2]	H	Level
99	mcu_xgpt_irq[3]	H	Level
100	mcu_xgpt_irq[4]	H	Level
101	mcu_xgpt_irq[5]	H	Level

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GIC ID	Interrupt source/name	Polarity	Trigger type
102	mcu_xgpt_irq[6]	H	Level
103	mcu_xgpt_irq[7]	H	Level
104	usb_mcu_irq_b[0]	L	Level
105	(Reserved)	-	-
106	ts_irq_b	L	Edge
107	ts_batch_irq_b	L	Edge
108	lowbattery_irq_b	L	Edge
109	pwm_irq_b	L	Level
110	therm_ctrl_irq_b	L	Level
111	msdc0_irq_b	L	Level
112	msdc1_irq_b	L	Level
113	msdc2_irq_b	L	Level
114	msdc3_irq_b	L	Level
115	(Reserved)	-	-
116	i2c0_irqb	L	Level
117	i2c1_irqb	L	Level
118	i2c2_irqb	L	Level
119	i2c3_irqb	L	Level
120	(Reserved)	-	-
121	(Reserved)	-	-
122	btif_irq_b	L	Edge
123	uart0_irq_b	L	Level
124	uart1_irq_b	L	Level
125	uart2_irq_b	L	Level
126	uart3_irq_b	L	Level
127	uart4_irq_b	L	Level
128	(Reserved)	-	-
129	dma_irq[0] (HIF0)	L	Level
130	dma_irq[1] (IRDA)	L	Level
131	dma_irq[2] (I2C0)	L	Level
132	dma_irq[3] (I2C1)	L	Level
133	dma_irq[4] (I2C2)	L	Level
134	dma_irq[5] (I2C3)	L	Level
135	dma_irq[6] (uart0_tx)	L	Level
136	dma_irq[7] (uart0_rx)	L	Level
137	dma_irq[8] (uart1_tx)	L	Level

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GIC ID	Interrupt source/name	Polarity	Trigger type
138	dma_irq[9] (uart1_rx)	L	Level
139	dma_irq[10] (uart2_tx)	L	Level
140	dma_irq[11] (uart2_rx)	L	Level
141	dma_irq[12] (uart3_tx)	L	Level
142	dma_irq[13] (uart3_rx)	L	Level
143	dma_irq[14] (uart4_tx)	L	Level
144	dma_irq[15] (uart4_rx)	L	Level
145	dma_irq[16] (btif_tx)	L	Level
146	dma_irq[17] (btif_rx)	L	Level
147	(Reserved)	-	-
148	(Reserved)	-	-
149	disppwm_irq_b	L	Level
150	spi0_irq_b	L	Level
151	msdc0_wakeup_ps_irq	H	Edge
152	msdc1_wakeup_ps_irq	H	Edge
153	msdc2_wakeup_ps_irq	H	Edge
154	msdc3_wakeup_ps_irq	H	Edge
155	irda_irq	H	Level
156	irtx_irq	H	Level
157	ptp_fsm_irq_b	L	Level
158	conn2ap_btif_wakeup_out_b	L	Edge
159	(Reserved)	-	-
160	wdt_irq_b	L	Edge
161	(Reserved)	-	-
162	(Reserved)	-	-
163	(Reserved)	-	-
164	dcc_aparm_irq	L	Level
165	(Reserved)	-	-
166	aparm_domain_irq_b	L	Level
167	aparm_decerr_irq_b	L	Level
168	domain_abort_irq	H	Level
169	bus_dbg_tracker_irq_b	L	Level
170	(Reserved)	-	-
171	ccif1_ap_irq	H	Level
172	ccif0_ap_irq	H	Level
173	trng_irq_b	L	Level
174	(Reserved)	-	-
175	(Reserved)	-	-
176	afe_mcu_irq_b	L	Level

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GIC ID	Interrupt source/name	Polarity	Trigger type
177	cldma_ap_irq	H	Level
178	mmu_irq_b	L	Level
179	mmu_sec_irq_b	L	Level
180	gce_secure_irq_b	L	Level
181	refresh_rate_int_pulse_b	L	Edge
182	gcpu_irq_b	L	Level
183	gce_irq_b	L	Level
184	apxgpt_irq_b	L	Level
185	eint_irq[0](arm_eint_irq)	H	Level
186	eint_event_irq_b	L	Level
187	eint_direct_irq[0]	H	Level
188	eint_direct_irq[1]	H	Level
189	eint_direct_irq[2]	H	Level
190	eint_direct_irq[3]	H	Level
191	(Reserved)	-	-
192	(Reserved)	-	-
193	(Reserved)	-	-
194	(Reserved)	-	-
195	pmic_wrap_err	H	Level
196	kp_irq_b	L	Edge
197	spm_irq_b[0]	L	Level
198	spm_irq_b[1]	L	Level
199	spm_irq_b[2]	L	Level
200	spm_irq_b[3]	L	Level
201	(Reserved)	-	-
202	(Reserved)	-	-
203	(Reserved)	-	-
204	(Reserved)	-	-
205	sej_apxgpt_irq_b	L	Level
206	sej_wdt_irq_b	L	Level
207	(Reserved)	-	-
208	smi_larb0_irq_b	L	Level
209	smi_larb1_irq_b	L	Level
210	smi_larb2_irq_b	L	Level
211	vdec_irq_b	L	Level
212	venc_irq_b	L	Level
213	jpgenc_irq_b	L	Level
214	seninf_irq_b	L	Level
215	cam0_irq_b	L	Level
216	cam1_irq_b	L	Level

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GIC ID	Interrupt source/name	Polarity	Trigger type
217	cam2_irq_b	L	Level
218	disp_mutex_irq_b	L	Level
219	mdp_rdma_irq_b	L	Level
220	mdp_rsz0_irq_b	L	Level
221	mdp_rsz1_irq_b	L	Level
222	mdp_tdshp_irq_b	L	Level
223	mdp_wdma_irq_b	L	Level
224	mdp_wrot_irq_b	L	Level
225	disp_ovl0_irq_b	L	Level
226	disp_rdma0_irq_b	L	Level
227	disp_rdma1_irq_b	L	Level
228	disp_wdma0_irq_b	L	Level
229	disp_color_irq_b	L	Level
230	disp_ccorr_irq_b	L	Level
231	disp_aal_irq_b	L	Level
232	disp_gamma_irq_b	L	Level
233	disp_dither_irq_b	L	Level
234	smi_larb3_irq_b	L	Level
235	dsi0_irq_b	L	Level
236	dpi0_irq_b	L	Level
237	mmsys_top_irq_b	L	Level
238	camsv_irq_b	L	Level
239	camsc_irq1_b	L	Level
240	fdvt_irq_b	L	Level
241	jpgdec_irq_b	L	Level
242	mfg_irq_b[0]	L	Level
243	mfg_irq_b[1]	L	Level
244	mfg_irq_b[2]	L	Level
245	(Reserved)	-	-
246	(Reserved)	-	-
247	(Reserved)	-	-
248	(Reserved)	-	-
249	(Reserved)	-	-
250	(Reserved)	-	-
251	(Reserved)	-	-
252	(Reserved)	-	-
253	md_wdt_irq_b	L	Edge
254	(Reserved)	-	-
255	(Reserved)	-	-
256	(Reserved)	-	-

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GIC ID	Interrupt source/name	Polarity	Trigger type
257	conn_wdt_irq_b	L	Edge
258	wf_hif_int_b	L	Level
259	conn2ap_btif_wakeup_out_b	L	Level
260	bt_cvsd_int_b	L	Level
261	c2k_wdt_irq_b	L	Edge
262	c2k_sdio_host_fn1_int_irq_b	L	Level
263	cirq_event_irq_b	L	Level
264	(Reserved)	-	-
265	(Reserved)	-	-
266	(Reserved)	-	-
267	(Reserved)	-	-
268	(Reserved)	-	-
269	(Reserved)	-	-
270	(Reserved)	-	-
271	(Reserved)	-	-
272	(Reserved)	-	-
273	sec_vio_abort_n	L	Level

3.1.4 Register Definition

This section describes the registers defined in the MCUCFG_REG block in the MCU system.

Module name: mcucfg_reg Base address: (+10200000h)

Address	Name	Width	Register Function
10200620	**INT_POL_CTL0**	32	Interrupt Polarity Control
10200624	**INT_POL_CTL1**	32	Interrupt Polarity Control
10200628	**INT_POL_CTL2**	32	Interrupt Polarity Control
1020062C	**INT_POL_CTL3**	32	Interrupt Polarity Control
10200630	**INT_POL_CTL4**	32	Interrupt Polarity Control
10200634	**INT_POL_CTL5**	32	Interrupt Polarity Control
10200638	**INT_POL_CTL6**	32	Interrupt Polarity Control
1020063C	**INT_POL_CTL7**	32	Interrupt Polarity Control
10200650	**CCI_ADDRMAP**	32	CCI ADDR Map Register
10200654	**CCI_CONFIG**	32	CCI Config Register
10200658	**CCI_PERIPHBASE**	32	CCI Peripheral Base Register
1020065C	**CCI_nEVNTCNTOVFL**	32	CCI Performance Monitor Overflow
10200670	**XGPT_CTL**	32	
10200674	**XGPT_IDX**	32	
10200680	**MCUSYS_REVID**	32	MCUSYS Revision ID
10200684	**MCUSYS_RW_RSVD0**	32	Read and Write Reservation Register 0

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Address	Name	Width	Register Function
10200688	MCUSYS_RW_RSVD1	32	Read and Write Reservation Register 1

10200620 **INT_POL_CTL0** **Interrupt Polarity Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	int_pol_ctl0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	int_pol_ctl0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		int_pol_ctl0	**Controls MCUSYS GIC SPI0~SPI31 polarity** 0: Active high 1: Active low

10200624 **INT_POL_CTL1** **Interrupt Polarity Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	int_pol_ctl1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	int_pol_ctl1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		int_pol_ctl1	**Controls MCUSYS GIC SPI32~SPI63 polarity** 0: Active high 1: Active low

10200628 **INT_POL_CTL2** **Interrupt Polarity Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	int_pol_ctl2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	int_pol_ctl2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
31:0		int_pol_ctl2	**Controls MCUSYS GIC SPI64~SPI95 polarity** 0: Active high 1: Active low

1020062C **INT_POL_CTL3** **Interrupt Polarity Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	int_pol_ctl3[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	int_pol_ctl3[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		int_pol_ctl3	**Controls MCUSYS GIC SPI96~SPI127 polarity** 0: Active high 1: Active low

10200630 **INT_POL_CTL4** **Interrupt Polarity Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	int_pol_ctl4[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	int_pol_ctl4[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		int_pol_ctl4	**Controls MCUSYS GIC SPI128~SPI59 polarity** 0: Active high 1: Active low

10200634 **INT_POL_CTL5** **Interrupt Polarity Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	int_pol_ctl5[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	int_pol_ctl5[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
31:0		int_pol_ctl5	**Controls MCUSYS GIC SPI160~SP191 polarity** 0: Active high 1: Active low

10200638 **INT_POL_CTL6** **Interrupt Polarity Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	int_pol_ctl6[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	int_pol_ctl6[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		int_pol_ctl6	**Controls MCUSYS GIC SPI192~SP223 polarity** 0: Active high 1: Active low

1020063C **INT_POL_CTL7** **Interrupt Polarity Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	int_pol_ctl7[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	int_pol_ctl7[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		int_pol_ctl7	**Controls MCUSYS GIC SPI224~SP255 polarity** 0: Active high 1: Active low

10200650 **CCI_ADDRMAP** **CCI ADDR Map Register** **AAAAAAA0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADDR_MAP15		ADDR_MAP14		ADDR_MAP13		ADDR_MAP12		ADDR_MAP11		ADDR_MAP10		ADDR_MAP9		ADDR_MAP8	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADDR_MAP7		ADDR_MAP6		ADDR_MAP5		ADDR_MAP4		ADDR_MAP3		ADDR_MAP2		ADDR_MAP1		ADDR_MAP0	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	1	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31:30		ADDR_MAP15	**Memory map from 512GB to 1TB**
29:28		ADDR_MAP14	**Memory map from 256GB to 512GB**
27:26		ADDR_MAP13	**Memory map from 128GB to 256GB**
25:24		ADDR_MAP12	**Memory map from 64GB to 128GB**
23:22		ADDR_MAP11	**Memory map from 32GB to 64GB**
21:20		ADDR_MAP10	**Memory map from 16GB to 32GB**
19:18		ADDR_MAP9	**Memory map from 8GB to 16GB**
17:16		ADDR_MAP8	**Memory map from 4GB to 8GB**
15:14		ADDR_MAP7	**Memory map from 3.5GB to 4GB**
13:12		ADDR_MAP6	**Memory map from 3GB to 3.5GB**
11:10		ADDR_MAP5	**Memory map from 2.5GB to 3GB**
9:8		ADDR_MAP4	**Memory map from 2GB to 2.5GB**
7:6		ADDR_MAP3	**Memory map from 1.5GB to 2GB**
5:4		ADDR_MAP2	**Memory map from 1GB to 1.5GB**
3:2		ADDR_MAP1	**Memory map from 0.5GB to 1GB**
1:0		ADDR_MAP0	**Memory map from 0GB to 0.5GB** 00: Map to M0 01: Map to M1 10: Map to M2 11: Map to M1 & M2 interleaved by 4KB

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10200654 CCI_CONFIG CCI Config Register 016000FE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CCI_CONFIG[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CCI_CONFIG[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0

Bit(s)	Mnemonic	Name	Description
31:0		CCI_CONFIG	

10200658 CCI_PERIPH BASE CCI Peripheral Base Register 10300000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CCI_PERIPHBASE[31:16]															
Type	RW															
Reset	0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CCI_PERIPHBASE[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CCI_PERIPHBAS	CCI control register base

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Bit(s)	Mnemonic	Name	Description
		E	

10200 65C **CCI_nEVNTCNTOVFL** **CCI Performance Monitor Overflow** **0000001F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CCI_nEVENTCNTOVERFLOW				
Type												RO				
Reset												1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
4:0		CCI_nEVENTCNTOVERFLOW	**CCI event counter overflow bit** 1'b0: Overflow 1'b1: Not overflow bit0: cci_nevent_cnt0 bit1: cci_nevent_cnt1 bit2: cci_nevent_cnt2 bit3: cci_nevent_cnt3 bit4: cci_nevent_cnt4

10200670 **XGPT_CTL** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	XGPT_CTL[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XGPT_CTL[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		XGPT_CTL	

10200674 **XGPT_IDX** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					XGPT_IDX											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
11:0		XGPT_IDX	**XGPT control index register** 12'h000: CPUXGPT control register [10:8] : ckmode, 3'b100: 26MHz/4, 3'b010: 26MHz/2, 3'b001: 26MHz [1]: Halt-on-debug enable bit [0]: XGPT enable bit 12'h004: CPUXGPT status register (RO) 12'h008(L)~12'h00C(H): XGPT counter value initialization register. Update when 12'h008 is programmed. 12'h030: XGPT IRQ Mask [7:0] register 12'h034(L)~12'h038(H): XGPT interrupt CNT0 register. Update when 12'h034 is programmed. 12'h03C(L)~12'h040(H): XGPT interrupt CNT1 register. Update when 12'h03C is programmed. 12'h044(L)~12'h048(H): XGPT interrupt CNT2 register. Update when 12'h044 is programmed. 12'h04C(L)~12'h050(H): XGPT interrupt CNT3 register. Update when 12'h04C is programmed. 12'h054(L)~12'h058(H): XGPT interrupt CNT4 register. Update when 12'h054 is programmed. 12'h05C(L)~12'h060(H): XGPT interrupt CNT5 register. Update when 12'h05C is programmed. 12'h064(L)~12'h068(H): XGPT interrupt CNT6 register. Update when 12'h064 is programmed. 12'h06C(L)~12'h070(H): XGPT interrupt CNT7 register. Update when 12'h06C is programmed. 12'h074(L)~12'h078(H): Current 64-bit XGPT timer counting value

10200680 **MCUSYS_REVID** **MCUSYS Revision ID** **00000101**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**mcusys_platfrom_info**				**mcusys_platfrom_version**				**mcusys_platfrom_revision**							
Type	RU				RU				RU							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
15:12		mcusys_platfrom_info	4'b0000: Single-little 4'b0001: Dual-little 4'b0010: Single-big 4'b0011: Dual-big 4'b0100: Big-little
11:8		mcusys_platfrom_version	Platform version
7:0		mcusys_platfrom_revision	Platform revision

10200684 **MCUSYS_RW_RSVD0** **Read and Write Reservation Register 0** **00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	mcusys_rw_rsvd0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mcusys_rw_rsvd0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		mcusys_rw_rsvd0	MCUSYS reserved read/write register 0

10200688 **MCUSYS_RW_RSVD1** **Read and Write Reservation Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	mcusys_rw_rsvd1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mcusys_rw_rsvd1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		mcusys_rw_rsvd1	MCUSYS reserved read/write register 1

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3.2 On-chip Memory Controller

3.2.1 Introduction

The on-chip memory controller provides the boot ROM and SRAM resources.

3.2.2 Features

The memory controller has the following features

- 64KB on-chip ROM, with memory access protection and detection
- 64 KB on-chip SRAM, with memory access protection and detection
- 256 KB L2 share SRAM
- Chip ID

The following table is the memory map of on-chip ROM and SRAM.

Table 3-2. Memory map of on-chip memory controller

Bank	Start address	End address	Size	Device
0	0x0000_0000	0x0000_FFFF	64KB	ROM
	0x0010_0000	0x0010_FFFF	64KB	SRAM
	0x0020_0000	0x0023_FFFF	256KB	L2 Share SRAM

3.2.3 Block Diagram

The on-chip memory controller consists of a SRAM controller, a ROM controller, an AXI-FPC bus bridge, a bus interface unit, setting register and chip ID unit (see Figure 3-1). Detailed functionality is described in the following sections.

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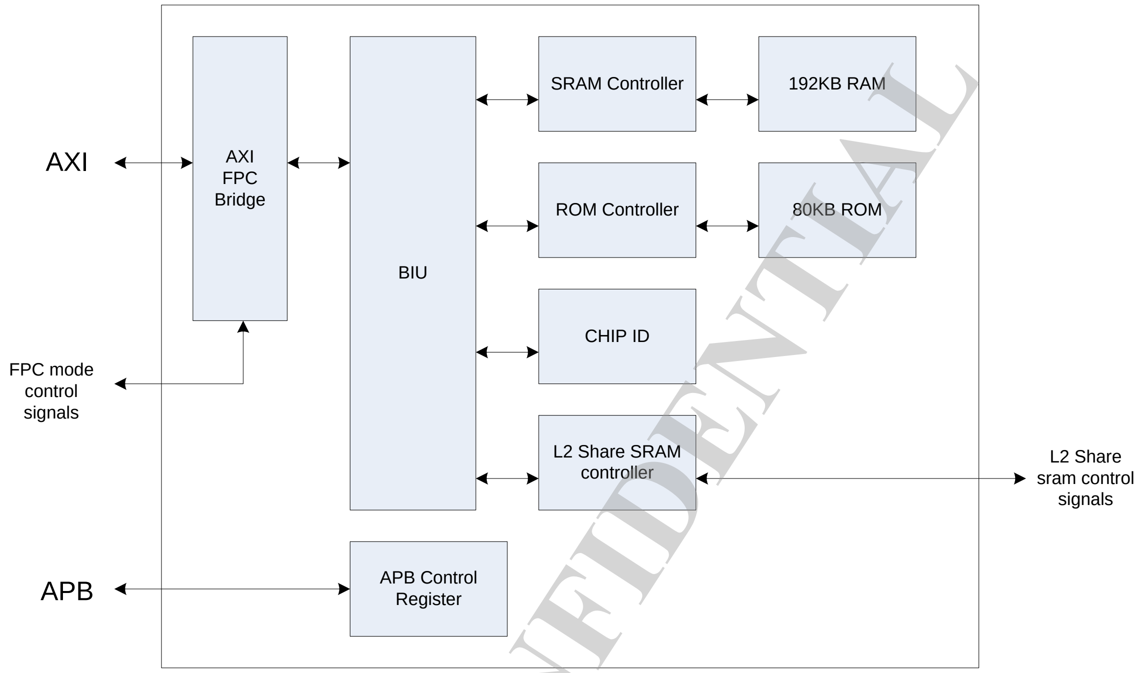

Figure 3-1. Block diagram of on-chip memory controller

3.2.3.1 BOOT ROM Power Down Mode

Boot ROM power down mode is used in the following scenarios:

1. After system boot, boot ROM will be powered down and prevented from any probe of ROM content
2. In MCDI (multi-core-deep-idle), it is the bootstrap for suspend/resume CPU.

The power down mode can be entered by setting *SRAMROM_SEC_CTRL.sramrom_sw_rom_pd* = 1. The bus interface unit will return a far jump instruction when receiving the read transactions. The jump address can be configurable by the *SRAMROM_BOOT_ADDR* register.

3.2.3.2 BOOT ROM FPC Mode

Boot ROM FPC mode is mainly used in Function Pattern mode. When the chip is trapped into FPC mode, the AXI-FPC bridge will block all the transactions to ROM address by returning a far jump instruction, with jump address specified in SRAMROM_FPC_BOOT_ADDR. The default value of SRAMROM_FPC_BOOT_ADDR is 0. The AXI-FPC bridge will automatically unblock the transaction when the FPC program is downloaded to SRAM memory address space.

3.2.3.3 On-Chip SRAM Security Protection

The on-chip SRAM can be partitioned into 2 regions with different security protection configurations. The bus interface unit performs permission check based on the settings, records the first violated

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address in the *SEC_VIO_ADDR* register and issues interrupts to the host processor. The violation interrupt can be cleared by a write to *SEC_VIO_ACK*.

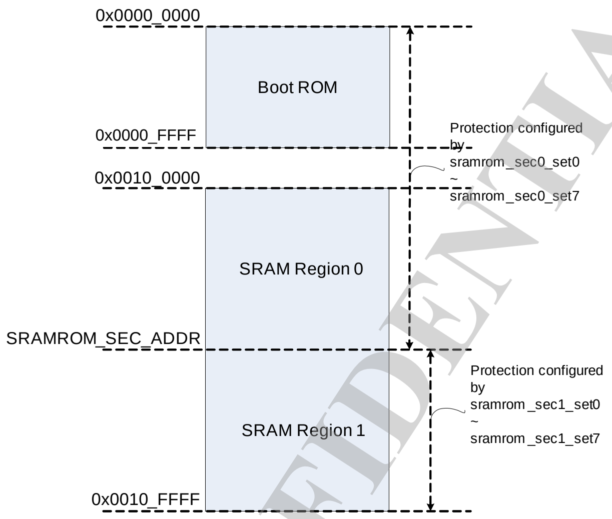

Figure 3-2. Security memory protection scheme

3.2.4 Register Definition

Module name: sramrom Base address: (+10202000h)

Address	Name	Width	Register Function
10202010	**SEC_VIO_STAT**	32	Security Violation Status Register
10202014	**SEC_VIO_ADDR**	32	Security Violation Address Register
10202018	**SEC_VIO_ACK**	32	Security Violation Acknowledge Register
10202020	**PWR_CTRL**	32	PWR_CTRL
10202034	**BOOT_META0**	32	META Data Register 0
10202038	**BOOT_META1**	32	META Data Register 1
1020203C	**BOOT_META2**	32	META Data Register 2
10202040	**BOOT_META3**	32	META Data Register 3
10202050	**BOOT_META_NR0**	32	Non-resettable META Data Register 0
10202054	**BOOT_META_NR1**	32	Non-resettable META Data Register 1
10202058	**BOOT_META_NR2**	32	Non-resettable META Data Register 2
1020205C	**BOOT_META_NR3**	32	Non-resettable META Data Register 3

10202010 SEC_VIO_STAT Security Violation Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sec_vio_						sec_vio_domain									

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	rw															
Type	RO						RO									
Reset	0						0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																sec_vio
Type																RO
Reset																0

Bit(s)	Mnemonic	Name	Description
31		sec_vio_rw	**Indicates the direction of transaction which violates security setting** 0: Read 1: Write
25:24		sec_vio_domain	**Indicates the domain of transaction which violates security setting** 00: Domain 0 01: Domain 1 10: Domain 2 11: Reserved
0		sec_vio	**Indicates a security violation occurs in accessing on-chip SRAM/ROM** 0: Normal 1: Security violation IRQ pending

10202014 SEC_VIO_ADDR Security Violation Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sec_vio_addr[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sec_vio_addr[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		sec_vio_addr	Address of the transaction which violates security setting

10202018 SEC_VIO_ACK Security Violation Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sec_vio_ack[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sec_vio_ack[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		sec_vio_ack	A write to this register will clear sec_vio bit in SEC_VIO_STAT.

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10202020 PWR_CTRL PWR_CTRL 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																rom_swrst_B
Type																RW
Reset																1

Bit(s)	Mnemonic	Name	Description
0		rom_swrst_B	**This bit is to control SW reset or not.** 0: SW reset 1: No SW reset

10202034 BOOT_META0 META Data Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_meta0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_meta0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_meta0	**Meta data register** General purpose register for boot-up. Can be reset by WDT reset.

10202038 BOOT_META1 META Data Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_meta1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_meta1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_meta1	**Meta data register** General purpose register for boot-up. Can be reset by WDT reset.

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1020203C **BOOT_META2** **META Data Register 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_meta2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_meta2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_meta2	**Meta data register** General purpose register for boot-up. Can be reset by WDT reset.

10202040 **BOOT_META3** **META Data Register 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_meta3[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_meta3[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_meta3	**Meta data register** General purpose register for boot-up. Can be reset by WDT reset.

10202050 **BOOT_META_NR0** **Non-resettable META Data Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_meta_nr0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_meta_nr0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_meta_nr0	**Meta data register** General purpose register for boot-up. Can only be reset by HW reset; cannot be reset by WDT reset.

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10202054 BOOT_META_NR1 Non-resettable META Data Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_meta_nr1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_meta_nr1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_meta_nr1	**Meta data register** General purpose register for boot-up. Can only be reset by HW reset; cannot be reset by WDT reset.

10202058 BOOT_META_NR2 Non-resettable META Data Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_meta_nr2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_meta_nr2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_meta_nr2	**Meta data register** General purpose register for boot-up. Can only be reset by HW reset; cannot be reset by WDT reset.

1020205C BOOT_META_NR3 Non-resettable META Data Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_meta_nr3[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_meta_nr3[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_meta_nr3	**Meta data register** General purpose register for boot-up. Can only be reset by HW reset; cannot be reset by WDT reset.

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3.3 External Interrupt Controller

3.3.1 Introduction

The external interrupt controller (EINTC) processes all off-chip interrupt sources and forwards interrupt request signals to AP MCU.

3.3.2 Features

EINTC supports up to 213 external interrupt signals and performs the following processes to the interrupt signals coming from external sources:

- Polarity inversion
- Edge/level trigger selection
- De-bounce with a configurable 32kHz clock (optional)

According to the register configuration, the external interrupt source will be forwarded to the Cortex-A7 built-in interrupt controller with different IRQ signals, eint_irq or eint_direct_irq. EINTC generates wakeup events to AP MCU.

3.3.3 Block Diagram

Figure 3-3 is the block diagram of the external interrupt controller in MT6735. Every functional block is controlled by the corresponding control registers defined in next section.

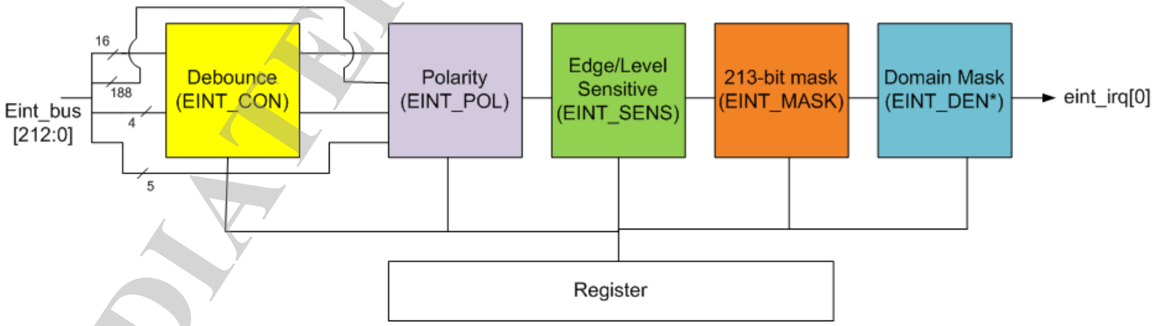

Figure 3-3. Block diagram of external interrupt controller

Normally the external interrupt source goes through the de-bounce unit which is driven by 32kHz clock and triggers the corresponding CPU with eint_irq. Therefore, the minimum latency from eint_bus to eint_irq is 30.52µs.

The following tables list the signal connections to the interrupt controller of CPU.

Table 3-3. External interrupt request signal connection

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IRQ name	AP MCU INTC
eint_irq[0]	IRQ[185]
eint_event_b	IRQ[186]
deint_irq[0]	IRQ[187]
deint_irq[1]	IRQ[188]
deint_irq[2]	IRQ[189]
deint_irq[3]	IRQ[190]

Table 3-4. Definitions of domains

Domain number	Target CPU/DSP
0	Application CPU

3.3.4 Register Definition

Module name: ap_cirq_eint Base address: (+10005000h)

Address	Name	Width	Register Function
10005000	EINT_STA0	32	External Interrupt Status Register
10005004	EINT_STA1	32	External Interrupt Status Register
10005008	EINT_STA2	32	External Interrupt Status Register
1000500C	EINT_STA3	32	External Interrupt Status Register
10005010	EINT_STA4	32	External Interrupt Status Register
10005014	EINT_STA5	32	External Interrupt Status Register
10005018	EINT_STA6	32	External Interrupt Status Register
10005040	EINT_ACK0	32	External Interrupt Acknowledge Register
10005044	EINT_ACK1	32	External Interrupt Acknowledge Register
10005048	EINT_ACK2	32	External Interrupt Acknowledge Register
1000504C	EINT_ACK3	32	External Interrupt Acknowledge Register
10005050	EINT_ACK4	32	External Interrupt Acknowledge Register
10005054	EINT_ACK5	32	External Interrupt Acknowledge Register
10005058	EINT_ACK6	32	External Interrupt Acknowledge Register
10005080	EINT_MASK0	32	External Interrupt Mask Register
10005084	EINT_MASK1	32	External Interrupt Mask Register
10005088	EINT_MASK2	32	External Interrupt Mask Register
1000508C	EINT_MASK3	32	External Interrupt Mask Register
10005090	EINT_MASK4	32	External Interrupt Mask Register
10005094	EINT_MASK5	32	External Interrupt Mask Register
10005098	EINT_MASK6	32	External Interrupt Mask Register
100050C0	EINT_MASK_SET0	32	External Interrupt Mask Set Register
100050C4	EINT_MASK_SET1	32	External Interrupt Mask Set Register
100050C8	EINT_MASK_SET2	32	External Interrupt Mask Set Register
100050CC	EINT_MASK_SET3	32	External Interrupt Mask Set Register
100050D0	EINT_MASK_SET4	32	External Interrupt Mask Set Register
100050D4	EINT_MASK_SET5	32	External Interrupt Mask Set Register

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Address	Name	Width	Register Function
100050D8	EINT_MASK_SET6	32	External Interrupt Mask Set Register
10005100	EINT_MASK_CLR0	32	External Interrupt Mask Set Register
10005104	EINT_MASK_CLR1	32	External Interrupt Mask Set Register
10005108	EINT_MASK_CLR2	32	External Interrupt Mask Set Register
1000510C	EINT_MASK_CLR3	32	External Interrupt Mask Set Register
10005110	EINT_MASK_CLR4	32	External Interrupt Mask Set Register
10005114	EINT_MASK_CLR5	32	External Interrupt Mask Set Register
10005118	EINT_MASK_CLR6	32	External Interrupt Mask Set Register
10005140	EINT_SENS0	32	External Interrupt Sensitivity Register
10005144	EINT_SENS1	32	External Interrupt Sensitivity Register
10005148	EINT_SENS2	32	External Interrupt Sensitivity Register
1000514C	EINT_SENS3	32	External Interrupt Sensitivity Register
10005150	EINT_SENS4	32	External Interrupt Sensitivity Register
10005154	EINT_SENS5	32	External Interrupt Sensitivity Register
10005158	EINT_SENS6	32	External Interrupt Sensitivity Register
10005180	EINT_SENS_SET0	32	External Interrupt Sensitivity Set Register
10005184	EINT_SENS_SET1	32	External Interrupt Sensitivity Set Register
10005188	EINT_SENS_SET2	32	External Interrupt Sensitivity Set Register
1000518C	EINT_SENS_SET3	32	External Interrupt Sensitivity Set Register
10005190	EINT_SENS_SET4	32	External Interrupt Sensitivity Set Register
10005194	EINT_SENS_SET5	32	External Interrupt Sensitivity Set Register
10005198	EINT_SENS_SET6	32	External Interrupt Sensitivity Set Register
100051C0	EINT_SENS_CLR0	32	External Interrupt Sensitivity Clear Register
100051C4	EINT_SENS_CLR1	32	External Interrupt Sensitivity Clear Register
100051C8	EINT_SENS_CLR2	32	External Interrupt Sensitivity Clear Register
100051CC	EINT_SENS_CLR3	32	External Interrupt Sensitivity Clear Register
100051D0	EINT_SENS_CLR4	32	External Interrupt Sensitivity Clear Register
100051D4	EINT_SENS_CLR5	32	External Interrupt Sensitivity Clear Register
100051D8	EINT_SENS_CLR6	32	External Interrupt Sensitivity Clear Register
10005200	EINT_SOFT0	32	Software Interrupt Register
10005204	EINT_SOFT1	32	Software Interrupt Register
10005208	EINT_SOFT2	32	Software Interrupt Register
1000520C	EINT_SOFT3	32	Software Interrupt Register
10005210	EINT_SOFT4	32	Software Interrupt Register
10005214	EINT_SOFT5	32	Software Interrupt Register
10005218	EINT_SOFT6	32	Software Interrupt Register
10005240	EINT_SOFT_SET0	32	Software Interrupt Set Register
10005244	EINT_SOFT_SET1	32	Software Interrupt Set Register
10005248	EINT_SOFT_SET2	32	Software Interrupt Set Register
1000524C	EINT_SOFT_SET3	32	Software Interrupt Set Register
10005250	EINT_SOFT_SET4	32	Software Interrupt Set Register
10005254	EINT_SOFT_SET5	32	Software Interrupt Set Register
10005258	EINT_SOFT_SET6	32	Software Interrupt Set Register
10005280	EINT_SOFT_CLR0	32	Software Interrupt Clear Register
10005284	EINT_SOFT_CLR1	32	Software Interrupt Clear Register
10005288	EINT_SOFT_CLR2	32	Software Interrupt Clear Register

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Address	Name	Width	Register Function
1000528C	EINT_SOFT_CLR3	32	Software Interrupt Clear Register
10005290	EINT_SOFT_CLR4	32	Software Interrupt Clear Register
10005294	EINT_SOFT_CLR5	32	Software Interrupt Clear Register
10005298	EINT_SOFT_CLR6	32	Software Interrupt Clear Register
10005300	EINT_POL0	32	External Interrupt Polarity Register
10005304	EINT_POL1	32	External Interrupt Polarity Register
10005308	EINT_POL2	32	External Interrupt Polarity Register
1000530C	EINT_POL3	32	External Interrupt Polarity Register
10005310	EINT_POL4	32	External Interrupt Polarity Register
10005314	EINT_POL5	32	External Interrupt Polarity Register
10005318	EINT_POL6	32	External Interrupt Polarity Register
10005340	EINT_POL_SET0	32	External Interrupt Polarity Set Register
10005344	EINT_POL_SET1	32	External Interrupt Polarity Set Register
10005348	EINT_POL_SET2	32	External Interrupt Polarity Set Register
1000534C	EINT_POL_SET3	32	External Interrupt Polarity Set Register
10005350	EINT_POL_SET4	32	External Interrupt Polarity Set Register
10005354	EINT_POL_SET5	32	External Interrupt Polarity Set Register
10005358	EINT_POL_SET6	32	External Interrupt Polarity Set Register
10005380	EINT_POL_CLR0	32	External Interrupt Polarity Clear Register
10005384	EINT_POL_CLR1	32	External Interrupt Polarity Clear Register
10005388	EINT_POL_CLR2	32	External Interrupt Polarity Clear Register
1000538C	EINT_POL_CLR3	32	External Interrupt Polarity Clear Register
10005390	EINT_POL_CLR4	32	External Interrupt Polarity Clear Register
10005394	EINT_POL_CLR5	32	External Interrupt Polarity Clear Register
10005398	EINT_POL_CLR6	32	External Interrupt Polarity Clear Register
10005400	EINT_D0EN0	32	Domain 0 External Interrupt Enable Control Register
10005404	EINT_D0EN1	32	Domain 0 External Interrupt Enable Control Register
10005408	EINT_D0EN2	32	Domain 0 External Interrupt Enable Control Register
1000540C	EINT_D0EN3	32	Domain 0 External Interrupt Enable Control Register
10005410	EINT_D0EN4	32	Domain 0 External Interrupt Enable Control Register
10005414	EINT_D0EN5	32	Domain 0 External Interrupt Enable Control Register
10005418	EINT_D0EN6	32	Domain 0 External Interrupt Enable Control Register
10005500	EINT_DBNC_3_0	32	External Interrupt Debounce Control Register
10005504	EINT_DBNC_7_4	32	External Interrupt Debounce Control Register
10005508	EINT_DBNC_B_8	32	External Interrupt Debounce Control Register
1000550C	EINT_DBNC_F_C	32	External Interrupt Debounce Control Register
100055CC	EINT_DBNC_C_F_C	32	External Interrupt Debounce Control Register
10005600	EINT_DBNC_SET_3_0	32	External Interrupt Debounce Control Register
10005604	EINT_DBNC_SET_7_4	32	External Interrupt Debounce Control Register
10005608	EINT_DBNC_SET_B_8	32	External Interrupt Debounce Control Register
1000560C	EINT_DBNC_SET_F_C	32	External Interrupt Debounce Control Register
100056CC	EINT_DBNC_SET_C_F_C	32	External Interrupt Debounce Control Register

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Address	Name	Width	Register Function
10005700	EINT_DBNC_CLR_3_0	32	External Interrupt Debounce Control Register
10005704	EINT_DBNC_CLR_7_4	32	External Interrupt Debounce Control Register
10005708	EINT_DBNC_CLR_B_8	32	External Interrupt Debounce Control Register
1000570C	EINT_DBNC_CLR_F_C	32	External Interrupt Debounce Control Register
100057CC	EINT_DBNC_CLR_C_F_C	32	External Interrupt Debounce Control Register
10005800	DEINT_CON	32	Direct Couple EINT Control Register
10005840	DEINT_SEL_3_0	32	Direct Couple EINT Select Control Register
10005880	DEINT_SEL_SET_3_0	32	Direct Couple EINT Select Control Set Register
100058C0	DEINT_SEL_CLR_3_0	32	Direct Couple EINT Select Control Clear Register
10005900	EINT_EEVT	32	EINT Wakeup Event Status Register
10005A00	EINT_RAW_STA0	32	External Interrupt Raw Status Register
10005A04	EINT_RAW_STA1	32	External Interrupt Raw Status Register
10005A08	EINT_RAW_STA2	32	External Interrupt Raw Status Register
10005A0C	EINT_RAW_STA3	32	External Interrupt Raw Status Register
10005A10	EINT_RAW_STA4	32	External Interrupt Raw Status Register
10005A14	EINT_RAW_STA5	32	External Interrupt Raw Status Register
10005A18	EINT_RAW_STA6	32	External Interrupt Raw Status Register

10005000 **EINT_STA0** **External Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mne	EINT_PEND0[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	EINT_PEND0[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_PEND0	Each bit read as 1 indicates the corresponding external interrupt is pending

10005004 **EINT_STA1** **External Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mne	EINT_PEND1[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	EINT_PEND1[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31:0		EINT_PEND1	Each bit read as 1 indicates the corresponding external interrupt is pending

10005008 EINT_STA2 External Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mne	EINT_PEND2[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	EINT_PEND2[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_PEND2	Each bit read as 1 indicates the corresponding external interrupt is pending

1000500C EINT_STA3 External Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mne	EINT_PEND3[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	EINT_PEND3[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_PEND3	Each bit read as 1 indicates the corresponding external interrupt is pending

10005010 EINT_STA4 External Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mne	EINT_PEND4[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	EINT_PEND4[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_PEND4	Each bit read as 1 indicates the corresponding external interrupt is pending

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10005014 EINT_STA5 External Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mne	EINT_PEND5[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	EINT_PEND5[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_PEND5	Each bit read as 1 indicates the corresponding external interrupt is pending

10005018 EINT_STA6 External Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_PEND6[20:16]				
Type												RO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_PEND6[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_PEND6	Each bit read as 1 indicates the corresponding external interrupt is pending

10005040 EINT_ACK0 External Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_ACK0[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_ACK0[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_ACK0	Write 1 to specific bit to acknowledge the corresponding external interrupt.

10005044 EINT_ACK1 External Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_ACK1[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	EINT_ACK1[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_ACK1	Write 1 to specific bit to acknowledge the corresponding external interrupt.

10005048 EINT_ACK2 External Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_ACK2[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_ACK2[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_ACK2	Write 1 to specific bit to acknowledge the corresponding external interrupt.

1000504C EINT_ACK3 External Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_ACK3[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_ACK3[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_ACK3	Write 1 to specific bit to acknowledge the corresponding external interrupt.

10005050 EINT_ACK4 External Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_ACK4[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_ACK4[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_ACK4	Write 1 to specific bit to acknowledge the corresponding external interrupt.

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10005054 EINT_ACK5 External Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_ACK5[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_ACK5[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_ACK5	Write 1 to specific bit to acknowledge the corresponding external interrupt.

10005058 EINT_ACK6 External Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_ACK6[20:16]				
Type												WO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_ACK6[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_ACK6	Write 1 to specific bit to acknowledge the corresponding external interrupt.

10005080 EINT_MASK0 External Interrupt Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK0[31:16]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK0[15:0]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK0	External interrupt mask value

10005084 EINT_MASK1 External Interrupt Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK1[31:16]															

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Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EINT_MASK1[15:0]**															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK1	External interrupt mask value

10005088 EINT_MASK2 External Interrupt Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**EINT_MASK2[31:16]**															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EINT_MASK2[15:0]**															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK2	External interrupt mask value

1000508C EINT_MASK3 External Interrupt Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**EINT_MASK3[31:16]**															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EINT_MASK3[15:0]**															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK3	External interrupt mask value

10005090 EINT_MASK4 External Interrupt Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**EINT_MASK4[31:16]**															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EINT_MASK4[15:0]**															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

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Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK4	External interrupt mask value

10005094 EINT_MASK5 External Interrupt Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK5[31:16]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK5[15:0]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK5	External interrupt mask value

10005098 EINT_MASK6 External Interrupt Mask Register 001FFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_MASK6[20:16]				
Type												RO				
Reset												1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK6[15:0]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
20:0		EINT_MASK6	External interrupt mask value

100050C0 EINT_MASK_SET0 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_SET0[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_SET0[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_SET0	Write 1 to specific bit to set up the mask of corresponding external interrupt.

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100050C4 **EINT_MASK_SET1** **External Interrupt Mask Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_SET1[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_SET1[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_SET1	Write 1 to specific bit to set up the mask of corresponding external interrupt.

100050C8 **EINT_MASK_SET2** **External Interrupt Mask Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_SET2[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_SET2[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_SET2	Write 1 to specific bit to set up the mask of corresponding external interrupt.

100050CC **EINT_MASK_SET3** **External Interrupt Mask Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_SET3[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_SET3[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_SET3	Write 1 to specific bit to set up the mask of corresponding external interrupt.

100050D0 **EINT_MASK_SET4** **External Interrupt Mask Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	**EINT_MASK_SET4[31:16]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EINT_MASK_SET4[15:0]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_SET4	Write 1 to specific bit to set up the mask of corresponding external interrupt.

100050D4 **EINT_MASK_SET5** **External Interrupt Mask Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**EINT_MASK_SET5[31:16]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EINT_MASK_SET5[15:0]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_SET5	Write 1 to specific bit to set up the mask of corresponding external interrupt.

100050D8 **EINT_MASK_SET6** **External Interrupt Mask Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												**EINT_MASK_SET6[20:16]**				
Type												WO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EINT_MASK_SET6[15:0]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_MASK_SET6	Write 1 to specific bit to set up the mask of corresponding external interrupt.

10005100 **EINT_MASK_CLR0** **External Interrupt Mask Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**EINT_MASK_CLR0[31:16]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EINT_MASK_CLR0[15:0]**															

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Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_CLR0	Write 1 to specific bit to set up the mask of corresponding external interrupt.

10005104 **EINT_MASK_CLR1** **External Interrupt Mask Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_CLR1[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_CLR1[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_CLR1	Write 1 to specific bit to set up the mask of corresponding external interrupt.

10005108 **EINT_MASK_CLR2** **External Interrupt Mask Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_CLR2[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_CLR2[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_CLR2	Write 1 to specific bit to set up the mask of corresponding external interrupt.

1000510C **EINT_MASK_CLR3** **External Interrupt Mask Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_CLR3[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_CLR3[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_CLR3	Write 1 to specific bit to set up the mask of corresponding external interrupt.

10005110 **EINT_MASK_CLR4** **External Interrupt Mask Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_CLR4[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_CLR4[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_CLR4	Write 1 to specific bit to set up the mask of corresponding external interrupt.

10005114 **EINT_MASK_CLR5** **External Interrupt Mask Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_CLR5[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_CLR5[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_CLR5	Write 1 to specific bit to set up the mask of corresponding external interrupt.

10005118 **EINT_MASK_CLR6** **External Interrupt Mask Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_MASK_CLR6[20:16]				
Type												WO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_CLR6[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_MASK_CLR6	Write 1 to specific bit to set up the mask of corresponding external interrupt.

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10005140 EINT_SENS0 External Interrupt Sensitivity Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS0[31:16]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS0[15:0]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS0	External interrupt sensitivity value

10005144 EINT_SENS1 External Interrupt Sensitivity Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS1[31:16]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS1[15:0]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS1	External interrupt sensitivity value

10005148 EINT_SENS2 External Interrupt Sensitivity Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS2[31:16]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS2[15:0]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS2	External interrupt sensitivity value

1000514C EINT_SENS3 External Interrupt Sensitivity Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS3[31:16]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS3[15:0]															

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Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS3	External interrupt sensitivity value

10005150 **EINT_SENS4** **External Interrupt Sensitivity Register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS4[31:16]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS4[15:0]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS4	External interrupt sensitivity value

10005154 **EINT_SENS5** **External Interrupt Sensitivity Register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS5[31:16]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS5[15:0]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS5	External interrupt sensitivity value

10005158 **EINT_SENS6** **External Interrupt Sensitivity Register** **001FFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_SENS6[20:16]				
Type												RO				
Reset												1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS6[15:0]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
20:0		EINT_SENS6	External interrupt sensitivity value

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10005180 **EINT_SENS_SET0** **External Interrupt Sensitivity Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_SET0[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_SET0[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_SET0	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

10005184 **EINT_SENS_SET1** **External Interrupt Sensitivity Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_SET1[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_SET1[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_SET1	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

10005188 **EINT_SENS_SET2** **External Interrupt Sensitivity Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_SET2[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_SET2[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_SET2	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

1000518C **EINT_SENS_SET3** **External Interrupt Sensitivity Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	**EINT_SENS_SET3[31:16]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EINT_SENS_SET3[15:0]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_SET3	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

10005190 EINT_SENS_SET4 External Interrupt Sensitivity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**EINT_SENS_SET4[31:16]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EINT_SENS_SET4[15:0]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_SET4	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

10005194 EINT_SENS_SET5 External Interrupt Sensitivity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**EINT_SENS_SET5[31:16]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EINT_SENS_SET5[15:0]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_SET5	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

10005198 EINT_SENS_SET6 External Interrupt Sensitivity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												**EINT_SENS_SET6[20:16]**				
Type												WO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EINT_SENS_SET6[15:0]**															

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Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_SENS_SET6	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

100051C0 EINT_SENS_CLR0 External Interrupt Sensitivity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_CLR0[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR0[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_CLR0	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

100051C4 EINT_SENS_CLR1 External Interrupt Sensitivity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_CLR1[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR1[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_CLR1	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

100051C8 EINT_SENS_CLR2 External Interrupt Sensitivity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_CLR2[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR2[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_CLR2	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

100051CC **EINT_SENS_CLR3** **External Interrupt Sensitivity Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_CLR3[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR3[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_CLR3	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

100051D0 **EINT_SENS_CLR4** **External Interrupt Sensitivity Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_CLR4[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR4[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_CLR4	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

100051D4 **EINT_SENS_CLR5** **External Interrupt Sensitivity Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_CLR5[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR5[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_CLR5	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

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100051D8 **EINT_SENS_CLR6** **External Interrupt Sensitivity Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_SENS_CLR6[20:16]				
Type												WO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR6[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_SENS_CLR6	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

10005200 **EINT_SOFT0** **Software Interrupt Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT0[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT0[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT0	Software interrupt value

10005204 **EINT_SOFT1** **Software Interrupt Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT1[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT1[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT1	Software interrupt value

10005208 **EINT_SOFT2** **Software Interrupt Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT2[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EINT_SOFT2[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT2	Software interrupt value

1000520C EINT_SOFT3 Software Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**EINT_SOFT3[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EINT_SOFT3[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT3	Software interrupt value

10005210 EINT_SOFT4 Software Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**EINT_SOFT4[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EINT_SOFT4[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT4	Software interrupt value

10005214 EINT_SOFT5 Software Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**EINT_SOFT5[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EINT_SOFT5[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT5	Software interrupt value

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10005218 EINT_SOFT6 Software Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_SOFT6[20:16]				
Type												RO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT6[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_SOFT6	Software interrupt value

10005240 EINT_SOFT_SET0 Software Interrupt Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_SET0[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_SET0[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_SET0	Write 1 to specific bit to set up the corresponding software interrupt.

10005244 EINT_SOFT_SET1 Software Interrupt Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_SET1[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_SET1[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_SET1	Write 1 to specific bit to set up the corresponding software interrupt.

10005248 EINT_SOFT_SET2 Software Interrupt Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_SET2[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_SET2[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_SET2	Write 1 to specific bit to set up the corresponding software interrupt.

1000524C **EINT_SOFT_SET3** **Software Interrupt Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_SET3[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_SET3[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_SET3	Write 1 to specific bit to set up the corresponding software interrupt.

10005250 **EINT_SOFT_SET4** **Software Interrupt Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_SET4[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_SET4[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_SET4	Write 1 to specific bit to set up the corresponding software interrupt.

10005254 **EINT_SOFT_SET5** **Software Interrupt Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_SET5[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_SET5[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_SET5	Write 1 to specific bit to set up the corresponding software interrupt.

10005258 EINT_SOFT_SET6 Software Interrupt Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_SOFT_SET6[20:16]				
Type												WO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_SET6[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_SOFT_SET6	Write 1 to specific bit to set up the corresponding software interrupt.

10005280 EINT_SOFT_CLR0 Software Interrupt Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_CLR0[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_CLR0[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_CLR0	Write 1 to specific bit to set up the corresponding software interrupt.

10005284 EINT_SOFT_CLR1 Software Interrupt Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_CLR1[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_CLR1[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_CL	Write 1 to specific bit to set up the corresponding software

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Bit(s)	Mnemonic	Name	Description
		R1	interrupt.

10005288 **EINT_SOFT_CLR2** **Software Interrupt Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_CLR2[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_CLR2[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_CLR2	Write 1 to specific bit to set up the corresponding software interrupt.

1000528C **EINT_SOFT_CLR3** **Software Interrupt Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_CLR3[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_CLR3[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_CLR3	Write 1 to specific bit to set up the corresponding software interrupt.

10005290 **EINT_SOFT_CLR4** **Software Interrupt Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_CLR4[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_CLR4[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_CLR4	Write 1 to specific bit to set up the corresponding software interrupt.

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10005294 EINT_SOFT_CLR5 Software Interrupt Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_CLR5[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_CLR5[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_CLR5	Write 1 to specific bit to set up the corresponding software interrupt.

10005298 EINT_SOFT_CLR6 Software Interrupt Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_SOFT_CLR6[20:16]				
Type												WO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_CLR6[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_SOFT_CLR6	Write 1 to specific bit to set up the corresponding software interrupt.

10005300 EINT_POL0 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL0[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL0[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL0	External interrupt polarity value

10005304 EINT_POL1 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL1[31:16]															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EINT_POL1[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL1	External interrupt polarity value

10005308 EINT_POL2 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**EINT_POL2[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EINT_POL2[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL2	External interrupt polarity value

1000530C EINT_POL3 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**EINT_POL3[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EINT_POL3[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL3	External interrupt polarity value

10005310 EINT_POL4 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**EINT_POL4[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EINT_POL4[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL4	External interrupt polarity value

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10005314 EINT_POL5 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL5[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL5[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL5	External interrupt polarity value

10005318 EINT_POL6 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_POL6[20:16]				
Type												RO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL6[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_POL6	External interrupt polarity value

10005340 EINT_POL_SET0 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_SET0[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET0[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_SET0	Write 1 to specific bit to set up the polarity of corresponding external interrupt.

10005344 EINT_POL_SET1 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_SET1[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET1[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_SET1	Write 1 to specific bit to set up the polarity of corresponding external interrupt.

10005348 **EINT_POL_SET2** **External Interrupt Polarity Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_SET2[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET2[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_SET2	Write 1 to specific bit to set up the polarity of corresponding external interrupt.

1000534C **EINT_POL_SET3** **External Interrupt Polarity Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_SET3[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET3[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_SET3	Write 1 to specific bit to set up the polarity of corresponding external interrupt.

10005350 **EINT_POL_SET4** **External Interrupt Polarity Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_SET4[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET4[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_SET4	Write 1 to specific bit to set up the polarity of corresponding external interrupt.

10005354 **EINT_POL_SET5** **External Interrupt Polarity Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_SET5[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET5[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_SET5	Write 1 to specific bit to set up the polarity of corresponding external interrupt.

10005358 **EINT_POL_SET6** **External Interrupt Polarity Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_POL_SET6[20:16]				
Type												WO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET6[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_POL_SET6	Write 1 to specific bit to set up the polarity of corresponding external interrupt.

10005380 **EINT_POL_CLR0** **External Interrupt Polarity Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_CLR0[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR0[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_CLR	Write 1 to specific bit to clear the polarity of corresponding external

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Bit(s)	Mnemonic	Name	Description
		0	interrupt.

10005384 **EINT_POL_CLR1** **External Interrupt Polarity Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_CLR1[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR1[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_CLR1	Write 1 to specific bit to clear the polarity of corresponding external interrupt.

10005388 **EINT_POL_CLR2** **External Interrupt Polarity Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_CLR2[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR2[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_CLR2	Write 1 to specific bit to clear the polarity of corresponding external interrupt.

1000538C **EINT_POL_CLR3** **External Interrupt Polarity Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_CLR3[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR3[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_CLR3	Write 1 to specific bit to clear the polarity of corresponding external interrupt.

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10005390 **EINT_POL_CLR4** **External Interrupt Polarity Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_CLR4[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR4[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_CLR4	Write 1 to specific bit to clear the polarity of corresponding external interrupt.

10005394 **EINT_POL_CLR5** **External Interrupt Polarity Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_CLR5[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR5[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_CLR5	Write 1 to specific bit to clear the polarity of corresponding external interrupt.

10005398 **EINT_POL_CLR6** **External Interrupt Polarity Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_POL_CLR6[20:16]				
Type												WO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR6[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_POL_CLR6	Write 1 to specific bit to clear the polarity of corresponding external interrupt.

10005400 **EINT_D0EN0** **Domain 0 External Interrupt Enable Control Register** **00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_DoENo[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_DoENo[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_DoEN0	Write 1 to specific bit to enable the corresponding software external interrupt in domain 0.

10005404 **EINT_DoEN1** **Domain 0 External Interrupt Enable Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_DoEN1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_DoEN1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_DoEN1	Write 1 to specific bit to enable the corresponding software external interrupt in domain 0.

10005408 **EINT_DoEN2** **Domain 0 External Interrupt Enable Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_DoEN2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_DoEN2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_DoEN2	Write 1 to specific bit to enable the corresponding software external interrupt in domain 0.

1000540C **EINT_DoEN3** **Domain 0 External Interrupt Enable Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_DoEN3[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	EINT_D0EN3[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_D0EN3	Write 1 to specific bit to enable the corresponding software external interrupt in domain 0.

10005410 EINT_D0EN4 Domain 0 External Interrupt Enable Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_D0EN4[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_D0EN4[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_D0EN4	Write 1 to specific bit to enable the corresponding software external interrupt in domain 0.

10005414 EINT_D0EN5 Domain 0 External Interrupt Enable Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_D0EN5[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_D0EN5[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_D0EN5	Write 1 to specific bit to enable the corresponding software external interrupt in domain 0.

10005418 EINT_D0EN6 Domain 0 External Interrupt Enable Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_D0EN6[20:16]				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_D0EN6[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
20:0		EINT_D0EN6	Write 1 to specific bit to enable the corresponding software external interrupt in domain 0.

10005500 **EINT_DBNC_3_0** **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DBNC_SETTING3**						**DBNC_RST3**	**EN3**	**DBNC_SETTING2**						**DBNC_RST2**	**EN2**
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DBNC_SETTING1**						**DBNC_RST1**	**EN1**	**DBNC_SETTING0**						**DBNC_RST0**	**EN0**
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING3	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
25		DBNC_RST3	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN3	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING2	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
17		DBNC_RST2	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN2	**Enables de-bounce function** 0: Disable 1: Enable

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Bit(s)	Mnemonic	Name	Description
15:12		DBNC_SETTING1	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
9		DBNC_RST1	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN1	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING0	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
1		DBNC_RST0	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN0	**Enables de-bounce function** 0: Disable 1: Enable

10005504 **EINT_DBNC_7_4** **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DBNC_SETTING7**						**DBNC_RST7**	**EN7**	**DBNC_SETTING6**						**DBNC_RST6**	**EN6**
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DBNC_SETTING5**						**DBNC_RST5**	**EN5**	**DBNC_SETTING4**						**DBNC_RST4**	**EN4**
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING7	**De-bounce setting** 0000: 0.125ms

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Bit(s)	Mnemonic	Name	Description
			0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST7	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN7	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING6	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST6	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN6	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING5	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST5	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN5	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING4	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms

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Bit(s)	Mnemonic	Name	Description
			0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST4	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN4	**Enables de-bounce function** 0: Disable 1: Enable

10005508 **EINT_DBNC_B_8** **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING11						DBNC_RST11	EN11	DBNC_SETTING10						DBNC_RST10	EN10
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING9						DBNC_RST9	EN9	DBNC_SETTING8						DBNC_RST8	EN8
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING11	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST11	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN11	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING10	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms

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Bit(s)	Mnemonic	Name	Description
			0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST10	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN10	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING9	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST9	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN9	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING8	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST8	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN8	**Enables de-bounce function** 0: Disable 1: Enable

1000550C **EINT_DBNC_F_C** **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DBNC_SETTING15**						**DBNC_RST15**	**EN15**	**DBNC_SETTING14**						**DBNC_RST14**	**EN14**
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING13						DBNC_RST13	EN13	DBNC_SETTING12						DBNC_RST12	EN12
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING15	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST15	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN15	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING14	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST14	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN14	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING13	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST13	**Resets de-bounce counter** 0: Negative 1: Positive

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Bit(s)	Mnemonic	Name	Description
8		EN13	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING 12	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST12	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN12	**Enables de-bounce function** 0: Disable 1: Enable

100055CC **EINT_DBNC_CFC** **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING207						DBNC_RST207	EN207	DBNC_SETTING206						DBNC_RST206	EN206
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING205						DBNC_RST205	EN205	DBNC_SETTING204						DBNC_RST204	EN204
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING 207	0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST207	0: Negative 1: Positive
24		EN207	0: Disable 1: Enable

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Bit(s)	Mnemonic	Name	Description
23:20		DBNC_SETTING 206	0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST206	0: Negative 1: Positive
16		EN206	0: Disable 1: Enable
15:12		DBNC_SETTING 205	0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST205	0: Negative 1: Positive
8		EN205	0: Disable 1: Enable
7:4		DBNC_SETTING 204	0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST204	0: Negative 1: Positive
0		EN204	0: Disable 1: Enable

10005600 **EINT_DBNC_SET_3_0** **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_SET3						DBNC_RST_SET3	EN_SET3	DBNC_SETTING_SET2						DBNC_RST_SET2	EN_SET2
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_SET1						DBNC_RST_SET1	EN_SET1	DBNC_SETTING_SET0						DBNC_RST_SET0	EN_SET0
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_SET3	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
25		DBNC_RST_SET3	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_SET3	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING_SET2	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
17		DBNC_RST_SET2	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_SET2	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_SET1	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
9		DBNC_RST_SET	**Resets de-bounce counter**

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Bit(s)	Mnemonic	Name	Description
		1	0: Negative 1: Positive
8		EN_SET1	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_SET0	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
1		DBNC_RST_SET0	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_SET0	**Enables de-bounce function** 0: Disable 1: Enable

10005604 **EINT_DBNC_SET_7_4** **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_SET7						DBNC_RST_SET7	EN_SET7	DBNC_SETTING_SET6						DBNC_RST_SET6	EN_SET6
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DBNC_SETTING_SET5						DBNC_RST_SET5	EN_SET5	DBNC_SETTING_SET4						DBNC_RST_SET4	EN_SET4
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_SET7	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms

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Bit(s)	Mnemonic	Name	Description
25		DBNC_RST_SET7	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_SET7	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING_SET6	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST_SET6	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_SET6	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_SET5	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST_SET5	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_SET5	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_SET4	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST_SET4	**Resets de-bounce counter** 0: Negative 1: Positive

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Bit(s)	Mnemonic	Name	Description
0		EN_SET4	**Enables de-bounce function** 0: Disable 1: Enable

10005608 **EINT_DBNC_SET_B_8** **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_SET11						DBNC_RST_SET11	EN_SET11	DBNC_SETTING_SET10						DBNC_RST_SET10	EN_SET10
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_SET9						DBNC_RST_SET9	EN_SET9	DBNC_SETTING_SET8						DBNC_RST_SET8	EN_SET8
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_SET11	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST_SET11	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_SET11	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING_SET10	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST_SET10	**Resets de-bounce counter** 0: Negative

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Bit(s)	Mnemonic	Name	Description
			1: Positive
16		EN_SET10	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_SET9	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST_SET9	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_SET9	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_SET8	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST_SET8	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_SET8	**Enables de-bounce function** 0: Disable 1: Enable

1000560C **EINT_DBNC_SET_F_C** **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DBNC_SETTING_SET15**						**DBNC_RST_SET15**	**EN_SET15**	**DBNC_SETTING_SET14**						**DBNC_RST_SET14**	**EN_SET14**
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DBNC_SETTING_SET13**						**DBNC_RST_SET1**	**EN_SET13**	**DBNC_SETTING_SET12**						**DBNC_RST_SET1**	**EN_SET12**

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							3								2	
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_SET15	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST_SET15	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_SET15	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING_SET14	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST_SET14	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_SET14	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_SET13	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST_SET13	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_SET13	**Enables de-bounce function** 0: Disable

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Bit(s)	Mnemonic	Name	Description
			1: Enable
7:4		DBNC_SETTING_SET12	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST_SET12	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_SET12	**Enables de-bounce function** 0: Disable 1: Enable

100056CC **EINT_DBNC_SET_C_F_C** **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DBNC_SETTING_SET207**						**DBNC_RST_SET207**	**EN_SET207**	**DBNC_SETTING_SET206**						**DBNC_RST_SET206**	**EN_SET206**
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DBNC_SETTING_SET205**						**DBNC_RST_SET205**	**EN_SET205**	**DBNC_SETTING_SET204**						**DBNC_RST_SET204**	**EN_SET204**
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_SET207	0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST_SET207	0: Negative 1: Positive
24		EN_SET207	0: Disable 1: Enable

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Bit(s)	Mnemonic	Name	Description
23:20		DBNC_SETTING_SET206	0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST_SET206	0: Negative 1: Positive
16		EN_SET206	0: Disable 1: Enable
15:12		DBNC_SETTING_SET205	0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST_SET205	0: Negative 1: Positive
8		EN_SET205	0: Disable 1: Enable
7:4		DBNC_SETTING_SET204	0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST_SET204	0: Negative 1: Positive
0		EN_SET204	0: Disable 1: Enable

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10005700 **EINT_DBNC_CLR_3_0** **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_CLR_CLR3						DBNC_RST3	EN_CLR3		DBNC_SETTING_CLR_CLR2					DBNC_RST2	EN_CLR2
Type	WO						WO	WO		WO					WO	WO
Reset	0	0	0	0			0	0		0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_CLR_						DBN	EN_	DBNC_SETTING_CLR_						DBN	EN_

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	CLR1						C_RST1	CLR1	CLR0						C_RST0	CLR0
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_CLR_CLR3	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
25		DBNC_RST3	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_CLR3	**Enables de-bounce function** 0: Disable 1: Enable
22:20		DBNC_SETTING_CLR_CLR2	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
17		DBNC_RST2	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_CLR2	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_CLR_CLR1	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
9		DBNC_RST1	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_CLR1	**Enables de-bounce function**

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Bit(s)	Mnemonic	Name	Description
			0: Disable 1: Enable
7:4		DBNC_SETTING_CLR_CLR0	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
1		DBNC_RST0	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_CLR0	**Enables de-bounce function** 0: Disable 1: Enable

10005704 **EINT_DBNC_CLR_7_4** **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_CLR_CLR7						DBNC_RST7	EN_CLR7		DBNC_SETTING_CLR_CLR6					DBNC_RST6	EN_CLR6
Type	WO						WO	WO		WO					WO	WO
Reset	0	0	0	0			0	0		0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_CLR_CLR5						DBNC_RST5	EN_CLR5	DBNC_SETTING_CLR_CLR4						DBNC_RST4	EN_CLR4
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_CLR_CLR7	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST7	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_CLR7	**Enables de-bounce function** 0: Disable 1: Enable

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Bit(s)	Mnemonic	Name	Description
22:20		DBNC_SETTING_CLR_CLR6	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST6	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_CLR6	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_CLR_CLR5	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST5	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_CLR5	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_CLR_CLR4	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST4	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_CLR4	**Enables de-bounce function** 0: Disable 1: Enable

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10005708	EINT_DBNC_CLR_B_8	External Interrupt Debounce Control Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_CLR_CLR11						DBNC_RST11	EN_CLR11		DBNC_SETTING_CLR_CLR10					DBNC_RST10	EN_CLR10
Type	WO						WO	WO		WO					WO	WO
Reset	0	0	0	0			0	0		0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_CLR_CLR9						DBNC_RST9	EN_CLR9	DBNC_SETTING_CLR_CLR8						DBNC_RST8	EN_CLR8
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_CLR_CLR11	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST11	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_CLR11	**Enables de-bounce function** 0: Disable 1: Enable
22:20		DBNC_SETTING_CLR_CLR10	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST10	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_CLR10	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_CLR_CLR9	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms

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Bit(s)	Mnemonic	Name	Description
			0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST9	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_CLR9	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_CLR_CLR8	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST8	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_CLR8	**Enables de-bounce function** 0: Disable 1: Enable

1000570C **EINT_DBNC_CLR_F_C** **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_CLR_CLR15						DBNC_RST15	EN_CLR15		DBNC_SETTING_CLR_CLR14					DBNC_RST14	EN_CLR14
Type	WO						WO	WO		WO					WO	WO
Reset	0	0	0	0			0	0		0	0	0			0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DBNC_SETTING_CLR_CLR13						DBNC_RST13	EN_CLR13	DBNC_SETTING_CLR_CLR12						DBNC_RST12	EN_CLR12
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_CLR_CLR15	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms

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Bit(s)	Mnemonic	Name	Description
			0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST15	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_CLR15	**Enables de-bounce function** 0: Disable 1: Enable
22:20		DBNC_SETTING_CLR_CLR14	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST14	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_CLR14	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_CLR_CLR13	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST13	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_CLR13	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_CLR_CLR12	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms

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Bit(s)	Mnemonic	Name	Description
			Others: 0.5ms
1		DBNC_RST12	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_CLR12	**Enables de-bounce function** 0: Disable 1: Enable

100057CC **EINT_DBNC_CLR_C_F_C** **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DBNC_SETTING_CLR_CLR207**						**DBNC_RST207**	**EN_CLR207**		**DBNC_SETTING_CLR_CLR206**					**DBNC_RST206**	**EN_CLR206**
Type	WO						WO	WO		WO					WO	WO
Reset	0	0	0	0			0	0		0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DBNC_SETTING_CLR_CLR205**						**DBNC_RST205**	**EN_CLR205**	**DBNC_SETTING_CLR_CLR204**						**DBNC_RST204**	**EN_CLR204**
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_CLR_CLR207	0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST207	0: Negative 1: Positive
24		EN_CLR207	0: Disable 1: Enable
22:20		DBNC_SETTING_CLR_CLR206	0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST206	0: Negative 1: Positive

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Bit(s)	Mnemonic	Name	Description
16		EN_CLR206	0: Disable 1: Enable
15:12		DBNC_SETTING_CLR_CLR205	0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST205	0: Negative 1: Positive
8		EN_CLR205	0: Disable 1: Enable
7:4		DBNC_SETTING_CLR_CLR204	0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST204	0: Negative 1: Positive
0		EN_CLR204	0: Disable 1: Enable

10005800 **DEINT_CON** **Direct Couple EINT Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DEINT_CON3	DEINT_CON2	DEINT_CON1	DEINT_CON0
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3		DEINT_CON3	**Controls direct couple EINT3** 0: Disable 1: Enable
2		DEINT_CON2	**Controls direct couple EINT2** 0: Disable 1: Enable

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Bit(s)	Mnemonic	Name	Description
1		DEINT_CON1	**Controls direct couple EINT1** 0: Disable 1: Enable
0		DEINT_CON0	**Controls direct couple EINT0** 0: Disable 1: Enable

10005840 DEINT_SEL_3_0 Direct Couple EINT Select Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEINT_SEL3								DEINT_SEL2							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEINT_SEL1								DEINT_SEL0							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		DEINT_SEL3	**Selects direct couple EINT3** #: EINT number
23:16		DEINT_SEL2	**Selects direct couple EINT2** #: EINT number
15:8		DEINT_SEL1	**Selects direct couple EINT1** #: EINT number
7:0		DEINT_SEL0	**Selects direct couple EINT0** #: EINT number

10005880 DEINT_SEL_SET_3_0 Direct Couple EINT Select Control Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEINT_SEL3								DEINT_SEL2							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEINT_SEL1								DEINT_SEL0							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		DEINT_SEL3	**Sets up direct couple EINT3 selection** #: EINT number
23:16		DEINT_SEL2	**Sets up direct couple EINT2 selection** #: EINT number
15:8		DEINT_SEL1	**Sets up direct couple EINT1 selection** #: EINT number
7:0		DEINT_SEL0	**Sets up direct couple EINT0 selection** #: EINT number

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100058C0 DEINT_SEL_CLR_3_0 Direct Couple EINT Select Control Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEINT_SEL3								DEINT_SEL2							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEINT_SEL1								DEINT_SEL0							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		DEINT_SEL3	**Clears direct couple EINT3 selection** #: EINT number
23:16		DEINT_SEL2	**Clears direct couple EINT2 selection** #: EINT number
15:8		DEINT_SEL1	**Clears direct couple EINT1 selection** #: EINT number
7:0		DEINT_SEL0	**Clears direct couple EINT0 selection** #: EINT number

10005900 EINT_EEVT EINT Wakeup Event Status Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EINT_EEVT
Type																RO
Reset																1

Bit(s)	Mnemonic	Name	Description
0		EINT_EEVT	EINT wakeup event status

10005A00 EINT_RAW_STA0 External Interrupt Raw Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_RAW_PEND0[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_RAW_PEND0[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
31:0		EINT_RAW_PEND0	Each bit read as 1 indicates the corresponding external interrupt is pending (no matter it's mask or not)

10005A04 EINT_RAW_STA1 External Interrupt Raw Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_RAW_PEND1[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_RAW_PEND1[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_RAW_PEND1	Each bit read as 1 indicates the corresponding external interrupt is pending (no matter it's mask or not)

10005A08 EINT_RAW_STA2 External Interrupt Raw Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_RAW_PEND2[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_RAW_PEND2[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_RAW_PEND2	Each bit read as 1 indicates the corresponding external interrupt is pending (no matter it's mask or not)

10005A0C EINT_RAW_STA3 External Interrupt Raw Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_RAW_PEND3[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_RAW_PEND3[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_RAW_PEND3	Each bit read as 1 indicates the corresponding external interrupt is pending (no matter it's mask or not)

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10005A10 **EINT_RAW_STA4** **External Interrupt Raw Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_RAW_PEND4[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_RAW_PEND4[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_RAW_PEND4	Each bit read as 1 indicates the corresponding external interrupt is pending (no matter it's mask or not)

10005A14 **EINT_RAW_STA5** **External Interrupt Raw Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_RAW_PEND5[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_RAW_PEND5[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_RAW_PEND5	Each bit read as 1 indicates the corresponding external interrupt is pending (no matter it's mask or not)

10005A18 **EINT_RAW_STA6** **External Interrupt Raw Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_RAW_PEND6[20:16]				
Type												RO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_RAW_PEND6[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_RAW_PEND6	Each bit read as 1 indicates the corresponding external interrupt is pending (no matter it's mask or not)

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3.3.5 Programming Guide

3.3.5.1 Register Bit Set/Clear

For efficient bit set up/clear operation, the following registers have specific bit set/clear registers:

- EINT_MASK
- EINT_SOFT
- EINT_DBNC
- EINT_POL

Write 1 to the specified bit of the set/clear register to set up or clear the corresponding bit in the status register.

3.3.5.2 Domain Control

For instance, if you would like int_bus[3] to trigger eint_irq[0], bit 3 in the EINT_D0EN register should be set.

3.3.5.3 EINT De-bounce Control Sequence

1. Set up EINT_CON (PRESCALER, POL, CNT) and enable de-bounce (EN).
2. Wait for 3*32K (~100us).
3. Write RSTDBC (self-clear).
4. Wait for 3*32K (~100us).
5. Write EINT_INTACK to ack/clear all statuses.
6. Unmask EINT_MASK.

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3.4 System Interrupt Controller

3.4.1 Introduction

For processors which have embedded interrupt controllers (GIC) in it, the part of the MCUSYS will need to keep feeding clock and power to make interrupt functional. However, due to power/leakage overhead introduced by higher clock ratio and deep submicron processes, reserving an always on (or frequently turned on) domain in MCUSYS has became power ineffective. The system interrupt controller (SYS_CIRQ) is a low power interrupt controller designed to work outside MCUSYS as a second level interrupt controller. With SYS_CIRQ, the MCUSYS can be completely turned off to improve system power consumption without losing interrupts.

3.4.2 Features

SYS_CIRQ supports up to 159 interrupts which can configure following attributes individually.

- Polarity inversion
- Edge/level trigger selection

The 159 interrupts feed through SYS_CIRQ and connect to GIC in MCUSYS. When SYS_CIRQ is enabled, it will record the edge-sensitive interrupts and generate a pulse signal to CPU GIC when the flush command is executed.

3.4.3 Block Diagram

Figure 3-4 is the system level block diagram of the system interrupt controller.

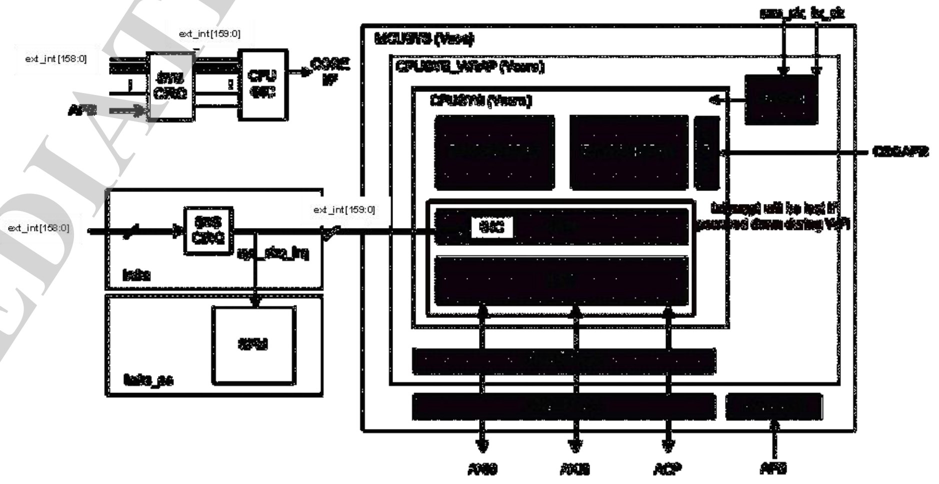

Figure 3-4. System level block diagram of system interrupt controller

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The SYS_CIRQ controller is integrated in between MCUSYS and other interrupt sources as the second level interrupt controller. All interrupts are fed through SYS_CIRQ controller then bypassed to MCUSYS. In normal mode (where MCUSYS GIC is active), SYS_CIRQ is disabled and interrupts will be directly issued to MCUSYS. When MCUSYS enters the sleep mode, where GIC is power downed, the SYS_CIRQ controller will be enabled and monitor all edge-trigger interrupts (only edge-triggered interrupt will be lost in this scenario). When an edge-trigger interrupt is triggered, it will be recorded in SYS_CIRQ_STA register and can be restored to GIC by SW context restore or the SYS_CIRQ flush function.

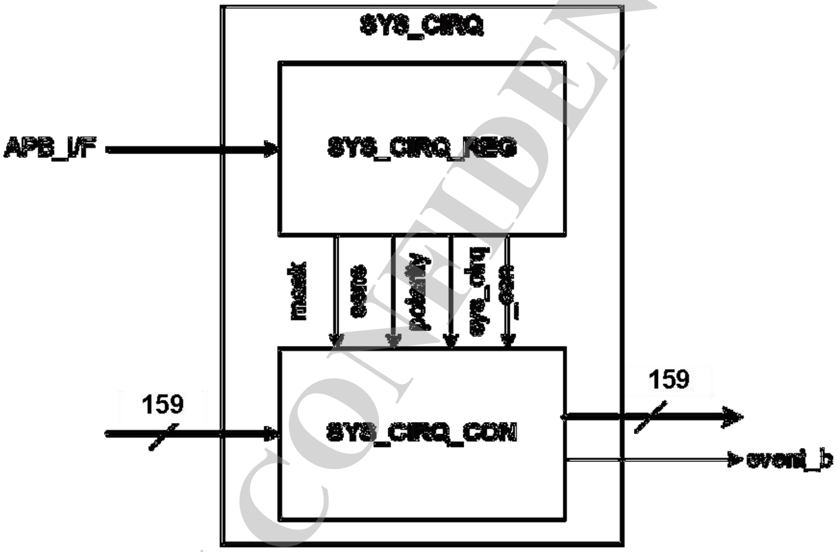

Figure 3-5. Block diagram of system interrupt controller

Figure 3-5 is the architecture of SYS_CIRQ. SYS_CIRQ_REG stores the mask/sensitivity/polarity attributes of each interrupt signal, and SYS_CIRQ_CON is used to mask and detect edge-triggered interrupts.

3.4.4 Register Definition

Module name: sys_cirq Base address: (+10204000h)

Address	Name	Width	Register Function
10204000	CIRQ_STA0	32	System CIRQ Status Register
10204004	CIRQ_STA1	32	System CIRQ Status Register
10204008	CIRQ_STA2	32	System CIRQ Status Register
1020400C	CIRQ_STA3	32	System CIRQ Status Register
10204010	CIRQ_STA4	32	System CIRQ Status Register
10204040	CIRQ_ACK0	32	System CIRQ Acknowledge Register
10204044	CIRQ_ACK1	32	System CIRQ Acknowledge Register
10204048	CIRQ_ACK2	32	System CIRQ Acknowledge Register
1020404C	CIRQ_ACK3	32	System CIRQ Acknowledge Register
10204050	CIRQ_ACK4	32	System CIRQ Acknowledge Register

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Address	Name	Width	Register Function
10204080	CIRQ_MASK0	32	System CIRQ Mask Register
10204084	CIRQ_MASK1	32	System CIRQ Mask Register
10204088	CIRQ_MASK2	32	System CIRQ Mask Register
1020408C	CIRQ_MASK3	32	System CIRQ Mask Register
10204090	CIRQ_MASK4	32	System CIRQ Mask Register
102040C0	CIRQ_MASK_SET0	32	System CIRQ Mask Set Register
102040C4	CIRQ_MASK_SET1	32	System CIRQ Mask Set Register
102040C8	CIRQ_MASK_SET2	32	System CIRQ Mask Set Register
102040CC	CIRQ_MASK_SET3	32	System CIRQ Mask Set Register
102040D0	CIRQ_MASK_SET4	32	System CIRQ Mask Set Register
10204100	CIRQ_MASK_CLR0	32	System CIRQ Mask Set Register
10204104	CIRQ_MASK_CLR1	32	System CIRQ Mask Set Register
10204108	CIRQ_MASK_CLR2	32	System CIRQ Mask Set Register
1020410C	CIRQ_MASK_CLR3	32	System CIRQ Mask Set Register
10204110	CIRQ_MASK_CLR4	32	System CIRQ Mask Set Register
10204140	CIRQ_SENS0	32	System CIRQ Sensitivity Register
10204144	CIRQ_SENS1	32	System CIRQ Sensitivity Register
10204148	CIRQ_SENS2	32	System CIRQ Sensitivity Register
1020414C	CIRQ_SENS3	32	System CIRQ Sensitivity Register
10204150	CIRQ_SENS4	32	System CIRQ Sensitivity Register
10204180	CIRQ_SENS_SET0	32	System CIRQ Sensitivity Set Register
10204184	CIRQ_SENS_SET1	32	System CIRQ Sensitivity Set Register
10204188	CIRQ_SENS_SET2	32	System CIRQ Sensitivity Set Register
1020418C	CIRQ_SENS_SET3	32	System CIRQ Sensitivity Set Register
10204190	CIRQ_SENS_SET4	32	System CIRQ Sensitivity Set Register
102041C0	CIRQ_SENS_CLR0	32	System CIRQ Sensitivity Clear Register
102041C4	CIRQ_SENS_CLR1	32	System CIRQ Sensitivity Clear Register
102041C8	CIRQ_SENS_CLR2	32	System CIRQ Sensitivity Clear Register
102041CC	CIRQ_SENS_CLR3	32	System CIRQ Sensitivity Clear Register
102041D0	CIRQ_SENS_CLR4	32	System CIRQ Sensitivity Clear Register
10204200	CIRQ_POL0	32	External Interrupt Polarity Register
10204204	CIRQ_POL1	32	External Interrupt Polarity Register
10204208	CIRQ_POL2	32	External Interrupt Polarity Register

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Address	Name	Width	Register Function
1020420C	CIRQ_POL3	32	External Interrupt Polarity Register
10204210	CIRQ_POL4	32	External Interrupt Polarity Register
10204240	CIRQ_POL_SET0	32	External Interrupt Polarity Set Register
10204244	CIRQ_POL_SET1	32	External Interrupt Polarity Set Register
10204248	CIRQ_POL_SET2	32	External Interrupt Polarity Set Register
1020424C	CIRQ_POL_SET3	32	External Interrupt Polarity Set Register
10204250	CIRQ_POL_SET4	32	External Interrupt Polarity Set Register
10204280	CIRQ_POL_CLR0	32	External Interrupt Polarity Clear Register
10204284	CIRQ_POL_CLR1	32	External Interrupt Polarity Clear Register
10204288	CIRQ_POL_CLR2	32	External Interrupt Polarity Clear Register
1020428C	CIRQ_POL_CLR3	32	External Interrupt Polarity Clear Register
10204290	CIRQ_POL_CLR4	32	External Interrupt Polarity Clear Register
10204300	CIRQ_CON	32	System CIRQ Control Register

10204000 CIRQ_STA0 System CIRQ Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mne	CIRQ_PEND0[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	CIRQ_PEND0[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_PEND0	Each bit read as 1 indicates the corresponding system CIRQ is pending

10204004 CIRQ_STA1 System CIRQ Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mne	CIRQ_PEND1[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	CIRQ_PEND1[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_PEND1	Each bit read as 1 indicates the corresponding system CIRQ is pending

10204008 CIRQ_STA2 System CIRQ Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mne	CIRQ_PEND2[31:16]															

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Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	**CIRQ_PEND2[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_PEND2	Each bit read as 1 indicates the corresponding system CIRQ is pending

1020400C **CIRQ_STA3** **System CIRQ Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mne	**CIRQ_PEND3[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	**CIRQ_PEND3[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_PEND3	Each bit read as 1 indicates the corresponding system CIRQ is pending

10204010 **CIRQ_STA4** **System CIRQ Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**CIRQ_PEND4[30:16]**														
Type		RO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CIRQ_PEND4[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_PEND4	Each bit read as 1 indicates the corresponding system CIRQ is pending

10204040 **CIRQ_ACK0** **System CIRQ Acknowledge Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CIRQ_ACK0[31:16]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CIRQ_ACK0[15:0]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_ACK0	Write 1 to specific bit acknowledges the corresponding system CIRQ

10204044 CIRQ_ACK1 System CIRQ Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_ACK1[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK1[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_ACK1	Write 1 to specific bit acknowledges the corresponding system CIRQ

10204048 CIRQ_ACK2 System CIRQ Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_ACK2[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK2[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_ACK2	Write 1 to specific bit acknowledges the corresponding system CIRQ

1020404C CIRQ_ACK3 System CIRQ Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_ACK3[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK3[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_ACK3	Write 1 to specific bit acknowledges the corresponding system CIRQ

10204050 CIRQ_ACK4 System CIRQ Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_ACK4[30:16]														
Type		WO														

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Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CIRQ_ACK4[15:0]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_ACK4	Write 1 to specific bit acknowledges the corresponding system CIRQ

10204080 **CIRQ_MASK0** **System CIRQ Mask Register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CIRQ_MASK0[31:16]**															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CIRQ_MASK0[15:0]**															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK0	System CIRQ mask value

10204084 **CIRQ_MASK1** **System CIRQ Mask Register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CIRQ_MASK1[31:16]**															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CIRQ_MASK1[15:0]**															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK1	System CIRQ mask value

10204088 **CIRQ_MASK2** **System CIRQ Mask Register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CIRQ_MASK2[31:16]**															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CIRQ_MASK2[15:0]**															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

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Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK2	System CIRQ mask value

1020408C **CIRQ_MASK3** **System CIRQ Mask Register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK3[31:16]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK3[15:0]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK3	System CIRQ mask value

10204090 **CIRQ_MASK4** **System CIRQ Mask Register** **7FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_MASK4[30:16]														
Type		RO														
Reset		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK4[15:0]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_MASK4	System CIRQ mask value

102040C0 **CIRQ_MASK_SET0** **System CIRQ Mask Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_SET0[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET0[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_SET0	Write 1 to specific bit to set up the mask of the corresponding system CIRQ.

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102040C4 **CIRQ_MASK_SET1** **System CIRQ Mask Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_SET1[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET1[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_SET1	Write 1 to specific bit to set up the mask of the corresponding system CIRQ.

102040C8 **CIRQ_MASK_SET2** **System CIRQ Mask Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_SET2[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET2[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_SET2	Write 1 to specific bit to set up the mask of the corresponding system CIRQ.

102040CC **CIRQ_MASK_SET3** **System CIRQ Mask Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_SET3[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET3[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_SET3	Write 1 to specific bit to set up the mask of the corresponding system CIRQ.

102040D0 **CIRQ_MASK_SET4** **System CIRQ Mask Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name		**CIRQ_MASK_SET4[30:16]**														
Type		WO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CIRQ_MASK_SET4[15:0]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_MASK_SET4	Write 1 to specific bit to set up the mask of the corresponding system CIRQ.

10204100 CIRQ_MASK_CLR0 System CIRQ Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CIRQ_MASK_CLR0[31:16]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CIRQ_MASK_CLR0[15:0]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_CLR0	Write 1 to specific bit to clear the mask of the corresponding system CIRQ.

10204104 CIRQ_MASK_CLR1 System CIRQ Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CIRQ_MASK_CLR1[31:16]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CIRQ_MASK_CLR1[15:0]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_CLR1	Write 1 to specific bit to clear the mask of the corresponding system CIRQ.

10204108 CIRQ_MASK_CLR2 System CIRQ Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CIRQ_MASK_CLR2[31:16]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CIRQ_MASK_CLR2[15:0]**															

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Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_CLR2	Write 1 to specific bit to clear the mask of the corresponding system CIRQ.

1020410C **CIRQ_MASK_CLR3** **System CIRQ Mask Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_CLR3[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR3[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_CLR3	Write 1 to specific bit to clear the mask of the corresponding system CIRQ.

10204110 **CIRQ_MASK_CLR4** **System CIRQ Mask Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_MASK_CLR4[30:16]														
Type		WO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR4[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_MASK_CLR4	Write 1 to specific bit to clear the mask of the corresponding system CIRQ.

10204140 **CIRQ_SENS0** **System CIRQ Sensitivity Register** **FFFFFFE3**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS0[31:16]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS0[15:0]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS0	System CIRQ sensitivity value

10204144 CIRQ_SENS1 System CIRQ Sensitivity Register FEFC7FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS1[31:16]															
Type	RO															
Reset	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS1[15:0]															
Type	RO															
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS1	System CIRQ sensitivity value

10204148 CIRQ_SENS2 System CIRQ Sensitivity Register FFEFDFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS2[31:16]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS2[15:0]															
Type	RO															
Reset	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS2	System CIRQ sensitivity value

1020414C CIRQ_SENS3 System CIRQ Sensitivity Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS3[31:16]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS3[15:0]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS3	System CIRQ sensitivity value

10204150 CIRQ_SENS4 System CIRQ Sensitivity Register 7F77FFFF

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_SENS4[30:16]														
Type		RO														
Reset		1	1	1	1	1	1	1	0	1	1	1	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS4[15:0]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_SENS4	System CIRQ sensitivity value

10204180 **CIRQ_SENS_SET0** **System CIRQ Sensitivity Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_SET0[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET0[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_SET0	Write 1 to specific bit to set up the sensitivity of the corresponding system CIRQ.

10204184 **CIRQ_SENS_SET1** **System CIRQ Sensitivity Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_SET1[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET1[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_SET1	Write 1 to specific bit to set up the sensitivity of the corresponding system CIRQ.

10204188 **CIRQ_SENS_SET2** **System CIRQ Sensitivity Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_SET2[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET2[15:0]															

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Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_SET2	Write 1 to specific bit to set up the sensitivity of the corresponding system CIRQ.

1020418C CIRQ_SENS_SET3 System CIRQ Sensitivity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_SET3[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET3[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_SET3	Write 1 to specific bit to set up the sensitivity of the corresponding system CIRQ.

10204190 CIRQ_SENS_SET4 System CIRQ Sensitivity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_SENS_SET4[30:16]														
Type		WO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET4[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_SENS_SET4	Write 1 to specific bit to set up the sensitivity of the corresponding system CIRQ.

102041C0 CIRQ_SENS_CLR0 System CIRQ Sensitivity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_CLR0[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR0[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_CLR0	Write 1 to specific bit to clear the sensitivity of the corresponding system CIRQ.

102041C4 CIRQ_SENS_CLR1 System CIRQ Sensitivity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_CLR1[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR1[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_CLR1	Write 1 to specific bit to clear the sensitivity of the corresponding system CIRQ.

102041C8 CIRQ_SENS_CLR2 System CIRQ Sensitivity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_CLR2[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR2[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_CLR2	Write 1 to specific bit to clear the sensitivity of the corresponding system CIRQ.

102041CC CIRQ_SENS_CLR3 System CIRQ Sensitivity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_CLR3[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR3[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_CLR3	Write 1 to specific bit to clear the sensitivity of the corresponding system CIRQ.

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102041D0 **CIRQ_SENS_CLR4** **System CIRQ Sensitivity Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_SENS_CLR4[30:16]														
Type		WO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR4[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_SENS_CLR4	Write 1 to specific bit to clear the sensitivity of the corresponding system CIRQ.

10204200 **CIRQ_POL0** **External Interrupt Polarity Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL0[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL0[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL0	System CIRQ polarity value

10204204 **CIRQ_POL1** **External Interrupt Polarity Register** **00038000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL1[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL1[15:0]															
Type	RO															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL1	System CIRQ polarity value

10204208 **CIRQ_POL2** **External Interrupt Polarity Register** **00102001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL2[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	**CIRQ_POL2[15:0]**															
Type	RO															
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL2	System CIRQ polarity value

1020420C CIRQ_POL3 External Interrupt Polarity Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CIRQ_POL3[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CIRQ_POL3[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL3	System CIRQ polarity value

10204210 CIRQ_POL4 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**CIRQ_POL4[30:16]**														
Type		RO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CIRQ_POL4[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_POL4	System CIRQ polarity value

10204240 CIRQ_POL_SET0 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CIRQ_POL_SET0[31:16]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CIRQ_POL_SET0[15:0]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_SET0	Write 1 to specific bit to set up the polarity of the corresponding system CIRQ.

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10204244 **CIRQ_POL_SET1** **External Interrupt Polarity Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_SET1[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET1[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_SET1	Write 1 to specific bit to set up the polarity of the corresponding system CIRQ.

10204248 **CIRQ_POL_SET2** **External Interrupt Polarity Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_SET2[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET2[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_SET2	Write 1 to specific bit to set up the polarity of the corresponding system CIRQ.

1020424C **CIRQ_POL_SET3** **External Interrupt Polarity Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_SET3[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET3[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_SET3	Write 1 to specific bit to set up the polarity of the corresponding system CIRQ.

10204250 **CIRQ_POL_SET4** **External Interrupt Polarity Set Register** **00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_POL_SET4[30:16]														
Type		WO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET4[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_POL_SET4	Write 1 to specific bit to set up the polarity of the corresponding system CIRQ.

10204280 **CIRQ_POL_CLR0** **External Interrupt Polarity Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_CLR0[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR0[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_CLR0	Write 1 to specific bit to clear the polarity of the corresponding system CIRQ.

10204284 **CIRQ_POL_CLR1** **External Interrupt Polarity Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_CLR1[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR1[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_CLR1	Write 1 to specific bit to clear the polarity of the corresponding system CIRQ.

10204288 **CIRQ_POL_CLR2** **External Interrupt Polarity Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_CLR2[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	**CIRQ_POL_CLR2[15:0]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_CLR2	Write 1 to specific bit to clear the polarity of the corresponding system CIRQ.

1020428C CIRQ_POL_CLR3 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CIRQ_POL_CLR3[31:16]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CIRQ_POL_CLR3[15:0]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_CLR3	Write 1 to specific bit to clear the polarity of the corresponding system CIRQ.

10204290 CIRQ_POL_CLR4 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**CIRQ_POL_CLR4[30:16]**														
Type		WO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CIRQ_POL_CLR4[15:0]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_POL_CLR4	Write 1 to specific bit to clear the polarity of the corresponding system CIRQ.

10204300 CIRQ_CON System CIRQ Control Register 80000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CIRQ_EVENT_B**															
Type	RO															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**CIRQ_FLUS**	**CIRQ_EDGE**	**CIRQ_EN**

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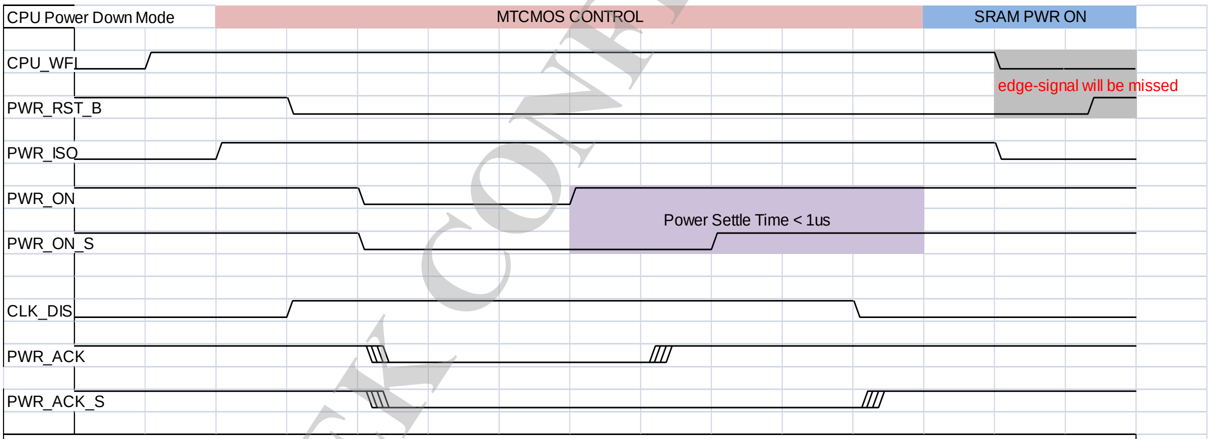
														H	_ON LY	
Type														WO	RW	RW
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
31		CIRQ_EVENT_B	**Indicates sys_cirq_irq_b is triggered**
2		CIRQ_FLUSH	**Flushes pending interrupts**
1		CIRQ_EDGE_ONLY	**Sets up edge-only mode** Only edge-triggered interrupt will be recorded.
0		CIRQ_EN	**Enable bit of system CIRQ controller**

3.4.5 Programming Guide

3.4.5.1 MCUSYS MTCMOS Sequence



Note:
1. MEM_CKISO should connect to PISO cell to isolate the CLOCK and CHIP SEL input ports of SRAM to LOW
2. All the MEM_PDN and MEM_SLEEP_B signals come from the SPM in always power on domain.
3. MEM_SLEEP_B should always keep HIGH when SRAM power down
4. All the signals are controled by CPU(Software) or SPM

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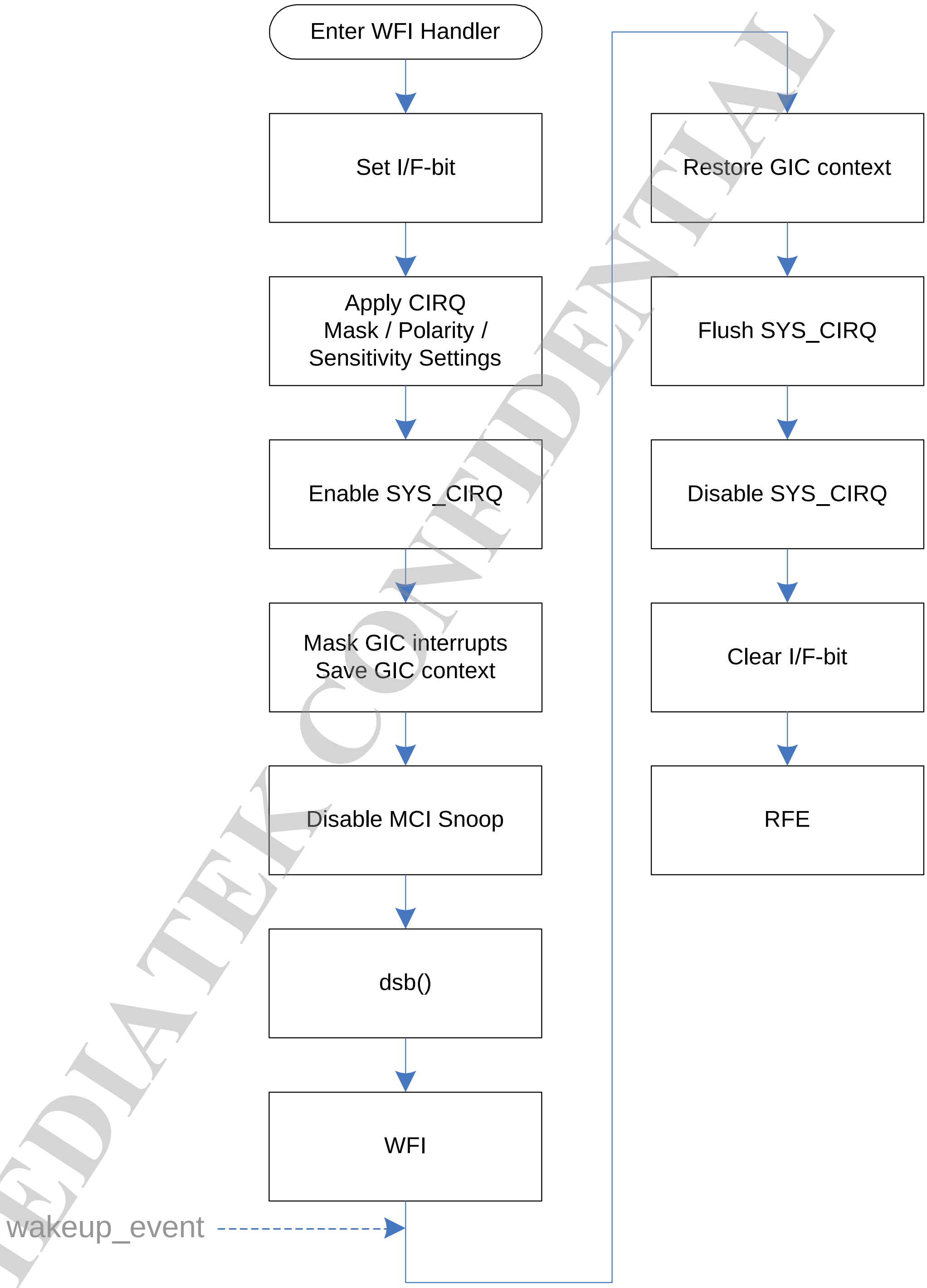
3.4.5.2 SW Flow



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3.5 Infrastructure System Configuration Module

3.5.1 Introduction

The infrastructure system configuration module (INFRACFG) provides reset, clock and miscellaneous control signals in the infrastructure system.

3.5.2 Features

INFRACFG provides the following control signals to the functional blocks inside the infrastructure system:

- Software reset signals
- Clock gating control signals
- Dynamic clock management control signals
- Top AXI bus fabric control signals
- Dynamic clock management function

3.5.2.1 DCM in Details

The dynamic clock management function is used to slow down the clock frequency for power saving when the system is in idle state automatically.

Figure 3-6 gives a sample clock waveform when DCM is activated. In this example, the clock frequency in DCM mode is set to quarter of the original clock. The ratio of clock frequency slow-down is controlled by the INFRA_DCMFSEL register.

After the bus idle signal is low, it will take several cycles of latency to make the slow-down clock return to the normal frequency. The cycle number varies with the runtime status of the clock gating logic and will somehow cause minor performance impact. In order to minimize the impact when the system is in heavy load status, the INFRA_DCMDBC register controls the cycle count once the bus idle signal is asserted. Setting the de-bounce cycle to be longer and enabling the function will reduce the probability of the system entering the DCM mode.

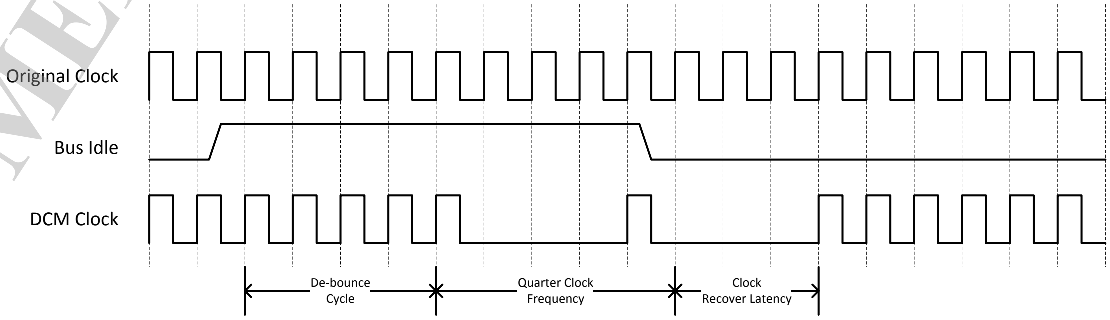

Figure 3-6. DCM in action

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3.5.2.2 AXI Fabric Control

The AXI fabric control registers help prevent the system bus from hanging up caused by improper access while some parts of the system are in the power-down state. See the figure below for the location of SI node 0 to SI node 4 and the sleep protector and find the corresponding control registers in section 3.5.3 "Register Definition".

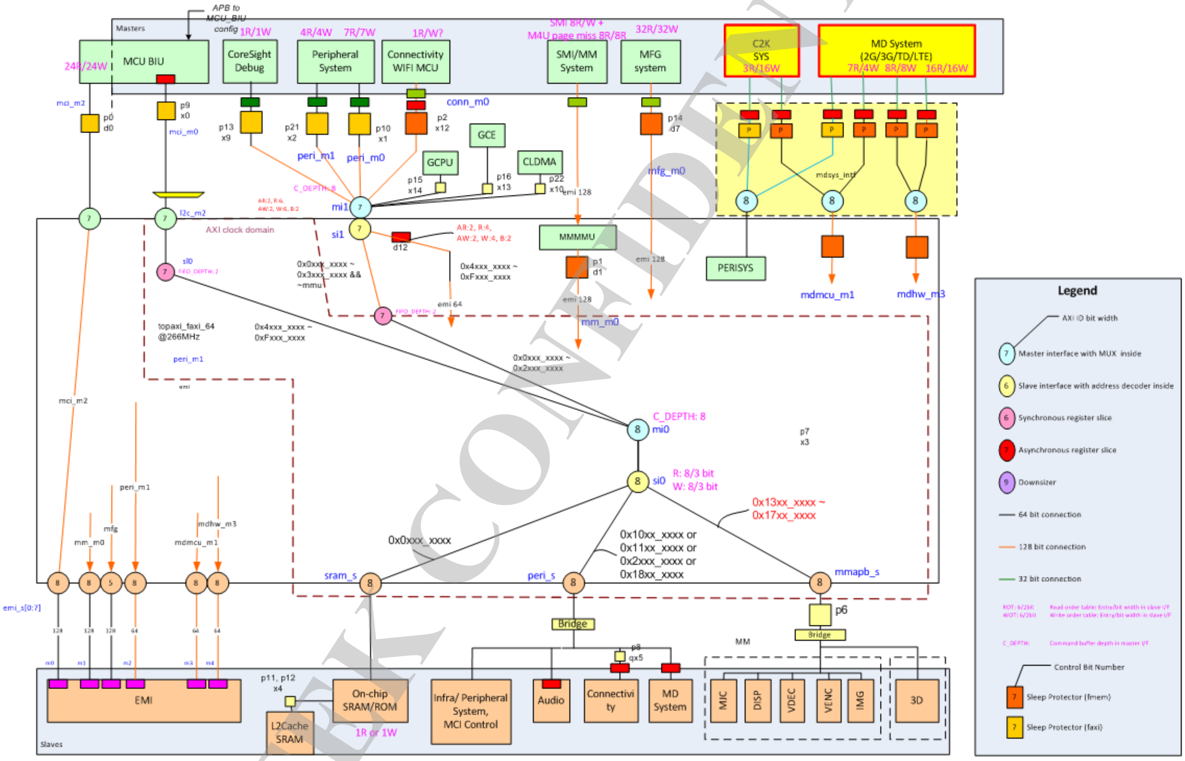

Figure 3-7. Top AXI fabric and control blocks

3.5.3 Register Definition

Module name: infracfg_ao_reg Base address: (+10000000h)

Address	Name	Width	Register Function
10000000	TOP_CKMUXSEL	32	TOPCKGEN Clock MUX Control Register
10000008	TOP_CKDIV1	32	TOPCKGEN Clock Divider 1 Control Register
10000010	INFRA_TOPCKGEN_DCMCTL	32	TOPCKGEN Cortex-A7 DCM Control Register
10000014	INFRA_TOPCKGEN_DCMDBC	32	TOPCKGEN DCM Debounce Control Register
10000030	INFRA_RST0	32	Infrasys Reset Control Register SET
10000034	INFRA_RST1	32	Infrasys Reset Control Register CLEAR
10000040	INFRA_GLOBALCON_PDN0	32	Infrasys Power Down Set Register

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Address	Name	Width	Register Function
10000044	INFRA_PDN1	32	Infrasys Power Down Clear Register
10000048	INFRA_PDN_STA	32	Infrasys Power Down Status Register
10000050	INFRA_GLOBALCON_DCMCTL	32	Infrasys DCM Control Register
10000054	INFRA_GLOBALCON_DCMDBC	32	Infrasys DCM Debounce Register
10000058	INFRA_GLOBALCON_DCMFSEL	32	Infrasys DCM Frequency Control Register
10000060	INFRA_MDSYS1_CTRL_PDN0	32	MDSYS1 Control Infrasys Power Down Set Register
10000064	INFRA_MDSYS1_CTRL_PDN1	32	MDSYS1 Control Infrasys Power Down Clear Register
10000068	INFRA_MDSYS2_CTRL_PDN0	32	MDSYS2 Control Infrasys Power Down Set Register
1000006C	INFRA_MDSYS2_CTRL_PDN1	32	MDSYS2 Control Infrasys Power Down Clear Register
1000018C	INFRA_AO_MBIST_RESULT	32	infra_ao MBIST Result Register
100001A0	INFRA_AO_MBIST_DELSEL	32	infra_ao DELSEL SRAM MBIST Control Register
100001A4	INFRA_AO_MBIST_BSEL	32	infra_ao BSEL SRAM MBIST Control Register
100001A8	INFRA_AO_MBIST_DEBUG	32	infra_ao MBIST DEBUG Register
100001AC	INFRA_AO_MBIST_FUSE_MON	32	
100001B0	INFRA_AO_MBIST_HOLDB	32	infra_ao MBIST HOLDB Register
100001B4	INFRA_AO_MBIST_MODE	32	infra_ao MBIST Mode Register
100001B8	INFRA_AO_MBIST_MON_SEL	32	infra_ao MBIST Monitor Sel Register
100001C0	INFRA_AO_MBIST_FUSE_GPU	32	infra_ao MBIST GPU Fuse Register
100001EC	INFRA_AO_MBIST_FUSE_MM	32	infra_ao MBIST MM Fuse Register
10000200	TOPAXI_SI0_CTL	32	Top AXI Fabric SI0 Control Register
10000204	TOPAXI_SI1_CTL	32	Top AXI Fabric SI1 Control Register
10000208	TOPAXI_MDBUS_CTRL	32	MDSYS AXI Fabric Control Register
10000220	TOPAXI_PROT_EN	32	Top AXI Protect Module Control Register
10000224	TOPAXI_PROT_STA0	32	Top AXI Protect Module Status Register 0
10000228	TOPAXI_PROT_STA1	32	Top AXI Protect Module Status Register 1
1000022C	TOPAXI_AXI_ASLICE_CTRL	32	Top AXI Aslice Control Register
10000300	MD1_BANK0_	32	MDSYS1 Bank0 Remap Register 0

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Address	Name	Width	Register Function
	MAP0		
10000304	MD1_BANK0_MAP1	32	MDSYS1 Bank0 Remap Register 1
10000308	MD1_BANK4_MAP0	32	MDSYS1 Bank4 Remap Register 0
1000030C	MD1_BANK4_MAP1	32	MDSYS1 Bank4 Remap Register 1
10000310	MD2_BANK0_MAP0	32	MDSYS2 Bank0 Remap Register 0
10000314	MD2_BANK0_MAP1	32	MDSYS2 Bank0 Remap Register 1
10000318	MD2_BANK4_MAP0	32	MDSYS2 Bank4 Remap Register 0
1000031C	MD2_BANK4_MAP1	32	MDSYS2 Bank4 Remap Register 1
10000320	CONN_MAP0	32	CONNSYS EMI Address Remap Register
10000324	CONN_SIDEBAND	32	CONSYS to Bus Sideband Signals
10000330	C2K_CONFIG	32	C2K AP Config
10000334	C2K_STATUS	32	C2K Status
10000338	C2K_SPM_CTRL	32	C2k SPM Control
10000340	LTE_OCCUPYANT	32	LTE Occupy ant
10000344	C2K_OCCUPYANT	32	C2K Occupy ant
1000034C	CLDMA_CTRL	32	CLDMA Control Register
10000500	INFRA_AO_DBG_CON0	32	INFRA_AO Debug Control 0
10000504	INFRA_AO_DBG_CON1	32	INFRA_AO Debug Control 1
10000508	INFRA_AO_DBG_CON2	32	INFRA_AO Debug Control 2
1000050C	INFRA_AO_DBG_CON3	32	INFRA_AO Debug Control 3
10000700	INFRA_MISC	32	Infrasys Miscellaneous Control Register
10000704	INFRA_ACP	32	Infrasys CPU Coherence Control Register
10000708	INFRA_BONDING	32	INFRA_BONDING
10000800	SRAMROM_BOOT_ADDR	32	SRAMROM Boot Address Register
10000804	SRAMROM_SEC_CTRL	32	SRAMROM Secure Control Register
10000808	SRAMROM_SEC_ADDR	32	SRAMROM Region Address Register
1000080C	SRAMROM_FPC_BOOT_ADDR	32	SRAMROM Region Address Register
10000810	SRAMROM_FPC_BOOT_CON	32	SRAMROM FPC Boot Control Register
10000814	SRAMROM_SEC_CTRL2	32	SRAMROM Secure Control Register
10000818	SRAMROM_BOOT_MISC0	32	SRAMROM Spare Register 0
1000081C	SRAMROM_BO	32	SRAMROM Spare Register 1

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Address	Name	Width	Register Function
	OT_MISC1		
10000820	SRAMROM_BOOT_MISC2	32	SRAMROM Spare Register 2
10000824	SRAMROM_BOOT_MISC3	32	SRAMROM Spare Register 3
10000828	SRAMROM_BOOT_MISC4	32	SRAMROM Spare Register 4
1000082C	SRAMROM_BOOT_MISC5	32	SRAMROM Spare Register 5
10000830	SRAMROM_BOOT_MISC6	32	SRAMROM Spare Register 6
10000834	SRAMROM_BOOT_MISC7	32	SRAMROM Spare Register 7
10000838	SRAMROM_MISC_LOCK_KEY	32	SRAMROM_MISC_LOCK_KEY
1000083C	SRAMROM_MISC_LOCK_CON	32	SRAMROM_MISC_LOCK_CON
10000840	SRAMROM_MISC_RST_CON	32	SRAMROM_MISC_RST_CON
10000844	SRAMROM_MISC_SEC_CON	32	SRAMROM_MISC_SEC_CON
10000F00	INFRA_AO_SEC_CON	32	INFRA AO Secure Control Register
10000F10	GCPU_SEC_CON	32	GCPU AO Control Register

10000000 TOP_CKMUXSEL TOPCKGEN Clock MUX Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name													mux1_sel			
Type													RW			
Reset													0	0		

Bit(s)	Mnemonic	Name	Description
3:2		mux1_sel	**Selects TOPCKGEN ARMPLL clock MUX 1** 00: CLKSQ 01: ARMPLL 10: MAINPLL 11: 1'b0

10000008 TOP_CKDIV1 TOPCKGEN Clock Divider 1 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name												clkdiv1_sel				
Type												RW				

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Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		clkdiv1_sel	TOPCKGEN ARMPLL clock divider 1 setting

10000010 **INFRA_TOPCKGEN_DCMCTL** **TOPCKGEN Cortex-A7 DCM Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**arm_dcm_wfe_enable**	**arm_dcm_wfi_enable**	**infra_dcm_enable**
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2		arm_dcm_wfe_enable	**Enables CortexA7 DCM in WFE mode** 0: Disable 1: Enable
1		arm_dcm_wfi_enable	**Enables CortexA7 DCM in WFI mode** 0: Disable 1: Enable
0		infra_dcm_enable	**Enables TOP Bus DCM** 0: Disable 1: Enable

10000014 **INFRA_TOPCKGEN_DCMDBC** **TOPCKGEN DCM Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**topckgen_dcm_dbc_cnt**						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6:0		topckgen_dcm_dbc_cnt	DCM debouncing counter

10000030 **INFRA_RST0** **Infrasys Reset Control Register SET** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name						cldma_top_pd_rst	ccif1_rst	mm_iommu_rst	gce_rst	sys_cirq_rst	trng_rst	ccif_ao_rst	emi_ao_reg_rst	dramco_rst	ccif_rst	emi_rst
Type						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							usbsif_top_rst	cldma_ao_top_rst	pmic_wrap_rst	kp_rst	scpsys_rst	apxgpt_rst	ap_cirq_eint_rst		dramco_ao_rst	emi_reg_rst
Type							RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset							0	0	0	0	0	0	0		0	0

Bit(s)	Mnemonic	Name	Description
26		cldma_top_pd_rst	**CLDMA PDN software reset** 0: Normal 1: Enable reset
25		ccif1_rst	**CCIF1 software reset** 0: Normal 1: Enable reset
24		mm_iommu_rst	**mm_iommu software reset** 0: Normal 1: Enable reset
23		gce_rst	**GCE software reset** 0: Normal 1: Enable reset
22		sys_cirq_rst	**SYSCIRQ software reset** 0: Normal 1: Enable reset
21		trng_rst	**TRNG software reset** 0: Normal 1: Enable reset
20		ccif_ao_rst	**CCIF software reset** 0: Normal 1: Enable reset
19		emi_ao_reg_rst	**EMI APB software reset** 0: Normal 1: Enable reset
18		dramco_rst	**DRAMC software reset** 0: Normal 1: Enable reset
17		ccif_rst	**CCIF software reset** 0: Normal 1: Enable reset
16		emi_rst	**EMI software reset** 0: Normal 1: Enable reset
9		usbsif_top_rst	**usbsif_top software reset** 0: Normal 1: Enable reset
8		cldma_ao_top_rst	**cldma_ao_top_ software reset** 0: Normal 1: Enable reset
7		pmic_wrap_rst	**PMIC wrapper software reset** 0: Normal

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Bit(s)	Mnemonic	Name	Description
			1: Enable reset
6		kp_rst	**Keypad software reset** 0: Normal 1: Enable reset
5		scpsys_rst	**SCPSYS software reset** 0: Normal 1: Enable reset
4		apxgpt_rst	**apxgpt software reset** 0: Normal 1: Enable reset
3		ap_cirq_eint_rst	**EINT software reset** 0: Normal 1: Enable reset
1		dramc0_ao_rst	**DRAMC 0 software reset** 0: Normal 1: Enable reset
0		emi_reg_rst	**EMI APB software reset** 0: Normal 1: Enable reset

10000034 **INFRA_RST1** **Infrasys Reset Control Register CLEAR** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						cldma_top_pd_rst	ccif1_rst	mm_iommu_rst	gce_rst	sys_cirq_rst	trng_rst	ccif_ao_rst	emi_ao_reg_rst	dramco_rst	ccif_rst	emi_rst
Type						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								cldma_ao_top_rst	pmic_wrap_rst	kp_rst	scpsys_rst	apxgpt_rst	ap_cirq_eint_rst		dramco_ao_rst	emi_reg_rst
Type								RW	RW	RW	RW	RW	RW		RW	RW
Reset								0	0	0	0	0	0		0	0

Bit(s)	Mnemonic	Name	Description
26		cldma_top_pd_rst	**CLDMA PDN software reset** 0: Normal 1: Enable reset
25		ccif1_rst	**CCIF1 software reset** 0: Normal 1: Enable reset
24		mm_iommu_rst	**mm_iommu software reset** 0: Normal 1: Enable reset
23		gce_rst	**GCE software reset** 0: Normal 1: Enable reset
22		sys_cirq_rst	**SYSCIRQ software reset** 0: Normal 1: Enable reset

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Bit(s)	Mnemonic	Name	Description
21		trng_rst	**TRNG software reset** 0: Normal 1: Enable reset
20		ccif_ao_rst	**CCIF software reset** 0: Normal 1: Enable reset
19		emi_ao_reg_rst	**EMI APB software reset** 0: Normal 1: Enable reset
18		dramco_rst	**DRAMC software reset** 0: Normal 1: Enable reset
17		ccif_rst	**CCIF software reset** 0: Normal 1: Enable reset
16		emi_rst	**EMI software reset** 0: Normal 1: Enable reset
8		cldma_ao_top_rst	**cldma_ao_top_ software reset** 0: Normal 1: Enable reset
7		pmic_wrap_rst	**PMIC wrapper software reset** 0: Normal 1: Enable reset
6		kp_rst	**Keypad software reset** 0: Normal 1: Enable reset
5		scpsys_rst	**SCPSYS software reset** 0: Normal 1: Enable reset
4		apxgpt_rst	**APXGPT software reset** 0: Normal 1: Enable reset
3		ap_cirq_eint_rst	**EINT software reset** 0: Normal 1: Enable reset
1		dramco_ao_rst	**DRAMC 0 software reset** 0: Normal 1: Enable reset
0		emi_reg_rst	**EMI APB software reset** 0: Normal 1: Enable reset

10000040 **INFRA_GLOBALCON_PDN0** **Infrasys Power Down Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									pmic_wrap_pdn	pmic_spi_pdn	ccif1_ap_ctrl_pdn	ccif0_ap_ctrl_pdn	sej_pdn	apxgpt_pdn		kp_pdn
Type									RW	RW	RW	RW	RW	RW		RW
Reset									0	0	0	0	0	0		0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**connmcu_bus_pdn**			**cldma_pdn**	**md1ahb_bus_pdn**	**md1hwmix_bus_pdn**	**md1mcu_bus_pdn**	**m4u_pdn**	**l2c_sram_pdn**	**gcpu_pdn**	**audio_pdn**	**devapc_pdn**	**cpum_pdn**	**trng_pdn**	**gce_pdn**	**dbgclk_pdn**
Type	RW			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23		pmic_wrap_pdn	**Sets up PMIC_WRAP clock power-down (AP control)** 0: Unchanged 1: Clock-off
22		pmic_spi_pdn	**Sets up PMIC SPI clock power-down (AP control)** 0: Unchanged 1: Clock-off
21		ccif1_ap_ctrl_pdn	**Sets up CCIF1 clock power-down (AP control)** 0: Unchanged 1: Clock-off
20		ccif0_ap_ctrl_pdn	**Sets up CCIF0 clock power-down (AP control)** 0: Unchanged 1: Clock-off
19		sej_pdn	**Sets up SEJ clock power-down** 0: Unchanged 1: Clock-off
18		apxgpt_pdn	**Sets up KP clock power-down** 0: Unchanged 1: Clock-off
16		kp_pdn	**Sets up KP clock power-down** 0: Unchanged 1: Clock-off
15		connmcu_bus_pdn	**Sets up CONNSYS MCU AXI clock power-down** 0: Unchanged 1: Clock-off
12		cldma_pdn	**Sets up CLDMA clock power-down** 0: Unchanged 1: Clock-off
11		md1ahb_bus_pdn	**Sets up MDSYS1 AHB clock power-down** 0: Unchanged 1: Clock-off
10		md1hwmix_bus_pdn	**Sets up MDSYS1 HWMIX AXI clock power-down** 0: Unchanged 1: Clock-off
9		md1mcu_bus_pdn	**Sets up MDSYS1 CR4 AXI clock power-down** 0: Unchanged 1: Clock-off
8		m4u_pdn	**Sets up M4U clock power-down** 0: Unchanged 1: Clock-off
7		l2c_sram_pdn	**Sets up L2C SRAM clock power-down** 0: Unchanged 1: Clock-off
6		gcpu_pdn	**Sets up GCPU clock power-down** 0: Unchanged 1: Clock-off

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Bit(s)	Mnemonic	Name	Description
5		audio_pdn	**Sets up AUDIO clock power-down** 0: Unchanged 1: Clock-off
4		devapc_pdn	**Sets up DEVICE APC power-down** 0: Unchanged 1: Clock-off
3		cpum_pdn	**Sets up CPUM clock power-down** 0: Unchanged 1: Clock-off
2		trng_pdn	**Sets up TRNG clock power-down** 0: Unchanged 1: Clock-off
1		gce_pdn	**Sets up GCE clock power-down** 0: Unchanged 1: Enable clock
0		dbgclk_pdn	**Sets up debug system clock power-down** 0: Unchanged 1: Clock-off

10000044 INFRA_PDN1 Infrasys Power Down Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									pmic_wrap_pdn	pmic_spi_pdn	ccif1_ap_ctrl_pdn	ccif0_ap_ctrl_pdn	sej_pdn	apxgpt_pdn		kp_pdn
Type									RW	RW	RW	RW	RW	RW		RW
Reset									0	0	0	0	0	0		0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	connmcu_bus_pdn			cldma_pdn	md1ahb_bus_pdn	md1hwmix_bus_pdn	md1mcu_bus_pdn	m4u_pdn	l2c_sram_pdn	gcpu_pdn	audio_pdn	devapc_pdn	cpum_pdn	trng_pdn	gce_pdn	dbgclk_pdn
Type	RW			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23		pmic_wrap_pdn	**Clears PMIC_WRAP clock power-down (AP control)** 0: Unchanged 1: Enable clock
22		pmic_spi_pdn	**Clears PMIC SPI clock power-down (AP control)** 0: Unchanged 1: Enable clock
21		ccif1_ap_ctrl_pdn	**Clears CCIF1 clock power-down (AP control)** 0: Unchanged 1: Enable clock
20		ccif0_ap_ctrl_pdn	**Clears CCIF0 clock power-down (AP control)** 0: Unchanged 1: Enable clock
19		sej_pdn	**Clears SEJ clock power-down** 0: Unchanged 1: Enable clock
18		apxgpt_pdn	**Clears APXGPT clock power-down** 0: Unchanged

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Bit(s)	Mnemonic	Name	Description
			1: Enable clock
16		kp_pdn	**Clears KP clock power-down** 0: Unchanged 1: Enable clock
15		connmcu_bus_pdn	**Sets up CONNSYS MCU AXI clock power-down** 0: Unchanged 1: Enable clock
12		cldma_pdn	**Clears CLDMA clock power-down** 0: Unchanged 1: Clock-off
11		md1ahb_bus_pdn	**Clears MDSYS1 AHB clock power-down** 0: Unchanged 1: Enable clock
10		md1hwmix_bus_pdn	**Clears MDSYS1 HWMIX AXI clock power-down** 0: Unchanged 1: Enable clock
9		md1mcu_bus_pdn	**Clears MDSYS1 CR4 AXI clock power-down** 0: Unchanged 1: Enable clock
8		m4u_pdn	**Clears M4U clock power-down** 0: Unchanged 1: Enable clock
7		l2c_sram_pdn	**Clears L2C SRAM clock power-down** 0: Unchanged 1: Enable clock
6		gcpu_pdn	**Clears GCPU clock power-down** 0: Unchanged 1: Enable clock
5		audio_pdn	**Clears AUDIO clock power-down** 0: Unchanged 1: Enable clock
4		devapc_pdn	**Clears DEVICE APC power-down** 0: Unchanged 1: Enable clock
3		cpum_pdn	**Clears CPUM clock power- down** 0: Unchanged 1: Enable clock
2		trng_pdn	**Clears TRNG clock power-down** 0: Unchanged 1: Enable clock
1		gce_pdn	**Clears GCE clock power-down** 0: Unchanged 1: Enable clock
0		dbgclk_pdn	**Clears debug system clock power-down** 0: Unchanged 1: Enable clock

10000048 **INFRA_PDN_STA** **Infrasys Power Down Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name									pmic_wrap_share_pdn_sta	pmic_spi_share_pdn_sta	ccif1_share_pdn_sta	ccif0_share_pdn_sta	sejpdn_sta	apxgpt_pdn_sta		kp_pdn_sta
Type									RU	RU	RU	RU	RU	RU		RU
Reset									0	0	0	0	0	0		0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	connmcu_bus_pdn			cldma_pdn_sta	md1ahb_bus_pdn_sta	md1hwmix_bus_pdn_sta	md1mcu_bus_pdn_sta	m4u_pdn_sta	l2c_sram_pdn_sta	efuse_pdn_sta	audio_pdn_sta	devapc_sta	cpum_sta	trng_sta	gce_sta	dbgclk_sta
Type	RW			RU	RU	RU	RU	RU	RU	RU	RU	RW	RW	RW	RW	RW
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23		pmic_wrap_share_pdn_sta	**PMIC_WRAP clock power-down status** 0: Unchanged 1: Clock-off
22		pmic_spi_share_pdn_sta	**PMIC SPI clock power-down status** 0: Unchanged 1: Clock-off
21		ccif1_share_pdn_sta	**CCIF1 clock power-down status (AP & MD control)** 0: Unchanged 1: Clock-off
20		ccif0_share_pdn_sta	**CCIF0 clock power-down status (AP & MD control)** 0: Unchanged 1: Clock-off
19		sejpdn_sta	**SEJ clock power-down status** 0: Unchanged 1: Clock-off
18		apxgpt_pdn_sta	**apxgpt clock power-down status** 0: Unchanged 1: Clock-off
16		kp_pdn_sta	**KP clock power-down status** 0: Unchanged 1: Clock-off
15		connmcu_bus_pdn	**CONNSYS MCU AXI clock power down status** 0: Unchanged 1: Clock-off
12		cldma_pdn_sta	**CLDMA AXI clock power-down status** 0: Unchanged 1: Clock-off
11		md1ahb_bus_pdn_sta	**MDSYS1 AHB clock power-down status** 0: Unchanged 1: Clock-off
10		md1hwmix_bus_pdn_sta	**MDSYS1 HWMIX AXI clock power-down status** 0: Unchanged 1: Clock-off
9		md1mcu_bus_pdn_sta	**MDSYS1 CR4 AXI clock power-down status** 0: Unchanged 1: Clock-off
8		m4u_pdn_sta	**M4U clock power-down status** 0: Unchanged 1: Clock-off

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Bit(s)	Mnemonic	Name	Description
7		l2c_sram_pdn_sta	**L2C SRAM AXI clock power-down status** 0: Unchanged 1: Clock-off
6		efusec_pdn_sta	**EFUSEC clock power-down status** 0: Unchanged 1: Clock-off
5		audio_pdn_sta	**AUDIO clock power-down status** 0: Unchanged 1: Clock-off
4		devapc_sta	**DEVICE APC power down status** 0: Unchanged 1: Enable clock
3		cpum_sta	**CPUM clock power down status** 0: Unchanged 1: Enable clock
2		trng_sta	**TRNG clock power down status** 0: Unchanged 1: Enable clock
1		gce_sta	**GCE clock power down status** 0: Unchanged 1: Enable clock
0		dbgclk_sta	**Debug system clock power down status** 0: Unchanged 1: Enable clock

10000050 **INFRA_GLOBALCON_DCMCTL** **Infrasys DCM Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**l2c_sram_infra_dcm_en**	**axi_clock_gated_en**							**fmem_dcm_enable**	**faxi_dcm_enable**
Type							RW	RW							RW	RW
Reset							0	0							0	0

Bit(s)	Mnemonic	Name	Description
9		l2c_sram_infra_dcm_en	**Enables L2C SRAM DCM** 0: Disable 1: Enable
8		axi_clock_gated_en	**Stops AXI clock in DCM mode** 0: Disable 1: Enable
1		fmem_dcm_enable	**Enables AXI clock DCM** 0: Disable 1: Enable
0		faxi_dcm_enable	**Enables EMI clock DCM**

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Bit(s)	Mnemonic	Name	Description
			0: Disable 1: Enable

10000054 **INFRA_GLOBALCON_DCMDBC** **Infrasys DCM Debounce Register** **007F007F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								dcm_dbc_enable_fmem		dcm_dbc_cnt_fmem						
Type								RW		RW						
Reset								0		1	1	1	1	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name								faxi_dcm_dbc_enable		dcm_dbc_cnt						
Type								RW		RW						
Reset								0		1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
24		dcm_dbc_enable_fmem	**Enables DCM debouncing counter for FMEM** 0: Disable 1: Enable
22:16		dcm_dbc_cnt_fmem	**DCM debouncing counter for FMEM**
8		faxi_dcm_dbc_enable	**Enables DCM debouncing counter for AXI clock** 0: Disable 1: Enable
6:0		dcm_dbc_cnt	**DCM debouncing counter**

10000058 **INFRA_GLOBALCON_DCMFSEL** **Infrasys DCM Frequency Control Register** **0F0F0703**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				dcm_full_fsel_fmem								dcm_full_fsel				
Type				RW								RW				
Reset				0	1	1	1	1				0	1	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					dcm_half_fsel									dcm_qtr_fsel		
Type					RW									RW		
Reset					0	1	1	1						0	1	1

Bit(s)	Mnemonic	Name	Description
28:24		dcm_full_fsel_fmem	**Selects DCM frequency for full speed clock** 1xxxx: 1/1 01xxx: 1/2 001xx: 1/4 0001x: 1/8 00001: 1/16

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Bit(s)	Mnemonic	Name	Description
			00000: 1/32
20:16		dcm_full_fsel	**Selects DCM frequency for full speed clock** 1xxxx: 1/1 01xxx: 1/2 001xx: 1/4 0001x: 1/8 00001: 1/16 00000: 1/32
11:8		dcm_half_fsel	**Selects DCM frequency for half speed clock** 1xxx: 1/2 01xx: 1/4 001x: 1/8 0001: 1/16 0000: 1/32
2:0		dcm_qtr_fsel	**Selects DCM frequency for quarter speed clock** 1xx: 1/4 01x: 1/8 001: 1/16 000: 1/32

10000060 **INFRA_MDSYS1_CTRL_PDN0** **MDSYS1 Control Infrasys Power Down Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									md1_pmic_wrap_pdn		md1_ccif1_md_ctrl_pdn	md1_ccifo_md_ctrl_pdn				
Type									RW		RW	RW				
Reset									0		0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
23		md1_pmic_wrap_pdn	**Sets up PMIC_WRAP clock power-down (MDSYS1 control)** 0: Unchanged 1: Clock-off
21		md1_ccif1_md_ctrl_pdn	**Sets up CCIF1 clock power-down (MDSYS1 control)** 0: Unchanged 1: Clock-off
20		md1_ccifo_md_ctrl_pdn	**Sets up CCIF0 clock power-down (MDSYS1 control)** 0: Unchanged 1: Clock-off

10000064 **INFRA_MDSYS1_CTRL_PDN1** **MDSYS1 Control Infrasys Power Down Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									md1_		md1_	md1_				

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									pmic_wrap_pdn		ccif1_md_ctrl_pdn	ccif0_md_ctrl_pdn				
Type									RW		RW	RW				
Reset									0		0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
23		md1_pmic_wrap_pdn	**Clears PMICWRAP clock power-down (MDSYS1 control)** 0: Unchanged 1: Enable clock
21		md1_ccif1_md_ctrl_pdn	**Sets up CCIF1 clock power-down (MDSYS1 control)** 0: Unchanged 1: Clock-off
20		md1_ccif0_md_ctrl_pdn	**Clears CCIF0 clock power-down (MDSYS1 control)** 0: Unchanged 1: Clock-off

10000068 **INFRA_MDSYS2_CTRL_PDN0** **MDSYS2 Control Infrasys Power Down Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									md2_pmic_wrap_pdn		md2_ccif1_md_ctrl_pdn	md2_ccif0_md_ctrl_pdn				
Type									RW		RW	RW				
Reset									0		0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
23		md2_pmic_wrap_pdn	**Sets up PMIC_WRAP clock power-down (MDSYS2 control)** 0: Unchanged 1: Clock-off
21		md2_ccif1_md_ctrl_pdn	**Sets up CCIF1 clock power-down (MDSYS2 control)** 0: Unchanged 1: Clock-off
20		md2_ccif0_md_ctrl_pdn	**Sets up CCIF0clock power-down (MDSYS2 control)** 0: Unchanged 1: Clock-off

1000006C **INFRA_MDSYS2_CTRL_PDN1** **MDSYS2 Control Infrasys Power Down Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name									**md2_pmic_wrap_pdn**		**md2_ccif1_md_ctrl_pdn**	**md2_ccif0_md_ctrl_pdn**				
Type									RW		RW	RW				
Reset									0		0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
23		md2_pmic_wrap_pdn	**Clears PMICWRAP clock power-down (MDSYS2 control)** 0: Unchanged 1: Enable clock
21		md2_ccif1_md_ctrl_pdn	**Clears CCIF1 clock power-down (MDSYS2 control)** 0: Unchanged 1: Enable clock
20		md2_ccif0_md_ctrl_pdn	**Clears CCIF0 clock power-down (MDSYS2 control)** 0: Unchanged 1: Enable clock

1000018C **INFRA_AO_MBIST_RESULT** **infra_ao MBIST Result Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**sramrom_mbisr_rp_fail_1**													**fhctl_mbist_fail_0**	**scpsys_mbist_fail_1**	**scpsys_mbist_fail_0**
Type	RO													RO	RO	RO
Reset	0	0	0	0										0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**fhctl_mbist_done**	**scpsys_mbist_done**
Type															RO	RO
Reset															0	0

Bit(s)	Mnemonic	Name	Description
31:28		sramrom_mbisr_rp_fail_1	**sramrom_mbisr_rp_fail[11:8]** 0: Pass 1: Fail
18		fhctl_mbist_fail_0	**fhctl_mbist_fail_0** 0: Pass 1: Fail
17		scpsys_mbist_fail_1	**scpsys_mbist_fail_1** 0: Pass 1: Fail
16		scpsys_mbist_fail_0	**scpsys_mbist_fail_0** 0: Pass 1: Fail
1		fhctl_mbist_done	**fhctl_mbist_done** 0: Not done

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Bit(s)	Mnemonic	Name	Description
			1: Done
0		scpsys_mbist_done	**scpsys_mbist_done** 0: Not done 1: Done

100001A0 **INFRA_AO_MBIST_DELSEL** **infra_ao DELSEL SRAM MBIST Control Register** **00000AAA**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**infra_ao_fhctl_mem_delsel**				**infra_ao_scpsys_mem1_delsel**				**infra_ao_scpsys_mem0_delsel**			
Type					RW				RW				RW			
Reset					1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
11:8		infra_ao_fhctl_mem_delsel	SRAM delsel of FHCTL
7:4		infra_ao_scpsys_mem1_delsel	SRAM delsel of scpsys
3:0		infra_ao_scpsys_mem0_delsel	SRAM delsel of scpsys

100001A4 **INFRA_AO_MBIST_BSEL** **infra_ao BSEL SRAM MBIST Control Register** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**infra_ao_mbist_bsel**							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
7:0		infra_ao_mbist_bsel	**Selects infra_ao MBIST byte** (obsolete)

100001A8 **INFRA_AO_MBIST_DEBUG** **infra_ao MBIST DEBUG Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													**ram_fuse_load**		**sramrom_ram_mbisr_rprst_b**	**infra_ao_mbist_rst_b**

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Type													RW		RW	RW
Reset													0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**infra_ao_mbist_background**		
Type														RW		
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
19		ram_fuse_load	**Enables RAM fuse load** 0: Disable 1: Enable load
17		sramrom_ram_mbisr_rprst_b	**Enables SRAMROM MBISR reset enable (low active)** 0: Reset 1: Does not reset
16		infra_ao_mbist_rst_b	**Enables infra_ao_mbist reset (low active)** 0: Reset 1: Does not reset
2:0		infra_ao_mbist_background	**Selects infra_ao_mbist data background**

100001AC **INFRA_AO_MBIST_FUSE_MON** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**afe_sysram_pre_fuse_o**				**sramrom_ram_mbisr_rp_ok_o**								**sramrom_ram_mbisr_rp_fail_o[7:4]**			
Type	RO				RO								RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**sramrom_ram_mbisr_rp_fail_o[3:0]**					**sramrom_ram_pre_fuse**							**sramrom_ram_mbisr_rp_ok_1**			
Type	RO					RO							RO			
Reset	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		afe_sysram_pre_fuse_o	**afe_sysram_pre_fuse_o**
27:20		sramrom_ram_mbisr_rp_ok_o	**sramrom_ram_mbisr_rp_ok[7:0]** 0: Repair not finished 1: Repair done
19:12		sramrom_ram_mbisr_rp_fail_o	**sramrom_ram_mbisr_rp_fail[7:0]** 0: Pass 1: Fail
10:4		sramrom_ram_pre_fuse	**sramrom_ram_pre_fuse**
3:0		sramrom_ram_mbisr_rp_ok_1	**sramrom_ram_mbisr_rp_ok[11:8]** 0: Repair not finished 1: Repair done

100001B0 **INFRA_AO_M** **infra_ao MBIST HOLDB Register** **00000003**

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BIST_HOLDB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															fhctl_mbist_holdb	scpsys_mbist_holdb
Type															RW	RW
Reset															1	1

Bit(s)	Mnemonic	Name	Description
1		fhctl_mbist_holdb	scpsys_mbist_holdb
0		scpsys_mbist_holdb	sramrom_sram_mbist_holdb

100001B4 **INFRA_AO_MBIST_MODE** **infra_ao MBIST Mode Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	scpsys_mbist_sleep_test	scpsys_mbist_sleep_w	scpsys_mbist_sleep_r	scpsys_mbist_sleep_inv												
Type	RW	RW	RW	RW												
Reset	0	0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															fhctl_mbist_mode	scpsys_mbist_mode
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
31		scpsys_mbist_sleep_test	**scpsys_mbist_sleep_test**
30		scpsys_mbist_sleep_w	**scpsys_mbist_sleep_w**
29		scpsys_mbist_sleep_r	**scpsys_mbist_sleep_r**
28		scpsys_mbist_sleep_inv	**scpsys_mbist_sleep_inv**
1		fhctl_mbist_mode	**fhctl_mbist_mode** 0: Disable 1: Enable
0		scpsys_mbist_mode	**scpsys_mbist_mode** 0: Disable 1: Enable

100001B8 **INFRA_AO_M** **infra_ao MBIST Monitor Sel Register** **00000000**

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BIST_MON_SEL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														infra_ao_mbist_fail_sel		
Type														RW		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
18:16		infra_ao_mbist_fail_sel	infra_ao_mbist_fail_sel

100001C0 INFRA_AO_MBIST_FUSE_GPU infra_ao MBIST GPU Fuse Register 00007F7F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		mbist_mfg_repaire_pre_fuse_0								mbist_mfg_repaire_pre_fuse_1						
Type		RO								RO						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		mbist_mfg_repair_fuse_0								mbist_mfg_repair_fuse_1						
Type		RO								RO						
Reset		1	1	1	1	1	1	1		1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
30:24		mbist_mfg_repaire_pre_fuse_0	mbist_mfg_repaire_pre_fuse_0
22:16		mbist_mfg_repaire_pre_fuse_1	mbist_mfg_repaire_pre_fuse_1
14:8		mbist_mfg_repair_fuse_0	mbist_mfg_repair_fuse_0
6:0		mbist_mfg_repair_fuse_1	mbist_mfg_repair_fuse_1

100001EC INFRA_AO_MBIST_FUSE_MM infra_ao MBIST MM Fuse Register 007F003F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		img_pre_fuse								img_fuse						
Type		RO								RO						
Reset		0	0	0	0	0	0	0		1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			mdp_wrot_pre_fuse								mdp_wrot_fuse					
Type			RO								RO					
Reset			0	0	0	0	0	0			1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
30:24		img_pre_fuse	img_pre_fuse
22:16		img_fuse	img_fuse
13:8		mdp_wrot_pre_fuse	mdp_wrot_pre_fuse
5:0		mdp_wrot_fuse	mdp_wrot_fuse

10000200 **TOPAXI_SI0_CTL** **Top AXI Fabric SI0 Control Register** **05000070**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	topaxi_cg_disable				topaxi_mst_sync_sel		topaxi_slv_sync_sel									
Type	RW				RW		RW									
Reset	0				0	1	0	1								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name										topaxi_sio_way_en					topaxi_sio_ctrl_bypass	topaxi_sio_outstanding_disable
Type										RW					RW	RW
Reset										1	1	1			0	0

Bit(s)	Mnemonic	Name	Description
31		topaxi_cg_disable	**Disables auto clock gating of all AXI components**
27:26		topaxi_mst_sync_sel	**Selects TOPAXI async slice master side sync**
25:24		topaxi_slv_sync_sel	**Selects TOPAXI async slice slave side sync**
6:4		topaxi_sio_way_en	**Controls output path of TOPAXI SI0** [6]: mmapb_s [5]: peri_s [4]: sram_s
1		topaxi_sio_ctrl_bypass	**Bypasses idle check when updating SI settings**
0		topaxi_sio_outstanding_disable	**Disables outstanding capability of SI0**

10000204 **TOPAXI_SI1_CTL** **Top AXI Fabric SI1 Control Register** **10000030**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				mmapb_wbuf_early_en												
Type				RW												
Reset				1												
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name											topaxi_si1_				topax	topax

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											way_en				i_si1_ctrl_bypass	i_si1_outstanding_disable
Type											RW				RW	RW
Reset											1	1			0	0

Bit(s)	Mnemonic	Name	Description
28		mmapb_wbuf_early_en	**Disables/Bypasses MMAPB write buffer** 0: Disable 1: Enable
5:4		topaxi_si1_way_en	**Controls output path of TOPAXI SI1** [5]: peri_m1 [4]: topaxi_m1
1		topaxi_si1_ctrl_bypass	**Bypasses idle check when updating SI settings**
0		topaxi_si1_outstanding_disable	**Disables outstanding capability of SI1**

10000208 **TOPAXI_MDBUS_CTRL** **MDSYS AXI Fabric Control Register** **00000019**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												conn_ahb2axi_merge_en	conn_ahb2axi_eight_byte_bus	conn_ahb2axi_ahb_buffer_en	conn_ahb2axi_hbstrb_en	conn_ahb2axi_hsecur_en
Type												RW	RW	RW	RW	RW
Reset												1	1	0	0	1

Bit(s)	Mnemonic	Name	Description
4		conn_ahb2axi_merge_en	**Enables CONNSYS AHB2AXI transaction merge** 0: Disable 1: Enable
3		conn_ahb2axi_eight_byte_bus	**CONNSYS AHB2AXI eight byte bus** 0: Disable 1: Enable
2		conn_ahb2axi_ahb_buffer_en	**Enables CONNSYS AHB2AXI transaction bufferable** 0: Disable 1: Enable
1		conn_ahb2axi_hbstrb_en	**Enables CONNSYS AHB2AXI transaction byte strboe** 0: Disable 1: Enable
0		conn_ahb2axi_hsecur_en	**Enables CONNSYS AHB2AXI secure transaction** 0: Disable 1: Enable

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10000220 **TOPAXI_PROT_EN** **Top AXI Protect Module Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ap2md_md3_prot_en	md3_m1_prot_en	md3_m0_prot_en	ap2md_md1_prot_en	md1_m3_prot_en	md1_m2_prot_en	md1_m1_prot_en	md1_m0_prot_en		cldma_m0_prot_en	peri_m1_port_en	infra_adb_prot_en	emi_adb_prot_en			gce_prot_en
Type	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW	RW	RW			RW
Reset	0	0	0	0	0	0	0	0		0	0	0	0			0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	gcpu_prot_en	mfg_m_prot_en	dbg_m_prot_en	l2ss_aff_prot_en	l2ss_smi_prot_en	peri_m0_prot_en	l2c_m2_prot_en	conn_slv_prot_en		mmapb_s_prot_en	sramrom_l2c_slp_protect_en	mdhw_protect_en	mdmcu_protect_en	conn_mst_prot_en	mm_m0_prot_en	mci_m2_prot_en
Type	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		ap2md_md3_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
30		md3_m1_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
29		md3_m0_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
28		ap2md_md1_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
27		md1_m3_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
26		md1_m2_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
25		md1_m1_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
24		md1_m0_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
22		cldma_m0_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
21		peri_m1_port_en	**Enables AXI protection unit** 0: Disable 1: Enable
20		infra_adb_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
19		emi_adb_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable

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Bit(s)	Mnemonic	Name	Description
16		gce_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
15		gcpu_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
14		mfg_m_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
13		dbg_m_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
12		l2ss_aff_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
11		l2ss_smi_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
10		peri_m0_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
9		l2c_m2_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
8		conn_slv_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
6		mmapb_s_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
5		sramrom_l2c_slp_protect_en	**Enables AXI protection unit** 0: Disable 1: Enable
4		mdhw_protect_en	**Enables AXI protection unit** 0: Disable 1: Enable
3		mdmcu_protect_en	**Enables AXI protection unit** 0: Disable 1: Enable
2		conn_mst_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
1		mm_m0_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
0		mci_m2_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable

10000224 **TOPAXI_PRO** **Top AXI Protect Module Status Register 0** **00001F67**

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T_STA0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ap2md_md3_prot_idle	md3_m1_prot_idle	md3_m0_prot_idle	ap2md_md1_prot_idle	md1_m3_prot_idle	md1_m2_prot_idle	md1_m1_prot_idle	md1_m0_prot_idle		cldma_m0_prot_idle	peri_m1_port_idle	infra_adb_prot_idle	emi_adb_prot_idle			gce_prot_idle
Type	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW	RW	RW			RW
Reset	0	0	0	0	0	0	0	0		0	0	0	0			0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	gcpu_prot_idle	mfg_prot_idle	dbg_m_prot_idle	l2ss_aff_prot_idle	l2ss_smi_prot_idle	peri_m0_prot_idle	l2c_m2_prot_idle	conn_slv_prot_idle		mmapb_s_prot_idle	l2c_sram_idle	mdhw_protect_idle	mdmcu_protect_idle	conn_mst_prot_idle	mm_m0_prot_idle	mci_m2_prot_idle
Type	RW	RW	RW	RU	RU	RU	RU	RU		RU	RU	RW	RW	RU	RU	RU
Reset	0	0	0	1	1	1	1	1		1	1	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
31		ap2md_md3_prot_idle	**Indicates protect is in idle state** 0: Busy 1: Idle
30		md3_m1_prot_idle	**Indicates protect is in idle state** 0: Busy 1: Idle
29		md3_m0_prot_idle	**Indicates protect is in idle state** 0: Busy 1: Idle
28		ap2md_md1_prot_idle	**Indicates protect is in idle state** 0: Busy 1: Idle
27		md1_m3_prot_idle	**Indicates protect is in idle state** 0: Busy 1: Idle
26		md1_m2_prot_idle	**Indicates protect is in idle state** 0: Busy 1: Idle
25		md1_m1_prot_idle	**Indicates protect is in idle state** 0: Busy 1: Idle
24		md1_m0_prot_idle	**Indicates protect is in idle state** 0: Busy 1: Idle
22		cldma_m0_prot_idle	**Indicates protect is in idle state** 0: Busy 1: Idle
21		peri_m1_port_idle	**Indicates protect is in idle state** 0: Busy 1: Idle
20		infra_adb_prot_idle	**Indicates protect is in idle state** 0: Busy 1: Idle
19		emi_adb_prot_idle	**Indicates protect is in idle state** 0: Busy 1: Idle
16		gce_prot_idle	**Indicates protect is in idle state** 0: Busy

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Bit(s)	Mnemonic	Name	Description
			1: Idle
15		gcpu_prot_idle	**Indicates protect is in idle state** 0: Busy 1: Idle
14		mfg_prot_idle	**Indicates protect is in idle state** 0: Busy 1: Idle
13		dbg_m_prot_idle	**Indicates protect is in idle state** 0: Busy 1: Idle
12		l2ss_aff_prot_idle	**Indicates protect is in idle state** 0: Busy 1: Idle
11		l2ss_smi_prot_idle	**Indicates protect is in idle state** 0: Busy 1: Idle
10		peri_m0_prot_idle	**Indicates protect is in idle state** 0: Busy 1: Idle
9		l2c_m2_prot_idle	**Indicates protect is in idle state** 0: Busy 1: Idle
8		conn_slv_prot_idle	**Indicates protect is in idle state** 0: Busy 1: Idle
6		mmapb_s_prot_idl e	**Indicates protect is in idle state** 0: Busy 1: Idle
5		l2c_sram_idle	**Indicates protect is in idle state** 0: Busy 1: Idle
4		mdhw_protect_idle	**Indicates protect is in idle state** 0: Busy 1: Idle
3		mdmcu_protect_idl e	**Indicates protect is in idle state** 0: Busy 1: Idle
2		conn_mst_prot_idl e	**Indicates protect is in idle state** 0: Busy 1: Idle
1		mm_m0_prot_idle	**Indicates protect is in idle state** 0: Busy 1: Idle
0		mci_m2_prot_idle	**Indicates protect is in idle state** 0: Busy 1: Idle

10000228 **TOPAXI_PROT_STA1** **Top AXI Protect Module Status Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	**ap2md_md3_prot_rdy**	**md3_m1_prot_rdy**	**md3_m0_prot_rdy**	**ap2md_md1_prot_rdy**	**md1_m3_prot_rdy**	**md1_m2_prot_rdy**	**md1_m1_prot_rdy**	**md1_m0_prot_rdy**		**cldma_m0_prot_rdy**	**peri_m1_port_rdy**	**infra_adb_prot_rdy**	**emi_adb_prot_rdy**			**gce_prot_rdy**
Type	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW	RW	RW			RW
Reset	0	0	0	0	0	0	0	0		0	0	0	0			0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**gcpu_prot_rdy**	**mfg_prot_rdy**	**dbg_m_prot_rdy**	**l2ss_aff_prot_rdy**	**l2ss_smi_prot_rdy**	**peri_m0_prot_rdy**	**l2c_m2_prot_rdy**	**conn_slv_prot_rdy**		**mmapb_s_prot_rdy**	**sramrom_l2c_slp_protect_rdy**	**mdhw_protect_rdy**	**mdmcu_protect_rdy**	**conn_mst_prot_rdy**	**mm_m0_prot_rdy**	**mci_m2_prot_rdy**
Type	RW	RW	RW	RU	RU	RU	RU	RU		RU	RU	RW	RW	RU	RU	RU
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		ap2md_md3_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
30		md3_m1_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
29		md3_m0_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
28		ap2md_md1_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
27		md1_m3_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
26		md1_m2_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
25		md1_m1_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
24		md1_m0_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
22		cldma_m0_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
21		peri_m1_port_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
20		infra_adb_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
19		emi_adb_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
16		gce_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready

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Bit(s)	Mnemonic	Name	Description
15		gcpu_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
14		mfg_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
13		dbg_m_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
12		l2ss_aff_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
11		l2ss_smi_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
10		peri_m0_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
9		l2c_m2_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
8		conn_slv_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
6		mmapb_s_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
5		sramrom_l2c_slp_protect_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
4		mdhw_protect_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
3		mdmcu_protect_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
2		conn_mst_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
1		mm_m0_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
0		mci_m2_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready

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1000022C **TOPAXI_AXI_ASLICE_CTRL** **Top AXI Aslice Control Register** **41454145**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reserved_aslice_slv_sy						md1hwmix_m2_aslice_		md1cr4_m1_aslice_slv				infra_peri_aslice_slv_s		topaxi_aslice_slv_sync	

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	nc_sel						slv_sync_se l		_sync_sel				ync_sel		_sel	
Type	RW						RW		RW				RW		RW	
Reset	0	1					0	1	0	1			0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**reserved_aslice_mst_sync_sel**						**md1hwmix_m2_aslice_mst_sync_sel**		**md1cr4_m1_aslice_mst_sync_sel**				**infra_peri_mst_sync_sel**		**topaxi_aslice_mst_sync_sel**	
Type	RW						RW		RW				RW		RW	
Reset	0	1					0	1	0	1			0	1	0	1

Bit(s)	Mnemonic	Name	Description
25:24		md1hwmix_m2_aslice_slv_sync_sel	**Selects AXI aslice slave sync** 00: Sync 1T 01: Sync 2T 10: Sync 3T 11: Sync 3T
23:22		md1cr4_m1_aslice_slv_sync_sel	**Selects AXI aslice slave sync** 00: Sync 1T 01: Sync 2T 10: Sync 3T 11: Sync 3T
19:18		infra_peri_aslice_slv_sync_sel	**Selects AXI aslice slave sync** 00: Sync 1T 01: Sync 2T 10: Sync 3T 11: Sync 3T
17:16		topaxi_aslice_slv_sync_sel	**Selects AXI aslice slave sync** 00: Sync 1T 01: Sync 2T 10: Sync 3T 11: Sync 3T
9:8		md1hwmix_m2_aslice_mst_sync_sel	**Selects AXI aslice master sync** 00: Sync 1T 01: Sync 2T 10: Sync 3T 11: Sync 3T
7:6		md1cr4_m1_aslice_mst_sync_sel	**Selects AXI aslice master sync** 00: Sync 1T 01: Sync 2T 10: Sync 3T 11: Sync 3T
3:2		infra_peri_mst_sync_sel	**Selects AXI aslice master sync** 00: Sync 1T 01: Sync 2T 10: Sync 3T 11: Sync 3T
1:0		topaxi_aslice_mst_sync_sel	**Selects AXI aslice master sync** 00: Sync 1T 01: Sync 2T 10: Sync 3T 11: Sync 3T

10000300	**MD1_BANK0_MAP0**	**MDSYS1 Bank0 Remap Register 0**	**00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**md1_bo_map3_addr**							**md1_bo_map3_en**	**md1_bo_map2_addr**							**md1_bo_map2_en**
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**md1_bo_map1_addr**							**md1_bo_map1_en**	**md1_bo_map0_addr**							**md1_bo_map0_en**
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25		md1_bo_map3_addr	**Sub-bank3 remap address register**
24		md1_bo_map3_en	**Sub-bank3 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_011 will be remapped to bo_map3_addr. 0: Disable 1: Enable
23:17		md1_bo_map2_addr	**Sub-bank2 remap address register**
16		md1_bo_map2_en	**Sub-bank2 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_010 will be remapped to bo_map2_addr. 0: Disable 1: Enable
15:9		md1_bo_map1_addr	**Sub-bank1 remap address register**
8		md1_bo_map1_en	**Sub-bank1 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_001 will be remapped to bo_map1_addr. 0: Disable 1: Enable
7:1		md1_bo_map0_addr	**Sub-bank0 remap address register**
0		md1_bo_map0_en	**Sub-bank0 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_000 will be remapped to bo_map0_addr. 0: Disable 1: Enable

10000304 **MD1_BANK0_MAP1** **MDSYS1 Bank0 Remap Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**md1_bo_map7_addr**							**md1_bo_map7_en**	**md1_bo_map6_addr**							**md1_bo_map6_en**
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**md1_bo_map5_addr**							**md1_bo_m**	**md1_bo_map4_addr**							**md1_bo_m**

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								ap5_en								ap4_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25		md1_b0_map7_addr	**Sub-bank7 remap address register**
24		md1_b0_map7_en	**Sub-bank7 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_111 will be remapped to b0_map7_addr. 0: Disable 1: Enable
23:17		md1_b0_map6_addr	**Sub-bank6 remap address register**
16		md1_b0_map6_en	**Sub-bank6 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_110 will be remapped to b0_map6_addr. 0: Disable 1: Enable
15:9		md1_b0_map5_addr	**Sub-bank5 remap address register**
8		md1_b0_map5_en	**Sub-bank5 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_101 will be remapped to b0_map5_addr. 0: Disable 1: Enable
7:1		md1_b0_map4_addr	**Sub-bank4 remap address register**
0		md1_b0_map4_en	**Sub-bank4 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_100 will be remapped to b0_map4_addr. 0: Disable 1: Enable

10000308 **MD1_BANK4_MAP0** **MDSYS1 Bank4 Remap Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	md1_b4_map3_addr							md1_b4_map3_en	md1_b4_map2_addr							md1_b4_map2_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md1_b4_map1_addr							md1_b4_map1_en	md1_b4_map0_addr							md1_b4_map0_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25		md1_b4_map3_addr	**Sub-bank3 remap address register**

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Bit(s)	Mnemonic	Name	Description
24		md1_b4_map3_en	**Sub-bank3 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_011 will be remapped to b4_map3_addr. 0: Disable 1: Enable
23:17		md1_b4_map2_addr	**Sub-bank2 remap address register**
16		md1_b4_map2_en	**Sub-bank2 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_010 will be remapped to b4_map2_addr. 0: Disable 1: Enable
15:9		md1_b4_map1_addr	**Sub-bank1 remap address register**
8		md1_b4_map1_en	**Sub-bank1 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_001 will be remapped to b0_map1_addr. 0: Disable 1: Enable
7:1		md1_b4_map0_addr	**Sub-bank0 remap address register**
0		md1_b4_map0_en	**Sub-bank0 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_000 will be remapped to b4_map0_addr. 0: Disable 1: Enable

1000030C **MD1_BANK4_MAP1** **MDSYS1 Bank4 Remap Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**md1_b4_map7_addr**							**md1_b4_map7_en**	**md1_b4_map6_addr**							**md1_b4_map6_en**
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**md1_b4_map5_addr**							**md1_b4_map5_en**	**md1_b4_map4_addr**							**md1_b4_map4_en**
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25		md1_b4_map7_addr	**Sub-bank7 remap address register**
24		md1_b4_map7_en	**Sub-bank7 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_111 will be remapped to b4_map7_addr. 0: Disable 1: Enable
23:17		md1_b4_map6_addr	**Sub-bank6 remap address register**

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Bit(s)	Mnemonic	Name	Description
16		md1_b4_map6_en	**Sub-bank6 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_110 will be remapped to b4_map6_addr. 0: Disable 1: Enable
15:9		md1_b4_map5_addr	**Sub-bank5 remap address register**
8		md1_b4_map5_en	**Sub-bank5 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_101 will be remapped to b4_map5_addr. 0: Disable 1: Enable
7:1		md1_b4_map4_addr	**Sub-bank4 remap address register**
0		md1_b4_map4_en	**Sub-bank4 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_100 will be remapped to b4_map4_addr. 0: Disable 1: Enable

10000310 **MD2_BANK0_MAP0** **MDSYS2 Bank0 Remap Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**md2_b0_map3_addr**							**md2_b0_map3_en**	**md2_b0_map2_addr**							**md2_b0_map2_en**
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**md2_b0_map1_addr**							**md2_b0_map1_en**	**md2_b0_map0_addr**							**md2_b0_map0_en**
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25		md2_b0_map3_addr	**Sub-bank3 remap address register**
24		md2_b0_map3_en	**Sub-bank3 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_011 will be remapped to b0_map3_addr. 0: Disable 1: Enable
23:17		md2_b0_map2_addr	**Sub-bank2 Remap address register**
16		md2_b0_map2_en	**Sub-bank2 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_010 will be remapped to b0_map2_addr. 0: Disable 1: Enable
15:9		md2_b0_map1_addr	**Sub-bank1 remap address register**

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Bit(s)	Mnemonic	Name	Description
8		md2_b0_map1_en	**Sub-bank1 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_001 will be remapped to b0_map1_addr. 0: Disable 1: Enable
7:1		md2_b0_map0_addr	**Sub-bank0 remap address register**
0		md2_b0_map0_en	**Sub-bank0 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_000 will be remapped to b0_map0_addr. 0: Disable 1: Enable

10000314 **MD2_BANK0_MAP1** **MDSYS2 Bank0 Remap Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	md2_b0_map7_addr							md2_b0_map7_en	md2_b0_map6_addr							md2_b0_map6_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md2_b0_map5_addr							md2_b0_map5_en	md2_b0_map4_addr							md2_b0_map4_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25		md2_b0_map7_addr	**Sub-bank7 Remap address register**
24		md2_b0_map7_en	**Sub-bank7 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_111 will be remapped to b0_map7_addr. 0: Disable 1: Enable
23:17		md2_b0_map6_addr	**Sub-bank6 remap address register**
16		md2_b0_map6_en	**Sub-bank6 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_110 will be remapped to b0_map6_addr. 0: Disable 1: Enable
15:9		md2_b0_map5_addr	**Sub-bank5 remap address register**
8		md2_b0_map5_en	**Sub-bank5 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_101 will be remapped to b0_map5_addr. 0: Disable 1: Enable
7:1		md2_b0_map4_addr	**Sub-bank4 remap address register**

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Bit(s)	Mnemonic	Name	Description
0		md2_b0_map4_en	**Sub-bank4 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_100 will be remapped to b0_map4_addr. 0: Disable 1: Enable

10000318 MD2_BANK4_MAP0 MDSYS2 Bank4 Remap Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	md2_b4_map3_addr							md2_b4_map3_en	md2_b4_map2_addr							md2_b4_map2_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md2_b4_map1_addr							md2_b4_map1_en	md2_b4_map0_addr							md2_b4_map0_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25		md2_b4_map3_addr	**Sub-bank3 remap address register**
24		md2_b4_map3_en	**Sub-bank3 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_011 will be remapped to b4_map3_addr. 0: Disable 1: Enable
23:17		md2_b4_map2_addr	**Sub-bank2 remap address register**
16		md2_b4_map2_en	**Sub-bank2 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_010 will be remapped to b4_map2_addr. 0: Disable 1: Enable
15:9		md2_b4_map1_addr	**Sub-bank1 remap address register**
8		md2_b4_map1_en	**Sub-bank1 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_000 will be remapped to b4_map0_addr. 0: Disable 1: Enable
7:1		md2_b4_map0_addr	**Sub-bank0 remap address register**
0		md2_b4_map0_en	**Sub-bank0 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_000 will be remapped to b4_map0_addr. 0: Disable 1: Enable

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1000031C **MD2_BANK4_MAP1** **MDSYS2 Bank4 Remap Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**md2_b4_map7_addr**							**md2_b4_map7_en**	**md2_b4_map6_addr**							**md2_b4_map6_en**
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**md2_b4_map5_addr**							**md2_b4_map5_en**	**md2_b4_map4_addr**							**md2_b4_map4_en**
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25		md2_b4_map7_addr	**Sub-bank7 remap address register**
24		md2_b4_map7_en	**Sub-bank7 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_111 will be remapped to b4_map7_addr. 0: Disable 1: Enable
23:17		md2_b4_map6_addr	**Sub-bank6 remap address register**
16		md2_b4_map6_en	**Sub-bank6 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_110 will be remapped to b4_map6_addr. 0: Disable 1: Enable
15:9		md2_b4_map5_addr	**Sub-bank5 remap address register**
8		md2_b4_map5_en	**Sub-bank5 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_101 will be remapped to b4_map5_addr. 0: Disable 1: Enable
7:1		md2_b4_map4_addr	**Sub-bank4 remap address register**
0		md2_b4_map4_en	**Sub-bank4 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_100 will be remapped to b4_map4_addr. 0: Disable 1: Enable

10000320 **CONN_MAP0** **CONNSYS EMI Address Remap Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															**conn2ap_busreq_ultra**	**conn2ap_busreq_hp**
Type															RW	RW
Reset															0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				conn2ap_addr_remap_en	conn2ap_addr_remap											
Type				RW	RW											
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
17		conn2ap_busreq_ultra	**CONNSYS-to-AP EMI ultra request control register** 0: Disable EMI ultra request 1: Enable EMI ultra request
16		conn2ap_busreq_hp	**CONNSYS-to-AP high priority control register** 0: Normal bus arbitration priority. Connsys and perisys bus requests are round-robin. 1: High bus arbitration priority. Connsys bus request has high priority than perisys bus request.
12		conn2ap_addr_remap_en	**CONNSYS-to-AP EMI address remapping enable register** 0: Bypass. Only address[31:28] is remapped to 4'h8. address[27:20] is unchanged. 1: Enable remap. Address[31:20] will be equal to conn2ap_addr_remap.
11:0		conn2ap_addr_remap	**CONNSYS-to-AP EMI address remapping register** Replaces address[31:20] from connsys.

10000324 **CONN_SIDEBAND** **CONSYS to Bus Sideband Signals** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													conn_to_bus_ar_sideband			
Type													RW			
Reset													0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name													conn_to_bus_aw_sideband			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:16		conn_to_bus_ar_sideband	**CONNSYS-to-AP sideband** bit 0: share _en bit 1: mmu bit 2: ultra bit 3: preultra
3:0		conn_to_bus_aw_sideband	**CONNSYS-to-AP sideband** bit 0: share _en bit 1: mmu bit 2: ultra bit 3: preultra

10000330 **C2K_CONFIG** **C2K AP Config** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	c2k_ap_config[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c2k_ap_config[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		c2k_ap_config	

10000334 C2K_STATUS C2K Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	c2k_status[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c2k_status[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		c2k_status	

10000338 C2K_SPM_CTRL C2k SPM Control 00000014

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						ltel1_mtcmos_pd_req	ltel1_mem_pd_req	ltel1_clk_off_req	ltel1_pd_reserve_req	lte1_extpwr_off	md2_srcclkena		md1_srcclkena		ap_to_c2k_ready	ap_wakeup_c2k
Type						RW	RW	RW	RW	RW	RW		RW		RW	RW
Reset						0	0	0	0	0	0	1	0	1	0	0

Bit(s)	Mnemonic	Name	Description
10		ltel1_mtcmos_pd_req	
9		ltel1_mem_pd_req	
8		ltel1_clk_off_req	
7		ltel1_pd_reserve_req	
6		lte1_extpwr_off	
5:4		md2_srcclkena	
3:2		md1_srcclkena	
1		ap_to_c2k_ready	
0		ap_wakeup_c2k	

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10000340 LTE_OCCUPY_ANT LTE Occupy ant 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lte_occupy_ant															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		lte_occupy_ant	

10000344 C2K_OCCUPY_ANT C2K Occupy ant 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c2k_occupy_ant															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		c2k_occupy_ant	

1000034C CLDMA_CTRL CLDMA Control Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				cldma_mo_aruser								cldma_mo_awuser				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															reg_cldma_ap2ap_wakeup_event	cldma_ap_ip_busy_mask
Type															RW	RW
Reset															0	1

Bit(s)	Mnemonic	Name	Description
28:24		cldma_mo_aruser	
20:16		cldma_mo_awuser	
1		reg_cldma_ap2ap_wakeup_event	
0		cldma_ap_ip_busy	

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Bit(s)	Mnemonic	Name	Description
		_mask	

10000500 **INFRA_AO_DBG_CON0** **INFRA_AO Debug Control 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					infra_ao_debug_mon0											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0		infra_ao_debug_mon0	Debug monitor control register 0

10000504 **INFRA_AO_DBG_CON1** **INFRA_AO Debug Control 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					infra_ao_debug_mon1											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0		infra_ao_debug_mon1	Debug monitor control register 1

10000508 **INFRA_AO_DBG_CON2** **INFRA_AO Debug Control 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					infra_ao_debug_mon2											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0		infra_ao_debug_mon2	Debug monitor control register 2

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1000050C INFRA_AO_DBG_CON3 INFRA_AO Debug Control 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					infra_ao_debug_mon3											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0		infra_ao_debug_mon3	Debug monitor control register 3

10000700 INFRA_MISC Infrasys Miscellaneous Control Register 000032C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																lte_busy_sel[1:1]
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lte_busy_sel[0:0]	emitype_change_en	ap_usb2jtag_en	fhctl_f26m_en	conn_bt_cvsd_mask	ap2conn_osc_en	ap2conn_mcusys_wakeup_b	ap2conn_jtag_2wire	infra_md2_pdn_mask_en	infra_md1_pdn_mask_en	md2_dbgack_mask	md1_dbgack_mask	md_legacy_jtag_sel			emi_gated_with_dramc
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW			RW
Reset	0	0	1	1	0	0	1	0	1	1	0	0	0	0		0

Bit(s)	Mnemonic	Name	Description
16:15		lte_busy_sel	
14		emitype_change_en	**EMI type change enable register** 0: Disable EMI type change when address violation 1: Enable EMI type change when address violation
13		ap_usb2jtag_en	**USB2JTAG control register** 0: No change 1: Switch USB port as JTAG
12		fhctl_f26m_en	**FHCTL 26MHz clock gating register** 0: Disable 26M clock to FHCTL 1: Enable 26M clock to FHCTL
11		conn_bt_cvsd_mask	**BT CVDS interrupt masking register** 0: Unmask BT CVDS IRQ 1: mask BT CVDS IRQ
10		ap2conn_osc_en	**AP SW controlled connsys clock source enable register** 0: Disable connsys clock source 1: Enable connsys clock source
9		ap2conn_mcusys_wakeup_b	**AP SW triggered interrupt to CONSYS register** 0: AP enable interrupt request to CONNSYS 1: AP disable interrupt request to CONNSYS
8		ap2conn_jtag_2wir	**CONNSYS JTAG 2-wire switching register**

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Bit(s)	Mnemonic	Name	Description
		e	0: Disable 2-wire switching 1: Enable 2-wire switching
7		infra_md2_pdn_mask_en	**Power-down control options of AP/md1/md2 shared IP** (obsolete) 0: MD2 can control 1: MD2 cannot control
6		infra_md1_pdn_mask_en	**Power-down control options of AP/md1/md2 shared IP** 0: MD1 can control 1: MD1 cannot control
5		md2_dbgack_mask	**MD2 DBGACK option** (obsolete) 0: Enable MD2's ack 1: bypass MD2's ack
4		md1_dbgack_mask	**MD1 DBGACK option** 0: Enable MD1's ack 1: bypass MD1's ack
3:2		md_legacy_jtag_sel	**Selects MDSYS legacy JTAG** 0: cs_jtag_ap 1: LEGACY_JTAG 2: Reserved 3: Reserved
0		emi_gated_with_dramc	**EMI clock is gated when DRAMC is ilde.**

10000704 INFRA_ACP Infrasys CPU Coherence Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	sw_peri_mo_awcache				sw_peri_mo_arcache						mci_ar_snoop_en_ack	mci_aw_snoop_en_ack		mci_reorder_en	mci_ar_snoop_en	mci_aw_snoop_en
Type	RW				RW						RO	RO		RW	RW	RW
Reset	0	0	0	0	0	0	0	0			0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
15:12		sw_peri_mo_awcache	**Overrides perisys AXI AWCACHE**
11:8		sw_peri_mo_arcache	**Overrides perisys AXI ARCACHE**
5		mci_ar_snoop_en_ack	**MCI read snoop control status** 0: MCI read snoop is disabled. 1: MCI read snoop is enabled.
4		mci_aw_snoop_en_ack	**MCI write snoop control status** 0: MCI write snoop is disabled. 1: MCI write snoop is enabled.
2		mci_reorder_en	**MCI read command reorder queue** 0: Disable MCI reorder queue 1: Enable MCI reorder queue
1		mci_ar_snoop_en	**Controls MCI read snoop**

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Bit(s)	Mnemonic	Name	Description
			0: Disable MCI read snoop 1: Enable MCI read snoop
0		mci_aw_snoop_en	**Controls MCI write snoop** 0: Disable MCI write snoop 1: Enable MCI write snoop

10000708 INFRA_BONDING INFRA_BONDING 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															**usbdl**	
Type															RU	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**bonding_option**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
17:16		usbdl	usbdl
15:0		bonding_option	Bonding option

10000800 SRAMROM_BOOT_ADDR SRAMROM Boot Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**sramrom_b_addr[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**sramrom_b_addr[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		sramrom_b_addr	SRAMROM power-down jump address register

10000804 SRAMROM_SEC_CTRL SRAMROM Secure Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**sramrom_sw_rom_pd**			**sramrom_sec_addr_en**	**sramrom_sec1_set3**			**sramrom_sec1_set2**			**sramrom_sec1_set1**			**sramrom_sec1_set0**		
Type	RW			RW	RW			RW			RW			RW		
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**sramrom_seco_set3**			**sramrom_seco_set2**			**sramrom_seco_set1**			**sramrom_seco_seto**		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31		sramrom_sw_rom_pd	**SRAMROM software power-down control register** 0: Does not power down 1: Power down
28		sramrom_sec_addr_en	**SRAMROM region 0/1 enable register** 0: Disable region 0/1 protection 1: Enable region 0/1 protection and based on region 0/1's security setting
27:25		sramrom_sec1_set3	**Security setting for transactions from region 1, domain 3** 000: S R/W, NS R/W 001: S R/W, NS block 010: S R/W, NS RO 011: S R/W, NS WO 100: S RO, NS RO 101: S block, NS block 110: S block, NS block 111: S block, NS block
24:22		sramrom_sec1_set2	**Security setting for transactions from region1, domain 2** 000: S R/W, NS R/W 001: S R/W, NS block 010: S R/W, NS RO 011: S R/W, NS WO 100: S RO, NS RO 101: S block, NS block 110: S block, NS block 111: S block, NS block
21:19		sramrom_sec1_set1	**Security setting for transactions from region1, domain 1** 000: S R/W, NS R/W 001: S R/W, NS block 010: S R/W, NS RO 011: S R/W, NS WO 100: S RO, NS RO 101: S block, NS block 110: S block, NS block 111: S block, NS block
18:16		sramrom_sec1_set0	**Security setting for transactions from region1, domain 0** 000: S R/W, NS R/W 001: S R/W, NS block 010: S R/W, NS RO 011: S R/W, NS WO 100: S RO, NS RO 101: S block, NS block 110: S block, NS block 111: S block, NS block
11:9		sramrom_sec0_set3	**Security setting for transactions from region 0,domain 3** 000: S R/W, NS R/W 001: S R/W, NS block 010: S R/W, NS RO 011: S R/W, NS WO 100: S RO, NS RO 101: S block, NS block 110: S block, NS block 111: S block, NS block
8:6		sramrom_sec0_set2	**Security setting for transactions from region 0, domain 2** 000: S R/W, NS R/W 001: S R/W, NS block 010: S R/W, NS RO 011: S R/W, NS WO

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Bit(s)	Mnemonic	Name	Description
			100: S RO, NS RO 101: S block, NS block 110: S block, NS block 111: S block, NS block
5:3		sramrom_sec0_set1	**Security setting for transactions from region 0, domain 1** 000: S R/W, NS R/W 001: S R/W, NS block 010: S R/W, NS RO 011: S R/W, NS WO 100: S RO, NS RO 101: S block, NS block 110: S block, NS block 111: S block, NS block
2:0		sramrom_sec0_set0	**Security setting for transactions from region0, domain 0** 000: S R/W, NS R/W 001: S R/W, NS block 010: S R/W, NS RO 011: S R/W, NS WO 100: S RO, NS RO 101: S block, NS block 110: S block, NS block 111: S block, NS block

10000808 **SRAMROM_SEC_ADDR** **SRAMROM Region Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															sramrom_sec_addr[7:6]	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_sec_addr[5:0]															
Type	RW															
Reset	0	0	0	0	0	0										

Bit(s)	Mnemonic	Name	Description
17:10		sramrom_sec_addr	**Partitions internal SRAM into 2 regions** Region 0 is from 0x0010_0000 to 0x001X_XX00; Region 1 is from 0x001X_XX00 to 0x0013_FFFF. SRAMROM_SEC_ADDR specifies address[17:10].

1000080C **SRAMROM_FPC_BOOT_ADDR** **SRAMROM Region Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sramrom_fpc_boot_addr[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_fpc_boot_addr[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31:0		sramrom_fpc_boot_addr	**Specifies jump address of CPU when in FPC mode** Can only be written when unlocked.

10000810 SRAMROM_FPC_BOOT_CON SRAMROM FPC Boot Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sramrom_fpc_key[23:8]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_fpc_key[7:0]															sramrom_fpc_baddr_en
Type	WO															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Mnemonic	Name	Description
31:8		sramrom_fpc_key	**Stores magic key for enabling FPC bootstrap function** Enter 24'h34AE8C to unlock the function.
0		sramrom_fpc_b_addr_en	**When set to 1, the jump address specified in sramrom_fpc_boot_addr will take effect.** Can only be written when unlocked.

10000814 SRAMROM_SEC_CTRL2 SRAMROM Secure Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					sramrom_sec1_set7			sramrom_sec1_set6			sramrom_sec1_set5			sramrom_sec1_set4		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					sramrom_sec0_set7			sramrom_sec0_set6			sramrom_sec0_set5			sramrom_sec0_set4		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:25		sramrom_sec1_set7	**Security setting for transactions from region 1, domain 7** 000: S R/W, NS R/W 001: S R/W, NS block 010: S R/W, NS RO 011: S R/W, NS WO 100: S RO, NS RO 101: S block, NS block 110: S block, NS block 111: S block, NS block
24:22		sramrom_sec1_set6	**Security setting for transactions from region1, domain 6** 000: S R/W, NS R/W

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Bit(s)	Mnemonic	Name	Description
			001: S R/W, NS block 010: S R/W, NS RO 011: S R/W, NS WO 100: S RO, NS RO 101: S block, NS block 110: S block, NS block 111: S block, NS block
21:19		sramrom_sec1_set5	**Security setting for transactions from region1, domain 5** 000: S R/W, NS R/W 001: S R/W, NS block 010: S R/W, NS RO 011: S R/W, NS WO 100: S RO, NS RO 101: S block, NS block 110: S block, NS block 111: S block, NS block
18:16		sramrom_sec1_set4	**Security setting for transactions from region1, domain 4** 000: S R/W, NS R/W 001: S R/W, NS block 010: S R/W, NS RO 011: S R/W, NS WO 100: S RO, NS RO 101: S block, NS block 110: S block, NS block 111: S block, NS block
11:9		sramrom_sec0_set 7	**Security setting for transactions from region 0,domain 7** 000: S R/W, NS R/W 001: S R/W, NS block 010: S R/W, NS RO 011: S R/W, NS WO 100: S RO, NS RO 101: S block, NS block 110: S block, NS block 111: S block, NS block
8:6		sramrom_sec0_set 6	**Security setting for transactions from region 0, domain 6** 000: S R/W, NS R/W 001: S R/W, NS block 010: S R/W, NS RO 011: S R/W, NS WO 100: S RO, NS RO 101: S block, NS block 110: S block, NS block 111: S block, NS block
5:3		sramrom_sec0_set 5	**Security setting for transactions from region 0, domain 5** 000: S R/W, NS R/W 001: S R/W, NS block 010: S R/W, NS RO 011: S R/W, NS WO 100: S RO, NS RO 101: S block, NS block 110: S block, NS block 111: S block, NS block
2:0		sramrom_sec0_set 4	**Security setting for transactions from region0, domain 4** 000: S R/W, NS R/W 001: S R/W, NS block 010: S R/W, NS RO 011: S R/W, NS WO 100: S RO, NS RO 101: S block, NS block

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Bit(s)	Mnemonic	Name	Description
			110: S block, NS block 111: S block, NS block

10000818 SRAMROM_BOOT_MISC0 SRAMROM Spare Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sramrom_boot_misc0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_boot_misc0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		sramrom_boot_misc0	SARMROM spare register 0

1000081C SRAMROM_BOOT_MISC1 SRAMROM Spare Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sramrom_boot_misc1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_boot_misc1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		sramrom_boot_misc1	SARMROM spare register 1

10000820 SRAMROM_BOOT_MISC2 SRAMROM Spare Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sramrom_boot_misc2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_boot_misc2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		sramrom_boot_misc2	SARMROM spare register 2

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10000824 **SRAMROM_BOOT_MISC3** **SRAMROM Spare Register 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sramrom_boot_misc3[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_boot_misc3[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		sramrom_boot_misc3	SARMROM spare register 3

10000828 **SRAMROM_BOOT_MISC4** **SRAMROM Spare Register 4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sramrom_boot_misc4[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_boot_misc4[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		sramrom_boot_misc4	SARMROM spare register 4

1000082C **SRAMROM_BOOT_MISC5** **SRAMROM Spare Register 5** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sramrom_boot_misc5[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_boot_misc5[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		sramrom_boot_misc5	SARMROM spare register 5

10000830 **SRAMROM_BOOT_MISC6** **SRAMROM Spare Register 6** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	sramrom_boot_misc6[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_boot_misc6[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		sramrom_boot_misc6	SARMROM spare register 6

10000834 **SRAMROM_BOOT_MISC7** **SRAMROM Spare Register 7** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sramrom_boot_misc7[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_boot_misc7[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		sramrom_boot_misc7	SARMROM spare register 7

10000838 **SRAMROM_MISC_LOCK_KEY** **SRAMROM_MISC_LOCK_KEY** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRAMROM_MISC_LOCK_KEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		SRAMROM_MISC_LOCK_KEY	If the key matches 0xAD98, MISC_LOCK_CON, MISC_RST_CON, MISC_SEC_CON can be written.

1000083C **SRAMROM_MISC_LOCK_CON** **SRAMROM_MISC_LOCK_CON** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SRAMROM_BOOT_MISC7_LOCK_CON	SRAMROM_BOOT_MISC6_LOCK_CON	SRAMROM_BOOT_MISC5_LOCK_CON	SRAMROM_BOOT_MISC4_LOCK_CON	SRAMROM_BOOT_MISC3_LOCK_CON	SRAMROM_BOOT_MISC2_LOCK_CON	SRAMROM_BOOT_MISC1_LOCK_CON	SRAMROM_BOOT_MISC0_LOCK_CON
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7		SRAMROM_BOOT_MISC7_LOCK_CON	**SRAMROM_BOOT_MISC7 lock bit** 1 will change to 0 only after reset. 0: Unlock 1: Lock
6		SRAMROM_BOOT_MISC6_LOCK_CON	**SRAMROM_BOOT_MISC6 lock bit** 1 will change to 0 only after reset. 0: Unlock 1: Lock
5		SRAMROM_BOOT_MISC5_LOCK_CON	**SRAMROM_BOOT_MISC5 lock bit** 1 will change to 0 only after reset. 0: Unlock 1: Lock
4		SRAMROM_BOOT_MISC4_LOCK_CON	**SRAMROM_BOOT_MISC4 lock bit** 1will change to 0 only after reset. 0: Unlock 1: Lock
3		SRAMROM_BOOT_MISC3_LOCK_CON	**SRAMROM_BOOT_MISC3 lock bit** 1will change to 0 only after reset. 0: Unlock 1: Lock
2		SRAMROM_BOOT_MISC2_LOCK_CON	**SRAMROM_BOOT_MISC2 lock bit** 1will change to 0 only after reset. 0: Unlock 1: Lock
1		SRAMROM_BOOT_MISC1_LOCK_CON	**SRAMROM_BOOT_MISC1 lock bit** 1will change to 0 only after reset. 0: Unlock 1: Lock
0		SRAMROM_BOOT_MISC0_LOCK_CON	**SRAMROM_BOOT_MISC0 lock bit** 1will change to 0 only after reset. 0: Unlock 1: Lock

10000840 <u>SRAMROM_MISC_RST_CON</u> SRAMROM_MISC_RST_CON 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SRAMROM_B	SRAMROM_B	SRAMROM_B	SRAMROM_B	SRAMROM_B	SRAMROM_B	SRAMROM_B	SRAMROM_B

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									OOT_MISC7_RST_CON	OOT_MISC6_RST_CON	OOT_MISC5_RST_CON	OOT_MISC4_RST_CON	OOT_MISC3_RST_CON	OOT_MISC2_RST_CON	OOT_MISC1_RST_CON	OOT_MISC0_RST_CON
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7		SRAMROM_BOOT_MISC7_RST_CON	**BOOT_MISC7 reset control bit** 0: The content is reset after WDT. 1: The content is not reset after WDT.
6		SRAMROM_BOOT_MISC6_RST_CON	**BOOT_MISC6 reset control bit** 0: The content is reset after WDT. 1: The content is not reset after WDT.
5		SRAMROM_BOOT_MISC5_RST_CON	**BOOT_MISC5 reset control bit** 0: The content is reset after WDT. 1: The content is not reset after WDT.
4		SRAMROM_BOOT_MISC4_RST_CON	**BOOT_MISC4 reset control bit** 0: The content is reset after WDT. 1: The content is not reset after WDT.
3		SRAMROM_BOOT_MISC3_RST_CON	**BOOT_MISC3 reset control bit** 0: The content is reset after WDT. 1: The content is not reset after WDT.
2		SRAMROM_BOOT_MISC2_RST_CON	**BOOT_MISC2 reset control bit** 0: The content is reset after WDT. 1: The content is not reset after WDT.
1		SRAMROM_BOOT_MISC1_RST_CON	**BOOT_MISC1 reset control bit** 0: The content is reset after WDT. 1: The content is not reset after WDT.
0		SRAMROM_BOOT_MISC0_RST_CON	**BOOT_MISC0 reset control bit** 0: The content is reset after WDT. 1: The content is not reset after WDT.

10000844 **SRAMROM_MISC_SEC_CON** **SRAMROM_MISC_SEC_CON** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								SRAMROM_OTHER_SEC_CON	SRAMROM_BOOT_MISC7_SEC_CON	SRAMROM_BOOT_MISC6_SEC_CON	SRAMROM_BOOT_MISC5_SEC_CON	SRAMROM_BOOT_MISC4_SEC_CON	SRAMROM_BOOT_MISC3_SEC_CON	SRAMROM_BOOT_MISC2_SEC_CON	SRAMROM_BOOT_MISC1_SEC_CON	SRAMROM_BOOT_MISC0_SEC_CON
Type								RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8		SRAMROM_OTHER_SEC_CON	**MISC access control for MISC_LOCK_KEY, MISC_LOCK_CON, MISC_RST_CON, MISC_SEC_CON**

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Bit(s)	Mnemonic	Name	Description
			0: Follow DAPC setting 1: Secure R/W only
7		SRAMROM_BOOT_MISC7_SEC_CON	**BOOT_MISC7 secure control** 0: Follow DAPC setting 1: Secure R/W only
6		SRAMROM_BOOT_MISC6_SEC_CON	**BOOT_MISC6 secure control** 0: Follow DAPC setting 1: Secure R/W only
5		SRAMROM_BOOT_MISC5_SEC_CON	**BOOT_MISC5 secure control** 0: Follow DAPC setting 1: Secure R/W only
4		SRAMROM_BOOT_MISC4_SEC_CON	**BOOT_MISC4 secure control** 0: Follow DAPC setting 1: Secure R/W only
3		SRAMROM_BOOT_MISC3_SEC_CON	**BOOT_MISC3 secure control** 0: Follow DAPC setting 1: Secure R/W only
2		SRAMROM_BOOT_MISC2_SEC_CON	**BOOT_MISC2 secure control** 0: Follow DAPC setting 1: Secure R/W only
1		SRAMROM_BOOT_MISC1_SEC_CON	**BOOT_MISC1 secure control** 0: Follow DAPC setting 1: Secure R/W only
0		SRAMROM_BOOT_MISC0_SEC_CON	**BOOT_MISC0 secure control** 0: Follow DAPC setting 1: Secure R/W only

10000F00 **INFRA_AO_SEC_CON** **INFRA AO Secure Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															conn_map_lock	md2_map_lock
Type															RW	RW
Reset															0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	md1_map_lock													conn_map_sen	md2_map_sen	md1_map_sen
Type	RW													RW	RW	RW
Reset	0													0	0	0

Bit(s)	Mnemonic	Name	Description
17		conn_map_lock	**Lock register for CONNSYS remap register** 0: conn2ap_addr_remap and conn2ap_addr_remap_en of CONN_MAP0 and this bit can be modified. 1: conn2ap_addr_remap and conn2ap_addr_remap_en of CONN_MAP0 and this bit are locked.
16		md2_map_lock	**Lock register for MDSYS2 remap register** 0: MD2_BANK0_MAP0, MD2_BANK0_MAP1, MD2_BANK4_MAP0, MD2_BANK4_MAP1 and this bit can be modified. 1: MD2_BANK0_MAP0, MD2_BANK0_MAP1,

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Bit(s)	Mnemonic	Name	Description
			MD2_BANK4_MAP0, MD2_BANK4_MAP1 and this bit are locked.
15		md1_map_lock	**Lock register for MDSYS1 remap register** 0: MD1_BANK0_MAP0, MD1_BANK0_MAP1, MD1_BANK4_MAP0, MD1_BANK4_MAP1 and this bit can be modified. 1: MD1_BANK0_MAP0, MD1_BANK0_MAP1, MD1_BANK4_MAP0, MD1_BANK4_MAP1 and this bit are locked.
2		conn_map_sen	**Secure control register for CONNSYS remap register** 0: conn2ap_addr_remap and conn2ap_addr_remap_en of CONN_MAP0, conn_map_lock and this bit can be accessed in normal and secure world. 1: conn2ap_addr_remap and conn2ap_addr_remap_en of CONN_MAP0, conn_map_lock and this bit can only be accessed in secure world
1		md2_map_sen	**Secure control register for MDSYS2 remap** 0: MD2_BANK0_MAP0, MD2_BANK0_MAP1, MD2_BANK4_MAP0, MD2_BANK4_MAP1, md2_map_lock and this bit can be accessed in normal and secure world. 1: MD2_BANK0_MAP0, MD2_BANK0_MAP1, MD2_BANK4_MAP0, MD2_BANK4_MAP1, md2_map_lock and this bit can only be accessed in secure world.
0		md1_map_sen	**Secure control register for MDSYS1 remap** 0: MD1_BANK0_MAP0, MD1_BANK0_MAP1, MD1_BANK4_MAP0, MD1_BANK4_MAP1, md1_map_lock and this bit can be accessed in normal and secure world. 1: MD1_BANK0_MAP0, MD1_BANK0_MAP1, MD1_BANK4_MAP0, MD1_BANK4_MAP1, md1_map_lock and this bit can only be accessed in secure world.

10000F10 **GCPU_SEC_CON** **GCPU AO Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														gcpu_lock_sw_otp	gcpu_lock_trap	gcpu_init
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2		gcpu_lock_sw_otp	**Lock SW OTP flag** 0: Unlock 1: Lock SW OTP
1		gcpu_lock_trap	**Lock trapping flag** 0: Unlock 1: Lock trapping value
0		gcpu_init	**GCPU AO initialization flag** 0: Not initialized 1: Initialized

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Module name: infracfg_reg Base address: (+10201000h)

Address	Name	Width	Register Function
10201000	TOPAXI_SI0_STA	32	Top AXI Fabric SI0 Control Register
10201004	TOPAXI_SI1_CTL	32	Top AXI Fabric SI1 Control Register
1020101C	TOPAXI_MI_STA	32	TOP AXI Fabric MI Status
10201100	INFRA_TOP_DBG_CON0	32	INFRA TOP Debug Control 0
10201104	INFRA_TOP_DBG_CON1	32	INFRA TOP Debug Control 1
10201108	INFRA_TOP_DBG_CON2	32	INFRA TOP Debug Control 2
1020110C	INFRA_TOP_DBG_CON3	32	INFRA TOP Debug Control 3

10201000 **TOPAXI_SI0_STA** **Top AXI Fabric SI0 Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								topaxi_sio_ctrl_updated								
Type								RU								
Reset								0								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name			topaxi_sio_wr_ot_busy	topaxi_sio_rd_ot_busy	topaxi_sio_set_rid_miss	topaxi_sio_set_bid_miss	topaxi_sio_dfslv_set_wirq	topaxi_sio_dfslv_set_rirq	topaxi_sio_r_chnl_sel				topaxi_sio_b_chnl_sel			
Type			RU	RU	RU	RU	RU	RU	RU				RU			
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24		topaxi_sio_ctrl_updated	
13		topaxi_sio_wr_ot_busy	
12		topaxi_sio_rd_ot_busy	
11		topaxi_sio_set_rid_miss	
10		topaxi_sio_set_bid_miss	
9		topaxi_sio_dfslv_set_wirq	
8		topaxi_sio_dfslv_set_rirq	
7:4		topaxi_sio_r_chnl_sel	

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Bit(s)	Mnemonic	Name	Description
3:0		topaxi_si0_b_chnl_sel	

10201004 TOPAXI_SI1_CTL Top AXI Fabric SI1 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								topaxi_si1_ctrl_updated								
Type								RU								
Reset								0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			topaxi_si1_wr_ot_busy	topaxi_si1_rd_ot_busy	topaxi_si1_set_rid_miss	topaxi_si1_set_bid_miss	topaxi_si1_dfslv_set_wirq	topaxi_si1_dfslv_set_rirq		topaxi_si1_r_chnl_sel				topaxi_si1_b_chnl_sel		
Type			RU	RU	RU	RU	RU	RU		RU				RU		
Reset			0	0	0	0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
24		topaxi_si1_ctrl_updated	
13		topaxi_si1_wr_ot_busy	
12		topaxi_si1_rd_ot_busy	
11		topaxi_si1_set_rid_miss	
10		topaxi_si1_set_bid_miss	
9		topaxi_si1_dfslv_set_wirq	
8		topaxi_si1_dfslv_set_rirq	
6:4		topaxi_si1_r_chnl_sel	
2:0		topaxi_si1_b_chnl_sel	

1020101C TOPAXI_MI_STA TOP AXI Fabric MI Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									topaxi_mi1_w_b	topaxi_mi1_r_b	topaxi_mi1_err	topaxi_mi1_err	topaxi_mio_w_b	topaxi_mio_r_b	topaxi_mio_err	topaxi_mio_err

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									usy	usy	mid_set_birq	mid_set_rirq	usy	usy	mid_set_birq	mid_set_rirq
Type									RU	RU	RU	RU	RU	RU	RU	RU
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7		topaxi_mi1_w_busy	
6		topaxi_mi1_r_busy	
5		topaxi_mi1_errmid_set_birq	
4		topaxi_mi1_errmid_set_rirq	
3		topaxi_mi0_w_busy	
2		topaxi_mi0_r_busy	
1		topaxi_mi0_errmid_set_birq	
0		topaxi_mi0_errmid_set_rirq	

10201100 **INFRA_TOP_DBG_CON0** **INFRA TOP Debug Control 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**reg_debug_mon0**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		reg_debug_mon0	Debug monitor control register 0

10201104 **INFRA_TOP_DBG_CON1** **INFRA TOP Debug Control 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**reg_debug_mon1**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		reg_debug_mon1	Debug monitor control register 1

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10201108 **INFRA_TOP_DBG_CON2** **INFRA TOP Debug Control 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_debug_mon2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		reg_debug_mon2	Debug monitor control register 2

1020110C **INFRA_TOP_DBG_CON3** **INFRA TOP Debug Control 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_debug_mon3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		reg_debug_mon3	Debug monitor control register 3

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3.6 External Memory Interface

3.6.1 Introduction

The EMI controller schedules requests from the masters and issues commands to DRAMC in a efficiency way. The block conducts flow control for DRAMC and masters to avoid DRAM stall or data overflow or underflow. It also minimizes the latency of processor path to enhance the performance and tries to increase the DRAM efficiency. The block also informs clock control to gate the clock when it does not find any transaction right now. This block is designed to supply 266MHz bus clock frequency and can be scaled down to 195MHz.

3.6.2 Features

The EMI controller receives AXI master commands and issues them to the DRAM controller. It supports all AXI transaction type commands except for the fixed and cache commands. There are plenty of schedule options to schedule the command, which are:

- Starvation control
- Bandwidth limiter
- High priority
- Page hit control
- Read/write turn around prevent control

3.6.3 Block Diagram

In MT6735, the DRAM controller connects three systems via six AXI ports and supports connecting two rank DRAM devices at the same time. For cortex APMCU system, we provide a 128-bit AXI port for the connection. For the multimedia system, we provide a 128-bit AXI port for the connection. Besides, we provide three 64-bit AXI ports for connecting to modem MCU, modem 2G/3G HW and peripheral system. In the DRAM controller, the APB interface is for programming registers. Then we can initialize DRAM or other parameter settings.

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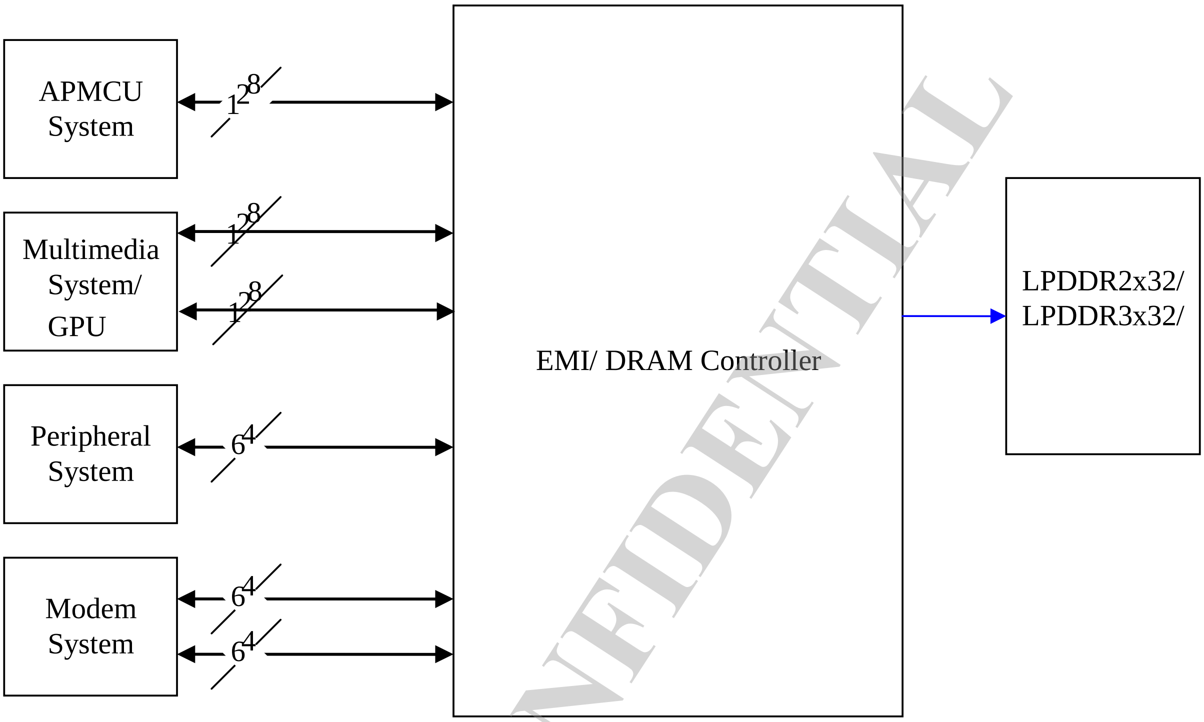

Figure 3-8. EMI/DRAM controller top connection

3.6.4 Register Definition

Module name: EMI_REG Base address: (+10203000h)

Address	Name	Width	Register Function
10203000	EMI_CONA	32	Address Mapping
10203008	EMI_CONB	32	Data Transfer Overhead for Specific Data Size
10203010	EMI_CONC	32	Data Transfer Overhead for Specific Data Size
10203018	EMI_COND	32	FIFO Status
10203020	EMI_CONE	32	Feature Setting
10203028	EMI_CONF	32	Address Scramble Setting
10203030	EMI_CONG	32	Data Transfer Overhead for Specific Non-36 bytes Alignment Data Size
10203038	EMI_CONH	32	Address Mapping 2
10203040	EMI_CONI	32	ISP Configuration
10203048	EMI_CONJ	32	ISP Configuration 1
10203050	EMI_CONK	32	ISP Configuration 2
10203060	EMI_CONM	32	MISC
10203078	EMI_MDCT	32	EMI MODEN Control Register
102030D0	EMI_TEST0	32	Test Mode 0
102030D8	EMI_TEST1	32	Test Mode 1
102030E0	EMI_TESTA	32	Test Mode A
102030E8	EMI_TESTB	32	Test Mode B
102030F0	EMI_TESTC	32	Test Mode B
102030F8	EMI_TESTD	32	Test Mode D

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Address	Name	Width	Register Function
10203100	EMI_ARBA	32	EMI Bandwidth Filter Control M0/1
10203108	EMI_ARBB	32	EMI Bandwidth Filter control M1
10203110	EMI_ARBC	32	EMI Bandwidth Filter control M2
10203118	EMI_ARBD	32	EMI Bandwidth Filter Control M3
10203120	EMI_ARBE	32	EMI Bandwidth Filter Control M4
10203128	EMI_ARBF	32	EMI Bandwidth Filter Control M5
10203134	EMI_ARBG_2ND	32	EMI Bandwidth Filter Control GPU_2
10203140	EMI_ARBI	32	Filter Priority Encode
10203144	EMI_ARBI_2ND	32	Filter Priority Encode for MD Requirement
10203148	EMI_ARBJ	32	Turn Around Command Number
1020314C	EMI_ARBJ_2ND	32	Turn Around Command Number for MD Requirement
10203150	EMI_ARBK	32	Channel Arbiter Control
10203154	EMI_ARBK_2ND	32	Channel Arbiter Control
10203158	EMI_SLCT	32	EMI Slave Control Registers
10203160	EMI_MPUA	32	Memory Protection Unit Control Registers A
10203168	EMI_MPUB	32	Memory Protection Unit Control Registers B
10203170	EMI_MPUC	32	Memory Protection Unit Control Registers C
10203178	EMI_MPUD	32	Memory Protection Unit Control Registers D
10203180	EMI_MPUE	32	Memory Protection Unit Control Registers E
10203188	EMI_MPUF	32	Memory Protection Unit Control Registers F
10203190	EMI_MPUG	32	Memory Protection Unit Control Registers G
10203198	EMI_MPUH	32	Memory Protection Unit Control Registers H
102031A0	EMI_MPUI	32	Memory Protection Unit Control Registers I
102031A4	EMI_MPUI_2ND	32	Memory Protection Unit Control Registers I
102031A8	EMI_MPUJ	32	Memory Protection Unit Control Registers J
102031AC	EMI_MPUJ_2ND	32	Memory Protection Unit Control Registers J
102031B0	EMI_MPUK	32	Memory Protection Unit Control Registers K
102031B4	EMI_MPUK_2ND	32	Memory Protection Unit Control Registers K
102031B8	EMI_MPUL	32	Memory Protection Unit Control Registers L
102031BC	EMI_MPUL_2ND	32	Memory Protection Unit Control Registers L
102031C0	EMI_MPUM	32	Memory Protection Unit Control Registers M
102031C8	EMI_MPUN	32	Memory Protection Unit Control Registers N
102031D0	EMI_MPUO	32	Memory Protection Unit Control Registers O
102031D8	EMI_MPUP	32	Memory Protection Unit Control Registers P
102031E0	EMI_MPUQ	32	Memory Protection Unit Control Registers Q
102031E8	EMI_MPUR	32	Memory Protection Unit Control Registers R
102031F0	EMI_MPUS	32	Memory Protection Unit Control Registers S
102031F8	EMI_MPUT	32	Memory Protection Unit Control Registers T
10203200	EMI_MPUU	32	Memory Protection Unit Control Registers U
10203220	EMI_MPUY	32	Memory Protection Unit Control Registers Y
10203260	EMI_MPUA2	32	Memory Protection Unit Control Registers A
10203268	EMI_MPUB2	32	Memory Protection Unit Control Registers B
10203270	EMI_MPUC2	32	Memory Protection Unit Control Registers C
10203278	EMI_MPUD2	32	Memory Protection Unit Control Registers D
10203280	EMI_MPUE2	32	Memory Protection Unit Control Registers E
10203288	EMI_MPUF2	32	Memory Protection Unit Control Registers F

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Address	Name	Width	Register Function
10203290	EMI_MPUG2	32	Memory Protection Unit Control Registers G
10203298	EMI_MPUH2	32	Memory Protection Unit Control Registers H
102032A0	EMI_MPUI2	32	Memory Protection Unit Control Registers I
102032A4	EMI_MPUI2_2ND	32	Memory Protection Unit Control Registers I
102032A8	EMI_MPUJ2	32	Memory Protection Unit Control Registers J
102032AC	EMI_MPUJ2_2ND	32	Memory Protection Unit Control Registers J
102032B0	EMI_MPUK2	32	Memory Protection Unit Control Registers K
102032B4	EMI_MPUK2_2ND	32	Memory Protection Unit Control Registers K
102032B8	EMI_MPUL2	32	Memory Protection Unit Control Registers L
102032BC	EMI_MPUL2_2ND	32	Memory Protection Unit Control Registers L
102032C0	EMI_MPUM2	32	Memory Protection Unit Control Registers M
102032C8	EMI_MPUN2	32	Memory Protection Unit Control Registers N
102032D0	EMI_MPUO2	32	Memory Protection Unit Control Registers O
102032D8	EMI_MPUP2	32	Memory Protection Unit Control Registers P
102032E0	EMI_MPUQ2	32	Memory Protection Unit Control Registers Q
102032E8	EMI_MPUR2	32	Memory Protection Unit Control Registers R
10203300	EMI_MPUU2	32	Memory Protection Unit Control Registers U
10203320	EMI_MPUY2	32	Memory Protection Unit Control Registers Y
10203400	EMI_BMEN	32	EMI Bus Monitor Control Registers
10203404	EMI_BSTP	32	EMI bus monitor auto stop count
10203408	EMI_BCNT	32	EMI 3rd Double-word Counter of Selected Masters
10203410	EMI_TACT	32	EMI 4th Double-Word Counter of Selected Masters
10203418	EMI_TSCT	32	EMI 3rd Double-word Counter of Selected Masters
10203420	EMI_WACT	32	EMI 4th Double-Word Counter of Selected Masters
10203428	EMI_WSCT	32	EMI 3rd Double-word Counter of Selected Masters
10203430	EMI_BACT	32	EMI 4th Double-Word Counter of Selected Masters
10203438	EMI_BSCT	32	EMI 3rd Double-word Counter of Selected Masters
10203440	EMI_MSEL	32	EMI 4th Double-Word Counter of Selected Masters
10203448	EMI_TSCT2	32	EMI 4th Double-Word Counter of Selected Masters
10203450	EMI_TSCT3	32	EMI 3rd Double-word Counter of Selected Masters
10203458	EMI_WSCT2	32	EMI 4th Double-Word Counter of Selected Masters
10203460	EMI_WSCT3	32	EMI 3rd Double-word Counter of Selected Masters
10203464	EMI_WSCT4	32	EMI 4th Double-Word Counter of Selected Masters
10203468	EMI_MSEL2	32	EMI Master Selection for 4th and 5th Counters
10203470	EMI_MSEL3	32	EMI Master Selection for 6th and 7th Counters
10203478	EMI_MSEL4	32	EMI Master Selection for 8th and 9th Counters
10203480	EMI_MSEL5	32	EMI Master Selection for 10th and 11th Counters
10203488	EMI_MSEL6	32	EMI Master Selection for 12th and 13th Counters
10203490	EMI_MSEL7	32	EMI Master Selection for 14th and 15th Counters
10203498	EMI_MSEL8	32	EMI Master Selection for 16th and 17th Counters
102034A0	EMI_MSEL9	32	EMI Master Selection for 18th and 19th Counters
102034A8	EMI_MSEL10	32	EMI Master Selection for 20th and 21st Counters
102034B0	EMI_BMID0	32	EMI ID Selection for 1- 2 Transaction Type Counters
102034B4	EMI_BMID1	32	EMI ID Selection for 3- 4 Transaction Type Counters

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Address	Name	Width	Register Function
102034B8	EMI_BMID2	32	EMI ID Selection for 5- 6 Transaction Type Counters
102034BC	EMI_BMID3	32	EMI ID Selection for 7- 8 Transaction Type Counters
102034C0	EMI_BMID4	32	EMI ID Selection for 9- 10 Transaction Type Counters
102034C4	EMI_BMID5	32	EMI ID Selection for 11- 12 Transaction Type Counters
102034C8	EMI_BMID6	32	EMI ID Selection for 13- 14 Transaction Type Counters
102034CC	EMI_BMID7	32	EMI ID Selection for 15- 16 Transaction Type Counters
102034D0	EMI_BMID8	32	EMI ID Selection for 17- 18 Transaction Type Counters
102034D4	EMI_BMID9	32	EMI ID Selection for 19- 20 Transaction Type Counters
102034D8	EMI_BMID10	32	EMI ID Selection for 21 Transaction Type Counters
102034E0	EMI_BMEN1	32	EMI ID Selection Enabling
102034E8	EMI_BMEN2	32	EMI ID Selection Enabling
102034F8	EMI_BMRW0	32	EMI ID Selection High Bit for 1-16 Transaction Type Counters
102034FC	EMI_BMRW1	32	EMI ID Selection High Bit for 1-16 Transaction Type Counters
10203500	EMI_TTYPE1	32	EMI 1st Transaction Type Counter of Selected Masters
10203508	EMI_TTYPE2	32	EMI 2nd Transaction Type Counter of Selected Masters
10203510	EMI_TTYPE3	32	EMI 3rd Transaction Type Counter of Selected Masters
10203518	EMI_TTYPE4	32	EMI 4th Transaction Type Counter of Selected Masters
10203520	EMI_TTYPE5	32	EMI 5th Transaction Type Counter of Selected Masters
10203528	EMI_TTYPE6	32	EMI 6th Transaction Type Counter of Selected Masters
10203530	EMI_TTYPE7	32	EMI 7th Transaction Type Counter of Selected Masters
10203538	EMI_TTYPE8	32	EMI 8th Transaction Type Counter of Selected Masters
10203540	EMI_TTYPE9	32	EMI 9th Transaction Type Counter of Selected Masters
10203548	EMI_TTYPE10	32	EMI 10th Transaction Type Counter of Selected Masters
10203550	EMI_TTYPE11	32	EMI 11th Transaction Type Counter of Selected Masters
10203558	EMI_TTYPE12	32	EMI 12th Transaction Type Counter of Selected Masters
10203560	EMI_TTYPE13	32	EMI 13th Transaction Type Counter of Selected Masters
10203568	EMI_TTYPE14	32	EMI 14th Transaction Type Counter of Selected Masters
10203570	EMI_TTYPE15	32	EMI 15th Transaction Type Counter of Selected Masters
10203578	EMI_TTYPE16	32	EMI 16th Transaction Type Counter of Selected Masters
10203580	EMI_TTYPE17	32	EMI 17th Transaction Type Counter of Selected Masters
10203588	EMI_TTYPE18	32	EMI 18th Transaction Type Counter of Selected Masters
10203590	EMI_TTYPE19	32	EMI 19th Transaction Type Counter of Selected Masters
10203598	EMI_TTYPE20	32	EMI 20th Transaction Type Counter of Selected Masters
102035A0	EMI_TTYPE21	32	EMI 21st Transaction Type Counter of Selected Masters
102035E0	EMI_WP_ADR	32	Watch Point Address
102035E8	EMI_WP_CTRL	32	Watch Point Range
102035F0	EMI_CHKER	32	EMI AXI Checker
102035F4	EMI_CHKER_TYPE	32	EMI AXI Checker Type
102035F8	EMI_CHKER_ADR	32	EMI AXI Checker Address

10203000 EMI_CONA Address Mapping 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name					RAN K_P OS										DUA L_R ANK _EN	
Type					RW										RW	
Reset					0										0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ROW2ND		ROW						COL2ND		COL				DW3 2_E N	
Type	RW		RW						RW		RW				RW	
Reset	0	0	0	0					0	0	0	0			1	

Bit(s)	Name	Description
27	RANK_POS	**Selects memory mapping** 0: Address = {rank, row, bank,col} 1: Address = {row, rank, bank, col}. This mode is only supported when dual rank has the same bank and column bits.
17	DUAL_RANK_EN	**Enables two DRAM in one channel mode for channel 0** 0: Disable dual rank mode 1: Enable dual rank mode
15:14	ROW2ND	**Rank 2 row address bit number** 0: 13-bit column address 1: 14-bit column address 2: 15-bit column address 3: 16-bit column address
13:12	ROW	**Row address bit number** 0: 13-bit column address 1: 14-bit column address 2: 15-bit column address 3: 16-bit column address
7:6	COL2ND	**Rank 2 Column address bit number** 0: 9-bit column address (x32 only) 1: 10-bit column address 2: 11-bit column address 3: Reserved
5:4	COL	**Column address bit number** 0: 9-bit column address (x32 only) 1: 10-bit column address 2: 11-bit column address 3: Reserved
1	DW32_EN	**32-bit data bus setting** 0: Reserved 1: Data bus support 32 bits.

10203008 **EMI_CONB** **Data Transfer Overhead for Specific Data Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FOUR								THREE							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TWO								ONE							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:24	FOUR	**Overhead for four cycles of data transfer** 0: 0 overhead 1: 1/16 overhead 2: 1/8 overhead ... 255: 15+ (15/16) overhead
23:16	THREE	**Overhead for three cycles of data transfer** 0: 0 overhead 1: 1/16 overhead 2: 1/8 overhead ... 255: 15+ (15/16) overhead
15:8	TWO	**Overhead for two cycles of data transfer.** 0: 0 overhead 1: 1/16 overhead 2: 1/8 overhead ... 255: 15+ (15/16) overhead
7:0	ONE	**Overhead for one cycle of data transfer** 0: 0 overhead 1: 1/16 overhead 2: 1/8 overhead. ... 255: 15+ (15/16) overhead

10203010 **EMI_CONC** **Data Transfer Overhead for Specific Data Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EIGHT								SEVEN							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIX								FIVE							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	EIGHT	**Overhead for eight cycles of data transfer** 0: 0 overhead 1: 1/16 overhead 2: 1/8 overhead ... 255: 15+ (15/16) overhead
23:16	SEVEN	**Overhead for seven cycles data transfer** 0: 0 overhead 1: 1/16 overhead 2: 1/8 overhead ... 255: 15+ (15/16) overhead
15:8	SIX	**Overhead for six cycles of data transfer** 0: 0 overhead 1: 1/16 overhead 2: 1/8 overhead ...

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Bit(s)	Name	Description
		255: 15+ (15/16) overhead
7:0	FIVE	**Overhead for five cycles of data transfer** 0: 0 overhead 1: 1/16 overhead 2: 1/8 overhead ... 255: 15+ (15/16) overhead

10203018 EMI_COND FIFO Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WFF_BUSY_HIGH				WFF_BUSY_LOW				RFF_BUSY_HIGH				RFF_BUSY_LOW			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WFF_EMPTY_HIGH				WFF_EMPTY_LOW				RFF_EMPTY_HIGH				RFF_EMPTY_LOW			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	WFF_BUSY_HIGH	If the remaining write command FIFO is smaller than or equal to this field, rff_busy will be asserted.
27:24	WFF_BUSY_LOW	If the remaining write command FIFO is larger than this field, rff_busy will be de-asserted.
23:20	RFF_BUSY_HIGH	If the remaining read command FIFO is smaller than or equal to this field, rff_busy will be asserted.
19:16	RFF_BUSY_LOW	If the remaining read command FIFO is larger than this field, rff_busy will be de-asserted.
15:12	WFF_EMPTY_HIGH	If the remaining write command FIFO is smaller than this field, rff_empty will be de-asserted.
11:8	WFF_EMPTY_LOW	If the remaining write command FIFO is larger than or equal to this field, rff_empty will be asserted.
7:4	RFF_EMPTY_HIGH	If the remaining read command FIFO is smaller than this field, rff_empty will be de-asserted.
3:0	RFF_EMPTY_LOW	If the remaining read command FIFO is larger than or equal to this field, rff_empty will be asserted.

10203020 EMI_CONE Feature Setting 00000048

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AP_BUSY_WR_LAT								AP_BUSY_RD_LAT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AP_BUSY_THR				RCMD_OO_THR				DRAMC_CMD_CNT			
Type					RW				RW				RW			
Reset					0	0	0	0	0	1	0	0	1	0	0	0

Bit(s)	Name	Description
31:24	AP_BUSY_WR_LAT	**EMI APMCU busy threshold** If BW usage is over AP_BUSY_THR/16, EMI will change APMCU write starvation counter to AP_BUSY_WR_LAT.

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Bit(s)	Name	Description
23:16	AP_BUSY_RD_LAT	**EMI APMCU busy threshold** If BW usage is over AP_BUSY_THR/16, EMI will change APMCU read starvation counter to AP_BUSY_RD_LAT.
11:8	AP_BUSY_THR	**EMI APMCU busy threshold** If BW usage is over AP_BUSY_THR/16, EMI will change APMCU starvation counter to AP_BUSY_RD_LAT and AP_BUSY_WR_LAT. 0: Does not use AP_BUSY_RD_LAT and AP_BUSY_WR_LAT. 1: 1/16 BW --- 14: 14/16 BW 15: 15/16 BW
7:4	RCMD_OO_THR	**When RDQ is less than or equal to RCMD_OO_THR, EMI will stop reading out-of-order push.** This field cannot be 0.
3:0	DRAMC_CMD_CNT	**DRAMC command FIFO count for test**

10203028 EMI_CONF Address Scramble Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BIT16_SCRAMBLE				BIT15_SCRAMBLE				BIT14_SCRAMBLE				BIT13_SCRAMBLE			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIT12_SCRAMBLE				BIT11_SCRAMBLE											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Name	Description
31:28	BIT16_SCRAMBLE	**Enables scramble with address bit[19:16]** xxx1: XOR with address bit[16] xx1x: XOR with address bit[17] x1xx: XOR with address bit[18] 1xxx: XOR with address bit[19]
27:24	BIT15_SCRAMBLE	**Enables scramble with address bit[19:16]** xxx1: XOR with address bit[16] xx1x: XOR with address bit[17] x1xx: XOR with address bit[18] 1xxx: XOR with address bit[19]
23:20	BIT14_SCRAMBLE	**Enables scramble with address bit[19:16]** xxx1: XOR with address bit[16] xx1x: XOR with address bit[17] x1xx: XOR with address bit[18] 1xxx: XOR with address bit[19]
19:16	BIT13_SCRAMBLE	**Enables scramble with address bit[19:16]** xxx1: XOR with address bit[16] xx1x: XOR with address bit[17] x1xx: XOR with address bit[18] 1xxx: XOR with address bit[19]
15:12	BIT12_SCRAMBLE	**Enables scramble with address bit[19:16]** xxx1: XOR with address bit[16] xx1x: XOR with address bit[17] x1xx: XOR with address bit[18] 1xxx: XOR with address bit[19]

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Bit(s)	Name	Description
11:8	BIT11_SCRAMBLE	**Enables scramble with address bit[19:16]** SEDA does not support bit[11:9] scramble. xxx1: XOR with address bit[16] xx1x: XOR with address bit[17] x1xx: XOR with address bit[18] 1xxx: XOR with address bit[19]

10203030 **EMI_CONG** **Data Transfer Overhead for Specific Non-36 bytes Alignment Data Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EIGHT								SIX							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FOUR								TWO							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	EIGHT	**Overhead for eight cycles of data transfer** 0: 0 overhead 1: 1/16 overhead 2: 1/8 overhead ... 255: 15+ (15/16) overhead
23:16	SIX	**Overhead for six cycles of data transfer** 0: 0 overhead 1: 1/16 overhead 2: 1/8 overhead ... 255: 15+ (15/16) overhead
15:8	FOUR	**Overhead for four cycles of data transfer.** 0: 0 overhead 1: 1/16 overhead 2: 1/8 overhead ... 255: 15+ (15/16) overhead
7:0	TWO	**Overhead for two cycles of data transfer** 0: 0 overhead 1: 1/16 overhead 2: 1/8 overhead. ... 255: 15+ (15/16) overhead

10203038 **EMI_CONH** **Address Mapping 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHN1_RANK1_SIZE				CHN1_RANK0_SIZE				CHN0_RANK1_SIZE				CHN0_RANK0_SIZE			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																

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Reset																

Bit(s)	Name	Description
31:28	CHN1_RANK1_SIZE	**Channel 1 rank 1 DRAM size** 0: Depend on CONA setting Others: Channel 1 rank 1 DRAM size is CHN1_RANK1_SIZE*256MB.
27:24	CHN1_RANK0_SIZE	**Channel 1 rank 0 DRAM size** 0: Depend on CONA setting Others: Channel 1 rank 0 DRAM size is CHN1_RANK0_SIZE*256MB.
23:20	CHN0_RANK1_SIZE	**Channel 0 rank 1 DRAM size** 0: Depend on CONA setting Others: Channel 0 rank 1 DRAM size is CHN1_RANK1_SIZE*256MB.
19:16	CHN0_RANK0_SIZE	**Channel 0 rank 0 DRAM size** 0: Depend on CONA setting Others: Channel 0 rank 0 DRAM size is CHN0_RANK0_SIZE*256MB.

10203040 EMI_CONI ISP Configuration 00000006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ISP_WR_LATENCY								ISP_RD_LATENCY							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPU_WR_OS_THR_2				GPU_RD_OS_THR_2				ISP_ID2_EN		ISP_ID1_EN			MM_W_INFO_NUM		
Type	RW				RW				RW		RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0		1	1	

Bit(s)	Name	Description
31:24	ISP_WR_LATENCY	**Allowable write latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
23:16	ISP_RD_LATENCY	**Allowable read latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
15:12	GPU_WR_OS_THR_2	**Slave port write outstanding number** 0/1/2~14/15 is 0/1/2/3/~/15.
11:8	GPU_RD_OS_THR_2	**Slave port read outstanding number** 0/1/2~14/15 is 0/4/6/~/30
7:6	ISP_ID2_EN	**Enables ISP ID match set 2** bit 0: Enable read bit 1: Enable write
5:4	ISP_ID1_EN	**Enables ISP ID match set 1** bit 0: Enable read bit 1: Enable write
2:1	MM_W_INFO_NUM	**MM port write information queue number**

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10203048 EMI_CONJ ISP Configuration 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ISP_ID_SET1_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISP_ID_SET1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ISP_ID_SET1_EN	Enables ISP ID match set 1 bit
15:0	ISP_ID_SET1	ISP ID match set 1

10203050 EMI_CONK ISP Configuration 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ISP_UD_SET2_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISP_ID_SET2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ISP_UD_SET2_EN	Enables ISP ID match set 2 bit
15:0	ISP_ID_SET2	ISP ID match set 2

10203060 EMI_CONM MISC 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EMI_DCM_DIS								WR_RSV_NOR_NUM				RD_RSV_NOR_NUM			
Type	RW								RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						EMI_ENABLE	AGE_SPEED		PAGE_HIT_HIGH_PRIO_M7	PAGE_HIT_HIGH_PRIO_M6	PAGE_HIT_HIGH_PRIO_M5	PAGE_HIT_HIGH_PRIO_M4	PAGE_HIT_HIGH_PRIO_M3	PAGE_HIT_HIGH_PRIO_M2	PAGE_HIT_HIGH_PRIO_M1	PAGE_HIT_HIGH_PRIO_M0
Type						RW	RW		RW	RW	RW	RW	RW	RW	RW	RW
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	EMI_DCM_DIS	**Disables EMI DCM** Bit 0: Disable write command and data DCM Bit 1: Disable read command DCM Bit 2: Disable read data DCM Bit 3: Reserved Bit 4: Disable emi_check module DCM

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Bit(s)	Name	Description
		Bit 5: Disable emi_command arbiter DCM Bit 6: Disable EMI top DCM Bit 7: Disable EMI APB DCM
23:20	WR_RSV_NOR_NUM	**Reserved write buffer for M0, ultra and under BW limiter request**
19:16	RD_RSV_NOR_NUM	**Reserved read buffer for M0, ultra and under BW limiter request**
10	EMI_ENABLE	**Enables EMI/DRAMC access** 0: No agent can access EMI or DRAMC. EMI will issue INT when someone accesses EMI. 1: Normal mode. EMI/DRAMC can be accessed.
9:8	AGE_SPEED	**Age decrement speed when bandwidth usage is larger than allocated one** 00: No decrement when bandwidth usage is larger than allocated one 01: 1/4 speed decrement when bandwidth usage is larger than allocated one 10: Normal speed decrement when bandwidth usage is larger than allocated one 11: 1/2 speed decrement when bandwidth usage is larger than allocated one
7	PAGE_HIT_HIGH_PRIO_M7	**Setting of page hit command is received first** 0: Does not receive page hit command when the master has issued allocated bandwidth 1: Receive page hit command first
6	PAGE_HIT_HIGH_PRIO_M6	**Setting of page hit command is received first** 0: Does not receive page hit command when the master has issued allocated bandwidth 1: Receive page hit command first
5	PAGE_HIT_HIGH_PRIO_M5	**Setting of page hit command is received first** 0: Does not receive page hit command when the master has issued allocated bandwidth 1: Receive page hit command first
4	PAGE_HIT_HIGH_PRIO_M4	**Setting of page hit command is received first** 0: Does not receive page hit command when the master has issued allocated bandwidth 1: Receive page hit command first
3	PAGE_HIT_HIGH_PRIO_M3	**Setting of page hit command is received first** 0: Does not receive page hit command when the master has issued allocated bandwidth 1: Receive page hit command first
2	PAGE_HIT_HIGH_PRIO_M2	**Setting of page hit command is received first** 0: Does not receive page hit command when the master has issued allocated bandwidth 1: Receive page hit command first
1	PAGE_HIT_HIGH_PRIO_M1	**Setting of page hit command is received first** 0: Does not receive page hit command when the master has issued allocated bandwidth 1: Receive page hit command first
0	PAGE_HIT_HIGH_PRIO_M0	**Setting of page hit command is received first** 0: Does not receive page hit command when the master has issued allocated bandwidth 1: Receive page hit command first

10203078 EMI_MDCT EMI MODEN Control Register 12000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name		WR_AP_RSV_NUM				RD_AP_RSV_NUM				WR_ULTRA_RSV_NUM				RD_ULTRA_RSV_NUM		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	1	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SBR_WRAP_MODE	MDMCU_SBR_EN	EXPIRE_SBR_EN	ULTRA_SBR_EN	W_ULTRA_WAIT_EN	R_ULTRA_W AIT_EN	W_ALL_WAIT_EN	R_ALL_WAIT_EN	W_ULTRA_STAR_WAIT_EN	R_ULTRA_STAR_WAIT_EN	W_S_AGE_EN	R_S_AGE_EN	W_S_ULT_EN	R_S_ULT_EN	W_A_ULT_EN	R_A_ULT_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:28	WR_AP_RSV_NUM	**Reserved write buffer for APMCU & ultra**
26:24	RD_AP_RSV_NUM	**Reserved read buffer for APMCU & ultra**
22:20	WR_ULTRA_RSV_NUM	**Reserved write buffer for ultra**
18:16	RD_ULTRA_RSV_NUM	**Reserved read buffer for ultra**
15	SBR_WRAP_MODE	**1: All 32B wrap accesses use 32-byte wrap mode.**
14	MDMCU_SBR_EN	**Enables MDMCU command same bank reorder push**
13	EXPIRE_SBR_EN	**Enables starvation expired command EMI to DRAMC same bank reorder push**
12	ULTRA_SBR_EN	**Enables ultra command EMI to DRAMC same bank reorder push**
11	W_ULTRA_WAIT_EN	**Enables Write ultra command waiting when page miss for MD read requirement. MD write is not applied.** 0: Does not wait 1: Wait until bank is not busy.
10	R_ULTRA_WAIT_EN	**Enables read ultra command waiting when page miss for MD read requirement. MD read is not applied.** 0: Does not wait 1: Wait until bank is not busy.
9	W_ALL_WAIT_EN	**Enables write ultra command waiting when page miss** 0: Does not wait 1: Wait until bank is not busy.
8	R_ALL_WAIT_EN	**Enables read ultra command waiting when page miss** 0: Does not wait 1: Wait until bank is not busy.
7	W_ULTRA_STAR_WAIT_EN	**Enables write ultra and starvation command waiting when page miss for MD read requirement** MD read is not applied. 0: Does not wait 1: Wait until bank is not busy.
6	R_ULTRA_STAR_WAIT_EN	**Enables read ultra and starvation command waiting when page miss for MD read requirement** MD read is not applied. 0: Does not wait 1: Wait until bank is not busy.
5	W_S_AGE_EN	**Enables M3 write starvation higher than other feature** 0: Does not enable write starvation higher than other feature 1: Support write starvation higher than other feature.
4	R_S_AGE_EN	**Enables M3 read starvation higher than other feature**

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Bit(s)	Name	Description
		0: Does not enable read starvation higher than other feature 1: Support read starvation higher than other feature.
3	W_S_ULT_EN	**Enables M3 write ultra high priority higher than other feature** 0: Does not enable read ultra high priority higher than other feature 1: Support read ultra high priority higher than other feature.
2	R_S_ULT_EN	**Enables M3 read ultra high priority higher than other feature** 0: Does not enable read ultra high priority higher than other feature 1: Support read ultra high priority higher than other feature.
1	W_A_ULT_EN	**Enables M3 write always ultra high priority feature** 0: Does not always enable ultra high priority feature 1: Always support ultra high priority feature
0	R_A_ULT_EN	**Enables M3 read always ultra high priority feature** 0: Does not always enable ultra high priority feature 1: Always support ultra high priority feature

102030D0 **EMI_TEST0** **Test Mode 0** **88888888**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**M3_WR_OUTSTANDING**				**M3_RD_OUTSTANDING**				**M2_WR_OUTSTANDING**				**M2_RD_OUTSTANDING**			
Type	RW				RW				RW				RW			
Reset	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**M1_WR_OUTSTANDING**				**M1_RD_OUTSTANDING**				**M0_WR_OUTSTANDING**				**M0_RD_OUTSTANDING**			
Type	RW				RW				RW				RW			
Reset	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0

Bit(s)	Name	Description
31:28	M3_WR_OUTSTANDING	**Slave port write outstanding number** 0/1/2~14/15 is 0/1/2/3/~/15.
27:24	M3_RD_OUTSTANDING	**Slave port read outstanding number** 0/1/2~14/15 is 0/4/6/~/30.
23:20	M2_WR_OUTSTANDING	**Slave port write outstanding number** 0/1/2~14/15 is 0/1/2/3/~/15.
19:16	M2_RD_OUTSTANDING	**Slave port read outstanding number** 0/1/2~14/15 is 0/4/6/~/30.
15:12	M1_WR_OUTSTANDING	**Slave port write outstanding number** 0/1/2~14/15 is 0/1/2/3/~/15.
11:8	M1_RD_OUTSTANDING	**Slave port read outstanding number** 0/1/2~14/15 is 0/4/6/~/30.
7:4	M0_WR_OUTSTANDING	**Slave port write outstanding number** 0/1/2~14/15 is 0/1/2/3/~/15.
3:0	M0_RD_OUTSTANDING	**Slave port read outstanding number** 0/1/2~14/15 is 0/2/4/~/30.

102030D8 **EMI_TEST1** **Test Mode 1** **88888888**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**M7_WR_OUTSTANDING**				**M7_RD_OUTSTANDING**				**M6_WR_OUTSTANDING**				**M6_RD_OUTSTANDING**			
Type	RW				RW				RW				RW			
Reset	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**M5_WR_OUTSTANDING**				**M5_RD_OUTSTANDING**				**M4_WR_OUTSTANDING**				**M4_RD_OUTSTANDING**			
Type	RW				RW				RW				RW			
Reset	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0

Bit(s)	Name	Description
31:28	M7_WR_OUTSTANDING	**Slave port write outstanding number** 0/1/2~14/15 is 0/1/2/3/~/15.
27:24	M7_RD_OUTSTANDING	**Slave port read outstanding number** 0/1/2~14/15 is 0/4/6/~/30.
23:20	M6_WR_OUTSTANDING	**Slave port write outstanding number** 0/1/2~14/15 is 0/1/2/3/~/15.
19:16	M6_RD_OUTSTANDING	**Slave port read outstanding number.** 0/1/2~14/15 is 0/4/6/~/30
15:12	M5_WR_OUTSTANDING	**Slave port write outstanding number** 0/1/2~14/15 is 0/1/2/3/~/15.
11:8	M5_RD_OUTSTANDING	**Slave port read outstanding number** 0/1/2~14/15 is 0/4/6/~/30.
7:4	M4_WR_OUTSTANDING	**Slave port write outstanding number** 0/1/2~14/15 is 0/1/2/3/~/15.
3:0	M4_RD_OUTSTANDING	**Slave port read outstanding number** 0/1/2~14/15 is 0/4/6/~/30.

102030E0 **EMI_TESTA** **Test Mode A** **33433343**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**RM_FG_CMD_THR2**				**RM_SERV_CNT_THR2**				**RM_FG_CMD_THR1**				**RM_SERV_CNT_THR1**		
Type		RW				RW				RW				RW		
Reset		0	1	1		0	1	1		1	0	0		0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**WM_FG_CMD_THR2**				**WM_SERV_CNT_THR2**				**WM_FG_CMD_THR1**				**WM_SERV_CNT_THR1**		
Type		RW				RW				RW				RW		
Reset		0	1	1		0	1	1		1	0	0		0	1	1

Bit(s)	Name	Description
30:28	RM_FG_CMD_THR2	**R_have_request_mask = serv_write & !r_have_urgent & ! more_than_max_write & [(serv_cnt <= RM_SERV_CNT_THR1 & FG_Pending_Cmd >= RM_FG_CMD_THR1) | (wcb_unmasked_diff_bk_cnt >= RM_SERV_CNT_THR2 & FG_Pending_Cmd >= WM_FG_CMD_THR2)]** This field cannot be 0.
26:24	RM_SERV_CNT_THR2	**R_have_request_mask = serv_write & !r_have_urgent & ! more_than_max_write & [(serv_cnt <= RM_SERV_CNT_THR1 & FG_Pending_Cmd >= RM_FG_CMD_THR1) | (wcb_unmasked_diff_bk_cnt >= RM_SERV_CNT_THR2 & FG_Pending_Cmd >= WM_FG_CMD_THR2)]**

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Bit(s)	Name	Description
22:20	RM_FG_CMD_THR1	**R_have_request_mask = serv_write & !r_have_urgent & ! more_than_max_write & [(serv_cnt <= RM_SERV_CNT_THR1 & FG_Pending_Cmd >= RM_FG_CMD_THR1) | (wcb_unmasked_diff_bk_cnt >= RM_SERV_CNT_THR2 & FG_Pending_Cmd >= WM_FG_CMD_THR2)]** This field cannot be 0.
18:16	RM_SERV_CNT_THR1	**R_have_request_mask = serv_write & !r_have_urgent & ! more_than_max_write & [(serv_cnt <= RM_SERV_CNT_THR1 & FG_Pending_Cmd >= RM_FG_CMD_THR1) | (wcb_unmasked_diff_bk_cnt >= RM_SERV_CNT_THR2 & FG_Pending_Cmd >= WM_FG_CMD_THR2)]**
14:12	WM_FG_CMD_THR2	**W_have_request_mask = !serv_write & !w_have_urgent & !more_than_max_read & [(serv_cnt <= WM_SERV_CNT_THR1 & FG_Pending_Cmd >= WM_FG_CMD_THR1) | (rcb_unmasked_diff_bk_cnt >= WM_SERV_CNT_THR2 & FG_Pending_Cmd >= WM_FG_CMD_THR2)]** This field cannot be 0.
10:8	WM_SERV_CNT_THR2	**W_have_request_mask = !serv_write & !w_have_urgent & !more_than_max_read & [(serv_cnt <= WM_SERV_CNT_THR1 & FG_Pending_Cmd >= WM_FG_CMD_THR1) | (rcb_unmasked_diff_bk_cnt >= WM_SERV_CNT_THR2 & FG_Pending_Cmd >= WM_FG_CMD_THR2)]**
6:4	WM_FG_CMD_THR1	**W_have_request_mask = !serv_write & !w_have_urgent & !more_than_max_read & [(serv_cnt <= WM_SERV_CNT_THR1 & FG_Pending_Cmd >= WM_FG_CMD_THR1) | (rcb_unmasked_diff_bk_cnt >= WM_SERV_CNT_THR2 & FG_Pending_Cmd >= WM_FG_CMD_THR2)]** This field cannot be 0.
2:0	WM_SERV_CNT_THR1	**W_have_request_mask = !serv_write & !w_have_urgent & !more_than_max_read & [(serv_cnt <= WM_SERV_CNT_THR1 & FG_Pending_Cmd >= WM_FG_CMD_THR1) | (rcb_unmasked_diff_bk_cnt >= WM_SERV_CNT_THR2 & FG_Pending_Cmd >= WM_FG_CMD_THR2)]**

102030E8 EMI_TESTB Test Mode B 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RD_INTERLEAVE_DIS								BW_THR				RD_DATA_MODE	WCMD_MDMCU_SUPER	RCMD_DMCU_SUPER	WR_CHK_ORDER
Type	RW								RW				RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BW_THR_LEN		Mo_SHORT_DIS	RCMD_ISSUE_IN_ORDER	EARLY_RSP_DIS	EARLY_RESP_PROWR_DIS	SBR_MASK_CHK	DBG_OUT_EN	WR_ULTRA_WO_MASK	RSV_CHK_DQ	BYTE32_WRAP_EN	HALF_AGE_EN	COMMAND_SPLIT_EN	RFF_PBC_MASK_EN	RD_PBC_MASK_EN	PREULTRA_ENABLE
Type	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:24	RD_INTERLEAVE_DIS	**Disables read data interleave function by port.**
23:20	BW_THR	**EMI BW threshold length** If BW usage is less than BW_THR/16, EMI will force M0 ultra. 0: Always non-ultra 1: 1/16 BW ... 14: 14/16 BW 15: Always enable ultra
19	RD_DATA_MODE	0: Mask master of DRAMC input data before SRAM arbiter. 1: Mask master of DRAMC input data after SRAM arbiter.
18	WCMD_MDMCU_SUPER	**MDMCU write high priority command has higher priority than other write commands.**
17	RCMD_MDMCU_SUPER	**MDMCU read high priority command has higher priority than other read command.**
16	WR_CHK_ORDER	**Writes command to DRAMC keep ID order**
15:14	BW_THR_LEN	**EMI BW threshold length** If BW usage is less than BW_THR/16, EMI will force M0 ultra. 2'b00: 256 cycles 2'b01: 512 cycles 2'b10: 1,024 cycles 2'b11: 2,048 cycles.
13	M0_SHORT_DIS	**When all FIFOs are unused, APMCU reads can bypss read command FIFO to reduce 1 cycle latency.** 0: Enable 1: Disable
12	RCMD_ISSUE_IN_ORDER	**Read command issue to DRAMC is in order** 0: Out- of- order 1: In order
11	EARLY_RSP_DIS	0: Enable early response function 1: Disable early response function
10	EARLY_RESP_PRO_WR_DIS	**When read early response occurs, EMI sets up related write FIFO to be expired.**
9	SBR_MASK_CHK	0. Non-SBR command does not check reorder mask. 1: Non-SBR command checks reorder mask.
8	DBG_OUT_EN	**Enables debug output**
7	WR_ULTRA_WO_MASK	**1: Ultra write command with starvation counter =0 doesn't need to defer read ultra with starvation counter =0**
6	RSV_CHK_DQ	**When EMI reserves buffer for AP, ultra and normal,** 0: Check command FIFO only 1: Check command and data FIFO
5	BYTE32_WRAP_EN	**Processes wrap command in 32-byte alignment** 0: Process wrap command in 16-byte alignment 1: Process wrap command in 32-byte alignment
4	HALF_AGE_EN	**Shortens starvation value for high priority command** 0: Does not shorten starvation value 1: Shorten starvation value for high priority command
3	COMMAND_SPLIT_EN	**Splits long burst read command into two short commands.** 0: Does not split read command 1: Split read command
2	RFF_PBC_MASK_EN	**Masks write command when row conflict with read command.** 0: Write commands will not be masked. 1: Mask write commands

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Bit(s)	Name	Description
1	RD_PBC_MASK_EN	**Masks read command when row conflict with read command.** 0: Read commands will not be masked. 1: Mask read commands
0	PREULTRA_ENABLE	**When this feature is enabled, FIFO has the same ID as command arbiter granted ultra and preultra command.** 1. Starvation counter /2 or /4 by setting 2. Starvation counter doesn't check BW limiter.

102030F0 EMI_TESTC Test Mode B 38470000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CDWF_THR			DEFER_WR_WDATA_THR				DEFER_WR_RDATA_THR				DEFER_WR_WO_READ_PUSH	DEFER_WR_GROUP2	DEFER_WR_GROUP	URGENT_READ_FIRST
Type		RW			RW				RW				RW	RW	RW	RW
Reset		0	1	1	1	0	0	0	0	1	0	0	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RD_REORDER_DIS								M7_HIGH	M6_HIGH	M5_HIGH	M4_HIGH	M3_HIGH	M2_HIGH	M1_HIGH	M0_HIGH
Type	RW								RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:28	CDWF_THR	**Conditional DRAMC write flush issue threshold**
27:24	DEFER_WR_WDATA_THR	**Defer write group option 2** When DRAMC pending write data are larger than defer_wr_wdata_thr, EMI stop pushing write command. 0/1/2/~/15 means write data is 0/4/8/~/60 This field cannot be 0.
23:20	DEFER_WR_RDATA_THR	**Defers write group option 1** When DRAMC pending read data are larger than defer_wr_rdata_thr, EMI stop pushing write command. 0/1/2/~/15 means write data is 0/4/8/~/60 This field cannot be 0.
19	DEFER_WR_WO_READ_PUSH	**Channel arbiter will mask write when DRAMC queue counter is less than threshold** Enable DEFER_WR_WO_READ_PUSH to remove read push in DRAMC queue count.
18	DEFER_WR_GROUP2	**Defers write group option 2** When DRAMC pending write data are larger than defer_wr_wdata_thr, EMI will stop pushing write command.
17	DEFER_WR_GROUP	**Defers write group** When DRAMC pending read data are larger than defer_wr_rdata_thr, EMI will stop pushing write command.
16	URGENT_READ_FIRST	**Read first in channel arbiter**
15:8	RD_REORDER_DIS	**Disables read command re-order feature** 0: Enable 1: Disable

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Bit(s)	Name	Description
7	M7_HIGH	**Enables bandwidth guarantee** 0: Does not enable 1: Enable bandwidth guarantee
6	M6_HIGH	**Enables bandwidth guarantee** 0: Does not enable 1: Enable bandwidth guarantee
5	M5_HIGH	**Enables bandwidth guarantee** 0: Does not enable 1: Enable bandwidth guarantee
4	M4_HIGH	**Enables bandwidth guarantee** 0: Does not enable 1: Enable bandwidth guarantee
3	M3_HIGH	**Enables bandwidth guarantee** 0: Does not enable 1: Enable bandwidth guarantee
2	M2_HIGH	**Enables bandwidth guarantee** 0: Does not enable 1: Enable bandwidth guarantee
1	M1_HIGH	**Enables bandwidth guarantee** 0: Does not enable 1: Enable bandwidth guarantee
0	M0_HIGH	**Enables bandwidth guarantee** 0: Does not enable 1: Enable bandwidth guarantee

102030F8 EMI_TESTD Test Mode D 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EX_MODE	HARD_LIMIT	LOCK_DIS	WDF_DIS								WFF_DIS				
Type	RW	RW	RW	RW								RW				
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDF_FOR_SBR			RDF_DIS								RFF_DIS				
Type	RW			RW								RW				
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
31	EX_MODE	0: Overlapping write does not clear monitor. 1: Overlapping write clears monitor.
30	HARD_LIMIT	**Hard limit function** 0: Soft limit in channel arbiter 1: Hard limit in channel arbiter
29	LOCK_DIS	**Disables lock function** 0: Does not disable 1: Disable lock function
28:24	WDF_DIS	**Disables write data buffer number** Wait for 1ms to write 0 after 1 is written. If SW disables all buffers, EMI will be hanged. Due to LOCK EMI will need one FIFO to handle read/write at the same cycle case, EMI needs at least two(do not reserve the buffer) or three(reserve buffer) FIFO.

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Bit(s)	Name	Description
20:16	WFF_DIS	**Wait for 1ms to write 0 after 1 is written.** If SW disables all buffers, EMI will be hanged. Due to LOCK EMI will need one FIFO to handle read/write at the same cycle case, EMI needs at least two (do not reserve the buffer) or three (reserve the buffer) FIFOs.
15:13	RDF_FOR_SBR	**Disables read data buffer number for SBR command** Read data FIFO number - RDF_DIS - RDF_FOR_SBR must larger than 4.
12:8	RDF_DIS	**Wait for 1ms to write 0 after 1 is written.** If SW disables all buffers, EMI will be hanged. EMI needs at least (reserved buffer+1) read FIFO.
4:0	RFF_DIS	**Wait for 1ms to write 0 after 1 is written.** If SW disables all buffers, EMI will be hanged. Due to LOCK EMI needs one FIFO to handle read/write in the same cycle case, EMI needs at least two (do not reserve the buffer) or three (reserve the buffer) FIFOs.

10203100 EMI_ARBA EMI Bandwidth Filter Control M0/1 00004000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	M0_WR_LATENCY								M0_RD_LATENCY							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	M0_BANDWIDTH_DISABLE	M0_MODE	M0_HI_PRIO_DOM_BW	M0_BW_FILTER_EN	M0_BW_FILTER_LEN		M0_DOUBLE_HALF_BW			M0_ULTRA_DOM_BW	M0_BANDWIDTH					
Type	RW	RW	RW	RW	RW		RW			RW	RW					
Reset	0	1	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	M0_WR_LATENCY	**Allowable write latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
23:16	M0_RD_LATENCY	**Allowable read latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
15	M0_BANDWIDTH_DISABLE	**Stops counting consumed bandwidth** 0: Does not stop counting 1: Stop counting
14	M0_MODE	**Bandwidth limit mode** 0: Hard mode 1: Soft mode
13	M0_HI_PRIO_DOM_BW	**High priority requests dominate bandwidth limiter** 0: High priority requests from side-band signals should be controlled by bandwidth limiter. 1: High priority requests from side-band signals always dominate bandwidth limiter control.

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Bit(s)	Name	Description
12	M0_BW_FILTER_EN	**Enables bandwidth filter** 0: Disable 1: Enable
11:10	M0_BW_FILTER_LEN	**Enables bandwidth filter** 00: Filter length = 256 cycles 01: Filter length = 512 cycles 10: Filter length = 1,024 cycles 11: Filter length = 2,048 cycles
9:8	M0_DOUBLE_HALF_BW	**Combined with allocated bandwidth.** 00: Used for one channel LPDDR2-32, DDR3-32, LPDDR3-32 10: Used for two channel LPDDR2-32, DDR3-32, LPDDR3-32 01, 11: Reserved.
6	M0_ULTRA_DOM_BW	**Ultra requests dominate bandwidth limiter** 0: Ultra priority requests from side-band signals should be controlled by bandwidth limiter. 1: Ultra priority requests from side-band signals always dominate bandwidth limiter control.
5:0	M0_BANDWIDTH	**Allocated bandwidth** Cannot be 0 in hard mode. 0: Allocate 0 of the total bandwidth 1: Allocate 1/64 of the total bandwidth 2: Allocate 2/64 of the total bandwidth --- 63: Allocate 63/64 of the total bandwidth

10203108 EMI_ARBB EMI Bandwidth Filter control M1 00004000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	M1_WR_LATENCY								M1_RD_LATENCY							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	M1_BANDWIDTH_DISABLE	M1_MODE	M1_HI_PRIO_DOM_BW	M1_BW_FILTER_EN					M1_ULTRA_SLICE_EN	M1_ULTRA_DOM_BW	M1_BANDWIDTH					
Type	RW	RW	RW	RW					RW	RW	RW					
Reset	0	1	0	0					0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	M1_WR_LATENCY	**Allowable write latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
23:16	M1_RD_LATENCY	**Allowable read latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
15	M1_BANDWIDTH_	**Stops counting consumed bandwidth**

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Bit(s)	Name	Description
	DISABLE	0: Does not stop counting 1: Stop counting
14	M1_MODE	**Bandwidth limit mode** 0: Hard mode 1: Soft mode
13	M1_HI_PRIO_DOM_BW	**High priority requests dominate bandwidth limiter** 0: High priority requests from side-band signals should be controlled by bandwidth limiter. 1: High priority requests from side-band signals always dominate bandwidth limiter control.
12	M1_BW_FILTER_EN	**Enables bandwidth filter** 0: Disable 1: Enable
7	M1_ULTRA_SLICE_EN	**Enables M1 ultra slice**
6	M1_ULTRA_DOM_BW	**Ultra requests dominate bandwidth limiter** 0: Ultra priority requests from side-band signals should be controlled by bandwidth limiter. 1: Ultra priority requests from side-band signals always dominate bandwidth limiter control.
5:0	M1_BANDWIDTH	**Allocated bandwidth** Cannot be 0 in hard mode 0: Allocate 0 of the total bandwidth 1: Allocate 1/64 of the total bandwidth 2: Allocate 2/64 of the total bandwidth ... 63: Allocate 63/64 of the total bandwidth

10203110 EMI_ARBC EMI Bandwidth Filter control M2 00004000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	M2_WR_LATENCY								M2_RD_LATENCY							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	M2_BANDWIDTH_DISABLE	M2_MODE	M2_HI_PRIO_DOM_BW	M2_BW_FILTER_EN					M2_ULTRA_SLICE_EN	M2_ULTRA_DOM_BW	M2_BANDWIDTH					
Type	RW	RW	RW	RW					RW	RW	RW					
Reset	0	1	0	0					0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	M2_WR_LATENCY	**Allowable write latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
23:16	M2_RD_LATENCY	**Allowable read latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles

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Bit(s)	Name	Description
		... 255: 1,023 cycles
15	M2_BANDWIDTH_DISABLE	**Stops counting consumed bandwidth** 0: Does not stop counting 1: Stop counting
14	M2_MODE	**Bandwidth limit mode** 0: Hard mode 1: Soft mode
13	M2_HI_PRIO_DOM_BW	**High priority requests dominate bandwidth limiter** 0: High priority requests from side-band signals should be controlled by bandwidth limiter. 1: High priority requests from side-band signals always dominate bandwidth limiter control.
12	M2_BW_FILTER_EN	**Enables bandwidth filter** 0: Disable 1: Enable
7	M2_ULTRA_SLICE_EN	**Enables M2 ultra slice**
6	M2_ULTRA_DOM_BW	**Ultra requests dominate bandwidth limiter** 0: Ultra priority requests from side-band signals should be controlled by bandwidth limiter. 1: Ultra priority requests from side-band signals always dominate bandwidth limiter control.
5:0	M2_BANDWIDTH	**Allocated bandwidth** Cannot be 0 in hard mode 0: Allocate 0 of the total bandwidth 1: Allocate 1/64 of the total bandwidth 2: Allocate 2/64 of the total bandwidth ... 63: Allocate 63/64 of the total bandwidth

10203118 EMI_ARBD EMI Bandwidth Filter Control M3 00004000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	M3_WR_LATENCY								M3_RD_LATENCY							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	M3_BANDWIDTH_DISABLE	M3_MODE	M3_HI_PRIO_DOM_BW	M3_BW_FILTER_EN						M3_ULTRA_DOM_BW	M3_BANDWIDTH					
Type	RW	RW	RW	RW						RW	RW					
Reset	0	1	0	0						0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	M3_WR_LATENCY	**Allowable read latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles

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Bit(s)	Name	Description
23:16	M3_RD_LATENCY	**Allowable write latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
15	M3_BANDWIDTH_DISABLE	**Stops counting consumed bandwidth** 0: Does not stop counting 1: Stop counting
14	M3_MODE	**Bandwidth limit mode** 0: Hard mode 1: Soft mode
13	M3_HI_PRIO_DOM_BW	**High priority requests dominate bandwidth limiter** 0: High priority requests from side-band signals should be controlled by bandwidth limiter. 1: High priority requests from side-band signals always dominate bandwidth limiter control.
12	M3_BW_FILTER_EN	**Enables bandwidth filter** 0: Disable 1: Enable
6	M3_ULTRA_DOM_BW	**Ultra requests dominate bandwidth limiter** 0: Ultra priority requests from side-band signals should be controlled by bandwidth limiter. 1: Ultra priority requests from side-band signals always dominate bandwidth limiter control.
5:0	M3_BANDWIDTH	**Allocated bandwidth** Cannot be 0 in hard mode. 0: Allocate 0 of the total bandwidth 1: Allocate 1/64 of the total bandwidth 2: Allocate 2/64 of the total bandwidth ... 63: Allocate 63/64 of the total bandwidth

10203120 EMI_ARBE EMI Bandwidth Filter Control M4 00004000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	M4_WD_LATENCY								M4_RD_LATENCY							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	M4_BANDWIDTH_DISABLE	M4_MODE	M4_HI_PRIO_DOM_BW	M4_BW_FILTER_EN						M4_ULTRA_DOM_BW	M4_BANDWIDTH					
Type	RW	RW	RW	RW						RW	RW					
Reset	0	1	0	0						0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	M4_WD_LATENCY	**Allowable latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ...

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Bit(s)	Name	Description
		255: 1,023 cycles.
23:16	M4_RD_LATENCY	**Allowable latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
15	M4_BANDWIDTH_DISABLE	**Stops counting consumed bandwidth** 0: Does not stop counting 1: Stop counting
14	M4_MODE	**Bandwidth limit mode** 0: Hard mode 1: Soft mode
13	M4_HI_PRIO_DOM_BW	**High priority requests dominate bandwidth limiter** 0: High priority requests from side-band signals should be controlled by bandwidth limiter. 1: High priority requests from side-band signals always dominate bandwidth limiter control.
12	M4_BW_FILTER_EN	**Enables bandwidth filter** 0: Disable 1: Enable
6	M4_ULTRA_DOM_BW	**Ultra requests dominate bandwidth limiter** 0: Ultra priority requests from side-band signals should be controlled by bandwidth limiter. 1: Ultra priority requests from side-band signals always dominate bandwidth limiter control.
5:0	M4_BANDWIDTH	**Allocated bandwidth** Cannot be 0 in hard mode. 0: Allocate 0 of the total bandwidth 1: Allocate 1/64 of the total bandwidth 2: Allocate 2/64 of the total bandwidth ... 63: Allocate 63/64 of the total bandwidth

10203128 EMI_ARBF EMI Bandwidth Filter Control M5 00004000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	M5_WR_LATENCY								M5_RD_LATENCY							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	M5_BANDWIDTH_DISABLE	M5_MODE	M5_HI_PRIO_DOM_BW	M5_BW_FILTER_EN					M5_ULTRA_SLICE_EN	M5_ULTRA_DOM_BW	M5_BANDWIDTH					
Type	RW	RW	RW	RW					RW	RW	RW					
Reset	0	1	0	0					0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	M5_WR_LATENCY	**Allowable write latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles

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Bit(s)	Name	Description
		... 255: 1,023 cycles
23:16	M5_RD_LATENCY	**Allowable read latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
15	M5_BANDWIDTH_DISABLE	**Stops counting consumed bandwidth** 0: Does not stop counting 1: Stop counting
14	M5_MODE	**Bandwidth limit mode** 0: Hard mode 1: Soft mode
13	M5_HI_PRIO_DOM_BW	**High priority requests dominate bandwidth limiter** 0: High priority requests from side-band signals should be controlled by bandwidth limiter. 1: High priority requests from side-band signals always dominate bandwidth limiter control.
12	M5_BW_FILTER_EN	**Enables bandwidth filter** 0: Disable 1: Enable
7	M5_ULTRA_SLICE_EN	**Enable M5 ultra slice**
6	M5_ULTRA_DOM_BW	**Ultra requests dominate bandwidth limiter** 0: Ultra priority requests from side-band signals should be controlled by bandwidth limiter. 1: Ultra priority requests from side-band signals always dominate bandwidth limiter control.
5:0	M5_BANDWIDTH	**Allocated bandwidth** Cannot be 0 in hard mode 0: Allocate 0 of the total bandwidth 1: Allocate 1/64 of the total bandwidth 2: Allocate 2/64 of the total bandwidth ... 63: Allocate 63/64 of the total bandwidth

10203134 **EMI_ARBG_2ND** **EMI Bandwidth Filter Control GPU_2** **00004000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPU_WR_LATENCY								GPU_RD_LATENCY							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPU_BANDWIDTH_DISABLE	GPU_MODE	GPU_HI_PRIO_DOM_BW	GPU_BW_FILTER_EN						GPU_ULTRA_DOM_BW	GPU_BANDWIDTH					
Type	RW	RW	RW	RW						RW	RW					
Reset	0	1	0	0						0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:24	GPU_WR_LATENCY	**Allowable write latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
23:16	GPU_RD_LATENCY	**Allowable read latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
15	GPU_BANDWIDTH_DISABLE	**Stops counting consumed bandwidth** 0: Does not stop counting 1: Stop counting
14	GPU_MODE	**Bandwidth limit mode** 0: Hard mode 1: Soft mode
13	GPU_HI_PRIO_DOM_BW	**High priority requests dominate bandwidth limiter** 0: High priority requests from side-band signals should be controlled by bandwidth limiter. 1: High priority requests from side-band signals always dominate bandwidth limiter control.
12	GPU_BW_FILTER_EN	**Enables bandwidth filter** 0: Disable 1: Enable
6	GPU_ULTRA_DOM_BW	**Ultra requests dominate bandwidth limiter** 0: Ultra priority requests from side-band signals should be controlled by bandwidth limiter. 1: Ultra priority requests from side-band signals always dominate bandwidth limiter control.
5:0	GPU_BANDWIDTH	**Allocated bandwidth** Cannot be 0 in hard mode 0: Allocate 0 of the total bandwidth 1: Allocate 1/64 of the total bandwidth 2: Allocate 2/64 of the total bandwidth ... 63: Allocate 63/64 of the total bandwidth

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10203140 EMI_ARBI Filter Priority Encode 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	URGENT_2ND				LLAT				URGENT				MISS			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIT				LIMIT				AGE				ULTRA			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	URGENT_2ND	**2nd urgent priority code** The waiting time for the command is going to expire. Bigger number means higher priority. This number must be smaller than the older age code. 0: The lowest priority

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Bit(s)	Name	Description
		1: Priority higher than 0 ... 15: The highest priority
27:24	LLAT	**Low latency request priority code** This means one command has the longest time delay with the previous page miss command among all command candidates. Bigger number means higher priority. This number must be smaller than the older age code. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority
23:20	URGENT	**Urgent priority code** The waiting time for the command is going to expire. Larger number means higher priority. This number must be smaller than the older age code. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority
19:16	MISS	**No page miss with previous commands priority code** This means the page miss overhead can be hidden by the data cycles. Bigger number means higher priority. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority
15:12	HIT	**Page hit priority code** Bigger number means higher priority. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority
11:8	LIMIT	**No bandwidth limit priority code** The master does not consume its requested bandwidth. Bigger number means higher priority. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority
7:4	AGE	**Order age priority code** The waiting time for the command is expired. Bigger number means higher priority. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority
3:0	ULTRA	**Ultra high priority code** Bigger number means higher priority. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority

10203144 **EMI_ARBI_2ND** **Filter Priority Encode for MD Requirement** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	URGENT_2ND				LLAT				URGENT				MISS			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIT				LIMIT				AGE				ULTRA			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	URGENT_2ND	**2nd urgent priority code** The waiting time for the command is going to expire. Bigger number means higher priority. This number must be smaller than the older age code. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority
27:24	LLAT	**Low latency request priority code** This means one command has the longest time delay with the previous page miss command among all command candidates. Bigger number means higher priority. This number must be smaller than the older age code. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority
23:20	URGENT	**Urgent priority code** The waiting time for the command is going to expire. Larger number means higher priority. This number must be smaller than the older age code. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority
19:16	MISS	**No page miss with previous commands priority code** This means the page miss overhead can be hidden by the data cycles. Bigger number means higher priority. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority
15:12	HIT	**Page hit priority code** Bigger number means higher priority. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority
11:8	LIMIT	**No bandwidth limit priority code** The master does not consume its requested bandwidth. Bigger number means higher priority. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority
7:4	AGE	**Order age priority code** The waiting time for the command is expired. Bigger number means higher priority. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority
3:0	ULTRA	**Ultra high priority code**

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Bit(s)	Name	Description
		Bigger number means higher priority. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority

10203148 **<u>EMI_ARBJ</u>** **Turn Around Command Number** **00684848**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RD_ULTRA_RDCNT_MIN**				**WR_ULTRA_WRCNT_MIN**				**POST_WR_CNT**				**WR_DLY_CYC**			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RDCNT_MIN**				**RDCNT**				**WRCNT_MIN**				**WRCNT**			
Type	RW				RW				RW				RW			
Reset	0	1	0	0	1	0	0	0	0	1	0	0	1	0	0	0

Bit(s)	Name	Description
31:28	RD_ULTRA_RDCNT_MIN	**Issues read command numbers and changes to write commands when having urgent write command and urgent read command** 0: 4 read commands 1: 8 read commands ... 15: Does not change to write command
27:24	WR_ULTRA_WRCNT_MIN	**Issues write command numbers and changes to read commands when having urgent read command and urgent write command** 0: 2 write commands 1: 4 write commands ... 15: Does not change to read command
23:20	POST_WR_CNT	**Switches servicing read command to write command when there is n write commands and no read commands (combined with WR_DLY_CYC)** 0: 1 pending write command ... 15: 16 pending write commands
19:16	WR_DLY_CYC	**Delayed cycle number to issue write command when there is no pending read commands** 0: 1 cycle ... 15: 16 cycles
15:12	RDCNT_MIN	**Issues read command numbers and changes to write commands when having urgent write command** 0: 1 read command 1: 2 read commands ... 15: Does not change to write command
11:8	RDCNT	**Issues read command numbers and changes to write commands** 0: 4 read commands 1: 8 read commands ... 15: Does not change to write command
7:4	WRCNT_MIN	**Issues write command numbers and changes to read commands when having urgent read command** 0: 1 write command

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Bit(s)	Name	Description
		1: 2 write commands ... 15: Does not change to read command
3:0	WRCNT	**Issues write command numbers and changes to read commands** 0: 2 write commands 1: 4 write commands ... 15: Does not change to read command

1020314C **EMI_ARBJ_2ND** **Turn Around Command Number for MD Requirement** **00684848**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RD_ULTRA_RDCNT_MIN				WR_ULTRA_WRCNT_MIN				POST_WR_CNT				WR_DLY_CYC			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDCNT_MIN				RDCNT				WRCNT_MIN				WRCNT			
Type	RW				RW				RW				RW			
Reset	0	1	0	0	1	0	0	0	0	1	0	0	1	0	0	0

Bit(s)	Name	Description
31:28	RD_ULTRA_RDCNT_MIN	**Issues read command numbers and changes to write commands when having urgent write command and urgent read command** 0: 4 read commands 1: 8 read commands ... 15: Does not change to write command
27:24	WR_ULTRA_WRCNT_MIN	**Issues write command numbers and changes to read commands when having urgent read command and urgent write command** 0: 2 write command 1: 4 write commands ... 15: Does not change to read command
23:20	POST_WR_CNT	**Switches servicing read command to write command when there is n write commands and no read commands (combined with WR_DLY_CYC)** 0: 1 pending write command ... 15: 16 pending write commands
19:16	WR_DLY_CYC	**Delayed cycle number to issue write command when there is no pending read commands** 0: 1 cycle ... 15: 16 cycles
15:12	RDCNT_MIN	**Issues read command numbers and changes to write commands when having urgent write command** 0: 1 read command 1: 2 read commands ... 15: Does not change to write command
11:8	RDCNT	**Issues read command numbers and changes to write commands** 0: 4 read command 1: 8 read commands ...

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Bit(s)	Name	Description
		15: Does not change to write command
7:4	WRCNT_MIN	**Issues write command numbers and changes to read commands when having urgent read command** 0: 1 write commands 1: 2 write commands ... 15: Does not change to read command
3:0	WRCNT	**Issues write command numbers and changes to read commands** 0: 2 write command 1: 4 write commands ... 15: Does not change to read command

10203150 EMI_ARBK Channel Arbiter Control 64003C7C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MULTI_CONF_BAN_PRO_NUM				RD_BAN_PRO_NUM				URGENT_CYC_2ND				URGENT_CYC_1St			
Type	RW				RW				RW				RW			
Reset	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			MULTI_CONF_BAN_PRO	RD_BAN_PRO	PAGE_MISS_DLY_CYC				WR_SERV_CNT_MAX				RD_SERV_CNT_MAX			
Type			RW	RW	RW				RW				RW			
Reset			1	1	1	1	0	0	0	1	1	1	1	1	0	0

Bit(s)	Name	Description
31:28	MULTI_CONF_BAN_PRO_NUM	**When row conflict command is larger than MULTI_CONF_BAN_PRO_NUM, EMI will inform DRAMC to promote this bank.**
27:24	RD_BAN_PRO_NUM	**When critical latency bank command is larger than RD_BAN_PRO_NUM, EMI will inform DRAMC to promote this bank.**
23:20	URGENT_CYC_2ND	**Second level urgent active when the acceptable latency is less than specified cycles.** 0: 31 cycles. ... 15: 511 cycles.
19:16	URGENT_CYC_1St	**First level urgent active when the acceptable latency is less than specified cycles.** 0: 31 cycles. ... 15: 511 cycles.
13	MULTI_CONF_BAN_PRO	**When row conflict command is larger than MULTI_CONF_BAN_PRO, EMI will inform DRAMC to promote this bank.** 1: Enable 0: Disable
12	RD_BAN_PRO	**When critical latency bank command is larger than RD_BAN_PRO, EMI will inform DRAMC to promote this bank.** 1: Enable 0: Disable

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Bit(s)	Name	Description
11:8	PAGE_MISS_DLY_CYC	**Delays command request n cycles to channel arbiter when the command is page miss with previous grant command** 0: Delay 5 cycles ... 15: Delay 20 cycles
7:4	WR_SERV_CNT_MAX	**Read request will be masked in some conditions. However, when write issue is over WR_SERV_CNT_MAXx2, read mask will be disabled.**
3:0	RD_SERV_CNT_MAX	**Write request will be mask on some condition. However, when read issue is over RD_SERV_CNT_MAXx4, write mask will be disabled.**

10203154 **EMI_ARBK_2ND** **Channel Arbiter Control** **64003C7C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MULTI_CONF_BAN_PRO_NUM				RD_BAN_PRO_NUM				URGENT_CYC_2ND				URGENT_CYC_1St			
Type	RW				RW				RW				RW			
Reset	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			MULTI_CONF_BAN_PRO	RD_BAN_PRO	PAGE_MISS_DLY_CYC				WR_SERV_CNT_MAX				RD_SERV_CNT_MAX			
Type			RW	RW	RW				RW				RW			
Reset			1	1	1	1	0	0	0	1	1	1	1	1	0	0

Bit(s)	Name	Description
31:28	MULTI_CONF_BAN_PRO_NUM	**When row conflict command is larger than MULTI_CONF_BAN_PRO_NUM, EMI will inform DRAMC to promote this bank.**
27:24	RD_BAN_PRO_NUM	**When critical latency bank command is larger than RD_BAN_PRO_NUM, EMI will inform DRAMC to promote this bank.**
23:20	URGENT_CYC_2ND	**Second level urgent active when the acceptable latency is less than specified cycles.** 0: 31 cycles. ... 15: 511 cycles.
19:16	URGENT_CYC_1St	**When critical latency bank command is larger than RD_BAN_PRO, EMI will inform DRAMC to promote this bank.** 0: Disable 1: Enable
13	MULTI_CONF_BAN_PRO	**First level urgent active when the acceptable latency is less than specified cycles.** 0: 31 cycles ... 15: 511 cycles.
12	RD_BAN_PRO	**When row conflict command is larger than MULTI_CONF_BAN_PRO, EMI will inform DRAMC to promote this bank.** 0: Disable 1: Enable

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Bit(s)	Name	Description
11:8	PAGE_MISS_DLY_CYC	**Delays command request n cycles to channel arbiter when the command is page miss with previous grant command** 0: Delay 5 cycles ... 15: Delay 20 cycles
7:4	WR_SERV_CNT_MAX	**Read request will be masked in some condition. However, when write issue is over WR_SERV_CNT_MAXx2, read mask will be disabled.**
3:0	RD_SERV_CNT_MAX	**Write request will be mask on some condition. However, when read issue is over RD_SERV_CNT_MAXx4, write mask will be disabled.**

10203158 EMI_SLCT EMI Slave Control Registers 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	M7_HI_PRIO_IND_EN	M6_HI_PRIO_IND_EN	M5_HI_PRIO_IND_EN	M4_HI_PRIO_IND_EN	M3_HI_PRIO_IND_EN	M2_HI_PRIO_IND_EN	M1_HI_PRIO_IND_EN	M0_HI_PRIO_IND_EN	M7_LLAT_EN	M6_LLAT_EN	M5_LLAT_EN	M4_LLAT_EN	M3_LLAT_EN	M2_LLAT_EN	M1_LLAT_EN	M0_LLAT_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HI_PRIO_EN_M7	HI_PRIO_EN_M6	HI_PRIO_EN_M5	HI_PRIO_EN_M4	HI_PRIO_EN_M3	HI_PRIO_EN_M2	HI_PRIO_EN_M1	HI_PRIO_EN_M0								
Type	RW	RW	RW	RW	RW	RW	RW	RW								
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Name	Description
31	M7_HI_PRIO_IND_EN	**Enables read high priority indication to DRAMC feature(for real-time GPU)** 0: Does not support high priority indication feature 1: Support high priority indication feature
30	M6_HI_PRIO_IND_EN	**Enables read high priority indication to DRAMC feature(for normal GPU)** 0: Does not support high priority indication feature 1: Support high priority indication feature
29	M5_HI_PRIO_IND_EN	**Enables read high priority indication to DRAMC feature** 0: Does not support high priority indication feature 1: Support high priority indication feature
28	M4_HI_PRIO_IND_EN	**Enables read high priority indication to DRAMC feature** 0: Does not support high priority indication feature 1: Support high priority indication feature
27	M3_HI_PRIO_IND_EN	**Enables read high priority indication to DRAMC feature** 0: Does not support high priority indication feature 1: Support high priority indication feature
26	M2_HI_PRIO_IND_EN	**Enables read high priority indication to DRAMC feature** 0: Does not support high priority indication feature 1: Support high priority indication feature
25	M1_HI_PRIO_IND_EN	**Enables read high priority indication to DRAMC feature** For PERISYS input from M0/1.

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Bit(s)	Name	Description
		0: Does not support high priority indication feature 1: Support high priority indication feature
24	M0_HI_PRIO_IND_EN	**Enables read high priority indication to DRAMC feature** For APMCU input from M0/1. 0: Does not support high priority indication feature 1: Support high priority indication feature
23	M7_LLAT_EN	**Enables read low latency feature** For real-time GPU. 0: Does not support low latency feature 1: Support low latency feature
22	M6_LLAT_EN	**Enables read low latency feature** For normal GPU. 0: Does not support low latency feature 1: Support low latency feature
21	M5_LLAT_EN	**Enables read low latency feature** 0: Does not support low latency feature 1: Support low latency feature
20	M4_LLAT_EN	**Enables read low latency feature** 0: Does not support low latency feature 1: Support low latency feature
19	M3_LLAT_EN	**Enables read low latency feature** 0: Does not support low latency feature 1: Support low latency feature
18	M2_LLAT_EN	**Enables read low latency feature** 0: Does not support low latency feature 1: Support low latency feature
17	M1_LLAT_EN	**Enables read low latency feature** For PERISYS input from M0/1. 0: Does not support low latency feature 1: Support low latency feature
16	M0_LLAT_EN	**Enables read low latency feature** For APMCU input from M0/1. 0: Does not support low latency feature 1: Support low latency feature
15	HI_PRIO_EN_M7	**Enables high priority feature** 0: Does not support high priority feature 1: Support high priority feature
14	HI_PRIO_EN_M6	**Enables high priority feature** 0: Does not support high priority feature 1: Support high priority feature
13	HI_PRIO_EN_M5	**Enables high priority feature** 0: Does not support high priority feature 1: Support high priority feature
12	HI_PRIO_EN_M4	**Enables high priority feature** 0: Does not support high priority feature 1: Support high priority feature
11	HI_PRIO_EN_M3	**Enables high priority feature** 0: Does not support high priority feature 1: Support high priority feature.
10	HI_PRIO_EN_M2	**Enables high priority feature** 0: Does not support high priority feature 1: Support high priority feature.
9	HI_PRIO_EN_M1	**Enables high priority feature**

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Bit(s)	Name	Description
		0: Does not support high priority feature 1: Support high priority feature.
8	HI_PRIO_EN_M0	**Enables high priority feature** 0: Does not support high priority feature 1: Support high priority feature.

10203160 **EMI_MPUA** **Memory Protection Unit Control Registers A** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_0	Memory protection Region 0 start address addr[31:16]
15:0	MPU_STOP_ADDR_0	Memory protection Region 0 stop address addr[31:16]

10203168 **EMI_MPUB** **Memory Protection Unit Control Registers B** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_1	Memory protection Region 1 start address addr[31:16]
15:0	MPU_STOP_ADDR_1	Memory protection Region 1 stop address addr[31:16]

10203170 **EMI_MPUC** **Memory Protection Unit Control Registers C** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:16	MPU_START_ADDR_2	Memory protection Region 2 start address addr[31:16]
15:0	MPU_STOP_ADDR_2	Memory protection Region 2 stop address addr[31:16]

10203178 EMI_MPUD Memory Protection Unit Control Registers D 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_3	Memory protection Region 3 start address addr[31:16]
15:0	MPU_STOP_ADDR_3	Memory protection Region 3 stop address addr[31:16]

10203180 EMI_MPUE Memory Protection Unit Control Registers E 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_4	Memory protection Region 4 start address addr[31:16]
15:0	MPU_STOP_ADDR_4	Memory protection Region 4 stop address addr[31:16]

10203188 EMI_MPUF Memory Protection Unit Control Registers F 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:16	MPU_START_ADDR_5	Memory protection Region 5 start address addr[31:16]
15:0	MPU_STOP_ADDR_5	Memory protection Region 5 stop address addr[31:16]

10203190 **EMI_MPUG** **Memory Protection Unit Control Registers G** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_6	Memory protection Region 6 start address addr[31:16]
15:0	MPU_STOP_ADDR_6	Memory protection Region 6 stop address addr[31:16]

10203198 **EMI_MPUH** **Memory Protection Unit Control Registers H** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_7	Memory protection Region 7 start address addr[31:16]
15:0	MPU_STOP_ADDR_7	Memory protection Region 7 stop address addr[31:16]

102031A0 **EMI_MPUI** **Memory Protection Unit Control Registers I** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R1_LOCK				R1D3_APC			R1D2_APC			R1D1_APC			R1D0_APC		
Type	RW				RW			RW			RW			RW		
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R0_LOC				R0D3_APC			R0D2_APC			R0D1_APC			R0D0_APC		

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	K															
Type	RW				RW			RW			RW			RW		
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R1_LOCK	**Controls Region 1 configuration lock** 0: No lock 1: Region 1 & Region 1 control register are unchangeable.
27:25	R1D3_APC	**Same as R0D0_APC**
24:22	R1D2_APC	**Same as R0D0_APC**
21:19	R1D1_APC	**Same as R0D0_APC**
18:16	R1D0_APC	**Same as R0D0_APC**
15	R0_LOCK	**Controls Region 0 configuration lock** 0: No lock 1: Region 0 & Region 0 control register are unchangeable.
11:9	R0D3_APC	**Same as R0D0_APC**
8:6	R0D2_APC	**Same as R0D0_APC**
5:3	R0D1_APC	**Same as R0D0_APC**
2:0	R0D0_APC	**000: No protection** 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden 110: Only security write is forbidden

102031A4 **EMI_MPUI_2ND** **Memory Protection Unit Control Registers I** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**R1D7_APC**			**R1D6_APC**			**R1D5_APC**			**R1D4_APC**		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**R0D7_APC**			**R0D6_APC**			**R0D5_APC**			**R0D4_APC**		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:25	R1D7_APC	**Same as R0D0_APC**
24:22	R1D6_APC	**Same as R0D0_APC**
21:19	R1D5_APC	**Same as R0D0_APC**
18:16	R1D4_APC	**Same as R0D0_APC**
11:9	R0D7_APC	**Same as R0D0_APC**
8:6	R0D6_APC	**Same as R0D0_APC**
5:3	R0D5_APC	**Same as R0D0_APC**
2:0	R0D4_APC	**000: No protection** 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden

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Bit(s)	Name	Description
		110: Only security write is forbidden

102031A8 EMI_MPUJ Memory Protection Unit Control Registers J 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R3_LOCK				R3D3_APC			R3D2_APC			R3D1_APC			R3D0_APC		
Type	RW				RW			RW			RW			RW		
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R2_LOCK				R2D3_APC			R2D2_APC			R2D1_APC			R2D0_APC		
Type	RW				RW			RW			RW			RW		
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R3_LOCK	**Controls Region 3 configuration lock** 0: No lock 1: Region 3 & Region 3 control register are unchangeable.
27:25	R3D3_APC	**Same as R2D0_APC**
24:22	R3D2_APC	**Same as R2D0_APC**
21:19	R3D1_APC	**Same as R2D0_APC**
18:16	R3D0_APC	**Same as R2D0_APC**
15	R2_LOCK	**Controls Region 2 configuration lock** 0: No lock 1: Region 2 & Region 2 control register are unchangeable.
11:9	R2D3_APC	**Same as R2D0_APC**
8:6	R2D2_APC	**Same as R2D0_APC**
5:3	R2D1_APC	**Same as R2D0_APC**
2:0	R2D0_APC	**000: No protection** 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden

102031AC EMI_MPUJ_2ND Memory Protection Unit Control Registers J 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					R3D7_APC			R3D6_APC			R3D5_APC			R3D4_APC		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					R2D7_APC			R2D6_APC			R2D5_APC			R2D4_APC		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
27:25	R3D7_APC	**Same as R2D0_APC**
24:22	R3D6_APC	**Same as R2D0_APC**
21:19	R3D5_APC	**Same as R2D0_APC**
18:16	R3D4_APC	**Same as R2D0_APC**
11:9	R2D7_APC	**Same as R2D0_APC**
8:6	R2D6_APC	**Same as R2D0_APC**
5:3	R2D5_APC	**Same as R2D0_APC**
2:0	R2D4_APC	**000: No protection** 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden

102031B0 **EMI_MPUK** **Memory Protection Unit Control Registers K** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R5_LOCK				R5D3_APC			R5D2_APC			R5D1_APC			R5D0_APC		
Type	RW				RW			RW			RW			RW		
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R4_LOCK				R4D3_APC			R4D2_APC			R4D1_APC			R4D0_APC		
Type	RW				RW			RW			RW			RW		
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R5_LOCK	**Controls Region 5 configuration lock** 0: No lock 1: Region 5 & Region 5 control register are unchangeable.
27:25	R5D3_APC	**Same as R4D0_APC**
24:22	R5D2_APC	**Same as R4D0_APC**
21:19	R5D1_APC	**Same as R4D0_APC**
18:16	R5D0_APC	**Same as R4D0_APC**
15	R4_LOCK	**Controls Region 4 configuration lock** 0: No lock 1: Region 4 & Region 4 control register are unchangeable.
11:9	R4D3_APC	**Same as R4D0_APC**
8:6	R4D2_APC	**Same as R4D0_APC**
5:3	R4D1_APC	**Same as R4D0_APC**
2:0	R4D0_APC	**000: No protection** 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden

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102031B4 EMI_MPUK_2ND Memory Protection Unit Control Registers K 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					R5D7_APC			R5D6_APC			R5D5_APC			R5D4_APC		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					R4D7_APC			R4D6_APC			R4D5_APC			R4D4_APC		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:25	R5D7_APC	**Same as R4D0_APC**
24:22	R5D6_APC	**Same as R4D0_APC**
21:19	R5D5_APC	**Same as R4D0_APC**
18:16	R5D4_APC	**Same as R4D0_APC**
11:9	R4D7_APC	**Same as R4D0_APC**
8:6	R4D6_APC	**Same as R4D0_APC**
5:3	R4D5_APC	**Same as R4D0_APC**
2:0	R4D4_APC	**000: No protection** 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden

102031B8 EMI_MPUL Memory Protection Unit Control Registers L 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R7_LOCK				R7D3_APC			R7D2_APC			R7D1_APC			R7D0_APC		
Type	RW				RW			RW			RW			RW		
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R6_LOCK				R6D3_APC			R6D2_APC			R6D1_APC			R6D0_APC		
Type	RW				RW			RW			RW			RW		
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R7_LOCK	**Controls Region 7 configuration lock** 0: No lock 1: Region 7 & Region 7 control register are unchangeable. *Note: All region registers (EMI_MPUA~EMI_MPUH) and region violation control registers (EMI_MPUI~EMI_MPUL) are allowed to be access in the secure mode only when D0_SEC = 1 or D1_SEC = 1 or D2_SEC = 1.*
27:25	R7D3_APC	**Same as R6D0_APC**
24:22	R7D2_APC	**Same as R6D0_APC**

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Bit(s)	Name	Description
21:19	R7D1_APC	**Same as R6D0_APC**
18:16	R7D0_APC	**Same as R6D0_APC**
15	R6_LOCK	**Controls Region 6 configuration lock** 0: No lock 1: Region 6 & Region 6 control register are unchangeable.
11:9	R6D3_APC	**Same as R6D0_APC**
8:6	R6D2_APC	**Same as R6D0_APC**
5:3	R6D1_APC	**Same as R6D0_APC**
2:0	R6D0_APC	**000: No protection** 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden

102031BC **EMI_MPUL_2ND** **Memory Protection Unit Control Registers L** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**R7D7_APC**			**R7D6_APC**			**R7D5_APC**			**R7D4_APC**		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**R6D7_APC**			**R6D6_APC**			**R6D5_APC**			**R6D4_APC**		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:25	R7D7_APC	**Same as R6D0_APC**
24:22	R7D6_APC	**Same as R6D0_APC**
21:19	R7D5_APC	**Same as R6D0_APC**
18:16	R7D4_APC	**Same as R6D0_APC**
11:9	R6D7_APC	**Same as R6D0_APC**
8:6	R6D6_APC	**Same as R6D0_APC**
5:3	R6D5_APC	**Same as R6D0_APC**
2:0	R6D4_APC	**000: No protection** 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden

102031C0 **EMI_MPUM** **Memory Protection Unit Control Registers M** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**D0_LOCK**	**D0_SEC**		**D0_REP**					**D0_MASK_HI**							

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Type	RW	RW		RW					RW							
Reset	0	0		0					0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**D0_OOR_MASK**	**APB_VIO_MASK0**	**D0_MASK**							
Type							RW	RW	RW							
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	D0_LOCK	**Controls domain 0 violation control register lock access** 0: No lock 1: D0_mask[7:0], D0_SEC, D0_LOCK are not changeable.
30	D0_SEC	**Controls domain 0 violation control register secure access** 0: Domain 0 violation control register can be accessed in secure/non-secure mode. 1: Domain 0 violation control register can be accessed in secure mode only. Domain 0 violation control register include EMI_MPUA~EMI_MPUL, EMI_MPUM, EMI_MPUP, EMI_MPUS, EMI_MPUT
28	D0_REP	**Controls Domain 0 violation response** 0: AXI response OKAY when violation 1: AXI response SLVERR when violation
23:16	D0_MASK_HI	**Masks Domain 0 region violation** 0000_0001: Set to 1 to mask Region 8 violation to Domain 0 0000_0010: Set to 1 to mask Region 9 violation to Domain 0 0000_0100: Set to 1 to mask Region 10 violation to Domain 0 0000_1000: Set to 1 to mask Region 11 violation to Domain 0 0001_0000: Set to 1 to mask Region 12 violation to Domain 0 0010_0000: Set to 1 to mask Region 13 violation to Domain 0 0100_0000: Set to 1 to mask Region 14 violation to Domain 0 1000_0000: Set to 1 to mask Region 15 violation to Domain 0
9	D0_OOR_MASK	**Masks Domain 0 out of range** 0: Disable mask 1: Enable mask
8	APB_VIO_MASK0	**Masks Domain 0 APB**
7:0	D0_MASK	**Masks Domain 0 region violation** 0000_0001: Set to 1 to mask Region 0 violation to Domain 0 0000_0010: Set to 1 to mask Region 1 violation to Domain 0 0000_0100: Set to 1 to mask Region 2 violation to Domain 0 0000_1000: Set to 1 to mask Region 3 violation to Domain 0 0001_0000: Set to 1 to mask Region 4 violation to Domain 0 0010_0000: Set to 1 to mask Region 5 violation to Domain 0 0100_0000: Set to 1 to mask Region 6 violation to Domain 0 1000_0000: Set to 1 to mask Region 7 violation to Domain 0

102031C8 **EMI_MPUN** **Memory Protection Unit Control Registers N** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**D1_LOCK**	**D1_SEC**		**D1_REP**					**D1_MASK_HI**							
Type	RW	RW		RW					RW							
Reset	0	0		0					0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**D1_**	**APB**	**D1_MASK**							

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							OOR_MASK	_VIO_MASK1								
Type							RW	RW	RW							
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	D1_LOCK	**Controls Domain 1 violation control register lock access** 0: No lock 1: D1_mask[7:0], D1_SEC, D1_LOCK are not changeable.
30	D1_SEC	**Controls domain 1 violation control register secure access** 0: Domain 1 violation control register can be accessed in both secure/non-secure mode. 1: Domain 1 violation control register can be accessed in secure mode only. Domain 1 violation control register include EMI_MPUA~EMI_MPUL, EMI_MPUN, EMI_MPUQ, EMI_MPUS, EMI_MPUT
28	D1_REP	**Controls Domain 1 violation response** 0: AXI response OKAY when violation 1: AXI response SLVERR when violation
23:16	D1_MASK_HI	**Masks Domain 1 region violation** 0000_0001: Set to 1 to mask Region 8 violation to Domain 1 0000_0010: Set to 1 to mask Region 9 violation to Domain 1 0000_0100: Set to 1 to mask Region 10 violation to Domain 1 0000_1000: Set to 1 to mask Region 11 violation to Domain 1 0001_0000: Set to 1 to mask Region 12 violation to Domain 1 0010_0000: Set to 1 to mask Region 13 violation to Domain 1 0100_0000: Set to 1 to mask Region 14 violation to Domain 1 1000_0000: Set to 1 to mask Region 15 violation to Domain 1
9	D1_OOR_MASK	**Masks Domain 1 out of range** 0: Disable mask 1: Enable mask
8	APB_VIO_MASK1	**Masks Domain 1 APB**
7:0	D1_MASK	**Masks Domain 1 region violation** 0000_0001: Set to 1 to mask Region 0 violation to Domain 1 0000_0010: Set to 1 to mask Region 1 violation to Domain 1 0000_0100: Set to 1 to mask Region 2 violation to Domain 1 0000_1000: Set to 1 to mask Region 3 violation to Domain 1 0001_0000: Set to 1 to mask Region 4 violation to Domain 1 0010_0000: Set to 1 to mask Region 5 violation to Domain 1 0100_0000: Set to 1 to mask Region 6 violation to Domain 1 1000_0000: Set to 1 to mask Region 7 violation to Domain 1

102031D0 **EMI_MPUO** **Memory Protection Unit Control Registers O** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**D2_LOCK**	**D2_SEC**		**D2_REP**					**D2_MASK_HI**							
Type	RW	RW		RW					RW							
Reset	0	0		0					0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**D2_OOR_MASK**	**APB_VIO_MASK2**	**D2_MASK**							

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Type							RW	RW	RW							
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	D2_LOCK	**Controls Domain 2 violation control register lock access** 0: No lock 1: D2_mask[7:0], D2_SEC, D2_LOCK are not changeable.
30	D2_SEC	**Controls domain 2 violation control register secure access** 0: Domain 2 violation control register can be accessed in both secure/non-secure mode. 1: Domain 2 violation control register can be accessed in secure mode only. Domain 2 violation control register include EMI_MPUA~EMI_MPUL, EMI_MPUO, EMI_MPUR, EMI_MPUS, EMI_MPUT
28	D2_REP	**Controls Domain 2 violation response** 0: AXI response OKAY when violation 1: AXI response SLVERR when violation
23:16	D2_MASK_HI	**Masks Domain 2 region violation** 0000_0001: Set to 1 to mask Region 8 violation to Domain 2 0000_0010: Set to 1 to mask Region 9 violation to Domain 2 0000_0100: Set to 1 to mask Region 10 violation to Domain 2 0000_1000: Set to 1 to mask Region 11 violation to Domain 2 0001_0000: Set to 1 to mask Region 12 violation to Domain 2 0010_0000: Set to 1 to mask Region 13 violation to Domain 2 0100_0000: Set to 1 to mask Region 14 violation to Domain 2 1000_0000: Set to 1 to mask Region 15 violation to Domain 2
9	D2_OOR_MASK	**Masks Domain 2 out of range** 0: Disable mask 1: Enable mask
8	APB_VIO_MASK2	**Masks Domain 2 APB**
7:0	D2_MASK	**Masks Domain 2 region violation** 0000_0001: Set to 1 to mask Region 0 violation to Domain 2 0000_0010: Set to 1 to mask Region 1 violation to Domain 2 0000_0100: Set to 1 to mask Region 2 violation to Domain 2 0000_1000: Set to 1 to mask Region 3 violation to Domain 2 0001_0000: Set to 1 to mask Region 4 violation to Domain 2 0010_0000: Set to 1 to mask Region 5 violation to Domain 2 0100_0000: Set to 1 to mask Region 6 violation to Domain 2 1000_0000: Set to 1 to mask Region 7 violation to Domain 2

102031D8 EMI_MPUP Memory Protection Unit Control Registers P 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									R15_VIO	R14_VIO	R13_VIO	R12_VIO	R11_VIO	R10_VIO	R9_VIO	R8_VIO
Type									W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							OOR_VIO	APB_VIO	R7_VIO	R6_VIO	R5_VIO	R4_VIO	R3_VIO	R2_VIO	R1_VIO	R0_VIO
Type							W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23	R15_VIO	**Region 15 abort violation status to Domain 0**

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Bit(s)	Name	Description
		0: No Region 7 abort violation 1: Region 7 abort violation
22	R14_VIO	**Region 14 abort violation status to Domain 0** 0: No Region 6 abort violation 1: Region 6 abort violation
21	R13_VIO	**Region 13 abort violation status to Domain 0** 0: No Region 5 abort violation 1: Region 5 abort violation
20	R12_VIO	**Region 12 abort violation status to Domain 0** 0: No Region 4 abort violation 1: Region 4 abort violation
19	R11_VIO	**Region 11 abort violation status to Domain 0** 0: No Region 3 abort violation 1: Region 3 abort violation
18	R10_VIO	**Region 10 abort violation status to Domain 0** 0: No Region 2 abort violation 1: Region 2 abort violation
17	R9_VIO	**Region 9 abort violation status to Domain 0** 0: No Region 1 abort violation 1: Region 1 abort violation
16	R8_VIO	**Region 8 abort violation status to Domain 0** EMI will first record the unmask device abort information at EMI_MPUS and EMI_MPUT if unmasking and set up the corresponding R0_VIO status bit. Clear R0_VIO for EMI to record the next violation status. When multiple violations occur, the corresponding D0_VIO_STA status bit will be set. However, only the device abort information will be recorded at VIO_DBGx, and its content will not be changed until the software clears it. 0: No Region 0 abort violation 1: Region 0 abort violation
9	OOR_VIO	**Out of range abort violation status to Domain 0** 0: No out of range abort violation 1: Out of range abort violation
8	APB_VIO	**APB abort violation status to Domain 0** 0: No APB abort violation 1: APB abort violation *Note: EMI_MPUP is allowed to be accessed in the secure mode only when D0_SEC = 1.*
7	R7_VIO	**Region 7 abort violation status to Domain 0** 0: No Region 7 abort violation 1: Region 7 abort violation
6	R6_VIO	**Region 6 abort violation status to Domain 0** 0: No Region 6 abort violation 1: Region 6 abort violation
5	R5_VIO	**Region 5 abort violation status to Domain 0** 0: No Region 5 abort violation 1: Region 5 abort violation
4	R4_VIO	**Region 4 abort violation status to Domain 0** 0: No Region 4 abort violation 1: Region 4 abort violation
3	R3_VIO	**Region 3 abort violation status to Domain 0** 0: No Region 3 abort violation 1: Region 3 abort violation
2	R2_VIO	**Region 2 abort violation status to Domain 0** 0: No Region 2 abort violation

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Bit(s)	Name	Description
		1: Region 2 abort violation
1	R1_VIO	**Region 1 abort violation status to Domain 0** 0: No Region 1 abort violation 1: Region 1 abort violation
0	R0_VIO	**Region 0 abort violation status to Domain 0** EMI will first record first the unmask device abort information at EMI_MPUS and EMI_MPUT if unmasking and set up the corresponding R0_VIO status bit. Clear R0_VIO for EMI to record the next violation status. When multiple violations occur, the corresponding D0_VIO_STA status bit will be set. However, only the device abort information will be recorded at VIO_DBGx, and its content will not be changed until the software clears it. 0: No Region 0 abort violation 1: Region 0 abort violation

102031E0 **EMI_MPUQ** **Memory Protection Unit Control Registers Q** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									R15_VIO	R14_VIO	R13_VIO	R12_VIO	R11_VIO	R10_VIO	R9_VIO	R8_VIO
Type									W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							OOR_VIO	APB_VIO	R7_VIO	R6_VIO	R5_VIO	R4_VIO	R3_VIO	R2_VIO	R1_VIO	R0_VIO
Type							W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23	R15_VIO	**Region 15 abort violation status to Domain 1** 0: No Region 7 abort violation 1: Region 7 abort violation
22	R14_VIO	**Region 14 abort violation status to Domain 1** 0: No Region 6 abort violation 1: Region 6 abort violation
21	R13_VIO	**Region 13 abort violation status to Domain 1** 0: No Region 5 abort violation 1: Region 5 abort violation
20	R12_VIO	**Region 12 abort violation status to Domain 1** 0: No Region 4 abort violation 1: Region 4 abort violation
19	R11_VIO	**Region 11 abort violation status to Domain 1** 0: No Region 3 abort violation 1: Region 3 abort violation
18	R10_VIO	**Region 10 abort violation status to Domain 1** 0: No Region 2 abort violation 1: Region 2 abort violation
17	R9_VIO	**Region 9 abort violation status to Domain 1** 0: No Region 1 abort violation 1: Region 1 abort violation
16	R8_VIO	**Region 8 abort violation status to Domain 1** EMI will first record the unmask device abort information at EMI_MPUS and

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Bit(s)	Name	Description
		EMI_MPUT if unmasking and set up the corresponding R0_VIO status bit. Clear R0_VIO for EMI to record the next violation status. When multiple violations occur, the corresponding D0_VIO_STA status bit will be set. However, only the device abort information will be recorded at VIO_DBGx, and its content will not be changed until the software clears it. 0: No Region 0 abort violation 1: Region 0 abort violation
9	OOR_VIO	**Out of range abort violation status to Domain 1** 0: No out of range abort violation 1: Out of range abort violation
8	APB_VIO	**APB abort violation status to Domain 1** 0: No APB abort violation 1: APB abort violation *Note: EMI_MPUQ is allowed to be accessed in the secure mode only when D1_SEC = 1.*
7	R7_VIO	**Region 7 abort violation status to Domain 1** 0: No Region 7 abort violation 1: Region 7 abort violation
6	R6_VIO	**Region 6 abort violation status to Domain 1** 0: No Region 6 abort violation 1: Region 6 abort violation
5	R5_VIO	**Region 5 abort violation status to Domain 1** 0: No Region 5 abort violation 1: Region 5 abort violation
4	R4_VIO	**Region 4 abort violation status to Domain 1** 0: No Region 4 abort violation 1: Region 4 abort violation
3	R3_VIO	**Region 3 abort violation status to Domain 1** 0: No Region 3 abort violation 1: Region 3 abort violation
2	R2_VIO	**Region 2 abort violation status to Domain 1** 0: No Region 2 abort violation 1: Region 2 abort violation
1	R1_VIO	**Region 1 abort violation status to Domain 1** 0: No Region 1 abort violation 1: Region 1 abort violation
0	R0_VIO	**Region 0 abort violation status to Domain 1** 0: No Region 0 abort violation 1: Region 0 abort violation

102031E8 EMI_MPUR Memory Protection Unit Control Registers R 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									R15_VIO	R14_VIO	R13_VIO	R12_VIO	R11_VIO	R10_VIO	R9_VIO	R8_VIO
Type									W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset									0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							OOR_VIO	APB_VIO	R7_VIO	R6_VIO	R5_VIO	R4_VIO	R3_VIO	R2_VIO	R1_VIO	R0_VIO
Type							W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset							0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
23	R15_VIO	**Region 15 abort violation status to Domain 2** 0: No Region 7 abort violation 1: Region 7 abort violation
22	R14_VIO	**Region 14 abort violation status to Domain 2** 0: No Region 6 abort violation 1: Region 6 abort violation
21	R13_VIO	**Region 13 abort violation status to Domain 2** 0: No Region 5 abort violation 1: Region 5 abort violation
20	R12_VIO	**Region 12 abort violation status to Domain 2** 0: No Region 4 abort violation 1: Region 4 abort violation
19	R11_VIO	**Region 11 abort violation status to Domain 2** 0: No Region 3 abort violation 1: Region 3 abort violation
18	R10_VIO	**Region 10 abort violation status to Domain 2** 0: No Region 2 abort violation 1: Region 2 abort violation
17	R9_VIO	**Region 9 abort violation status to Domain 2** 0: No Region 1 abort violation 1: Region 1 abort violation
16	R8_VIO	**Region 8 abort violation status to Domain 2** EMI will first record the unmask device abort information at EMI_MPUS and EMI_MPUT if unmasking and set up the corresponding R0_VIO status bit. Clear R0_VIO for EMI to record the next violation status. When multiple violations occur, the corresponding D0_VIO_STA status bit will be set. However, only the device abort information will be recorded at VIO_DBGx, and its content will not be changed until the software clears it. 0: No Region 0 abort violation 1: Region 0 abort violation
9	OOR_VIO	**Out of range abort violation status to Domain 2** 0: No out of range abort violation 1: Out of range abort violation
8	APB_VIO	**APB abort violation status to Domain 2** 0: No APB abort violation 1: APB abort violation *Note: EMI_MPUR is allowed to be accessed in the secure mode only when D2_SEC = 1.*
7	R7_VIO	**Region 7 abort violation status to Domain 2** 0: No Region 7 abort violation 1: Region 7 abort violation
6	R6_VIO	**Region 6 abort violation status to Domain 2** 0: No Region 6 abort violation 1: Region 6 abort violation
5	R5_VIO	**Region 5 abort violation status to Domain 2** 0: No Region 5 abort violation 1: Region 5 abort violation
4	R4_VIO	**Region 4 abort violation status to Domain 2** 0: No Region 4 abort violation 1: Region 4 abort violation
3	R3_VIO	**Region 3 abort violation status to Domain 2** 0: No Region 3 abort violation 1: Region 3 abort violation

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Bit(s)	Name	Description
2	R2_VIO	**Region 2 abort violation status to domain 2** 0: No Region 2 abort violation 1: Region 2 abort violation
1	R1_VIO	**Region 1 abort violation status to domain 2** 0: No Region 1 abort violation 1: Region 1 abort violation
0	R0_VIO	**Region 0 abort violation status to domain 2** 0: No Region 0 abort violation 1: Region 0 abort violation

102031F0 EMI_MPUS Memory Protection Unit Control Registers S 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CLR		R_VIO	W_VIO			FIX_ABORT	APB_ABORT	DOMAIN_ID				REGION_ABORT			
Type	WO		RO	RO			RO	RO	RO				RO			
Reset	0		0	0			0	0	0	0	0		0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			MASTER_ID													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	CLR	**Clears debugging information** 0: No action 1: Clear debugging information
29	R_VIO	**Read violation** 0: Abort is not caused by a READ violation. 1: Abort is caused by a READ violation.
28	W_VIO	**Write violation** 0: Abort is not caused by a WRITE violation. 1: Abort is caused by a WRITE violation.
25	FIX_ABORT	**Indicates if fix transaction violation causes the abort** 0: Abort is not caused by a APB violation. 1: Abort is caused by a APB violation.
24	APB_ABORT	**Indicates if APB violation causes the abort** 0: Abort is not caused by a APB violation. 1: Abort is caused by a APB violation.
23:21	DOMAIN_ID	**Violation domain ID** 00: Domain 0 violation 01: Domain 1 violation 10: Domain 2 violation 11: Domain 3 violation 11: Reserved
19:16	REGION_ABORT	**Violated region** 0: Region 0 is violated. 1: Region 1 is violated. 2: Region 2 is violated. ... 15: Region 15 is violated.
13:0	MASTER_ID	**Records the violation master ID {AXI ID, Port ID}** AXI ID: 13 bits Port ID: 3 bits

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Bit(s)	Name	Description
		Bit115 at 0x1f0[27:26]

102031F8 EMI_MPUT Memory Protection Unit Control Registers T 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_ERROR_ADDR[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_ERROR_ADDR[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MPU_ERROR_ADDR	**Violation address** If the violation comes from APB, the violation address will record the register offset value. *Note: EMI_MPUS and EMI_MPUT are allowed to be cleared in the secure mode when D0_SEC = 1 or D1_SEC = 1 or D2_SEC = 1.*

10203200 EMI_MPUU Memory Protection Unit Control Registers U 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	D3_LOCK	D3_SEC		D3_REP					D3_MASK_HI							
Type	RW	RW		RW					RW							
Reset	0	0		0					0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							D3_OOR_MASK	APB_VIO_MASK3	D3_MASK							
Type							RW	RW	RW							
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	D3_LOCK	**Controls Domain 3 violation control register lock access** 0: No lock 1: D3_mask[7:0], D3_SEC, D3_LOCK are not changeable.
30	D3_SEC	**Controls Domain 3 violation control register secure access** 0: Domain 3 violation control register can be accessed in both secure/non-secure mode. 1: Domain 3 violation control register can be accessed in secure mode only. Domain 3 violation control register include EMI_MPUA~EMI_MPUL, EMI_MPUU, EMI_MPUV, EMI_MPUS, EMI_MPUT
28	D3_REP	**Controls Domain 3 violation response** 0: AXI response OKAY when violation 1: AXI response SLVERR when violation
23:16	D3_MASK_HI	**Masks Domain 3 region violation** 0000_0001: Set to 1 to mask Region 8 violation to Domain 3 0000_0010: Set to 1 to mask Region 9 violation to Domain 3

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Bit(s)	Name	Description
		0000_0100: Set to 1 to mask Region 10 violation to Domain 3 0000_1000: Set to 1 to mask Region 11 violation to Domain 3 0001_0000: Set to 1 to mask Region 12 violation to Domain 3 0010_0000: Set to 1 to mask Region 13 violation to Domain 3 0100_0000: Set to 1 to mask Region 14 violation to Domain 3 1000_0000: Set to 1 to mask Region 15 violation to Domain 3
9	D3_OOR_MASK	**Masks Domain 3 out of range** 0: Disable mask 1: Enable mask
8	APB_VIO_MASK3	**Masks Domain 3 APB**
7:0	D3_MASK	**Masks Domain 3 region violation** 0000_0001: Set to 1 to mask Region 0 violation to Domain 3 0000_0010: Set to 1 to mask Region 1 violation to Domain 3 0000_0100: Set to 1 to mask Region 2 violation to Domain 3 0000_1000: Set to 1 to mask Region 3 violation to Domain 3 0001_0000: Set to 1 to mask Region 4 violation to Domain 3 0010_0000: Set to 1 to mask Region 5 violation to Domain 3 0100_0000: Set to 1 to mask Region 6 violation to Domain 3 1000_0000: Set to 1 to mask Region 7 violation to Domain 3

10203220 EMI_MPUY Memory Protection Unit Control Registers Y 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									R15_VIO	R14_VIO	R13_VIO	R12_VIO	R11_VIO	R10_VIO	R9_VIO	R8_VIO
Type									W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							OOR_VIO	APB_VIO	R7_VIO	R6_VIO	R5_VIO	R4_VIO	R3_VIO	R2_VIO	R1_VIO	R0_VIO
Type							W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23	R15_VIO	**Region 15 abort violation status to Domain 3** 0: No Region 7 abort violation 1: Region 7 abort violation
22	R14_VIO	**Region 14 abort violation status to Domain 3** 0: No Region 6 abort violation 1: Region 6 abort violation
21	R13_VIO	**Region 13 abort violation status to Domain 3** 0: No Region 5 abort violation 1: Region 5 abort violation
20	R12_VIO	**Region 12 abort violation status to Domain 3** 0: No Region 4 abort violation 1: Region 4 abort violation
19	R11_VIO	**Region 11 abort violation status to Domain 3** 0: No Region 3 abort violation 1: Region 3 abort violation
18	R10_VIO	**Region 10 abort violation status to Domain 3** 0: No Region 2 abort violation 1: Region 2 abort violation

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Bit(s)	Name	Description
17	R9_VIO	**Region 9 abort violation status to Domain 3** 0: No Region 1 abort violation 1: Region 1 abort violation
16	R8_VIO	**Region 8 abort violation status to Domain 3** EMI will first record the unmask device abort information at EMI_MPUS and EMI_MPUT if unmasking and set up the corresponding R0_VIO status bit. Clear R0_VIO for EMI to record the next violation status. When multiple violations occur, the corresponding D0_VIO_STA status bit will be set. However, only the device abort information will be recorded at VIO_DBGx, and its content will not be changed until the software clears it. 0: No Region 0 abort violation 1: Region 0 abort violation
9	OOR_VIO	**Out of range abort violation status to Domain 3** 0: No out of range abort violation 1: Out of range abort violation
8	APB_VIO	**APB abort violation status to Domain 3** 0: No APB abort violation 1: APB abort violation Note: EMI_MPUR is allowed to be accessed in the secure mode only when D2_SEC = 1.
7	R7_VIO	**Region 7 abort violation status to Domain 3** 0: No Region 7 abort violation 1: Region 7 abort violation
6	R6_VIO	**Region 6 abort violation status to Domain 3** 0: No Region 6 abort violation 1: Region 6 abort violation
5	R5_VIO	**Region 5 abort violation status to Domain 3** 0: No Region 5 abort violation 1: Region 5 abort violation
4	R4_VIO	**Region 4 abort violation status to Domain 3** 0: No Region 4 abort violation 1: Region 4 abort violation
3	R3_VIO	**Region 3 abort violation status to Domain 3** 0: No Region 3 abort violation 1: Region 3 abort violation
2	R2_VIO	**Region 2 abort violation status to Domain 3** 0: No Region 2 abort violation 1: Region 2 abort violation
1	R1_VIO	**Region 1 abort violation status to Domain 3** 0: No Region 1 abort violation 1: Region 1 abort violation
0	R0_VIO	**Region 0 abort violation status to Domain 3** 0: No Region 0 abort violation 1: Region 0 abort violation

10203260 EMI_MPUA2 Memory Protection Unit Control Registers A 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_8															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_8															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_8	Memory protection Region 8 start address addr[31:16]
15:0	MPU_STOP_ADDR_8	Memory protection Region 8 stop address addr[31:16]

10203268 EMI_MPUB2 Memory Protection Unit Control Registers B 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MPU_START_ADDR_9**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MPU_STOP_ADDR_9**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_9	Memory protection Region 9 start address addr[31:16]
15:0	MPU_STOP_ADDR_9	Memory protection Region 9 stop address addr[31:16]

10203270 EMI_MPUC2 Memory Protection Unit Control Registers C 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MPU_START_ADDR_10**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MPU_STOP_ADDR_10**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_10	Memory protection Region 10 start address addr[31:16]
15:0	MPU_STOP_ADDR_10	Memory protection Region 10 stop address addr[31:16]

10203278 EMI_MPUD2 Memory Protection Unit Control Registers D 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MPU_START_ADDR_11**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MPU_STOP_ADDR_11**															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_11	Memory protection Region 11 start address addr[31:16]
15:0	MPU_STOP_ADDR_11	Memory protection Region 11 stop address addr[31:16]

10203280 EMI_MPUE2 Memory Protection Unit Control Registers E 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_12															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_12															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_12	Memory protection Region 12 start address addr[31:16]
15:0	MPU_STOP_ADDR_12	Memory protection Region 12 stop address addr[31:16]

10203288 EMI_MPUF2 Memory Protection Unit Control Registers F 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_13															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_13															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_13	Memory protection Region 13 start address addr[31:16]
15:0	MPU_STOP_ADDR_13	Memory protection Region 13 stop address addr[31:16]

10203290 EMI_MPUG2 Memory Protection Unit Control Registers G 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_14															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_14															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_14	Memory protection Region 14 start address addr[31:16]
15:0	MPU_STOP_ADDR_14	Memory protection Region 14 stop address addr[31:16]

10203298 EMI_MPUH2 Memory Protection Unit Control Registers H 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_15	Memory protection Region 15 start address addr[31:16]
15:0	MPU_STOP_ADDR_15	Memory protection Region 15 stop address addr[31:16]

102032A0 EMI_MPUI2 Memory Protection Unit Control Registers I 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R9_LOCK				R9D3_APC			R9D2_APC			R9D1_APC			R9D0_APC		
Type	RW				RW			RW			RW			RW		
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R8_LOCK				R8D3_APC			R8D2_APC			R8D1_APC			R8D0_APC		
Type	RW				RW			RW			RW			RW		
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R9_LOCK	**Controls Region 9 configuration lock** 0: No lock 1: Region 9 & Region 9 control register are unchangeable.
27:25	R9D3_APC	**Same as R8D0_APC**
24:22	R9D2_APC	**Same as R8D0_APC**
21:19	R9D1_APC	**Same as R8D0_APC**
18:16	R9D0_APC	**Same as R8D0_APC**
15	R8_LOCK	**Controls Region 8 configuration lock** 0: No lock 1: Region 8 & Region 8 control register are unchangeable.

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Bit(s)	Name	Description
11:9	R8D3_APC	**Same as R8D0_APC**
8:6	R8D2_APC	**Same as R8D0_APC**
5:3	R8D1_APC	**Same as R8D0_APC**
2:0	R8D0_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden 110: Only security write is forbidden

102032A4 **EMI_MPUI2_2ND** **Memory Protection Unit Control Registers I** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					R9D7_APC			R9D6_APC			R9D5_APC			R9D4_APC		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					R8D7_APC			R8D6_APC			R8D5_APC			R8D4_APC		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:25	R9D7_APC	Same as R8D0_APC
24:22	R9D6_APC	Same as R8D0_APC
21:19	R9D5_APC	Same as R8D0_APC
18:16	R9D4_APC	Same as R8D0_APC
11:9	R8D7_APC	Same as R8D0_APC
8:6	R8D6_APC	Same as R8D0_APC
5:3	R8D5_APC	Same as R8D0_APC
2:0	R8D4_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden 110: Only security write is forbidden

102032A8 **EMI_MPUJ2** **Memory Protection Unit Control Registers J** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R11_LOCK				R11D3_APC			R11D2_APC			R11D1_APC			R11D0_APC		
Type	RW				RW			RW			RW			RW		
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R10_LOCK				R10D3_APC			R10D2_APC			R10D1_APC			R10D0_APC		
Type	RW				RW			RW			RW			RW		
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31	R11_LOCK	**Controls Region 11 configuration lock** 0: No lock 1: Region 11 & Region 11 control register are unchangeable.
27:25	R11D3_APC	**Same as R10D0_APC**
24:22	R11D2_APC	**Same as R10D0_APC**
21:19	R11D1_APC	**Same as R10D0_APC**
18:16	R11D0_APC	**Same as R10D0_APC**
15	R10_LOCK	**Controls Region 10 configuration lock** 0: No lock 1: Region 10 & Region 10 control register are unchangeable.
11:9	R10D3_APC	**Same as R10D0_APC**
8:6	R10D2_APC	**Same as R10D0_APC**
5:3	R10D1_APC	**Same as R10D0_APC**
2:0	R10D0_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden

102032AC **EMI_MPUJ2_2ND** **Memory Protection Unit Control Registers J** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					R11D7_APC			R11D6_APC			R11D5_APC			R11D4_APC		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					R10D7_APC			R10D6_APC			R10D5_APC			R10D4_APC		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:25	R11D7_APC	Same as R10D0_APC
24:22	R11D6_APC	Same as R10D0_APC
21:19	R11D5_APC	Same as R10D0_APC
18:16	R11D4_APC	Same as R10D0_APC
11:9	R10D7_APC	Same as R10D0_APC
8:6	R10D6_APC	Same as R10D0_APC
5:3	R10D5_APC	Same as R10D0_APC
2:0	R10D4_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden

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102032B0	**EMI_MPUK 2**	**Memory Protection Unit Control Registers K**	**00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R13_LOCK				R13D3_APC			R13D2_APC			R13D1_APC			R13D0_APC		
Type	RW				RW			RW			RW			RW		
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R12_LOCK				R12D3_APC			R12D2_APC			R12D1_APC			R12D0_APC		
Type	RW				RW			RW			RW			RW		
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R13_LOCK	**Controls Region 13 configuration lock** 0: No lock 1: Region 13 & Region 13 control register are unchangeable.
27:25	R13D3_APC	**Same as R12D0_APC**
24:22	R13D2_APC	**Same as R12D0_APC**
21:19	R13D1_APC	**Same as R12D0_APC**
18:16	R13D0_APC	**Same as R12D0_APC**
15	R12_LOCK	**Controls Region 12 configuration lock** 0: No lock 1: Region 12 & Region 12 control register are unchangeable.
11:9	R12D3_APC	**Same as R12D0_APC**
8:6	R12D2_APC	**Same as R12D0_APC**
5:3	R12D1_APC	**Same as R12D0_APC**
2:0	R12D0_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden

102032B4	**EMI_MPUK 2_2ND**	**Memory Protection Unit Control Registers K**	**00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					R13D7_APC			R13D6_APC			R13D5_APC			R13D4_APC		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					R12D7_APC			R12D6_APC			R12D5_APC			R12D4_APC		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:25	R13D7_APC	Same as R12D0_APC
24:22	R13D6_APC	Same as R12D0_APC
21:19	R13D5_APC	Same as R12D0_APC

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Bit(s)	Name	Description
18:16	R13D4_APC	Same as R12D0_APC
11:9	R12D7_APC	Same as R12D0_APC
8:6	R12D6_APC	Same as R12D0_APC
5:3	R12D5_APC	Same as R12D0_APC
2:0	R12D4_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden

102032B8 EMI_MPUL2 Memory Protection Unit Control Registers L 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**R15_LOCK**				**R15D3_APC**			**R15D2_APC**			**R15D1_APC**			**R15D0_APC**		
Type	RW				RW			RW			RW			RW		
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**R14_LOCK**				**R14D3_APC**			**R14D2_APC**			**R14D1_APC**			**R14D0_APC**		
Type	RW				RW			RW			RW			RW		
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R15_LOCK	**Controls Region 15 configuration lock** 0: No lock 1: Region 15 & Region 15 control register are unchangeable. *Note: All region registers (EMI_MPUA2~EMI_MPUH) and region violation control registers (EMI_MPUI2~EMI_MPUL2) are allowed to be access in the secure mode only when D0_SEC = 1 or D1_SEC = 1 or D2_SEC = 1.*
27:25	R15D3_APC	**Same as R14D0_APC**
24:22	R15D2_APC	**Same as R14D0_APC**
21:19	R15D1_APC	**Same as R14D0_APC**
18:16	R15D0_APC	**Same as R14D0_APC**
15	R14_LOCK	**Controls Region 14 configuration lock** 0: No lock 1: Region 14 & Region 14 control register are unchangeable.
11:9	R14D3_APC	**Same as R14D0_APC**
8:6	R14D2_APC	**Same as R14D0_APC**
5:3	R14D1_APC	**Same as R14D0_APC**
2:0	R14D0_APC	**000: No protection** 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden

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102032BC **EMI_MPUL2_2ND** **Memory Protection Unit Control Registers L** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**R15D7_APC**			**R15D6_APC**			**R15D5_APC**			**R15D4_APC**		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**R14D7_APC**			**R14D6_APC**			**R14D5_APC**			**R14D4_APC**		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:25	R15D7_APC	Same as R14D0_APC
24:22	R15D6_APC	Same as R14D0_APC
21:19	R15D5_APC	Same as R14D0_APC
18:16	R15D4_APC	Same as R14D0_APC
11:9	R14D7_APC	Same as R14D0_APC
8:6	R14D6_APC	Same as R14D0_APC
5:3	R14D5_APC	Same as R14D0_APC
2:0	R14D4_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden

102032C0 **EMI_MPUM2** **Memory Protection Unit Control Registers M** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**D4_LOCK**	**D4_SEC**		**D4_REP**					**D4_MASK_HI**							
Type	RW	RW		RW					RW							
Reset	0	0		0					0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**D4_OOR_MASK**	**APB_VIO_MASK0**	**D4_MASK**							
Type							RW	RW	RW							
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	D4_LOCK	**Controls Domain 4 violation control register lock access** 0: No lock 1: D4_mask[7:0], D4_SEC, D4_LOCK are not changeable.
30	D4_SEC	**Controls Domain 4 violation control register secure access** 0: Domain 4 violation control register can be accessed in secure/non-secure mode. 1: Domain 4 violation control register can be accessed in secure mode only. Domain 4 violation control register include EMI_MPUA2~EMI_MPUL2, EMI_MPUM2, EMI_MPUP2, EMI_MPUS, EMI_MPUT

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Bit(s)	Name	Description
28	D4_REP	**Controls Domain 4 violation response** 0: AXI response OKAY when violation 1: AXI response SLVERR when violation
23:16	D4_MASK_HI	**Masks Domain 4 region violation** 0000_0001: Set to 1 to mask Region 8 violation to Domain 4 0000_0010: Set to 1 to mask Region 9 violation to Domain 4 0000_0100: Set to 1 to mask Region 10 violation to Domain 4 0000_1000: Set to 1 to mask Region 11 violation to Domain 4 0001_0000: Set to 1 to mask Region 12 violation to Domain 4 0010_0000: Set to 1 to mask Region 13 violation to Domain 4 0100_0000: Set to 1 to mask Region 14 violation to Domain 4 1000_0000: Set to 1 to mask Region 15 violation to Domain 4
9	D4_OOR_MASK	**Masks Domain 4 out of range** 0: Disable mask 1: Enable mask
8	APB_VIO_MASK0	**Masks Domain 4 APB**
7:0	D4_MASK	**Masks Domain 4 region violation** 0000_0001: Set to 1 to mask Region 0 violation to Domain 4 0000_0010: Set to 1 to mask Region 1 violation to Domain 4 0000_0100: Set to 1 to mask Region 2 violation to Domain 4 0000_1000: Set to 1 to mask Region 3 violation to Domain 4 0001_0000: Set to 1 to mask Region 4 violation to Domain 4 0010_0000: Set to 1 to mask Region 5 violation to Domain 4 0100_0000: Set to 1 to mask Region 6 violation to Domain 4 1000_0000: Set to 1 to mask Region 7 violation to Domain 4

102032C8 **EMI_MPUN2** **Memory Protection Unit Control Registers N** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	D5_LOCK	D5_SEC		D5_REP					D5_MASK_HI							
Type	RW	RW		RW					RW							
Reset	0	0		0					0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							D5_OOR_MASK	APB_VIO_MASK1	D5_MASK							
Type							RW	RW	RW							
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	D5_LOCK	**Controls Domain 5 violation control register lock access** 0: No lock 1: D5_mask[7:0], D5_SEC, D5_LOCK are not changeable.
30	D5_SEC	**Controls Domain 5 violation control register secure access** 0: Domain 5 violation control register can be accessed in both secure/non-secure mode. 1: Domain 5 violation control register can be accessed in secure mode only. Domain 5 violation control register include EMI_MPUA2~EMI_MPUL2, EMI_MPUN2, EMI_MPUQ2, EMI_MPUS, EMI_MPUT
28	D5_REP	**Controls Domain 5 violation response** 0: AXI response OKAY when violation

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Bit(s)	Name	Description
		1: AXI response SLVERR when violation
23:16	D5_MASK_HI	**Masks Domain 5 region violation** 0000_0001: Set to 1 to mask Region 8 violation to Domain 5 0000_0010: Set to 1 to mask Region 9 violation to Domain 5 0000_0100: Set to 1 to mask Region 10 violation to Domain 5 0000_1000: Set to 1 to mask Region 11 violation to Domain 5 0001_0000: Set to 1 to mask Region 12 violation to Domain 5 0010_0000: Set to 1 to mask Region 13 violation to Domain 5 0100_0000: Set to 1 to mask Region 14 violation to Domain 5 1000_0000: Set to 1 to mask Region 15 violation to Domain 5
9	D5_OOR_MASK	**Masks Domain 5 out of range** 0: Disable mask 1: Enable mask
8	APB_VIO_MASK1	**Masks Domain 5 APB**
7:0	D5_MASK	**Masks Domain 5 region violation** 0000_0001: Set to 1 to mask Region 0 violation to Domain 5 0000_0010: Set to 1 to mask Region 1 violation to Domain 5 0000_0100: Set to 1 to mask Region 2 violation to Domain 5 0000_1000: Set to 1 to mask Region 3 violation to Domain 5 0001_0000: Set to 1 to mask Region 4 violation to Domain 5 0010_0000: Set to 1 to mask Region 5 violation to Domain 5 0100_0000: Set to 1 to mask Region 6 violation to Domain 5 1000_0000: Set to 1 to mask Region 7 violation to Domain 5

102032D0 **EMI_MPUO2** **Memory Protection Unit Control Registers O** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**D6_LOCK**	**D6_SEC**		**D6_REP**					**D6_MASK_HI**							
Type	RW	RW		RW					RW							
Reset	0	0		0					0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**D6_OOR_MASK**	**APB_VIO_MASK2**	**D6_MASK**							
Type							RW	RW	RW							
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	D6_LOCK	**Controls Domain 6 violation control register lock access** 0: No lock 1: D6_mask[7:0], D6_SEC, D6_LOCK are not changeable.
30	D6_SEC	**Controls Domain 6 violation control register secure access** 0: Domain 6 violation control register can be accessed in both secure/non-secure mode. 1: Domain 6 violation control register can be accessed in secure mode only. Domain 6 violation control register include EMI_MPUA2~EMI_MPUL2, EMI_MPUO2, EMI_MPUR2, EMI_MPUS, EMI_MPUT
28	D6_REP	**Controls Domain 6 violation response** 0: AXI response OKAY when violation 1: AXI response SLVERR when violation
23:16	D6_MASK_HI	**Masks Domain 6 region violation**

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Bit(s)	Name	Description
		0000_0001: Set to 1 to mask Region 8 violation to Domain 6 0000_0010: Set to 1 to mask Region 9 violation to Domain 6 0000_0100: Set to 1 to mask Region 10 violation to Domain 6 0000_1000: Set to 1 to mask Region 11 violation to Domain 6 0001_0000: Set to 1 to mask Region 12 violation to Domain 6 0010_0000: Set to 1 to mask Region 13 violation to Domain 6 0100_0000: Set to 1 to mask Region 14 violation to Domain 6 1000_0000: Set to 1 to mask Region 15 violation to Domain 6
9	D6_OOR_MASK	**Masks Domain 6 out of range** 0: Disable mask 1: Enable mask
8	APB_VIO_MASK2	**Masks Domain 6 APB**
7:0	D6_MASK	**Masks Domain 6 region violation** 0000_0001: Set to 1 to mask Region 0 violation to Domain 6 0000_0010: Set to 1 to mask Region 1 violation to Domain 6 0000_0100: Set to 1 to mask Region 2 violation to Domain 6 0000_1000: Set to 1 to mask Region 3 violation to Domain 6 0001_0000: Set to 1 to mask Region 4 violation to Domain 6 0010_0000: Set to 1 to mask Region 5 violation to Domain 6 0100_0000: Set to 1 to mask Region 6 violation to Domain 6 1000_0000: Set to 1 to mask Region 7 violation to Domain 6

102032D8 **EMI_MPUP2** **Memory Protection Unit Control Registers P** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									**R15_VIO**	**R14_VIO**	**R13_VIO**	**R12_VIO**	**R11_VIO**	**R10_VIO**	**R9_VIO**	**R8_VIO**
Type									W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**OOR_VIO**	**APB_VIO**	**R7_VIO**	**R6_VIO**	**R5_VIO**	**R4_VIO**	**R3_VIO**	**R2_VIO**	**R1_VIO**	**R0_VIO**
Type							W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23	R15_VIO	**Region 15 abort violation status to Domain 4** 0: No Region 15 abort violation 1: Region 15 abort violation
22	R14_VIO	**Region 14 abort violation status to Domain 4** 0: No Region 14 abort violation 1: Region 14 abort violation
21	R13_VIO	**Region 13 abort violation status to Domain 4** 0: No Region 13 abort violation 1: Region 13 abort violation
20	R12_VIO	**Region 12 abort violation status to Domain 4** 0: No Region 12 abort violation 1: Region 12 abort violation
19	R11_VIO	**Region 11 abort violation status to Domain 4** 0: No Region 11 abort violation 1: Region 11 abort violation
18	R10_VIO	**Region 10 abort violation status to Domain 4**

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Bit(s)	Name	Description
		0: No Region 10 abort violation 1: Region 10 abort violation
17	R9_VIO	**Region 9 abort violation status to Domain 4** 0: No Region 9 abort violation 1: Region 9 abort violation
16	R8_VIO	**Region 8 abort violation status to Domain 4** EMI will first record the unmask device abort information at EMI_MPUS and EMI_MPUT if unmasking and set up the corresponding R8_VIO status bit. Clear R8_VIO for EMI to record the next violation status. When multiple violations occur, the corresponding D0_VIO_STA status bit will be set. However, only the device abort information will be recorded at VIO_DBGx, and its content will not be changed until the software clears it. 0: No Region 8 abort violation 1: Region 8 abort violation
9	OOR_VIO	**Out of range abort violation status to Domain 4** 0: No out of range abort violation 1: Out of range abort violation
8	APB_VIO	**APB abort violation status to Domain 4** 0: No APB abort violation 1: APB abort violation *Note: EMI_MPUP2 is allowed to be accessed in the secure mode only when D4_SEC = 1.*
7	R7_VIO	**Region 7 abort violation status to Domain 4** 0: No Region 7 abort violation 1: Region 7abort violation
6	R6_VIO	**Region 6 abort violation status to Domain 4** 0: No Region 6 abort violation 1: Region 6 abort violation
5	R5_VIO	**Region 5 abort violation status to Domain 4** 0: No Region 5 abort violation 1: Region 5 abort violation
4	R4_VIO	**Region 4 abort violation status to Domain 4** 0: No Region 4 abort violation 1: Region 4 abort violation
3	R3_VIO	**Region 3 abort violation status to Domain 4** 0: No Region 3 abort violation 1: Region 3 abort violation
2	R2_VIO	**Region 2 abort violation status to Domain 4** 0: No Region 2 abort violation 1: Region 2 abort violation
1	R1_VIO	**Region 1 abort violation status to Domain 4** 0: No Region 1 abort violation 1: Region 1 abort violation
0	R0_VIO	**Region 0 abort violation status to Domain 4** EMI will first record the unmask device abort information at EMI_MPUS and EMI_MPUT if unmasking and set up the corresponding R0_VIO status bit. Clear R0_VIO for EMI to record the next violation status. When multiple violations occur, the corresponding D0_VIO_STA status bit will be set. However, only the device abort information will be recorded at VIO_DBGx, and its content will not be changed until the software clears it. 0: No Region 0 abort violation 1: Region 0 abort violation

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102032E0	EMI_MPUQ2	Memory Protection Unit Control Registers Q	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									R15_VIO	R14_VIO	R13_VIO	R12_VIO	R11_VIO	R10_VIO	R9_VIO	R8_VIO
Type									W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							OOR_VIO	APB_VIO	R7_VIO	R6_VIO	R5_VIO	R4_VIO	R3_VIO	R2_VIO	R1_VIO	R0_VIO
Type							W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23	R15_VIO	**Region 15 abort violation status to Domain 5** 0: No Region 15 abort violation 1: Region 15 abort violation
22	R14_VIO	**Region 14 abort violation status to Domain 5** 0: No Region 14 abort violation 1: Region 14 abort violation
21	R13_VIO	**Region 13 abort violation status to Domain 5** 0: No Region 13 abort violation 1: Region 13 abort violation
20	R12_VIO	**Region 12 abort violation status to Domain 5** 0: No Region 12 abort violation 1: Region 12 abort violation
19	R11_VIO	**Region 11 abort violation status to Domain 5** 0: No Region 11 abort violation 1: Region 11 abort violation
18	R10_VIO	**Region 10 abort violation status to Domain 5** 0: No Region 10 abort violation 1: Region 10 abort violation
17	R9_VIO	**Region 9 abort violation status to Domain 5** 0: No Region 9 abort violation 1: Region 9 abort violation
16	R8_VIO	**Region 8 abort violation status to Domain 5** EMI will first record the unmask device abort information at EMI_MPUS and EMI_MPUT if unmasking and set up the corresponding R8_VIO status bit. Clear R8_VIO for EMI to record the next violation status. When multiple violations occur, the corresponding D0_VIO_STA status bit will be set. However, only the device abort information will be recorded at VIO_DBGx, and its content will not be changed until the software clears it. 0: No Region 8 abort violation 1: Region 8 abort violation
9	OOR_VIO	**Out of range abort violation status to Domain 5** 0: No out of range abort violation 1: Out of range abort violation
8	APB_VIO	**APB abort violation status to Domain 5** 0: No APB abort violation 1: APB abort violation *Note: EMI_MPUP2 is allowed to be accessed in the secure mode only when D4_SEC = 1.*
7	R7_VIO	**Region 7 abort violation status to Domain 5** 0: No Region 7 abort violation

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Bit(s)	Name	Description
		1: Region 7abort violation
6	R6_VIO	**Region 6 abort violation status to Domain 5** 0: No Region 6 abort violation 1: Region 6 abort violation
5	R5_VIO	**Region 5 abort violation status to Domain 5** 0: No Region 5 abort violation 1: Region 5 abort violation
4	R4_VIO	**Region 4 abort violation status to Domain 5** 0: No Region 4 abort violation 1: Region 4 abort violation
3	R3_VIO	**Region 3 abort violation status to Domain 5** 0: No Region 3 abort violation 1: Region 3 abort violation
2	R2_VIO	**Region 2 abort violation status to Domain 5** 0: No Region 2 abort violation 1: Region 2 abort violation
1	R1_VIO	**Region 1 abort violation status to Domain 5** 0: No Region 1 abort violation 1: Region 1 abort violation
0	R0_VIO	**Region 0 abort violation status to Domain 5** 0: No Region 0 abort violation 1: Region 0 abort violation

102032E8 **EMI_MPUR2** **Memory Protection Unit Control Registers R** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									R15_VIO	R14_VIO	R13_VIO	R12_VIO	R11_VIO	R10_VIO	R9_VIO	R8_VIO
Type									W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							OOR_VIO	APB_VIO	R7_VIO	R6_VIO	R5_VIO	R4_VIO	R3_VIO	R2_VIO	R1_VIO	R0_VIO
Type							W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23	R15_VIO	**Region 15 abort violation status to Domain 6** 0: No Region 15 abort violation 1: Region 15 abort violation
22	R14_VIO	**Region 14 abort violation status to Domain 6** 0: No Region 14 abort violation 1: Region 14 abort violation
21	R13_VIO	**Region 13 abort violation status to Domain 6** 0: No Region 13 abort violation 1: Region 13 abort violation
20	R12_VIO	**Region 12 abort violation status to Domain 6** 0: No Region 12 abort violation 1: Region 12 abort violation
19	R11_VIO	**Region 11 abort violation status to Domain 6**

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Bit(s)	Name	Description
		0: No Region 11 abort violation 1: Region 11 abort violation
18	R10_VIO	**Region 10 abort violation status to Domain 6** 0: No Region 10 abort violation 1: Region 10 abort violation
17	R9_VIO	**Region 9 abort violation status to Domain 6** 0: No Region 9 abort violation 1: Region 9 abort violation
16	R8_VIO	**Region 8 abort violation status to Domain 6** EMI will first record the unmask device abort information at EMI_MPUS and EMI_MPUT if unmasking and set up the corresponding R8_VIO status bit. Clear R8_VIO for EMI to record the next violation status. When multiple violations occur, the corresponding D0_VIO_STA status bit will be set. However, only the device abort information will be recorded at VIO_DBGx, and its content will not be changed until the software clears it. 0: No Region 8 abort violation 1: Region 8 abort violation
9	OOR_VIO	**Out of range abort violation status to Domain 6** 0: No out of range abort violation 1: Out of range abort violation
8	APB_VIO	**APB abort violation status to Domain 6** 0: No APB abort violation 1: APB abort violation Note: EMI_MPUR2 is allowed to be accessed in the secure mode only when D6_SEC = 1.
7	R7_VIO	**Region 7 abort violation status to Domain 6** 0: No Region 7 abort violation 1: Region 7abort violation
6	R6_VIO	**Region 6 abort violation status to Domain 6** 0: No Region 6 abort violation 1: Region 6 abort violation
5	R5_VIO	**Region 5 abort violation status to Domain 6** 0: No Region 5 abort violation 1: Region 5 abort violation
4	R4_VIO	**Region 4 abort violation status to Domain 6** 0: No Region 4 abort violation 1: Region 4 abort violation
3	R3_VIO	**Region 3 abort violation status to Domain 6** 0: No Region 3 abort violation 1: Region 3 abort violation
2	R2_VIO	**Region 2 abort violation status to Domain 6** 0: No Region 2 abort violation 1: Region 2 abort violation
1	R1_VIO	**Region 1 abort violation status to Domain 6** 0: No Region 1 abort violation 1: Region 1 abort violation
0	R0_VIO	**Region 0 abort violation status to Domain 6** 0: No Region 0 abort violation 1: Region 0 abort violation

10203300	**EMI_MPUU 2**	**Memory Protection Unit Control Registers U**	**00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	D7_LOCK	D7_SEC		D7_REP					D7_MASK_HI							
Type	RW	RW		RW					RW							
Reset	0	0		0					0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							D7_OOR_MASK	APB_VIO_MASK3	D7_MASK							
Type							RW	RW	RW							
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	D7_LOCK	**Controls Domain 7 violation control register lock access** 0: No lock 1: D7_mask[7:0], D7_SEC, D7_LOCK are not changeable.
30	D7_SEC	**Controls Domain 7 violation control register secure access** 0: Domain 7 violation control register can be accessed in both secure/non-secure mode. 1: Domain 7 violation control register can be accessed in secure mode only. Domain 7 violation control register include EMI_MPUA2~EMI_MPUL2, EMI_MPUU2, EMI_MPUV, EMI_MPUS, EMI_MPUT
28	D7_REP	**Controls Domain 7 violation response** 0: AXI response OKAY when violation 1: AXI response SLVERR when violation
23:16	D7_MASK_HI	**Masks Domain 7 region violation** 0000_0001: Set to 1 to mask Region 8 violation to Domain 7 0000_0010: Set to 1 to mask Region 9 violation to Domain 7 0000_0100: Set to 1 to mask Region 10 violation to Domain 7 0000_1000: Set to 1 to mask Region 11 violation to Domain 7 0001_0000: Set to 1 to mask Region 12 violation to Domain 7 0010_0000: Set to 1 to mask Region 13 violation to Domain 7 0100_0000: Set to 1 to mask Region 14 violation to Domain 7 1000_0000: Set to 1 to mask Region 15 violation to Domain 7
9	D7_OOR_MASK	**Masks Domain 7 out of range** 0: Disable mask 1: Enable mask
8	APB_VIO_MASK3	**Masks Domain 7 APB**
7:0	D7_MASK	**Masks Domain 7 region violation** 0000_0001: Set to 1 to mask Region 0 violation to Domain 7 0000_0010: Set to 1 to mask Region 1 violation to Domain 7 0000_0100: Set to 1 to mask Region 2 violation to Domain 7 0000_1000: Set to 1 to mask Region 3 violation to Domain 7 0001_0000: Set to 1 to mask Region 4 violation to Domain 7 0010_0000: Set to 1 to mask Region 5 violation to Domain 7 0100_0000: Set to 1 to mask Region 6 violation to Domain 7 1000_0000: Set to 1 to mask Region 7 violation to Domain 7

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10203320 EMI_MPUY2 Memory Protection Unit Control Registers Y 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									R15_VIO	R14_VIO	R13_VIO	R12_VIO	R11_VIO	R10_VIO	R9_VIO	R8_VIO
Type									W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C

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Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**OOR_VIO**	**APB_VIO**	**R7_VIO**	**R6_VIO**	**R5_VIO**	**R4_VIO**	**R3_VIO**	**R2_VIO**	**R1_VIO**	**R0_VIO**
Type							W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23	R15_VIO	**Region 15 abort violation status to Domain 7** 0: No Region 15 abort violation 1: Region 15 abort violation
22	R14_VIO	**Region 14 abort violation status to Domain 7** 0: No Region 14 abort violation 1: Region 14 abort violation
21	R13_VIO	**Region 13 abort violation status to Domain 7** 0: No Region 13 abort violation 1: Region 13 abort violation
20	R12_VIO	**Region 12 abort violation status to Domain 7** 0: No Region 12 abort violation 1: Region 12 abort violation
19	R11_VIO	**Region 11 abort violation status to Domain 7** 0: No Region 11 abort violation 1: Region 11 abort violation
18	R10_VIO	**Region 10 abort violation status to Domain 7** 0: No Region 10 abort violation 1: Region 10 abort violation
17	R9_VIO	**Region 9 abort violation status to Domain 7** 0: No Region 9 abort violation 1: Region 9 abort violation
16	R8_VIO	**Region 8 abort violation status to Domain 7** EMI will first record the unmask device abort information at EMI_MPUS and EMI_MPUT if unmasking and set up the corresponding R8_VIO status bit. Clear R8_VIO for EMI to record the next violation status. When multiple violations occur, the corresponding D0_VIO_STA status bit will be set. However, only the device abort information will be recorded at VIO_DBGx, and its content will not be changed until the software clears it. 0: No Region 8 abort violation 1: Region 8 abort violation
9	OOR_VIO	**Out of range abort violation status to Domain 7** 0: No out of range abort violation 1: Out of range abort violation
8	APB_VIO	**APB abort violation status to Domain 7** 0: No APB abort violation 1: APB abort violation *Note: EMI_MPUR2 is allowed to be accessed in the secure mode only when D6_SEC = 1.*
7	R7_VIO	**Region 7 abort violation status to Domain 7** 0: No Region 7 abort violation 1: Region 7abort violation
6	R6_VIO	**Region 6 abort violation status to Domain 7** 0: No Region 6 abort violation 1: Region 6 abort violation
5	R5_VIO	**Region 5 abort violation status to Domain 7** 0: No Region 5 abort violation 1: Region 5 abort violation

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Bit(s)	Name	Description
4	R4_VIO	**Region 4 abort violation status to Domain 7** 0: No Region 4 abort violation 1: Region 4 abort violation
3	R3_VIO	**Region 3 abort violation status to Domain 7** 0: No Region 3 abort violation 1: Region 3 abort violation
2	R2_VIO	**Region 2 abort violation status to Domain 7** 0: No Region 2 abort violation 1: Region 2 abort violation
1	R1_VIO	**Region 1 abort violation status to Domain 7** 0: No Region 1 abort violation 1: Region 1 abort violation
0	R0_VIO	**Region 0 abort violation status to Domain 7** 0: No Region 0 abort violation 1: Region 0 abort violation

10203400 EMI_BMEN EMI Bus Monitor Control Registers 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEL_TRANS_TYPE								SEL_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								BC_OVERRUN			BUS_MON_RW			BUS_MON_STP	BUS_MON_PAUSE	BUS_MON_EN
Type								RO			RW			RO	RW	RW
Reset								0			0	0		0	0	0

Bit(s)	Name	Description
31:24	SEL_TRANS_TYPE	**Uses SEL_MASTER (EMI_BMEN[30:16]) to select transaction type to be recorded** The result can be read from EMI_TTYPE1. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL_TRANS_TYPE[3:0]: 0000 ~ 1111 1-beat ~ 16-beat SEL_TRANS_TYPE[6:4]: 000 ~ 100 1/2/4/8/16-byte SEL_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
23:16	SEL_MASTER	**Monitors selected masters (master 0 ~ 7)** EMI_BMEN[16]: ARM 0 EMI_BMEN[17]: ARM 1 EMI_BMEN[18]: MM 1 EMI_BMEN[19]: MDMCU EMI_BMEN[20]: Modem EMI_BMEN[21]: Multimedia 0 EMI_BMEN[22]: GPU 0 EMI_BMEN[23]: GPU 1
8	BC_OVERRUN	**Bus counter (BUSCYC_CNT, WORD_ALL_CNT, BUSY_CNT) .**
5:4	BUS_MON_RW	**Bus monitor for read/write** 00: Monitor read/write transactions 01: Monitor only read transactions 10: Monitor only write transactions 11: Monitor read/write transactions
2	BUS_MON_STP	**Pauses monitor circuit**

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Bit(s)	Name	Description
1	BUS_MON_PAUSE	**Pauses monitor circuit** 0: Does not pause 1: Pause *Note: When SW configures this bit, SW should turn off EMI and infra DCM or dummy read DDR.*
0	BUS_MON_EN	**Enables monitor circuit** When disabled, all monitor counters will be cleared. 0: Disable 1: Enable *Note: When SW configures this bit, SW should turn off EMI and infra DCM or dummy read DDR.*

10203404 EMI_BSTP EMI Bus Monitor Auto Stop Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUSCYC_STOP[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUSCYC_STOP[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUSCYC_STOP	**When bus cycle count equals CUSCYC_STOP, all counters stop automatically.** If BUSCYC_STOP is set to 0, the counter cannot stop automatically.

10203408 EMI_BCNT EMI 3rd Double-word Counter of Selected Masters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUSCYC_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUSCYC_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUSCYC_CNT	**Bus cycle counter** Keeps to the maximum when reached. This counter is counted by a DCM clock. Thus the absolute time referred to this counter will be affected under the idle mode, during which the EMI clock is gated.

10203410 EMI_TACT EMI 4th Double-Word Counter of Selected Masters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TRANS_ALL_CNT[31:16]															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TRANS_ALL_CNT[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TRANS_ALL_CNT	**Counter for transactions of all masters (master 0 ~ 6)** Keeps to the maximum when reached

10203418 EMI_TSCT EMI 3rd Double-word Counter of Selected Masters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**TRANS_CNT[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TRANS_CNT[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TRANS_CNT	**Counter for transactions of all masters (master 0 ~ master 6)** The first counter for transactions of selected masters (master 0 ~ 6). Will keep to the maximum when reached. It is also counter for EMI cycles and will keep to the maximum when reached.

10203420 EMI_WACT EMI 4th Double-Word Counter of Selected Masters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**WORD_ALL_CNT[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**WORD_ALL_CNT[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD_ALL_CNT	**Counter for access amount (unit: double words, 8-byte) to EMI of all masters (master 0 ~ 6)** Keeps to the maximum when reached

10203428 EMI_WSCT EMI 3rd Double-word Counter of Selected Masters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**WORD_CNT[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD_CNT	**First counter for access amount (unit: double words, 8-byte) to EMI of selected masters (master 0 ~ 6)** Keeps to the maximum when reached.

10203430 EMI_BACT EMI 4th Double-Word Counter of Selected Masters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BAND_WORD_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BAND_WORD_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BAND_WORD_CNT	**Bandwidth counter for access amount (unit: double words, 16-byte) to EMI of selected masters (master 0 ~ 6)** Will keep to the maximum when reached. If the EMI clock and DRAM clock is 1:1, one EMI cycle will represent 8 bytes. If the EMI clock and DRAM clock is 1:2, one EMI cycle will represent 16 bytes.

10203438 EMI_BSCT EMI 3rd Double-word Counter of Selected Masters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OVERHEAD_WORD_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OVERHEAD_WORD_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OVERHEAD_WORD_CNT	**Overhead counter for access amount (unit: double words, 8-byte) to EMI of selected masters (master 0 ~ 6)** Will keep to the maximum when reached. When the EMI clock and DRAM clock is 1:1, one EMI cycle will represent 8 bytes. When the EMI clock and DRAM clock is 1:2, one EMI cycle will represent 16 bytes.

10203440 EMI_MSEL EMI 4th Double-Word Counter of Selected Masters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	SEL3_TRANS_TYPE								SEL3_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEL2_TRANS_TYPE								SEL2_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	SEL3_TRANS_TYPE	**Uses SEL3_TRANS_TYPE + SEL3_MASTER (EMI_MSEL[31:16]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE3. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL3_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL3_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL3_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
23:16	SEL3_MASTER	**Monitors the selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT3, EMI_WSCT3, EMI_TTYPE3)**
15:8	SEL2_TRANS_TYPE	**Uses SEL2_TRANS_TYPE + SEL2_MASTER (EMI_MSEL[15:0]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE2. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL2_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL2_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL2_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
7:0	SEL2_MASTER	**Monitors the selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT2, EMI_WSCT2, EMI_TTYPE2)**

10203448 EMI_TSCT2 EMI 4th Double-Word Counter of Selected Masters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TRANS2_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANS2_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TRANS2_CNT	**Second counter for transactions of selected masters (master 0 ~ 6)** Will keep to the maximum when reached.

10203450 EMI_TSCT3 EMI 3rd Double-word Counter of Selected Masters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TRANS3_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANS3_CNT[15:0]															

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Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TRANS3_CNT	**Third counter for transactions of selected masters (master 0 ~ 6)** Will keep to the maximum when reached.

10203458 EMI_WSCT2 EMI 4th Double-Word Counter of Selected Masters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD2_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD2_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD2_CNT	**Second counter for access amount (unit: double words, 8-byte) to EMI of selected masters (master 0 ~ 6)** Will keep to the maximum when reached.

10203460 EMI_WSCT3 EMI 3rd Double-word Counter of Selected Masters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD3_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD3_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD3_CNT	**Third counter for access amount (unit: double words, 8-byte) to EMI of selected masters (master 0 ~ 6)** Will keep to the maximum when reached.

10203464 EMI_WSCT4 EMI 4th Double-Word Counter of Selected Masters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD4_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD4_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	WORD4_CNT	**Fourth counter for access amount (unit: double words, 8-byte) to EMI of selected masters (master 0 ~ 6)** Will keep to the maximum when reached.

10203468 EMI_MSEL2 EMI Master Selection for 4th and 5th Counters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEL5_TRANS_TYPE								SEL5_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEL4_TRANS_TYPE								SEL4_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	SEL5_TRANS_TYPE	**Uses SEL5_TRANS_TYPE + SEL5_MASTER (EMI_MSEL2[31:16]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE5. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL5_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL5_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL5_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
23:16	SEL5_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT5, EMI_WSCT5, EMI_TTYPE5)**
15:8	SEL4_TRANS_TYPE	**Uses SEL4_TRANS_TYPE + SEL4_MASTER (EMI_MSEL2[15:0]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE4. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL4_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL4_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL4_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
7:0	SEL4_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT4, EMI_WSCT4, EMI_TTYPE4)**

10203470 EMI_MSEL3 EMI Master Selection for 6th and 7th Counters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEL7_TRANS_TYPE								SEL7_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEL6_TRANS_TYPE								SEL6_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	SEL7_TRANS_TYP	**Uses SEL7_TRANS_TYPE + SEL7_MASTER (EMI_MSEL3[31:16])**

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Bit(s)	Name	Description
	E	**to select the transaction type to be recorded** The result can be read from EMI_TTYPE7. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL7_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL7_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL7_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
23:16	SEL7_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT7, EMI_WSCT7, EMI_TTYPE7)**
15:8	SEL6_TRANS_TYP E	**Uses SEL6_TRANS_TYPE + SEL6_MASTER (EMI_MSEL3[15:0]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE6. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL6_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL6_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL6_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
7:0	SEL6_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT6, EMI_WSCT6, EMI_TTYPE6)**

10203478 EMI_MSEL4 EMI Master Selection for 8th and 9th Counters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEL9_TRANS_TYPE								SEL9_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEL8_TRANS_TYPE								SEL8_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	SEL9_TRANS_TYP E	**Uses SEL9_TRANS_TYPE + SEL9_MASTER (EMI_MSEL4[31:16]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE9. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL9_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL9_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL9_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
23:16	SEL9_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT9, EMI_WSCT9, EMI_TTYPE9)**
15:8	SEL8_TRANS_TYP E	**Uses SEL8_TRANS_TYPE + SEL8_MASTER (EMI_MSEL4[15:0]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE8. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL8_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL8_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL8_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
7:0	SEL8_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT8, EMI_WSCT8, EMI_TTYPE8)**

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10203480 EMI_MSEL5 EMI Master Selection for 10th and 11th Counters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEL11_TRANS_TYPE								SEL11_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEL10_TRANS_TYPE								SEL10_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	SEL11_TRANS_TYPE	**Uses SEL11_TRANS_TYPE + SEL11_MASTER (EMI_MSEL5[31:16]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE11. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL11_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL11_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL11_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
23:16	SEL11_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT11, EMI_WSCT11, EMI_TTYPE11)**
15:8	SEL10_TRANS_TYPE	**Uses SEL10_TRANS_TYPE + SEL10_MASTER (EMI_MSEL5[15:0]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE10. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL10_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL10_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL10_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
7:0	SEL10_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT10, EMI_WSCT10, EMI_TTYPE10)**

10203488 EMI_MSEL6 EMI Master Selection for 12th and 13th Counters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEL13_TRANS_TYPE								SEL13_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEL12_TRANS_TYPE								SEL12_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	SEL13_TRANS_TYPE	**Uses SEL13_TRANS_TYPE + SEL13_MASTER (EMI_MSEL6[31:16]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE13. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL13_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL13_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL13_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
23:16	SEL13_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT13, EMI_WSCT13, EMI_TTYPE13)**

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Bit(s)	Name	Description
15:8	SEL12_TRANS_TYPE	**Uses SEL12_TRANS_TYPE + SEL12_MASTER (EMI_MSEL6[15:0]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE12. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL12_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL12_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL12_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
7:0	SEL12_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT12, EMI_WSCT12, EMI_TTYPE12)**

10203490 EMI_MSEL7 EMI Master Selection for 14th and 15th Counters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEL15_TRANS_TYPE								SEL15_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEL14_TRANS_TYPE								SEL14_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	SEL15_TRANS_TYPE	**Uses SEL15_TRANS_TYPE + SEL15_MASTER (EMI_MSEL7[31:16]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE15. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL15_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL15_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL15_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
23:16	SEL15_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT15, EMI_WSCT15, EMI_TTYPE15)**
15:8	SEL14_TRANS_TYPE	**Uses SEL14_TRANS_TYPE + SEL14_MASTER (EMI_MSEL7[15:0]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE14. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL14_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL14_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL14_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
7:0	SEL14_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT14, EMI_WSCT14, EMI_TTYPE14)**

10203498 EMI_MSEL8 EMI Master Selection for 16th and 17th Counters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEL17_TRANS_TYPE								SEL17_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEL16_TRANS_TYPE								SEL16_MASTER							

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Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	SEL17_TRANS_TYPE	**Uses SEL17_TRANS_TYPE + SEL17_MASTER (EMI_MSEL8[31:16]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE17. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL17_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL17_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL17_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
23:16	SEL17_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT17, EMI_WSCT17, EMI_TTYPE17)**
15:8	SEL16_TRANS_TYPE	**Uses SEL16_TRANS_TYPE + SEL16_MASTER (EMI_MSEL8[15:0]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE16. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL16_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL16_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL16_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
7:0	SEL16_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT16, EMI_WSCT16, EMI_TTYPE16)**

102034A0 **EMI_MSEL9** **EMI Master Selection for 18th and 19th Counters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEL19_TRANS_TYPE								SEL19_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEL18_TRANS_TYPE								SEL18_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	SEL19_TRANS_TYPE	**Uses SEL19_TRANS_TYPE + SEL19_MASTER (EMI_MSEL9[31:16]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE19. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL19_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL19_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL19_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
23:16	SEL19_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT19, EMI_WSCT19, EMI_TTYPE19)**
15:8	SEL18_TRANS_TYPE	**Uses SEL18_TRANS_TYPE + SEL18_MASTER (EMI_MSEL9[15:0]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE18. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL18_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL18_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL18_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
7:0	SEL18_MASTER	**Monitors selected masters (master 0 ~ 6) for the second**

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Bit(s)	Name	Description
		transaction/word/type counters (EMI_TSCT18, EMI_WSCT18, EMI_TTYPE18)

102034A8 **EMI_MSEL10** **EMI Master Selection for 20th and 21st Counters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEL21_TRANS_TYPE								SEL21_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEL20_TRANS_TYPE								SEL20_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	SEL21_TRANS_TYPE	**Uses SEL21_TRANS_TYPE + SEL21_MASTER (EMI_MSEL10[31:16]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE21. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL21_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL21_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL21_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
23:16	SEL21_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT21, EMI_WSCT21, EMI_TTYPE21)**
15:8	SEL20_TRANS_TYPE	**Uses SEL20_TRANS_TYPE + SEL20_MASTER (EMI_MSEL10[15:0]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE20. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL20_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL20_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL20_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
7:0	SEL20_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT20, EMI_WSCT20, EMI_TTYPE20)**

102034B0 **EMI_BMID0** **EMI ID Selection for 1- 2 Transaction Type Counters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SEL2_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SEL1_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	SEL2_ID	ID selection 2
9:0	SEL1_ID	ID selection 1

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102034B4 **EMI_BMID1** **EMI ID Selection for 3- 4 Transaction Type Counters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SEL4_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SEL3_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	SEL4_ID	ID selection 4
9:0	SEL3_ID	ID selection 3

102034B8 **EMI_BMID2** **EMI ID Selection for 5- 6 Transaction Type Counters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SEL6_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SEL5_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	SEL6_ID	ID selection 6
9:0	SEL5_ID	ID selection 5

102034BC **EMI_BMID3** **EMI ID Selection for 7- 8 Transaction Type Counters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SEL8_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SEL7_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	SEL8_ID	ID selection 8
9:0	SEL7_ID	ID selection 7

102034C0 **EMI_BMID4** **EMI ID Selection for 9- 10 Transaction Type** **00000000**

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Counters

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SEL10_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SEL9_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	SEL10_ID	ID selection 10
9:0	SEL9_ID	ID selection 9

102034C4 **EMI_BMID5** **EMI ID Selection for 11- 12 Transaction Type Counters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SEL12_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SEL11_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	SEL12_ID	ID selection 12
9:0	SEL11_ID	ID selection 11

102034C8 **EMI_BMID6** **EMI ID Selection for 13- 14 Transaction Type Counters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SEL14_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SEL13_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	SEL14_ID	ID selection 14
9:0	SEL13_ID	ID selection 13

102034CC **EMI_BMID7** **EMI ID Selection for 15- 16 Transaction Type Counters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SEL16_ID									

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Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**SEL15_ID**									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	SEL16_ID	ID selection 16
9:0	SEL15_ID	ID selection 15

102034D0 **EMI_BMID8** **EMI ID Selection for 17- 18 Transaction Type Counters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							**SEL18_ID**									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**SEL17_ID**									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	SEL18_ID	ID selection 18
9:0	SEL17_ID	ID selection 17

102034D4 **EMI_BMID9** **EMI ID Selection for 19- 20 Transaction Type Counters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							**SEL20_ID**									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**SEL19_ID**									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	SEL20_ID	ID selection 20
9:0	SEL19_ID	ID selection 19

102034D8 **EMI_BMID10** **EMI ID Selection for 21 Transaction Type Counters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**SEL21_ID**									

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Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	SEL21_ID	ID selection 21

102034E0 EMI_BMEN1 EMI ID Selection Enabling 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												**HPRI_EN[20:16]**				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**HPRI_EN[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	HPRI_EN	Enables high-priority filter for selected masters

102034E8 EMI_BMEN2 EMI ID Selection Enabling 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						**NON_ALIGN_CNT_SEL**	**BAN_LAT_CNT_SEL**					**SEL_ID_EN[20:16]**				
Type						RW	RW					RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SEL_ID_EN[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26	NON_ALIGN_CNT_SEL	**All counter for non-32B align except for bus cycle count and trans_all count** 0: Normal counter. 1: Only count cross 32B transcation
25:24	BAN_LAT_CNT_SEL	**Enables type count used for bank usage count/Latency count enabling** 00: Type counter. 01/11: ttType1-- ttype8 and ttype9 -- ttype16 changes as bank usage count 10: tTtype1 -- ttype7 changes as total latencies for m0 -- m6, and ttype9 -- ttype15 changes as total transaction counts for m0 -- m6
20:0	SEL_ID_EN	**21'h0: No ID selection for 21 type counters** 21'h1: Enable ID selection for type counter 1 21'h2: Enable ID selection for type counter 2 21'h4: Enable ID selection for type counter 3 ... 21'h100000: Enable ID selection for type counter 21.

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102034F8	EMI_BMRW0	EMI ID Selection High Bit for 1-16 Transaction Type Counters	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEL16_RW		SEL15_RW		SEL14_RW		SEL13_RW		SEL12_RW		SEL11_RW		SEL10_RW		SEL9_RW	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEL8_RW		SEL7_RW		SEL6_RW		SEL5_RW		SEL4_RW		SEL3_RW		SEL2_RW		SEL1_RW	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	SEL16_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
29:28	SEL15_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
27:26	SEL14_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
25:24	SEL13_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
23:22	SEL12_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
21:20	SEL11_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
19:18	SEL10_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
17:16	SEL9_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
15:14	SEL8_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
13:12	SEL7_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
11:10	SEL6_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only

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Bit(s)	Name	Description
		10: Monitor write transaction only 11: Monitor read and write transaction
9:8	SEL5_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
7:6	SEL4_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
5:4	SEL3_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
3:2	SEL2_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
1:0	SEL1_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction

102034FC **EMI_BMRW1** **EMI ID Selection High Bit for 1-16 Transaction Type Counters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SEL21_RW		SEL20_RW		SEL19_RW		SEL18_RW		SEL17_RW	
Type							RW		RW		RW		RW		RW	
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:8	SEL21_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
7:6	SEL20_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
5:4	SEL19_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
3:2	SEL18_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
1:0	SEL17_RW	00: Follow EMI_BMEN[5:4] setting

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Bit(s)	Name	Description
		01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction

10203500 **EMI_TTYPE1** **EMI 1st Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE1_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE1_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE1_CNT	**1st counter for number of a transaction type of selected masters (SEL_TRANS_TYPE + SEL_MASTER) (EMI_BMEN[31:16])** Will keep to the maximum when reached.

10203508 **EMI_TTYPE2** **EMI 2nd Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE2_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE2_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE2_CNT	**2nd counter for number of a transaction type of selected masters (SEL2_TRANS_TYPE + SEL2_MASTER) (EMI_MSEL[15:0])** Will keep to the maximum when reached.

10203510 **EMI_TTYPE3** **EMI 3rd Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE3_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE3_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:0	TTYPE3_CNT	**3rd counter for number of a transaction type of selected masters (SEL3_TRANS_TYPE + SEL3_MASTER) (EMI_MSEL[31:16])** Will keep to the maximum when reached.

10203518 **EMI_TTYPE4** **EMI 4th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE4_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE4_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE4_CNT	**4th counter for number of a transaction type of selected masters (SEL4_TRANS_TYPE + SEL4_MASTER) (EMI_MSEL2[15:0])** Will keep to the maximum when reached.

10203520 **EMI_TTYPE5** **EMI 5th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE5_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE5_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE5_CNT	**5th counter for number of a transaction type of selected masters (SEL5_TRANS_TYPE + SEL5_MASTER) (EMI_MSEL2 [31:16])** Will keep to the maximum when reached.

10203528 **EMI_TTYPE6** **EMI 6th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE6_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE6_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:0	TTYPE6_CNT	**6th counter for number of a transaction type of selected masters (SEL6_TRANS_TYPE + SEL6_MASTER) (EMI_MSEL3[15:0])** Will keep to the maximum when reached.

10203530 **EMI_TTYPE7** **EMI 7th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE7_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE7_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE7_CNT	**7th counter for number of a transaction type of selected masters (SEL7_TRANS_TYPE + SEL7_MASTER) (EMI_MSEL3[31:16])** Will keep to the maximum when reached.

10203538 **EMI_TTYPE8** **EMI 8th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE8_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE8_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE8_CNT	**8th counter for number of a transaction type of selected masters (SEL8_TRANS_TYPE + SEL8_MASTER) (EMI_MSEL4[15:0])** Will keep to the maximum when reached.

10203540 **EMI_TTYPE9** **EMI 9th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE9_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE9_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:0	TTYPE9_CNT	**9th counter for number of a transaction type of selected masters (SEL9_TRANS_TYPE + SEL9_MASTER) (EMI_MSEL4[31:16])** Will keep to the maximum when reached.

10203548 **EMI_TTYPE10** **EMI 10th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE10_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE10_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE10_CNT	**10th counter for number of a transaction type of selected masters (SEL10_TRANS_TYPE + SEL10_MASTER) (EMI_MSEL5[15:0])** Will keep to the maximum when reached.

10203550 **EMI_TTYPE11** **EMI 11th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE11_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE11_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE11_CNT	**11th counter for number of a transaction type of selected masters (SEL11_TRANS_TYPE + SEL11_MASTER) (EMI_MSEL5[31:16])** Will keep to the maximum when reached.

10203558 **EMI_TTYPE12** **EMI 12th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE12_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE12_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:0	TTYPE12_CNT	**12th counter for number of a transaction type of selected masters (SEL12_TRANS_TYPE + SEL12_MASTER) (EMI_MSEL6[15:0])** Will keep to the maximum when reached.

10203560 **EMI_TTYPE 13** **EMI 13th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE13_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE13_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE13_CNT	**13th counter for number of a transaction type of selected masters (SEL13_TRANS_TYPE + SEL13_MASTER) (EMI_MSEL6[31:16])** Will keep to the maximum when reached.

10203568 **EMI_TTYPE 14** **EMI 14th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE14_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE14_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE14_CNT	**14th counter for number of a transaction type of selected masters (SEL14_TRANS_TYPE + SEL14_MASTER) (EMI_MSEL7[15:0])** Will keep to the maximum when reached.

10203570 **EMI_TTYPE 15** **EMI 15th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE15_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE15_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:0	TTYPE15_CNT	**15th counter for number of a transaction type of selected masters (SEL15_TRANS_TYPE + SEL15_MASTER) (EMI_MSEL7[31:16])** Will keep to the maximum when reached.

10203578 **EMI_TTYPE 16** **EMI 16th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE16_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE16_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE16_CNT	**16th counter for number of a transaction type of selected masters (SEL16_TRANS_TYPE + SEL16_MASTER) (EMI_MSEL8[15:0])** Will keep to the maximum when reached.

10203580 **EMI_TTYPE 17** **EMI 17th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE17_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE17_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE17_CNT	**17th counter for number of a transaction type of selected masters (SEL17_TRANS_TYPE + SEL17_MASTER) (EMI_MSEL8[31:16])** Will keep to the maximum when reached.

10203588 **EMI_TTYPE 18** **EMI 18th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE18_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE18_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:0	TTYPE18_CNT	**18th counter for number of a transaction type of selected masters (SEL18_TRANS_TYPE + SEL18_MASTER) (EMI_MSEL9[15:0])** Will keep to the maximum when reached.

10203590 **EMI_TTYPE 19** **EMI 19th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE19_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE19_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE19_CNT	**19th counter for number of a transaction type of selected masters (SEL19_TRANS_TYPE + SEL19_MASTER) (EMI_MSEL9[31:16])** Will keep to the maximum when reached.

10203598 **EMI_TTYPE 20** **EMI 20th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE20_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE20_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE20_CNT	**20th counter for number of a transaction type of selected masters (SEL20_TRANS_TYPE + SEL20_MASTER) (EMI_MSEL10[15:0])** Will keep to the maximum when reached.

102035A0 **EMI_TTYPE 21** **EMI 21st Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE21_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE21_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:0	TTYPE21_CNT	**21st counter for number of a transaction type of selected masters (SEL21_TRANS_TYPE + SEL21_MASTER) (EMI_MSEL10[31:16])** Will keep to the maximum when reached.

102035E0 **EMI_WP_ADR** **Watch Point Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**EMI_WP_ADR[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EMI_WP_ADR[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EMI_WP_ADR	Watch point address

102035E8 **EMI_WP_CTRL** **Watch Point Range** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**WP_INT_EN**	**NON_ALIGN_CHK_INT_EN**	**LOCK_CHK_INT_EN**	**ADR_CHK_INT_EN**		**EMI_WP_SLVERR**	**WP_WR_DIS**	**WP_RD_DIS**	**EMI_WP_TYPE**		**EMI_WP_RANGE**					
Type	RW	RW	RW	RW		RW	RW	RW	RW		RW					
Reset	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	WP_INT_EN	**Enables watch point hit interrupt**
14	NON_ALIGN_CHK_INT_EN	**Enables AXI non-32B align check interrupt**
13	LOCK_CHK_INT_EN	**Enables AXI Lock command issue check interrupt.**
12	ADR_CHK_INT_EN	**Enables AXI address violation (corss 4KB boundary) interrupt**
10	EMI_WP_SLVERR	**Watch point hit return slave error**
9	WP_WR_DIS	**Write hit watch point** EMI does not write data to DRAM.
8	WP_RD_DIS	**Read hit watch point** EMI does not read data from DRAMC and returns 0 to master.
7:6	EMI_WP_TYPE	**Checks watch point read/write** 11: Check read and write

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Bit(s)	Name	Description
5:0	EMI_WP_RANGE	01: Check read only 10: Check write only **Watch point range:** 4: 16-byte range (check EMP_WP_ADR[31:4]) 5: 32-bytes range (check EMP_WP_ADR[31:5]) 6: 64-bytes range (check EMP_WP_ADR[31:6]) ... 32: 4G-byte range Others: Illegal

102035F0 EMI_CHKER EMI AXI Checker 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**WP_HIT**	**AXI_NON_ALIGN_ISSUE**	**AXI_Lock_issue**	**AXI_ADR_VIO**	**AXI_VIO_WR**			**VIO_CLR**	**NON_ALIGN_CHK_MST**				**WP_EN**	**NON_ALIGN_CHK_EN**	**LOCK_CHK_EN**	**ADR_CHK_EN**
Type	RO	RO	RO	RO	RO			W1C	RW				RW	RW	RW	RW
Reset	0	0	0	0	0			0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AXI_VIO_ID**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	WP_HIT	**AXI hit watch point range**
30	AXI_NON_ALIGN_ISSUE	**AXI non-align command issue**
29	AXI_Lock_issue	**AXI Lock command issue**
28	AXI_ADR_VIO	**AXI address violation (cross 4KB boundary).**
27	AXI_VIO_WR	**AXI violation (lock or cross 4KB boundary) access type** 0: Read 1: Write
24	VIO_CLR	**Violation information (bit 29..16 and EMI_CHKER_ADR) cleared to 0**
23:20	NON_ALIGN_CHK_MST	**AXI non-32B align check master number** 0~7: Port 0~7 8: All ports
19	WP_EN	**Enables watch point**
18	NON_ALIGN_CHK_EN	**Checks AXI non-32B align**
17	LOCK_CHK_EN	**Enables AXI Lock command issue checker**
16	ADR_CHK_EN	**Enables AXI address violation (cross 4KB boundary) checker**
15:0	AXI_VIO_ID	**AXI violation (lock or cross 4KB boundary) ID**

102035F4 EMI_CHKER_TYPE EMI AXI Checker Type 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AXI_CHECKER_TYP							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	AXI_CHECKER_TYP	[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat [6:4]: 000 ~ 100: 1/2/4/8/16-byte [7]: 0/1 Burst type: WRAP/INCR

102035F8 **EMI_CHKER_ADR** **EMI AXI Checker Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AXI_VIO_ADR[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AXI_VIO_ADR[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AXI_VIO_ADR	Issues AXI lock command

3.6.5 Programming Guide

To start EMI function, program the settings in the following manner.

1. Program supporting one channel DRAM.
2. Program DRAM address mapping type, e.g. column bit number, row bit number and bank bit number. Put the address map as “row, ban, chn, col” or “ban[2], row, ban[1:0], chn, col” or “row, ban, col”.
3. Set the DRAM bit number to 16 bits or 32 bits data bus.
4. Program the latency for each AXI interface of which the request will be set to high priority when the age counter expires. (In the beginning, treat all the requests from one AXI port as the same ID.)
5. Allocate the bandwidth requirement for each AXI port and set up the bandwidth limiter value. Next, guarantee that the total bandwidth set does not exceed 100%.
6. Set up the bandwidth limiter for each AXI ports as soft limit or hard limit.
7. Program the security region addresses and numbers.

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3.7 DRAM Controller

3.7.1 Overview

DRAM controller supports the following DRAM bus configuration:

1. LPDDR2 32-bit @ 533MHz (1,066M bps/per bit channel)
2. LPDDR3 32-bit @ 667MHz (1,333M bps/per bit channel)

See the table below for the DRAM bus signals:

Table 3-5. DRAM bus signal list (refer to DRAMC side)

Signal name	Type	Description
CK0/CK1	Input	DRAM clock signal
CK0#/CK1#	Input	DRAM clock invert signal
MA[9:0]	Input	Address for all memories/CA bus for LPDDR2/3
CKE	Input	Clock enable signal for DRAM
CS# [1:0]	Input	RANK1~RANK0 selection signal
DQ[31:0]	I/O	Data bus for LPDDR2/LPDDR3
DQM[1:0]	Input	Data mask
DQS[3:0]	I/O	Data strobe
DQS#[3:0]	I/O	Differential data strobe in LPDDR2/3
REXTDN	I/O	Output driving calibration

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See below for the DRAM bus command truth table:

Table 3-6. DRAM bus command truth table (LPDDR2/3)

		SDR Command Pins			DDR CA pins (10)										
SDRAM Command	NVM Command	CKE		CS_N	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CK_t EDGE
		CK_t(n-1)	CK_t(n)												
MRW	MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	↑
				X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	↓
MRR	MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	↑
				X	MA6	MA7	X								↓
Refresh (per bank)[11]	-	H	H	L	L	L	H	L	X						↑
				X	X										↓
Refresh (all bank)	-	H	H	L	L	L	H	H	X						↑
				X	X										↓
Enter Self Refresh	Enter Power Down	H	L	L	L	L	H	X							↑
		X		X	X										↓
Activate (bank)	Activate (row buffer)	H	H	L	L	H	R8/a15	R9/a16	R10/a17	R11/a18	R12/a19	BA0	BA1	BA2	↑
				X	R0/a5	R1/a6	R2/a7	R3/a8	R4/a9	R5/a10	R6/a11	R7/a12	R13/a13	R14/a14	↓
Write (bank)	Write (RDB)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
				X	AP[3,4]	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
Read (bank)	Read (RDB)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
				X	AP[3,4]	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
Precharge (pre bank, all bank)	Preactive (RAB)	H	H	L	H	H	L	H	AB/a30	X/a31	X/a32	BA0	BA1	BA2	↑
				X	X/a20	X/a21	X/a22	X/a23	X/a24	X/a25	X/a26	X/a27	X/a28	X/a29	↓
BST	BST	H	H	L	H	H	L	L	X						↑
				X	X										↓
Enter Deep Power Down	Enter Power Down	H	L	L	H	H	L	X							↑
		X		X	X										↓
NOP	NOP	H	H	L	H	H	H	X							↑
				X	X										↓
Maintain PD, SREF, DPD (NOP)	Maintain Power Down (NOP)	L	L	L	H	H	H	X							↑
				X	X										↓
NOP	NOP	H	H	H	X										↑
				X	X										↓
Maintain PD, SREF, DPD (NOP)	Maintain Power Down (NOP)	L	L	H	X										↑
				X	X										↓
Enter Power Down	Enter Power Down	H	L	H	X										↑
		X		X	X										↓
Exit PD, SREF, DPD	Exit Power Down	L	H	H	X										↑
		X		X	X										↓

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These tables are applied when CKE is asserted at the clock cycle before CS# is asserted. Read and write accesses to the DDR SDRAM are burst oriented. The accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. The accesses begin with the registration of an ACTIVE command, followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

As with standard SDRAMs, the pipelined, multi-bank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

The DDR SDRAM operates from a differential clock (CK and CK#). Commands (address and control signals) are registered at every positive and negative edges of CK for LPDDR2/3. The input data are registered on both edges of DQS, and the output data are referenced to both edges of DQS, as well as to both edges of CK. DQS is center-aligned with data for WRITEs. Without DLL inside mobile DRAM's (LPDDR2/3), DQS is not edge-aligned with data for READs.

The commands for LPDDR2/3 SDRAM are encoded in MA0 ~ MA9 and transfer at double rate of clock frequency such as DQ.

Other key points of Denali DRAM controller:

- Supports column address bit number from 8 to 11
- Supports DRAM burst length 4 and 8
- Supports maximum LPDDR2/3 8G-bit device

3.7.2 Features

- 128-bit data bus interface with BE[15:0] for write data mask
- LEN has 4-bit, 0 ~ 15 DLE's/WDLE's
- Supports END_SIZE for optimize utilization rate
- Supports WDLE for split transaction
- Supports HDLE (DLE64) side band signal for early responses
- Supports high-priority side band signal for reducing request latency
- A request cannot cross page boundary
- Supports 2X frequency mode (frequency ratio of DRAMC:DRAM = 1:2) for timing optimization
- Supports dual-scheduler function for 1T command rate under 2X frequency mode for performance optimization
- Supports power-down and self-refresh for power saving
- Supports clock stop for power saving
- Supports input DQS/DQ timing calibration for PVT variation
- Supports read/write command out of order control

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3.7.2.1 Reference

- LPDDR2 spec: http://www.jedec.org/download/search/JESD209-2.pdf

3.7.3 Block Diagram

The major blocks of DRAM controller are command decoder, command pool, bus scheduler, timing controller DDR PHY and response generator.

The requests from Arbiter are pushed to command pool to wait for execution in order. The bus scheduler inspects the precharge/active pool and command FIFO and decides which DRAM bus command, e.g. PRECHARGE, ACTIVE, READ or WRITE, is issued to the DRAM bus. The goals of bus scheduler are to raise the bus utilization rate and lower the response latency. The timing control unit is responsible for the integrity of DRAM bus timing such as pre-charge to active delay (tRP), active to command delay (tRCD) and bus turnaround time. The bus scheduler refers to the information and choose the next DRAM bus command. The DRAM interface unit is responsible for generating DRAM bus commands, transmitting data and DQS to DDR DRAM and receiving data and DQS from DDR DRAM. The response generator produces the response signals for all DRAM agents such as DLE and RDAT.

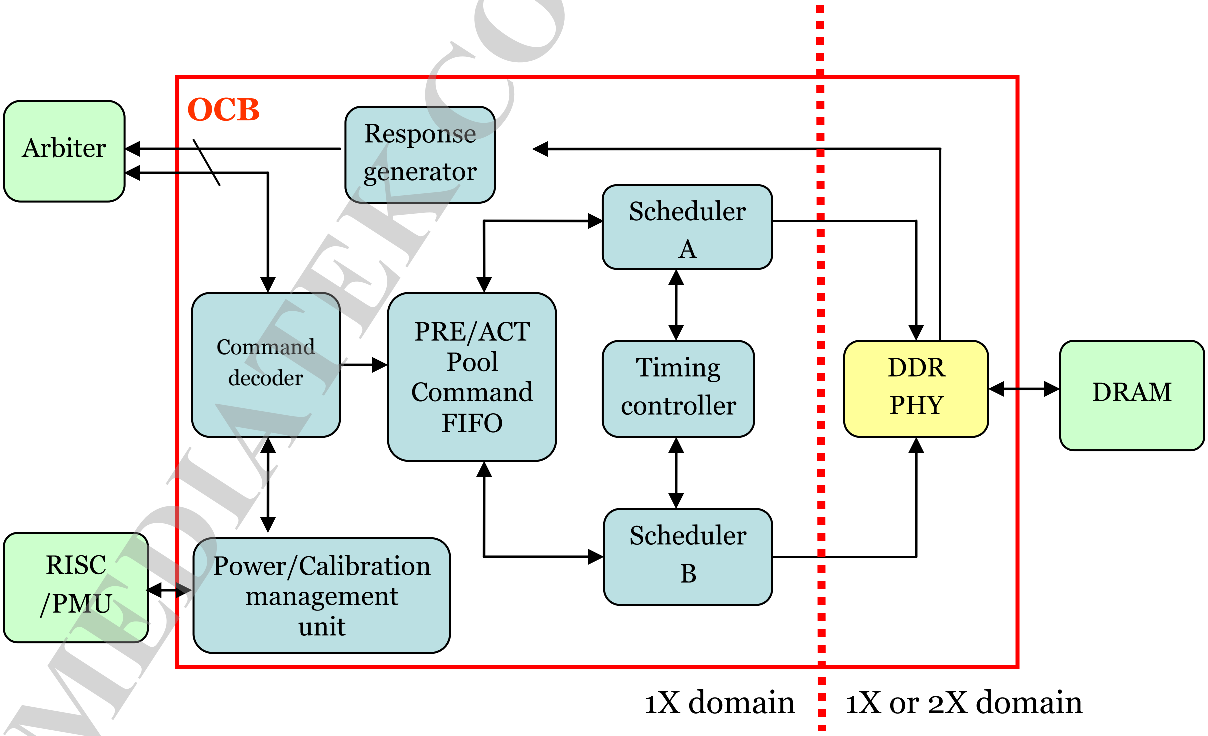

Figure 3-9. Block diagram of DRAM controller

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3.7.4 Register Definition

10214000 ACTIM0 DRAM AC Timing Setting 0 22564154

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TRCD				TRP				TFAW				TWR			
Type	RW				RW				RW				RW			
Reset	0	0	1	0	0	0	1	0	0	1	0	1	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BL2	REG_00_DUMMY		CL2	TWTR				TRC				TRAS			
Type	RW	RW		RW	RW				RW				RW			
Reset	0	1		0	0	0	0	1	0	1	0	1	0	1	0	0

Bit(s)	Mnemonic	Name	Description
31:28	**TRCD**	TRCD	**tRCD Timing setting** tRCD = (1 + TRCD) DRAMC clock cycles Note: DRAMC clock = 2*DRAM clock when FDIV2 (0x7c[0]) = 1 DRAMC clock = 1*DRAM clock when FDIV2 (0x7c[0]) = 0
27:24	**TRP**	TRP	**tRP timing setting** tRP = (1 + TRP) DRAMC clock cycles
23:20	**TFAW**	TFAW	**tFAW timing setting** tFAW = (8 + TFAW) DRAMC clock cycles Note: 0x1e8[1] is added for TFAW[4].
19:16	**TWR**	TWR	**tWR timing setting** For LPDDR2/DDR3: Write command to precharge command TWR >= WL + tDQSS + (BL)/2 + tWR For LPDDR1: Last data-in to precharge command tWR = (1 + TWR) DRAMC clock cycles
15	**BL2**	BL2	**When FDIV2 (0x7c[0]) = 1, 1 for burst length 4** When FDIV2 (0x7c[0]) = 0, set this to 0
14	**REG_00_DUMMY**	REG_00_DUMMY	**Dummy registers**
12	**CL2**	CL2	**CAS latency timing setting for DDR1** CAS latency = 2
11:8	**TWTR**	TWTR	**tWTR timing setting** tWTR = (1 + TWTR) DRAMC clock cycles under LPDDR1 (WL + BL/2 + 1 + tWTR) = (3 + TWTR) DRAMC clock cycles under LPDDR2/DDR3 Note: The TWTR value must be smaller than or equal to 3 under LPDDR1; smaller than or equal to 'ha under other memories.
7:4	**TRC**	TRC	**tRC timing setting** tRC = (8 + TRC) DRAMC clock cycles Note: 0x1e8[0] is added for TRC[4].
3:0	**TRAS**	TRAS	**tRAS timing setting** tRAS = (8 + TRAS) DRAMC clock cycles

10214004 CONF1 DRAM Configuration 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SREF_CK_DLY		TCKESRX		TEST LP	SELF REF				TCMD						

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Type	RW		RW		RW	RW				RW						
Reset	0	0	0	0	0	0				0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CKEON**		**FW2R**			**BL4**	**MATYPE**		**TRRD**				**PAGDIS**			**DM64BITEN**
Type	RW		RW			RW	RW		RW				RW			RW
Reset	0		0			0	0	0	0	0			0			0

Bit(s)	Mnemonic	Name	Description
31:30	**SREF_CK_DLY**	SREF_CK_DLY	**For self-refresh clock stop timing**
29:28	**TCKESRX**	TCKESRX	**Add tCKESRX margin for pcddr3 mode** -TCKESRX=0 6 dram_clock -TCKESRX=1 8 dram_clock -TCKESRX=2 10 dram_clock -TCKESRX=3 12 dram_clock
27	**TESTLP**	TESTLP	**Infinite self test loop enabling for test agent 1** 0: Disable loop 1: Enable loop
26	**SELFREF**	SELFREF	**Enables self-refresh mode** 0: Disable 1: Eanble self-refresh
22:20	**TCMD**	TCMD	**Test command** TCMD[2]: RAS_ TCMD[1]: CAS_ TCMD[0]: WE_
15	**CKEON**	CKEON	**Enables CKE function** 0: Disable power-down function. CKE will keep high. 1: Enable power-down function. CKE will go down when idle.
13	**FW2R**	FW2R	**Fast write to read turnaround time (for DDR-I only)** 0: Turnaround time is 0T. 1: Turnaround time is 1T.
10	**BL4**	BL4	**When FDIV2 (0x7c[0]) = 0** 0: Burst length 8 1: DRAM burst length 4 When FDIV2 (0x7c[0]) = 1 0: Reserved 1: DRAM burst length 8 When FDIV2 (0x7c[0]) = 1, set 0x00[15] = 1 for burst length 4 .
9:8	**MATYPE**	MATYPE	**DRAM column address width** 00: 8 bits 01: 9 bits 10: 10 bits 11: 11 bits
7:6	**TRRD**	TRRD	**tRRD timing setting** tRRD = (1 + TRRD) DRAMC clock cycles Note: 0x1e8[3] is added for TRRD[2].
3	**PAGDIS**	PAGDIS	**Disables page mode** 0: Disable page mode. Every transaction is page-miss. 1: Enable page mode. Page will keep opening after being accessed.
0	**DM64BITEN**	DM64BITEN	**DDR:** When FDIV2 (0x7c[0]) = 0, 0: 32-bit DRAM 1: 64-bit DRAM When FDIV2 (0x7c[0]) = 1, 0: 16-bit DRAM

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Bit(s)	Mnemonic	Name	Description
			1: 32-bit DRAM

10214008 CONF2 DRAM Configuration 2 10000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TEST2W	TEST2R	TEST1	REFDIS		REFTHD			FREBWEN						FREBW[9:8]	
Type	RW	RW	RW	RW		RW			RW						RW	
Reset	0	0	0	1		0	0	0	0						0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREBW[7:0]								REFCNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**TEST2W**	TEST2W	**Enables Test Agent 2 write** 0: Disable write cycle 1: Enable write cycle
30	**TEST2R**	TEST2R	**Enables Test Agent 2 read** 0: Disable read cycle 1: Enable read cycle
29	**TEST1**	TEST1	**Enables Test Agent 1** 0: Disable test agent 1 1: Enable test agent 1
28	**REFDIS**	REFDIS	**Disables refresh** 0: Enable 1: Disable
26:24	**REFTHD**	REFTHD	**Refresh threshold value for promoting refresh request to high-priority** 0 means always high-priority
23	**FREBWEN**	FREBW_FREN	**Enables tREFBW use xtal clock counter**
17:8	**FREBW**	FREBW_FR	**6720ns/(XTALFR_clock) -1**
7:0	**REFCNT**	REFCNT	**Refresh period = (REFCNT*16) DRAMC clock cycles** Set the value according to DRAM spec and DRAMC frequency.

10214018 R0DELDLY RANK0 DQS Input Delay Chain Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DEL3DLY								DEL2DLY						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DEL1DLY								DEL0DLY						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:24	**DEL3DLY**	DEL3DLY	**RANK0 DQS3 input delay line setting** Total delay in typical case = (0.03*DEL3DLY) ns
22:16	**DEL2DLY**	DEL2DLY	**RANK0 DQS2 input delay line setting** Total delay in typical case = (0.03*DEL2DLY) ns

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Bit(s)	Mnemonic	Name	Description
14:8	**DEL1DLY**	DEL1DLY	**RANK0 DQS1 input delay line setting** Total delay in typical case = (0.03*DEL1DLY) ns
6:0	**DEL0DLY**	DEL0DLY	**RANK0 DQS0 input delay line setting** Total delay in typical case = (0.03*DEL0DLY) ns

1021401C <u>R1DELDLY</u> RANK1 DQS Input Delay Chain Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DEL7DLY								DEL6DLY						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name		DEL5DLY								DEL4DLY						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:24	**DEL7DLY**	DEL7DLY	**RANK1 DQS3 input delay line setting** Total delay in typical case = (0.03*DEL7DLY) ns
22:16	**DEL6DLY**	DEL6DLY	**RANK1 DQS2 input delay line setting** Total delay in typical case = (0.03*DEL6DLY) ns
14:8	**DEL5DLY**	DEL5DLY	**RANK1 DQS1 input delay line setting** Total delay in typical case = (0.03*DEL5DLY) ns
6:0	**DEL4DLY**	DEL4DLY	**RANK1 DQS0 input delay line setting** Total delay in typical case = (0.03*DEL4DLY) ns

10214020 <u>R0DIFDLY</u> RANK0 DQS Input Delay Chain Offset Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DIF3DLY								DIF2DLY						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name		DIF1DLY								DIF0DLY						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:24	**DIF3DLY**	DIF3DLY	**RANK0 offset of DQS3 input delay line setting for auto mode** Total delay in typical case = [0.03*(DIF3DLY + DLLCNT)]ns, binary-coded
22:16	**DIF2DLY**	DIF2DLY	**RANK0 offset of DQS2 input delay line setting for auto mode** Total delay in typical case = [(0.03*(DIF2DLY + DLLCNT)]ns, binary-coded
14:8	**DIF1DLY**	DIF1DLY	**RANK0 offset of DQS1 input delay line setting for auto mode** Total delay in typical case = [0.03*(DIF1DLY + DLLCNT)]ns, binary-coded
6:0	**DIF0DLY**	DIF0DLY	**RANK0 offset of DQS0 input delay line setting for auto**

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Bit(s)	Mnemonic	Name	Description
			mode Total delay in typical case = [0.03*(DIF0DLY + DLLCNT)]ns, binary-coded

10214024 R1DIFDLY RANK1 DQS Input Delay Chain Offset Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DIF7DLY								DIF6DLY						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DIF5DLY								DIF4DLY						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:24	**DIF7DLY**	DIF7DLY	**RANK1 offset of DQS3 input delay line setting for auto mode** Total delay in typical case = [0.03*(DIF7DLY + DLLCNT)]ns, binary-coded
22:16	**DIF6DLY**	DIF6DLY	**RANK1 offset of DQS2 input delay line setting for auto mode** Total delay in typical case = [0.03*(DIF6DLY + DLLCNT)]ns, binary-coded
14:8	**DIF5DLY**	DIF5DLY	**RANK1 offset of DQS1 input delay line setting for auto mode** Total delay in typical case = [0.03*(DIF5DLY + DLLCNT)]ns, binary-coded
6:0	**DIF4DLY**	DIF4DLY	**RANK1 offset of DQS0 input delay line setting for auto mode** Total delay in typical case = [0.03*(DIF4DLY + DLLCNT)]ns, binary-coded

10214028 DLLCONF DLL Configuration 8000FF01

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REG_28_DUMMY1	DLLFRZ		MDQS												
Type	RW	RW		RW												
Reset	1	0		0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REG_28_DUMMY0															
Type	RW															
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31	**REG_28_DUMMY1**	REG_28_DUMMY1	**Dummy registers**
30	**DLLFRZ**	DLLFRZ	**Auto-calibration value update when refreshing cycle** 0: Disable 1: Enable

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Bit(s)	Mnemonic	Name	Description
28	**MDQS**	MDQS	**Manual mode for DQS input delay setting** 0: Auto set DQS input delay by DLL 1: Manually set DQS input delay by register
15:0	**REG_28_DUMMY0**	REG_28_DUMMY0	**Dummy registers**

10214044 TEST2_3 Test Agent 2 Configuration 3 08000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**ADVPREEN**	**ADVREFEN**	**DMPGTIM**										**TRFC**			
Type	RW	RW	RW										RW			
Reset	0	0	0	0	1	0	0	0					0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**PERBIT**	**DQSUPDMODE**	**MANUDQSUPD**	**MANUDLLFRZ**	**DQDLYAUTO**	**DQSICALSTP**			**TESTAUDPAT**		**DQSICALUPD**	**DQSICALEN**	**TESTCNT**			
Type	RW	RW	RW	RW	RW	RW			RW		RW	RW	RW			
Reset	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**ADVPREEN**	ADVPREEN	**Enables advanced precharge function** When page is idle for DMPGTIM cycles, the page is closed automatically. 0: Disable advanced precharge function 1: Enable advanced precharge function
30	**ADVREFEN**	ADVREFEN	**Enables advanced refresh function** Used only for DDR3; DDR3 supports refresh pull-in function; refer DDR3 spec for details. 0: Disable advnaced precharge function 1: Enable advanced precharge function
29:24	**DMPGTIM**	DMPGTIM	**Advanced precharge function timer** Used with ADVPREEN. Unit: DRAMC clock
19:16	**TRFC**	TRFC	**tRFC timing setting** tRFC = (11 + TRFC[7:0]) DRAMC clock cycles Note: 0x1e8[7:4] is added for TRFC[7:4].
15	**PERBIT**	PERBIT	**Per Bit HW calibration**
14	**DQSUPDMODE**	DQSUPDMODE	**0: Original manual mode for DQS input delay** 1: Update manual DQS input delay only while MANUDQSUPD=1 and DLLFRZ
13	**MANUDQSUPD**	MANUDQSUPD	**Enables on-line manual DQS input delay adjustment** 0: Disable DQS input delay adjustment 1: Enable DQS input delay adjustment. New value will be updated during refresh period.
12	**MANUDLLFRZ**	MANUDLLFRZ	**Manual freeze DLL counter** 0: DLL counter will be updated by HW. 1: DLL counter will be frozen for SW reading.
11	**DQDLYAUTO**	DQDLYAUTO	**DQ delay auto-update during calibration** 0: No update 1: Update
10:8	**DQSICALSTP**	DQSICALSTP	**HW calibration step (=DQSICALSTP*2)**
7	**TESTAUDP**	TESTAUDPAT	**Selects audio pattern as test pattern of Test Agent 2**

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Bit(s)	Mnemonic	Name	Description
	AT		0: ISI pattern 1: Audio pattern
5	**DQSICALUPD**	DQSICALUPD	**Updates DQS input delay setting to calibrated value** 0: Disable update 1: Enable update
4	**DQSICALEN**	DQSICALEN	**Enables HW calibration** 0: Disable HW calibration 1: Enable HW calibration
3:0	**TESTCNT**	TESTCNT	**Test loop number of Test Agent 2** Loop number = 2^(TESTCNT)

10214048 TEST2_4 Test Agent 2 Configuration 4 0000110D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TZQCS															TESTXTALKPAT
Type	RW															RW
Reset	0	0	0	0	0	0	0	0								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TESTAUDMODE	TESTAUDBITINV		TESTAUDINIT							TEST2DISSCRAM	TESTAUDINC				
Type	RW	RW		RW							RW	RW				
Reset	0	0		1	0	0	0	1			0	0	1	1	0	1

Bit(s)	Mnemonic	Name	Description
31:24	**TZQCS**	TZQCS	**tZQCS timing setting** tZQCS = (2 + TZQCS) DRAMC clock cycles
16	**TESTXTALKPAT**	TESTXTALKPAT	**Selects cross-talk pattern as test pattern of Test Agent 2** 0: ISI pattern 1: Cross-talk pattern, when TESTAUDPAT = 0
15	**TESTAUDMODE**	TESTAUDMODE	**Enables audio pattern: Write after read** 0: Read only 1: Write after read
14	**TESTAUDBITINV**	TESTAUDBITINV	**Enables audio pattern bit inversion** 0: No bit inversion 1: Bit inversion
12:8	**TESTAUDINIT**	TESTAUDINIT	**Initial bit inverse position for audio pattern**
5	**TEST2DISSCRAM**	TEST2DISSCRAM	**Test agent bypass scramble function** 0: Does not bypass scramble function 1: Bypass scramble function
4:0	**TESTAUDINC**	TESTAUDINC	**Bit inverse incremental value for audio pattern**

1021404C CATRAINING CATRAINING Configuration 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CATRAINMRS	CATRAINEN	
Type														RW	RW	
Reset														0	0	

Bit(s)	Mnemonic	Name	Description
2	CATRAINMRS	CATRAINMRS	In CA training mode, set to 1 for MRW to MR41/MR48/MR42.
1	CATRAINEN	CATRAINEN	In CA training mode, set to 1 for CA training session and additional CA training session.

10214050 CATRAINING2 CATRAINING Configuration 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CATRAINCA_Y															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CATRAINCA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16	CATRAINCA_Y	CATRAINCA_Y	CA training pattern Y (YP0 and YP1) for MA[9:0]
15:0	CATRAINCA	CATRAINCA	CA training pattern X (XP0 and XP1) for MA[9:0]

10214054 WODT WODT Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						NORMPOP_LEN				WODTDEN	DISWODTE2	DISWODTE	DISWODT			WODTFIXOFF
Type						RW				RW	RW	RW	RW			RW
Reset						0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
10:8	NORMPOP_LEN	NORMPOP_LEN	**RX DQS/DQ calibration with normal read access cycle** Only valid when DQSICALI_NEW=1.
6	WODTDEN	WODTDEN	**Disables write ODT when DRAM is powered down** 1'b0: Enable this function 1'b1: Disable this function,
5	DISWODTE2	DISWODTE2	**Write ODT disabling extends 2T or not** 1'b1: Extend 2T
4	DISWODTE	DISWODTE	**Write ODT disabling extends 1T or not** 1'b1: Extend 1T

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Bit(s)	Mnemonic	Name	Description
3:1	**DISWODT**	DISWODT	**Write ODT disabling time after read** 3'b000: read_odt_enable 3'b001: read_odt_enable_syn1t 3'b010: read_odt_enable_syn2t
0	**WODTFIX OFF**	WODTFIXOFF	**Fixes write ODT to disable** For CA training or ZQ calibration. 1'b1: Fixed to disable ODT

1021407C **DDR2CTL** **DDR2 Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RODTE**				**FIXRODT**	**RODT**				**TWODT**						
Type	RW				RW	RW				RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TR2W**					**TRTP**				**DATLAT**			**WOEN**	**ROEN**	**DDR2EN**	**FDIV2**
Type	RW					RW				RW			RW	RW	RW	RW
Reset	0	0	0	0		0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**RODTE**	RODTE	**Enables read ODT extend 1T mode** 0: Does not extend 1T 1: Extend 1T Unit: DRAM clock cycle
27	**FIXRODT**	FIXRODT	**Fix read cycle ODT signal** Fix the ODT signal value (to control the PAD termination) as always enabled 0: Not fixed on ODT 1: Fixed on ODT
26:24	**RODT**	RODT	**Read ODT timing control for DDR2** 000: For CL3 001: For CL4 and CL5 010: for CL6 and CL7
22:16	**TWODT**	TWODT	**Write ODT latency enabling for DDR2** 111111: For all cases Others: Reserved
15:12	**TR2W**	TR2W	**Read to write interval time = (TR2W[3:0] + 3) DRAMC clock cycles** TR2W values are the same when >= 'h9
10:8	**TRTP**	TRTP	**tRTP = (TRTP + 1) DRAMC clock cycle** In LPDDR, tRTP = BL/2, HW design guarantees it; no need to set up TRTP. In LPDDR2, tRTP begins (BL/2 - 2) clock cycles after the read command. In DDR3, precharge can be issued after AL + tRTP.
6:4	**DATLAT**	DATLAT	**Internal read data timing control** The register and 0xE4[4] (DATLAT3) 4'b0101: CL6, CL7 for DDR2 4'b0100: CL4, CL5 for DDR2 4'b0111: CL9, CL10 for GDDR3 4'b1000: CL11, CL12 for GDDR3
3	**WOEN**	WOEN	**Enables write ODT**

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Bit(s)	Mnemonic	Name	Description
			0: Disable Write ODT 1: Enable Write ODT
2	**ROEN**	ROEN	**Enables read ODT** 0: Disable Read ODT 1: Enable Read ODT
1	**DDR2EN**	DDR2EN	**Enables DDR2** 0: Disable DDR2 function 1: Enable DDR2 function
0	**FDIV2**	FDIV2	**Half frequency mode** 0: DRAMC clock cycle = DRAM clock cycle 1: DRAMC clock cycle = 2 * DRAM clock cycle

10214088 MRS MRS Value Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MRSRK					MRSOP							
Type				RW					RW							
Reset				0					0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MRSBA			MRSMA												
Type	RW			RW												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28	**MRSRK**	MRSRK	
23:16	**MRSOP**	MRSOP	**For LPDDR2 MRW's OP (MRS_OP[7:0])**
15:13	**MRSBA**	MRSBA	**For non-LPDDR2 MRW bank address**
12:0	**MRSMA**	MRSMA	**For MRR/MRW address**

1021408C CLK1DELAY Clock 1 Output Delay Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												DQ16COM1				
Type												RW				
Reset												0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DQCMD		CLK1DLY	
Type													RW		RW	
Reset													0		0	

Bit(s)	Mnemonic	Name	Description
20	**DQ16COM1**	DQ16COM1	**DDR3 16-bit data from MACRO_COM1, instead of MACRO_COM0** 0: Disable 1: Enable
3	**DQCMD**	DQCMD	**DQ16~31 as command/address output** 0: Disable 1: Enable
1	**CLK1DLY**	FIFOLEN1	**Read FIFO length in DDRPHY**

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Bit(s)	Mnemonic	Name	Description
			0: 8-level 1: 4-level

10214094 R0DQSIEN RANK0 DQS Input Range Fine Tuner 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		R0DQS3IEN								R0DQS2IEN						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		R0DQS1IEN								R0DQS0IEN						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:24	**R0DQS3IEN**	R0DQS3IEN	**RANK0 DQS3 gating delay control** DRAMC uses the gated DQS to sample DQ. To get the right gated DQS, the gating signal should be adjusted to match DRAM, PCB and other components. 1 step = 20ps.
22:16	**R0DQS2IEN**	R0DQS2IEN	**RANK0 DQS2 gating delay control**
14:8	**R0DQS1IEN**	R0DQS1IEN	**RANK0 DQS1 gating delay control**
6:0	**R0DQS0IEN**	R0DQS0IEN	**RANK0 DQS0 gating delay control**

10214098 R1DQSIEN RANK1 DQS Input Range Fine Tuner 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		R1DQS3IEN								R1DQS2IEN						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		R1DQS1IEN								R1DQS0IEN						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:24	**R1DQS3IEN**	R1DQS3IEN	**RANK1 DQS3 gating delay control** DRAMC uses the gated DQS to sample DQ. To get the right gated DQS, the gating signal should be adjusted to match DRAM, PCB and other components. 1 step = 20ps.
22:16	**R1DQS2IEN**	R1DQS2IEN	**RANK1 DQS2 gating delay control**
14:8	**R1DQS1IEN**	R1DQS1IEN	**RANK1 DQS1 gating delay control**
6:0	**R1DQS0IEN**	R1DQS0IEN	**RANK1 DQS0 gating delay control**

102140B4 DRVCTL00 Pad Driving Control Setting 00 AA00AA00

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REG_B4_DUMMY1															
Type	RW															
Reset	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQCDRVP				DQCDRVN				REG_B4_DUMMY0							
Type	RW				RW				RW							
Reset	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16	**REG_B4_DUMMY1**	REG_B4_DUMMY1	**Dummy registers**
15:12	**DQCDRVP**	DQCDRVP	**DQ16-31 P driving control** **Refer to IBIST model for driving strength.**
11:8	**DQCDRVN**	DQCDRVN	**DQ16-31 N driving control** **Refer to IBIST model for driving strength.**
7:0	**REG_B4_DUMMY0**	REG_B4_DUMMY0	**Dummy registers**

102140B8 DRVCTL0 Pad Driving Control Setting 0 AA00AA00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQSDRVP				DQSDRVN					DSODTP				DSODTN		
Type	RW				RW					RW				RW		
Reset	1	0	1	0	1	0	1	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQDRVP				DQDRVN					DQODTP				DQODTN		
Type	RW				RW					RW				RW		
Reset	1	0	1	0	1	0	1	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
31:28	**DQSDRVP**	DQSDRVP	**DQS P driving control** **Refer to IBIST model for driving strength.**
27:24	**DQSDRVN**	DQSDRVN	**DQS N driving control** **Refer to IBIST model for driving strength.**
22:20	**DSODTP**	DSODTP	**DQSODT P driving control** **Refer to IBIST model for driving strength.**
18:16	**DSODTN**	DSODTN	**DQSODT N driving control** **Refer to IBIST model for driving strength.**
15:12	**DQDRVP**	DQDRVP	**DQ0-15 P driving control** **Refer to IBIST model for driving strength.**
11:8	**DQDRVN**	DQDRVN	**DQ0-15 N driving control** **Refer to IBIST model for driving strength.**
6:4	**DQODTP**	DQODTP	**DQODT P driving control** **Refer to IBIST model for driving strength.**
2:0	**DQODTN**	DQODTN	**DQODT N driving control** **Refer to IBIST model for driving strength.**

102140C0 DLLSEL DLL Selection Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DLL67SEL		DLL45SEL		DLL23SEL		DLL01SEL		DLLCNTSEL		AUTOKMODE		CMPEN			

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Type	RW		RW		RW		RW		RW		RW		RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CMPDRVP				CMPDRVN					CMPODTP						
Type	RW				RW					RW						
Reset	0	0	0	0	0	0	0	0		0	0	0				

Bit(s)	Mnemonic	Name	Description
31:30	**DLL67SEL**	DLL67SEL	**Selects DLL6 and DLL7 counter**
29:28	**DLL45SEL**	DLL45SEL	**Selects DLL4 and DLL5 counter**
27:26	**DLL23SEL**	DLL23SEL	**Selects DLL2 and DLL3 counter**
25:24	**DLL01SEL**	DLL01SEL	**Selects DLL0 and DLL1 counter**
23:22	**DLLCNTSEL**	DLLCNTSEL	**Selects DLL counter** Refer the previous bit fields for meaning
21:20	**AUTOKMODE**	AUTOKMODE	**Selects OCD/ODT calibration mode** 00: Disable auto calibration 01: DRVP mode 10: DRVN mode 11: ODTP mode
19	**CMPEN**	CMPEN	**Enables compensation counter** 0: dDisable 1: Enable
15:12	**CMPDRVP**	CMPDRVP	**Connects to CMP pad DRVP[3:0]**
11:8	**CMPDRVN**	CMPDRVN	**Connects to CMP pad DRVN[3:0]**
6:4	**CMPODTP**	CMPODTP	**CMP ODT P driving control**

102140D8 MCKDLY Memory Clock Delay Chain Setting 00000900

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PINMUX			_16BITFULL						ODTREN			DISDQIEN			
Type	RW			RW						RW			RW			
Reset	0	0		0						0			0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIXDQIEN				REG_D8_DUMMY											
Type	RW				RW											
Reset	0	0	0	0	1	0	0	1								

Bit(s)	Mnemonic	Name	Description
31:30	**PINMUX**	PINMUX	**PINMUX function (S1, S0)** If (F0.30 ==1'b0), 00: Default 01: LPDDR2 10: LPDDR3 11: DDR3_16B Else (F0.30 ==1'b1), 00: LPDDR2/LPDDR3 pop/SBS 01: DDR3 x8 10: DDR3 x16 11: DDR3 x32
28	**_16BITFULL**	_16BITFULL	**DRAM bus is 16-bit and FDIV2 = 0**
22	**ODTREN**	ODTREN	**Turns on write ODT when reading** 0: Disable

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Bit(s)	Mnemonic	Name	Description
			1: Enable
19:16	**DISDQIEN**	DISDQIEN	**Disables DQ input enabling** 0: DQ input enable when necessary 1: DQ input disable
15:12	**FIXDQIEN**	FIXDQIEN	**DQ input enabled fixed mode** 0: DQ input enable when necessary 1: Keep DQ input always on
11:8	**REG_D8_DUMMY**	REG_D8_DUMMY	**Dummy registers**

102140E0 DQSCTL1 DQS Input Range Control 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DQSIENMODE		DQSINCTL										
Type				RW		RW										
Reset				0		0	0	0								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
28	**DQSIENMODE**	DQSIENMODE	**Selects DQS gating mode** 0: Pulse mode 1: Burst mode
26:24	**DQSINCTL**	DQSINCTL	**DQS input range control by M_CK** 0/1/ .../7 = delay 0/1/ .../7T Unit: DRAMC clock cycle

102140E4 PADCTL4 Pad control 4 00000200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name							PBREF_DISBYREFNUM		DDR3EN	ZQCSEN	BC4OTF	DATLAT3	CKEFIXOFF	CKEFIXON	GDDR3RST	CKEBYCTL
Type							RW		RW	RW	RW	RW	RW	RW	RW	RW
Reset							1		0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
9	**PBREF_DISBYREFNUM**	PBREF_DISBYREFNUNUM	**Disables perbank refresh when queue exceeds threshold**
7	**DDR3EN**	DDR3EN	**Enables DDR3 mode** 0: Not enable DDR3 1: Enable

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Bit(s)	Mnemonic	Name	Description
6	**ZQCSEN**	ZQCSEN	**Enables ZQCS (ZQ calibration short), for DDR3 only** 0: Disable 1: Enable
5	**BC4OTF**	BC4OTF	**Burst chop 4 on the fly mode** 0: Disable 1: Enable
4	**DATLAT3**	DATLAT3	**Read data latch timing control bit 3**
3	**CKEFIXOFF**	CKEFIXOFF	**CKE always off** 0: CKE hardware control 1: CKE always off
2	**CKEFIXON**	CKEFIXON	**CKE always on** 0: CKE hardware control 1: CKE always on
1	**GDDR3RST**	GDDR3RST	**Enables GDDR3/DDR3 reset pin** 0: Disable reset 1: Enable reset
0	**CKEBYCTL**	CKEBYCTL	**CKE control by hardware configuration or by controller** 0: Bby hardware configuration 1: By controller

102140F0 PHYCTL1 DDR PHY Control 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DQ4BMUX**	**PINMUX2**														
Type	RW	RW														
Reset	0	0														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**DCMCOMSEL**
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
31	**DQ4BMUX**	DQ4BMUX	**DQ 4-bit multiplex for LPDDR2/3, DDR3** 0: Disable 1: Enable
30	**PINMUX2**	PINMUX2	**PINMUX function (S2)** If (F0.30 = 1'b0), 00: Default 01: LPDDR2 10: LPDDR3 11: DDR3_16B Else (F0.30 = 1'b1), 00: LPDDR2/LPDDR3 pop/SBS 01: DDR3 x8 10: DDR3 x16 11: DDR3 x32
0	**DCMCOMSEL**	DCMCOMSEL	**Comb clock gating in refresh cycle when DCM is enabled**

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102140F4 GDDR3CTL1 GDDR3 Control 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RFRINTEN	RFRINTCTL	RDATRST	_8BKEN	PHY_SYNC_MASK	DAT_SYNC_MASK	GT_SYNC_MASK	GTDMW_SYNC_MASK				
Type					RW	RW	RW	RW	RW	RW	RW	RW				
Reset					0	0	0	0	0	0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
27	RFRINTEN	RFRINTEN	**Enables refresh-rate interrupt control for LPDDR2** 0: Disable 1: Enable
26	RFRINTCTL	RFRINTCTL	**Refresh-rate interrupt control** 0: Interrupt occrus at refresh-rate group change, {x4/x2/x1}, {x0.25}, {x0.125}. 1: Interrupt occurs at every refresh-rate change.
25	RDATRST	RDATRST	**Resets read data counter** 0: Disable 1: Enable reset
24	_8BKEN	_8BKEN	**Enables 8-bank device** 0: For 4-bank device 1: For 8-bank device
23	PHY_SYNC_MASK	PHY_SYNC_MASK	**Auto updates dqsien fine-tune value** By dummy write 0: Enable 1: Disable
22	DAT_SYNC_MASK	DAT_SYNC_MASK	**Auto updates value with bus-ck gating control** 0: Enable 1: Disable
21	GT_SYNC_MASK	GT_SYNC_MASK	**Auto triggers DATRST (exits self-refresh)** 0: Enable 1: Disable
20	GTDMW_SYNC_MASK	GTDMW_SYNC_MASK	**Auto triggers PHY_RESET (exits self-refresh)** 0: Enable 1: Disable

102140F8 PADCTL7 Pad control 7 EDCB0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REG_F8_DUMMY															
Type	RW															
Reset	1	1	1	0	1	1	0	1	1	1	0	0	1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							DRAMOEN	LBTEST								
Type							RW	RW								
Reset							0	0								

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Bit(s)	Mnemonic	Name	Description
31:16	**REG_F8_DUMMY**	REG_F8_DUMMY	**Dummy registers**
9	**DRAMOEN**	DRAMOEN	**Enables DRAM pin output** 0: Disable, DRAM pin will be Hi-Z. 1: Enable
8	**LBTEST**	LBTEST	**Enables loop-back test mode** 0: Disable 1: Enable

102140FC **MISCTL0** **MISC Control 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			TXP		EMIPREEN	REFP_ARB_EN	REFA_ARB_EN	PBC_ARB_EN	PBC_ARB_E1T			ASYNCEN				
Type			RW		RW	RW	RW	RW	RW			RW				
Reset		0	0	0	0	0	0	0	0			0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
30:28	**TXP**	TXP	**tXP timing setting** tXP = (2 + TXP) DRAMC clock cycles
27	**EMIPREEN**	EMIPREEN	**Enables advanced precharge function by EMI side-band signals** Note: This function is valid only when ADVPREEN is enabled. 0: Disable 1: Enable
26	**REFP_ARB_EN**	REFP_ARB_EN	**Per-bank refresh blocks EMI arbitration** 0: Disable 1: Enable
25	**REFA_ARB_EN**	REFA_ARB_EN	**All-bank refresh blocks EMI arbitration** 0: Disable 1: Enable
24	**PBC_ARB_EN**	PBC_ARB_EN	**Block page-miss requests in EMI arbitration** 0: Disable 1: Enable
23	**PBC_ARB_E1T**	PBC_ARB_E1T	**Early de-assertion of blocking page-miss requests 1T in EMI arbitration** 0: Disable 1: Enable
20	**ASYNCEN**	ASYNCEN	**Asynchronous mode enabling between DRAMC & DDRPHY** 0: Synchronous mode 1: Asynchronous mode

10214100 **OCDK** **OCD Calibration Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDATKEY	WDATKEY		WDATITL	WDATKEY	WDATKEY		DRVREF	WDATKEY	WDATKEY			WDATKEY	WDATKEY		

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	7	6		V	5	4			3	2			1	0		
Type	RW	RW		RW	RW	RW		RW	RW	RW			RW	RW		
Reset	0	0		0	0	0		0	0	0			0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DRDELSWEN				DRDELSWSEL			AUTOCALDRV	AUTOKCNT							
Type	RW				RW			RW	RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**WDATKEY7**	WDATKEY7	**Data encryption key bit 7**
30	**WDATKEY6**	WDATKEY6	**Data encryption key bit 6**
28	**WDATITLV**	WDATITLV	**Enables data scramble** 0: Disable 1: Enable
27	**WDATKEY5**	WDATKEY5	**Data encryption key bit 5**
26	**WDATKEY4**	WDATKEY4	**Data encryption key bit 4**
24	**DRVREF**	DRVREF	**Driving change only when in refresh cycle** 0: Disable. Change will be applied directly. 1: Enable, Change will be applied during refresh.
23	**WDATKEY3**	WDATKEY3	**Data encryption key bit 3**
22	**WDATKEY2**	WDATKEY2	**Data encryption key bit 2**
19	**WDATKEY1**	WDATKEY1	**Data encryption key bit 1**
18	**WDATKEY0**	WDATKEY0	**Data encryption key bit 0**
15	**DRDELSWEN**	DRDELSWEN	**Enables DQS input delay switching for different ranks** 0: Disable 1: Enable
11:9	**DRDELSWSEL**	DRDELSWSEL	**Timing control of DQS input delay switching for different ranks** Unit: DRAMC clock
8	**AUTOCALDRV**	AUTOCALDRV	**OCD calibration** 0: Disable calibration 1: Enable calibration
7:0	**AUTOKCNT**	AUTOKCNT	**Auto calibration counter** Set up timer for calibration cycle. Unit: DRAMC clock

10214110 RKCFG Rank Configuration 0B051100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					REG_110_DUMMY	RKSIZE							XRTW2W		XRTW2R	
Type					RW	RW							RW		RW	
Reset					1	0	1	1					0	1	0	1

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**XRTR2W**				**XRTR2R**			**PBREFEN**			**MRS2RK**	**RKSWAP**	**RKMODE**		
Type		RW				RW			RW			RW	RW	RW		
Reset		0	0	1		0	0	1	0			0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27	**REG_110_DUMMY**	REG_110_DUMMY	**Dummy registers**
26:24	**RKSIZE**	RKSIZE	**Selects rank address** 000: ADDR[31] 001: ADDR[30] 010: ADDR[29] 011: ADDR[28] 100: ADDR[27] 101: ADDR[26] 110: ADDR[25] 111: ADDR[24]
19:18	**XRTW2W**	XRTW2W	**Cross rank timing W2W** Unit: DRAM controller clock
17:16	**XRTW2R**	XRTW2R	**Cross rank timing W2R** Unit: DRAM controller clock
14:12	**XRTR2W**	XRTR2W	**Cross rank timing R2W** Note: XRTR2W = 6/7 has the same setting. Unit: DRAM controller clock
10:8	**XRTR2R**	XRTR2R	**Cross rank timing R2R** Unit: DRAM controller clock
7	**PBREFEN**	PBREFEN	**Enables per-bank refresh for LPDDR2** 0: Disable 1: Enable
4	**MRS2RK**	MRS2RK	**MRS commands are sent to 2 ranks simulataneously** 0: Disable 1: Enable
3	**RKSWAP**	RKSWAP	**Swaps CS<->CS1** 0: Disable 1: Enable
2:0	**RKMODE**	RKMODE	**Supports multi-rank mode** Set to non-zero for multi-rank.

10214124 **DQSGCTL** **Input DQS Gating Control** **00000088**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**R1DQSG_COARSE_DLY_COM1**		**R0DQSG_COARSE_DLY_COM1**		**R1DQSG_COARSE_DLY_COM0**		**R0DQSG_COARSE_DLY_COM0**	
Type									RW		RW		RW		RW	
Reset									1	0	0	0	1	0	0	0

Bit(s)	Mnemonic	Name	Description
7:6	**R1DQSG_COARSE_DL**	R1DQSG_COARSE	**RANK1 coarse tune delay setting for DQS2/3 gating signal**

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Bit(s)	Mnemonic	Name	Description
	Y_COM1	_DLY_COM1	**before dummy PAD** Unit: 0.25/0.5T of DRAMC clock in 2X/1X mode
5:4	**R0DQSG_COARSE_DLY_COM1**	R0DQSG_COARSE_DLY_COM1	**RANK0 coarse tune delay setting for DQS2/3 gating signal before dummy PAD** Unit: 0.25/0.5T of DRAMC clock in 2X/1X mode
3:2	**R1DQSG_COARSE_DLY_COM0**	R1DQSG_COARSE_DLY_COM0	**RANK1 coarse tune delay setting for DQS0/1 gating signal before dummy PAD** Unit: 0.25/0.5T of DRAMC clock in 2X/1X mode
1:0	**R0DQSG_COARSE_DLY_COM0**	R0DQSG_COARSE_DLY_COM0	**RANK0 coarse tune delay setting for DQS0/1 gating signal before dummy PAD** Unit: 0.25/0.5T of DRAMC clock in 2X/1X mode

10214130 CLKENCTL DRAM Clock Enable Control 50000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**REG_130_DUMMY**	**CLK1EN**	**CLK0EN**												
Type		RW	RW	RW												
Reset		1	0	1												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
30	**REG_130_DUMMY**	REG_130_DUMMY	**Dummy registers**
29	**CLK1EN**	CLK1EN	**Enables DRAM clock 1** 0: Disable 1: Enable
28	**CLK0EN**	CLK0EN	**Enables DRAM clock 0** 0: Disable 1: Enable

1021413C WLEV Write Leveling Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DQS_SEL3**	**DQS_SEL2**	**DQS_SEL1**	**DQS_SEL0**				**DQS_WLEV**				**DQS_B3_G**	**DQS_B2_G**	**DQS_B1_G**	**DQS_B0_G**	**write_level_en**
Type	RW	RW	RW	RW				RW				RW	RW	RW	RW	RW
Reset	0	0	0	0				0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**DQS_SEL3**	DQS_SEL3	**DQS bit 3 will be calibrated during write leveling.** DQS_SEL3, DQS_SEL2, DQS_SEL1 and DQS_SEL0 can be enabled simultaneously.

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Bit(s)	Mnemonic	Name	Description
			0: Disable 1: Enable
14	**DQS_SEL2**	DQS_SEL2	**DQS bit 2 will be calibrated during write leveling.** DQS_SEL3, DQS_SEL2, DQS_SEL1 and DQS_SEL0 can be enabled simultaneously. 0: Disable 1: Enable
13	**DQS_SEL1**	DQS_SEL1	**DQS bit 1 will be calibrated during write leveling.** DQS_SEL3, DQS_SEL2, DQS_SEL1 and DQS_SEL0 can be enabled simultaneously. 0: Disable 1: Enable
12	**DQS_SEL0**	DQS_SEL0	**DQS bit 0 will be calibrated during write leveling.** DQS_SEL3, DQS_SEL2, DQS_SEL1 and DQS_SEL0 can be enabled simultaneously. 0: Disable 1: Enable
8	**DQS_WLEV**	DQS_WLEV	**Trigger one DQS pulse when write leveling.** **0:disable** **1: enable**
4	**DQS_B3_G**	DQS_B3_G	**DQS is high at phase 3 when write leveling.** DQS_B0_G, DQS_B1_G, DQS_B2_G and DQS_B3_G can be enabled simultaneously. 0: Disable 1: Enable
3	**DQS_B2_G**	DQS_B2_G	**DQS is high at phase 2 when write leveling. DQS_B0_G, DQS_B1_G, DQS_B2_G, DQS_B3_G can be enabled simultaneously. 0:disable** **1: enable**
2	**DQS_B1_G**	DQS_B1_G	**DQS is high at phase 1 when write leveling.** DQS_B0_G, DQS_B1_G, DQS_B2_G and DQS_B3_G can be enabled simultaneously. 0: Disable 1: Enable
1	**DQS_B0_G**	DQS_B0_G	**DQS is high at phase 0 when write leveling.** DQS_B0_G, DQS_B1_G, DQS_B2_G and DQS_B3_G can be enabled simultaneously. 0: Disable 1: Enable
0	**write_level_en**	write_level_en	**Enables write_level_en to let DQS low when write leveling** 0: Disable 1: Enable

10214168 **ARBCTL0** **Arbitration Control 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**WDATACNTDIS**	**RDATACNTDIS**	**MAXPENDCNT**							
Type							RW	RW	RW							
Reset							0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
9	**WDATACNTDIS**	WDATACNTDIS	**Disables write data counter to EMI** 0: Enable 1: Disable. Write data counter is always 0.
8	**RDATACNTDIS**	RDATACNTDIS	**Disables read data counter to EMI** 0: Enable 1: Disable. Read data counter is always 0.
7:0	**MAXPENDCNT**	MAXPENDCNT	**Maximum pending number to block the arbitration**

102141C0 DQSCAL0 DQS CAL Control 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STBCALEN															
Type	RW															
Reset	0															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	R0DQSIENHLMTEN	R0DQSIENHLMT							R0DQSIENLLMTEN	R0DQSIENLLMT						
Type	RW	RW							RW	RW						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**STBCALEN**	STBCALEN	**Enables DQS strobe calibration** 0: Disable 1: Enable
15	**R0DQSIENHLMTEN**	R0DQSIENHLMTEN	**Enables RANK0 DQS strobe calibration high-limit** 0: Disable 1: Enable
14:8	**R0DQSIENHLMT**	R0DQSIENHLMT	**RANK0 DQS strobe calibration high-limit value**
7	**R0DQSIENLLMTEN**	R0DQSIENLLMTEN	**Enables RANK0 DQS strobe calibration low-limit** 0: Disable 1: Enable
6:0	**R0DQSIENLLMT**	R0DQSIENLLMT	**RANK0 DQS strobe calibration low-limit value**

102141C4 DQSCAL1 DQS CAL Control 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													RANKINCTL			
Type													RW			
Reset													0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	R1DQSIENHLMTEN	R1DQSIENHLMT							R1DQSIENLLMTEN	R1DQSIENLLMT						
Type	RW	RW							RW	RW						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
19:16	**RANKINCTL**	RANKINCTL	**Rank selection delay setting** 0~11 = 1~12T DRAMC
15	**R1DQSIENHLMTEN**	R1DQSIENHLMTEN	**Enables RANK1 DQS strobe calibration high-limit** 0: Disable 1: Enable
14:8	**R1DQSIENHLMT**	R1DQSIENHLMT	**RANK1 DQS strobe calibration high-limit value**
7	**R1DQSIENLLMTEN**	R1DQSIENLLMTEN	**Enables RANK1 DQS strobe calibration low-limit** 0: Disable 1: Enable
6:0	**R1DQSIENLLMT**	R1DQSIENLLMT	**RANK1 DQS strobe calibration low-limit value**

102141DC **DRAMC_PD_CTRL** **PD Mode Parameter** **D0622842**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**COMBCLKCTRL**	**PHYCLKDYNGEN**		**REG_1DC_DUMMY1**		**MIOCKCTRLOFF**	**DCMEN**	**REFFRERUN**	**REFCNT_FR_CLK**							
Type	RW	RW		RW		RW	RW	RW	RW							
Reset	1	1		1		0	0	0	0	1	1	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TXREFCNT**								**RA15TOCS1**	**DCMDLYREF**			**R_DMCOMBPHY_CLKENSAME**	**PHYCLK_REFWKEN**	**REG_1DC_DUMMY0**	
Type	RW								RW	RW			RW	RW	RW	
Reset	0	0	1	0	1	0	0	0	0	1	0	0	0	0	1	

Bit(s)	Mnemonic	Name	Description
31	**COMBCLKCTRL**	COMBCLKCTRL	**Controls DQPHY clock dynamic gating (gating during all-bank refresh)** 0: Always no gating 1: Controlled by DRAMC
30	**PHYCLKDYNGEN**	PHYCLKDYNGEN	**Controls CMDPHY clock dynamic gating** 0: Always no gating 1: Controlled by DRAMC
28	**REG_1DC_DUMMY1**	REG_1DC_DUMMY1	**Dummy registers**
26	**MIOCKCTRLOFF**	MIOCKCTRLOFF	**DRAM CLK gating parameter** 0: Controlled by DRAMC 1: Always no gating
25	**DCMEN**	DCMEN	**DRAMC non-freerun clock gating function** 0: Disable 1: Enable
24	**REFFRERUN**	REFFRERUN	**Uses FREE-RUN CLK to count reflesh period**
23:16	**REFCNT_FR_CLK**	REFCNT_FR_CLK	**Refresh period = (REFCNT_FR_CLK) DRAMC FREE-RUN clock cycles** Set up the value according to DRAM spec and DRAMC FREE-RUN

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Bit(s)	Mnemonic	Name	Description
			frequency.
15:8	**TXREFCNT**	TXREFCNT	**tXSR** 258T/3T~258T for DDR3/LPDDR2
7	**RA15TOCS1**	RA15TOCS1	**Output RA15 by CS1 pin** 0: Disable 1: Enable
6:4	**DCMDLYREF**	DCMDLYREF	**Number of delay cycles to wake up DCM by the refresh command which is counted by the FREE-RUN clock** Note: This value cannot be set to 3'b000.
3	**R_DMCOMBPHY_CLKENSAME**	R_DMCOMBPHY_CLKENSAME	**DQPHY clock dynamic gating control will be the same with CMDPHY clock dynamic gating control.** (There will be no gating when in all-bank refresh.)
2	**PHYCLK_REFWKEN**	PHYCLK_REFWKEN	**If R_DMPHYCLK_REFWKEN is enabled, CMDPHY clock will not need to be waken up when refresh_wakeup_clk_pre = 1.**
1	**REG_1DC_DUMMY0**	REG_1DC_DUMMY0	**Dummy registers**

102141E0 **LPDDR2_3** **LPDDR2/LPDDR3 Setting** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**ADRDECEN**			**LPDDR2EN**	**WDATRGO**											
Type	RW			RW	RW											
Reset	0			0	0											
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
31	**ADRDECEN**	ADRDECEN	**Decodes DRAM address** 0: By EMI 1: By DRAMC
28	**LPDDR2EN**	LPDDR2EN	**Enables LPDDR2** 0: Disable 1: Enable
27	**WDATRGO**	WDATRGO	**Enables register output data by DRAMC** 0: Disable 1: Enable

102141E4 **SPCMD** **Special Command Mode** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									**ZQCSCNT**							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**DQSGCNTRST**	**DQSGCNTEN**		**SCPRE**	**TCMDEN**	**ZQCEN**	**AREFEN**	**PREAEN**	**MRREN**	**MRWEN**
Type							RW	RW		RW	RW	RW	RW	RW	RW	RW

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Reset							0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:16	**ZQCSCNT**	ZQCSCNT	**Every refresh number to issue ZQCS commands** Only for DDR3.
9	**DQSGCNTRST**	DQSGCNTRST	**Resets DQS gating window counter**
8	**DQSGCNTEN**	DQSGCNTEN	**Enables DQS gating window counter**
6	**SCPRE**	SCPRE	**Disables special command push** 1: Disable
5	**TCMDEN**	TCMDEN	**Enables test command** 0: Disable 1: Enable
4	**ZQCEN**	ZQCEN	**Enables ZQ calibration** 0: Disable 1: Enable
3	**AREFEN**	AREFEN	**Enables Auto Refresh command** 0: Disable 1: Enable
2	**PREAEN**	PREAEN	**Enables Precharge all command** 0: Disable 1: Enable
1	**MRREN**	MRREN	**Enables Mode register read command** 0: Disable 1: Enable
0	**MRWEN**	MRWEN	**Enables Mode register write command** 0: Disable 1: Enable

102141E8 ACTIM1 DRAM AC Timing Setting 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**LPDDR3EN**		**REFRDIS**	**TRPAB**		**REFRCNT**							
Type				RW		RW	RW		RW							
Reset				0		0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TRFCPB**								**TRFC_BIT7_4**				**TRRD_BIT2**		**TFAW_BIT4**	**TRC_BIT4**
Type	RW								RW				RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0

Bit(s)	Mnemonic	Name	Description
28	**LPDDR3EN**	LPDDR3EN	**Enables LPDDR3** 0: Disable 1: Enable
26	**REFRDIS**	REFRDIS	**Disables refresh auto update function** Set to 1 when MRWEN is used at run time; disabled after mrw_response =1.
25:24	**TRPAB**	TRPAB	**All-bank precharge timing for LPDDR2/3** tRPAB = TRP + TRPAB

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Bit(s)	Mnemonic	Name	Description
23:16	**REFRCNT**	REFRCNT	**Every refresh number to issue MRR commands for refresh rates** Only for LPDDR2/3.
15:8	**TRFCPB**	TRFCPB	**tRFCPB timing setting** tRFCPB = (11 + TRFCPB[7:0]) DRAMC clock cycles
7:4	**TRFC_BIT7_4**	TRFC_BIT7_4	**tRFC timing setting for bit 7 ~ 4**
3	**TRRD_BIT2**	TRRD_BIT2	**tRRD timing setting for bit 2**
1	**TFAW_BIT4**	TFAW_BIT4	**tFAW timing setting for bit 4**
0	**TRC_BIT4**	TRC_BIT4	**tRC timing setting for bit 4**

102141EC **PERFCTL0** **Performance Control 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**DISDMOEDIS**
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**WFLUSHEN**	**RWHPRICTL**	**CS2RANK**	**EMILLATEN**	**RWAGEEN**	**RWLLATEN**	**RWHPRIEN**	**RWOFOWNUM**			**RWOFOEN**				**DUALSCHEN**
Type		RW	RW	RW	RW	RW	RW	RW	RW			RW				RW
Reset		0	0	0	0	0	0	0	0	0	0	0				0

Bit(s)	Mnemonic	Name	Description
16	**DISDMOEDIS**	DISDMOEDIS	**For power saving, the self-refresh may disable the IO output enable** 0: Enable power saving function 1: Disable power saving function
14	**WFLUSHEN**	WFLUSHEN	**Controls write flush** 0: Disable 1: Enable
13	**RWHPRICTL**	RWHPRICTL	**Controls high-priority arbitration** 0: With waiting AC timing ready 1: Without waiting AC timing ready
12	**CS2RANK**	CS2RANK	**CS0 is also applied to CS1** 0: Disable 1: Enable
11	**EMILLATEN**	EMILLATEN	**Supports EMI read/write bank low-latency promotion Not along with requests** 0: Does not support 1: Support
10	**RWAGEEN**	RWAGEEN	**Supports EMI read/write aging tag** 0: Does not support 1: Support
9	**RWLLATEN**	RWLLATEN	**Supports EMI read/write low-latency** 0: Does not support 1: Support
8	**RWHPRIEN**	RWHPRIEN	**Supports EMI read/write high-priority**

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Bit(s)	Mnemonic	Name	Description
	N		0: Does not support 1: Support
7:5	**RWOFOWNUM**	RWOFOWNUM	**Continuous write transactions allowed** 0: No limit n: Allow (n+1) continuous write transactions
4	**RWOFOEN**	RWOFOEN	**Enables read/write out of order control** 0: Disable 1: Enable
0	**DUALSCHEN**	DUALSCHEN	**Enables dual scheduler** Only effective when FDIV2 = 1. 0: Disable 1: Enable

102141F0 **AC_DERATING** **AC Time Derating Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**TRRD_DERATE**					**TRPAB_DERATE**		**TRP_DERATE**				**TRAS_DERATE**			
Type		RW					RW		RW				RW			
Reset		0	0	0			0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**TRC_DERATE**					**TRCD_DERATE**							**ACDERATEEN**
Type				RW					RW							RW
Reset				0	0	0	0	0	0	0	0	0				0

Bit(s)	Mnemonic	Name	Description
30:28	**TRRD_DERATE**	TRRD_DERATE	**tRRD de-rate timing setting** tRRD = (1 + TRRD_DERATE) DRAMC clock cycles
25:24	**TRPAB_DERATE**	TRPAB_DERATE	**All-bank precharge de-rate timing for LPDDR2/LPDDR3** tRPAB = TRP_DERATE + TRPAB_DERATE
23:20	**TRP_DERATE**	TRP_DERATE	**tRP de-rate timing setting** tRP = (1 + TRP_DERATE) DRAMC clock cycles
19:16	**TRAS_DERATE**	TRAS_DERATE	**tRAS de-rate timing setting** tRAS = (8 + TRAS_DERATE) DRAMC clock cycles
12:8	**TRC_DERATE**	TRC_DERATE	**tRC de-rate timing setting** tRC = (8 + TRC_DERATE) DRAMC clock cycles
7:4	**TRCD_DERATE**	TRCD_DERATE	**tRCD de-rate timing setting** tRCD = (1 + TRCD_DERATE) DRAMC clock cycles
0	**ACDERATEEN**	ACDERATEEN	**Enable sLPDDR2/LPDDR3 AC timing de-rating control Effective when REFRESH_RATE >= 6.** 0: Disable 1: Enable

102141F4 **RRRATE_CTL** **Refresh Rate Control** **00020100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												**RR_BIT2_SEL**				
Type												RW				
Reset												0	0	0	1	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RR_BIT1_SEL								RR_BIT0_SEL				
Type				RW								RW				
Reset				0	0	0	0	1				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:16	RR_BIT2_SEL	RR_BIT2_SEL	**Selects refresh rate data bit 2 from 32-bit input read data** 00000: Select bit 0 00001: Select bit 1 00010: Select bit 2 ... 11111: Select bit 31
12:8	RR_BIT1_SEL	RR_BIT1_SEL	**Selects refresh rate data bit 1 from 32-bit input read data** 00000: Select bit 0 00001: Select bit 1 00010: Select bit 2 ... 11111: Select bit 31
4:0	RR_BIT0_SEL	RR_BIT0_SEL	**Selects refresh rate data bit 0 from 32-bit input read data** 00000: Select bit 0 00001: Select bit 1 00010: Select bit 2 ... 11111: Select bit 31

102141F8 AC_TIME_05T AC Time 0.5T Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					XRTW2R_M05T	TWTR_M05T	XRTR2W_05T	TR2W_05T			TRRD_05T_DERATE	TRAS_05T_DERATE	TRPAB_05T_DERATE	TRP_05T_DERATE	TRCD_05T_DERATE	TRC_05T_DERATE
Type					RW	RW	RW	RW			RW	RW	RW	RW	RW	RW
Reset					0	0	0	0			0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name			TFAW_05T	TRRD_05T		TWR_M05T	TRAS_05T	TRPAB_05T	TRP_05T	TRCD_05T	TRTP_05T	TXP_05T		TRFC_05T	TRFCPB_05T	TRC_05T
Type			RW	RW		RW	RW	RW	RW	RW	RW	RW		RW	RW	RW
Reset			0	0		0	0	0	0	0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
27	XRTW2R_M05T	XRTW2R_M05T	**Enables minus 0.5T control for cross-rank W2R** 0: Disable 1: Enable
26	TWTR_M05T	TWTR_M05T	**Enables mimus 0.5T control for tWTR** 0: Disable 1: Enable
25	XRTR2W_05T	XRTR2W_05T	**Enables 0.5T control for cross-rank tRTW** Note: This bit cannot be enabled when XRTR2W is set to the maximum value. 0: Disable 1: Enable
24	TR2W_05T	TR2W_05T	**Enables 0.5T control for tRTW** 0: Disable 1: Enable

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Bit(s)	Mnemonic	Name	Description
21	**TRRD_05T_DERATE**	TRRD_05T_DERATE	**tRRD 0.5T de-rate timing setting** Note: This bit cannot be enabled when TRRD_DERATE is set to the maximum value. 0: Disable 1: Enable
20	**TRAS_05T_DERATE**	TRAS_05T_DERATE	**tRAS 0.5T de-rate timing setting** 0: Disable 1: Enable
19	**TRPAB_05T_DERATE**	TRPAB_05T_DERATE	**tRPab 0.5T de-rate timing setting** 0: Disable 1: Enable
18	**TRP_05T_DERATE**	TRP_05T_DERATE	**tRP 0.5T de-rate timing setting** Note: This bit cannot be enabled when TRP_DERATE is set to the maximum value. 0: Ddisable 1: Enable
17	**TRCD_05T_DERATE**	TRCD_05T_DERATE	**tRCD 0.5T de-rate timing setting** Enable 0.5T control for tRCD. Note: This bit cannot be enabled when TRCD_DERATE is set to the maximum value. 0: Disable 1: Enable
16	**TRC_05T_DERATE**	TRC_05T_DERATE	**tRC 0.5T de-rate timing setting** 0: Disable 1: Enable
13	**TFAW_05T**	TFAW_05T	**Enables 0.5T control for tFAW** 0: disable 1: enable
12	**TRRD_05T**	TRRD_05T	**Enables 0.5T control for tRRD.** **Note: This bit cannot be enabled when TRRD is set to the maximum value.** 0: Disable 1: Enable
10	**TWR_M05T**	TWR_M05T	**Enables minus 0.5T control for tWR** 0: Disable 1: Enable
9	**TRAS_05T**	TRAS_05T	**Enables 0.5T control for tRAS** 0: Disable 1: Enable
8	**TRPAB_05T**	TRPAB_05T	**Enables 0.5T control for tRPab** 0: Disable 1: Enable
7	**TRP_05T**	TRP_05T	**Enables 0.5T control for tRP** Note: This bit cannot be enabled when TRP is set to the maximum value. 0: Disable 1: Enable
6	**TRCD_05T**	TRCD_05T	**Enables 0.5T control for tRCD** Note: This bit cannot be enabled when TRCD is set to the maximum value. 0: Disable 1: Enable
5	**TRTP_05T**	TRTP_05T	**Enables 0.5T control for tRTP** 0: Disable 1: Enable

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Bit(s)	Mnemonic	Name	Description
4	**TXP_05T**	TXP_05T	**Enables 0.5T control for tXP** 0: Disable 1: Enable
2	**TRFC_05T**	TRFC_05T	**Enables 0.5T control for tTRC** 0: Disable 1: Enable
1	**TRFCPB_05T**	TRFCPB_05T	**Enables 0.5T control for tTRCpb** 0: Disable 1: Enable
0	**TRC_05T**	TRC_05T	**Enables 0.5T control for tRC** 0: Disable 1: Enable

10214210 DQIDLY1 DQ Input Delay 1 Chain Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DQ3DEL								DQ2DEL			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DQ1DEL								DQ0DEL			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:24	**DQ3DEL**	DQ3DEL	**DQ input delay chain setting for bit 3** Unit: 20ps
19:16	**DQ2DEL**	DQ2DEL	**DQ input delay chain setting for bit 2** Unit: 20ps
11:8	**DQ1DEL**	DQ1DEL	**DQ input delay chain setting for bit 1** Unit: 20ps
3:0	**DQ0DEL**	DQ0DEL	**DQ input delay chain setting for bit 0** Unit: 20ps

10214214 DQIDLY2 DQ Input Delay 2 Chain Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DQ7DEL								DQ6DEL			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DQ5DEL								DQ4DEL			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:24	**DQ7DEL**	DQ7DEL	**DQ input delay chain setting for bit 7** Unit: 20ps
19:16	**DQ6DEL**	DQ6DEL	**DQ input delay chain setting for bit 6** Unit: 20ps

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Bit(s)	Mnemonic	Name	Description
11:8	**DQ5DEL**	DQ5DEL	**DQ input delay chain setting for bit 5** Unit: 20ps
3:0	**DQ4DEL**	DQ4DEL	**DQ input delay chain setting for bit 4** Unit: 20ps

10214218 DQIDLY3 DQ Input Delay 3 Chain Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DQ11DEL								DQ10DEL			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DQ9DEL								DQ8DEL			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:24	**DQ11DEL**	DQ11DEL	**DQ input delay chain setting for bit 11** Unit: 20ps
19:16	**DQ10DEL**	DQ10DEL	**DQ input delay chain setting for bit 10** Unit: 20ps
11:8	**DQ9DEL**	DQ9DEL	**DQ input delay chain setting for bit 9** Unit: 20ps
3:0	**DQ8DEL**	DQ8DEL	**DQ input delay chain setting for bit 8** Unit: 20ps

1021421C DQIDLY4 DQ Input Delay 4 Chain Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DQ15DEL								DQ14DEL			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DQ13DEL								DQ12DEL			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:24	**DQ15DEL**	DQ15DEL	**DQ input delay chain setting for bit 15** Unit: 20ps
19:16	**DQ14DEL**	DQ14DEL	**DQ input delay chain setting for bit 14** Unit: 20ps
11:8	**DQ13DEL**	DQ13DEL	**DQ input delay chain setting for bit 13** Unit: 20ps
3:0	**DQ12DEL**	DQ12DEL	**DQ input delay chain setting for bit 12** Unit: 20ps

10214220 DQIDLY5 DQ Input Delay 5 Chain Setting 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**DQ19DEL**								**DQ18DEL**			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**DQ17DEL**								**DQ16DEL**			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:24	**DQ19DEL**	DQ19DEL	**DQ input delay chain setting for bit 19** Unit: 20ps
19:16	**DQ18DEL**	DQ18DEL	**DQ input delay chain setting for bit 18** Unit: 20ps
11:8	**DQ17DEL**	DQ17DEL	**DQ input delay chain setting for bit 17** Unit: 20ps
3:0	**DQ16DEL**	DQ16DEL	**DQ input delay chain setting for bit 16** Unit: 20ps

10214224 DQIDLY6 DQ Input Delay 6 Chain Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**DQ23DEL**								**DQ22DEL**			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**DQ21DEL**								**DQ20DEL**			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:24	**DQ23DEL**	DQ23DEL	**DQ input delay chain setting for bit 23** Unit: 20ps
19:16	**DQ22DEL**	DQ22DEL	**DQ input delay chain setting for bit 22** Unit: 20ps
11:8	**DQ21DEL**	DQ21DEL	**DQ input delay chain setting for bit 21** Unit: 20ps
3:0	**DQ20DEL**	DQ20DEL	**DQ input delay chain setting for bit 20** Unit: 20ps

10214228 DQIDLY7 DQ Input Delay 7 Chain Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**DQ27DEL**								**DQ26DEL**			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**DQ25DEL**								**DQ24DEL**			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
27:24	**DQ27DEL**	DQ27DEL	**DQ input delay chain setting for bit 27** Unit: 20ps
19:16	**DQ26DEL**	DQ26DEL	**DQ input delay chain setting for bit 26** Unit: 20ps
11:8	**DQ25DEL**	DQ25DEL	**DQ input delay chain setting for bit 25** Unit: 20ps
3:0	**DQ24DEL**	DQ24DEL	**DQ input delay chain setting for bit 24** Unit: 20ps

1021422C DQIDLY8 DQ Input Delay 8 Chain Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DQ31DEL								DQ30DEL			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DQ29DEL								DQ28DEL			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:24	**DQ31DEL**	DQ31DEL	**DQ input delay chain setting for bit 31** Unit: 20ps
19:16	**DQ30DEL**	DQ30DEL	**DQ input delay chain setting for bit 30** Unit: 20ps
11:8	**DQ29DEL**	DQ29DEL	**DQ input delay chain setting for bit 29** Unit: 20ps
3:0	**DQ28DEL**	DQ28DEL	**DQ input delay chain setting for bit 28** Unit: 20ps

102143D8 DQSSAMPLEV DQS Sample Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													sample_out1_DQS3	sample_out1_DQS2	sample_out1_DQS1	sample_out1_DQS0
Type													RO	RO	RO	RO
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3	**sample_out1_DQS3**	sample_out1_DQS3	**Sampled value for DQS3** 0: Late 1: Early
2	**sample_out1_DQS2**	sample_out1_DQS2	**Sampled value for DQS2** 0: Late 1: Early

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Bit(s)	Mnemonic	Name	Description
1	**sample_out1_DQS1**	sample_out1_DQS1	**Sampled value for DQS1** 0: Late 1: Early
0	**sample_out1_DQS0**	sample_out1_DQS0	**Sampled value for DQS0** 0: Late 1: Early

1020E02C TESTMODE Test Mode Configuration 1 55010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TESTM_PAT0															REG_2C_DUMMY
Type	RW															RW
Reset	0	1	0	1	0	1	0	1								1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
31:24	**TESTM_PAT0**	TESTM_PAT0	Test-pattern 0 for test mode
16	**REG_2C_DUMMY**	REG_2C_DUMMY	Dummy registers

1020E03C TEST2_1 Test Agent 2 Configuration 1 01200000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TEST2_PAT0								TEST2_BASE_28to5[23:16]							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TEST2_BASE_28to5[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**TEST2_PAT0**	TEST2_PAT0	Test-pattern 0 for Test Agent 2
23:0	**TEST2_BASE_28to5**	TEST2_BASE_28to5	Test base address for Test Agent 2

1020E040 TEST2_2 Test Agent 2 Configuration 2 00010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TEST2_PAT1								TEST2_OFF_28to5[23:16]							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TEST2_OFF_28to5[15:0]															

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Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**TEST2_PAT1**	TEST2_PAT1	Test-pattern 1 for Test Agent 2
23:0	**TEST2_OFF_28to5**	TEST2_OFF_28to5	Test offset address for Test Agent 2

1020E104 LBWDAT0 Loop Back Data 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LBWDATA0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LBWDATA0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**LBWDATA0**	LBWDATA0	Loop-back test mode data 0

1020E108 LBWDAT1 Loop Back Data 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LBWDATA1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LBWDATA1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**LBWDATA1**	LBWDATA1	Loop-back test mode data 1

1020E10C LBWDAT2 Loop Back Data 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LBWDATA2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LBWDATA2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**LBWDATA**	LBWDATA2	Loop-back test mode data 2

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Bit(s)	Mnemonic	Name	Description
	2		

1020E114 CKPHDET Clock Phase Detection Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CKPHCNTEN							
Type									RW							
Reset									0							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CKPHCHKCYC															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23	CKPHCNTEN	CKPHCNTEN	**Enables MEMPLL in/out clock phase detection counter** 0: Disable 1: Enable
15:0	CKPHCHKCYC	CKPHCHKCYC	**MEMPLL in/out clock phase detection counter cycle** Unit: DRAMC clock

1020E1D8 DMMonitor Monitor Parameter 00C80000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	JMTRCNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													BUSMONEN_SW	MONPAUSE_SW		JMTR_EN
Type													RW	RW		RW
Reset													0	0		0

Bit(s)	Mnemonic	Name	Description
31:16	JMTRCNT	JMTRCNT	**Sets up monitor period for jitter meter**
3	BUSMONEN_SW	BUSMONEN_SW	**Enables bus monitor** Cannot be used with BUSMONEN_HW at the same time. 0: Disable 1: Enable
2	MONPAUSE_SW	MONPAUSE_SW	**Pauses bus monitor counter** Cannot be used with MONPAUSE_HW at the same time. 0: Disable 1: Enable
0	JMTR_EN	JMTR_EN	**Enables jitter meter** 0: Disable 1: Enable

1020E280 R2R_page_hit R2R_page_hit_counter 00000000

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_counter

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R2R_page_hit_counter[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R2R_page_hit_counter[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**R2R_page_hit_counter**	R2R_page_hit_counter	For debugging

1020E284 **R2R_page_miss_counter** **R2R_page_miss_counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R2R_page_miss_counter[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R2R_page_miss_counter[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**R2R_page_miss_counter**	R2R_page_miss_counter	For debugging

1020E288 **R2R_interbank_counter** **R2R_interbank_counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R2R_interbank_counter[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R2R_interbank_counter[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**R2R_interbank_counter**	R2R_interbank_counter	For debugging

1020E28C **R2W_page_hit_counter** **R2W_page_hit_counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	**R2W_page_hit_counter[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**R2W_page_hit_counter[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**R2W_page_hit_counter**	R2W_page_hit_counter	For debugging

1020E290 **R2W_page_miss_counter** **R2W_page_miss_counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**R2W_page_miss_counter[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**R2W_page_miss_counter[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**R2W_page_miss_counter**	R2W_page_miss_counter	For debugging

1020E294 **R2W_interbank_counter** **R2W_interbank_counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**R2W_interbank_counter[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**R2W_interbank_counter[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**R2W_interbank_counter**	R2W_interbank_counter	For debugging

1020E298 **W2R_page_hit_counter** **W2R_page_hit_counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**W2R_page_hit_counter[31:16]**															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**W2R_page_hit_counter[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**W2R_page_hit_counter**	W2R_page_hit_counter	For debugging

1020E29C **W2R_page_miss_counter** **W2R_page_miss_counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**W2R_page_miss_counter[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**W2R_page_miss_counter[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**W2R_page_miss_counter**	W2R_page_miss_counter	For debugging

1020E2A0 **W2R_interbank_counter** **W2R_interbank_counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**W2R_interbank_counter[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**W2R_interbank_counter[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**W2R_interbank_counter**	W2R_interbank_counter	For debugging

1020E2A4 **W2W_page_hit_counter** **W2W_page_hit_counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**W2W_page_hit_counter[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	W2W_page_hit_counter[15:0]
Type	RO
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit(s)	Mnemonic	Name	Description
31:0	**W2W_page_hit_counter**	W2W_page_hit_counter	For debugging

1020E2A8 **W2W_page_miss_counter** **W2W_page_miss_counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	W2W_page_miss_counter[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	W2W_page_miss_counter[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**W2W_page_miss_counter**	W2W_page_miss_counter	For debugging

1020E2AC **W2W_interbank_counter** **W2W_interbank_counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	W2W_interbank_counter[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	W2W_interbank_counter[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**W2W_interbank_counter**	W2W_interbank_counter	For debugging

1020E2B0 **dramc_idle_counter** **dramc_idle_counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dramc_idle_counter[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dramc_idle_counter[15:0]															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**dramc_idle_counter**	dramc_idle_counter	For debugging

1020E2B4 **freerun_26m_counter** **freerun_26m_counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**freerun_26m_counter[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**freerun_26m_counter[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**freerun_26m_counter**	freerun_26m_counter	For debugging

1020E2B8 **refresh_pop_counter** **refresh_pop_counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**refresh_pop_counter[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**refresh_pop_counter[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**refresh_pop_counter**	refresh_pop_counter	For debugging

1020E2BC **JMETER_ST** **Jitter Meter Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**JMTR_DONE**	**ONES_CNT**														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**ZEROS_CNT**														
Type		RO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
31	**JMTR_DONE**	JMTR_DONE	**Jitter meter result is updated.** 0: Not ready 1: Update result
30:16	**ONES_CNT**	ONES_CNT	**Ones counter result**
14:0	**ZEROS_CNT**	ZEROS_CNT	**Zeros counter result**

1020E2C0 **DQ_CAL_MAX_0** **DQ Input Calibration Per Bit 3-0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQ0_3_DLY_MAX								DQ0_2_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQ0_1_DLY_MAX								DQ0_0_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DQ0_3_DLY_MAX**	DQ0_3_DLY_MAX	DQ bit 3 input maximum delay
23:16	**DQ0_2_DLY_MAX**	DQ0_2_DLY_MAX	DQ bit 2 input maximum delay
15:8	**DQ0_1_DLY_MAX**	DQ0_1_DLY_MAX	DQ bit 1 input maximum delay
7:0	**DQ0_0_DLY_MAX**	DQ0_0_DLY_MAX	DQ bit 0 input maximum delay

1020E2C4 **DQ_CAL_MAX_1** **DQ Input Calibration Per Bit 7-4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQ0_7_DLY_MAX								DQ0_6_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQ0_5_DLY_MAX								DQ0_4_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DQ0_7_DLY_MAX**	DQ0_7_DLY_MAX	DQ bit 7 input maximum delay
23:16	**DQ0_6_DLY_MAX**	DQ0_6_DLY_MAX	DQ bit 6 input maximum delay
15:8	**DQ0_5_DLY_MAX**	DQ0_5_DLY_MAX	DQ bit 5 input maximum delay
7:0	**DQ0_4_DLY_MAX**	DQ0_4_DLY_MAX	DQ bit 4 input maximum delay

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1020E2C8 **DQ_CAL_MAX_2** **DQ Input Calibration Per Bit 11-8** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQ1_3_DLY_MAX								DQ1_2_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQ1_1_DLY_MAX								DQ1_0_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	DQ1_3_DLY_MAX	DQ1_3_DLY_MAX	DQ bit 11 input maximum delay
23:16	DQ1_2_DLY_MAX	DQ1_2_DLY_MAX	DQ bit 10 input maximum delay
15:8	DQ1_1_DLY_MAX	DQ1_1_DLY_MAX	DQ bit 9 input maximum delay
7:0	DQ1_0_DLY_MAX	DQ1_0_DLY_MAX	DQ bit 8 input maximum delay

1020E2CC **DQ_CAL_MAX_3** **DQ Input Calibration Per Bit 15-12** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQ1_7_DLY_MAX								DQ1_6_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQ1_5_DLY_MAX								DQ1_4_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	DQ1_7_DLY_MAX	DQ1_7_DLY_MAX	DQ bit 15 input maximum delay
23:16	DQ1_6_DLY_MAX	DQ1_6_DLY_MAX	DQ bit 14 input maximum delay
15:8	DQ1_5_DLY_MAX	DQ1_5_DLY_MAX	DQ bit 13 input maximum delay
7:0	DQ1_4_DLY_MAX	DQ1_4_DLY_MAX	DQ bit 12 input maximum delay

1020E2D0 **DQ_CAL_MAX_4** **DQ Input Calibration Per Bit 19-16** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQ2_3_DLY_MAX								DQ2_2_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQ2_1_DLY_MAX								DQ2_0_DLY_MAX							

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Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	DQ2_3_DLY_MAX	DQ2_3_DLY_MAX	DQ bit 19 input maximum delay
23:16	DQ2_2_DLY_MAX	DQ2_2_DLY_MAX	DQ bit 18 input maximum delay
15:8	DQ2_1_DLY_MAX	DQ2_1_DLY_MAX	DQ bit 17 input maximum delay
7:0	DQ2_0_DLY_MAX	DQ2_0_DLY_MAX	DQ bit 16 input maximum delay

1020E2D4 **DQ_CAL_MAX_5** **DQ Input Calibration Per Bit 23-20** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQ2_7_DLY_MAX								DQ2_6_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQ2_5_DLY_MAX								DQ2_4_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	DQ2_7_DLY_MAX	DQ2_7_DLY_MAX	DQ bit 23 input maximum delay
23:16	DQ2_6_DLY_MAX	DQ2_6_DLY_MAX	DQ bit 22 input maximum delay
15:8	DQ2_5_DLY_MAX	DQ2_5_DLY_MAX	DQ bit 21 input maximum delay
7:0	DQ2_4_DLY_MAX	DQ2_4_DLY_MAX	DQ bit 20 input maximum delay

1020E2D8 **DQ_CAL_MAX_6** **DQ Input Calibration Per Bit 27-34** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQ3_3_DLY_MAX								DQ3_2_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQ3_1_DLY_MAX								DQ3_0_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	DQ3_3_DLY_MAX	DQ3_3_DLY_MAX	DQ bit 27 input maximum delay
23:16	DQ3_2_DLY_MAX	DQ3_2_DLY_MAX	DQ bit 26 input maximum delay

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Bit(s)	Mnemonic	Name	Description
15:8	**DQ3_1_DLY_MAX**	DQ3_1_DLY_MAX	DQ bit 25 input maximum delay
7:0	**DQ3_0_DLY_MAX**	DQ3_0_DLY_MAX	DQ bit 24 input maximum delay

1020E2DC **DQ_CAL_MAX_7** **DQ Input Calibration Per Bit 31-28** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DQ3_7_DLY_MAX**								**DQ3_6_DLY_MAX**							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DQ3_5_DLY_MAX**								**DQ3_4_DLY_MAX**							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DQ3_7_DLY_MAX**	DQ3_7_DLY_MAX	DQ bit 31 input maximum delay
23:16	**DQ3_6_DLY_MAX**	DQ3_6_DLY_MAX	DQ bit 30 input maximum delay
15:8	**DQ3_5_DLY_MAX**	DQ3_5_DLY_MAX	DQ bit 29 input maximum delay
7:0	**DQ3_4_DLY_MAX**	DQ3_4_DLY_MAX	DQ bit 28 input maximum delay

1020E2E0 **DQS_CAL_MIN_0** **DQS Input Calibration Per Bit 3-0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DQS0_3_DLY_MIN**								**DQS0_2_DLY_MIN**							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DQS0_1_DLY_MIN**								**DQS0_0_DLY_MIN**							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DQS0_3_DLY_MIN**	DQS0_3_DLY_MIN	DQS bit 3 input minimum delay
23:16	**DQS0_2_DLY_MIN**	DQS0_2_DLY_MIN	DQS bit 2 input minimum delay
15:8	**DQS0_1_DLY_MIN**	DQS0_1_DLY_MIN	DQS bit 1 input minimum delay
7:0	**DQS0_0_DLY_MIN**	DQS0_0_DLY_MIN	DQS bit 0 input minimum delay

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1020E2E4 DQS_CAL_MIN_1 DQS Input Calibration Per Bit 7-4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQS0_7_DLY_MIN								DQS0_6_DLY_MIN							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQS0_5_DLY_MIN								DQS0_4_DLY_MIN							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DQS0_7_DLY_MIN**	DQS0_7_DLY_MIN	DQS bit 7 input minimum delay
23:16	**DQS0_6_DLY_MIN**	DQS0_6_DLY_MIN	DQS bit 6 input minimum delay
15:8	**DQS0_5_DLY_MIN**	DQS0_5_DLY_MIN	DQS bit 5 input minimum delay
7:0	**DQS0_4_DLY_MIN**	DQS0_4_DLY_MIN	DQS bit 4 input minimum delay

1020E2E8 DQS_CAL_MIN_2 DQS Input Calibration Per Bit 11-8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQS1_3_DLY_MIN								DQS1_2_DLY_MIN							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQS1_1_DLY_MIN								DQS1_0_DLY_MIN							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DQS1_3_DLY_MIN**	DQS1_3_DLY_MIN	DQS bit 11 input minimum delay
23:16	**DQS1_2_DLY_MIN**	DQS1_2_DLY_MIN	DQS bit 10 input minimum delay
15:8	**DQS1_1_DLY_MIN**	DQS1_1_DLY_MIN	DQS bit 9 input minimum delay
7:0	**DQS1_0_DLY_MIN**	DQS1_0_DLY_MIN	DQS bit 8 input minimum delay

1020E2EC DQS_CAL_MIN_3 DQS Input Calibration Per Bit 15-12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQS1_7_DLY_MIN								DQS1_6_DLY_MIN							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQS1_5_DLY_MIN								DQS1_4_DLY_MIN							
Type	RO								RO							

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DQS1_7_DLY_MIN**	DQS1_7_DLY_MIN	DQS bit 15 input minimum delay
23:16	**DQS1_6_DLY_MIN**	DQS1_6_DLY_MIN	DQS bit 14 input minimum delay
15:8	**DQS1_5_DLY_MIN**	DQS1_5_DLY_MIN	DQS bit 13 input minimum delay
7:0	**DQS1_4_DLY_MIN**	DQS1_4_DLY_MIN	DQS bit 12 input minimum delay

1020E2F0 **DQS_CAL_MIN_4** **DQS Input Calibration Per Bit 19-16** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQS2_3_DLY_MIN								DQS2_2_DLY_MIN							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQS2_1_DLY_MIN								DQS2_0_DLY_MIN							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DQS2_3_DLY_MIN**	DQS2_3_DLY_MIN	DQS bit 19 input minimum delay
23:16	**DQS2_2_DLY_MIN**	DQS2_2_DLY_MIN	DQS bit 18 input minimum delay
15:8	**DQS2_1_DLY_MIN**	DQS2_1_DLY_MIN	DQS bit 17 input minimum delay
7:0	**DQS2_0_DLY_MIN**	DQS2_0_DLY_MIN	DQS bit 16 input minimum delay

1020E2F4 **DQS_CAL_MIN_5** **DQS Input Calibration Per Bit 23-20** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQS2_7_DLY_MIN								DQS2_6_DLY_MIN							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQS2_5_DLY_MIN								DQS2_4_DLY_MIN							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DQS2_7_DLY_MIN**	DQS2_7_DLY_MIN	DQS bit 23 input minimum delay
23:16	**DQS2_6_DLY_MIN**	DQS2_6_DLY_MIN	DQS bit 22 input minimum delay
15:8	**DQS2_5_D**	DQS2_5_DLY_MI	DQS bit 21 input minimum delay

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Bit(s)	Mnemonic	Name	Description
	LY_MIN	N	
7:0	**DQS2_4_DLY_MIN**	DQS2_4_DLY_MIN	DQS bit 20 input minimum delay

1020E2F8 **DQS_CAL_MIN_6** **DQS Input Calibration Per Bit 27-34** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQS3_3_DLY_MIN								DQS3_2_DLY_MIN							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQS3_1_DLY_MIN								DQS3_0_DLY_MIN							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DQS3_3_DLY_MIN**	DQS3_3_DLY_MIN	DQS bit 27 input minimum delay
23:16	**DQS3_2_DLY_MIN**	DQS3_2_DLY_MIN	DQS bit 26 input minimum delay
15:8	**DQS3_1_DLY_MIN**	DQS3_1_DLY_MIN	DQS bit 25 input minimum delay
7:0	**DQS3_0_DLY_MIN**	DQS3_0_DLY_MIN	DQS bit 24 input minimum delay

1020E2FC **DQS_CAL_MIN_7** **DQS Input Calibration Per Bit 31-28** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQS3_7_DLY_MIN								DQS3_6_DLY_MIN							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQS3_5_DLY_MIN								DQS3_4_DLY_MIN							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DQS3_7_DLY_MIN**	DQS3_7_DLY_MIN	DQS bit 31 input minimum delay
23:16	**DQS3_6_DLY_MIN**	DQS3_6_DLY_MIN	DQS bit 30 input minimum delay
15:8	**DQS3_5_DLY_MIN**	DQS3_5_DLY_MIN	DQS bit 29 input minimum delay
7:0	**DQS3_4_DLY_MIN**	DQS3_4_DLY_MIN	DQS bit 28 input minimum delay

1020E300 **DQS_CAL_MA** **DQS Input Calibration Per Bit 3-0** **00000000**

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X_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQS0_3_DLY_MAX								DQS0_2_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQS0_1_DLY_MAX								DQS0_0_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DQS0_3_DLY_MAX**	DQS0_3_DLY_MAX	DQS bit 3 input maximum delay
23:16	**DQS0_2_DLY_MAX**	DQS0_2_DLY_MAX	DQS bit 2 input maximum delay
15:8	**DQS0_1_DLY_MAX**	DQS0_1_DLY_MAX	DQS bit 1 input maximum delay
7:0	**DQS0_0_DLY_MAX**	DQS0_0_DLY_MAX	DQS bit 0 input maximum delay

1020E304 **DQS_CAL_MAX_1** **DQS Input Calibration Per Bit 7-4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQS0_7_DLY_MAX								DQS0_6_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQS0_5_DLY_MAX								DQS0_4_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DQS0_7_DLY_MAX**	DQS0_7_DLY_MAX	DQS bit 7 input maximum delay
23:16	**DQS0_6_DLY_MAX**	DQS0_6_DLY_MAX	DQS bit 6 input maximum delay
15:8	**DQS0_5_DLY_MAX**	DQS0_5_DLY_MAX	DQS bit 5 input maximum delay
7:0	**DQS0_4_DLY_MAX**	DQS0_4_DLY_MAX	DQS bit 4 input maximum delay

1020E308 **DQS_CAL_MAX_2** **DQS Input Calibration Per Bit 11-8** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQS1_3_DLY_MAX								DQS1_2_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQS1_1_DLY_MAX								DQS1_0_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31:24	**DQS1_3_DLY_MAX**	DQS1_3_DLY_MAX	DQS bit 11 input maximum delay
23:16	**DQS1_2_DLY_MAX**	DQS1_2_DLY_MAX	DQS bit 10 input maximum delay
15:8	**DQS1_1_DLY_MAX**	DQS1_1_DLY_MAX	DQS bit 9 input maximum delay
7:0	**DQS1_0_DLY_MAX**	DQS1_0_DLY_MAX	DQS bit 8 input maximum delay

1020E30C **DQS_CAL_MAX_3** **DQS Input Calibration Per Bit 15-12** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQS1_7_DLY_MAX								DQS1_6_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQS1_5_DLY_MAX								DQS1_4_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DQS1_7_DLY_MAX**	DQS1_7_DLY_MAX	DQS bit 15 input maximum delay
23:16	**DQS1_6_DLY_MAX**	DQS1_6_DLY_MAX	DQS bit 14 input maximum delay
15:8	**DQS1_5_DLY_MAX**	DQS1_5_DLY_MAX	DQS bit 13 input maximum delay
7:0	**DQS1_4_DLY_MAX**	DQS1_4_DLY_MAX	DQS bit 12 input maximum delay

1020E310 **DQS_CAL_MAX_4** **DQS Input Calibration Per Bit 19-16** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQS2_3_DLY_MAX								DQS2_2_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQS2_1_DLY_MAX								DQS2_0_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DQS2_3_DLY_MAX**	DQS2_3_DLY_MAX	DQS bit 19 input maximum delay
23:16	**DQS2_2_DLY_MAX**	DQS2_2_DLY_MAX	DQS bit 18 input maximum delay
15:8	**DQS2_1_DLY_MAX**	DQS2_1_DLY_MAX	DQS bit 17 input maximum delay
7:0	**DQS2_0_DLY_MAX**	DQS2_0_DLY_MAX	DQS bit 16 input maximum delay

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1020E314 DQS_CAL_MAX_5 DQS Input Calibration Per Bit 23-20 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQS2_7_DLY_MAX								DQS2_6_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQS2_5_DLY_MAX								DQS2_4_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	DQS2_7_DLY_MAX	DQS2_7_DLY_MAX	DQS bit 23 input maximum delay
23:16	DQS2_6_DLY_MAX	DQS2_6_DLY_MAX	DQS bit 22 input maximum delay
15:8	DQS2_5_DLY_MAX	DQS2_5_DLY_MAX	DQS bit 21 input maximum delay
7:0	DQS2_4_DLY_MAX	DQS2_4_DLY_MAX	DQS bit 20 input maximum delay

1020E318 DQS_CAL_MAX_6 DQS Input Calibration Per Bit 27-34 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQS3_3_DLY_MAX								DQS3_2_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQS3_1_DLY_MAX								DQS3_0_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	DQS3_3_DLY_MAX	DQS3_3_DLY_MAX	DQS bit 27 input maximum delay
23:16	DQS3_2_DLY_MAX	DQS3_2_DLY_MAX	DQS bit 26 input maximum delay
15:8	DQS3_1_DLY_MAX	DQS3_1_DLY_MAX	DQS bit 25 input maximum delay
7:0	DQS3_0_DLY_MAX	DQS3_0_DLY_MAX	DQS bit 24 input maximum delay

1020E31C DQS_CAL_MAX_7 DQS Input Calibration Per Bit 31-28 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQS3_7_DLY_MAX								DQS3_6_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQS3_5_DLY_MAX								DQS3_4_DLY_MAX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DQS3_7_DLY_MAX**	DQS3_7_DLY_MAX	DQS bit 31 input maximum delay
23:16	**DQS3_6_DLY_MAX**	DQS3_6_DLY_MAX	DQS bit 30 input maximum delay
15:8	**DQS3_5_DLY_MAX**	DQS3_5_DLY_MAX	DQS bit 29 input maximum delay
7:0	**DQS3_4_DLY_MAX**	DQS3_4_DLY_MAX	DQS bit 28 input maximum delay

1020E350 DQICAL0 DQS Input Calibration 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DQ3_DLY_MAX								DQ2_DLY_MAX						
Type		RO								RO						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DQ1_DLY_MAX								DQ0_DLY_MAX						
Type		RO								RO						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:24	**DQ3_DLY_MAX**	DQ3_DLY_MAX	DQ byte 3 input maximum delay
22:16	**DQ2_DLY_MAX**	DQ2_DLY_MAX	DQ byte 2 input maximum delay
14:8	**DQ1_DLY_MAX**	DQ1_DLY_MAX	DQ byte 1 input maximum delay
6:0	**DQ0_DLY_MAX**	DQ0_DLY_MAX	DQ byte 0 input maximum delay

1020E354 DQICAL1 DQS Input Calibration 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DQS3_DLY_MIN								DQS2_DLY_MIN						
Type		RO								RO						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DQS1_DLY_MIN								DQS0_DLY_MIN						
Type		RO								RO						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:24	**DQS3_DLY_MIN**	DQS3_DLY_MIN	DQS3 input minimum delay
22:16	**DQS2_DLY_MIN**	DQS2_DLY_MIN	DQS2 input minimum delay
14:8	**DQS1_DLY**	DQS1_DLY_MIN	DQS1 input minimum delay

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Bit(s)	Mnemonic	Name	Description
	_MIN		
6:0	**DQS0_DLY_MIN**	DQS0_DLY_MIN	DQS0 input minimum delay

1020E358 DQICAL2 DQS Input Calibration 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DQS3_DLY_MAX								DQS2_DLY_MAX						
Type		RO								RO						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DQS1_DLY_MAX								DQS0_DLY_MAX						
Type		RO								RO						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:24	**DQS3_DLY_MAX**	DQS3_DLY_MAX	DQS3 input maximum delay
22:16	**DQS2_DLY_MAX**	DQS2_DLY_MAX	DQS2 input maximum delay
14:8	**DQS1_DLY_MAX**	DQS1_DLY_MAX	DQS1 input maximum delay
6:0	**DQS0_DLY_MAX**	DQS0_DLY_MAX	DQS0 input maximum delay

1020E35C DQICAL3 DQS Input Calibration 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DQS3_DLY_AVG								DQS2_DLY_AVG						
Type		RO								RO						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DQS1_DLY_AVG								DQS0_DLY_AVG						
Type		RO								RO						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:24	**DQS3_DLY_AVG**	DQS3_DLY_AVG	DQS3 input delay average
22:16	**DQS2_DLY_AVG**	DQS2_DLY_AVG	DQS2 input delay average
14:8	**DQS1_DLY_AVG**	DQS1_DLY_AVG	DQS1 input delay average
6:0	**DQS0_DLY_AVG**	DQS0_DLY_AVG	DQS0 input delay average

1020E370 CMP_ERR CMP Error 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CMP_ERR[31:16]															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CMP_ERR[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CMP_ERR**	CMP_ERR	Bitwise auto test fails.

1020E374 **R0DQSIENDLY** RANK0 DQS Input Gating Delay Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		R0DQS3IENDLY								R0DQS2IENDLY						
Type		RO								RO						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		R0DQS1IENDLY								R0DQS0IENDLY						
Type		RO								RO						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:24	**R0DQS3IENDLY**	R0DQS3IENDLY	RANK0 DQS input gating delay for DQS3
22:16	**R0DQS2IENDLY**	R0DQS2IENDLY	RANK0 DQS input gating delay for DQS2
14:8	**R0DQS1IENDLY**	R0DQS1IENDLY	RANK0 DQS input gating delay for DQS1
6:0	**R0DQS0IENDLY**	R0DQS0IENDLY	RANK0 DQS input gating delay for DQS0

1020E378 **R1DQSIENDLY** RANK1 DQS Input Gating Delay Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		R1DQS3IENDLY								R1DQS2IENDLY						
Type		RO								RO						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		R1DQS1IENDLY								R1DQS0IENDLY						
Type		RO								RO						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:24	**R1DQS3IENDLY**	R1DQS3IENDLY	RANK1 DQS input gating delay for DQS3
22:16	**R1DQS2IENDLY**	R1DQS2IENDLY	RANK1 DQS input gating delay for DQS2
14:8	**R1DQS1IENDLY**	R1DQS1IENDLY	RANK1 DQS input gating delay for DQS1
6:0	**R1DQS0IENDLY**	R1DQS0IENDLY	RANK1 DQS input gating delay for DQS0

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1020E3A0 DQSDLY0 DQS Input Delay Setting 0 0F0F0F0F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DEL3DLY								DEL2DLY						
Type		RO								RO						
Reset		0	0	0	1	1	1	1		0	0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DEL1DLY								DEL0DLY						
Type		RO								RO						
Reset		0	0	0	1	1	1	1		0	0	0	1	1	1	1

Bit(s)	Mnemonic	Name	Description
30:24	**DEL3DLY**	DEL3DLY	DQS input delay for DQS3
22:16	**DEL2DLY**	DEL2DLY	DQS input delay for DQS2
14:8	**DEL1DLY**	DEL1DLY	DQS input delay for DQS1
6:0	**DEL0DLY**	DEL0DLY	DQS input delay for DQS0

1020E3B8 SPCMDRESP Special Command Response 00010300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																SREF_STATE
Type																RO
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DRAM_HWCFG		REFRESH_RATE					TCMD_RESPONSE	ZQC_RESPONSE	AREF_RESPONSE	PREA_RESPONSE	MRR_RESPONSE	MRW_RESPONSE
Type				RO		RO					RO	RO	RO	RO	RO	RO
Reset				0		0	1	1			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	**SREF_STATE**	SREF_STATE	**Self-refresh status** 0: Does not enter 1: Enter
12	**DRAM_HWCFG**	DRAM_HWCFG	**Configures DRAM hardware** 1: LPDDR1 0: Others
10:8	**REFRESH_RATE**	REFRESH_RATE	**Refresh rate reading from LPDDR2/LPDDR3** 001: 4 x tREFI 010: 2 x tREFI 011: 1 x tREFI 100: 0.5 x tREFI, only for LPDDR3 101: 0.25 x tREFI 110: 2.25 x tREFI Others: Refer to LPDDR2/LPDDR3 spec.
5	**TCMD_RESPONSE**	TCMD_RESPONSE	**TCMD command response**
4	**ZQC_RESPONSE**	ZQC_RESPONSE	**ZQC command response**
3	**AREF_RESPONSE**	AREF_RESPONSE	**AREF command response**

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Bit(s)	Mnemonic	Name	Description
2	**PREA_RESPONSE**	PREA_RESPONSE	**PREA command response**
1	**MRR_RESPONSE**	MRR_RESPONSE	**MRR command response**
0	**MRW_RESPONSE**	MRW_RESPONSE	**MRW command response**

1020E3BC **IORGCNT** **IO Ring Counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OFF23DLY															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFF22DLY															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16	**OFF23DLY**	IO_RING_COUNTER	270 degree I/O clock offset counter for group 5
15:0	**OFF22DLY**	IO_RING_COUNTER_K	180 degree I/O clock offset counter for group 5

1020E3C0 **DQSGNWCNT0** **DQS Gating Window Counter 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dqs1r_gating_counter								dqs1f_gating_counter							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dqs0r_gating_counter								dqs0f_gating_counter							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**dqs1r_gating_counter**	dqs1r_gating_counter	Rising DQS gating counter for group 1
23:16	**dqs1f_gating_counter**	dqs1f_gating_counter	Falling DQS gating counter for group 1
15:8	**dqs0r_gating_counter**	dqs0r_gating_counter	Rising DQS gating counter for group 0
7:0	**dqs0f_gating_counter**	dqs0f_gating_counter	Falling DQS gating counter for group 0

1020E3C4 **DQSGNWCNT1** **DQS Gating Window Counter 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dqs3r_gating_counter								dqs3f_gating_counter							

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Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**dqs2r_gating_counter**								**dqs2f_gating_counter**							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**dqs3r_gating_counter**	dqs3r_gating_counter	Rising DQS gating counter for group 3
23:16	**dqs3f_gating_counter**	dqs3f_gating_counter	Falling DQS gating counter for group 3
15:8	**dqs2r_gating_counter**	dqs2r_gating_counter	Rising DQS gating counter for group 2
7:0	**dqs2f_gating_counter**	dqs2f_gating_counter	Falling DQS gating counter for group 2

1020E3C8 DQSGNWCNT2 DQS Gating Window Counter 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**dqs0r_pre_gating_counter**								**dqs0f_pre_gating_counter**							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**dqs0r_pos_gating_counter**								**dqs0f_pos_gating_counter**							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**dqs0r_pre_gating_counter**	dqs0r_pre_gating_counter	Rising pre DQS gating counter for group 0
23:16	**dqs0f_pre_gating_counter**	dqs0f_pre_gating_counter	Falling pre DQS gating counter for group 0
15:8	**dqs0r_pos_gating_counter**	dqs0r_pos_gating_counter	Rising post DQS gating counter for group 0
7:0	**dqs0f_pos_gating_counter**	dqs0f_pos_gating_counter	Falling post DQS gating counter for group 0

1020E3CC DQSGNWCNT3 DQS Gating Window Counter 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**dqs1r_pre_gating_counter**								**dqs1f_pre_gating_counter**							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**dqs1r_pos_gating_counter**								**dqs1f_pos_gating_counter**							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31:24	**dqs1r_pre_gating_counter**	dqs1r_pre_gating_counter	Rising pre DQS gating counter for group 1
23:16	**dqs1f_pre_gating_counter**	dqs1f_pre_gating_counter	Falling pre DQS gating counter for group 1
15:8	**dqs1r_pos_gating_counter**	dqs1r_pos_gating_counter	Rising post DQS gating counter for group 1
7:0	**dqs1f_pos_gating_counter**	dqs1f_pos_gating_counter	Falling post DQS gating counter for group 1

1020E3D0 DQSGNWCNT4 DQS Gating Window Counter 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dqs2r_pre_gating_counter								dqs2f_pre_gating_counter							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dqs2r_pos_gating_counter								dqs2f_pos_gating_counter							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**dqs2r_pre_gating_counter**	dqs2r_pre_gating_counter	Rising pre DQS gating counter for group 2
23:16	**dqs2f_pre_gating_counter**	dqs2f_pre_gating_counter	Falling pre DQS gating counter for group 2
15:8	**dqs2r_pos_gating_counter**	dqs2r_pos_gating_counter	Rising post DQS gating counter for group 2
7:0	**dqs2f_pos_gating_counter**	dqs2f_pos_gating_counter	Falling post DQS gating counter for group 2

1020E3D4 DQSGNWCNT5 DQS Gating Window Counter 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dqs3r_pre_gating_counter								dqs3f_pre_gating_counter							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dqs3r_pos_gating_counter								dqs3f_pos_gating_counter							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**dqs3r_pre**	dqs3r_pre_gating_	Rising pre DQS gating counter for group 3

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Bit(s)	Mnemonic	Name	Description
	_gating_counter	counter	
23:16	**dqs3f_pre_gating_counter**	dqs3f_pre_gating_counter	Falling pre DQS gating counter for group 3
15:8	**dqs3r_pos_gating_counter**	dqs3r_pos_gating_counter	Rising post DQS gating counter for group 3
7:0	**dqs3f_pos_gating_counter**	dqs3f_pos_gating_counter	Falling post DQS gating counter for group 3

1020E3D8 DQSSAMPLEV DQS Sample Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name							CMPCNT									
Type							RO									
Reset							0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
9:4	**CMPCNT**	CMPCNT	CMP counter value

1020E3E8 CKPHCNT Clock Phase Detection Result 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CKPHCHKCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**CKPHCHKCNT**	CKPHCHKCNT	MEMPLL in/out clock phase detection result counter

1020E3FC TESTRPT Test Agent Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				CALI_DONE_MON				LB_CMP_FAIL						DLE_CNT_OK		
Type				RO				RO						RO		
Reset				0				0						0		
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name		DM_CMP_				DM_CMP_										

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		ERR				CPT										
Type		RO				RO										
Reset		0				0										

Bit(s)	Mnemonic	Name	Description
28	**CALI_DONE_MON**	CALI_DONE_MON	Calibration result is updated; SW can disable calibration
24	**LB_CMP_FAIL**	LB_CMP_FAIL	Loop-back test mode comparison fails.
18	**DLE_CNT_OK**	DLE_CNT_OK	DLE counter is right for Test Agent 2.
14	**DM_CMP_ERR**	DM_CMP_ERR	Read data comparison error for Test Agent 2
10	**DM_CMP_CPT**	DM_CMP_CPT	Read data comparison ready for Test Agent 2

1021300C PADCTL1 DRAM Pad Control 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CS1DLY				CLKDLY											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
31:28	**CS1DLY**	CS1DLY	**CS1 signal output delay** Bigger value means longer delay; 1 step = 20ps
27:24	**CLKDLY**	CLKDLY	**DRAM clock signal output delay** Bigger value means longer delay; 1 step = 20ps

10213010 PADCTL2 DRAM Pad Control 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQM3DLY				DQM2DLY				DQM1DLY				DQM0DLY			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:12	**DQM3DLY**	DQM3DLY	**DRAM DQM[3] signal output delay** Bigger value means longer delay; 1 step = 20ps
11:8	**DQM2DLY**	DQM2DLY	**DRAM DQM[2] signal output delay** Bigger value means longer delay; 1 step = 20ps
7:4	**DQM1DLY**	DQM1DLY	**DRAM DQM[1] signal output delay** Bigger value means longer delay; 1 step = 20ps
3:0	**DQM0DLY**	DQM0DLY	**DRAM DQM[0] signal output delay**

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Bit(s)	Mnemonic	Name	Description
			Bigger value means longer delay; 1 step = 20ps

10213014 PADCTL3 DRAM Pad Control 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DQS3ODLY				DQS2ODLY				DQS1ODLY				DQS0ODLY			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:12	**DQS3ODLY**	DQS3ODLY	**DRAM DQS3 signal output delay** Bigger value means longer delay; 1 step = 20ps
11:8	**DQS2ODLY**	DQS2ODLY	**DRAM DQS2 signal output delay** Bigger value means longer delay; 1 step = 20ps
7:4	**DQS1ODLY**	DQS1ODLY	**DRAM DQS1 signal output delay** Bigger value means longer delay; 1 step = 20ps
3:0	**DQS0ODLY**	DQS0ODLY	**DRAM DQS0 signal output delay** Bigger value means longer delay; 1 step = 20ps

10213028 DLLCONF DLL Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											WCKSEL2					
Type											RW					
Reset											0					
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
21	**WCKSEL2**	WCKSEL2	**Enables MIO_CK_DIV2 clocks input for MACRO_COM1 (data byte 2, 3)** 0: Disable 1: Enable

1021307C DDR2CTL DDR2 Control Register 00000080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		WLAT														
Type		RW														
Reset		0	0	0												
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name									IOPD							
Type									RW							
Reset									1							

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Bit(s)	Mnemonic	Name	Description
30:28	**WLAT**	WLAT	**Write latency for LPDDR/LPDDR2/DDR3: 3'b000/WLAT+1/WLAT+3** For example, DDR3 write latency = 5T, set WLAT = 2 Note: WLAT of LPDDR2 should further add 1T for 1T tDQSS spec. Unit: DRAM clock cycle
7	**IOPD**	IOPD	**0: PD is always 0.** 1: PD is controlled by HW.

10213090 **IOCTL** **IO Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SIOEN															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
31	**SIOEN**	SIOEN	**Enables DQS signal output** 0: Differential output 1: Single-end output

102130B8 **DRVCTL0** **PAD Driving Control Setting 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									DQSRTTBPJ				DQSRTTBNJ			
Type									RW				RW			
Reset									0				0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DQRTTBPJ				DQRTTBNJ			
Type									RW				RW			
Reset									0				0			

Bit(s)	Mnemonic	Name	Description
23	**DQSRTTBPJ**	DQSRTTBPJ	DQS PAD RTTBPJ port control
19	**DQSRTTBNJ**	DQSRTTBNJ	DQS PAD RTTBNJ port control
7	**DQRTTBPJ**	DQRTTBPJ	DQ PAD RTTBPJ port control
3	**DQRTTBNJ**	DQRTTBNJ	DQ PAD RTTBNJ port control

102130BC **DRVCTL1** **PAD Driving Control Setting 1** **AA00AA00**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	**CLKDRVP**				**CLKDRVN**				**CLKRTTBPJ**	**CKODTP**			**CLKRTTBNJ**	**CKODTN**		
Type	RW				RW				RW	RW			RW	RW		
Reset	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CMDDRVP**				**CMDDRVN**				**CMDRTTBPJ**	**CMDODTP**			**CMDRTTBNJ**	**CMDODTN**		
Type	RW				RW				RW	RW			RW	RW		
Reset	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28	**CLKDRVP**	CLKDRVP	**CLK P driving control** Refer to IBIST model for driving strength.
27:24	**CLKDRVN**	CLKDRVN	**CLK N driving control** Refer to IBIST model for driving strength.
23	**CLKRTTBPJ**	CLKRTTBPJ	**CLK PAD RTTBPJ port control**
22:20	**CKODTP**	CKODTP	**CLK ODT P driving control** Refer to IBIST model for driving strength.
19	**CLKRTTBNJ**	CLKRTTBNJ	**CLK PAD RTTBNJ port control**
18:16	**CKODTN**	CKODTN	**CLK ODT N driving control** Refer to IBIST model for driving strength.
15:12	**CMDDRVP**	CMDDRVP	**CMD P driving control** Refer to IBIST model for driving strength.
11:8	**CMDDRVN**	CMDDRVN	**CMD N driving control** Refer to IBIST model for driving strength.
7	**CMDRTTBPJ**	CMDRTTBPJ	**CMD PAD RTTBPJ port control**
6:4	**CMDODTP**	CMDODTP	**CMD ODT P driving control** Refer to IBIST model for driving strength.
3	**CMDRTTBNJ**	CMDRTTBNJ	**CMD PAD RTTBNJ port control**
2:0	**CMDODTN**	CMDODTN	**CMD ODT N driving control** Refer to IBIST model for driving strength.

102130C0 **DLLSEL** **DLL Selection Setting** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														**CMPCAL**	**CMPDRVNE**	**CMPDRVPE**
Type														RW	RW	RW
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**CMODTPE**				**CMODTNE**	**CMPODTN**		
Type									RW				RW	RW		
Reset									0				0	0	0	0

Bit(s)	Mnemonic	Name	Description
18	**CMPCAL**	CMPCAL	Connects to CMP pad CALP

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Bit(s)	Mnemonic	Name	Description
17	**CMPDRVNE**	CMPDRVNE	Connects to CMP pad DRVNE
16	**CMPDRVPE**	CMPDRVPE	Connects to CMP pad DRVPE
7	**CMODTPE**	CMODTPE	CMP PAD ODTPE port
3	**CMODTNE**	CMODTNE	CMP PAD ODTNE port
2:0	**CMPODTN**	CMPODTN	CMP ODT N driving control

102130CC TDSEL0 IO Output Duty Control 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**DQS3TDSEL**								**DQS2TDSEL**			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**CMDTDSEL**								**CLKTDSEL**			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:24	**DQS3TDSEL**	DQS3TDSEL	DQS3 output duty control
19:16	**DQS2TDSEL**	DQS2TDSEL	DQS2 output duty control
11:8	**CMDTDSEL**	CMDTDSEL	Command output duty control
3:0	**CLKTDSEL**	CLKTDSEL	DRAM clock output duty control

102130D0 TDSEL1 IO Output Duty Control 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**DQS1TDSEL**								**DQS0TDSEL**			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DQB3TDSEL**				**DQB2TDSEL**				**DQB1TDSEL**				**DQB0TDSEL**			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:24	**DQS1TDSEL**	DQS1TDSEL	DQS1 output duty control
19:16	**DQS0TDSEL**	DQS0TDSEL	DQS0 output duty control
15:12	**DQB3TDSEL**	DQB3TDSEL	DQ byte3 output duty control
11:8	**DQB2TDSEL**	DQB2TDSEL	DQ byte2 output duty control
7:4	**DQB1TDSEL**	DQB1TDSEL	DQ byte1 output duty control
3:0	**DQB0TDSEL**	DQB0TDSEL	DQ byte0 output duty control

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Bit(s)	Mnemonic	Name	Description
	L		

102130DC **DQSCTL0** **DQS Input Range Control 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									DQS1CTL[11:4]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQS1CTL[3:0]				DQS0CTL											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:12	**DQS1CTL**	DQS1CTL	**DQS1 input range control, 1 hot encoding** Unit: 1/2 DRAM clock cycle
11:0	**DQS0CTL**	DQS0CTL	**DQS0 input range control, 1 hot encoding** Unit: 1/2 DRAM clock cycle

102130E0 **DQSCTL1** **DQS Input Range Control 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									DQS3CTL[11:4]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQS3CTL[3:0]				DQS2CTL											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:12	**DQS3CTL**	DQS3CTL	**DQS3 input range control, 1 hot encoding** Unit: 1/2 DRAM clock cycle
11:0	**DQS2CTL**	DQS2CTL	**DQS2 input range control, 1 hot encoding** Unit: 1/2 DRAM clock cycle

102130E4 **PADCTL4** **PAD Control 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CLKPADCTL				CMDPADCTL				DQSPADCTL				DQPADCTL			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DQSRTT				DQRTT										
Type		RW				RW										
Reset		0	0	0		0	0	0								

Bit(s)	Mnemonic	Name	Description
31:28	**CLKPADCTL**	CLKPADCTL	Clock pad control

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Bit(s)	Mnemonic	Name	Description
27:24	**CMDPADCTL**	CMDPADCTL	CMD pad control
23:20	**DQSPADCTL**	DQSPADCTL	DQS pad control
19:16	**DQPADCTL**	DQPADCTL	DQ pad control
14:12	**DQSRTT**	DQSRTT	DQS termination control
10:8	**DQRTT**	DQRTT	DQ termination control

102130E8 **PADCTL5** **PAD Control 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			**DQS3RDSEL**								**DQS2RDSEL**					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**DQS1RDSEL**								**DQS0RDSEL**					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:24	**DQS3RDSEL**	DQS3RDSEL	**DQS 3 RDSEL (duty cycle control)** Unit: 50ps
21:16	**DQS2RDSEL**	DQS2RDSEL	**DQS 2 RDSEL (duty cycle control)** Unit: 50ps
13:8	**DQS1RDSEL**	DQS1RDSEL	**DQS 1 RDSEL (duty cycle control)** Unit: 50ps
5:0	**DQS0RDSEL**	DQS0RDSEL	**DQS 0 RDSEL (duty cycle control)** Unit: 50ps

102130EC **PADCTL6** **PAD Control 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			**DQ3RDSEL**								**DQ2RDSEL**					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**DQ1RDSEL**								**DQ0RDSEL**					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:24	**DQ3RDSEL**	DQ3RDSEL	**DQ Byte 3 RDSEL (duty cycle control)** Unit: 50ps
21:16	**DQ2RDSEL**	DQ2RDSEL	**DQ Byte 2 RDSEL (duty cycle control)** Unit: 50ps
13:8	**DQ1RDSEL**	DQ1RDSEL	**DQ Byte 1 RDSEL (duty cycle control)** Unit: 50ps
5:0	**DQ0RDSEL**	DQ0RDSEL	**DQ Byte 0 RDSEL (duty cycle control)** Unit: 50ps

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102130F0 **PHYCTL1** **DDR PHY Control 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				PHYRST				FIXDQSIEN								
Type				RW				RW								
Reset				0				0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
28	**PHYRST**	PHYRST	**Enables PHY reset** 0: Disable 1: Enable
24	**FIXDQSIEN**	FIXDQSIEN	**DQS input enable always on** 0: Hardware control 1: Always on

102130F4 **GDDR3CTL1** **GDDR3 Control 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				PHYSYNCM												
Type				RW												
Reset				0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
28	**PHYSYNCM**	PHYSYNCM	Sync mode uses inverted PHY_M_CK.

102130FC **MISCTL0** **MISC Control 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															INTLBT	MODE18V
Type															RW	RW
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
17	**INTLBT**	INTLBT	**IO internal loop back** 0: Disable

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Bit(s)	Mnemonic	Name	Description
			1: Enable
16	**MODE18V**	MODE18V	**IO voltage operating condition** 0: 1.2V 1: 1.8V

10213124 DQSGCTL Input DQS Gating Control AA080000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**NEWDQSG_SEL**	**RESERVEd_0x124**												**BYPASS_DMPAD_COM1**	**BYPASS_DMPAD_COM0**	**DMYPAD_RXSEL**
Type	RW	RW												RW	RW	RW
Reset	1	0	1	0	1	0	1	0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DQSG_FINE_DLY_COM1**				**DQSG_FINE_DLY_COM0**											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
31	**NEWDQSG_SEL**	NEWDQSG_SEL	**DQS gating control method** 0: Old 1: New
18	**BYPASS_DMPAD_COM1**	BYPASS_DMPAD_COM1	**Bypasses dummy PAD for DQS2/3 gating signal** 0: Does not bypass 1: Bypass
17	**BYPASS_DMPAD_COM0**	BYPASS_DMPAD_COM0	**Bypasses dummy PAD for DQS0/1 gating signal** 0: Does not bypass 1: Bypass
16	**DMYPAD_RXSEL**	DMYPAD_RXSEL	**Selects O/O1 pin of dummy PAD for gating signal input** 0: O pin 1: O1 pin
15:12	**DQSG_FINE_DLY_COM1**	DQSG_FINE_DLY_COM1	**Fine-tunes delay setting for DQS2/3 gating signal before dummy PAD** Unit: 20ps
11:8	**DQSG_FINE_DLY_COM0**	DQSG_FINE_DLY_COM0	**Fine-tunes delay setting for DQS1/0 gating signal before dummy PAD** Unit: 20ps

10213140 DQSGCTL1 DQS Gating Delay Control 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**DQSIPRE1DLY**								**DQSIPOS1DLY**						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**DQSIPRE0DLY**								**DQSIPOS0DLY**						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
30:24	**DQSIPRE1 DLY**	DQSIPRE1DLY	DQS PRE delay control for DQS1
22:16	**DQSIPOS1 DLY**	DQSIPOS1DLY	DQS POS delay control for DQS1
14:8	**DQSIPRE0 DLY**	DQSIPRE0DLY	DQS PRE delay control for DQS0
6:0	**DQSIPOS0 DLY**	DQSIPOS0DLY	DQS POS delay control for DQS0

10213144 DQSGCTL2 DQS Gating Delay Control 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DQSIPRE3DLY								DQSIPOS3DLY						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DQSIPRE2DLY								DQSIPOS2DLY						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:24	**DQSIPRE3 DLY**	DQSIPRE3DLY	DQS PRE delay control for DQS3
22:16	**DQSIPOS3 DLY**	DQSIPOS3DLY	DQS POS delay control for DQS3
14:8	**DQSIPRE2 DLY**	DQSIPRE2DLY	DQS PRE delay control for DQS2
6:0	**DQSIPOS2 DLY**	DQSIPOS2DLY	DQS POS delay control for DQS2

102131A8 CMDDLY0 Command Delay CTL0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RA3DLY								RA2DLY			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RA1DLY								RA0DLY			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:24	**RA3DLY**	RA3DLY	**RA output delay chain setting for bit 3** Unit: 20ps
19:16	**RA2DLY**	RA2DLY	**RA output delay chain setting for bit 2** Unit: 20ps
11:8	**RA1DLY**	RA1DLY	**RA output delay chain setting for bit 1** Unit: 20ps
3:0	**RA0DLY**	RA0DLY	**RA output delay chain setting for bit 0** Unit: 20ps

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102131AC CMDDLY1 Command Delay CTL1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RA7DLY								RA6DLY			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RA5DLY								RA4DLY			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:24	**RA7DLY**	RA7DLY	**RA output delay chain setting for bit 7** Unit: 20ps
19:16	**RA6DLY**	RA6DLY	**RA output delay chain setting for bit 6** Unit: 20ps
11:8	**RA5DLY**	RA5DLY	**RA output delay chain setting for bit 5** Unit: 20ps
3:0	**RA4DLY**	RA4DLY	**RA output delay chain setting for bit 4** Unit: 20ps

102131B0 CMDDLY2 Command Delay CTL2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RA11DLY								RA10DLY			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RA9DLY								RA8DLY			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:24	**RA11DLY**	RA11DLY	**RA output delay chain setting for bit 11** Unit: 20ps
19:16	**RA10DLY**	RA10DLY	**RA output delay chain setting for bit 10** Unit: 20ps
11:8	**RA9DLY**	RA9DLY	**RA output delay chain setting for bit 9** Unit: 20ps
3:0	**RA8DLY**	RA8DLY	**RA output delay chain setting for bit 8** Unit: 20ps

102131B4 CMDDLY3 Command Delay CTL3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					BA2DLY								BA1DLY			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					BA0DLY								RA12DLY			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

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Bit(s)	Mnemonic	Name	Description
27:24	**BA2DLY**	BA2DLY	**BA output delay chain setting for bit 2** Unit: 20ps
19:16	**BA1DLY**	BA1DLY	**BA output delay chain setting for bit 1** Unit: 20ps
11:8	**BA0DLY**	BA0DLY	**BA output delay chain setting for bit 0** Unit: 20ps
3:0	**RA12DLY**	RA12DLY	**RA output delay chain setting for bit 12** Unit: 20ps

102131B8 CMDDLY4 Command Delay CTL4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				CASDLY								RASDLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CKEDLY								CSDLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	**CASDLY**	CASDLY	**CAS output delay chain setting** Unit: 20ps
20:16	**RASDLY**	RASDLY	**RAS output delay chain setting** Unit: 20ps
12:8	**CKEDLY**	CKEDLY	**CKE output delay chain setting** Unit: 20ps
4:0	**CSDLY**	CSDLY	**CS output delay chain setting** Unit: 20ps

102131BC CMDDLY5 Command Delay CTL5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				OTDLY								RA13DLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WEDLY												
Type				RW												
Reset				0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
28:24	**OTDLY**	OTDLY	**OTD output delay chain setting** Unit: 20ps
20:16	**RA13DLY**	RA13DLY	**RA output delay chain setting for bit 13** Unit: 20ps
12:8	**WEDLY**	WEDLY	**WE output delay chain setting** Unit: 20ps

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102131C0 DQSCAL0 DQS CAL Control 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RA14DLY								RA15DLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
28:24	**RA14DLY**	RA14DLY	**RA output delay chain setting for bit 14** Unit: 20ps
20:16	**RA15DLY**	RA15DLY	**RA output delay chain setting for bit 15** Unit: 20ps

102131E0 LPDDR2_3 LPDDR2/LPDDR3 Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		SELO1ASO	DDRA14			FASTOE	DDRA15	DDRCS1		DDRODT	DDRCKE	DDRCS	DDRRAS	DDRCAS	DDRWE	DDRBA[2:2]
Type		RW	RW			RW	RW	RW		RW	RW	RW	RW	RW	RW	RW
Reset		0	0			0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DDRBA[1:0]		DDRA													
Type	RW		RW													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30	**SELO1ASO**	SELO1ASO	**Selects IO O1 as output** 0: Select O 1: Select O1
29	**DDRA14**	DDRA14	**DDR mode for A[14] pin (PDDR2/3 DDR command rate)** 0: Disable 1: Enable
26	**FASTOE**	FASTOE	**Enables fast IO output** 0: Disable 1: Enable
25	**DDRA15**	DDRA15	**DDR mode for A[15] pin (LPDDR2/3 DDR command rate)** 0: Disable 1: Enable
24	**DDRCS1**	DDRCS1	**DDR mode for CS1 pin (LPDDR2/3 DDR command rate)** 0: Disable 1: Enable
22	**DDRODT**	DDRODT	**DDR mode for ODT pin (LPDDR2/3 DDR command rate)** 0: Disable 1: Enable
21	**DDRCKE**	DDRCKE	**DDR mode for CKE pin (LPDDR2/3 DDR command rate)** 0: Disable 1: Enable

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Bit(s)	Mnemonic	Name	Description
20	**DDRCS**	DDRCS	**DDR mode for CS pin (LPDDR2/3 DDR command rate)** 0: Disable 1: Enable
19	**DDRRAS**	DDRRAS	**DDR mode for RAS pin (LPDDR2/3 DDR command rate)** 0: Disable 1: Enable
18	**DDRCAS**	DDRCAS	**DDR mode for CAS pin (LPDDR2/3 DDR command rate)** 0: Disable 1: Enable
17	**DDRWE**	DDRWE	**DDR mode for WE pin (LPDDR2/3 DDR command rate)** 0: Disable 1: Enable
16:14	**DDRBA**	DDRBA	**DDR mode for BA[2:0] pin (LPDDR2/3 DDR command rate)** 0: Disable 1: Enable
13:0	**DDRA**	DDRA	**DDR mode for A[13:0] pin (LPDDR2/3 DDR command rate)** 0: Disable 1: Enable

102131E4 **SPCMD** **Special Command Mode** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					IORINGTIMER											
Type					RW											
Reset					0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			CMPPD													
Type			RW													
Reset			0													

Bit(s)	Mnemonic	Name	Description
27:24	**IORINGTIMER**	IORINGTIMER	Set up [11:8] of IO ring timer counter value where [7:0] is 8'hff.
13	**CMPPD**	CMPPD	Powers down control of CMP IO

10213200 **DQODLY1** **DQ Output Delay 1 Chain Setting** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQ7DLY				DQ6DLY				DQ5DLY				DQ4DLY			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQ3DLY				DQ2DLY				DQ1DLY				DQ0DLY			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28	**DQ7DLY**	DQ7DLY	**DQ output delay chain setting for bit 7** Unit: 20ps

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Bit(s)	Mnemonic	Name	Description
27:24	**DQ6DLY**	DQ6DLY	**DQ output delay chain setting for bit 6** Unit: 20ps
23:20	**DQ5DLY**	DQ5DLY	**DQ output delay chain setting for bit 5** Unit: 20ps
19:16	**DQ4DLY**	DQ4DLY	**DQ output delay chain setting for bit 4** Unit: 20ps
15:12	**DQ3DLY**	DQ3DLY	**DQ output delay chain setting for bit 3** Unit: 20ps
11:8	**DQ2DLY**	DQ2DLY	**DQ output delay chain setting for bit 2** Unit: 20ps
7:4	**DQ1DLY**	DQ1DLY	**DQ output delay chain setting for bit 1** Unit: 20ps
3:0	**DQ0DLY**	DQ0DLY	**DQ output delay chain setting for bit 0** Unit: 20ps

10213204 **DQODLY2** **DQ Output Delay 2 Chain Setting** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DQ15DLY**				**DQ14DLY**				**DQ13DLY**				**DQ12DLY**			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DQ11DLY**				**DQ10DLY**				**DQ9DLY**				**DQ8DLY**			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28	**DQ15DLY**	DQ15DLY	**DQ output delay chain setting for bit 15** Unit: 20ps
27:24	**DQ14DLY**	DQ14DLY	**DQ output delay chain setting for bit 14** Unit: 20ps
23:20	**DQ13DLY**	DQ13DLY	**DQ output delay chain setting for bit 13** Unit: 20ps
19:16	**DQ12DLY**	DQ12DLY	**DQ output delay chain setting for bit 12** Unit: 20ps
15:12	**DQ11DLY**	DQ11DLY	**DQ output delay chain setting for bit 11** Unit: 20ps
11:8	**DQ10DLY**	DQ10DLY	**DQ output delay chain setting for bit 10** Unit: 20ps
7:4	**DQ9DLY**	DQ9DLY	**DQ output delay chain setting for bit 9** Unit: 20ps
3:0	**DQ8DLY**	DQ8DLY	**DQ output delay chain setting for bit 8** Unit: 20ps

10213208 **DQODLY3** **DQ Output Delay 3 Chain Setting** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DQ23DLY**				**DQ22DLY**				**DQ21DLY**				**DQ20DLY**			
Type	RW				RW				RW				RW			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DQ19DLY**				**DQ18DLY**				**DQ17DLY**				**DQ16DLY**			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28	**DQ23DLY**	DQ23DLY	**DQ output delay chain setting for bit 23** Unit: 20ps
27:24	**DQ22DLY**	DQ22DLY	**DQ output delay chain setting for bit 22** Unit: 20ps
23:20	**DQ21DLY**	DQ21DLY	**DQ output delay chain setting for bit 21** Unit: 20ps
19:16	**DQ20DLY**	DQ20DLY	**DQ output delay chain setting for bit 20** Unit: 20ps
15:12	**DQ19DLY**	DQ19DLY	**DQ output delay chain setting for bit 19** Unit: 20ps
11:8	**DQ18DLY**	DQ18DLY	**DQ output delay chain setting for bit 18** Unit: 20ps
7:4	**DQ17DLY**	DQ17DLY	**DQ output delay chain setting for bit 17** Unit: 20ps
3:0	**DQ16DLY**	DQ16DLY	**DQ output delay chain setting for bit 16** Unit: 20ps

1021320C **DQODLY4** **DQ Output Delay 4 Chain Setting** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DQ31DLY**				**DQ30DLY**				**DQ29DLY**				**DQ28DLY**			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DQ27DLY**				**DQ26DLY**				**DQ25DLY**				**DQ24DLY**			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28	**DQ31DLY**	DQ31DLY	**DQ output delay chain setting for bit 31** Unit: 20ps
27:24	**DQ30DLY**	DQ30DLY	**DQ output delay chain setting for bit 30** Unit: 20ps
23:20	**DQ29DLY**	DQ29DLY	**DQ output delay chain setting for bit 29** Unit: 20ps
19:16	**DQ28DLY**	DQ28DLY	**DQ output delay chain setting for bit 28** Unit: 20ps
15:12	**DQ27DLY**	DQ27DLY	**DQ output delay chain setting for bit 27** Unit: 20ps
11:8	**DQ26DLY**	DQ26DLY	**DQ output delay chain setting for bit 26** Unit: 20ps
7:4	**DQ25DLY**	DQ25DLY	**DQ output delay chain setting for bit 25** Unit: 20ps
3:0	**DQ24DLY**	DQ24DLY	**DQ output delay chain setting for bit 24**

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Bit(s)	Mnemonic	Name	Description
			Unit: 20ps

10213380 **CATRAIN_WLEV_FEEDBACK** **DQ_O1_PATH_FEEDBACK** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQ_O1[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQ_O1[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DQ_O1**	DQ_O1	DQ O1 path feedback for CA training and write leveling

1021338C **STBEN0** **DQS Ring Counter 0** **00000003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STBEN0[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STBEN0[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
31:0	**STBEN0**	STBEN0	DQS0 ring counter

10213390 **STBEN1** **DQS Ring Counter 1** **00000003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STBEN1[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STBEN1[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
31:0	**STBEN1**	STBEN1	DQS1 ring counter

10213394 **STBEN2** **DQS Ring Counter 2** **00000003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STBEN2[31:16]															

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Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**STBEN2[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
31:0	**STBEN2**	STBEN2	DQS2 ring counter

10213398 STBEN3 DQS Ring Counter 3 00000003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**STBEN3[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**STBEN3[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
31:0	**STBEN3**	STBEN3	DQS3 ring counter

102133DC CMPOUT CMP output 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CMPOP**	**CMPON**														
Type	RO	RO														
Reset	0	0														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
31	**CMPOP**	CMPOP	Calibration output results from P-side impedance
30	**CMPON**	CMPON	Calibration output results from N-side impedance

102135C0 MPLLPON0 MEMPLL Power On Sequence Setting 0 21581B1B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**BIAS_EN_STB_TIME**								**BIAS_LPF_EN_STB_TIME**							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	1	0	1	0	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MEMPLL_EN_STB_TIME**								**DMALL_CK_EN_STB_TIME**							
Type	RW								RW							
Reset	0	0	0	1	1	0	1	1	0	0	0	1	1	0	1	1

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
31:24	BIAS_EN_STB_TIME	BIAS_EN_STB_TIME	**Selects de-bounce time for MEMPLL BIAS_EN signal** Unit: 3.125us
23:16	BIAS_LPF_EN_STB_TIME	BIAS_LPF_EN_STB_TIME	**Selects De-bounce time for MEMPLL BIAS_LPF_EN signal** Unit: 3.125us
15:8	MEMPLL_EN_STB_TIME	MEMPLL_EN_STB_TIME	**Selects De-bounce time for MEMPLL_EN signal** Unit: 0.0385us
7:0	DMALL_CK_EN_STB_TIME	DMALL_CK_EN_STB_TIME	**Selects De-bounce time for DMALL_CK_EN signal** Unit: 0.0385us

102135C4 MPLLPON1 MEMPLL Power On Sequence Setting 1 5096961E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DDSEN_STB_TIME								DIV_EN_STB_TIME							
Type	RW								RW							
Reset	0	1	0	1	0	0	0	0	1	0	0	1	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMPLL2_CK_EN_STB_TIME								ISO_EN_STB_TIME							
Type	RW								RW							
Reset	1	0	0	1	0	1	1	0	0	0	0	1	1	1	1	0

Bit(s)	Mnemonic	Name	Description
31:24	DDSEN_STB_TIME	DDSEN_STB_TIME	**Selects De-bounce time for MEMPLL DDSEN signal** Unit: 0.0385us
23:16	DIV_EN_STB_TIME	DIV_EN_STB_TIME	**Selects De-bounce time for MEMPLL DIV_EN signal** Unit: 0.154us
15:8	DMPLL2_CK_EN_STB_TIME	DMPLL2_CK_EN_STB_TIME	**Selects De-bounce time for DMPLL2_CK_EN signal** Unit: 0.154us
7:0	ISO_EN_STB_TIME	ISO_EN_STB_TIME	**Selects De-bounce time for MEMPLL ISO_EN signal** Unit: 3.125us

102135C8 MPLLPON2 MEMPLL Power On Sequence Setting 2 01010F01

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				BIAS_EN_STB_EN				BIAS_EN_SRC_SEL				BIAS_LPF_EN_STB_EN				BIAS_LPF_EN_SRC_SEL
Type				RW				RW				RW				RW
Reset				0				1				0				1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEMPLL4_EN_STB_EN	MEMPLL3_EN_STB_EN	MEMPLL2_EN_STB_EN	MEMPLL_EN_STB_EN	MEMPLL4_EN_SRC_SEL	MEMPLL3_EN_SRC_SEL	MEMPLL2_EN_SRC_SEL	MEMPLL_EN_SRC_SEL				DMALL_CK_EN_STB_EN				DMALL_CK_EN_SRC_SEL
Type	RW	RW	RW	RW	RW	RW	RW	RW				RW				RW
Reset	0	0	0	0	1	1	1	1				0				1

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Bit(s)	Mnemonic	Name	Description
28	**BIAS_EN_STB_EN**	BIAS_EN_STB_EN	**Enables MEMPLL BIAS_EN de-bounce** 1'b0: Does not de-bounce 1'b1: Enable de-bounce
24	**BIAS_EN_SRC_SEL**	BIAS_EN_SRC_SEL	**Selects MEMPLL BIAS_EN source** 1'b0: Control signal from sc_apbias_off 1'b1: Control signal from RG_MEMPLL_BIAS_EN (0x604[14])
20	**BIAS_LPF_EN_STB_EN**	BIAS_LPF_EN_STB_EN	**Enables MEMPLL BIAS_LPF_EN de-bounce** 1'b0: Does not de-bounce 1'b1: Enable de-bounce
16	**BIAS_LPF_EN_SRC_SEL**	BIAS_LPF_EN_SRC_SEL	**Selects MEMPLL BIAS_LPF_EN source** 1'b0: Control signal from sc_apbias_off 1'b1: Control signal from RG_MEMPLL_BIAS_LPF_EN (0x604[15])
15	**MEMPLL4_EN_STB_EN**	MEMPLL4_EN_STB_EN	**Enables MEMPLL4_EN de-bounce** 1'b0: Does not de-bounce 1'b1: Enable de-bounce
14	**MEMPLL3_EN_STB_EN**	MEMPLL3_EN_STB_EN	**Enables MEMPLL3_EN de-bounce** 1'b0: Does not de-bounce 1'b1: Enable de-bounce
13	**MEMPLL2_EN_STB_EN**	MEMPLL2_EN_STB_EN	**Enables MEMPLL2_EN de-bounce** 1'b0: Does not de-bounce 1'b1: Enable de-bounce
12	**MEMPLL_EN_STB_EN**	MEMPLL_EN_STB_EN	**Enables MEMPLL_EN de-bounce** 1'b0: Does not de-bounce 1'b1: Enable de-bounce
11	**MEMPLL4_EN_SRC_SEL**	MEMPLL4_EN_SRC_SEL	**Selects MEMPLL4_EN source** 1'b0: Control signal from sc_mempll3_off 1'b1: Control signal from RG_MEMPLL4_EN (0x61c[18])
10	**MEMPLL3_EN_SRC_SEL**	MEMPLL3_EN_SRC_SEL	**Selects MEMPLL3_EN source** 1'b0: Control signal from sc_mempll3_off 1'b1: Control signal from RG_MEMPLL3_EN (0x614[18])
9	**MEMPLL2_EN_SRC_SEL**	MEMPLL2_EN_SRC_SEL	**Selects MEMPLL2_EN source** 1'b0: Control signal from sc_apbias_off 1'b1: Control signal from RG_MEMPLL2_EN(0x60c[18])
8	**MEMPLL_EN_SRC_SEL**	MEMPLL_EN_SRC_SEL	**Selects MEMPLL_EN source** 1'b0: Control signal from sc_mempll1_off 1'b1: Control signal from RG_MEMPLL_EN (0x600[2])
4	**DMALL_CK_EN_STB_EN**	DMALL_CK_EN_STB_EN	**Enables DMALL_CK_EN de-bounce** 1'b0: Does not de-bounce 1'b1: Enable de-bounce
0	**DMALL_CK_EN_SRC_SEL**	DMALL_CK_EN_SRC_SEL	**Selects DMALL_CK_EN source** 1'b0: Control signal from sc_mempllout_off 1'b1: Control signal from R_DMALLCLK_EN (0x640[4])

102135CC **MPLLPON3** **MEMPLL Power On Sequence Setting 3** **01010101**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**DDSEN_STB_EN**				**DDSEN_SRC_SEL**		**DIV_EN_SRC_SEL**		**DIV_EN_STB_EN**				**DIV_EN_SRC_SEL**
Type				RW				RW		RW		RW				RW
Reset				0				1		0		0				1

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DMPLL2CLK_EN_STB_EN				DMPLL2CLK_EN_SRC_SEL				ISO_EN_STB_EN				ISO_EN_SRC_SEL
Type				RW				RW				RW				RW
Reset				0				1				0				1

Bit(s)	Mnemonic	Name	Description
28	**DDSEN_STB_EN**	DDSEN_STB_EN	**Enables MEMPLL DDSEN de-bounce** 1'b0: Does not de-bounce 1'b1: Enable de-bounce
24	**DDSEN_SRC_SEL**	DDSEN_SRC_SEL	**Selects MEMPLL DDSEN source** 1'b0: Control signal from sc_mempll2_off 1'b1: Control signal from RG_MEMPLL_DDSEN (0x600[25])
22	**DIV_EN_SC_SRC_SEL**	DIV_EN_SC_SRC_SEL	**Selects SC DIV_EN source** 1'b0: Control signal from sc_mempll2_off 1'b1: Control signal from sc_mempll1_off
20	**DIV_EN_STB_EN**	DIV_EN_STB_EN	**MEMPLL DIV_EN de-bounce** 1'b0: Does not de-bounce 1'b1: Enable de-bounce
16	**DIV_EN_SRC_SEL**	DIV_EN_SRC_SEL	**Selects MEMPLL DIV_EN source** 1'b0: Control signal from sc_mempll1_off or sc_mempll2_off 1'b1: Control signal from RG_MEMPLL_DIV_EN (0x604[24])
12	**DMPLL2CLK_EN_STB_EN**	DMPLL2CLK_EN_STB_EN	**Enables DMPLL2CLK_EN de-bounce** 1'b0: Does not de-bounce 1'b1: Enable de-bounce
8	**DMPLL2CLK_EN_SRC_SEL**	DMPLL2CLK_EN_SRC_SEL	**Selects DMPLL2CLK_EN source** 1'b0: Control signal from sc_memplllout_off 1'b1: Control signal from RG_DMPLL2CLK_EN (0x640[5])
4	**ISO_EN_STB_EN**	ISO_EN_STB_EN	**Enables ISO_EN_STB_EN de-bounce** 1'b0: Does not de-bounce 1'b1: Enable de-bounce
0	**ISO_EN_SRC_SEL**	ISO_EN_SRC_SEL	**Selects ISO_EN source** 1'b0: Control signal from sc_memplllout_off 1'b1: Control signal from RG_DMPLL2CLK_EN (0x620[3])

10213600 **MEMPLL0** **MEMPLL Register Setting 0** **044C8000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_MEMPLL_VCO_DIF_EN	RG_MEMPLL_CKCTRL		RG_MEMPLL_ACCEN	RG_MEMPLL_FBKSEL		RG_MEMPLL_DDSEN	RG_MEMPLL_FBDIV							RG_MEMPLL_PREDIV	
Type	RW	RW		RW	RW		RW	RW							RW	
Reset	0	0	0	0	0	1	0	0	0	1	0	0	1	1	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RG_MEMPLL_POSDIV		RG_MEMPLL_VCODIV_SEL	RG_MEMPLL_BLP	RG_MEMPLL_BP	RG_MEMPLL_BR	RG_MEMPLL_BC	RG_MEMPLL_DIVEN			RG_MEMPLL_MONCK_EN	RG_MEMPLL_MONVC_EN	RG_MEMPLL_MONREF_EN	RG_MEMPLL_EN	RG_MEMPLL_RST_DLY	

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Type	RW		RW	RW	RW	RW	RW	RW			RW	RW	RW	RW	RW	
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**RG_MEMPLL_VCO_DIF_EN**	RG_MEMPLL_VCO_DIF_EN	**Removed in design**
30:29	**RG_MEMPLL_CKCTRL**	RG_MEMPLL_CKCTRL	**Removed in design**
28	**RG_MEMPLL_ACCEN**	RG_MEMPLL_ACCEN	**Removed in design**
27:26	**RG_MEMPLL_FBKSEL**	RG_MEMPLL_FBKSEL	**Removed in design**
25	**RG_MEMPLL_DDSEN**	RG_MEMPLL_DDSEN	**Removed in design**
24:18	**RG_MEMPLL_FBDIV**	RG_MEMPLL_FBDIV	**Removed in design**
17:16	**RG_MEMPLL_PREDIV**	RG_MEMPLL_PREDIV	**Pre-divider ratio of MEMPLL** 2'b00: Fref = Fin/1 2'b01: Fref = Fin/2 2'b1X: Fref = Fin/4
15:14	**RG_MEMPLL_POSDIV**	RG_MEMPLL_POSDIV	**Post-divider ratio for single-end clock output of MEMPLL** 2'b00: VCO/1 2'b01: VCO/2 2'b1X: VCO/4
13	**RG_MEMPLL_VCO_DIV_SEL**	RG_MEMPLL_VCO_DIV_SEL	**Selects VCO div2 of MEMPLL** 1'b0: /1 1'b1: /2
12	**RG_MEMPLL_BLP**	RG_MEMPLL_BLP	**Selects LPF bandwidth of MEMPLL** 1'b0: 40MHz 1'b1: 20MHz
11	**RG_MEMPLL_BP**	RG_MEMPLL_BP	**Adjusts capacitance for bandwidth of MEMPLL** 1'b0: When RG_PLL_BR=1'b0 1'b1: When RG_PLL_BR=1'b1
10	**RG_MEMPLL_BR**	RG_MEMPLL_BR	**Adjusts resistance for bandwidth of MEMPLL** 1'b0: BW = Fref/10 1'b1: BW = Fref/20
9	**RG_MEMPLL_BC**	RG_MEMPLL_BC	**Removed in design**
8:6	**RG_MEMPLL_DIVEN**	RG_MEMPLL_DIVEN	**Removed in design**
5	**RG_MEMPLL_MONCK_EN**	RG_MEMPLL_MONCK_EN	**Enables monitor VCO clock for debugging of MEMPLL** 1'b0: Disable 1'b1: Enable
4	**RG_MEMPLL_MONVC_EN**	RG_MEMPLL_MONVC_EN	**Enables monitor Vctrl voltage for debugging of MEMPLL** 1'b0: Disable 1'b1: Enable
3	**RG_MEMPLL_MONREF_EN**	RG_MEMPLL_MONREF_EN	**Enables PFD clock out for frequency meter of MEMPLL** 1'b0: Disable 1'b1: Enable
2	**RG_MEMPLL_EN**	RG_MEMPLL_EN	**Enables MEMPLL** 1'b0: Disable

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Bit(s)	Mnemonic	Name	Description
			1'b1: Enable
1:0	**RG_MEMPLL_RST_DLY**	RG_MEMPLL_RST_DLY	

10213604 **MEMPLL1** **MEMPLL Register Setting 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_MEMPLL_DIV							RG_MEMPLL_DIV_EN	RG_MEMPLL_RESERVE							
Type	RW							RW	RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_MEMPLL_BIAS_LPF_EN	RG_MEMPLL_BIAS_EN	RG_MEMPLL_RESERVE1[5]	RG_MEMPLL_RESERVE1[4]	RG_MEMPLL_RESERVE1[3]	RG_MEMPLL_RESERVE1[2]	RG_MEMPLL_RESERVE1[1]	RG_MEMPLL_RESERVE1[0]	RG_MEMPLL_TEST[7]	RG_MEMPLL_TEST[6:5]		RG_MEMPLL_TEST[4]	RG_MEMPLL_TEST[3]	RG_MEMPLL_TEST[2]	RG_MEMPLL_TEST[1]	RG_MEMPLL_TEST[0]
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25	**RG_MEMPLL_DIV**	RG_MEMPLL_DIV	**Control bits of Divider for (APLL+DDS) of MEMPLL**
24	**RG_MEMPLL_DIV_EN**	RG_MEMPLL_DIV_EN	**Enables the Divider for (APLL+DDS) of MEMPLL**
23:16	**RG_MEMPLL_RESERVE**	RG_MEMPLL_RESERVE	
15	**RG_MEMPLL_BIAS_LPF_EN**	RG_MEMPLL_BIAS_LPF_EN	**Enables Constant-Gm bias LPF of MEMPLL** 1'b0: Bypass LPF 1'b1: Enable LPF
14	**RG_MEMPLL_BIAS_EN**	RG_MEMPLL_BIAS_EN	**Enables Constant-Gm bias of MEMPLL** 1'b0: Disable 1'b1: Enable
13	**RG_MEMPLL_RESERVE1[5]**	RG_MEMPLL_RESERVE1_5	
12	**RG_MEMPLL_RESERVE1[4]**	RG_MEMPLL_RESERVE1_4	
11	**RG_MEMPLL_RESERVE1[3]**	RG_MEMPLL_RESERVE1_3	
10	**RG_MEMPLL_RESERVE1[2]**	RG_MEMPLL_RESERVE1_2	
9	**RG_MEMPLL_RESERVE1[1]**	RG_MEMPLL_RESERVE1_1	

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Bit(s)	Mnemonic	Name	Description
8	RG_MEMPLL_RESERVE1[0]	RG_MEMPLL_RESERVE1_0	
7	RG_MEMPLL_TEST[7]	RG_MEMPLL_TEST_7	**Enables test circuit monitor clock of MEMPLL** 1'b0: Off 1'b1: On
6:5	RG_MEMPLL_TEST[6:5]	RG_MEMPLL_TEST_6_5	**Adjusts open drain current of MEMPLL** 2'b00: 10mA 2'b01: 20mA 2'b10: 30mA 2'b11: 40mA
4	RG_MEMPLL_TEST[4]	RG_MEMPLL_TEST_4	**Enables test circuit open drain of MEMPLL** 1'b0: Off 1'b1: On
3	RG_MEMPLL_TEST[3]	RG_MEMPLL_TEST_3	**Enables test circuit of MEMPLL** 1'b0: Off 1'b1: On
2	RG_MEMPLL_TEST[2]	RG_MEMPLL_TEST_2	
1	RG_MEMPLL_TEST[1]	RG_MEMPLL_TEST_1	
0	RG_MEMPLL_TEST[0]	RG_MEMPLL_TEST_0	

10213608 MEMPLL2 MEMPLL Register Setting 2 0000044C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_MEMPLL_TST_SEL								RG_MEMPLL_TEST[15:8]							
Type	RW								RW							
Reset	0	0	0	0					0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RG_MEMPLL2_VCO_DIF_EN	RG_MEMPLL2_CKCTRL		RG_MEMPLL2_ACCEN	RG_MEMPLL2_FBKSEL		RG_MEMPLL2_DDSEN	RG_MEMPLL2_FBDIV							RG_MEMPLL2_PREDIV	
Type	RW	RW		RW	RW		RW	RW							RW	
Reset	0	0	0	0	0	1	0	0	0	1	0	0	1	1	0	0

Bit(s)	Mnemonic	Name	Description
31:28	RG_MEMPLL_TST_SEL	RG_MEMPLL_TST_SEL	**Removed in design**
23:16	RG_MEMPLL_TEST[15:8]	RG_MEMPLL_TEST_15_8	
15	RG_MEMPLL2_VCO_DIF_EN	RG_MEMPLL2_VCO_DIF_EN	
14:13	RG_MEMPLL2_CKCTRL	RG_MEMPLL2_CKCTRL	

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Bit(s)	Mnemonic	Name	Description
	RL		
12	**RG_MEMPLL2_ACCEN**	RG_MEMPLL2_ACCEN	
11:10	**RG_MEMPLL2_FBKSEL**	RG_MEMPLL2_FBKSEL	**Selects feedback clock of MEMPLL 2** 1'b0: Fvco/1 1'b1: Fvco/2
9	**RG_MEMPLL2_DDSEN**	RG_MEMPLL2_DDSEN	
8:2	**RG_MEMPLL2_FBDIV**	RG_MEMPLL2_FBDIV	**Feedback divide ratio of MEMPLL 2** 7'd0: /1 7'd1: /2 ... 7'd127: /128
1:0	**RG_MEMPLL2_PREDIV**	RG_MEMPLL2_PREDIV	**Pre-divider ratio of MEMPLL 2** 2'b00: Fref = Fin/1 2'b01: Fref = Fin/2 2'b1X: Fref = Fin/4

1021360C **MEMPLL3** **MEMPLL Register Setting 3** **60000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RG_MEMPLL2_POSDIV**		**RG_MEMPLL2_VCO_DIV_SEL**	**RG_MEMPLL2_BLP**	**RG_MEMPLL2_BP**	**RG_MEMPLL2_BR**	**RG_MEMPLL2_BC**	**RG_MEMPLL2_DIVEN**			**RG_MEMPLL2_MONCK_EN**	**RG_MEMPLL2_MONVC_EN**	**RG_MEMPLL2_MONREF_EN**	**RG_MEMPLL2_EN**	**RG_MEMPLL2_RST_DLY**	
Type	RW		RW	RW	RW	RW	RW	RW			RW	RW	RW	RW	RW	
Reset	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RG_MEMPLL2_M4PDIV**		**RG_MEMPLL2_FB_MCK_SEL**	**RG_MEMPLL2_RESERVE**								
Type					RW		RW	RW								
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:30	**RG_MEMPLL2_POSDIV**	RG_MEMPLL2_POSDIV	**Post-divider ratio for single-end clock output of MEMPLL 2** 2'b00: VCO/1 2'b01: VCO/2 2'b1X: VCO/4
29	**RG_MEMPLL2_VCO_DIV_SEL**	RG_MEMPLL2_VCO_DIV_SEL	**Selects VCO div2 of MEMPLL 2** 1'b0: /1 1'b1: /2
28	**RG_MEMPLL2_BLP**	RG_MEMPLL2_BLP	**Selects LPF bandwidth of MEMPLL 2** 1'b0: 40MHz 1'b1: 20MHz
27	**RG_MEMPLL2_BP**	RG_MEMPLL2_BP	**Adjusts capacitance for bandwidth of MEMPLL 2** 1'b0: When RG_PLL_BR=1'b0 1'b1: When RG_PLL_BR=1'b1

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Bit(s)	Mnemonic	Name	Description
26	**RG_MEMPLL2_BR**	RG_MEMPLL2_BR	**Adjusts resistance for bandwidth of MEMPLL 2** 1'b0: BW = Fref/10 1'b1: BW = Fref/20
25	**RG_MEMPLL2_BC**	RG_MEMPLL2_BC	**Reduces OP current of MEMPLL 2** 1'b0: 10uA 1'b1: 5uA
24:22	**RG_MEMPLL2_DIVEN**	RG_MEMPLL2_DIVEN	**Time domain cap multiplication ratio of MEMPLL 2** 3'd0: x1 3'd1: x2 ... 3'd6: x64
21	**RG_MEMPLL2_MONCK_EN**	RG_MEMPLL2_MONCK_EN	**Enables monitor VCO clock for debugging of MEMPLL 2** 1'b0: Disable 1'b1: Enable
20	**RG_MEMPLL2_MONVC_EN**	RG_MEMPLL2_MONVC_EN	**Enables monitor Vctrl voltage for debugging of MEMPLL 2** 1'b0: Disable 1'b1: Enable
19	**RG_MEMPLL2_MONREF_EN**	RG_MEMPLL2_MONREF_EN	**Enables PFD clock out for frequency meter of MEMPLL 2** 1'b0: Disable 1'b1: Enable
18	**RG_MEMPLL2_EN**	RG_MEMPLL2_EN	**Enable MEMPLL 2** 1'b0: Disable 1'b1: Enable
17:16	**RG_MEMPLL2_RST_DLY**	RG_MEMPLL2_RST_DLY	
11:10	**RG_MEMPLL2_M4PDIV**	RG_MEMPLL2_M4PDIV	**Controls M4PDIV of MEMPLL 2** 2'b00: div1 2'b01: div2 2'b10: div4 2'b11: div8
9	**RG_MEMPLL2_FB_MCK_SEL**	RG_MEMPLL2_FB_MCK_SEL	**Mux for feedback clock of MEMPLL 2** 1'b0: Internal loop 2'b1: Outer loop
8:0	**RG_MEMPLL2_RESERVE**	RG_MEMPLL2_RESERVE	

10213610 **<u>MEMPLL4</u>** **MEMPLL Register Setting 4** **0000044C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RG_MEMPLL2_REF_DL**					**RG_MEMPLL2_FB_DL**					**RG_MEMPLL2_DL_RESERVE**					
Type	RW					RW					RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_MEMPLL3_VCO_DIF_EN**	**RG_MEMPLL3_CKCTRL**		**RG_MEMPLL3_ACCEN**	**RG_MEMPLL3_FBKSEL**		**RG_MEMPLL3_DDSEN**	**RG_MEMPLL3_FBDIV**							**RG_MEMPLL3_PREDIV**	
Type	RW	RW		RW	RW		RW	RW							RW	
Reset	0	0	0	0	0	1	0	0	0	1	0	0	1	1	0	0

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Bit(s)	Mnemonic	Name	Description
31:27	**RG_MEMPLL2_REF_DL**	RG_MEMPLL2_REF_DL	**Adjusts MEMPHYPLL skew between reference clock and feedback clock of MEMPLL 2**
26:22	**RG_MEMPLL2_FB_DL**	RG_MEMPLL2_FB_DL	**Adjusts MEMCTLPLL skew between reference clock and feedback clock of MEMPLL 2**
21:16	**RG_MEMPLL2_DL_RESERVE**	RG_MEMPLL2_DL_RESERVE	
15	**RG_MEMPLL3_VCO_DIF_EN**	RG_MEMPLL3_VCO_DIF_EN	
14:13	**RG_MEMPLL3_CKCTRL**	RG_MEMPLL3_CKCTRL	
12	**RG_MEMPLL3_ACCEN**	RG_MEMPLL3_ACCEN	
11:10	**RG_MEMPLL3_FBKSEL**	RG_MEMPLL3_FBKSEL	**Selects feedback clock of MEMPLL 3** 1'b0: Fvco/1 1'b1: Fvco/2
9	**RG_MEMPLL3_DDSEN**	RG_MEMPLL3_DDSEN	
8:2	**RG_MEMPLL3_FBDIV**	RG_MEMPLL3_FBDIV	**Feedback divide ratio of MEMPLL 3** 7'd0: /1 7'd1: /2 ... 7'd127: /128
1:0	**RG_MEMPLL3_PREDIV**	RG_MEMPLL3_PREDIV	**Pre-divider ratio of MEMPLL 3** 2'b00: Fref = Fin/1 2'b01: Fref = Fin/2 2'b1X: Fref = Fin/4

10213614 **MEMPLL5** **MEMPLL Register Setting 5** **60000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_MEMPLL3_POSDIV		RG_MEMPLL3_VCO_DIV_SEL	RG_MEMPLL3_BLP	RG_MEMPLL3_BP	RG_MEMPLL3_BR	RG_MEMPLL3_BC	RG_MEMPLL3_DIVEN			RG_MEMPLL3_MONCK_EN	RG_MEMPLL3_MONVC_EN	RG_MEMPLL3_MONREF_EN	RG_MEMPLL3_EN	RG_MEMPLL3_RST_DLY	
Type	RW		RW	RW	RW	RW	RW	RW			RW	RW	RW	RW	RW	
Reset	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_MEMPLL3_M4PDIV		RG_MEMPLL3_FB_MCK_SEL	RG_MEMPLL3_RESERVE								
Type					RW		RW	RW								
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
31:30	RG_MEMPLL3_POSDIV	RG_MEMPLL3_POSDIV	**Post-divider ratio for single-end clock output of MEMPLL 3** 2'b00: VCO/1 2'b01: VCO/2 2'b1X: VCO/4
29	RG_MEMPLL3_VCO_DIV_SEL	RG_MEMPLL3_VCO_DIV_SEL	**Selects VCO div2 of MEMPLL 3** 1'b0: /1 1'b1: /2
28	RG_MEMPLL3_BLP	RG_MEMPLL3_BLP	**Selects LPF bandwidth of MEMPLL 3** 1'b0: 40MHz 1'b1: 20MHz
27	RG_MEMPLL3_BP	RG_MEMPLL3_BP	**Adjusts capacitance for bandwidth of MEMPLL 3** 1'b0: When RG_PLL_BR=1'b0 1'b1: When RG_PLL_BR=1'b1
26	RG_MEMPLL3_BR	RG_MEMPLL3_BR	**Adjusts resistance for bandwidth of MEMPLL 3** 1'b0: BW = Fref/10 1'b1: BW = Fref/20
25	RG_MEMPLL3_BC	RG_MEMPLL3_BC	**Reduces OP current of MEMPLL 3** 1'b0: 10uA 1'b1: 5uA
24:22	RG_MEMPLL3_DIVEN	RG_MEMPLL3_DIVEN	**Time domain cap multiplication ratio of MEMPLL 3** 3'd0: x1 3'd1: x2 ... 3'd6: x64
21	RG_MEMPLL3_MONCK_EN	RG_MEMPLL3_MONCK_EN	**Enables monitor VCO clock for debugging of MEMPLL 3** 1'b0: Disable 1'b1: Enable
20	RG_MEMPLL3_MONVC_EN	RG_MEMPLL3_MONVC_EN	**Enables monitor Vctrl Voltage for debugging of MEMPLL 3** 1'b0: Disable 1'b1: Enable
19	RG_MEMPLL3_MONREF_EN	RG_MEMPLL3_MONREF_EN	**Enables PFD clock out for frequency meter of MEMPLL 3** 1'b0: Disable 1'b1: Enable
18	RG_MEMPLL3_EN	RG_MEMPLL3_EN	**Enables MEMPLL 3** 1'b0: Disable 1'b1: Enable
17:16	RG_MEMPLL3_RST_DLY	RG_MEMPLL3_RST_DLY	
11:10	RG_MEMPLL3_M4PDIV	RG_MEMPLL3_M4PDIV	**Controls M4PDIV of MEMPLL 3** 2'b00: div1 2'b01: div2 2'b10: div4 2'b11: div8
9	RG_MEMPLL3_FB_MCK_SEL	RG_MEMPLL3_FB_MCK_SEL	**Mux for feedback clock of MEMPLL 3** 1'b0: Internal loop 2'b1: Outer loop
8:0	RG_MEMPLL3_RESERVE	RG_MEMPLL3_RESERVE	

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10213618 MEMPLL6 MEMPLL Register Setting 6 0000044C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_MEMPLL3_REF_DL					RG_MEMPLL3_FB_DL					RG_MEMPLL3_DL_RESERVE					
Type	RW					RW					RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_MEMPLL4_VCO_DIF_EN	RG_MEMPLL4_CKCTRL		RG_MEMPLL4_ACCEN	RG_MEMPLL4_FBKSEL		RG_MEMPLL4_DDSEN	RG_MEMPLL4_FBDIV							RG_MEMPLL4_PREDIV	
Type	RW	RW		RW	RW		RW	RW							RW	
Reset	0	0	0	0	0	1	0	0	0	1	0	0	1	1	0	0

Bit(s)	Mnemonic	Name	Description
31:27	**RG_MEMPLL3_REF_DL**	RG_MEMPLL3_REF_DL	**Adjusts MEMPHYPLL skew between reference clock and feedback clock of MEMPLL 3**
26:22	**RG_MEMPLL3_FB_DL**	RG_MEMPLL3_FB_DL	**Adjusts MEMCTLPLL skew between reference clock and feedback clock of MEMPLL 3**
21:16	**RG_MEMPLL3_DL_RESERVE**	RG_MEMPLL3_DL_RESERVE	
15	**RG_MEMPLL4_VCO_DIF_EN**	RG_MEMPLL4_VCO_DIF_EN	
14:13	**RG_MEMPLL4_CKCTRL**	RG_MEMPLL4_CKCTRL	
12	**RG_MEMPLL4_ACCEN**	RG_MEMPLL4_ACCEN	
11:10	**RG_MEMPLL4_FBKSEL**	RG_MEMPLL4_FBKSEL	**Selects feedback clock of MEMPLL 4** 1'b0: Fvco/1 1'b1: Fvco/2
9	**RG_MEMPLL4_DDSEN**	RG_MEMPLL4_DDSEN	
8:2	**RG_MEMPLL4_FBDIV**	RG_MEMPLL4_FBDIV	**Feedback divide ratio of MEMPLL 4** 7'd0: /1 7'd1: /2 ... 7'd127: /128
1:0	**RG_MEMPLL4_PREDIV**	RG_MEMPLL4_PREDIV	**Pre-divider ratio of MEMPLL 4** 2'b00: Fref = Fin/1 2'b01: Fref = Fin/2 2'b1X: Fref = Fin/4

1021361C MEMPLL7 MEMPLL Register Setting 7 60000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_MEMPLL4_POSDIV		RG_MEMPLL4	RG_MEMPLL4	RG_MEMPLL4	RG_MEMPLL4	RG_MEMPLL4	RG_MEMPLL4_DIVEN			RG_MEMPLL4	RG_MEMPLL4	RG_MEMPLL4	RG_MEMPLL4	RG_MEMPLL4_RST_DLY	

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			_VCO_DIV_SEL	_BLP	_BP	_BR	_BC				_MONCK_EN	_MONVC_EN	_MONREF_EN	_EN		
Type	RW		RW	RW	RW	RW	RW	RW			RW	RW	RW	RW	RW	
Reset	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_MEMPLL4_M4PDIV		RG_MEMPLL4_FB_MCK_SEL	RG_MEMPLL4_RESERVE								
Type					RW		RW	RW								
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:30	RG_MEMPLL4_POSDIV	RG_MEMPLL4_POSDIV	**Post-divider ratio for single-end clock output of MEMPLL 4** 2'b00: VCO/1 2'b01: VCO/2 2'b1X: VCO/4
29	RG_MEMPLL4_VCO_DIV_SEL	RG_MEMPLL4_VCO_DIV_SEL	**Selects VCO div2 of MEMPLL 4** 1'b0: /1 1'b1: /2
28	RG_MEMPLL4_BLP	RG_MEMPLL4_BLP	**Selects LPF bandwidth of MEMPLL 4** 1'b0: 40MHz 1'b1: 20MHz
27	RG_MEMPLL4_BP	RG_MEMPLL4_BP	**Adjusts capacitance for bandwidth of MEMPLL 4** 1'b0: When RG_PLL_BR=1'b0 1'b1: When RG_PLL_BR=1'b1
26	RG_MEMPLL4_BR	RG_MEMPLL4_BR	**Adjusts resistance for bandwidth of MEMPLL 4** 1'b0: BW = Fref/10 1'b1: BW = Fref/20
25	RG_MEMPLL4_BC	RG_MEMPLL4_BC	**Reduces OP current of MEMPLL 4** 1'b0: 10uA 1'b1: 5uA
24:22	RG_MEMPLL4_DIVEN	RG_MEMPLL4_DIVEN	**Time domain cap multiplication ratio of MEMPLL 4** 3'd0: x1 3'd1: x2 ... 3'd6: x64
21	RG_MEMPLL4_MONCK_EN	RG_MEMPLL4_MONCK_EN	**Enables monitor VCO clock for debugging of MEMPLL 4** 1'b0: Disable 1'b1: Enable
20	RG_MEMPLL4_MONVC_EN	RG_MEMPLL4_MONVC_EN	**Enables monitor Vctrl voltage for debugging of MEMPLL 4** 1'b0: Disable 1'b1: Enable
19	RG_MEMPLL4_MONREF_EN	RG_MEMPLL4_MONREF_EN	**Enables PFD clock out for frequency meter of MEMPLL 4** 1'b0: Disable 1'b1: Enable
18	RG_MEMPLL4_EN	RG_MEMPLL4_EN	**Enables MEMPLL 4** 1'b0: Disable 1'b1: Enable
17:16	RG_MEMPLL4_RST_DLY	RG_MEMPLL4_RST_DLY	
11:10	RG_MEMPLL4_M4PD	RG_MEMPLL4_M4PDIV	**Controls M4PDIV of MEMPLL 4** 2'b00: div1

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Bit(s)	Mnemonic	Name	Description
	IV		2'b01: div2 2'b10: div4 2'b11: div8
9	**RG_MEMPLL4_FB_MCK_SEL**	RG_MEMPLL4_FB_MCK_SEL	**Mux for feedback clock of MEMPLL 4** 1'b0: Internal loop 2'b1: Outer loop
8:0	**RG_MEMPLL4_RESERVE**	RG_MEMPLL4_RESERVE	

10213620 MEMPLL8 MEMPLL Register Setting 8 00008C00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RG_MEMPLL4_REF_DL**					**RG_MEMPLL4_FB_DL**					**RG_MEMPLL4_DL_RESERVE**					
Type	RW					RW					RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_MEMPLL_SDM_DI_EN**	**RG_MEMPLL_SDM_HREN**		**RG_DMSS_CLK_PH_INV**	**RG_MEMPLL_SDM_ORD**		**RG_MEMPLL_SDM_DI_LS**		**RG_MEMPLL_LVROD_EN**	**RG_DMSS_LPF_EN**	**RG_DMSS_MON_EN**	**RG_DMSS_NCPO_EN**	**RG_DMSS_NCPO_ISO_EN**			
Type	RW	RW		RW	RW		RW		RW	RW	RW	RW	RW			
Reset	1	0		0	1	1	0	0	0	0	0	0	0			

Bit(s)	Mnemonic	Name	Description
31:27	**RG_MEMPLL4_REF_DL**	RG_MEMPLL4_REF_DL	Adjusts MEMPHYPLL skew between reference clock and feedback clock of MEMPLL 4
26:22	**RG_MEMPLL4_FB_DL**	RG_MEMPLL4_FB_DL	Adjusts MEMCTLPLL skew between reference clock and feedback clock of MEMPLL 4
21:16	**RG_MEMPLL4_DL_RESERVE**	RG_MEMPLL4_DL_RESERVE	
15	**RG_MEMPLL_SDM_DI_EN**	RG_MEMPLL_SDM_DI_EN	
14	**RG_MEMPLL_SDM_HREN**	RG_MEMPLL_SDM_HREN	
12	**RG_DMSS_CLK_PH_INV**	RG_DMSS_CLK_PH_INV	Removed in design
11:10	**RG_MEMPLL_SDM_ORD**	RG_MEMPLL_SDM_ORD	
9:8	**RG_MEMPLL_SDM_DI_LS**	RG_MEMPLL_SDM_DI_LS	
7	**RG_MEMPLL_LVROD_EN**	RG_MEMPLL_LVROD_EN	
6	**RG_DMSS**	RG_DMSS_LPF_E	Removed in design

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Bit(s)	Mnemonic	Name	Description
	_LPF_EN	N	
5	**RG_DMSS_MONEN**	RG_DMSS_MONEN	Removed in design
4	**RG_DMSS_NCPO_EN**	RG_DMSS_NCPO_EN	Removed in design
3	**RG_DMSS_NCPO_ISO_EN**	RG_DMSS_NCPO_ISO_EN	Enables DDS NCPO ISO

10213624 MEMPLL9 MEMPLL Register Setting 9 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_MEMPLL_N_INFO[30:0][30:15]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_MEMPLL_N_INFO[30:0][14:0]															RG_MEMPLL_N_INFO_CHG
Type	RW															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:1	**RG_MEMPLL_N_INFO[30:0]**	RG_MEMPLL_N_INFO_30_0	RG_MEMPLL_N_INFO[30:0]
0	**RG_MEMPLL_N_INFO_CHG**	RG_MEMPLL_N_INFO_CHG	RG_MEMPLL_N_INFO_CHG

10213628 MEMPLL10 MEMPLL Register Setting 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_DMSS_PI_PL_EN	RG_DMSS_POSTDIV2	RG_DMSS_PREDIV2	RG_DMSS_PWDB	RG_DMSS_RSTB	RG_DMSS_RST_SEL	RG_DMSS_SEL_EXT	RG_DMSS_VADJ								
Type	RW	RW	RW	RW	RW	RW	RW	RW								
Reset	0	0	0	0	0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_MEMPLL_SDM_SSC_DELTA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**RG_DMSS_PI_PL_EN**	RG_DMSS_PI_PL_EN	Removed in design
30	**RG_DMSS_POSTDIV**	RG_DMSS_POSTDIV2	Removed in design

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Bit(s)	Mnemonic	Name	Description
	2		
29	RG_DMSS_PREDIV2	RG_DMSS_PREDIV2	Removed in design
28	RG_DMSS_PWDB	RG_DMSS_PWDB	Removed in design
27	RG_DMSS_RSTB	RG_DMSS_RSTB	Removed in design
26	RG_DMSS_RST_SEL	RG_DMSS_RST_SEL	Removed in design
25	RG_DMSS_SEL_EXT	RG_DMSS_SEL_EXT	Removed in design
24	RG_DMSS_VADJ	RG_DMSS_VADJ	Removed in design
15:0	RG_MEMPLL_SDM_SSC_DELTA	RG_MEMPLL_SDM_SSC_DELTA	Controls SDM SSC dither amplitude

1021362C **MEMPLL11** **MEMPLL Register Setting 11** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_MEMPLL_SDM_SSC_PRD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_MEMPLL_SDM_SSC_DELTA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16	RG_MEMPLL_SDM_SSC_PRD	RG_MEMPLL_SDM_SSC_PRD	Controls SDM SSC dither period
15:0	RG_MEMPLL_SDM_SSC_DELTA1	RG_MEMPLL_SDM_SSC_DELTA1	Controls SDM SSC dither amplitude for initialization

10213630 **MEMPLL12** **MEMPLL Register Setting 12** **20000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_DMSS_SSC_EN	RG_DMSS_SSC_PHASE_INI	RG_DMSS_SSC_TRI_EN	Reserved								REXTDN_PD_CONTROL	RG_MEMPLL_CLK0_DUTY[4:1]			
Type	RW	RW	RW	RW								RW	RW			
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_MEMPLL_CLK0_DUTY[0:0]	RG_MEMPLL_CLK90_DUTY					RG_MEMPLL_CLK180_DUTY					RG_MEMPLL_CLK270_DUTY				

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Type	RW	RW					RW					RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**RG_DMSS_SSC_EN**	RG_DMSS_SSC_EN	**Enables DDS SSC**
30	**RG_DMSS_SSC_PHASE_INI**	RG_DMSS_SSC_PHASE_INI	**DDS SSC initial phase direction** 0: Downward 1: Upward
29	**RG_DMSS_SSC_TRI_EN**	RG_DMSS_SSC_TRI_EN	**Enables DDS SSC**
20	**REXTDN_PD_CONTROL**	REXTDN_PD_CONTROL	**Set No_USE to 1'b1 to save power.**
19:15	**RG_MEMPLL_CLK0_DUTY**	RG_MEMPLL_CLK0_DUTY	**MEMPLL2_CK0_DUTY_CTRL** **Bit 19:** 0: Select H width duty adjustment 1: Select Low width duty adjustment **Bit 18~17: Low width delay** 2'b00: No delay 2'b01: 20ps 2'b10: 40ps 2'b11: 60ps **Bit 16~15: High width delay** 2'b00: No delay 2'b01: 20ps 2'b10: 40ps 2'b11: 60ps
14:10	**RG_MEMPLL_CLK90_DUTY**	RG_MEMPLL_CLK90_DUTY	**MEMPLL2_CK90_DUTY_CTRL** **Bit 14:** 0: Select H width duty adjustment 1: Select Low width duty adjustment **Bit 13~12: Low width delay** 2'b00: No delay 2'b01: 20ps 2'b10: 40ps 2'b11: 60ps **Bit 11~10: High width delay** 2'b00: No delay 2'b01: 20ps 2'b10: 40ps 2'b11: 60ps
9:5	**RG_MEMPLL_CLK180_DUTY**	RG_MEMPLL_CLK180_DUTY	**MEMPLL2_CK180_DUTY_CTRL** **Bit 9:** 0: Select H width duty adjustment 1: Select Low width duty adjustment **Bit 8~7: Low width delay** 2'b00: No delay 2'b01: 20ps 2'b10: 40ps 2'b11: 60ps **Bit 6~5: High width delay** 2'b00: No delay 2'b01: 20ps 2'b10: 40ps 2'b11: 60ps
4:0	**RG_MEMP**	RG_MEMPLL_CLK	**MEMPLL2_CK270_DUTY_CTRL**

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Bit(s)	Mnemonic	Name	Description
	LL_CLK270_DUTY	270_DUTY	**Bit 4:** 0: Select H width duty adjustment 1: Select Low width duty adjustment **Bit 3~2: Low width delay** 2'b00: No delay 2'b01: 20ps 2'b10: 40ps 2'b11: 60ps **Bit 1~0: High width delay** 2'b00: No delay 2'b01: 20ps 2'b10: 40ps 2'b11: 60ps

10213640 **MEMPLL_DIVIDER** **MEMPLL Divider Register Control** **00000003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R_D_MIO_CK_CG_EN	R_D_MIO_CK_DIV2_270_CG_EN	R_D_MIO_CK_DIV2_180_CG_EN	R_D_MIO_CK_DIV2_90_CG_EN	R_D_MIO_CK_DIV2_00_CG_EN	R_D_PHY_M_CK_CG_EN	R_C_MIO_CK_DIV2_270_CG_EN	R_C_MIO_CK_DIV2_180_CG_EN	R_C_MIO_CK_DIV2_90_CG_EN	R_C_PHY_M_CK_CG_EN	R_C_MIO_CK_CG_EN	R_Async_D_PHY_CK_CG_EN	R_CMD_M_CK_CG_EN	R_MEMPLL2_CKOUT_CG_EN	R_MEMPLL3_CKOUT_CG_EN	R_MEMPLL2_FB_M_CK_CG_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R_COMB_M_CK_CG_EN	R_DDRPHY_CLK_EN_COMSEL							R_ADMEMPLL2_CKOUT0_PRE_EN	R_CMD_RCLK_CTL_M_CK_SEL	R_DMPLL2CLK_EN	R_DMALLCLK_EN	R_CMD_RCLK_CTL_M_CK_SEL	R_DM1PLL_SYNC_MODE	R_DMBYP_PLL3	R_DMBYP_PLL4
Type	RW	RW							RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0							0	0	0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
31	R_D_MIO_CK_CG_EN	R_D_MIO_CK_CG_EN	**Controls DDRPHY D_MIO_CK clock gating** 0: Disable 1: Enable
30	R_D_MIO_CK_DIV2_270_CG_EN	R_D_MIO_CK_DIV2_270_CG_EN	**Controls DDRPHY MIO_CK_DIV2_270 clock gating** 0: Disable 1: Enable
29	R_D_MIO_CK_DIV2_180_CG_EN	R_D_MIO_CK_DIV2_180_CG_EN	**Controls DDRPHY MIO_CK_DIV2_180 clock gating** 0: Disable 1: Enable
28	R_D_MIO_CK_DIV2_90_CG_EN	R_D_MIO_CK_DIV2_90_CG_EN	**Controls DDRPHY MIO_CK_DIV2_90 clock gating** 0: Disable 1: Enable
27	R_D_MIO_CK_DIV2_00_CG_EN	R_D_MIO_CK_DIV2_00_CG_EN	**Controls DDRPHY MIO_CK_DIV2_00 clock gating** 0: Disable 1: Enable

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Bit(s)	Mnemonic	Name	Description
26	**R_D_PHY_M_CK_CG_EN**	R_D_PHY_M_CK_CG_EN	**Controls DDRPHY D_PHY_M_CK clock gating** 0: Disable 1: Enable
25	**R_C_MIO_CK_DIV2_270_CG_EN**	R_C_MIO_CK_DIV2_270_CG_EN	**Controls DDRPHY C_MIO_CK_DIV2_270 clock gating** 0: Disable 1: Enable
24	**R_C_MIO_CK_DIV2_180_CG_EN**	R_C_MIO_CK_DIV2_180_CG_EN	**Controls DDRPHY C_MIO_CK_DIV2_180 clock gating** 0: Disable 1: Enable
23	**R_C_MIO_CK_DIV2_90_CG_EN**	R_C_MIO_CK_DIV2_90_CG_EN	**Controls DDRPHY C_MIO_CK_DIV2_90 clock gating** 0: Disable 1: Enable
22	**R_C_PHY_M_CK_CG_EN**	R_C_PHY_M_CK_CG_EN	**Controls DDRPHY C_PHY_M_CK clock gating** 0: Disable 1: Enable
21	**R_C_MIO_CK_CG_EN**	R_C_MIO_CK_CG_EN	**Controls DDRPHY C_MIO_CK clock gating** 0: Disable 1: Enable
20	**R_Async_D_PHY_CK_CG_EN**	R_Async_D_PHY_CK_CG_EN	**Controls DDRPHY async D_PHY_M_CK clock gating** 0: Disable 1: Enable
19	**R_CMD_M_CK_CG_EN**	R_CMD_M_CK_CG_EN	**Controls DDRPHY CMD M-CK clock gating** 0: Disable 1: Enable
18	**R_MEMPLL2_CKOUT_CG_EN**	R_MEMPLL2_CKOUT_CG_EN	**Controls MEMPLL2 clock root clock gating** 0: Disable 1: Enable
17	**R_MEMPLL3_CKOUT_CG_EN**	R_MEMPLL3_CKOUT_CG_EN	**Controls MEMPLL3 clock root clock gating** 0: Disable 1: Enable
16	**R_MEMPLL2_FB_M_CK_CG_EN**	R_MEMPLL2_FB_M_CK_CG_EN	**Controls MEMPLL2 FB clock gating** 0: Enable 1: Disable
15	**R_COMB_M_CK_CG_EN**	R_COMB_M_CK_CG_EN	**Controls DDRPHY COMB clock gating** 0: Disable 1: Enable
14	**R_DDRPHY_CLK_EN_COM_SEL**	R_DDRPHY_CLK_EN_COM_SEL	**Selects DDRPHY COMB clock gating control source** 0: New source 1: Old control source
7	**R_AD_MEMPLL2_CKOUT0_PRE_EN**	R_AD_MEMPLL2_CKOUT0_PRE_EN	**0: disable AD_MEMPLL2_CKOUT0_PRE** 1: enable AD_MEMPLL2_CKOUT0_PRE
6	**R_CMD_RCLK_CTL_M_CK_SEL**	R_CMD_RCLK_CTL_M_CK_SEL	**Selects DDRPHY CMD DRAM RCLK block M_CK source** 0: Select gating M_CK as clock source 1: Select non-gating M_CK as clock source
5	**R_DMPLL2CLK_EN**	R_DMPLL2CLK_EN	**Enables 4-phase output clocks of MEMPLL2** 0: Disable 1: Enable

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Bit(s)	Mnemonic	Name	Description
4	**R_DMALLCLK_EN**	R_DMALLCLK_EN	**Enables all output clocks of MEMPLL divider, except for feedback clocks to MEMPLL** 0: Disable 1: Enable
3	**R_CMD_RCLK_CTL_M_CK_SEL**	R_DDR_CMD_CK_CG_EN	**Controls DDRPHY DDR3 CMD block clock gating** 0: Disable 1: Enable
2	**R_DM1PLL_SYNC_MODE**	R_DM1PLL_SYNC_MODE	**Enables synchronous mode under 1-PLL clock scheme** 0: Asynchronous mode 1: Synchronous mode
1	**R_DMBYP_PLL3**	R_DMBYP_PLL3	**Bypasses PLL core 3** 0: Does not bypass 1: Bypass
0	**R_DMBYP_PLL4**	R_DMBYP_PLL4	**Bypasses PLL core 4** 0: Does not bypass 1: Bypass

10213644 VREFCTL VREF Register Setting 0 0000007D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**CMPCALENN**	**CMPCALENP**	**INTREFTUNE**					**INTREF_DS**		**EN_INTREF**
Type							RW	RW	RW					RW		RW
Reset							0	0	0	1	1	1	1	1	0	1

Bit(s)	Mnemonic	Name	Description
9	**CMPCALENN**	CMPCALENN	**Enables P-impedance calibration**
8	**CMPCALENP**	CMPCALENP	**Enables N-impedance calibration**
7:3	**INTREFTUNE**	INTREFTUNE	**Fine-tunes VREF, REFTUNE4:MSB and REFTUNE0:LSB**
2:1	**INTREF_DS**	INTREF_DS	**Controls VREF current consumption** 00: Weakest 11: Strongest current consumption
0	**EN_INTREF**	EN_INTREF	**Enables internal VREF control** 0: Disable 1: Enable

3.7.5 Programming Guide

Steps of DRAM initialization

1. Set up DRAM AC timing parameter.
2. Follow DRAM spec to complete DRAM initialization including mode register programming.
3. Enable calibration for DQ/DQS window.

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4. Set up refresh rate counter.
5. Normal operation.

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3.8 AP_DMA

3.8.1 Introduction

There is always a DMA in a platform. The purpose of DMA is performing data transfer between different slaves. There are several slaves in a platform, and the major one is external memory, e.g. DRAM. There are also internal SRAM and some slave ports for the peripheral to transfer data. For saving software efforts, DMA delivers a virtual FIFO concept to help the software maintain read and write pointer when the software accesses data from a ring buffer. As the bus goes more and more efficient, the old DMA still utilizes the AHB bus protocol and may decrease its performance. Another problem is that when the old DMA meets byte alignment addresses or byte alignment sizes, it will need some software efforts to help solve head and tail non word alignment problems or let DMA to simply issues single-1-byte requests to conquer the byte-alignment problem. This will harm the overall system because the single-1-byte transaction is quite inefficient. The DMA efficiency is now improved by increasing its bus efficiency, including data buffering and overcoming byte alignment problems.

3.8.2 Features

APDMA has the following DMA engines.

- HIF DMA engine*1
- IRDA DMA engine*1
- I2C DMA engine*4
- UART0 TX DMA engine*1
- UART0 RX DMA engine*1
- UART1 TX DMA engine*1
- UART1 RX DMA engine*1
- UART2 TX DMA engine*1
- UART2 RX DMA engine*1
- UART3 TX DMA engine*1
- UART3 RX DMA engine*1
- UART4 TX DMA engine*1
- UART4 RX DMA engine*1
- UART4 TX DMA engine*1
- UART4 RX DMA engine*1

The DMA engines and corresponding peripheral devices are listed below.

Table 3-7. Relationship between engines and devices

Engine	Peripheral device
HIF_0	Connsys (sdctl)
IRDA_0	IRDA
I2C_0 ~ I2C_3	I2C_0 ~ I2C_3

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Engine	Peripheral device
UART0 ~ UART3	UART0 ~ UART3
UART4	BTIF
UART4	C2K

3.8.3 Block Diagram

Figure 3-10 is the basic block diagram of AP_DMA. There are total 15 channels in DMA. The external AXI interface is connected to the peripheral AXI bus fabric to provide external memory access ability. The internal AXI interface is also connected to the peripheral AXI bus fabric and is re-directed to related peripherals, e.g. HIF, I2C and UART. A memory block is used as a buffer which makes the transfer on the AXI bus interface more efficient. An APB interface is used to program registers for both global registers and local registers existing in every individual DMA channel.

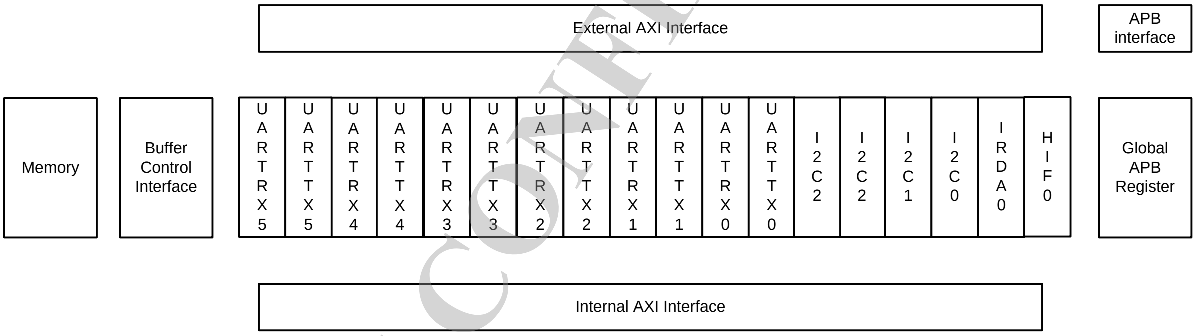

Figure 3-10. APDMA block diagram

3.8.4 Register Definition

3.8.4.1 Global Control Registers

There are several registers put together for the software to monitor. However, if the software is to change them, they can only be written through individual DMA registers. The global register is only for the software to watch all DMA running statuses and interrupt flags together. Note that the security ability of all global registers belongs to the GSEC_EN bit. When this bit is set to 1, only the security transaction can write the global register (global reset and global slow-down). If a non-security read transaction is issued to read the interrupt flag or running status, only statuses of non-security engines can be reported, and others will always be 0.

Module name: AP_DMA Base address: (+11000000h)

Address	Name	Width	Register Function
11000000	AP_DMA_GLOBAL_INT_FLAG	32	AP DMA Global Interrupt Flag Register
11000004	AP_DMA_GLOBAL_RST	32	AP DMA Reset Register
11000008	AP_DMA_GLOBAL	32	AP DMA Global Running Status Register

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Address	Name	Width	Register Function
	_RUNNING_STATUS		Indicates if each DMA engine is running or not.
1100000C	AP_DMA_GLOBAL_SLOW_DOWN	32	AP DMA AXI Slow Down Register
11000010	AP_DMA_GLOBAL_SEC_EN	32	AP DMA Security Enable Register
11000014	AP_DMA_GLOBAL_GSEC_EN	32	AP DMA Global Security Enable Register
11000018	AP_DMA_GLOBAL_VIO_DBG1	32	AP DMA Security Latch Address Register
1100001C	AP_DMA_GLOBAL_VIO_DBG0	32	AP DMA Global Security Abort Register
11000020	AP_DMA_HIF0_SEC_EN	32	AP HIF0 DMA Security Enable Register
11000024	AP_DMA_IrDA_SEC_EN	32	AP irda0 DMA Security Enable Register
11000028	AP_DMA_I2C0_SEC_EN	32	AP I2C0 DMA Security Enable Register
1100002C	AP_DMA_I2C1_SEC_EN	32	AP I2C1 DMA Security Enable Register
11000030	AP_DMA_I2C2_SEC_EN	32	AP I2C2 DMA Security Enable Register
11000034	AP_DMA_I2C3_SEC_EN	32	AP I2C3 DMA Security Enable Register
11000038	AP_DMA_UART0_TX_SEC_EN	32	AP UART0 TX DMA Security Enable Register
1100003C	AP_DMA_UART0_RX_SEC_EN	32	AP UART0 RX DMA Security Enable Register
11000040	AP_DMA_UART1_TX_SEC_EN	32	AP UART1 TX DMA Security Enable Register
11000044	AP_DMA_UART1_RX_SEC_EN	32	AP UART1 RX DMA Security Enable Register
11000048	AP_DMA_UART2_TX_SEC_EN	32	AP UART2 TX DMA Security Enable Register
1100004C	AP_DMA_UART2_RX_SEC_EN	32	AP UART2 RX DMA Security Enable Register
11000050	AP_DMA_UART3_TX_SEC_EN	32	AP UART3 TX DMA Security Enable Register
11000054	AP_DMA_UART3_RX_SEC_EN	32	AP UART3 RX DMA Security Enable Register
11000058	AP_DMA_UART4_TX_SEC_EN	32	AP UART4 TX DMA Security Enable Register
1100005C	AP_DMA_UART4_RX_SEC_EN	32	AP UART4 RX DMA Security Enable Register
11000060	AP_DMA_UART5_TX_SEC_EN	32	AP UART5 TX DMA Security Enable Register
11000064	AP_DMA_UART5_RX_SEC_EN	32	AP UART5 RX DMA Security Enable Register
11000070	AP_DMA_MD_INT_EN	32	AP DMA MD Interrupt Enable Register
11000080	AP_DMA_HIF_0_INT_FLAG	32	Peripheral DMA Interrupt Flag Register
11000084	AP_DMA_HIF_0_INT_EN	32	Peripheral DMA Interrupt Enable Register
11000088	AP_DMA_HIF_0_EN	32	Peripheral DMA Enable Register

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Address	Name	Width	Register Function
1100008C	AP_DMA_HIF_0_RST	32	Peripheral DMA Reset Register
11000090	AP_DMA_HIF_0_STOP	32	Peripheral DMA Enable Register
11000094	AP_DMA_HIF_0_FLUSH	32	Peripheral DMA Flush Register
11000098	AP_DMA_HIF_0_CON	32	Peripheral DMA Control Register
1100009C	AP_DMA_HIF_0_SRC_ADDR	32	Peripheral DMA SRC Address Register
110000A0	AP_DMA_HIF_0_DST_ADDR	32	Peripheral DMA DST Address Register
110000A4	AP_DMA_HIF_0_LEN	32	Peripheral DMA Transfer Length Register
110000B8	AP_DMA_HIF_0_INT_BUF_SIZE	32	Peripheral DMA Internal Buffer Size Register
110000D0	AP_DMA_HIF_0_DEBUG_STATUS_00	32	Peripheral DMA Debug Status 00 Register
11000100	AP_DMA_IrDA_0_INT_FLAG	32	Peripheral DMA Interrupt Flag Register
11000104	AP_DMA_IrDA_0_INT_EN	32	Peripheral DMA Interrupt Enable Register
11000108	AP_DMA_IrDA_0_EN	32	Peripheral DMA Enable Register
1100010C	AP_DMA_IrDA_0_RST	32	Peripheral DMA Reset Register
11000110	AP_DMA_IrDA_0_STOP	32	Peripheral DMA Enable Register
11000114	AP_DMA_IrDA_0_FLUSH	32	Peripheral DMA Flush Register
11000118	AP_DMA_IrDA_0_CON	32	Peripheral DMA Control Register
1100011C	AP_DMA_IrDA_0_MEM_ADDR	32	Peripheral DMA Memory Address Register
11000124	AP_DMA_IrDA_0_LEN	32	Peripheral DMA Transfer Length Register
11000138	AP_DMA_IrDA_0_INT_BUF_SIZE	32	Peripheral DMA Internal Buffer Size Register
11000150	AP_DMA_IrDA_0_DEBUG_STATUS_00	32	Peripheral DMA Debug Status 00 Register
11000180	AP_DMA_I2C_0_INT_FLAG	32	Peripheral DMA Interrupt Flag Register
11000184	AP_DMA_I2C_0_INT_EN	32	Peripheral DMA Interrupt Enable Register
11000188	AP_DMA_I2C_0_EN	32	Peripheral DMA Enable Register
1100018C	AP_DMA_I2C_0_RST	32	Peripheral DMA Reset Register
11000190	AP_DMA_I2C_0_STOP	32	Peripheral DMA Enable Register
11000194	AP_DMA_I2C_0_FLUSH	32	Peripheral DMA Flush Register
11000198	AP_DMA_I2C_0_CON	32	Peripheral DMA Control Register

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Address	Name	Width	Register Function
1100019C	AP_DMA_I2C_0_TX_MEM_ADDR	32	Peripheral DMA Memory Address Register
110001A0	AP_DMA_I2C_0_RX_MEM_ADDR	32	Peripheral DMA Memory Address Register
110001A4	AP_DMA_I2C_0_TX_LEN	32	Peripheral DMA Transfer Length Register
110001A8	AP_DMA_I2C_0_RX_LEN	32	Peripheral DMA Transfer Length Register
110001B8	AP_DMA_I2C_0_INT_BUF_SIZE	32	Peripheral DMA Internal Buffer Size Register
110001D0	AP_DMA_I2C_0_DEBUG_STATUS_00	32	Peripheral DMA Debug Status 00 Register
11000200	AP_DMA_I2C_1_INT_FLAG	32	Peripheral DMA Interrupt Flag Register
11000204	AP_DMA_I2C_1_INT_EN	32	Peripheral DMA Interrupt Enable Register
11000208	AP_DMA_I2C_1_EN	32	Peripheral DMA Enable Register
1100020C	AP_DMA_I2C_1_RST	32	Peripheral DMA Reset Register
11000210	AP_DMA_I2C_1_STOP	32	Peripheral DMA Enable Register
11000214	AP_DMA_I2C_1_FLUSH	32	Peripheral DMA Flush Register
11000218	AP_DMA_I2C_1_CON	32	Peripheral DMA Control Register
1100021C	AP_DMA_I2C_1_TX_MEM_ADDR	32	Peripheral DMA Memory Address Register
11000220	AP_DMA_I2C_1_RX_MEM_ADDR	32	Peripheral DMA Memory Address Register
11000224	AP_DMA_I2C_1_TX_LEN	32	Peripheral DMA Transfer Length Register
11000228	AP_DMA_I2C_1_RX_LEN	32	Peripheral DMA Transfer Length Register
11000238	AP_DMA_I2C_1_INT_BUF_SIZE	32	Peripheral DMA Internal Buffer Size Register
11000250	AP_DMA_I2C_1_DEBUG_STATUS_00	32	Peripheral DMA Debug Status 00 Register
11000280	AP_DMA_I2C_2_INT_FLAG	32	Peripheral DMA Interrupt Flag Register
11000284	AP_DMA_I2C_2_INT_EN	32	Peripheral DMA Interrupt Enable Register
11000288	AP_DMA_I2C_2_EN	32	Peripheral DMA Enable Register
1100028C	AP_DMA_I2C_2_RST	32	Peripheral DMA Reset Register
11000290	AP_DMA_I2C_2_STOP	32	Peripheral DMA Enable Register
11000294	AP_DMA_I2C_2_FLUSH	32	Peripheral DMA Flush Register
11000298	AP_DMA_I2C_2_CON	32	Peripheral DMA Control Register
1100029C	AP_DMA_I2C_2_TX_MEM_ADDR	32	Peripheral DMA Memory Address Register
110002A0	AP_DMA_I2C_2_R	32	Peripheral DMA Memory Address Register

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Address	Name	Width	Register Function
	X_MEM_ADDR		
110002A4	AP_DMA_I2C_2_TX_LEN	32	Peripheral DMA Transfer Length Register
110002A8	AP_DMA_I2C_2_RX_LEN	32	Peripheral DMA Transfer Length Register
110002B8	AP_DMA_I2C_2_INT_BUF_SIZE	32	Peripheral DMA Internal Buffer Size Register
110002D0	AP_DMA_I2C_2_DEBUG_STATUS_00	32	Peripheral DMA Debug Status 00 Register
11000300	AP_DMA_I2C_3_INT_FLAG	32	Peripheral DMA Interrupt Flag Register
11000304	AP_DMA_I2C_3_INT_EN	32	Peripheral DMA Interrupt Enable Register
11000308	AP_DMA_I2C_3_EN	32	Peripheral DMA Enable Register
1100030C	AP_DMA_I2C_3_RST	32	Peripheral DMA Reset Register
11000310	AP_DMA_I2C_3_STOP	32	Peripheral DMA Enable Register
11000314	AP_DMA_I2C_3_FLUSH	32	Peripheral DMA Flush Register
11000318	AP_DMA_I2C_3_CON	32	Peripheral DMA Control Register
1100031C	AP_DMA_I2C_3_TX_MEM_ADDR	32	Peripheral DMA Memory Address Register
11000320	AP_DMA_I2C_3_RX_MEM_ADDR	32	Peripheral DMA Memory Address Register
11000324	AP_DMA_I2C_3_TX_LEN	32	Peripheral DMA Transfer Length Register
11000328	AP_DMA_I2C_3_RX_LEN	32	Peripheral DMA Transfer Length Register
11000338	AP_DMA_I2C_3_INT_BUF_SIZE	32	Peripheral DMA Internal Buffer Size Register
11000350	AP_DMA_I2C_3_DEBUG_STATUS_00	32	Peripheral DMA Debug Status 00 Register
11000380	AP_DMA_UART_0_TX_INT_FLAG	32	UART0 TX Virtual FIFO Interrupt Flag Register
11000384	AP_DMA_UART_0_TX_INT_EN	32	UART0 TX Virtual FIFO Interrupt Enable Register
11000388	AP_DMA_UART_0_TX_EN	32	UART0 TX Virtual FIFO Enable Register
1100038C	AP_DMA_UART_0_TX_RST	32	UART0 TX Virtual FIFO Reset Register
11000390	AP_DMA_UART_0_TX_STOP	32	UART0 TX Virtual FIFO Enable Register
11000394	AP_DMA_UART_0_TX_FLUSH	32	UART0 TX Virtual FIFO Flush Register
1100039C	AP_DMA_UART_0_TX_VFF_ADDR	32	UART0 TX Virtual FIFO Base Address Register
110003A4	AP_DMA_UART_0_TX_VFF_LEN	32	UART0 TX Virtual FIFO Length Register
110003A8	AP_DMA_UART_0_TX_VFF_THRE	32	UART0 TX Virtual FIFO Threshold Register
110003AC	AP_DMA_UART_0_TX_VFF_WPT	32	UART0 TX Virtual FIFO Write Pointer Register

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Address	Name	Width	Register Function
110003B0	AP_DMA_UART_0_TX_VFF_RPT	32	UART0 TX Virtual FIFO Read Pointer Register
110003B8	AP_DMA_UART_0_TX_INT_BUF_SIZE	32	UART0 TX Internal Buffer Size Register
110003BC	AP_DMA_UART_0_TX_VFF_VALID_SIZE	32	UART0 TX Virtual FIFO Valid Size Register
110003C0	AP_DMA_UART_0_TX_VFF_LEFT_SIZE	32	UART0 TX Virtual FIFO Left Size Register
110003D0	AP_DMA_UART_0_TX_DEBUG_STATUS_00	32	UART0 TX Debug Status 00
110003D4	AP_DMA_UART_0_TX_VFF_WPT_REAL	32	UART0 TX Virtual FIFO Write Pointer Register Value
110003D8	AP_DMA_UART_0_TX_VFF_WPT_VALID	32	UART0 TX Virtual FIFO Write Pointer Register by HW Control
110003E0	AP_DMA_UART_0_TX_FLUSH_ACT	32	UART0 TX Virtual FIFO Flush Status Register
110003E4	AP_DMA_UART_0_TX_HW_FLUSH	32	UART0 TX Virtual FIFO HW Flush Register
11000400	AP_DMA_UART_0_RX_INT_FLAG	32	UART0 RX Virtual FIFO Interrupt Flag Register
11000404	AP_DMA_UART_0_RX_INT_EN	32	UART0 RX Virtual FIFO Interrupt Enable Register
11000408	AP_DMA_UART_0_RX_EN	32	UART0 RX Virtual FIFO Enable Register
1100040C	AP_DMA_UART_0_RX_RST	32	UART0 RX Virtual FIFO Reset Register
11000410	AP_DMA_UART_0_RX_STOP	32	UART0 RX Virtual FIFO Enable Register
11000414	AP_DMA_UART_0_RX_FLUSH	32	UART0 RX Virtual FIFO Flush Register
1100041C	AP_DMA_UART_0_RX_VFF_ADDR	32	UART0 RX Virtual FIFO Base Address Register
11000424	AP_DMA_UART_0_RX_VFF_LEN	32	UART0 RX Virtual FIFO Length Register
11000428	AP_DMA_UART_0_RX_VFF_THRE	32	UART0 RX Virtual FIFO Threshold Register
1100042C	AP_DMA_UART_0_RX_VFF_WPT	32	UART0 RX Virtual FIFO Write Pointer Register
11000430	AP_DMA_UART_0_RX_VFF_RPT	32	UART0 RX Virtual FIFO Read Pointer Register
11000434	AP_DMA_UART_0_RX_FLOW_CTRL_THRE	32	UART0 RX Virtual FIFO Flow Control Threshold
11000438	AP_DMA_UART_0_RX_INT_BUF_SIZE	32	UART0 RX Internal Buffer Size Register
1100043C	AP_DMA_UART_0_RX_VFF_VALID_SIZE	32	UART0 RX Virtual FIFO Valid Size Register
11000440	AP_DMA_UART_0_RX_VFF_LEFT_SIZE	32	UART0 RX Virtual FIFO Left Size Register

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Address	Name	Width	Register Function
11000450	AP_DMA_UART_0_RX_DEBUG_STATUS_00	32	UART0 RX Debug Status 00
11000480	AP_DMA_UART_1_TX_INT_FLAG	32	UART1 TX Virtual FIFO Interrupt Flag Register
11000484	AP_DMA_UART_1_TX_INT_EN	32	UART1 TX Virtual FIFO Interrupt Enable Register
11000488	AP_DMA_UART_1_TX_EN	32	UART1 TX Virtual FIFO Enable Register
1100048C	AP_DMA_UART_1_TX_RST	32	UART1 TX Virtual FIFO Reset Register
11000490	AP_DMA_UART_1_TX_STOP	32	UART1 TX Virtual FIFO Enable Register
11000494	AP_DMA_UART_1_TX_FLUSH	32	UART1 TX Virtual FIFO Flush Register
1100049C	AP_DMA_UART_1_TX_VFF_ADDR	32	UART1 TX Virtual FIFO Base Address Register
110004A4	AP_DMA_UART_1_TX_VFF_LEN	32	UART1 TX Virtual FIFO Length Register
110004A8	AP_DMA_UART_1_TX_VFF_THRE	32	UART1 TX Virtual FIFO Threshold Register
110004AC	AP_DMA_UART_1_TX_VFF_WPT	32	UART1 TX Virtual FIFO Write Pointer Register
110004B0	AP_DMA_UART_1_TX_VFF_RPT	32	UART1 TX Virtual FIFO Read Pointer Register
110004B8	AP_DMA_UART_1_TX_INT_BUF_SIZE	32	UART1 TX Internal Buffer Size Register
110004BC	AP_DMA_UART_1_TX_VFF_VALID_SIZE	32	UART1 TX Virtual FIFO Valid Size Register
110004C0	AP_DMA_UART_1_TX_VFF_LEFT_SIZE	32	UART1 TX Virtual FIFO Left Size Register
110004D0	AP_DMA_UART_1_TX_DEBUG_STATUS_00	32	UART1 TX Debug Status 00
110004D4	AP_DMA_UART_1_TX_VFF_WPT_REAL	32	UART1 TX Virtual FIFO Write Pointer Register Value
110004D8	AP_DMA_UART_1_TX_VFF_WPT_VALID	32	UART1 TX Virtual FIFO Write Pointer Register by HW Control
110004E0	AP_DMA_UART_1_TX_FLUSH_ACT	32	UART1 TX Virtual FIFO Flush Status Register
110004E4	AP_DMA_UART_1_TX_HW_FLUSH	32	UART1 TX Virtual FIFO HW Flush Register
11000500	AP_DMA_UART_1_RX_INT_FLAG	32	UART1 RX Virtual FIFO Interrupt Flag Register
11000504	AP_DMA_UART_1_RX_INT_EN	32	UART1 RX Virtual FIFO Interrupt Enable Register
11000508	AP_DMA_UART_1_RX_EN	32	UART1 RX Virtual FIFO Enable Register
1100050C	AP_DMA_UART_1_RX_RST	32	UART1 RX Virtual FIFO Reset Register
11000510	AP_DMA_UART_1_RX_STOP	32	UART1 RX Virtual FIFO Enable Register

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Address	Name	Width	Register Function
11000514	AP_DMA_UART_1_RX_FLUSH	32	UART1 RX Virtual FIFO Flush Register
1100051C	AP_DMA_UART_1_RX_VFF_ADDR	32	UART1 RX Virtual FIFO Base Address Register
11000524	AP_DMA_UART_1_RX_VFF_LEN	32	UART1 RX Virtual FIFO Length Register
11000528	AP_DMA_UART_1_RX_VFF_THRE	32	UART1 RX Virtual FIFO Threshold Register
1100052C	AP_DMA_UART_1_RX_VFF_WPT	32	UART1 RX Virtual FIFO Write Pointer Register
11000530	AP_DMA_UART_1_RX_VFF_RPT	32	UART1 RX Virtual FIFO Read Pointer Register
11000534	AP_DMA_UART_1_RX_FLOW_CTRL_THRE	32	UART1 RX Virtual FIFO Flow Control Threshold
11000538	AP_DMA_UART_1_RX_INT_BUF_SIZE	32	UART1 RX Internal Buffer Size Register
1100053C	AP_DMA_UART_1_RX_VFF_VALID_SIZE	32	UART1 RX Virtual FIFO Valid Size Register
11000540	AP_DMA_UART_1_RX_VFF_LEFT_SIZE	32	UART1 RX Virtual FIFO Left Size Register
11000550	AP_DMA_UART_1_RX_DEBUG_STATUS_00	32	UART1 RX Debug Status 00
11000580	AP_DMA_UART_2_TX_INT_FLAG	32	UART2 TX Virtual FIFO Interrupt Flag Register
11000584	AP_DMA_UART_2_TX_INT_EN	32	UART2 TX Virtual FIFO Interrupt Enable Register
11000588	AP_DMA_UART_2_TX_EN	32	UART2 TX Virtual FIFO Enable Register
1100058C	AP_DMA_UART_2_TX_RST	32	UART2 TX Virtual FIFO Reset Register
11000590	AP_DMA_UART_2_TX_STOP	32	UART2 TX Virtual FIFO Enable Register
11000594	AP_DMA_UART_2_TX_FLUSH	32	UART2 TX Virtual FIFO Flush Register
1100059C	AP_DMA_UART_2_TX_VFF_ADDR	32	UART2 TX Virtual FIFO Base Address Register
110005A4	AP_DMA_UART_2_TX_VFF_LEN	32	UART2 TX Virtual FIFO Length Register
110005A8	AP_DMA_UART_2_TX_VFF_THRE	32	UART2 TX Virtual FIFO Threshold Register
110005AC	AP_DMA_UART_2_TX_VFF_WPT	32	UART2 TX Virtual FIFO Write Pointer Register
110005B0	AP_DMA_UART_2_TX_VFF_RPT	32	UART2 TX Virtual FIFO Read Pointer Register
110005B8	AP_DMA_UART_2_TX_INT_BUF_SIZE	32	UART2 TX Internal Buffer Size Register
110005BC	AP_DMA_UART_2_TX_VFF_VALID_SIZE	32	UART2 TX Virtual FIFO Valid Size Register
110005C0	AP_DMA_UART_2_TX_VFF_LEFT_SIZE	32	UART2 TX Virtual FIFO Left Size Register

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Address	Name	Width	Register Function
110005D0	AP_DMA_UART_2_TX_DEBUG_STATUS_00	32	UART2 TX Debug Status 00
110005D4	AP_DMA_UART_2_TX_VFF_WPT_REAL	32	UART2 TX Virtual FIFO Write Pointer Register Value
110005D8	AP_DMA_UART_2_TX_VFF_WPT_VALID	32	UART2 TX Virtual FIFO Write Pointer Register by HW Control
110005E0	AP_DMA_UART_2_TX_FLUSH_ACT	32	UART2 TX Virtual FIFO Flush Status Register
110005E4	AP_DMA_UART_2_TX_HW_FLUSH	32	UART2 TX Virtual FIFO HW Flush Register
11000600	AP_DMA_UART_2_RX_INT_FLAG	32	UART2 RX Virtual FIFO Interrupt Flag Register
11000604	AP_DMA_UART_2_RX_INT_EN	32	UART2 RX Virtual FIFO Interrupt Enable Register
11000608	AP_DMA_UART_2_RX_EN	32	UART2 RX Virtual FIFO Enable Register
1100060C	AP_DMA_UART_2_RX_RST	32	UART2 RX Virtual FIFO Reset Register
11000610	AP_DMA_UART_2_RX_STOP	32	UART2 RX Virtual FIFO Enable Register
11000614	AP_DMA_UART_2_RX_FLUSH	32	UART2 RX Virtual FIFO Flush Register
1100061C	AP_DMA_UART_2_RX_VFF_ADDR	32	UART2 RX Virtual FIFO Base Address Register
11000624	AP_DMA_UART_2_RX_VFF_LEN	32	UART2 RX Virtual FIFO Length Register
11000628	AP_DMA_UART_2_RX_VFF_THRE	32	UART2 RX Virtual FIFO Threshold Register
1100062C	AP_DMA_UART_2_RX_VFF_WPT	32	UART2 RX Virtual FIFO Write Pointer Register
11000630	AP_DMA_UART_2_RX_VFF_RPT	32	UART2 RX Virtual FIFO Read Pointer Register
11000634	AP_DMA_UART_2_RX_FLOW_CTRL_THRE	32	UART2 RX Virtual FIFO Flow Control Threshold
11000638	AP_DMA_UART_2_RX_INT_BUF_SIZE	32	UART2 RX Internal Buffer Size Register
1100063C	AP_DMA_UART_2_RX_VFF_VALID_SIZE	32	UART2 RX Virtual FIFO Valid Size Register
11000640	AP_DMA_UART_2_RX_VFF_LEFT_SIZE	32	UART2 RX Virtual FIFO Left Size Register
11000650	AP_DMA_UART_2_RX_DEBUG_STATUS_00	32	UART2 RX Debug Status 00
11000680	AP_DMA_UART_3_TX_INT_FLAG	32	UART3 TX Virtual FIFO Interrupt Flag Register
11000684	AP_DMA_UART_3_TX_INT_EN	32	UART3 TX Virtual FIFO Interrupt Enable Register
11000688	AP_DMA_UART_3_TX_EN	32	UART3 TX Virtual FIFO Enable Register
1100068C	AP_DMA_UART_3_TX_RST	32	UART3 TX Virtual FIFO Reset Register

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Address	Name	Width	Register Function
11000690	AP_DMA_UART_3_TX_STOP	32	UART3 TX Virtual FIFO Enable Register
11000694	AP_DMA_UART_3_TX_FLUSH	32	UART3 TX Virtual FIFO Flush Register
1100069C	AP_DMA_UART_3_TX_VFF_ADDR	32	UART3 TX Virtual FIFO Base Address Register
110006A4	AP_DMA_UART_3_TX_VFF_LEN	32	UART3 TX Virtual FIFO Length Register
110006A8	AP_DMA_UART_3_TX_VFF_THRE	32	UART3 TX Virtual FIFO Threshold Register
110006AC	AP_DMA_UART_3_TX_VFF_WPT	32	UART3 TX Virtual FIFO Write Pointer Register
110006B0	AP_DMA_UART_3_TX_VFF_RPT	32	UART3 TX Virtual FIFO Read Pointer Register
110006B8	AP_DMA_UART_3_TX_INT_BUF_SIZE	32	UART3 TX Internal Buffer Size Register
110006BC	AP_DMA_UART_3_TX_VFF_VALID_SIZE	32	UART3 TX Virtual FIFO Valid Size Register
110006C0	AP_DMA_UART_3_TX_VFF_LEFT_SIZE	32	UART3 TX Virtual FIFO Left Size Register
110006D0	AP_DMA_UART_3_TX_DEBUG_STATUS_00	32	UART3 TX Debug Status 00
110006D4	AP_DMA_UART_3_TX_VFF_WPT_REAL	32	UART3 TX Virtual FIFO Write Pointer Register Value
110006D8	AP_DMA_UART_3_TX_VFF_WPT_VALID	32	UART3 TX Virtual FIFO Write Pointer Register by HW Control
110006E0	AP_DMA_UART_3_TX_FLUSH_ACT	32	UART3 TX Virtual FIFO Flush Status Register
110006E4	AP_DMA_UART_3_TX_HW_FLUSH	32	UART3 TX Virtual FIFO HW Flush Register
11000700	AP_DMA_UART_3_RX_INT_FLAG	32	UART3 RX Virtual FIFO Interrupt Flag Register
11000704	AP_DMA_UART_3_RX_INT_EN	32	UART3 RX Virtual FIFO Interrupt Enable Register
11000708	AP_DMA_UART_3_RX_EN	32	UART3 RX Virtual FIFO Enable Register
1100070C	AP_DMA_UART_3_RX_RST	32	UART3 RX Virtual FIFO Reset Register
11000710	AP_DMA_UART_3_RX_STOP	32	UART3 RX Virtual FIFO Enable Register
11000714	AP_DMA_UART_3_RX_FLUSH	32	UART3 RX Virtual FIFO Flush Register
1100071C	AP_DMA_UART_3_RX_VFF_ADDR	32	UART3 RX Virtual FIFO Base Address Register
11000724	AP_DMA_UART_3_RX_VFF_LEN	32	UART3 RX Virtual FIFO Length Register
11000728	AP_DMA_UART_3_RX_VFF_THRE	32	UART3 RX Virtual FIFO Threshold Register
1100072C	AP_DMA_UART_3_RX_VFF_WPT	32	UART3 RX Virtual FIFO Write Pointer Register
11000730	AP_DMA_UART_3_	32	UART3 RX Virtual FIFO Read Pointer Register

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Address	Name	Width	Register Function
	RX_VFF_RPT		
11000734	AP_DMA_UART_3_RX_FLOW_CTRL_THRE	32	UART3 RX Virtual FIFO Flow Control Threshold
11000738	AP_DMA_UART_3_RX_INT_BUF_SIZE	32	UART3 RX Internal Buffer Size Register
1100073C	AP_DMA_UART_3_RX_VFF_VALID_SIZE	32	UART3 RX Virtual FIFO Valid Size Register
11000740	AP_DMA_UART_3_RX_VFF_LEFT_SIZE	32	UART3 RX Virtual FIFO Left Size Register
11000750	AP_DMA_UART_3_RX_DEBUG_STATUS_00	32	UART3 RX Debug Status 00
11000780	AP_DMA_UART_4_TX_INT_FLAG	32	UART4 TX Virtual FIFO Interrupt Flag Register
11000784	AP_DMA_UART_4_TX_INT_EN	32	UART4 TX Virtual FIFO Interrupt Enable Register
11000788	AP_DMA_UART_4_TX_EN	32	UART4 TX Virtual FIFO Enable Register
1100078C	AP_DMA_UART_4_TX_RST	32	UART4 TX Virtual FIFO Reset Register
11000790	AP_DMA_UART_4_TX_STOP	32	UART4 TX Virtual FIFO Enable Register
11000794	AP_DMA_UART_4_TX_FLUSH	32	UART4 TX Virtual FIFO Flush Register
1100079C	AP_DMA_UART_4_TX_VFF_ADDR	32	UART4 TX Virtual FIFO Base Address Register
110007A4	AP_DMA_UART_4_TX_VFF_LEN	32	UART4 TX Virtual FIFO Length Register
110007A8	AP_DMA_UART_4_TX_VFF_THRE	32	UART4 TX Virtual FIFO Threshold Register
110007AC	AP_DMA_UART_4_TX_VFF_WPT	32	UART4 TX Virtual FIFO Write Pointer Register
110007B0	AP_DMA_UART_4_TX_VFF_RPT	32	UART4 TX Virtual FIFO Read Pointer Register
110007B8	AP_DMA_UART_4_TX_INT_BUF_SIZE	32	UART4 TX Internal Buffer Size Register
110007BC	AP_DMA_UART_4_TX_VFF_VALID_SIZE	32	UART4 TX Virtual FIFO Valid Size Register
110007C0	AP_DMA_UART_4_TX_VFF_LEFT_SIZE	32	UART4 TX Virtual FIFO Left Size Register
110007D0	AP_DMA_UART_4_TX_DEBUG_STATUS_00	32	UART4 TX Debug Status 00
110007D4	AP_DMA_UART_4_TX_VFF_WPT_REAL	32	UART4 TX Virtual FIFO Write Pointer Register Value
110007D8	AP_DMA_UART_4_TX_VFF_WPT_VALID	32	UART4 TX Virtual FIFO Write Pointer Register by HW Control
110007E0	AP_DMA_UART_4_TX_FLUSH_ACT	32	UART4 TX Virtual FIFO Flush Status Register
110007E4	AP_DMA_UART_4_	32	UART4 TX Virtual FIFO HW Flush Register

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Address	Name	Width	Register Function
	TX_HW_FLUSH		
11000800	AP_DMA_UART_4_RX_INT_FLAG	32	UART4 RX Virtual FIFO Interrupt Flag Register
11000804	AP_DMA_UART_4_RX_INT_EN	32	UART4 RX Virtual FIFO Interrupt Enable Register
11000808	AP_DMA_UART_4_RX_EN	32	UART4 RX Virtual FIFO Enable Register
1100080C	AP_DMA_UART_4_RX_RST	32	UART4 RX Virtual FIFO Reset Register
11000810	AP_DMA_UART_4_RX_STOP	32	UART4 RX Virtual FIFO Enable Register
11000814	AP_DMA_UART_4_RX_FLUSH	32	UART4 RX Virtual FIFO Flush Register
1100081C	AP_DMA_UART_4_RX_VFF_ADDR	32	UART4 RX Virtual FIFO Base Address Register
11000824	AP_DMA_UART_4_RX_VFF_LEN	32	UART4 RX Virtual FIFO Length Register
11000828	AP_DMA_UART_4_RX_VFF_THRE	32	UART4 RX Virtual FIFO Threshold Register
1100082C	AP_DMA_UART_4_RX_VFF_WPT	32	UART4 RX Virtual FIFO Write Pointer Register
11000830	AP_DMA_UART_4_RX_VFF_RPT	32	UART4 RX Virtual FIFO Read Pointer Register
11000834	AP_DMA_UART_4_RX_FLOW_CTRL_THRE	32	UART4 RX Virtual FIFO Flow Control Threshold
11000838	AP_DMA_UART_4_RX_INT_BUF_SIZE	32	UART4 RX Internal Buffer Size Register
1100083C	AP_DMA_UART_4_RX_VFF_VALID_SIZE	32	UART4 RX Virtual FIFO Valid Size Register
11000840	AP_DMA_UART_4_RX_VFF_LEFT_SIZE	32	UART4 RX Virtual FIFO Left Size Register
11000850	AP_DMA_UART_4_RX_DEBUG_STATUS_00	32	UART4 RX Debug Status 00
11000880	AP_DMA_UART_5_TX_INT_FLAG	32	UART5 TX Virtual FIFO Interrupt Flag Register
11000884	AP_DMA_UART_5_TX_INT_EN	32	UART5 TX Virtual FIFO Interrupt Enable Register
11000888	AP_DMA_UART_5_TX_EN	32	UART5 TX Virtual FIFO Enable Register
1100088C	AP_DMA_UART_5_TX_RST	32	UART5 TX Virtual FIFO Reset Register
11000890	AP_DMA_UART_5_TX_STOP	32	UART5 TX Virtual FIFO Enable Register
11000894	AP_DMA_UART_5_TX_FLUSH	32	UART5 TX Virtual FIFO Flush Register
1100089C	AP_DMA_UART_5_TX_VFF_ADDR	32	UART5 TX Virtual FIFO Base Address Register
110008A4	AP_DMA_UART_5_TX_VFF_LEN	32	UART5 TX Virtual FIFO Length Register
110008A8	AP_DMA_UART_5_TX_VFF_THRE	32	UART5 TX Virtual FIFO Threshold Register
110008AC	AP_DMA_UART_5_	32	UART5 TX Virtual FIFO Write Pointer Register

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Address	Name	Width	Register Function
	TX_VFF_WPT		
110008B0	AP_DMA_UART_5_TX_VFF_RPT	32	UART5 TX Virtual FIFO Read Pointer Register
110008B8	AP_DMA_UART_5_TX_INT_BUF_SIZE	32	UART5 TX Internal Buffer Size Register
110008BC	AP_DMA_UART_5_TX_VFF_VALID_SIZE	32	UART5 TX Virtual FIFO Valid Size Register
110008C0	AP_DMA_UART_5_TX_VFF_LEFT_SIZE	32	UART5 TX Virtual FIFO Left Size Register
110008D0	AP_DMA_UART_5_TX_DEBUG_STATUS_00	32	UART5 TX Debug Status 00
110008D4	AP_DMA_UART_5_TX_VFF_WPT_REAL	32	UART5 TX Virtual FIFO Write Pointer Register Value
110008D8	AP_DMA_UART_5_TX_VFF_WPT_VALID	32	UART5 TX Virtual FIFO Write Pointer Register by HW Control
110008E0	AP_DMA_UART_5_TX_FLUSH_ACT	32	UART5 TX Virtual FIFO Flush Status Register
110008E4	AP_DMA_UART_5_TX_HW_FLUSH	32	UART5 TX Virtual FIFO HW Flush Register
11000900	AP_DMA_UART_5_RX_INT_FLAG	32	UART5 RX Virtual FIFO Interrupt Flag Register
11000904	AP_DMA_UART_5_RX_INT_EN	32	UART5 RX Virtual FIFO Interrupt Enable Register
11000908	AP_DMA_UART_5_RX_EN	32	UART5 RX Virtual FIFO Enable Register
1100090C	AP_DMA_UART_5_RX_RST	32	UART5 RX Virtual FIFO Reset Register
11000910	AP_DMA_UART_5_RX_STOP	32	UART5 RX Virtual FIFO Enable Register
11000914	AP_DMA_UART_5_RX_FLUSH	32	UART5 RX Virtual FIFO Flush Register
1100091C	AP_DMA_UART_5_RX_VFF_ADDR	32	UART5 RX Virtual FIFO Base Address Register
11000924	AP_DMA_UART_5_RX_VFF_LEN	32	UART5 RX Virtual FIFO Length Register
11000928	AP_DMA_UART_5_RX_VFF_THRE	32	UART5 RX Virtual FIFO Threshold Register
1100092C	AP_DMA_UART_5_RX_VFF_WPT	32	UART5 RX Virtual FIFO Write Pointer Register
11000930	AP_DMA_UART_5_RX_VFF_RPT	32	UART5 RX Virtual FIFO Read Pointer Register
11000934	AP_DMA_UART_5_RX_FLOW_CTRL_THRE	32	UART5 RX Virtual FIFO Flow Control Threshold
11000938	AP_DMA_UART_5_RX_INT_BUF_SIZE	32	UART5 RX Internal Buffer Size Register
1100093C	AP_DMA_UART_5_RX_VFF_VALID_SIZE	32	UART5 RX Virtual FIFO Valid Size Register
11000940	AP_DMA_UART_5_RX_VFF_LEFT_SIZE	32	UART5 RX Virtual FIFO Left Size Register

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Address	Name	Width	Register Function
11000950	AP_DMA_UART_5_RX_DEBUG_STATUS_00	32	UART5 RX Debug Status 00

11000000 **AP_DMA_GLOBAL_INT_FLAG** **AP DMA Global Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															UART5_RX	UART5_TX
Type															RU	RU
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UART4_RX	UART4_TX	UART3_RX	UART3_TX	UART2_RX	UART2_TX	UART1_RX	UART1_TX	UART0_RX	UART0_TX	IRDA	I2C3	I2C2	I2C1	I2C0	HIF0
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	UART5_RX	
16	UART5_TX	
15	UART4_RX	
14	UART4_TX	
13	UART3_RX	
12	UART3_TX	
11	UART2_RX	
10	UART2_TX	
9	UART1_RX	
8	UART1_TX	
7	UART0_RX	
6	UART0_TX	
5	IRDA	
4	I2C3	
3	I2C2	
2	I2C1	
1	I2C0	
0	HIF0	

11000004 **AP_DMA_GLOBAL_RST** **AP DMA Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HAR	WAR

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															D_RST	**M_RST**
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**General DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**General DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 then waits for all running statuses to be 0 and sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000008	AP_DMA_GLOBAL_RUNNING_STATUS	AP DMA Global Running Status Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															**UART5_RX**	**UART5_TX**
Type															RO	RO
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**UART4_RX**	**UART4_TX**	**UART3_RX**	**UART3_TX**	**UART2_RX**	**UART2_TX**	**UART1_RX**	**UART1_TX**	**UART0_RX**	**UART0_TX**	**I2C4**	**I2C3**	**I2C2**	**I2C1**	**I2C0**	**HIF0**
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	UART5_RX	0: Idle 1: Running
16	UART5_TX	0: Idle 1: Running
15	UART4_RX	0: Idle 1: Running
14	UART4_TX	0: Idle 1: Running
13	UART3_RX	0: Idle 1: Running
12	UART3_TX	0: Idle 1: Running
11	UART2_RX	0: Idle 1: Running
10	UART2_TX	0: Idle 1: Running
9	UART1_RX	0: Idle 1: Running
8	UART1_TX	0: Idle 1: Running

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Bit(s)	Name	Description
7	UART0_RX	0: Idle 1: Running
6	UART0_TX	0: Idle 1: Running
5	I2C4	0: Idle 1: Running
4	I2C3	0: Idle 1: Running
3	I2C2	0: Idle 1: Running
2	I2C1	0: Idle 1: Running
1	I2C0	0: Idle 1: Running
0	HIF0	0: Idle 1: Running

1100000C **AP_DMA_GLOBAL_SLOW_DOWN** **AP DMA AXI Slow Down Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	W_SLOW_CNT															W_SLOW_EN
Type	RW															RW
Reset	0	0	0	0	0	0	0	0	0	0						0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R_SLOW_CNT															R_SLOW_EN
Type	RW															RW
Reset	0	0	0	0	0	0	0	0	0	0						0

Bit(s)	Name	Description
31:22	W_SLOW_CNT	**AXI write to external AXI slow-down counter** 0 ~ 1023; the number means cycle. 0: Wait for 0 cycle then issue request 1: Wait for 1 cycle then issue request
16	W_SLOW_EN	**Enables AXI write to external AXI slow-down** 0: No slow-down 1: Slow down
15:6	R_SLOW_CNT	**AXI read from external AXI slow-down counter** 0 ~ 1023; the number means cycle. 0: Wait for 0 cycle then issue request 1: Wait for 1 cycle then issue request
0	R_SLOW_EN	**Enables ARM side AXI read from external AXI slow-down** 0: No slow-down 1: Slow down

11000010 **AP_DMA_G** **AP DMA Security Enable Register** **00000000**

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LOBAL_SEC_EN

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**LOCK**	**DLOCK**														
Type	RW	RW														
Reset	0	0														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**UART4_RX**	**UART4_TX**	**UART3_RX**	**UART3_TX**	**UART2_RX**	**UART2_TX**	**UART1_RX**	**UART1_TX**	**UART0_RX**	**UART0_TX**	**I2C2**	**I2C1**	**I2C0**	**HIF0**	**G_DMA1**	**G_DMA0**
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	LOCK	**Locks secure bit** 0: Unlock channel secure bit write 1: Lock channel secure bit
30	DLOCK	**Locks domain registers** 0: Unlock channel domain register write 1: Lock channel domain register write
15	UART4_RX	0: This channel is non-secure. 1: This channel is secure.
14	UART4_TX	0: This channel is non-secure. 1: This channel is secure.
13	UART3_RX	0: This channel is non-secure. 1: This channel is secure.
12	UART3_TX	0: This channel is non-secure. 1: This channel is secure.
11	UART2_RX	0: This channel is non-secure. 1: This channel is secure.
10	UART2_TX	0: This channel is non-secure. 1: This channel is secure.
9	UART1_RX	0: This channel is non-secure. 1: This channel is secure.
8	UART1_TX	0: This channel is non-secure. 1: This channel is secure.
7	UART0_RX	0: This channel is non-secure. 1: This channel is secure.
6	UART0_TX	0: This channel is non-secure. 1: This channel is secure.
5	I2C2	0: This channel is non-secure. 1: This channel is secure.
4	I2C1	0: This channel is non-secure. 1: This channel is secure.
3	I2C0	0: This channel is non-secure. 1: This channel is secure.
2	HIF0	0: This channel is non-secure. 1: This channel is secure.
1	G_DMA1	0: This channel is non-secure. 1: This channel is secure.
0	G_DMA0	0: This channel is non-secure. 1: This channel is secure.

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11000014 **AP_DMA_GLOBAL_GSEC_EN** **AP DMA Global Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GLOCK															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																GSEC_EN
Type																RW
Reset																0

Bit(s)	Name	Description
31	GLOCK	0: Unlock 1: Lock
0	GSEC_EN	**Controls global security enable** When this bit is set to 0, the overall channel will be treated as non-security channel. When this bit is set to 1, the security property will depend on each channel's sec_en. 0: Disable 1: Enable

11000018 **AP_DMA_GLOBAL_VIO_DBG1** **AP DMA Security Latch Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LAT_ADDR[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LAT_ADDR[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LAT_ADDR	When any non-security transaction accesses DMA security zone and when R_VID or W_VID is not 1, DMA will latch the address of this transaction.

1100001C **AP_DMA_GLOBAL_VIO_DBG0** **AP DMA Global Security Abort Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CLR															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																

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Reset																

Bit(s)	Name	Description
31	CLR	**SW writes 1 to CLR to clear R_VID, W_VID and APB_ABORT to 0.** 0: Keep status 1: Clear status

11000020 AP_DMA_HIFo_SEC_EN AP HIFo DMA Security Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SEC_EN
Type																WO
Reset																0

Bit(s)	Name	Description
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000024 AP_DMA_IrDA_SEC_EN AP irdao DMA Security Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SEC_EN
Type																WO
Reset																0

Bit(s)	Name	Description
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000028 AP_DMA_I2Co_SEC_EN AP I2Co DMA Security Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

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Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**SEC_EN**
Type																WO
Reset																0

Bit(s)	Name	Description
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

1100002C <u>AP_DMA_I2C1_SEC_EN</u> AP I2C1 DMA Security Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**SEC_EN**
Type																WO
Reset																0

Bit(s)	Name	Description
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000030 <u>AP_DMA_I2C2_SEC_EN</u> AP I2C2 DMA Security Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**SEC_EN**
Type																WO
Reset																0

Bit(s)	Name	Description
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

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11000034 **AP_DMA_I2C3_SEC_EN** **AP I2C3 DMA Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SEC_EN
Type																WO
Reset																0

Bit(s)	Name	Description
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000038 **AP_DMA_UART0_TX_SEC_EN** **AP UART0 TX DMA Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SEC_EN
Type																WO
Reset																0

Bit(s)	Name	Description
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

1100003C **AP_DMA_UART0_RX_SEC_EN** **AP UART0 RX DMA Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SEC_EN
Type																WO
Reset																0

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Bit(s)	Name	Description
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000040 AP_DMA_UART1_TX_SEC_EN AP UART1 TX DMA Security Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SEC_EN
Type																WO
Reset																0

Bit(s)	Name	Description
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000044 AP_DMA_UART1_RX_SEC_EN AP UART1 RX DMA Security Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SEC_EN
Type																WO
Reset																0

Bit(s)	Name	Description
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000048 AP_DMA_UART2_TX_S AP UART2 TX DMA Security Enable 00000000

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	EC_EN	Register	

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SEC_EN
Type																WO
Reset																0

Bit(s)	Name	Description
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

1100004C	AP_DMA_UART2_RX_SEC_EN	AP UART2 RX DMA Security Enable Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SEC_EN
Type																WO
Reset																0

Bit(s)	Name	Description
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000050	AP_DMA_UART3_TX_SEC_EN	AP UART3 TX DMA Security Enable Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SEC_EN
Type																WO
Reset																0

Bit(s)	Name	Description

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Bit(s)	Name	Description
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000054	AP_DMA_UART3_RX_SEC_EN	AP UART3 RX DMA Security Enable Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SEC_EN
Type																WO
Reset																0

Bit(s)	Name	Description
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000058	AP_DMA_UART4_TX_SEC_EN	AP UART4 TX DMA Security Enable Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SEC_EN
Type																WO
Reset																0

Bit(s)	Name	Description
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

1100005C	AP_DMA_UART4_RX_SEC_EN	AP UART4 RX DMA Security Enable Register	00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SEC_EN
Type																WO
Reset																0

Bit(s)	Name	Description
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000060 **AP_DMA_UART5_TX_SEC_EN** **AP UART5 TX DMA Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SEC_EN
Type																WO
Reset																0

Bit(s)	Name	Description
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000064 **AP_DMA_UART5_RX_SEC_EN** **AP UART5 RX DMA Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SEC_EN
Type																WO
Reset																0

Bit(s)	Name	Description
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be

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Bit(s)	Name	Description
		treated as security channel. 0: Disable 1: Enable

11000070 **AP_DMA_MD_INT_EN** **AP DMA MD Interrupt Enable Register** **8003FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MD_INT_EN														dcm_en_uart5_rx	dcm_en_uart5_tx
Type	RW														RW	RW
Reset	1														1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dcm_en_uart4_rx	dcm_en_uart4_tx	dcm_en_uart3_rx	dcm_en_uart3_tx	dcm_en_uart2_rx	dcm_en_uart2_tx	dcm_en_uart1_rx	dcm_en_uart1_tx	dcm_en_uart0_rx	dcm_en_uart0_tx	i2c3	i2c2	i2c1	i2c0	irda	hifo
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31	MD_INT_EN	0: Disable 1: Enable
17	dcm_en_uart5_rx	0: Disable DCM 1: Enable DCM
16	dcm_en_uart5_tx	0: Disable DCM 1: Enable DCM
15	dcm_en_uart4_rx	0: Disable DCM 1: Enable DCM
14	dcm_en_uart4_tx	0: Disable DCM 1: Enable DCM
13	dcm_en_uart3_rx	0: Disable DCM 1: Enable DCM
12	dcm_en_uart3_tx	0: Disable DCM 1: Enable DCM
11	dcm_en_uart2_rx	0: Disable DCM 1: Enable DCM
10	dcm_en_uart2_tx	0: Disable DCM 1: Enable DCM
9	dcm_en_uart1_rx	0: Disable DCM 1: Enable DCM
8	dcm_en_uart1_tx	0: Disable DCM 1: Enable DCM
7	dcm_en_uart0_rx	0: Disable DCM 1: Enable DCM
6	dcm_en_uart0_tx	0: Disable DCM 1: Enable DCM
5	i2c3	0: Disable DCM 1: Enable DCM
4	i2c2	0: Disable DCM 1: Enable DCM
3	i2c1	0: Disable DCM

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Bit(s)	Name	Description
		1: Enable DCM
2	i2c0	0: Disable DCM 1: Enable DCM
1	irda	0: Disable DCM 1: Enable DCM
0	hifo	0: Disable DCM 1: Enable DCM

11000080 AP_DMA_HIF_0_INT_FLAG Peripheral DMA Interrupt Flag Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name																FLAG_0
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG_0	**This flag is raised when DMA is finished.** Write 0 to clear it. 1. After normal operation is done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 2. If STOP =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 3. If FLUSH =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 4. If WARM_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1. 5. If HARD_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1.

11000084 AP_DMA_HIF_0_INT_EN Peripheral DMA Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name																INTEN_FLAG_0
Type																RW
Reset																0

Bit(s)	Name	Description

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Bit(s)	Name	Description
0	INTEN_FLAG_0	**Enables interrupt for FLAG_0** 0: Disable 1: Enable

11000088 **AP_DMA_HIF_0_EN** **Peripheral DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**EN**
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables peripheral DMA** Set to 1 to start DMA when other control registers are set. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When FLUSH is set, EN will be 0 after the nearest transaction is finished and all internal data are delivered to destination; then DMA stops. When STOP is set, EN will be 0 after the nearest transaction is finished. 0: Disable 1: Enable

1100008C **AP_DMA_HIF_0_RST** **Peripheral DMA Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**HARD_RST**	**WARM_RST**
Type															RW	A0
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

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11000090	AP_DMA_HIF_0_STOP	Peripheral DMA Enable Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE	STOP
Type															RW	A0
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses peripheral DMA** Set to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	**Stops peripheral DMA** Set to 1 to stop DMA and wait for EN to become 0. HW then auto sets STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000094	AP_DMA_HIF_0_FLUSH	Peripheral DMA Flush Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes peripheral DMA** Set to 1 to stop DMA and allow DMA to flush its internal buffer residual data to EMI. After flush is finished, DMA will set EN back to 0 and stop DMA. There may still be data not transferred (len may not be 0). SW will set FLUSH to 1, wait for EN to become 0, and HW will auto set FLUSH back to 0 to finish the flush mechanism. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000098	AP_DMA_HIF_0_CON	Peripheral DMA Control Register	00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															**BURST_LEN**	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**SLOW_CNT**												**SLOW_EN**	**FIX_EN**	**DIR**
Type		RW												RW	RW	RW
Reset		0	0	0	0	0	0	0	0	0	0			0	0	0

Bit(s)	Name	Description
17:16	BURST_LEN	**Peripheral DMA burst length** Valid value: 0~3 0: 1-4 1: 2-4 2: 3-4 3: 4-4
14:5	SLOW_CNT	**Peripheral DMA slow-down counter** Only the read side is slowed down; the overall throughput will also decrease. Supports up to 1,023 cycles. 0: 0 cycle 1: 1 cycle
2	SLOW_EN	**Enables general DMA slow-down** 0: Disable 1: Enable
1	FIX_EN	**Peripheral DMA fixed pattern** When FIX_EN is turned on, DIR will be ignored, and DMA will always treat this transfer as Tx. 0: Does not use fixed pattern 1: Use fixed pattern
0	DIR	0: Tx 1: Rx

1100009C **AP_DMA_HIF_0_SRC_ADDR** **Peripheral DMA SRC Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SRC_ADDR[31:16]**															
Type	A0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SRC_ADDR[15:0]**															
Type	A0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_ADDR	**General DMA source address** It can be any byte alignment. When DIR=1 (Rx mode), src_addr equals the HIF FIFO address and must be 4-byte aligned. When FIX_EN = 1, SRC_ADDR will be treated as FIX_PATTERN. dir=1: HIF FIFO address dir=0: Memory address

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110000A0 **AP_DMA_HIF_0_DST_ADDR** **Peripheral DMA DST Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DST_ADDR[31:16]															
Type	A0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DST_ADDR[15:0]															
Type	A0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DST_ADDR	**Peripheral DMA destination address** This address is the HIF FIFO address when in Tx (dir=0) mode or the memory address when in Rx (dir=1) mode. Do not set MEM_ADDR to be within the last 8 bytes before the 4KB boundary when you use SYSRAM as a Tx/Rx memory, e.g. 0xff9 ~ 0xfff is not allowed to be MEM_ADDR when you use SYSRAM as a Tx/Rx memory. dir=1: memory address dir=0: HIF FIFO address

110000A4 **AP_DMA_HIF_0_LEN** **Peripheral DMA Transfer Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													LEN[19:16]			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LEN[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

110000B8 **AP_DMA_HIF_0_INT_BUF_SIZE** **Peripheral DMA Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RO							

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Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	

110000D0 **AP_DMA_HIF_0_DEBUG_STATUS_00** **Peripheral DMA Debug Status 00 Register** **00000013**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RADDR_D								WADDR_D_LH						
Type		RO								RO						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		WADDR_D										R_CLR	WREQ	RREQ	W_Q_CLR	R_Q_CLR
Type		RO										RO	RO	RO	RO	RO
Reset		0	0	0	0	0	0	0				1	0	0	1	1

Bit(s)	Name	Description
30:24	RADDR_D	
22:16	WADDR_D_LH	
14:8	WADDR_D	
4	R_CLR	
3	WREQ	
2	RREQ	
1	W_Q_CLR	
0	R_Q_CLR	

11000100 **AP_DMA_IrDA_0_INT_FLAG** **Peripheral DMA Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG_0
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG_0	**This flag is raised when DMA is finished.** Write 0 to clear it. 1. After normal operation is done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 2. If STOP =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1.

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Bit(s)	Name	Description
		3. If FLUSH =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 4. If WARM_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1. 5. If HARD_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1.

11000104 **AP_DMA_IrDA_0_INT_EN** **Peripheral DMA Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INTEN_FLAG_0
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN_FLAG_0	**Enables interrupt for FLAG_0** 0: Disable 1: Enable

11000108 **AP_DMA_IrDA_0_EN** **Peripheral DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables peripheral DMA** Set to 1 to start DMA. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When FLUSH is set, EN will be 0 after the nearest transaction is finished and all internal data are delivered to destination; then DMA stops. When STOP is set, EN will be 0 after the nearest transaction is finished. 0: Disable 1: Enable

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1100010C	AP_DMA_Irda_0_RST	Peripheral DMA Reset Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000110	AP_DMA_Irda_0_STOP	Peripheral DMA Enable Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE	STOP
Type															RW	A0
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses peripheral DMA** Set to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	**Stops peripheral DMA** Set to 1 to stop DMA and wait for EN to become 0. HW then auto sets STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000114	AP_DMA_Irda_0_FLUSH	Peripheral DMA Flush Register	00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes peripheral DMA** Set to 1 to stop DMA and allow DMA to flush its internal buffer residual data to EMI. After flush is finished, DMA will set EN back to 0 and stop DMA. There may still be data not transferred (len may not be 0). SW will set FLUSH to 1, wait for EN to become 0, and HW will auto set FLUSH back to 0 to finish the flush mechanism. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000118 **AP_DMA_IrDA_0_CON** **Peripheral DMA Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FIX_EN	DIR
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	FIX_EN	**Peripheral DMA fixed pattern** When FIX_EN is turned on, DIR will be ignored, and DMA will always treat this transfer as Tx. 0: Does not use fixed pattern 1: Use fixed pattern
0	DIR	0: Tx 1: Rx

1100011C **AP_DMA_IrDA_0_MEM_ADDR** **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEM_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEM_ADDR[15:0]															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. When FIX_EN=1, MEM_ADDR will be treated as FIX_PATTERN. DO NOT set RX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as TX/RX memory, e.g. 0xff9 ~ 0xfff are not allowed to be MEM_ADDR when you use SYSRAM as TX/RX memory.

11000124 **AP_DMA_IrDA_0_LEN** **Peripheral DMA Transfer Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

11000138 **AP_DMA_IrDA_0_INT_BUF_SIZE** **Peripheral DMA Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	

11000150 **AP_DMA_IrDA_0_DEBUG_STATUS_00** **Peripheral DMA Debug Status 00 Register** **00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RADDR_D								WADDR_D_LH							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WADDR_D											R_CLR	WREQ	RREQ	W_Q_CLR	R_Q_CLR
Type	RO											RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
31:24	RADDR_D	
23:16	WADDR_D_LH	
15:8	WADDR_D	
4	R_CLR	
3	WREQ	
2	RREQ	
1	W_Q_CLR	
0	R_Q_CLR	

11000180 **AP_DMA_I2C_0_INT_FLAG** **Peripheral DMA Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FLAG_0	RX_FLAG	TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FLAG_0	**Raised when TX-to-RX is asserted when DMA engine is running.**
1	RX_FLAG	**Raised when RX DMA is finished.** Write 0 to clear it.
0	TX_FLAG	**This flag is raised when TX DMA is finished.** Write 0 to clear it. 1. After normal operation is done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 2. If STOP =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 3. If FLUSH =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 4. If WARM_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1. 5. If HARD_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1.

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11000184	AP_DMA_I2C_0_INT_EN	Peripheral DMA Interrupt Enable Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														INTEN_FLAG_0	INTEN_RX_FLAG	INTEN_TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	INTEN_FLAG_0	**Enables interrupt for FLAG_0** 0: Disable 1: Enable
1	INTEN_RX_FLAG	**Enables interrupt for RX_FLAG** 0: Disable 1: Enable
0	INTEN_TX_FLAG	**Enables interrupt for TX_FLAG** 0: Disable 1: Enable

11000188	AP_DMA_I2C_0_EN	Peripheral DMA Enable Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables peripheral DMA** Set to 1 to start DMA. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When FLUSH is set, EN will be 0 after the nearest transaction is finished and all internal data are delivered to destination; then DMA stops. When STOP is set, EN will be 0 after the nearest transaction is finished. 0: Disable 1: Enable

1100018C	AP_DMA_I2C_0_RST	Peripheral DMA Reset Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	A0
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000190 **AP_DMA_I2C_0_STOP** **Peripheral DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE	STOP
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses peripheral DMA** Set to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	**Stops peripheral DMA** Set to 1 to stop DMA and wait for EN to become 0. HW then auto sets STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000194 **AP_DMA_I2C_0_FLUSH** **Peripheral DMA Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes peripheral DMA** Set to 1 to stop DMA and allow DMA to flush its internal buffer residual data to EMI. After flush is finished, DMA will set EN back to 0 and stop DMA. There may still be data not transferred (len may not be 0). SW will set FLUSH to 1, wait for EN to become 0, and HW will auto set FLUSH back to 0 to finish the flush mechanism. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000198 **AP_DMA_I2C_0_CON** **Peripheral DMA Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FIX_EN	DIR
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	FIX_EN	**Peripheral DMA fixed pattern** When FIX_EN is turned on, DIR will be ignored, and DMA will always treat this transfer as Tx. 0: Does not use fixed pattern 1: Use fixed pattern
0	DIR	0: Tx 1: Rx

1100019C **AP_DMA_I2C_0_TX_MEM_ADDR** **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MEM_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MEM_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MEM_ADDR	**Peripheral DMA memory address**

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Bit(s)	Name	Description
		It can be any byte alignment. This address will be increased after each bus transaction. When FIX_EN = 1, TX_MEM_ADDR will be treated as FIX_PATTERN. DO NOT set TX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be TX_MEM_ADDR when you use SYSRAM as a source memory.

110001A0 **AP_DMA_I2C_0_RX_MEM_ADDR** **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MEM_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MEM_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. DO NOT set RX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be RX_MEM_ADDR when you use SYSRAM as a destination memory.

110001A4 **AP_DMA_I2C_0_TX_LEN** **Peripheral DMA Transfer Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

110001A8 **AP_DMA_I2C_0_RX_LE** **Peripheral DMA Transfer Length Register** **00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

110001B8	AP_DMA_I2C_0_INT_BUF_SIZE	Peripheral DMA Internal Buffer Size Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	

110001D0	AP_DMA_I2C_0_DEBUG_STATUS_00	Peripheral DMA Debug Status 00 Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RADDR_D								WADDR_D_LH							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WADDR_D											R_CLR	WREQ	RREQ	W_Q_CLR	R_Q_CLR
Type	RO											RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
31:24	RADDR_D	
23:16	WADDR_D_LH	

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Bit(s)	Name	Description
15:8	WADDR_D	
4	R_CLR	
3	WREQ	
2	RREQ	
1	W_Q_CLR	
0	R_Q_CLR	

11000200 **AP_DMA_I2C_1_INT_FLAG** **Peripheral DMA Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FLAG_0	RX_FLAG	TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FLAG_0	**Raised when TX-to-RX is asserted when DMA engine is running.**
1	RX_FLAG	**Raised when RX DMA is finished.** Write 0 to clear it.
0	TX_FLAG	**This flag is raised when TX DMA is finished.** Write 0 to clear it. 1. After normal operation is done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 2. If STOP =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 3. If FLUSH =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 4. If WARM_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1. 5. If HARD_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1.

11000204 **AP_DMA_I2C_1_INT_EN** **Peripheral DMA Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														INTEN_FLAG_0	INTEN_RX_FLAG	INTEN_TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

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Bit(s)	Name	Description
2	INTEN_FLAG_0	**Enables interrupt for FLAG_0** 0: Disable 1: Enable
1	INTEN_RX_FLAG	**Enables interrupt for RX_FLAG** 0: Disable 1: Enable
0	INTEN_TX_FLAG	**Enables interrupt for TX_FLAG** 0: Disable 1: Enable

11000208 AP_DMA_I2C_1_EN Peripheral DMA Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables peripheral DMA** Set to 1 to start DMA. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When FLUSH is set, EN will be 0 after the nearest transaction is finished and all internal data are delivered to destination; then DMA stops. When STOP is set, EN will be 0 after the nearest transaction is finished. 0: Disable 1: Enable

1100020C AP_DMA_I2C_1_RST Peripheral DMA Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable

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Bit(s)	Name	Description
		1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000210 **AP_DMA_I2C_1_STOP** **Peripheral DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name															PAUSE	STOP
Type															RW	A0
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses peripheral DMA** Set to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	**Stops peripheral DMA** Set to 1 to stop DMA and wait for EN to become 0. HW then auto sets STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000214 **AP_DMA_I2C_1_FLUSH** **Peripheral DMA Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes peripheral DMA** Set to 1 to stop DMA and allow DMA to flush its internal buffer residual data to EMI. After flush is finished, DMA will set EN back to 0 and stop DMA. There may still be data not transferred (len may not be 0). SW will set FLUSH to 1, wait for EN to become 0, and HW will auto set FLUSH back to 0 to finish the flush mechanism.

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Bit(s)	Name	Description
		Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

11000218 **AP_DMA_I2C_1_CON** **Peripheral DMA Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FIX_EN	DIR
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	FIX_EN	**Peripheral DMA fixed pattern** When FIX_EN is turned on, DIR will be ignored, and DMA will always treat this transfer as Tx. 0: Does not use fixed pattern 1: Use fixed pattern
0	DIR	0: Tx 1: Rx

1100021C **AP_DMA_I2C_1_TX_MEM_ADDR** **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MEM_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MEM_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. When FIX_EN = 1, TX_MEM_ADDR will be treated as FIX_PATTERN. DO NOT set TX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be TX_MEM_ADDR when you use SYSRAM as a source memory.

11000220 **AP_DMA_I2C_1_RX_MEM_ADDR** **Peripheral DMA Memory Address Register** **00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MEM_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MEM_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. DO NOT set RX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be RX_MEM_ADDR when you use SYSRAM as a destination memory.

11000224 **AP_DMA_I2C_1_TX_LEN** **Peripheral DMA Transfer Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

11000228 **AP_DMA_I2C_1_RX_LEN** **Peripheral DMA Transfer Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus

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Bit(s)	Name	Description
		transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

11000238	**AP_DMA_I2C_1_INT_BUF_SIZE**	**Peripheral DMA Internal Buffer Size Register**	**00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	

11000250	**AP_DMA_I2C_1_DEBUG_STATUS_00**	**Peripheral DMA Debug Status 00 Register**	**00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RADDR_D								WADDR_D_LH							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WADDR_D											R_CLR	WREQ	RREQ	W_Q_CLR	R_Q_CLR
Type	RO											RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
31:24	RADDR_D	
23:16	WADDR_D_LH	
15:8	WADDR_D	
4	R_CLR	
3	WREQ	
2	RREQ	
1	W_Q_CLR	
0	R_Q_CLR	

11000280	**AP_DMA_I2C_2_INT_FL**	**Peripheral DMA Interrupt Flag Register**	**00000000**

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AG

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FLAG_0	RX_FLAG	TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FLAG_0	**Raised when TX-to-RX is asserted when DMA engine is running.**
1	RX_FLAG	**Raised when RX DMA is finished.** Write 0 to clear it.
0	TX_FLAG	**This flag is raised when TX DMA is finished.** Write 0 to clear it. 1. After normal operation is done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 2. If STOP =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 3. If FLUSH =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 4. If WARM_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1. 5. If HARD_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1.

11000284 AP_DMA_I2C_2_INT_EN Peripheral DMA Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														INTEN_FLAG_0	INTEN_RX_FLAG	INTEN_TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	INTEN_FLAG_0	**Enables interrupt for FLAG_0** 0: Disable 1: Enable
1	INTEN_RX_FLAG	**Enables interrupt for RX_FLAG** 0: Disable 1: Enable
0	INTEN_TX_FLAG	**Enables interrupt for TX_FLAG** 0: Disable 1: Enable

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11000288 **AP_DMA_I2C_2_EN** **Peripheral DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables peripheral DMA** Set to 1 to start DMA. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When FLUSH is set, EN will be 0 after the nearest transaction is finished and all internal data are delivered to destination; then DMA stops. When STOP is set, EN will be 0 after the nearest transaction is finished. 0: Disable 1: Enable

1100028C **AP_DMA_I2C_2_RST** **Peripheral DMA Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000290 **AP_DMA_I2C_2_STOP** **Peripheral DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

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Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**PAUSE**	**STOP**
Type															RW	A0
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses peripheral DMA** Set to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	**Stops peripheral DMA** Set to 1 to stop DMA and wait for EN to become 0. HW then auto sets STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000294 **AP_DMA_I2C_2_FLUSH** **Peripheral DMA Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**FLUSH**
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes peripheral DMA** Set to 1 to stop DMA and allow DMA to flush its internal buffer residual data to EMI. After flush is finished, DMA will set EN back to 0 and stop DMA. There may still be data not transferred (len may not be 0). SW will set FLUSH to 1, wait for EN to become 0, and HW will auto set FLUSH back to 0 to finish the flush mechanism. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000298 **AP_DMA_I2C_2_CON** **Peripheral DMA Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**FIX_EN**	**DIR**

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Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	FIX_EN	**Peripheral DMA fixed pattern** When FIX_EN is turned on, DIR will be ignored, and DMA will always treat this transfer as Tx. 0: Does not use fixed pattern 1: Use fixed pattern
0	DIR	0: Tx 1: Rx

1100029C **AP_DMA_I2C_2_TX_MEM_ADDR** **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**TX_MEM_ADDR[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TX_MEM_ADDR[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. When FIX_EN = 1, TX_MEM_ADDR will be treated as FIX_PATTERN. DO NOT set TX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be TX_MEM_ADDR when you use SYSRAM as a source memory.

110002A0 **AP_DMA_I2C_2_RX_MEM_ADDR** **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RX_MEM_ADDR[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RX_MEM_ADDR[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. DO NOT set RX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be RX_MEM_ADDR when you use SYSRAM as a destination memory.

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110002A4 AP_DMA_I2C_2_TX_LEN Peripheral DMA Transfer Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

110002A8 AP_DMA_I2C_2_RX_LEN Peripheral DMA Transfer Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

110002B8 AP_DMA_I2C_2_INT_BUF_SIZE Peripheral DMA Internal Buffer Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RO							

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Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	

110002D0 AP_DMA_I2C_2_DEBUG_STATUS_0 — Peripheral DMA Debug Status 00 Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RADDR_D								WADDR_D_LH							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WADDR_D											R_CLR	WREQ	RREQ	W_Q_CLR	R_Q_CLR
Type	RO											RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
31:24	RADDR_D	
23:16	WADDR_D_LH	
15:8	WADDR_D	
4	R_CLR	
3	WREQ	
2	RREQ	
1	W_Q_CLR	
0	R_Q_CLR	

11000300 AP_DMA_I2C_3_INT_FLAG — Peripheral DMA Interrupt Flag Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FLAG_0	RX_FLAG	TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FLAG_0	**Raised when TX-to-RX is asserted when DMA engine is running.**
1	RX_FLAG	**Raised when RX DMA is finished.** Write 0 to clear it.
0	TX_FLAG	**This flag is raised when TX DMA is finished.**

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Bit(s)	Name	Description
		Write 0 to clear it. 1. After normal operation is done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 2. If STOP =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 3. If FLUSH =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 4. If WARM_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1. 5. If HARD_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1.

11000304 AP_DMA_I2C_3_INT_EN Peripheral DMA Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														INTEN_FLAG_0	INTEN_RX_FLAG	INTEN_TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	INTEN_FLAG_0	**Enables interrupt for FLAG_0** 0: Disable 1: Enable
1	INTEN_RX_FLAG	**Enables interrupt for RX_FLAG** 0: Disable 1: Enable
0	INTEN_TX_FLAG	**Enables interrupt for TX_FLAG** 0: Disable 1: Enable

11000308 AP_DMA_I2C_3_EN Peripheral DMA Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables peripheral DMA** Set to 1 to start DMA. When DMA is busy, EN will always be 1. When DMA is

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Bit(s)	Name	Description
		finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When FLUSH is set, EN will be 0 after the nearest transaction is finished and all internal data are delivered to destination; then DMA stops. When STOP is set, EN will be 0 after the nearest transaction is finished. 0: Disable 1: Enable

1100030C **AP_DMA_I2C_3_RST** **Peripheral DMA Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000310 **AP_DMA_I2C_3_STOP** **Peripheral DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE	STOP
Type															RW	A0
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses peripheral DMA** Set to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	**Stops peripheral DMA** Set to 1 to stop DMA and wait for EN to become 0. HW then auto sets STOP

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Bit(s)	Name	Description
		back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000314 **AP_DMA_I2C_3_FLUSH** **Peripheral DMA Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes peripheral DMA** Set to 1 to stop DMA and allow DMA to flush its internal buffer residual data to EMI. After flush is finished, DMA will set EN back to 0 and stop DMA. There may still be data not transferred (len may not be 0). SW will set FLUSH to 1, wait for EN to become 0, and HW will auto set FLUSH back to 0 to finish the flush mechanism. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000318 **AP_DMA_I2C_3_CON** **Peripheral DMA Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FIX_EN	DIR
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	FIX_EN	**Peripheral DMA fixed pattern** When FIX_EN is turned on, DIR will be ignored, and DMA will always treat this transfer as Tx. 0: Does not use fixed pattern 1: Use fixed pattern
0	DIR	0: Tx 1: Rx

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1100031C	AP_DMA_I2C_3_TX_MEM_ADDR	Peripheral DMA Memory Address Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MEM_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MEM_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. When FIX_EN = 1, TX_MEM_ADDR will be treated as FIX_PATTERN. DO NOT set TX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be TX_MEM_ADDR when you use SYSRAM as a source memory.

11000320	AP_DMA_I2C_3_RX_MEM_ADDR	Peripheral DMA Memory Address Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MEM_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MEM_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. DO NOT set RX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be RX_MEM_ADDR when you use SYSRAM as a destination memory.

11000324	AP_DMA_I2C_3_TX_LEN	Peripheral DMA Transfer Length Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	TX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

11000328	AP_DMA_I2C_3_RX_LEN	Peripheral DMA Transfer Length Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

11000338	AP_DMA_I2C_3_INT_BUF_SIZE	Peripheral DMA Internal Buffer Size Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	

11000350	AP_DMA_I2C_3_DEBUG_STATUS_00	Peripheral DMA Debug Status 00 Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	RADDR_D								WADDR_D_LH							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WADDR_D											R_CLR	WREQ	RREQ	W_Q_CLR	R_Q_CLR
Type	RO											RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
31:24	RADDR_D	
23:16	WADDR_D_LH	
15:8	WADDR_D	
4	R_CLR	
3	WREQ	
2	RREQ	
1	W_Q_CLR	
0	R_Q_CLR	

11000380 **AP_DMA_UART_0_TX_INT_FLAG** **UART0 TX Virtual FIFO Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG0
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG0	**Write 0 to clear it.** Interrupt will be issued to HW when FLAG=1. Mechanism: 1. SW puts data into VFF and detects TX_VFF_LEFT_SIZE is approaching 0. 2. SW sets INTEN=1 and leaves the task to wait for interrupt. 3. When HW delivers enough data to UART and makes TX_VFF_LEFT_SIZE >= TX_VFF_THRS, HW sets the flag to 1 and issues interrupt. 4. When SW receives this interrupt, it must set FLAG back to 0 and go on pushing data into VFF.

11000384 **AP_DMA_UART_0_TX_INT_EN** **UART0 TX Virtual FIFO Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name																**INTEN**
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	**Controls interrupt enable** This bit is used to control if the flag will be set to 1 when TX_VFF_LEFT_SIZE >= TX_VFF_THRS. 0: Does not set flag to 1, even tx_vff_left_size >= tx_vff_thrs 1: Set flag to 1 and HW auto sets inten back to 0 when tx_vff_left_size >= tx_vff_thrs.

11000388 AP_DMA_UART_0_TX_EN UART0 TX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**EN**
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART0 TX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When EN = 0 and MCU writes data to the VFF_W port (an AHB slave port), VFF_W will ignore this command, and the data will not be write to virtual FIFO. 0: Disable 1: Enable

1100038C AP_DMA_UART_0_TX_RST UART0 TX Virtual FIFO Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**HARD_RST**	**WARM_RST**
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism.

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Bit(s)	Name	Description
		0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RSTt to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000390 **AP_DMA_UART_0_TX_STOP** **UART0 TX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																A0
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART0 TX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000394 **AP_DMA_UART_0_TX_FLUSH** **UART0 TX Virtual FIFO Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART0 TX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. *Note: STOP and FLUSH cannot be set to 1 in the same operation.*

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Bit(s)	Name	Description
		0: Flush finished 1: Enable

1100039C	AP_DMA_UART_0_TX_VFF_ADDR	UART0 TX Virtual FIFO Base Address Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_VFF_ADDR[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_ADDR[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	TX_VFF_ADDR	**UART0 memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

110003A4	AP_DMA_UART_0_TX_VFF_LEN	UART0 TX Virtual FIFO Length Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	TX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

110003A8	AP_DMA_UART_0_TX_VFF_THRE	UART0 TX Virtual FIFO Threshold Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_THRE															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_THRE	**VFF threshold in byte alignment** In TX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In RX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

110003AC AP_DMA_UART_0_TX_VFF_WPT UART0 TX Virtual FIFO Write Pointer Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP
Type																RW
Reset																0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	TX_VFF_WPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP	**TX VFF write pointer wrap bit** It is initialized to 0. When wrapped to the ring head again, invert this bit. For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.
15:0	TX_VFF_WPT	**Byte alignment FIFO write pointer** For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.

110003B0 AP_DMA_UART_0_TX_VFF_RPT UART0 TX Virtual FIFO Read Pointer Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_RPT_WRAP
Type																RO
Reset																0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	TX_VFF_RPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_RPT_WRAP	**TX VFF read pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.

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Bit(s)	Name	Description
15:0	TX_VFF_RPT	**TX VFF read pointer maintained by hardware** In byte alignment.

110003B8 **AP_DMA_UART0_TX_INT_BUF_SIZE** **UART0 TX Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TX_INT_BUF_SIZE	**Virtual FIFO DMA TX internal buffer size** 0: 0 byte 1: 1 byte

110003BC **AP_DMA_UART0_TX_VFF_VALID_SIZE** **UART0 TX Virtual FIFO Valid Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_VALID_SIZE	**TX virtual FIFO valid size** 0: 0 byte 1: 1 byte

110003C0 **AP_DMA_UART0_TX_VFF_LEFT_SIZE** **UART0 TX Virtual FIFO Left Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	TX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_LEFT_SIZE	**TX virtual FIFO left size** 0: 0 byte 1: 1 byte

110003D0 **AP_DMA_UART_0_TX_DEBUG_STATUS_00** **UART0 TX Debug Status 00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				WADDR_D					FLUSH_ACT	FLUSH_STR	WD_ACT	RD_ACT	WREQ	RREQ	W_Q_CLR	R_Q_CLR
Type				RO					RO	RO	RO	RO	RO	RO	RO	RO
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
6	FLUSH_STR	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	
1	W_Q_CLR	
0	R_Q_CLR	

110003D4 **AP_DMA_UART_0_TX_VFF_WPT_REAL** **UART0 TX Virtual FIFO Write Pointer Register Value** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_REAL
Type																RO
Reset																0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_REAL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_REAL	**TX VFF write pointer wrap bit** If HW_FLUSH=1, sync to TX_VFF_WPT_WRAP_VALID. If HW_FLUSH=0, sync to TX_VFF_WPT_WRAP.
15:0	TX_VFF_WPT_REAL	**TX VFF write pointer** If HW_FLUSH=1, sync to TX_VFF_WPT_VALID. If HW_FLUSH=0, sync to TX_VFF_WPT.

110003D8 **AP_DMA_UART_0_TX_VFF_WPT_VALID** **UART0 TX Virtual FIFO Write Pointer Register by HW Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_VALID
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_VALID	**TX VFF write pointer wrap bit** If FLUSH= 0, sync to TX_VFF_WPT_WRAP. If flush, it will not update the value until the flush is finished.
15:0	TX_VFF_WPT_VALID	**TX VFF write pointer** If FLUSH= 0, sync to TX_VFF_WPT. If flush, it will not update the value until the flush is finished.

110003E0 **AP_DMA_UART_0_TX_FLUSH_ACT** **UART0 TX Virtual FIFO Flush Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLUSH_NEXT	FLUSH_ACT
Type															RO	RO

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Reset															0	0

Bit(s)	Name	Description
1	FLUSH_NEXT	There is a flush command when the UART0 TX channel is flushing.
0	FLUSH_ACT	UART0 TX channel flush status

110003E4 **AP_DMA_UART_0_TX_HW_FLUSH** **UART0 TX Virtual FIFO HW Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**HW_FLUSH**
Type																RW
Reset																0

Bit(s)	Name	Description
0	HW_FLUSH	**Flush control bit** Controls the UART TX write pointer if the SW setting value at flushing is updated. 0: Update WPT with SW setting 1: Update WPT when flush =0

11000400 **AP_DMA_UART_0_RX_INT_FLAG** **UART0 RX Virtual FIFO Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**FLAG1**	**FLAG0**
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	FLAG1	**Write 1 to clear it.** This flag is raised when UART issues flush to DMA and all data in UART FIFO are transferred to VFF.
0	FLAG0	**Write 1 to clear it.** This flag is raised when RX_VFF_VALID_SIZE >= RX_VFF_THRE. (VFF is almost full and MCU needs to consume those data.)

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11000404	AP_DMA_UART_0_RX_INT_EN	UART0 RX Virtual FIFO Interrupt Enable Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INTEN1	INTEN0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	INTEN1	**Controls interrupt enable** Only when this bit is set to 1 will flag1 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag1 will still be set to 1 regardless of this bit. 0: Disable 1: Enable
0	INTEN0	**Controls interrupt enable** Only when this bit is set to 1 will flag0 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag0 will still be set to 1 regardless of this bit. 0: Disable 1: Enable

11000408	AP_DMA_UART_0_RX_EN	UART0 RX Virtual FIFO Enable Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART0 RX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

1100040C	AP_DMA_UART_0_RX_RST	UART0 RX Virtual FIFO Reset Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000410 AP_DMA_UART_0_RX_STOP UART0 RX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																A0
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART0 RX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

11000414 AP_DMA_UART_0_RX_FLUSH UART0 RX Virtual FIFO Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0

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Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART0 RX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Flush finished 1: Enable

1100041C AP_DMA_UART_0_RX_VFF_ADDR UART0 RX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_VFF_ADDR[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_ADDR[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	RX_VFF_ADDR	**UART0 memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

11000424 AP_DMA_UART_0_RX_VFF_LEN UART0 RX Virtual FIFO Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	RX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

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11000428 **AP_DMA_UART_0_RX_VFF_THRE** **UART0 RX Virtual FIFO Threshold Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_THRE	**VFF threshold in byte alignment** In RX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In TX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

1100042C **AP_DMA_UART_0_RX_VFF_WPT** **UART0 RX Virtual FIFO Write Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_WPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_WPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_WPT_WRAP	**RX VFF write pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_WPT	**RX VFF write pointer maintained by hardware** In byte alignment.

11000430 **AP_DMA_UART_0_RX_VFF_RPT** **UART0 RX Virtual FIFO Read Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_RPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_RPT															

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Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_RPT_WRAP	**RX VFF read pointer wrap bit maintained by software** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_RPT	**RX VFF read pointer maintained by software** In byte alignment.

11000434 **AP_DMA_UART_0_RX_FLOW_CTRL_THRE** **UART0 RX Virtual FIFO Flow Control Threshold** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_FLOW_CTRL_THRE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RX_FLOW_CTRL_THRE	**VFF flow control threshold in byte alignment** In RX mode, DMA issues flow control when left size in VFF is smaller than the threshold.

11000438 **AP_DMA_UART_0_RX_INT_BUF_SIZE** **UART0 RX Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RX_INT_BUF_SIZE	**Virtual FIFO DMA RX internal buffer size** 0: 0 byte 1: 1 byte

1100043C **AP_DMA_UART_0_RX_VFF_VALID** **UART0 RX Virtual FIFO Valid Size Register** **00000000**

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SIZE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_VALID_SIZE	**RX virtual FIFO valid size** 0: 0 byte 1: 1 byte

11000440 **AP_DMA_UART_0_RX_VFF_LEFT_SIZE** **UART0 RX Virtual FIFO Left Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_LEFT_SIZE	**RX virtual FIFO left size** 0: 0 byte 1: 1 byte

11000450 **AP_DMA_UART_0_RX_DEBUG_STATUS_00** **UART0 RX Debug Status 00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D					FLUSH_ACT		WD_ACT	RD_ACT	WREQ	RREQ		
Type				RO					RO		RO	RO	RO	RO		
Reset				0	0	0	0	0	0		0	0	0	0		

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	

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Bit(s)	Name	Description
12:8	WADDR_D	
7	FLUSH_ACT	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	

11000480 **AP_DMA_UART_1_TX_INT_FLAG** **UART1 TX Virtual FIFO Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG0
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG0	**Write 0 to clear it.** Interrupt will be issued to HW when FLAG=1. Mechanism: 1. SW puts data into VFF and detects TX_VFF_LEFT_SIZE is approaching 0. 2. SW sets INTEN=1 and leaves the task to wait for interrupt. 3. When HW delivers enough data to UART and makes TX_VFF_LEFT_SIZE >= TX_VFF_THRS, HW sets the flag to 1 and issues interrupt. 4. When SW receives this interrupt, it must set FLAG back to 0 and go on pushing data into VFF.

11000484 **AP_DMA_UART_1_TX_INT_EN** **UART1 TX Virtual FIFO Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INTEN
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	**Controls interrupt enable** This bit is used to control if the flag will be set to 1 when TX_VFF_LEFT_SIZE >= TX_VFF_THRS. 0: Does not set flag to 1, even tx_vff_left_size >= tx_vff_thrs 1: Set flag to 1 and HW auto sets inten back to 0 when tx_vff_left_size >=

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Bit(s)	Name	Description
		tx_vff_thrs.

11000488 **AP_DMA_UART_1_TX_EN** **UART1 TX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART1 TX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When EN = 0 and MCU writes data to the VFF_W port (an AHB slave port), VFF_W will ignore this command, and the data will not be write to virtual FIFO. 0: Disable 1: Enable

1100048C **AP_DMA_UART_1_TX_RST** **UART1 TX Virtual FIFO Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RSTt to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

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11000490	AP_DMA_UART_1_TX_STOP	UART1 TX Virtual FIFO Enable Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																A0
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART1 TX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000494	AP_DMA_UART_1_TX_FLUSH	UART1 TX Virtual FIFO Flush Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART1 TX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Flush finished 1: Enable

1100049C	AP_DMA_UART_1_TX_VFF_ADDR	UART1 TX Virtual FIFO Base Address Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_VFF_ADDR[28:13]															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_ADDR[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	TX_VFF_ADDR	**UART1 memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

110004A4 AP_DMA_UART_1_TX_VFF_LEN UART1 TX Virtual FIFO Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	TX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

110004A8 AP_DMA_UART_1_TX_VFF_THRE UART1 TX Virtual FIFO Threshold Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_THRE	**VFF threshold in byte alignment** In TX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In RX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

110004AC AP_DMA_U UART1 TX Virtual FIFO Write Pointer 00000000

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	ART_1_TX_VFF_WPT	Register	

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP	**TX VFF write pointer wrap bit** It is initialized to 0. When wrapped to the ring head again, invert this bit. For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.
15:0	TX_VFF_WPT	**Byte alignment FIFO write pointer** For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.

110004B0	AP_DMA_UART_1_TX_VFF_RPT	UART1 TX Virtual FIFO Read Pointer Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_RPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_RPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_RPT_WRAP	**TX VFF read pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	TX_VFF_RPT	**TX VFF read pointer maintained by hardware** In byte alignment.

110004B8	AP_DMA_UART_1_TX_INT_BUF_SIZE	UART1 TX Internal Buffer Size Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

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Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TX_INT_BUF_SIZE	**Virtual FIFO DMA TX internal buffer size** 0: 0 byte 1: 1 byte

110004BC	AP_DMA_UART_1_TX_VFF_VALID_SIZE	UART1 TX Virtual FIFO Valid Size Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_VALID_SIZE	**TX virtual FIFO valid size** 0: 0 byte 1: 1 byte

110004C0	AP_DMA_UART_1_TX_VFF_LEFT_SIZE	UART1 TX Virtual FIFO Left Size Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_LEFT_SIZE	**TX virtual FIFO left size** 0: 0 byte 1: 1 byte

110004D0	AP_DMA_UART_1_TX_	UART1 TX Debug Status 00	00000000

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DEBUG_STATUS_00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D					FLUSH_ACT	FLUSH_STR	WD_ACT	RD_ACT	WREQ	RREQ	W_Q_CLR	R_Q_CLR
Type				RO					RO	RO	RO	RO	RO	RO	RO	RO
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
6	FLUSH_STR	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	
1	W_Q_CLR	
0	R_Q_CLR	

110004D4	**AP_DMA_UART_1_TX_VFF_WPT_REAL**	**UART1 TX Virtual FIFO Write Pointer Register Value**	**00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_REAL
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_REAL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_REAL	**TX VFF write pointer wrap bit** If HW_FLUSH=1, sync to TX_VFF_WPT_WRAP_VALID. If HW_FLUSH=0, sync to TX_VFF_WPT_WRAP.
15:0	TX_VFF_WPT_REAL	**TX VFF write pointer** If HW_FLUSH=1, sync to TX_VFF_WPT_VALID. If HW_FLUSH=0, sync to TX_VFF_WPT.

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110004D8	AP_DMA_UART_1_TX_VFF_WPT_VALID	UART1 TX Virtual FIFO Write Pointer Register by HW Control	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_VALID
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_VALID	**TX VFF write pointer wrap bit** If FLUSH= 0, sync to TX_VFF_WPT_WRAP. If flush, it will not update the value until the flush is finished.
15:0	TX_VFF_WPT_VALID	**TX VFF write pointer** If FLUSH= 0, sync to TX_VFF_WPT. If flush, it will not update the value until the flush is finished.

110004E0	AP_DMA_UART_1_TX_FLUSH_ACT	UART1 TX Virtual FIFO Flush Status Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLUSH_NEXT	FLUSH_ACT
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	FLUSH_NEXT	There is a flush command when the UART1 TX channel is flushing.
0	FLUSH_ACT	UART1 TX channel flush status

110004E4	AP_DMA_UART_1_TX_HW_FLUSH	UART1 TX Virtual FIFO HW Flush Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

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Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																HW_FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	HW_FLUSH	**Flush control bit** Controls the UART TX write pointer if the SW setting value at flushing is updated. 0: Update WPT with SW setting 1: Update WPT when flush =0

11000500	AP_DMA_UART_1_RX_INT_FLAG	UART1 RX Virtual FIFO Interrupt Flag Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLAG1	FLAG0
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	FLAG1	**Write 1 to clear it.** This flag is raised when UART issues flush to DMA and all data in UART FIFO are transferred to VFF.
0	FLAG0	**Write 1 to clear it.** This flag is raised when RX_VFF_VALID_SIZE >= RX_VFF_THRE. (VFF is almost full and MCU needs to consume those data.)

11000504	AP_DMA_UART_1_RX_INT_EN	UART1 RX Virtual FIFO Interrupt Enable Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INTEN1	INTEN0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
1	INTEN1	**Controls interrupt enable** Only when this bit is set to 1 will flag1 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag1 will still be set to 1 regardless of this bit. 0: Disable 1: Enable
0	INTEN0	**Controls interrupt enable** Only when this bit is set to 1 will flag0 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag0 will still be set to 1 regardless of this bit. 0: Disable 1: Enable

11000508 AP_DMA_UART_1_RX_EN UART1 RX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART1 RX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

1100050C AP_DMA_UART_1_RX_RST UART1 RX Virtual FIFO Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable

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Bit(s)	Name	Description
		1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000510 **AP_DMA_UART_1_RX_STOP** **UART1 RX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																A0
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART1 RX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

11000514 **AP_DMA_UART_1_RX_FLUSH** **UART1 RX Virtual FIFO Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART1 RX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Flush finished 1: Enable

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1100051C	AP_DMA_UART_1_RX_VFF_ADDR	UART1 RX Virtual FIFO Base Address Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_VFF_ADDR[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_ADDR[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	RX_VFF_ADDR	**UART1 memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

11000524	AP_DMA_UART_1_RX_VFF_LEN	UART1 RX Virtual FIFO Length Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	RX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

11000528	AP_DMA_UART_1_RX_VFF_THRE	UART1 RX Virtual FIFO Threshold Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	RX_VFF_THRE	**VFF threshold in byte alignment** In RX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In TX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

1100052C **AP_DMA_UART_1_RX_VFF_WPT** **UART1 RX Virtual FIFO Write Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_WPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_WPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_WPT_WRAP	**RX VFF write pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_WPT	**RX VFF write pointer maintained by hardware** In byte alignment.

11000530 **AP_DMA_UART_1_RX_VFF_RPT** **UART1 RX Virtual FIFO Read Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_RPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_RPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_RPT_WRAP	**RX VFF read pointer wrap bit maintained by software** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_RPT	**RX VFF read pointer maintained by software** In byte alignment.

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11000534 **AP_DMA_UART_1_RX_FLOW_CTRL_THRE** **UART1 RX Virtual FIFO Flow Control Threshold** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_FLOW_CTRL_THRE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RX_FLOW_CTRL_THRE	**VFF flow control threshold in byte alignment** In RX mode, DMA issues flow control when left size in VFF is smaller than the threshold.

11000538 **AP_DMA_UART_1_RX_INT_BUF_SIZE** **UART1 Rx Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RX_INT_BUF_SIZE	**Virtual FIFO DMA RX internal buffer size** 0: 0 byte 1: 1 byte

1100053C **AP_DMA_UART_1_RX_VFF_VALID_SIZE** **UART1 Rx Virtual FIFO Valid Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
15:0	RX_VFF_VALID_SIZE	**RX virtual FIFO valid size** 0: 0 byte 1: 1 byte

11000540	AP_DMA_UART_1_RX_VFF_LEFT_SIZE	UART1 RX Virtual FIFO Left Size Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_LEFT_SIZE	**RX virtual FIFO left size** 0: 0 byte 1: 1 byte

11000550	AP_DMA_UART_1_RX_DEBUG_STATUS_00	UART1 RX Debug Status 00	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				WADDR_D					FLUSH_ACT		WD_ACT	RD_ACT	WREQ	RREQ		
Type				RO					RO		RO	RO	RO	RO		
Reset				0	0	0	0	0	0		0	0	0	0		

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	

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11000580	AP_DMA_UART_2_TX_INT_FLAG	UART2 TX Virtual FIFO Interrupt Flag Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG0
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG0	**Write 0 to clear it.** Interrupt will be issued to HW when FLAG=1. Mechanism: 1. SW puts data into VFF and detects TX_VFF_LEFT_SIZE is approaching 0. 2. SW sets INTEN=1 and leaves the task to wait for interrupt. 3. When HW delivers enough data to UART and makes TX_VFF_LEFT_SIZE >= TX_VFF_THRS, HW sets the flag to 1 and issues interrupt. 4. When SW receives this interrupt, it must set FLAG back to 0 and go on pushing data into VFF.

11000584	AP_DMA_UART_2_TX_INT_EN	UART2 TX Virtual FIFO Interrupt Enable Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INTEN
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	**Controls interrupt enable** This bit is used to control if the flag will be set to 1 when TX_VFF_LEFT_SIZE >= TX_VFF_THRS. 0: Does not set flag to 1, even tx_vff_left_size >= tx_vff_thrs 1: Set flag to 1 and HW auto sets inten back to 0 when tx_vff_left_size >= tx_vff_thrs.

11000588	AP_DMA_UART_2_TX_EN	UART2 TX Virtual FIFO Enable Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name																EN
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART2 TX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When EN = 0 and MCU writes data to the VFF_W port (an AHB slave port), VFF_W will ignore this command, and the data will not be written to virtual FIFO. 0: Disable 1: Enable

1100058C <u>AP_DMA_UART_2_TX_RST</u> UART2 TX Virtual FIFO Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RSTt to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000590 <u>AP_DMA_UART_2_TX_STOP</u> UART2 TX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																A0
Reset																0

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Bit(s)	Name	Description
0	STOP	**Stops UART2 TX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000594 **AP_DMA_UART_2_TX_FLUSH** **UART2 TX Virtual FIFO Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART2 TX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1100059C **AP_DMA_UART_2_TX_VFF_ADDR** **UART2 TX Virtual FIFO Base Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_VFF_ADDR[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_ADDR[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	TX_VFF_ADDR	**UART2 memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

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110005A4	**AP_DMA_UART_2_TX_VFF_LEN**	**UART2 TX Virtual FIFO Length Register**	**00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	TX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

110005A8	**AP_DMA_UART_2_TX_VFF_THRE**	**UART2 TX Virtual FIFO Threshold Register**	**00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_THRE	**VFF threshold in byte alignment** In TX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In RX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

110005AC	**AP_DMA_UART_2_TX_VFF_WPT**	**UART2 TX Virtual FIFO Write Pointer Register**	**00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP	**TX VFF write pointer wrap bit** It is initialized to 0. When wrapped to the ring head again, invert this bit. For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.
15:0	TX_VFF_WPT	**Byte alignment FIFO write pointer** For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.

110005B0 **AP_DMA_UART_2_TX_VFF_RPT** **UART2 TX Virtual FIFO Read Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**TX_VFF_RPT_WRAP**
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TX_VFF_RPT**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_RPT_WRAP	**TX VFF read pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	TX_VFF_RPT	**TX VFF read pointer maintained by hardware** In byte alignment.

110005B8 **AP_DMA_UART_2_TX_INT_BUF_SIZE** **UART2 TX Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**TX_INT_BUF_SIZE**				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TX_INT_BUF_SIZE	**Virtual FIFO DMA TX internal buffer size** 0: 0 byte 1: 1 byte

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110005BC **AP_DMA_UART_2_TX_VFF_VALID_SIZE** **UART2 TX Virtual FIFO Valid Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_VALID_SIZE	**TX virtual FIFO valid size** 0: 0 byte 1: 1 byte

110005C0 **AP_DMA_UART_2_TX_VFF_LEFT_SIZE** **UART2 TX Virtual FIFO Left Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_LEFT_SIZE	**TX virtual FIFO left size** 0: 0 byte 1: 1 byte

110005D0 **AP_DMA_UART_2_TX_DEBUG_STATUS_00** **UART2 TX Debug Status 00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D					FLUSH_ACT	FLUSH_STR	WD_ACT	RD_ACT	WREQ	RREQ	W_QCLR	R_QCLR
Type				RO					RO	RO	RO	RO	RO	RO	RO	RO
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
6	FLUSH_STR	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	
1	W_Q_CLR	
0	R_Q_CLR	

110005D4	**AP_DMA_UART_2_TX_VFF_WPT_REAL**	**UART2 TX Virtual FIFO Write Pointer Register Value**	**00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**TX_VFF_WPT_WRAP_REAL**
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TX_VFF_WPT_REAL**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_REAL	**TX VFF write pointer wrap bit** If HW_FLUSH=1, sync to TX_VFF_WPT_WRAP_VALID. If HW_FLUSH=0, sync to TX_VFF_WPT_WRAP.
15:0	TX_VFF_WPT_REAL	**TX VFF write pointer** If HW_FLUSH=1, sync to TX_VFF_WPT_VALID. If HW_FLUSH=0, sync to TX_VFF_WPT.

110005D8	**AP_DMA_UART_2_TX_VFF_WPT_VALID**	**UART2 TX Virtual FIFO Write Pointer Register by HW Control**	**00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**TX_VFF_WPT_WRAP_VALI**

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																D
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TX_VFF_WPT_VALID**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_VALID	**TX VFF write pointer wrap bit** If FLUSH= 0, sync to TX_VFF_WPT_WRAP. If flush, it will not update the value until the flush is finished.
15:0	TX_VFF_WPT_VALID	**TX VFF write pointer** If FLUSH= 0, sync to TX_VFF_WPT. If flush, it will not update the value until the flush is finished.

110005E0 **AP_DMA_UART_2_TX_FLUSH_ACT** **UART2 TX Virtual FIFO Flush Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**FLUSH_NEXT**	**FLUSH_ACT**
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	FLUSH_NEXT	There is a flush command when the UART2 TX channel is flushing.
0	FLUSH_ACT	UART2 TX channel flush status

110005E4 **AP_DMA_UART_2_TX_HW_FLUSH** **UART2 TX Virtual FIFO HW Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**HW_FLUSH**
Type																RW
Reset																0

Bit(s)	Name	Description
0	HW_FLUSH	**Flush control bit** Controls the UART TX write pointer if the SW setting value at flushing is

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Bit(s)	Name	Description
		updated. 0: Update WPT with SW setting 1: Update WPT when flush =0

11000600	AP_DMA_UART_2_RX_INT_FLAG	UART2 RX Virtual FIFO Interrupt Flag Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLAG1	FLAG0
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	FLAG1	**Write 1 to clear it.** This flag is raised when UART issues flush to DMA and all data in UART FIFO are transferred to VFF.
0	FLAG0	**Write 1 to clear it.** This flag is raised when RX_VFF_VALID_SIZE >= RX_VFF_THRE. (VFF is almost full and MCU needs to consume those data.)

11000604	AP_DMA_UART_2_RX_INT_EN	UART2 RX Virtual FIFO Interrupt Enable Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INTEN1	INTEN0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	INTEN1	**Controls interrupt enable** Only when this bit is set to 1 will flag1 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag1 will still be set to 1 regardless of this bit. 0: Disable 1: Enable
0	INTEN0	**Controls interrupt enable** Only when this bit is set to 1 will flag0 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag0 will still be set to 1 regardless of this bit. 0: Disable

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Bit(s)	Name	Description
		1: Enable

11000608 **AP_DMA_UART_2_RX_EN** **UART2 RX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART2 RX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

1100060C **AP_DMA_UART_2_RX_RST** **UART2 RX Virtual FIFO Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000610 **AP_DMA_U** **UART2 RX Virtual FIFO Enable Register** **00000000**

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ART_2_RX_STOP

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**STOP**
Type																A0
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART2 RX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

11000614 **AP_DMA_UART_2_RX_FLUSH** **UART2 RX Virtual FIFO Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**FLUSH**
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART2 RX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Flush finished 1: Enable

1100061C **AP_DMA_UART_2_RX_VFF_ADDR** **UART2 RX Virtual FIFO Base Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_VFF_ADDR[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	RX_VFF_ADDR[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	RX_VFF_ADDR	**UART2 memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

11000624 AP_DMA_UART_2_RX_VFF_LEN UART2 RX Virtual FIFO Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	RX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

11000628 AP_DMA_UART_2_RX_VFF_THRE UART2 RX Virtual FIFO Threshold Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_THRE	**VFF threshold in byte alignment** In RX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In TX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

1100062C AP_DMA_UART_2_RX_VFF_WPT UART2 RX Virtual FIFO Write Pointer Register 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_WPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_WPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_WPT_WRAP	**RX VFF write pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_WPT	**RX VFF write pointer maintained by hardware** In byte alignment.

11000630 **AP_DMA_UART_2_RX_VFF_RPT** **UART2 RX Virtual FIFO Read Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_RPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_RPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_RPT_WRAP	**RX VFF read pointer wrap bit maintained by software** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_RPT	**RX VFF read pointer maintained by software** In byte alignment.

11000634 **AP_DMA_UART_2_RX_FLOW_CTRL_THRE** **UART2 RX Virtual FIFO Flow Control Threshold** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_FLOW_CTRL_THRE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
7:0	RX_FLOW_CTRL_THRE	**VFF flow control threshold in byte alignment** In RX mode, DMA issues flow control when left size in VFF is smaller than the threshold.

11000638	AP_DMA_UART_2_RX_INT_BUF_SIZE	UART2 RX Internal Buffer Size Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RX_INT_BUF_SIZE	**Virtual FIFO DMA RX internal buffer size** 0: 0 byte 1: 1 byte

1100063C	AP_DMA_UART_2_RX_VFF_VALID_SIZE	UART2 RX Virtual FIFO Valid Size Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_VALID_SIZE	**RX virtual FIFO valid size** 0: 0 byte 1: 1 byte

11000640	AP_DMA_UART_2_RX_VFF_LEFT_SIZE	UART2 RX Virtual FIFO Left Size Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

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Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_LEFT_SIZE	**RX virtual FIFO left size** 0: 0 byte 1: 1 byte

11000650 AP_DMA_UART_2_RX_DEBUG_STATUS_00 UART2 RX Debug Status 00 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D					FLUSH_ACT		WD_ACT	RD_ACT	WREQ	RREQ		
Type				RO					RO		RO	RO	RO	RO		
Reset				0	0	0	0	0	0		0	0	0	0		

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	

11000680 AP_DMA_UART_3_TX_INT_FLAG UART3 TX Virtual FIFO Interrupt Flag Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG
Type																RW
Reset																0

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Bit(s)	Name	Description
0	FLAG0	**Write 0 to clear it.** Interrupt will be issued to HW when FLAG=1. Mechanism: 1. SW puts data into VFF and detects TX_VFF_LEFT_SIZE is approaching 0. 2. SW sets INTEN=1 and leaves the task to wait for interrupt. 3. When HW delivers enough data to UART and makes TX_VFF_LEFT_SIZE >= TX_VFF_THRS, HW sets the flag to 1 and issues interrupt. 4. When SW receives this interrupt, it must set FLAG back to 0 and go on pushing data into VFF.

11000684 **AP_DMA_UART_3_TX_INT_EN** **UART3 TX Virtual FIFO Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**INTEN**
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	**Controls interrupt enable** This bit is used to control if the flag will be set to 1 when TX_VFF_LEFT_SIZE >= TX_VFF_THRS. 0: Does not set flag to 1, even tx_vff_left_size >= tx_vff_thrs 1: Set flag to 1 and HW auto sets inten back to 0 when tx_vff_left_size >= tx_vff_thrs.

11000688 **AP_DMA_UART_3_TX_EN** **UART3 TX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**EN**
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART3 TX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When EN = 0 and MCU writes data to the VFF_W port (an AHB slave port), VFF_W will ignore this command, and the data will not be written to virtual FIFO. 0: Disable

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Bit(s)	Name	Description
		1: Enable

1100068C **AP_DMA_UART_3_TX_RST** **UART3 TX Virtual FIFO Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RSTt to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000690 **AP_DMA_UART_3_TX_STOP** **UART3 TX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																A0
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART3 TX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

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11000694 AP_DMA_UART_3_TX_FLUSH UART3 TX Virtual FIFO Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART3 TX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Flush finished 1: Enable

1100069C AP_DMA_UART_3_TX_VFF_ADDR UART3 TX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_VFF_ADDR[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_ADDR[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	TX_VFF_ADDR	**UART3 memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

110006A4 AP_DMA_UART_3_TX_VFF_LEN UART3 TX Virtual FIFO Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEN															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	TX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

110006A8 **AP_DMA_UART_3_TX_VFF_THRE** **UART3 TX Virtual FIFO Threshold Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TX_VFF_THRE**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_THRE	**VFF threshold in byte alignment** In TX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In RX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

110006AC **AP_DMA_UART_3_TX_VFF_WPT** **UART3 TX Virtual FIFO Write Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**TX_VFF_WPT_WRAP**
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TX_VFF_WPT**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP	**TX VFF write pointer wrap bit** It is initialized to 0. When wrapped to the ring head again, invert this bit. For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.
15:0	TX_VFF_WPT	**Byte alignment FIFO write pointer** For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.

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110006B0	AP_DMA_UART_3_TX_VFF_RPT	UART3 TX Virtual FIFO Read Pointer Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_RPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_RPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_RPT_WRAP	**TX VFF read pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	TX_VFF_RPT	**TX VFF read pointer maintained by hardware** In byte alignment.

110006B8	AP_DMA_UART_3_TX_INT_BUF_SIZE	UART3 TX Internal Buffer Size Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TX_INT_BUF_SIZE	**Virtual FIFO DMA TX internal buffer size** 0: 0 byte 1: 1 byte

110006BC	AP_DMA_UART_3_TX_VFF_VALID_SIZE	UART3 TX Virtual FIFO Valid Size Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_VALID_SIZE															

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Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_VALID_SIZE	**TX virtual FIFO valid size** 0: 0 byte 1: 1 byte

110006C0	AP_DMA_UART_3_TX_VFF_LEFT_SIZE	UART3 TX Virtual FIFO Left Size Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_LEFT_SIZE	**TX virtual FIFO left size** 0: 0 byte 1: 1 byte

110006D0	AP_DMA_UART_3_TX_DEBUG_STATUS_00	UART3 TX Debug Status 00	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D					FLUSH_ACT	FLUSH_STR	WD_ACT	RD_ACT	WREQ	RREQ	W_Q_CLR	R_Q_CLR
Type				RO					RO	RO	RO	RO	RO	RO	RO	RO
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
6	FLUSH_STR	
5	WD_ACT	
4	RD_ACT	
3	WREQ	

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Bit(s)	Name	Description
2	RREQ	
1	W_Q_CLR	
0	R_Q_CLR	

110006D4	AP_DMA_UART_3_TX_VFF_WPT_REAL	UART3 TX Virtual FIFO Write Pointer Register Value	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_REAL
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_REAL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_REAL	**TX VFF write pointer wrap bit** If HW_FLUSH=1, sync to TX_VFF_WPT_WRAP_VALID. If HW_FLUSH=0, sync to TX_VFF_WPT_WRAP.
15:0	TX_VFF_WPT_REAL	**TX VFF write pointer** If HW_FLUSH=1, sync to TX_VFF_WPT_VALID. If HW_FLUSH=0, sync to TX_VFF_WPT.

110006D8	AP_DMA_UART_3_TX_VFF_WPT_VALID	UART3 TX Virtual FIFO Write Pointer Register by HW Control	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_VALID
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WR	**TX VFF write pointer wrap bit**

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Bit(s)	Name	Description
	AP_VALID	If FLUSH= 0, sync to TX_VFF_WPT_WRAP. If flush, it will not update the value until the flush is finished.
15:0	TX_VFF_WPT_VALID	**TX VFF write pointer** If FLUSH= 0, sync to TX_VFF_WPT. If flush, it will not update the value until the flush is finished.

110006E0 **AP_DMA_UART_3_TX_FLUSH_ACT** **UART3 TX Virtual FIFO Flush Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLUSH_NEXT	FLUSH_ACT
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	FLUSH_NEXT	There is a flush command when the UART3 TX channel is flushing.
0	FLUSH_ACT	UART3 TX channel flush status

110006E4 **AP_DMA_UART_3_TX_HW_FLUSH** **UART3 TX Virtual FIFO HW Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																HW_FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	HW_FLUSH	**Flush control bit** Controls the UART TX write pointer if the SW setting value at flushing is updated. 0: Update WPT with SW setting 1: Update WPT when flush =0

11000700 **AP_DMA_UART_3_RX_** **UART3 RX Virtual FIFO Interrupt Flag Register** **00000000**

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INT_FLAG

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLAG1	FLAG0
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	FLAG1	**Write 1 to clear it.** This flag is raised when UART issues flush to DMA and all data in UART FIFO are transferred to VFF.
0	FLAG0	**Write 1 to clear it.** This flag is raised when RX_VFF_VALID_SIZE >= RX_VFF_THRE. (VFF is almost full and MCU needs to consume those data.)

11000704 **AP_DMA_UART_3_RX_INT_EN** **UART3 RX Virtual FIFO Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INTEN1	INTEN0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	INTEN1	**Controls interrupt enable** Only when this bit is set to 1 will flag1 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag1 will still be set to 1 regardless of this bit. 0: Disable 1: Enable
0	INTEN0	**Controls interrupt enable** Only when this bit is set to 1 will flag0 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag0 will still be set to 1 regardless of this bit. 0: Disable 1: Enable

11000708 **AP_DMA_UART_3_RX_EN** **UART3 RX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

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Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**EN**
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART3 RX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

1100070C **AP_DMA_UART_3_RX_RST** **UART3 RX Virtual FIFO Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**HARD_RST**	**WARM_RST**
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000710 **AP_DMA_UART_3_RX_STOP** **UART3 RX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**STOP**
Type																A0
Reset																0

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Bit(s)	Name	Description
0	STOP	**Stops UART3 RX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

11000714 AP_DMA_UART_3_RX_FLUSH UART3 RX Virtual FIFO Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART3 RX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Flush finished 1: Enable

1100071C AP_DMA_UART_3_RX_VFF_ADDR UART3 RX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_VFF_ADDR[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RX_VFF_ADDR[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	RX_VFF_ADDR	**UART3 memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

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11000724 **AP_DMA_UART_3_RX_VFF_LEN** **UART3 RX Virtual FIFO Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	RX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

11000728 **AP_DMA_UART_3_RX_VFF_THRE** **UART3 RX Virtual FIFO Threshold Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_THRE	**VFF threshold in byte alignment** In RX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In TX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

1100072C **AP_DMA_UART_3_RX_VFF_WPT** **UART3 RX Virtual FIFO Write Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_WPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_WPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
16	RX_VFF_WPT_WRAP	**RX VFF write pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_WPT	**RX VFF write pointer maintained by hardware** In byte alignment.

11000730 AP_DMA_UART_3_RX_VFF_RPT UART3 RX Virtual FIFO Read Pointer Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_RPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_RPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_RPT_WRAP	**RX VFF read pointer wrap bit maintained by software** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_RPT	**RX VFF read pointer maintained by software** In byte alignment.

11000734 AP_DMA_UART_3_RX_FLOW_CTRL_THRE UART3 RX Virtual FIFO Flow Control Threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_FLOW_CTRL_THRE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RX_FLOW_CTRL_THRE	**VFF flow control threshold in byte alignment** In RX mode, DMA issues flow control when left size in VFF is smaller than the threshold.

11000738 AP_DMA_UART_3_RX_INT_BUF_SI UART3 RX Internal Buffer Size Register 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RX_INT_BUF_SIZE	**Virtual FIFO DMA RX internal buffer size** 0: 0 byte 1: 1 byte

1100073C	**AP_DMA_UART_3_RX_VFF_VALID_SIZE**	**UART3 RX Virtual FIFO Valid Size Register**	**00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_VALID_SIZE	**RX virtual FIFO valid size** 0: 0 byte 1: 1 byte

11000740	**AP_DMA_UART_3_RX_VFF_LEFT_SIZE**	**UART3 RX Virtual FIFO Left Size Register**	**00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_LEFT_SIZE	**RX virtual FIFO left size** 0: 0 byte 1: 1 byte

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11000750 **AP_DMA_UART_3_RX_DEBUG_STATUS_00** **UART3 RX Debug Status 00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D					FLUSH_ACT		WD_ACT	RD_ACT	WREQ	RREQ		
Type				RO					RO		RO	RO	RO	RO		
Reset				0	0	0	0	0	0		0	0	0	0		

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	

11000780 **AP_DMA_UART_4_TX_INT_FLAG** **UART4 TX Virtual FIFO Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG0
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG0	**Write 0 to clear it.** Interrupt will be issued to HW when FLAG=1. Mechanism: 1. SW puts data into VFF and detects TX_VFF_LEFT_SIZE is approaching 0. 2. SW sets INTEN=1 and leaves the task to wait for interrupt. 3. When HW delivers enough data to UART and makes TX_VFF_LEFT_SIZE >= TX_VFF_THRS, HW sets the flag to 1 and issues interrupt. 4. When SW receives this interrupt, it must set FLAG back to 0 and go on pushing data into VFF.

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11000784	AP_DMA_UART_4_TX_INT_EN	UART4 TX Virtual FIFO Interrupt Enable Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INTEN
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	**Controls interrupt enable** This bit is used to control if the flag will be set to 1 when TX_VFF_LEFT_SIZE >= TX_VFF_THRS. 0: Does not set flag to 1, even tx_vff_left_size >= tx_vff_thrs 1: Set flag to 1 and HW auto sets inten back to 0 when tx_vff_left_size >= tx_vff_thrs.

11000788	AP_DMA_UART_4_TX_EN	UART4 TX Virtual FIFO Enable Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART4 TX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When EN = 0 and MCU writes data to the VFF_W port (an AHB slave port), VFF_W will ignore this command, and the data will not be written to virtual FIFO. 0: Disable 1: Enable

1100078C	AP_DMA_UART_4_TX_RST	UART4 TX Virtual FIFO Reset Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RSTt to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000790 AP_DMA_UART_4_TX_STOP UART4 TX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																A0
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART4 TX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000794 AP_DMA_UART_4_TX_FLUSH UART4 TX Virtual FIFO Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

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Bit(s)	Name	Description
0	FLUSH	**Flushes UART4 TX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Flush finished 1: Enable

1100079C AP_DMA_UART_4_TX_VFF_ADDR UART4 TX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_VFF_ADDR[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_ADDR[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	TX_VFF_ADDR	**UART4 memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

110007A4 AP_DMA_UART_4_TX_VFF_LEN UART4 TX Virtual FIFO Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	TX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

110007A8 AP_DMA_UART_4_TX_ UART4 TX Virtual FIFO Threshold Register 00000000

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VFF_THRE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_THRE	**VFF threshold in byte alignment** In TX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In RX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

110007AC **AP_DMA_UART_4_TX_VFF_WPT** **UART4 TX Virtual FIFO Write Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP	**TX VFF write pointer wrap bit** It is initialized to 0. When wrapped to the ring head again, invert this bit. For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.
15:0	TX_VFF_WPT	**Byte alignment FIFO write pointer** For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.

110007B0 **AP_DMA_UART_4_TX_VFF_RPT** **UART4 TX Virtual FIFO Read Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_RPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_RPT															

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Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_RPT_WRAP	**TX VFF read pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	TX_VFF_RPT	**TX VFF read pointer maintained by hardware** In byte alignment.

110007B8 **AP_DMA_UART_4_TX_INT_BUF_SIZE** **UART4 TX Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TX_INT_BUF_SIZE	**Virtual FIFO DMA TX internal buffer size** 0: 0 byte 1: 1 byte

110007BC **AP_DMA_UART_4_TX_VFF_VALID_SIZE** **UART4 TX Virtual FIFO Valid Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_VALID_SIZE	**TX virtual FIFO valid size** 0: 0 byte 1: 1 byte

110007C0 **AP_DMA_UART_4_TX_VFF_LEFT_** **UART4 TX Virtual FIFO Left Size Register** **00000000**

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SIZE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_LEFT_SIZE	**TX virtual FIFO left size** 0: 0 byte 1: 1 byte

110007D0	**AP_DMA_UART_4_TX_DEBUG_STATUS_00**	**UART4 TX Debug Status 00**	**00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D					FLUSH_ACT	FLUSH_STR	WD_ACT	RD_ACT	WREQ	RREQ	W_Q_CLR	R_Q_CLR
Type				RO					RO	RO	RO	RO	RO	RO	RO	RO
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
6	FLUSH_STR	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	
1	W_Q_CLR	
0	R_Q_CLR	

110007D4	**AP_DMA_UART_4_TX_VFF_WPT_REAL**	**UART4 TX Virtual FIFO Write Pointer Register Value**	**00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_

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																VFF_WPT_WRAP_REAL
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_REAL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_REAL	**TX VFF write pointer wrap bit** If HW_FLUSH=1, sync to TX_VFF_WPT_WRAP_VALID. If HW_FLUSH=0, sync to TX_VFF_WPT_WRAP.
15:0	TX_VFF_WPT_REAL	**TX VFF write pointer** If HW_FLUSH=1, sync to TX_VFF_WPT_VALID. If HW_FLUSH=0, sync to TX_VFF_WPT.

110007D8 AP_DMA_UART_4_TX_VFF_WPT_VALID — UART4 TX Virtual FIFO Write Pointer Register by HW Control — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_VALID
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_VALID	**TX VFF write pointer wrap bit** If FLUSH= 0, sync to TX_VFF_WPT_WRAP. If flush, it will not update the value until the flush is finished.
15:0	TX_VFF_WPT_VALID	**TX VFF write pointer** If FLUSH= 0, sync to TX_VFF_WPT. If flush, it will not update the value until the flush is finished.

110007E0 AP_DMA_UART_4_TX_FLUSH_ACT — UART4 TX Virtual FIFO Flush Status Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

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Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**FLUSH_NEXT**	**FLUSH_ACT**
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	FLUSH_NEXT	There is a flush command when the UART4 TX channel is flushing.
0	FLUSH_ACT	UART4 TX channel flush status

110007E4 AP_DMA_UART_4_TX_HW_FLUSH UART4 TX Virtual FIFO HW Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**HW_FLUSH**
Type																RW
Reset																0

Bit(s)	Name	Description
0	HW_FLUSH	**Flush control bit** Controls the UART TX write pointer if the SW setting value at flushing is updated. 0: Update WPT with SW setting 1: Update WPT when flush =0

11000800 AP_DMA_UART_4_RX_INT_FLAG UART4 RX Virtual FIFO Interrupt Flag Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**FLAG1**	**FLAG0**
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	FLAG1	**Write 1 to clear it.** This flag is raised when UART issues flush to DMA and all data in UART FIFO are transferred to VFF.

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Bit(s)	Name	Description
0	FLAG0	**Write 1 to clear it.** This flag is raised when RX_VFF_VALID_SIZE >= RX_VFF_THRE. (VFF is almost full and MCU needs to consume those data.)

11000804 **AP_DMA_UART_4_RX_INT_EN** **UART4 RX Virtual FIFO Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INTEN1	INTEN0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	INTEN1	**Controls interrupt enable** Only when this bit is set to 1 will flag1 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag1 will still be set to 1 regardless of this bit. 0: Disable 1: Enable
0	INTEN0	**Controls interrupt enable** Only when this bit is set to 1 will flag0 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag0 will still be set to 1 regardless of this bit. 0: Disable 1: Enable

11000808 **AP_DMA_UART_4_RX_EN** **UART4 RX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART4 RX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

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1100080C **AP_DMA_UART_4_RX_RST** **UART4 RX Virtual FIFO Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000810 **AP_DMA_UART_4_RX_STOP** **UART4 RX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																A0
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART4 RX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

11000814 **AP_DMA_UART_4_RX_** **UART4 RX Virtual FIFO Flush Register** **00000000**

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FLUSH

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART4 RX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Flush finished 1: Enable

1100081C **AP_DMA_UART_4_RX_VFF_ADDR** **UART4 RX Virtual FIFO Base Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_VFF_ADDR[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_ADDR[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	RX_VFF_ADDR	**UART4 memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

11000824 **AP_DMA_UART_4_RX_VFF_LEN** **UART4 RX Virtual FIFO Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

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Bit(s)	Name	Description
15:3	RX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

11000828 **AP_DMA_UART_4_RX_VFF_THRE** **UART4 RX Virtual FIFO Threshold Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_THRE	**VFF threshold in byte alignment** In RX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In TX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

1100082C **AP_DMA_UART_4_RX_VFF_WPT** **UART4 RX Virtual FIFO Write Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_WPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_WPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_WPT_WRAP	**RX VFF write pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_WPT	**RX VFF write pointer maintained by hardware** In byte alignment.

11000830 **AP_DMA_UART_4_RX_VFF_RPT** **UART4 RX Virtual FIFO Read Pointer Register** **00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**RX_VFF_RPT_WRAP**
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RX_VFF_RPT**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_RPT_WRAP	**RX VFF read pointer wrap bit maintained by software** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_RPT	**RX VFF read pointer maintained by software** In byte alignment.

11000834 **AP_DMA_UART_4_RX_FLOW_CTRL_THRE** **UART4 RX Virtual FIFO Flow Control Threshold** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**RX_FLOW_CTRL_THRE**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RX_FLOW_CTRL_THRE	**VFF flow control threshold in byte alignment** In RX mode, DMA issues flow control when left size in VFF is smaller than the threshold.

11000838 **AP_DMA_UART_4_RX_INT_BUF_SIZE** **UART4 RX Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**RX_INT_BUF_SIZE**				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RX_INT_BUF_SIZ	**Virtual FIFO DMA RX internal buffer size**

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Bit(s)	Name	Description
	E	0: 0 byte 1: 1 byte

1100083C	AP_DMA_UART_4_RX_VFF_VALID_SIZE	UART4 RX Virtual FIFO Valid Size Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_VALID_SIZE	**RX virtual FIFO valid size** 0: 0 byte 1: 1 byte

11000840	AP_DMA_UART_4_RX_VFF_LEFT_SIZE	UART4 RX Virtual FIFO Left Size Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_LEFT_SIZE	**RX virtual FIFO left size** 0: 0 byte 1: 1 byte

11000850	AP_DMA_UART_4_RX_DEBUG_STATUS_00	UART4 RX Debug Status 00	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name				**WADDR_D**					**FLUSH_ACT**		**WD_ACT**	**RD_ACT**	**WREQ**	**RREQ**		
Type				RO					RO		RO	RO	RO	RO		
Reset				0	0	0	0	0	0		0	0	0	0		

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	

11000880 **AP_DMA_UART_5_TX_INT_FLAG** **UART5 TX Virtual FIFO Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**FLAG0**
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG0	**Write 0 to clear it.** Interrupt will be issued to HW when FLAG=1. Mechanism: 1. SW puts data into VFF and detects TX_VFF_LEFT_SIZE is approaching 0. 2. SW sets INTEN=1 and leaves the task to wait for interrupt. 3. When HW delivers enough data to UART and makes TX_VFF_LEFT_SIZE >= TX_VFF_THRS, HW sets the flag to 1 and issues interrupt. 4. When SW receives this interrupt, it must set FLAG back to 0 and go on pushing data into VFF.

11000884 **AP_DMA_UART_5_TX_INT_EN** **UART5 TX Virtual FIFO Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**INTEN**
Type																RW
Reset																0

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Bit(s)	Name	Description
0	INTEN	**Controls interrupt enable** This bit is used to control if the flag will be set to 1 when TX_VFF_LEFT_SIZE >= TX_VFF_THRS. 0: Does not set flag to 1, even tx_vff_left_size >= tx_vff_thrs 1: Set flag to 1 and HW auto sets inten back to 0 when tx_vff_left_size >= tx_vff_thrs.

11000888 **AP_DMA_UART_5_TX_EN** **UART5 TX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**EN**
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART5 TX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When EN = 0 and MCU writes data to the VFF_W port (an AHB slave port), VFF_W will ignore this command, and the data will not be written to virtual FIFO. 0: Disable 1: Enable

1100088C **AP_DMA_UART_5_TX_RST** **UART5 TX Virtual FIFO Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**HARD_RST**	**WARM_RST**
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)**

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Bit(s)	Name	Description
		SW sets WARM_RSTt to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000890	AP_DMA_UART_5_TX_STOP	UART5 TX Virtual FIFO Enable Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																A0
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART5 TX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000894	AP_DMA_UART_5_TX_FLUSH	UART5 TX Virtual FIFO Flush Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART5 TX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Flush finished 1: Enable

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1100089C	AP_DMA_UART_5_TX_VFF_ADDR	UART5 TX Virtual FIFO Base Address Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_VFF_ADDR[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_ADDR[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	TX_VFF_ADDR	**UART5 memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

110008A4	AP_DMA_UART_5_TX_VFF_LEN	UART5 TX Virtual FIFO Length Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	TX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

110008A8	AP_DMA_UART_5_TX_VFF_THRE	UART5 TX Virtual FIFO Threshold Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
15:0	TX_VFF_THRE	**VFF threshold in byte alignment** In TX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In RX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

110008AC **AP_DMA_UART_5_TX_VFF_WPT** **UART5 TX Virtual FIFO Write Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP	**TX VFF write pointer wrap bit** It is initialized to 0. When wrapped to the ring head again, invert this bit. For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.
15:0	TX_VFF_WPT	**Byte alignment FIFO write pointer** For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.

110008B0 **AP_DMA_UART_5_TX_VFF_RPT** **UART5 TX Virtual FIFO Read Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_RPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_RPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_RPT_WRAP	**TX VFF read pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	TX_VFF_RPT	**TX VFF read pointer maintained by hardware** In byte alignment.

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110008B8	AP_DMA_UART_5_TX_INT_BUF_SIZE	UART5 TX Internal Buffer Size Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TX_INT_BUF_SIZE	**Virtual FIFO DMA TX internal buffer size** 0: 0 byte 1: 1 byte

110008BC	AP_DMA_UART_5_TX_VFF_VALID_SIZE	UART5 TX Virtual FIFO Valid Size Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_VALID_SIZE	**TX virtual FIFO valid size** 0: 0 byte 1: 1 byte

110008C0	AP_DMA_UART_5_TX_VFF_LEFT_SIZE	UART5 TX Virtual FIFO Left Size Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	TX_VFF_LEFT_SIZE	**TX virtual FIFO left size** 0: 0 byte 1: 1 byte

110008D0	**AP_DMA_UART_5_TX_DEBUG_STATUS_00**	**UART5 TX Debug Status 00**	**00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**RADDR_D**								**WADDR_D_LH**				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**WADDR_D**					**FLUSH_ACT**	**FLUSH_STR**	**WD_ACT**	**RD_ACT**	**WREQ**	**RREQ**	**W_Q_CLR**	**R_Q_CLR**
Type				RO					RO	RO	RO	RO	RO	RO	RO	RO
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
6	FLUSH_STR	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	
1	W_Q_CLR	
0	R_Q_CLR	

110008D4	**AP_DMA_UART_5_TX_VFF_WPT_REAL**	**UART5 TX Virtual FIFO Write Pointer Register Value**	**00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**TX_VFF_WPT_WRAP_REAL**
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TX_VFF_WPT_REAL**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_REAL	**TX VFF write pointer wrap bit** If HW_FLUSH=1, sync to TX_VFF_WPT_WRAP_VALID. If HW_FLUSH=0, sync to TX_VFF_WPT_WRAP.
15:0	TX_VFF_WPT_REAL	**TX VFF write pointer** If HW_FLUSH=1, sync to TX_VFF_WPT_VALID. If HW_FLUSH=0, sync to TX_VFF_WPT.

110008D8 **AP_DMA_UART_5_TX_VFF_WPT_VALID** **UART5 TX Virtual FIFO Write Pointer Register by HW Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_VALID
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_VALID	**TX VFF write pointer wrap bit** If FLUSH= 0, sync to TX_VFF_WPT_WRAP. If flush, it will not update the value until the flush is finished.
15:0	TX_VFF_WPT_VALID	**TX VFF write pointer** If FLUSH= 0, sync to TX_VFF_WPT. If flush, it will not update the value until the flush is finished.

110008E0 **AP_DMA_UART_5_TX_FLUSH_ACT** **UART5 TX Virtual FIFO Flush Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLUSH_NEXT	FLUSH_ACT
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
1	FLUSH_NEXT	There is a flush command when the UART5 TX channel is flushing.
0	FLUSH_ACT	UART5 TX channel flush status

110008E4 **AP_DMA_UART_5_TX_HW_FLUSH** **UART5 TX Virtual FIFO HW Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																HW_FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	HW_FLUSH	**Flush control bit** Controls the UART TX write pointer if the SW setting value at flushing is updated. 0: Update WPT with SW setting 1: Update WPT when flush =0

11000900 **AP_DMA_UART_5_RX_INT_FLAG** **UART5 RX Virtual FIFO Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLAG1	FLAG0
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	FLAG1	**Write 1 to clear it.** This flag is raised when UART issues flush to DMA and all data in UART FIFO are transferred to VFF.
0	FLAG0	**Write 1 to clear it.** This flag is raised when RX_VFF_VALID_SIZE >= RX_VFF_THRE. (VFF is almost full and MCU needs to consume those data.)

11000904 **AP_DMA_UART_5_RX_** **UART5 RX Virtual FIFO Interrupt Enable Register** **00000000**

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INT_EN

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INTEN1	INTEN0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	INTEN1	**Controls interrupt enable** Only when this bit is set to 1 will flag1 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag1 will still be set to 1 regardless of this bit. 0: Disable 1: Enable
0	INTEN0	**Controls interrupt enable** Only when this bit is set to 1 will flag0 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag0 will still be set to 1 regardless of this bit. 0: Disable 1: Enable

11000908 AP_DMA_UART_5_RX_EN UART5 RX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART5 RX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

1100090C AP_DMA_UART_5_RX_RST UART5 RX Virtual FIFO Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000910 **AP_DMA_UART_5_RX_STOP** **UART5 RX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																A0
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART5 RX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

11000914 **AP_DMA_UART_5_RX_FLUSH** **UART5 RX Virtual FIFO Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

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Bit(s)	Name	Description
0	FLUSH	**Flushes UART5 RX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Flush finished 1: Enable

1100091C **AP_DMA_UART_5_RX_VFF_ADDR** **UART5 RX Virtual FIFO Base Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_VFF_ADDR[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_ADDR[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	RX_VFF_ADDR	**UART5 memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

11000924 **AP_DMA_UART_5_RX_VFF_LEN** **UART5 RX Virtual FIFO Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	RX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

11000928 **AP_DMA_UART_5_RX_** **UART5 RX Virtual FIFO Threshold Register** **00000000**

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VFF_THRE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_THRE	**VFF threshold in byte alignment** In RX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In TX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

1100092C **AP_DMA_UART_5_RX_VFF_WPT** **UART5 RX Virtual FIFO Write Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_WPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_WPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_WPT_WRAP	**RX VFF write pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_WPT	**RX VFF write pointer maintained by hardware** In byte alignment.

11000930 **AP_DMA_UART_5_RX_VFF_RPT** **UART5 RX Virtual FIFO Read Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_RPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_RPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
16	RX_VFF_RPT_WRAP	**RX VFF read pointer wrap bit maintained by software** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_RPT	**RX VFF read pointer maintained by software** In byte alignment.

11000934 **AP_DMA_UART_5_RX_FLOW_CTRL_THRE** **UART5 RX Virtual FIFO Flow Control Threshold** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_FLOW_CTRL_THRE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RX_FLOW_CTRL_THRE	**VFF flow control threshold in byte alignment** In RX mode, DMA issues flow control when left size in VFF is smaller than the threshold.

11000938 **AP_DMA_UART_5_RX_INT_BUF_SIZE** **UART5 RX Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RX_INT_BUF_SIZE	**Virtual FIFO DMA RX internal buffer size** 0: 0 byte 1: 1 byte

1100093C **AP_DMA_UART_5_RX_VFF_VALID_SIZE** **UART5 RX Virtual FIFO Valid Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RX_VFF_VALID_SIZE**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_VALID_SIZE	**RX virtual FIFO valid size** 0: 0 byte 1: 1 byte

11000940 **AP_DMA_UART_5_RX_VFF_LEFT_SIZE** UART5 RX Virtual FIFO Left Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RX_VFF_LEFT_SIZE**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_LEFT_SIZE	**RX virtual FIFO left size** 0: 0 byte 1: 1 byte

11000950 **AP_DMA_UART_5_RX_DEBUG_STATUS_00** UART5 RX Debug Status 00 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**RADDR_D**								**WADDR_D_LH**				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**WADDR_D**					**FLUSH_ACT**		**WD_ACT**	**RD_ACT**	**WREQ**	**RREQ**		
Type				RO					RO		RO	RO	RO	RO		
Reset				0	0	0	0	0	0		0	0	0	0		

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	

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Bit(s)	Name	Description
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	

3.8.5 Programming Guide

3.8.5.1 Warm Reset and Hard Reset

Warm reset and hard reset exist in DMA global control and each DMA engine. When warm reset is set, the engine will be reset after the current transaction is finished, and therefore the warm reset will not cause any bus hang. Conversely, when hard reset is set, the engine will be reset immediately, and therefore the bus may go down due to unfinished (and will never finish) transaction.

Mechanism of global warm reset

When the software is to re-start all engines or re-clear all engines in DMA, it can set the global WARM_RST to 1 and wait for (poll) all global running status to be 0. Next, set WARM_RST back to 0 to finish the global warm reset.

Mechanism of global hard reset

When the software is to re-start all engines or re-clear all engines in DMA without waiting for any period of time, it can set the global HARD_RST to 1 then back to 0 to finish the global hard reset. Note that this may break the bus protocol and cause system hang.

3.8.5.2 Pause and Resume

There are pause and resume functions available for general DMA and peripheral DMA. The mechanism is as the following:

1. Start DMA. (Program necessary settings, then set EN = 1.)
2. Pause DMA. (Set PAUSE = 1.)
3. Resume DMA. (Set PAUSE = 0.)
4. Wait for DMA to finish. (EN will become 0, and flag will be set to 1.)

The software can repeat step 2 and 3 many times when DMA is running and monitor the idle bit to see if DMA is stopped. DMA will not pause immediately and will wait for the last transaction to be finished.

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3.9 CQDMA

3.9.1 Introduction

There is always a DMA in a platform. The purpose of DMA is performing data transfer between different slaves. There are several slaves in a platform, and the major one is external memory, e.g. DRAM. There are also internal SRAM and some slave ports for the peripheral to transfer data. For saving software efforts, DMA delivers a virtual FIFO concept to help the software maintain read and write pointer when the software accesses data from a ring buffer. As the bus goes more and more efficient, the old DMA still utilizes the AHB bus protocol and may decrease its performance. Another problem is that when the old DMA meets byte alignment addresses or byte alignment sizes, it will need some software efforts to help solve head and tail non word alignment problems or let DMA to simply issues single-1-byte requests to conquer the byte-alignment problem. This will harm the overall system because the single-1-byte transaction is quite inefficient. The DMA efficiency is now improved by increasing its bus efficiency, including data buffering and overcoming byte alignment problems.

3.9.2 Features

CQDMA has the following DMA engines.

- GDMA engine

3.9.3 Block Diagram

Figure 3-11 is the basic block diagram of CQ_DMA. There is one channel in DMA. The external AXI interface is connected to DRAM to provide external memory access ability. A memory block is used as a buffer which makes the transfer on the AXI bus interface more efficient. An APB interface is used to program registers for both global registers and local registers existing in every individual DMA channel.

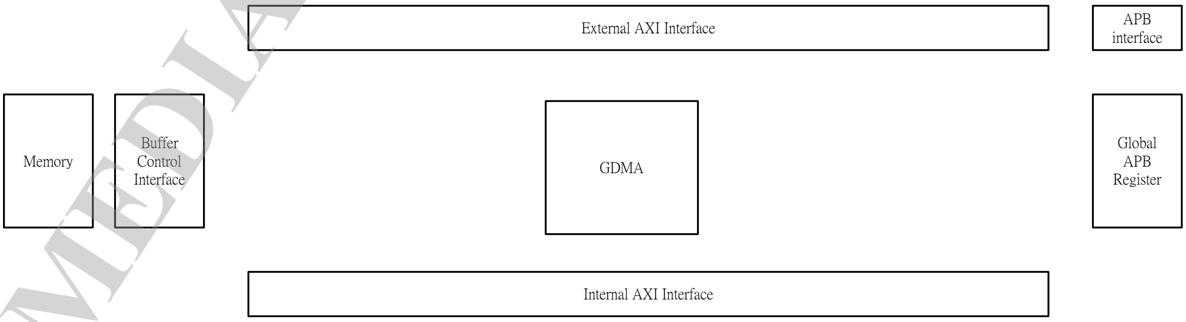

Figure 3-11. APDMA block diagram

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3.9.4 Register Definition

3.9.4.1 Global Control Registers

There are several registers put together for the software to monitor. However, if the software is to change them, they can only be written through individual DMA registers. The global register is only for the software to watch all DMA running statuses and interrupt flags together. Note that the security ability of all global registers belongs to the GSEC_EN bit. When this bit is set to 1, only the security transaction can write the global register (global reset and global slow-down). If a non-security read transaction is issued to read the interrupt flag or running status, only statuses of non-security engines can be reported, and others will always be 0.

See the table below for CQ_DMA engine control registers.

Module name: CQ_DMA Base address: (+10217C00h)

Address	Name	Width	Register Function
10217C00	CQ_DMA_G_DMA_INT_FLAG	32	General DMA Interrupt Flag Register
10217C04	CQ_DMA_G_DMA_INT_EN	32	General DMA Interrupt Enable Register
10217C08	CQ_DMA_G_DMA_EN	32	General DMA Enable Register
10217C0C	CQ_DMA_G_DMA_RST	32	General DMA Reset Register
10217C10	CQ_DMA_G_DMA_STOP	32	General DMA Stop Register
10217C14	CQ_DMA_G_DMA_FLUSH	32	General DMA Flush Register
10217C18	CQ_DMA_G_DMA_CON	32	General DMA Control Register
10217C1C	CQ_DMA_G_DMA_SRC_ADDR	32	General DMA Source Address Register
10217C20	CQ_DMA_G_DMA_DST_ADDR	32	General DMA Destination Address Register
10217C24	CQ_DMA_G_DMA_LEN1	32	General DMA Transfer Length 1 Register
10217C28	CQ_DMA_G_DMA_LEN2	32	General DMA Transfer Length 2 Register
10217C2C	CQ_DMA_G_DMA_JUMP_ADDR	32	General DMA Jump Address Register
10217C30	CQ_DMA_G_DMA_INT_BUF_SIZE	32	General DMA Internal Buffer Size Register
10217C34	CQ_DMA_G_DMA_CONNECT	32	General DMA Connect Register
10217C38	CQ_DMA_G_DMA_AXIATTR	32	General DMA AXI Attribute Register
10217C3C	CQ_DMA_G_DMA_APB_LATADDR	32	General DMA Security Latch Address Register
10217C58	CQ_DMA_G_DMA_SEC_EN	32	General DMA Security Enable Register
10217C60	CQ_DMA_G_DMA_ABORT	32	General DMA Security Abort Register

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Address	Name	Width	Register Function
10217C64	CQ_DMA_G_DMA_DCM_EN	32	General DMA HW DCM Enable
10217D00	CQ_DMA_G_DMA_1_INT_FLAG	32	General DMA Interrupt Flag Register
10217D04	CQ_DMA_G_DMA_1_INT_EN	32	General DMA Interrupt Enable Register
10217D08	CQ_DMA_G_DMA_1_EN	32	General DMA Enable Register
10217D0C	CQ_DMA_G_DMA_1_RST	32	General DMA Reset Register
10217D10	CQ_DMA_G_DMA_1_STOP	32	General DMA Stop Register
10217D14	CQ_DMA_G_DMA_1_FLUSH	32	General DMA Flush Register
10217D18	CQ_DMA_G_DMA_1_CON	32	General DMA Control Register
10217D1C	CQ_DMA_G_DMA_1_SRC_ADDR	32	General DMA Source Address Register
10217D20	CQ_DMA_G_DMA_1_DST_ADDR	32	General DMA Destination Address Register
10217D24	CQ_DMA_G_DMA_1_LEN1	32	General DMA Transfer Length 1 Register
10217D28	CQ_DMA_G_DMA_1_LEN2	32	General DMA Transfer Length 2 Register
10217D2C	CQ_DMA_G_DMA_1_JUMP_ADDR	32	General DMA Jump Address Register
10217D30	CQ_DMA_G_DMA_1_INT_BUF_SIZE	32	General DMA Internal Buffer Size Register
10217D34	CQ_DMA_G_DMA_1_CONNECT	32	General DMA Connect Register
10217D38	CQ_DMA_G_DMA_1_AXIATTR	32	General DMA AXI Attribute Register
10217D3C	CQ_DMA_G_DMA_1_APB_LATADDR	32	General DMA Security Latch Address Register
10217D58	CQ_DMA_G_DMA_1_SEC_EN	32	General DMA Security Enable Register
10217D60	CQ_DMA_G_DMA_1_ABORT	32	General DMA Security Abort Register
10217D64	CQ_DMA_G_DMA_1_DCM_EN	32	General DMA HW DCM Enable

10217C00 CQ_DMA_G_DMA_INT_FLAG General DMA Interrupt Flag Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name																FLAG
Type																RW
Reset																0

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Bit(s)	Name	Description
0	FLAG	**This flag will be raised when DMA is finished.** Write 0 to clear it. 1. When normal operation is done, EN will be set from 1 to 0, and the interrupt flag will be set to 1. 2. Set STOP=1 and operation will be done, then EN will be set from 1 to 0, and the interrupt flag will be set to 1. 3. Set FLUSH=1 and operation will be done, then EN will be set from 1 to 0, and the interrupt flag will be set to 1. 4. Set WARM_RST=1 and operation will be done, then EN will be set from 1 to 0, but the interrupt flag will not be set to 1. 5. Set HARD_RST=1 and operation will be done, then EN will be set from 1 to 0, but the interrupt flag will not be set to 1.

10217C04 CQ_DMA_G_DMA_INT_EN General DMA Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INTEN
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	**Controls interrupt enable** Only when this bit is set to 1 will the interrupt be sent to CPU to receive this interrupt. However, even without this bit set to 1, the flag can still be set to 1 when DMA is finished. 0: Disable, 1: Enable

10217C08 CQ_DMA_G_DMA_EN General DMA Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables general DMA** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset.

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Bit(s)	Name	Description
		0: Disable, 1: Enable.

10217C0C **CQ_DMA_G_DMA_RST** **General DMA Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**General DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**General DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to be 0, and HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

10217C10 **CQ_DMA_G_DMA_STOP** **General DMA Stop Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE	STOP
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses general DMA** Set PAUSE to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	**Stops general DMA** Set STOP to 1 to stop DMA and wait for EN to become 0 then set STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

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10217C14 **CQ_DMA_G_DMA_FLUSH** **General DMA Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**FLUSH**
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes general DMA** Set FLUSH to 1 to stop DMA and allow DMA to flush its internal buffer residual data to the outer memory. After flush is finished, DMA will set EN to 0 to stop DMA. There may still be data not transferred (len may not be 0 after EN = 0). SW sets FLUSH to 1 and waits for EN to become 0 then set FLUSH back to 0 to finish the flush mechanism. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

10217C18 **CQ_DMA_G_DMA_CON** **General DMA Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			**RSIZE**				**WSIZE**					**WRAP_SEL**		**BURST_LEN**		
Type			RW				RW					RW		RW		
Reset			0	0			0	0				0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**WRAP_EN**	**SLOW_CNT**										**RADDR_FIX_EN**	**WADDR_FIX_EN**	**SLOW_EN**	**FIX_EN**	
Type	RW	RW										RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
29:28	RSIZE	**General DMA read size** Only valid when RADDR_FIX_EN = 1. 0: Transaction size is 1 byte. 1: Transaction size is 2 bytes. 2: Transaction size is 4 bytes. 3: Transaction size is 1 byte.
25:24	WSIZE	**General DMA write size** Only valid when WADDR_FIX_EN = 1. 0: Transaction size is 1 byte. 1: Transaction size is 2 bytes. 2: Transaction size is 4 bytes. 3: Transaction size is 1 byte.
20	WRAP_SEL	**Selects general DMA wrap** 0: Read pointer (source)

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Bit(s)	Name	Description
		1: Write pointer (destination)
18:16	BURST_LEN	**General DMA burst length** Valid value: 0~7. The best case is to set it to 3(4-8). 0: 1-8 1: 2-8 2: 3-8 3: 4-8 4: 5-8 5: 6-8 6: 7-8 7: 7-8
15	WRAP_EN	**Enables general DMA wrap or double buffer** Its priority is higher than RADDR_FIX_EN or WADDR_FIX_EN. If WRAP_EN=1 and WRAP_SEL=1, WADDR_FIX_EN will not function. If WRAP_EN=1 and WRAP_SEL=0, RADDR_FIX_EN will not function. 0: Disable 1: Enable
14:5	SLOW_CNT	**General DMA slow-down counter** Only slows down the read side; the overall throughput will also be reduced. Supports up to 1,023 cycles. 0: 0 cycle 1: 1 cycle ...
4	RADDR_FIX_EN	**General DMA fixed read address** When FIX_EN=1 or "WRAP_EN=1 and WRAP_SEL=0", this bit will not function. When this function is enabled, note the following limits on DMA: 1. src_addr must be 8-byte aligned. 2. The read transaction size depends on RSIZE. 3. The burst length is always single. 4. dst_addr must not be at EMI. 0: means no fix 1: means fix
3	WADDR_FIX_EN	**General DMA fixed write address** When "WRAP_EN=1 and WRAP_SEL=1", this bit will not function. When this function is enabled, note the following limits on DMA: 1. dst_addr must be 8-byte aligned. 2. The write transaction size depends on WSIZE. 3. The burst length is always single. 4. dst_addr must not be at EMI. 0: means no fix 1: means fix
2	SLOW_EN	**Enables general DMA slow-down** 0: Disable 1: Enable
1	FIX_EN	**General DMA repeat inserting fixed pattern** Its priority is higher than RADDR_FIX_EN, i.e. when FIX_EN=1, RADDR_FIX_EN will be ignored. 0: No use fix pattern 1: Use fix pattern

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10217C1C **CQ_DMA_G_DMA_SRC_ADDR** **General DMA Source Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_ADDR[31:16]															

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Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SRC_ADDR[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_ADDR	**General DMA source address** Can be any byte alignment. This address will be changed after each bus transaction. However, when RADDR_FIX_EN = 1, src_addr must be 8-byte aligned. When FIX_EN = 1, SRC_ADDR will be treated as FIX_PATTERN.

10217C20 **CQ_DMA_G_DMA_DST_ADDR** **General DMA Destination Address Register** **00100000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DST_ADDR[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DST_ADDR[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DST_ADDR	**General DMA destination address** Can be any byte alignment. This address will be changed after each bus transaction. However, when WADDR_FIX_EN = 1, dst_addr must be 8-byte aligned.

10217C24 **CQ_DMA_G_DMA_LEN1** **General DMA Transfer Length 1 Register** **000FFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													**LEN1[19:16]**			
Type													RW			
Reset													1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**LEN1[15:0]**															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
19:0	LEN1	**General DMA transfer length** Can be any byte alignment. This number will decrease when data are fetched from the source side. This number also indicates how many data have not been delivered. 0: Zero byte transfer 1: One byte transfer ... When read fix and write wrap is set, LEN1 must be a multiple number of the byte number indicated by RSIZE.

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10217C28 **CQ_DMA_G_DMA_LEN2** **General DMA Transfer Length 2 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													**LEN2[19:16]**			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**LEN2[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	LEN2	**General DMA transfer length** Can be any byte alignment. This number will decrease when data are fetched from the source side. This number also indicates how many data have not been delivered. 0: Zero byte transfer 1: One byte transfer

10217C2C **CQ_DMA_G_DMA_JUMP_ADDR** **General DMA Jump Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**JUMP_ADDR[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**JUMP_ADDR[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	JUMP_ADDR	**General DMA end address** Can be any byte alignment. Only valid when wrap_en = 1.

10217C30 **CQ_DMA_G_DMA_INT_BUF_SIZE** **General DMA Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**INT_BUF_SIZE**							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	General DMA size of data in internal buffer

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10217C34 CQ_DMA_G_DMA_CONNECT General DMA Connect Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RATIO	DIR	CONNECT	
Type													RW	RW	RW	
Reset													0	0	0	0

Bit(s)	Name	Description
3	RATIO	0: 1/2 1: 1/1
2	DIR	0: req/ack connected to write side 1: req/ack connected to read side
1:0	CONNECT	**General DMA request/ack connection** 1, 2 and 3 are only valid when WADDR_FIX_EN = 1 or RADDR_FIX_EN = 1. 0: No connection 1: Connect set1 (req/ack) 2: Connect set2 (req/ack) 3: Connect set3 (req/ack)

10217C38 CQ_DMA_G_DMA_AXIATTR General DMA AXI Attribute Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												WUSER	WCACHE			
Type												RW	RW			
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RUSER	RCACHE			
Type												RW	RW			
Reset												0	0	0	0	0

Bit(s)	Name	Description
20	WUSER	0: Go through non-coherent bus. 1: Go through coherent bus. Set this bit when destination is SYSRAM.
19:16	WCACHE	
4	RUSER	0: Go through non-coherent bus. 1: Go through coherent bus. Set this bit when source is SYSRAM.
3:0	RCACHE	

10217C3C CQ_DMA_G_DMA_APB_LATADDR General DMA Security Latch Address Register 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**LAT_ADDR[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**LAT_ADDR[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LAT_ADDR	When any non-security transaction accesses DMA security zone and when R_VID or W_VID is not 1, DMA will latch the address of this transaction.

10217C58 CQ_DMA_G_DMA_SEC_EN General DMA Security Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**DOMAIN_CFG**		**SEC_EN**
Type														RW		RW
Reset														0	0	0

Bit(s)	Name	Description
2:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

10217C60 CQ_DMA_G_DMA_ABORT General DMA Security Abort Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CLR**		**R_VID**	**W_VID**				**APB_ABORT**								
Type	WO		RO	RO				RO								
Reset	0		0	0				0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31	CLR	**SW writes 1 to CLR to clear R_VID, W_VID, and APB_ABORT to 0.** 0: Keep status 1: Clear status
29	R_VID	
28	W_VID	

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Bit(s)	Name	Description
24	APB_ABORT	

10217C64 CQ_DMA_G_DMA_DCM_EN General DMA HW DCM Enable 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DCM_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	DCM_EN	**Sets up GDMA HW DCM enable** If dcm_en = 0, DMA will not auto gate the clock when DMA is idle.

10217D00 CQ_DMA_G_DMA_1_INT_FLAG General DMA Interrupt Flag Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG	**This flag will be raised when DMA is finished.** Write 0 to clear it. 1. When normal operation is done, EN will be set from 1 to 0, and the interrupt flag will be set to 1. 2. Set STOP=1 and operation will be done, then EN will be set from 1 to 0, and the interrupt flag will be set to 1. 3. Set FLUSH=1 and operation will be done, then EN will be set from 1 to 0, and the interrupt flag will be set to 1. 4. Set WARM_RST=1 and operation will be done, then EN will be set from 1 to 0, but the interrupt flag will not be set to 1. 5. Set HARD_RST=1 and operation will be done, then EN will be set from 1 to 0, but the interrupt flag will not be set to 1.

10217D04 CQ_DMA_G_DMA_1_INT_EN General DMA Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**INTEN**
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	**Controls interrupt enable** Only when this bit is set to 1 will the interrupt be sent to CPU to receive this interrupt. However, even without this bit set to 1, the flag can still be set to 1 when DMA is finished. 0: Disable 1: Enable

10217D08 **CQ_DMA_G_DMA_1_EN** **General DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**EN**
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables general DMA** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

10217D0C **CQ_DMA_G_DMA_1_RST** **General DMA Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**HARD_RST**	**WARM_RST**
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**General DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism.

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Bit(s)	Name	Description
		0: Disable 1: Enable
0	WARM_RST	**General DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to be 0, and HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

10217D10 **CQ_DMA_G_DMA_1_STOP** **General DMA Stop Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE	STOP
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses general DMA** Set PAUSE to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	**Stops general DMA** Set STOP to 1 to stop DMA and wait for EN to become 0 then set STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

10217D14 **CQ_DMA_G_DMA_1_FLUSH** **General DMA Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes general DMA** Set FLUSH to 1 to stop DMA and allow DMA to flush its internal buffer residual data to the outer memory. After flush is finished, DMA will set EN to 0 to stop DMA. There may still be data not transferred (len may not be 0 after EN = 0).

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Bit(s)	Name	Description
		SW sets FLUSH to 1 and waits for EN to become 0 then set FLUSH back to 0 to finish the flush mechanism. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

10217D18 **CQ_DMA_G_DMA_1_CON** **General DMA Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			**RSIZE**				**WSIZE**					**WRAP_SEL**		**BURST_LEN**		
Type			RW				RW					RW		RW		
Reset			0	0			0	0				0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**WRAP_EN**	**SLOW_CNT**										**RADDR_FIX_EN**	**WADDR_FIX_EN**	**SLOW_EN**	**FIX_EN**	
Type	RW	RW										RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
29:28	RSIZE	**General DMA read size** Only valid when RADDR_FIX_EN = 1. 0: Transaction size is 1 byte. 1: Transaction size is 2 bytes. 2: Transaction size is 4 bytes. 3: Transaction size is 1 byte.
25:24	WSIZE	**General DMA write size** Only valid when WADDR_FIX_EN = 1. 0: Transaction size is 1 byte. 1: Transaction size is 2 bytes. 2: Transaction size is 4 bytes. 3: Transaction size is 1 byte.
20	WRAP_SEL	**Selects general DMA wrap** 0: Read pointer (source) 1: Write pointer (destination)
18:16	BURST_LEN	**General DMA burst length** Valid values: 0~7. The best case is set it to 3(4-8). 0: 1-8 1: 2-8 2: 3-8 3: 4-8 4: 5-8 5: 6-8 6: 7-8 7: 7-8
15	WRAP_EN	**Enables general DMA wrap or double buffer** Its priority is higher than RADDR_FIX_EN or WADDR_FIX_EN. If WRAP_EN=1 and WRAP_SEL=1, WADDR_FIX_EN will not function. If WRAP_EN=1 and WRAP_SEL=0, RADDR_FIX_EN will not function. When FIX_EN=1, (if WRAP_EN=1, WRAP_SEL can only be set to 1, and read side cannot be set to wrap 0: Disable 1: Enable

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Bit(s)	Name	Description
14:5	SLOW_CNT	**General DMA slow-down counter** Only slows down the read side; the overall throughput will also be reduced. Supports up to 1,023 cycles. 0: 0 cycle 1: 1 cycle ...
4	RADDR_FIX_EN	**General DMA fixed read address** When FIX_EN=1 or "WRAP_EN=1 and WRAP_SEL=0", this bit will not function. When this function is enabled, note the following limits on DMA: 1. src_addr must be 8-byte aligned. 2. The read transaction size depends on RSIZE. 3. The burst length is always single. 4. dst_addr must not be at EMI. 0: No fix 1: Fix
3	WADDR_FIX_EN	**General DMA fixed write address** When "WRAP_EN=1 and WRAP_SEL=1", this bit will not function. When this function is enabled, note the following limits on DMA: 1. dst_addr must be 8-byte aligned. 2. The write transaction size depends on WSIZE. 3. The burst length is always single. 4. dst_addr must not be at EMI. 0: means no fix 1: means fix
2	SLOW_EN	**Enables general DMA slow-down** 0: Disable 1: Enable
1	FIX_EN	**General DMA repeat inserting fixed pattern** Its priority is higher than RADDR_FIX_EN, i.e. when FIX_EN=1, RADDR_FIX_EN will be ignored. 0: No use fix pattern 1: Use fix pattern

10217D1C **CQ_DMA_G_DMA_1_SRC_ADDR** **General DMA Source Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_ADDR	**General DMA source address** Can be any byte alignment. This address will be changed after each bus transaction. However, when RADDR_FIX_EN = 1, src_addr must be 8-byte aligned. When FIX_EN = 1, SRC_ADDR will be treated as FIX_PATTERN.

10217D20 **CQ_DMA_G_** **General DMA Destination Address Register** **00100000**

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DMA_1_DST_ADDR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DST_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DST_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DST_ADDR	**General DMA destination address** Can be any byte alignment. This address will be changed after each bus transaction. However, when WADDR_FIX_EN = 1, dst_addr must be 8-byte aligned.

10217D24 CQ_DMA_G_DMA_1_LEN1 General DMA Transfer Length 1 Register 000FFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													LEN1[19:16]			
Type													RW			
Reset													1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LEN1[15:0]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
19:0	LEN1	**General DMA transfer length** Can be any byte alignment. This number will decrease when data are fetched from the source side. This number also indicates how many data have not been delivered. 0: Zero byte transfer 1: One byte transfer ... When read fix and write wrap is set, LEN1 must be a multiple number of the byte number indicated by RSIZE.

10217D28 CQ_DMA_G_DMA_1_LEN2 General DMA Transfer Length 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													LEN2[19:16]			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LEN2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	LEN2	**General DMA transfer length**

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Bit(s)	Name	Description
		Can be any byte alignment. This number will decrease when data are fetched from the source side. This number also indicates how many data have not been delivered. 0: Zero byte transfer 1: One byte transfer

10217D2C CQ_DMA_G_DMA_1_JUMP_ADDR General DMA Jump Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	JUMP_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	JUMP_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	JUMP_ADDR	**General DMA end address** Can be any byte alignment. Only valid when wrap_en = 1.

10217D30 CQ_DMA_G_DMA_1_INT_BUF_SIZE General DMA Internal Buffer Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	General DMA size of data in the internal buffer

10217D34 CQ_DMA_G_DMA_1_CONNECT General DMA Connect Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RATIO	DIR	CONNECT	
Type													RW	RW	RW	
Reset													0	0	0	0

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Bit(s)	Name	Description
3	RATIO	**General DMA Request/ack connection ratio** 0: 1/2 1: 1/1
2	DIR	**General DMA Request/ack connection direction** 0: req/ack connected to write side 1: req/ack connected to read side
1:0	CONNECT	**General DMA request/ack connection** 1, 2 and 3 are only valid when WADDR_FIX_EN = 1 or RADDR_FIX_EN = 1. 0: No connection 1: Connect set1 (req/ack) 2: Connect set2 (req/ack) 3: Connect set3 (req/ack)

10217D38 CQ_DMA_G_DMA_1_AXIATTR General DMA AXI Attribute Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												WUSER	WCACHE			
Type												RW	RW			
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RUSER	RCACHE			
Type												RW	RW			
Reset												0	0	0	0	0

Bit(s)	Name	Description
20	WUSER	**General DMA AXI AWUSER signal** 0: Go through non-coherent bus. 1: Go through coherent bus. Set this bit when destination is SYSRAM.
19:16	WCACHE	**General DMA AXI AWCACHE signal**
4	RUSER	**General DMA AXI ARUSER signal** 0: Go through non-coherent bus. 1: Go through coherent bus. Set this bit when source is SYSRAM.
3:0	RCACHE	**General DMA AXI ARCACHE signal**

10217D3C CQ_DMA_G_DMA_1_APB_LATADDR General DMA Security Latch Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LAT_ADDR[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LAT_ADDR[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	LAT_ADDR	When any non-security transaction accesses DMA security zone and when R_VID or W_VID is not 1, DMA will latch the address of this transaction.

10217D58 **CQ_DMA_G_DMA_1_SEC_EN** **General DMA Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name														DOMAIN_CFG		SEC_EN
Type														RW		RW
Reset														0	0	0

Bit(s)	Name	Description
2:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

10217D60 **CQ_DMA_G_DMA_1_ABORT** **General DMA Security Abort Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CLR		R_VID	W_VID				APB_ABORT								
Type	WO		RO	RO				RO								
Reset	0		0	0				0								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name																
Type																
Reset																

Bit(s)	Name	Description
31	CLR	**SW writes 1 to CLR to clear R_VID, W_VID, and APB_ABORT to 0.** 0: Keep status 1: Clear status
29	R_VID	**Read violation**
28	W_VID	**Write violation**
24	APB_ABORT	

10217D64 **CQ_DMA_G_DMA_1_DCM** **General DMA HW DCM Enable** **00000001**

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EN

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DCM_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	DCM_EN	**Sets up GDMA HW DCM enable** If dcm_en = 0, DMA will not auto gate the clock when DMA is idle.

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4 Clock and Power Control

4.1 Top Clock Generator

4.1.1 Introduction

This section introduces the top clock generator (TOPCKGEN) and the clock architecture.

4.1.2 Features

TOPCKGEN is responsible for generating the following clock signals:

- Free clock generation for whole chip
- Infrastructure and peripheral system clock, including the top level AXI fabric clock
- Multimedia system clock
- Pad macro clocks to be synchronized with one of the above system

The module TOPCKGEN provides clock source selection. Each clock has several clock source selection and can be turned off as well. When switching certain clock from frequency A to frequency B, make sure frequency A and B are available.

It comprises glitch-free clock MUX and digital clock divider to generate various clock frequencies.

4.1.3 Block Diagram

4.1.3.1 Clock Architecture

There are clock generators not only in the top level hierarchy but also in every partition/system. Figure 4-1 shows the location of the top level clock generator.

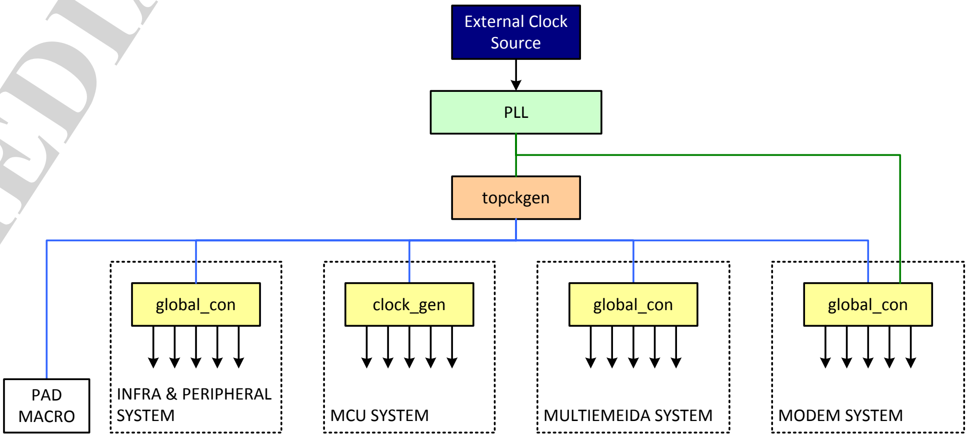

Figure 4-1. Block diagram of clock architecture

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4.1.3.2 Clock Multiplixer

Clock selection and generation have similar structure (see Figure 4-2). Several clock sources are provided. Choose one by specified register setting. The turn-off bit is provided as well to stop the clock output.

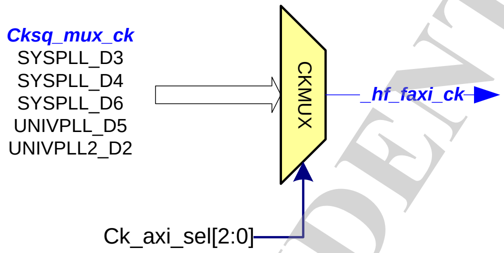

Figure 4-2. Example of clock multiplixer

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4.1.4 Clock PLL

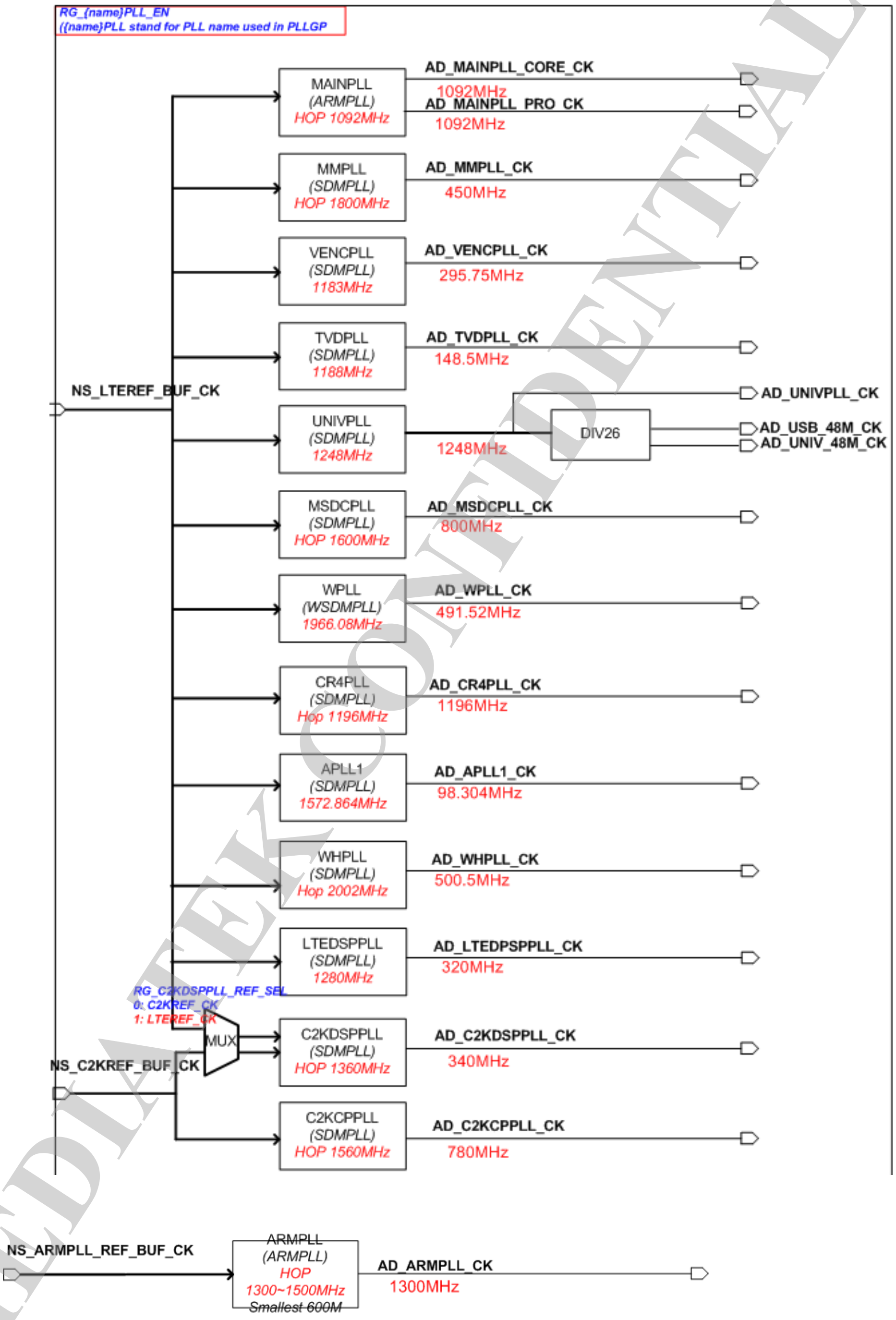

Figure 4-3. PLL block diagram

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4.1.5 PLL Related Control

The following table lists all PLLs inside the application system.

The enabling of PLL can be switched between software control and hardware control. The hardware control is from SCPSYS.

The hopping and SSC features can be switched between software control and hardware control. The hardware control is from FHCTL.

Table 4-1. PLL related control

PLL	Capability	Control by FHCTL	Control by SPM
ARMPLL	Hopping, SSC	Y	Y
MAINPLL	Hopping, SSC	Y	Y
UNIVPLL	Fix	N	Y
MSDCPLL	Hopping, SSC	Y	N
MMPLL	Hopping, SSC	Y	N
TVDPLL	Hopping, SSC	Y	N
VENCPLL	Hopping, SSC	Y	N
MEMPLL	Hopping, SSC	Y	Y
MIPIPLL	SSC	N	N
USB20_PHYA	Fix	N	N
APLL1	Hopping, SSC	N	N
WPLL	Fix	By MD	By MD
WHPLL	Hopping, SSC	By MD	By MD
CR4PLL	Hopping, SSC	By MD	By MD
MDPLL	Fix	By MD	By MD
C2KCPPLL	Hopping, SSC	By MD	By MD
C2KDSPPLL	Hopping, SSC	By MD	By MD
MDPLL2_SUB1 (ABB)	Fix	By MD	By MD
MDPLL2_SUB2 (ABB)	Fix	By MD	By MD
LTEDSPPLL	Hopping, SSC	By MD	By MD

4.1.6 Clock Gating

The clock gating for module TOPCKGEN is listed in the table below where DCM and turn-off settings are provided.

Table 4-2. Clock gating settings

Register name	Bit	Default	Function name	Description
CLK_MODE	8	1'b0	pdn_md_32k	Turns off 32K clock source to MD
DCM_CFG	[7]	1'b0	dcm_enable	Enables hf_faxi_ck DCM

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Register name	Bit	Default	Function name	Description
CLK_SCP_CFG_0	[0]	1'b0	sc_26ck_off_en	Turns on scpsys control path to gate 26MHz
	[1]	1'b0	sc_mem_ck_off_en	Turns on scpsys control path to gate DDRPHY
	[2]	1'b0	sc_axick_off_en	Turns on scpsys control path to gate hf_faxi_ck
	[4]	1'b0	sc_armck_off_en	Turns on scpsys control path to gate CA7 hf_farm_ck
	[5]	1'b0	sc_md_32k_off_en	Turns on scpsys control path to gate MD 32KHz
	[9]	1'b0	sc_mac_26m_off_en	Turns on scpsys control path to gate MIPI 26MHz
	[10]	1'b0	sc_armca15ck_off_en	Turns on scpsys control path to gate CA15 hf_farm_ck
CLK_SCP_CFG_1	[0]	1'b0	sc_axi_26m_sel_en	Turns on scpsys control path to switch hf_faxi_ck to 26MHz
	[4]	1'b0	sc_axick_dcm_dis_en	Turns on scpsys control path to disable DCM of hf_faxi_ck

4.1.7 Frequency Meter

There are two frequency meters inside TOPCKGEN. One is for PLLs and TEST clock, called abist_fmeter. The other is for clocks generated from TOPCKGEN, called ckgen_fmeter.
Both structures have PAD output that can observe frequency directly instead of reading results from the frequency meter. Abist_fmeter is outputted to CLKM[0] and ckgen_fmeter is outputted to DEBUG_MON[2].

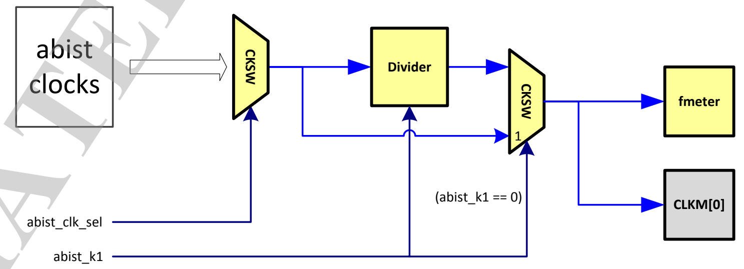

Figure 4-4. ABIST FMETER structure

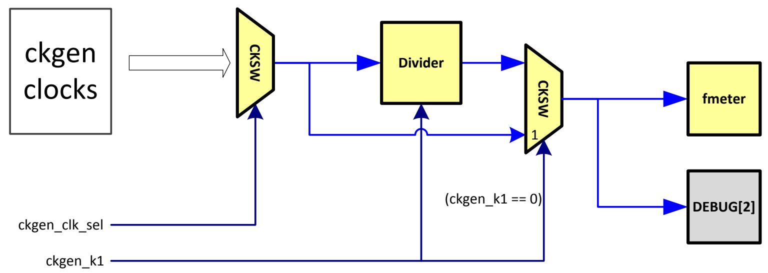

Figure 4-5. CKGEN FMETER structure

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4.1.8 Register Definition

Module name: TOPCKGEN Base address: (+10210000h)

Address	Name	Width	Register Function
10210000	CLK_MODE	32	Clock 26M, 32K PDN Control Register
10210004	DCM_CFG	32	AXI Bus Clock DCM Control Register
10210020	TST_SEL_0	32	Test Clock Selection Register 0
10210024	TST_SEL_1	32	Test Clock Selection Register 1
10210040	CLK_CFG_0	32	Function Clock Selection Register 0
10210044	CLK_CFG_0_SET	32	SET Control of CLK_CFG_0
10210048	CLK_CFG_0_CLR	32	CLR Control of CLK_CFG_0
10210050	CLK_CFG_1	32	Function Clock Selection Register 1
10210054	CLK_CFG_1_SET	32	SET Control of CLK_CFG_1
10210058	CLK_CFG_1_CLR	32	CLR Control of CLK_CFG_1
10210060	CLK_CFG_2	32	Function Clock Selection Register 2
10210064	CLK_CFG_2_SET	32	SET Control of CLK_CFG_2
10210068	CLK_CFG_2_CLR	32	CLR Control of CLK_CFG_2
10210070	CLK_CFG_3	32	Function Clock Selection Register 3
10210074	CLK_CFG_3_SET	32	SET Control of CLK_CFG_3
10210078	CLK_CFG_3_CLR	32	CLR Control of CLK_CFG_3
10210080	CLK_CFG_4	32	Function Clock Selection Register 4
10210084	CLK_CFG_4_SET	32	SET Control of CLK_CFG_4
10210088	CLK_CFG_4_CLR	32	CLR Control of CLK_CFG_4
10210090	CLK_CFG_5	32	Function Clock Selection Register 5
10210094	CLK_CFG_5_SET	32	SET Control of CLK_CFG_5
10210098	CLK_CFG_5_CLR	32	CLR Control of CLK_CFG_5
102100A0	CLK_CFG_6	32	Function Clock Selection Register 6
102100A4	CLK_CFG_6_SET	32	SET Control of CLK_CFG_6
102100A8	CLK_CFG_6_CLR	32	CLR Control of CLK_CFG_6
102100B0	CLK_CFG_7	32	Function Clock Selection Register 7
102100B4	CLK_CFG_7_SET	32	SET Control of CLK_CFG_7
102100B8	CLK_CFG_7_CLR	32	CLR Control of CLK_CFG_7
10210100	CLK_CFG_8	32	Function Clock Selection Register 8
10210104	CLK_CFG_9	32	Function Clock Selection Register 9
10210108	CLK_CFG_10	32	Debug Monitor Clock Selection Register

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Address	Name	Width	Register Function
1021010C	CLK_CFG_11	32	Debug Monitor Divider Control Register
10210200	CLK_SCP_CFG_0	32	SCP Control Register 0
10210204	CLK_SCP_CFG_1	32	SCP Control Register 1
10210210	CLK_MISC_CFG_0	32	MCU Clock Jitter Measurement Control Register
10210214	CLK_MISC_CFG_1	32	Frequency Meter Divider Control Register
10210218	CLK_MISC_CFG_2	32	MEM DCM Idle Signal Force Control
10210220	CLK26CALI_0	32	Frequency Meter Control Register 0
10210224	CLK26CALI_1	32	Frequency Meter Control Register 1
10210228	CLK26CALI_2	32	Frequency Meter Control Register 2
1021022C	CKSTA_REG	32	Function Clock Selection Status Register
10210230	TEST_MODE_CFG	32	Test Mode Control Register
10210308	MBIST_CFG_0	32	Debug Monitor Selection Register 0
1021030C	MBIST_CFG_1	32	Debug Monitor Selection Register 1
10210310	RESET_DEGLITCH_KEY	32	Reset Deglitch Enable Key Register
10210314	MBIST_CFG_3	32	Debug Monitor Selection Register 3

10210000 CLK_MODE Clock 26M, 32K PDN Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					pdn_conn_26m	pdn_conn_32k	pdn_md_26m	pdn_md_32k						pdn_25k	rtc32k_en	topckgen_en
Type					RW	RW	RW	RW						RW	RW	RW
Reset					0	0	0	0						0	0	0

Bit(s)	Name	Description
11	pdn_conn_26m	**Reserved. turn off 26M clock source to CONN. turn off this clock in flight mode** 1: Enable turn off
10	pdn_conn_32k	**Turns off 32K clock source to CONN. Turns off this clock in flight mode** 1: Enable turn off
9	pdn_md_26m	**Reserved. turn off 26M clock source to MD. turn off this clock in flight mode** 1: Enable turn off
8	pdn_md_32k	**Turns off 32K clock source to MD. Turns off this clock in flight mode** 1: Enable turn off
2	pdn_25k	**Turns off 25K clock generator** 0: Enable 1: Disable

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Bit(s)	Name	Description
1	rtc32k_en	**Enable 32K clock from RTC** 0: Disable 1: Enable
0	topckgen_en	**Enables TOPCKGEN** 0: Enable 1: Disable

10210004 DCM_CFG AXI Bus Clock DCM Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	mem_dcm_dbc_enable	mem_dcm_dbc_cnt							mem_dcm_enable	mem_dcm_idle_align	mem_dcm_cfg_latch	mem_dcm_full_fsel				
Type	RW	RW							RW	RW	RW	RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dcm_dbc_enable	dcm_dbc_cnt							dcm_enable			dcm_full_fsel				
Type	RW	RW							RW			RW				
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0

Bit(s)	Name	Description
31	mem_dcm_dbc_enable	**Enables DCM de-bounce counter** 1: Enable DCM de-bounce counter
30:24	mem_dcm_dbc_cnt	**DCM de-bounce counter**
23	mem_dcm_enable	**Enables hf_fmem_ck DCM** 1: Enable DCM
22	mem_dcm_idle_align	**Enables hf_fmem_ck DCM idle align** 1: Enable hf_fmem_ck DCM idle align
21	mem_dcm_cfg_latch	**rising edge trigger mem_dcm config latch** 1: trigger
20:16	mem_dcm_full_fsel	**Selects hf_fmem_ck DCM clock** 1xxxx: hd_fmem_ck = hf_fmem_ck 01xxx: hd_fmem_ck = hf_fmem_ck/2 001xx: hd_fmem_ck = hf_fmem_ck/4 0001x: hd_fmem_ck = hf_fmem_ck/8 00001: hd_fmem_ck = hf_fmem_ck/16 00000: hd_fmem_ck = hf_fmem_ck/32
15	dcm_dbc_enable	**Enables DCM de-bounce counter** 1: Enable DCM de-bounce counter
14:8	dcm_dbc_cnt	**DCM de-bounce counter**
7	dcm_enable	**Enables hf_faxi_ck DCM** 1: Enable DCM
4:0	dcm_full_fsel	**Selects hf_faxi_ck DCM clock** 1xxxx: hd_faxi_ck = hf_faxi_ck 01xxx: hd_faxi_ck = hf_faxi_ck/2 001xx: hd_faxi_ck = hf_faxi_ck/4 0001x: hd_faxi_ck = hf_faxi_ck/8 00001: hd_faxi_ck = hf_faxi_ck/16 00000: hd_faxi_ck = hf_faxi_ck/32

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10210020 TST_SEL_0 Test Clock Selection Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**fmsdc30_2_tstsel**		**fmsdc30_1_tstsel**		**fmsdc30_0_tstsel**		**fmsdc50_0_tstsel**		**fusb20_tstsel**		**fspi_tstsel**		**fuart_tstsel**		**fcamtg_tstsel**	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**fmfg_tstsel**		**fvdec_tstsel**		**fpwm_tstsel**		**fmm_tstsel**		**fddrphycfg_tstsel**		**fmem_tstsel**		**faxi_tstsel**		**tstclk2_sel**	**tstclk1_sel**
Type	RW		RW		RW		RW		RW		RW		RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	fmsdc30_2_tstsel	**Selects TST clock source** 1: tclk2 0: From PLL 1: From tclk3 2: From tstclk1 3: From tstclk2
29:28	fmsdc30_1_tstsel	**Selects TST clock source** 1: tclk2 0: From PLL 1: From tclk3 2: From tstclk1 3: From tstclk2
27:26	fmsdc30_0_tstsel	**Selects TST clock source** 1: tclk2 0: From PLL 1: From tclk3 2: From tstclk1 3: From tstclk2
25:24	fmsdc50_0_tstsel	**Selects TST clock source** 1: tclk2 0: From PLL 1: From tclk3 2: From tstclk1 3: From tstclk2
23:22	fusb20_tstsel	**Selects TST clock source** 1: tclk2 0: From PLL 1: From tclk3 2: From tstclk1 3: From tstclk2
21:20	fspi_tstsel	**Selects TST clock source** 1: tclk2 0: From PLL 1: From tclk3 2: From tstclk1 3: from tstclk2
19:18	fuart_tstsel	**Selects TST clock source** 1: tclk2 0: From PLL

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Bit(s)	Name	Description
		1: From tclk3 2: From tstclk1 3: From tstclk2
17:16	fcamtg_tstsel	**Selects TST clock source** 1: tclk2 0: From PLL 1: From tclk3 2: From tstclk1 3: From tstclk2
15:14	fmfg_tstsel	**Selects TST clock source** 1: tclk2 0: from PLL 1: from tclk3 2: from tstclk1 3: from tstclk2
13:12	fvdec_tstsel	**Selects TST clock source** 1: tclk2 0: From PLL 1: From tclk3 2: From tstclk1 3: From tstclk2
11:10	fpwm_tstsel	**Selects TST clock source** 1: tclk2 0: from PLL 1: from tclk3 2: from tstclk1 3: from tstclk2
9:8	fmm_tstsel	**Selects TST clock source** 1: tclk2 0: From PLL 1: From tclk3 2: From tstclk1 3: From tstclk2
7:6	fddrphycfg_tstsel	**Selects TST clock source** 1: tclk2 0: From PLL 1: From tclk3 2: From tstclk1 3: From tstclk2
5:4	fmem_tstsel	**Selects TST clock source** 1: tclk2 0: From PLL 1: From tclk3 2: From tstclk1 3: From tstclk2
3:2	faxi_tstsel	**Selects TST clock source** 1: tclk2 0: From PLL 1: From tclk3 2: From tstclk1 3: From tstclk2

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Bit(s)	Name	Description
1	tstclk2_sel	**Selects tstclk2 clock option** 0: tclk2 1: tclk5
0	tstclk1_sel	**Selects tstclk1 clock option** 0: tclk1 1: tclk4

10210024 TST_SEL_1 Test Clock Selection Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**fdisppwm_tstsel**		**firtx_tstsel**		**firda_tstsel**		**faud_2_tstsel**		**faud_1_tstsel**		**fmfg13m_tstsel**	
Type					RW		RW		RW		RW		RW		RW	
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**fscam_tstsel**		**fdpio_tstsel**		**fatb_tstsel**		**fscp_tstsel**		**fpmicspi_tstsel**		**faud_intbus_tstsel**		**faudio_tstsel**		**fmsdc30_3_tstsel**	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:26	fdisppwm_tstsel	**Selects TST clock source** 1: tclk2 0: From PLL 1: From tclk3 2: From tstclk1 3: From tstclk2
25:24	firtx_tstsel	**Selects TST clock source** 1: tclk2 0: From PLL 1: From tclk3 2: From tstclk1 3: From tstclk2
23:22	firda_tstsel	**Selects TST clock source** 1: tclk2 0: From PLL 1: From tclk3 2: From tstclk1 3: From tstclk2
21:20	faud_2_tstsel	**Selects TST clock source** 1: tclk2 0: From PLL 1: From tclk3 2: From tstclk1 3: From tstclk2
19:18	faud_1_tstsel	**Selects TST clock source** 1: tclk2 0: From PLL 1: From tclk3 2: From tstclk1 3: From tstclk2

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Bit(s)	Name	Description
17:16	fmfg13m_tstsel	**Selects TST clock source** 1: tclk2 0: From PLL 1: From tclk3 2: From tstclk1 3: From tstclk2
15:14	fscam_tstsel	**Selects TST clock source** 1: tclk2 0: From PLL 1: From tclk3 2: From tstclk1 3: From tstclk2
13:12	fdpio_tstsel	**Selects TST clock source** 1: tclk2 0: From PLL 1: From tclk3 2: From tstclk1 3: From tstclk2
11:10	fatb_tstsel	**Selects TST clock source** 1: tclk2 0: From PLL 1: From tclk3 2: From tstclk1 3: From tstclk2
9:8	fscp_tstsel	**Selects TST clock source** 1: tclk2 0: From PLL 1: From tclk3 2: From tstclk1 3: From tstclk2
7:6	fpmicspi_tstsel	**Selects TST clock source selection** 1: tclk2 0: From PLL 1: From tclk3 2: From tstclk1 3: From tstclk2
5:4	faud_intbus_tstsel	**Selects TST clock source** 1: tclk2 0: From PLL 1: From tclk3 2: From tstclk1 3: From tstclk2
3:2	faudio_tstsel	**Selects TST clock source** 1: tclk2 0: From PLL 1: From tclk3 2: From tstclk1 3: From tstclk2
1:0	fmsdc30_3_tstsel	**Selects TST clock source** 1: tclk2 0: From PLL

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Bit(s)	Name	Description
		1: From tclk3 2: From tstclk1 3: From tstclk2

10210040 CLK_CFG_0 Function Clock Selection Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**pdn_mm**			**clk_mm_inv**		**clk_mm_sel**			**pdn_ddrphycfg**			**clk_ddrphycfg_inv**				**clk_ddrphycfg_sel**
Type	RW			RW		RW			RW			RW				RW
Reset	0			0		0	0	0	0			0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**pdn_mem**			**clk_mem_inv**				**clk_mem_sel**	**pdn_axi**			**clk_axi_inv**		**clk_axi_sel**		
Type	RW			RW				RW	RW			RW		RW		
Reset	0			0				0	0			0		0	0	0

Bit(s)	Name	Description
31	pdn_mm	**Turns off hf_fmm_ck** 1: Enable clock off
28	clk_mm_inv	**Inverts hf_fmm_ck clock phase** 1: Enable phase invert
26:24	clk_mm_sel	**Selects hf_fmm_ck clock mux** 0: clk26m 1: vencpll_ck 2: syspll1_d2 3: syspll_d5 4: syspll1_d4 5: univpll_d5 6: univpll2_d2 7: dmpll_ck
23	pdn_ddrphycfg	**Turns off hf_fddrphycfg_ck** 1: Enable clock off
20	clk_ddrphycfg_inv	**Inverts hf_fddrphycfg_ck clock phase** 1: Enable phase invert
16	clk_ddrphycfg_sel	**Selects hf_fddrphycfg_ck clock mux** 0: clk26m;1: syspll1_d8
15	pdn_mem	**Turns off hf_fmem_ck** 1: Enable clock off
12	clk_mem_inv	**Inverts hf_fmem_ck clock phase** 1: Enable phase invert
8	clk_mem_sel	**Selects hf_fmem_ck clock mux** 0: clk26m;1: dmpll_ck
7	pdn_axi	**Turns off hf_faxi_ck** 1: Enable clock off
4	clk_axi_inv	**Inverts hf_faxi_ck clock phase** 1: Enable phase invert
2:0	clk_axi_sel	**Selects hf_faxi_ck clock mux**

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Bit(s)	Name	Description
		0: clk26m 1: syspll1_d2 2: syspll_d5 3: syspll1_d4 4: univpll_d5 5: univpll2_d2 6: dmpll_ck 7: dmpll_d2

10210044 **CLK_CFG_0_SET** **SET Control of CLK_CFG_0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_0_set[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_0_set[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_0_set	**Sets the correspondent bit of CLG_CFG_SEL_0** 0: Unchange 1: Set 1'b1 to the correspondent bit

10210048 **CLK_CFG_0_CLR** **CLR Control of CLK_CFG_0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_0_clr[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_0_clr[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_0_clr	**Clears the correspondent bit of CLG_CFG_SEL_0** 0: Unchange 1: Set 1'b0 to the correspondent bit

10210050 **CLK_CFG_1** **Function Clock Selection Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_camtg			clk_camtg_inv		clk_camtg_sel			pdn_mfg			clk_mfg_inv	clk_mfg_sel			
Type	RW			RW		RW			RW			RW	RW			
Reset	0			0		0	0	0	0			0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_vdec			clk_vdec_inv		clk_vdec_sel			pdn_pwm			clk_pwm_inv			clk_pwm_sel	
Type	RW			RW		RW			RW			RW			RW	
Reset	0			0		0	0	0	0			0			0	0

Bit(s)	Name	Description
31	pdn_camtg	**Turns off hf_fcamtg_ck** 1: Enable clock off
28	clk_camtg_inv	**Inverts hf_fcamtg_ck clock phase** 1: Enable phase invert
26:24	clk_camtg_sel	**Selects hf_fcamtg_ck clock mux** 0: clk26m 1: univpll_d26 2: univpll2_d2 3: syspll3_d2 4: syspll3_d4 5: msdcpll_d4 6: mmpll_d2
23	pdn_mfg	**Turns off hf_fmfg_ck** 1: Enable clock off
20	clk_mfg_inv	**Inverts hf_fmfg_ck clock phase** 1: Enable phase invert
19:16	clk_mfg_sel	**Selects hf_fmfg_ck clock mux** 0: clk26m 1: mmpll_ck 2: clk26m 3: clk26m 4: clk26m 5: clk26m 6: clk26m 7: clk26m 8: clk26m 9: syspll_d3 10: syspll1_d2 11: syspll_d5 12: univpll_d3 13: univpll1_d2
15	pdn_vdec	**Turns off hf_fvdec_ck** 1: Enable clock off
12	clk_vdec_inv	**Inverts hf_fvdec_ck clock phase** 1: Enable phase invert
10:8	clk_vdec_sel	**Selects hf_fvdec_ck clock mux** 0: clk26m 1: syspll1_d2 2: syspll_d5 3: syspll1_d4 4: univpll_d5 5: syspll_d2 6: syspll2_d2 7: msdcpll_d2
7	pdn_pwm	**Turns off f_fpwm_ck**

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Bit(s)	Name	Description
		1: Enable clock off
4	clk_pwm_inv	**Inverts f_fpwm_ck clock phase** 1: Enable phase invert
1:0	clk_pwm_sel	**Selects f_fpwm_ck clock mux** 0: clk26m 1: univpll2_d4 2: univpll3_d2 3: univpll1_d4

10210054 **CLK_CFG_1_SET** **SET Control of CLK_CFG_1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**clk_cfg_1_set[31:16]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**clk_cfg_1_set[15:0]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_1_set	**Sets the correspondent bit of CLG_CFG_SEL_1** 0: Unchange;1: Set 1'b1 to the correspondent bit

10210058 **CLK_CFG_1_CLR** **CLR Control of CLK_CFG_1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**clk_cfg_1_clr[31:16]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**clk_cfg_1_clr[15:0]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_1_clr	**Clears the correspondent bit of CLG_CFG_SEL_1** 0: Unchange;1: Set 1'b0 to the correspondent bit

10210060 **CLK_CFG_2** **Function Clock Selection Register 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**pdn_msdc50_0**			**clk_msdc50_0_inv**		**clk_msdc50_0_sel**			**pdn_usb20**			**clk_usb20_inv**			**clk_usb20_sel**	
Type	RW			RW		RW			RW			RW			RW	
Reset	0			0		0	0	0	0			0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**pdn_spi**			**clk_spi_inv**		**clk_spi_sel**			**pdn_uart**			**clk_uart_inv**				**clk_uart_sel**

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Type	RW			RW		RW			RW			RW				RW
Reset	0			0		0	0	0	0			0				0

Bit(s)	Name	Description
31	pdn_msdc50_0	**Turns off hf_fmsdc50_0_ck** 1: Enable clock off
28	clk_msdc50_0_inv	**Inverts hf_fmsdc50_0_ck clock phase** 1: Enable phase invert
26:24	clk_msdc50_0_sel	**Selects hf_fmsdc50_0_ck clock mux** 0: clk26m 1: syspll1_d2 2: syspll2_d2 3: syspll4_d2 4: univpll_d5 5: univpll1_d4
23	pdn_usb20	**Turns off f_fusb20_ck** 1: Enable clock off
20	clk_usb20_inv	**Inverts f_fusb20_ck clock phase** 1: Enable phase invert
17:16	clk_usb20_sel	**Selects f_fusb20_ck clock mux** 0: clk26m 1: univpll1_d8 2: univpll3_d4
15	pdn_spi	**Turns off hf_fspi_ck** 1: Enable clock off
12	clk_spi_inv	**Inverts hf_fspi_ck clock phase** 1: Enable phase invert
10:8	clk_spi_sel	**Selects hf_fspi_ck clock mux** 0: clk26m 1: syspll3_d2 2: msdcpll_d8 3: syspll2_d4 4: syspll4_d2 5: univpll2_d4 6: univpll1_d8
7	pdn_uart	**Turns off f_fuart_ck** 1: Enable clock off
4	clk_uart_inv	**Inverts f_fuart_ck clock phase** 1: Enable phase invert
0	clk_uart_sel	**Selects f_fuart_ck clock mux** 0: clk26m 1: univpll2_d8

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10210064	CLK_CFG_2_SET	SET Control of CLK_CFG_2	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_2_set[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	**clk_cfg_2_set[15:0]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_2_set	**Sets the correspondent bit of CLG_CFG_SEL_2** 0: Unchange 1: Set 1'b1 to the correspondent bit

10210068 **CLK_CFG_2_CLR** **CLR Control of CLK_CFG_2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**clk_cfg_2_clr[31:16]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**clk_cfg_2_clr[15:0]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_2_clr	**Clears the correspondent bit of CLG_CFG_SEL_2** 0: Unchange 1: Set 1'b0 to the correspondent bit

10210070 **CLK_CFG_3** **Function Clock Selection Register 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**pdn_msdc30_3**			**clk_msdc30_3_inv**	**clk_msdc30_3_sel**				**pdn_msdc30_2**			**clk_msdc30_2_inv**		**clk_msdc30_2_sel**		
Type	RW			RW	RW				RW			RW		RW		
Reset	0			0	0	0	0	0	0			0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**pdn_msdc30_1**			**clk_msdc30_1_inv**		**clk_msdc30_1_sel**			**pdn_msdc30_0**			**clk_msdc30_0_inv**	**clk_msdc30_0_sel**			
Type	RW			RW		RW			RW			RW	RW			
Reset	0			0		0	0	0	0			0	0	0	0	0

Bit(s)	Name	Description
31	pdn_msdc30_3	**Turns off hf_fmsdc30_3_ck** 1: Enable clock off
28	clk_msdc30_3_inv	**Inverts hf_fmsdc30_3_ck clock phase** 1: Enable phase invert
27:24	clk_msdc30_3_sel	**Selects hf_fmsdc30_3_ck clock mux** 0: clk26m 1: univpll2_d2 2: msdcpll_d4 3: syspll2_d2

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Bit(s)	Name	Description
		4: syspll1_d4 5: univpll1_d4 6: univpll_d26 7: msdcpll_d16 8: syspll2_d4
23	pdn_msdc30_2	**Turns off hf_fmsdc30_2_ck** 1: Enable clock off
20	clk_msdc30_2_inv	**Inverts hf_fmsdc30_2_ck clock phase** 1: Enable phase invert
18:16	clk_msdc30_2_sel	**Selects hf_fmsdc30_2_ck clock mux** 0: clk26m 1: univpll2_d2 2: msdcpll_d4 3: syspll2_d2 4: syspll1_d4 5: univpll1_d4 6: univpll_d26 7: syspll2_d4
15	pdn_msdc30_1	**Turns off hf_fmsdc30_1_ck** 1: Enable clock off
12	clk_msdc30_1_inv	**Inverts hf_fmsdc30_1_ck clock phase** 1: Enable phase invert
10:8	clk_msdc30_1_sel	**Selects hf_fmsdc30_1_ck clock mux** 0: clk26m 1: univpll2_d2 2: msdcpll_d4 3: syspll2_d2 4: syspll1_d4 5: univpll1_d4 6: univpll_d26 7: syspll2_d4
7	pdn_msdc30_0	**Turns off hf_fmsdc30_0_ck** 1: Enable clock off
4	clk_msdc30_0_inv	**Inverts hf_fmsdc30_0_ck clock phase** 1: Enable phase invert
3:0	clk_msdc30_0_sel	**Selects hf_fmsdc30_0_ck clock mux** 0: clk26m 1: msdcpll_ck 2: msdcpll_d2 3: msdcpll_d4 4: syspll2_d2 5: syspll1_d4 6: univpll1_d4 7: univpll_d3 8: univpll_d26 9: syspll2_d4 10: univpll_d2

10210074 CLK_CFG_3 SET Control of CLK_CFG_3 00000000

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SET

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_3_set[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_3_set[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_3_set	**Sets the correspondent bit of CLG_CFG_SEL_3** 0: Unchange 1: Set 1'b1 to the correspondent bit

10210078 CLK_CFG_3_CLR CLR Control of CLK_CFG_3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_3_clr[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_3_clr[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_3_clr	**Clears the correspondent bit of CLG_CFG_SEL_3** 0: Unchange 1: Set 1'b0 to the correspondent bit

10210080 CLK_CFG_4 Function Clock Selection Register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_scp			clk_scp_inv			clk_scp_sel		pdn_pmicspi			clk_pmicspi_inv		clk_pmicspi_sel		
Type	RW			RW			RW		RW			RW		RW		
Reset	0			0			0	0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_aud_intbus			clk_aud_intbus_inv			clk_aud_intbus_sel		pdn_audio			clk_audio_inv			clk_audio_sel	
Type	RW			RW			RW		RW			RW			RW	
Reset	0			0			0	0	0			0			0	0

Bit(s)	Name	Description
31	pdn_scp	**Turns off hf_fscp_ck** 1: Enable clock off
28	clk_scp_inv	**Inverts hf_fscp_ck clock phase** 1: Enable phase invert
25:24	clk_scp_sel	**Selects hf_fscp_ck clock mux**

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Bit(s)	Name	Description
		0: clk26m 1: syspll1_d8 2: dmpll_d2 3: dmpll_d4
23:21	pdn_pmicspi	**Turns off hf_fpmicspi_ck** 1: Enable clock off
20	clk_pmicspi_inv	**Inverts hf_fpmicspi_ck clock phase** 1: Enable phase invert
18:16	clk_pmicspi_sel	**Selects hf_fpmicspi_ck clock mux** 0: clk26m 1: syspll1_d8 2: syspll3_d4 3: syspll1_d16 4: univpll3_d4 5: univpll_d26 6: dmpll_d4 7: dmpll_d8
15	pdn_aud_intbus	**Turns off hf_faud_intbus_ck** 1: Enable clock off
12	clk_aud_intbus_inv	**Inverts hf_faud_intbus_ck clock phase** 1: Enable phase invert
9:8	clk_aud_intbus_sel	**Selects hf_faud_intbus_ck clock mux** 0: clk26m 1: syspll1_d4 2: syspll4_d2 3: dmpll_d4
7	pdn_audio	**Turns off hf_faudio_ck** 1: Enable clock off
4	clk_audio_inv	**Inverts hf_faudio_ck clock phase** 1: Enable phase invert
1:0	clk_audio_sel	**Selects hf_faudio_ck clock mux** 0: clk26m 1: syspll3_d4 2: syspll4_d4 3: syspll1_d16

10210084 **CLK_CFG_4_SET** **SET Control of CLK_CFG_4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_4_set[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_4_set[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_4_set	**Sets the correspondent bit of CLG_CFG_SEL_4**

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Bit(s)	Name	Description
		0: Unchange 1: Set 1'b1 to the correspondent bit

10210088 **CLK_CFG_4_CLR** **CLR Control of CLK_CFG_4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_4_clr[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_4_clr[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_4_clr	**Clears the correspondent bit of CLG_CFG_SEL_4** 0: Unchange 1: Set 1'b0 to the correspondent bit

10210090 **CLK_CFG_5** **Function Clock Selection Register 5** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_mfg13m			clk_mfg13m_inv				clk_mfg13m_sel	pdn_scam			clk_scam_inv			clk_scam_sel	
Type	RW			RW				RW	RW			RW			RW	
Reset	0			0				0	0			0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_dpio			clk_dpio_inv		clk_dpio_sel			pdn_atb			clk_atb_inv			clk_atb_sel	
Type	RW			RW		RW			RW			RW			RW	
Reset	0			0		0	0	0	0			0			0	0

Bit(s)	Name	Description
31	pdn_mfg13m	**Turns off hs_fmfg13m_ck** 1: Enable clock off
28	clk_mfg13m_inv	**Inverts hs_fmfg13m_ck clock phase** 1: Enable phase invert
24	clk_mfg13m_sel	**Selects hs_fmfg13m_ck clock mux** 0: clk26m 1: ad_sys_26m_d2
23	pdn_scam	**Turns off hf_fscam_ck** 1: Enable clock off
20	clk_scam_inv	**Inverts hf_fscam_ck clock phase** 1: Enable phase invert
17:16	clk_scam_sel	**Selects hf_fscam_ck clock mux** 0: clk26m 1: syspll3_d2 2: univpll2_d4

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Bit(s)	Name	Description
		3: vencpll_d3
15	pdn_dpio	**Turns off hf_fdpio_ck** 1: Enable clock off
12	clk_dpio_inv	**Inverts hf_fdpio_ck clock phase** 1: Enable phase invert
10:8	clk_dpio_sel	**Selects hf_fdpio_ck clock mux** 0: clk26m 1: tvdpll_ck 2: tvdpll_d2 3: tvdpll_d4 4: dpi_ck
7	pdn_atb	**Turns off hf_fatb_ck** 1: Enable clock off
4	clk_atb_inv	**Inverts hf_fatb_ck clock phase** 1: Enable phase invert
1:0	clk_atb_sel	**Selects hf_fatb_ck clock mux** 0: clk26m 1: syspll1_d2 2:syspll_d5 3: dmpll_ck

10210094 **CLK_CFG_5_SET** **SET Control of CLK_CFG_5** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_5_set[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_5_set[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_5_set	**Sets the correspondent bit of CLG_CFG_SEL_5** 0: Unchange 1: Set 1'b1 to the correspondent bit

10210098 **CLK_CFG_5_CLR** **CLR Control of CLK_CFG_5** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_5_clr[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_5_clr[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	clk_cfg_5_clr	**Clears the correspondent bit of CLG_CFG_SEL_5** 0: Unchange 1: Set 1'b0 to the correspondent bit

102100A0 CLK_CFG_6 Function Clock Selection Register 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_irtx			clk_irtx_inv				clk_irtx_sel	pdn_irda			clk_irda_inv				clk_irda_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_aud_2			clk_aud_2_inv				clk_aud_2_sel	pdn_aud_1			clk_aud_1_inv				clk_aud_1_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0

Bit(s)	Name	Description
31	pdn_irtx	**Turns off hf_firtx_ck** 1: Enable clock off
28	clk_irtx_inv	**Inverts hf_firtx_ck clock phase** 1: Enable phase invert
24	clk_irtx_sel	**Selects hf_firtx_ck clock mux** 0: clk26m 1: ad_sys_26m_ck
23	pdn_irda	**Turns off hf_firda_ck** 1: Enable clock off
20	clk_irda_inv	**Inverts hf_firda_ck clock phase** 1: Enable phase invert
16	clk_irda_sel	**Selects hf_firda_ck clock mux** 0: clk26m 1: univpll2_d4
15	pdn_aud_2	**Turns off hf_faud_2_ck** 1: Enable clock off
12	clk_aud_2_inv	**Inverts hf_faud_2_ck clock phase** 1: Enable phase invert
8	clk_aud_2_sel	**Selects hf_faud_2_ck clock mux** 0: clk26m 1: whpll_audio_ck
7	pdn_aud_1	**Turns off hf_faud_1_ck** 1: Enable clock off
4	clk_aud_1_inv	**Inverts hf_faud_1_ck clock phase** 1: Enable phase invert
0	clk_aud_1_sel	**Selects hf_faud_1_ck clock mux** 0: clk26m 1: ad_apll1_ck

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102100A4 CLK_CFG_6_SET SET Control of CLK_CFG_6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_6_set[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_6_set[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_6_set	**Sets the correspondent bit of CLG_CFG_SEL_6** 0: Unchange 1: Set 1'b1 to the correspondent bit

102100A8 CLK_CFG_6_CLR CLR Control of CLK_CFG_6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_6_clr[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_6_clr[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_6_clr	**Clears the correspondent bit of CLG_CFG_SEL_6** 0: Unchange 1: Set 1'b0 to the correspondent bit

102100B0 CLK_CFG_7 Function Clock Selection Register 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									pdn_disppwm			clk_disppwm_inv			clk_disppwm_sel	
Type									RW			RW			RW	
Reset									0			0			0	0

Bit(s)	Name	Description
7	pdn_disppwm	**Turns off hf_fdisppwm_ck** 1: Enable clock off
4	clk_disppwm_inv	**Inverts hf_fdisppwm_ck clock phase** 1: Enable phase invert
1:0	clk_disppwm_sel	**Selects hf_fdisppwm_ck clock mux**

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Bit(s)	Name	Description
		0: clk26m 1: univpll2_d4 2: syspll4_d2_d8 3: ad_sys_26m_ck

102100B4 **CLK_CFG_7_SET** **SET Control of CLK_CFG_7** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_7_set[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_7_set[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_7_set	**Sets the correspondent bit of CLG_CFG_SEL_7** 0: Unchange 1: Set 1'b1 to the correspondent bit

102100B8 **CLK_CFG_7_CLR** **CLR Control of CLK_CFG_7** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_7_clr[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_7_clr[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_7_clr	**Clears the correspondent bit of CLG_CFG_SEL_7** 0: Unchange 1: Set 1'b1 to the correspondent bit

10210100 **CLK_CFG_8** **Function Clock Selection Register 8** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			abist_clk_sel													
Type			RW													
Reset			0	0	0	0	0	0								

Bit(s)	Name	Description

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Bit(s)	Name	Description
13:8	abist_clk_sel	**Selects f_fabist_ck clock mux not glitch free** 01: AD_MAIN_H546M_CK 02: AD_MAIN_H364M_CK 03: AD_MAIN_H218P4M_CK 04: AD_MAIN_H156M_CK 05: AD_UNIV_624M_CK 06: AD_UNIV_416M_CK 07: AD_UNIV_249P6M_CK 08: AD_UNIV_178P3M_CK 09: AD_UNIV_48M_CK 10: AD_USB_48M_CK 11: AD_MMPLL_CK 12: AD_MSDCPLL_CK 13: AD_DPICLK 14: clkph_MCK_o 15: AD_MEMPLL2_CKOUT0_PRE_ISO 16: AD_APLL1_CK 17: AD_MDPLL1_416M_CK 18: AD_WPLL_245P76M_CK 19: AD_WHPLL_250P25M_CK 20: rtc32k_ck_i 21: AD_SYS_26M_CK 22: AD_VENCPLL_CK 23: AD_TVDPLL_CK 24: D_VENC_H98P6M_CK 25: AD_WHPLL_audio_CK 26~32: RESERVED 33: abist_clk1 34: abist_clk2 35: abist_clk3 36: abist_clk4 37: abist_clk5 38: abist_clk6 39: abist_clk7 40: abist_clk8 41: abist_clk9 42: abist_clk10 43: abist_clk11 44: abist_clk12 45: abist_clk13 46: abist_clk14 47: abist_clk15 48: abist_clk16 49: abist_clk17 50: abist_clk18 51: abist_clk19 52: abist_clk20 53: abist_clk21 54~63: Reserved

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10210104 CLK_CFG_9 Function Clock Selection Register 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											ckgen_clk_sel					
Type											RW					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

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Bit(s)	Name	Description
21:16	ckgen_clk_sel	**Selects f_fckgen_ck clock mux (not glitch free)** 01: hf_faxi_ck 02: hd_faxi_ck 03: hf_fdpio_ck 04: hf_fddrphycfg_ck 05: hf_fmm_ck 06: f_fpwm_ck 07: hf_fvdec_ck 08: hf_fmfg_ck 09: hf_fcamtg_ck 10: f_fuart_ck 11: hf_fspi_ck 12: f_fusb20_ck 13: hf_fmsdc30_0_ck 14: hf_fmsdc30_1_ck 15: hf_fmsdc30_2_ck 16: hf_faudio_ck 17: hf_faud_intbus_ck 18: hf_fpmicspi_ck 19: f_frtc_ck 20: f_f26m_ck 21: f_f32k_md1_ck 22: f_frtc_conn_ck 23: hf_fusb20p1_ck 24: hg_fmipicfg_ck 25: hd_haxi_nli_ck 26: hd_qaxidcm_ck 27: f_ffpc_ck 28: hf_fscam_ck 29: f_fckbus_ck_scan 30: f_fckrtc_ck_scan 31: hf_fatb_ck 32: hf_faud1_ck 33: hf_faud2_ck 34: hf_fmsdc50_0_ck 35: hf_firda_ck 36: hf_firtx_ck 37: hf_fdisppwm 38: hs_fmfg13m_ck

10210108 **CLK_CFG_10** **Debug Monitor Clock Selection Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**clk_ckmon4_sel**								**clk_ckmon3_sel**			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**clk_ckmon2_sel**								**clk_ckmon1_sel**			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
27:24	clk_ckmon4_sel	**Reserved**
19:16	clk_ckmon3_sel	**Selects f_fckmon3_ck clock mux (not glitch free)** 1: AD_SYS_26M_CK 2: rtc32k_ck_i 3: AD_WHPLL_CK 4: AD_WPLL_CK

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Bit(s)	Name	Description
		5: AD_MDPLL1_416M_CK 6: AD_MCUPLL_CK 7: clkph_MCLK_o 8: AD_DPICLK 9: AD_MSDCPLL_CK 10: AD_MMPLL_CK 11: AD_UNIV_178P3M_CK 12: AD_MAIN_H156M_CK 13: AD_VENCPLL_CK 14: AD_TVDPLL_CK 15: Reserved
11:8	clk_ckmon2_sel	**Selects f_fckmon2_ck clock mux (not glitch free)** 1: AD_SYS_26M_CK 2: rtc32k_ck_i 3: AD_WHPLL_CK 4: AD_WPLL_CK 5: AD_MDPLL1_416M_CK 6: AD_MCUPLL_CK 7: clkph_MCLK_o 8: AD_DPICLK 9: AD_MSDCPLL_CK 10: AD_MMPLL_CK 11: AD_UNIV_178P3M_CK 12: AD_MAIN_H156M_CK 13: AD_VENCPLL_CK 14: AD_TVDPLL_CK 15: Reserved
3:0	clk_ckmon1_sel	**Selects f_fckmon1_ck clock mux (not glitch free)** 1: AD_SYS_26M_CK 2: rtc32k_ck_i 3: AD_WHPLL_CK 4: AD_WPLL_CK 5: AD_MDPLL1_416M_CK 6: AD_MCUPLL_CK 7: clkph_MCLK_o 8: AD_DPICLK 9: AD_MSDCPLL_CK 10: AD_MMPLL_CK 11: AD_UNIV_178P3M_CK 12: AD_MAIN_H156M_CK 13: AD_VENCPLL_CK 14: AD_TVDPLL_CK 15: Reserved

1021010C CLK_CFG_11 Debug Monitor Divider Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ckmon4_k1								ckmon3_k1							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ckmon2_k1								ckmon1_k1							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	ckmon4_k1	Reserved
23:16	ckmon3_k1	Frequency = (clk_ckmon2_sel)/(ckmon_k2 + 1)

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Bit(s)	Name	Description
15:8	ckmon2_k1	Frequency = (clk_ckmon2_sel)/(ckmon_k2 + 1)
7:0	ckmon1_k1	Frequency = (clk_ckmon1_sel)/(ckmon_k1 + 1)

10210200 CLK_SCP_CFG_0 SCP Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name							sc_mac_26m_off_en	sc_conn_26m_off_en	sc_conn_32k_off_en	sc_md_26m_off_en	sc_md_32k_off_en	sc_armck_off_en	sc_smick_off_en	sc_axick_off_en	sc_memck_off_en	sc_26ck_off_en
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9	sc_mac_26m_off_en	0: Disable scpsys clock-off control 1: Enable scpsys clock-off control
8	sc_conn_26m_off_en	**Reserved** 0: Disable scpsys clock off-control 1: Enable scpsys clock off-control
7	sc_conn_32k_off_en	0: Disable scpsys clock-off control 1: Enable scpsys clock-off control
6	sc_md_26m_off_en	**Reserved** 0: Disable scpsys clock off-control 1: Enable scpsys clock off-control
5	sc_md_32k_off_en	0: Disable scpsys clock-off control 1: Enable scpsys clock-off control
4	sc_armck_off_en	0: Disable scpsys clock-off control 1: Enable scpsys clock-off control
3	sc_smick_off_en	**Reserved** 0: Disable scpsys clock off-control 1: Enable scpsys clock off-control
2	sc_axick_off_en	0: Disable scpsys clock-off control 1: Enable scpsys clock-off control
1	sc_memck_off_en	0: Disable scpsys clock-off control 1: Enable scpsys clock-off control
0	sc_26ck_off_en	0: Disable scpsys clock-off control 1: Enable scpsys clock-off control

10210204 CLK_SCP_CFG_1 SCP Control Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name												sc_ax				sc_ax

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												ick_dcm_dis_en				ick_26m_sel_en
Type												RW				RW
Reset												0				0

Bit(s)	Name	Description
4	sc_axick_dcm_dis_en	0: Disable scpsys clock-off control 1: Enable scpsys clock-off control
0	sc_axick_26m_sel_en	0: Disable scpsys clock-off control 1: Enable scpsys clock-off control

10210210 CLK_MISC_CFG_0 MCU Clock Jitter Measurement Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		rg_mcu_jit_ck_sel						rg_mcu_jit_cken						pdn_aud24m	pdn_aud22m	pdn_efuse
Type		RW						RW						RW	RW	RW
Reset		0	0	0				0						0	0	0

Bit(s)	Name	Description
14:12	rg_mcu_jit_ck_sel	**Reserved** 00: feedback clock from mcusys_par_wrap 01: feedback clock0 from mcusys internal 11: feedback clock1 from mcusys internal
8	rg_mcu_jit_cken	**Reserved** 0: Disable scpsys clock off-control 1: Enable scpsys clock off-control
2	pdn_aud24m	**Turns off f_faud24m_ck** 1: Enable turn off
1	pdn_aud22m	**Turns off f_faud22m_ck** 1: Enable turn off
0	pdn_efuse	**Turns off f_fefuse_ck** 1: Enable turn off

10210214 CLK_MISC_CFG_1 Frequency Meter Divider Control Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ckgen_k1								ckgen1_k1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	arm_k1								abist_k1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

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Bit(s)	Name	Description
31:24	ckgen_k1	**Divider setting of f_fckgen_ck**
23:16	ckgen1_k1	**For ckgen1 clock use** Debugs monitor. Reserved
15:8	arm_k1	**Divider setting of hf_farm_ck**
7:0	abist_k1	**Divider setting of f_fabist_ck**

10210218 **CLK_MISC_CFG_2** **MEM DCM Idle Signal Force Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**mem_dcm_force_idle**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	mem_dcm_force_idle	**mem_dcm_force_idle** bit0: infra_idle force bit1: mcusys_idle_force bit2: mfg_idle_force bit3: mdsys_idle_force bit4: c2k_idle_force 0: Idle not forced 1: Idle forced to high

10210220 **CLK26CALI_0** **Frequency Meter Control Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**rg_abist_clk_en**		**ckgen_clk_exc**	**ckgen_tri_cal**		**clk_exc**	**pll_test**	**abist_tri_cal**
Type									RW		RW	RW		RW	RW	RW
Reset									0		0	0		0	0	0

Bit(s)	Name	Description
7	rg_abist_clk_en	0: Disable rg_abist_clk 1: Enable rg_abist_clk
5	ckgen_clk_exc	**Selects measuring clock** 0: f_fckgen_ck 1: CLK26M
4	ckgen_tri_cal	**Triggers frequency meter on f_fckgen_ck** Auto-cleared when calibration is done 0: Disable 1: Enable
2	clk_exc	**Selects measuring clock**

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Bit(s)	Name	Description
		0: Disable 1: Enable
1	pll_test	**Selects clock divider test clock** 0: PLL 1: test clock
0	abist_tri_cal	**Triggers frequency meter on f_fabist_ck** Auto-cleared when calibration is done 0: Disable 1: Enable

10210224 CLK26CALI_1 Frequency Meter Control Register 1 03FF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							abist_load_cnt									
Type							RW									
Reset							1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cal_cnt															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	abist_load_cnt	
15:0	cal_cnt	**Frequency meter result of f_fabist_ck** Frequency = (26Mhz*cal_cnt)/(abist_load_cnt + 1)

10210228 CLK26CALI_2 Frequency Meter Control Register 2 03FF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ckgen_load_cnt									
Type							RW									
Reset							1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ckgen_cal_cnt															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	ckgen_load_cnt	
15:0	ckgen_cal_cnt	**Frequency meter result of f_fckgen_ck** Frequency = (26Mhz*cal_cnt)/(ckgen_load_cnt + 1)

1021022C CKSTA_REG Function Clock Selection Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																chg_sta

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Type																RU
Reset																0

Bit(s)	Name	Description
0	chg_sta	Clock switches changing in progress

10210230 **TEST_MODE_CFG** **Test Mode Control Register** **00000300**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**rg_conn_top2_test_mem_pd**	**rg_conn_top1_test_mem_pd**	**rg_conn_top2_test_pwr_on**	**rg_conn_top1_test_pwr_on**							**release_strap_pre**	**release_fpc_pad**
Type					RW	RW	RW	RW							RW	RW
Reset					0	0	1	1							0	0

Bit(s)	Name	Description
11	rg_conn_top2_test_mem_pd	
10	rg_conn_top1_test_mem_pd	
9	rg_conn_top2_test_pwr_on	
8	rg_conn_top1_test_pwr_on	Reserved
1	release_strap_pre	release_strap_pre
0	release_fpc_pad	release_fpc_pad

10210308 **MBIST_CFG_0** **Debug Monitor Selection Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**mbist_sel[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**mbist_sel[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	mbist_sel	**Selects clock monitor for debug monitor** Reserved

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1021030C MBIST_CFG_1 Debug Monitor Selection Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name										ckgen_byte_sel			peri_byte_sel		infra_byte_sel	
Type										RW			RW		RW	
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:4	ckgen_byte_sel	**Selects TOPCKGEN debug monitor**
3:2	peri_byte_sel	**Selects perisys debug monitor** Reserved
1:0	infra_byte_sel	**Selects infra_top debug monitor** Reserved

10210310 RESET_DEGLITCH_KEY Reset Deglitch Enable Key Register 67D2A357

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dgrst_en_key[31:16]															
Type	RW															
Reset	0	1	1	0	0	1	1	1	1	1	0	1	0	0	1	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	dgrst_en_key[15:0]															
Type	RW															
Reset	1	0	1	0	0	0	1	1	0	1	0	1	0	1	1	1

Bit(s)	Name	Description
31:0	dgrst_en_key	Writes 0x67D2_A357 to enable reset deglitch

10210314 MBIST_CFG_3 Debug Monitor Selection Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	usb_gpio_reg															
Type	RW															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Name	Description
15:8	usb_gpio_reg	Selects usb_i2c_mode

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4.1.9 Programming Guide

4.1.9.1 Clock Off

- The clock can be turned on/off through changing the value of pdn_*. However, this control cannot be switched along with clk_*_sel and clk_*_inv.
- It is recommended to change pdn_* with SET and CLEAR function provided by CLK_CFG_*_SET and CLK_CFG_*_CLR. Because there may be clock with multi-bit pdn_* which are planned to avoid read modify write from different sub-systems (APSYS, MDSYS) at the same time.
- SET and CLEAR function of CLK_CFG_* is a solution to avoid read modify write from different sub-systems.

4.1.9.1.1 Clock Switching

- Make sure clock A and clock B are available before changing the setting of clk_*_sel. If switched to a non-exist clock, the clock switch will be stuck until non-exist clock is turned on to free the clock switch.
- Supports multi-clock switching at the same time (without changing pdn_*)

Switching from clock A to clock B

1. Make sure clock B is ready.
2. Change clk_*_sel.
3. Wait until chg_sta = 1'b0 (optional).
4. Turn off clock A (optional).

4.1.9.1.2 Switch AXI to 26MHz by SCPSYS

The reflection time is about 17T 26MHz if all clocks are counted as 26MHz. Refer to the following formula:

$$4T\ Bus\ Clock_{(*1)} + 4T\ Current\ Clock_{(*2)} + 5T\ Reference\ Clock_{(*3)} + 1T\ Bus\ Clock_{(*4)} + 3T\ Target\ Clock_{(*5)}$$

Comment	Description
Bus clock	26MHz (in current project)
Ref clock	26MHz, balance with bus clock
*1	2T Sync + 1 T Control
*2	3T sync
*3	4T sync
*4	1T control. For async CLKSW like hf_fmem_ck used, it will be 2T sync.
*5	2T sync

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4.1.9.1.3 Frequency Meter

There are two frequency meters embedded inside TOPCKGEN.

1. Set fmeter_en to 1'b1.
2. Choose target clock by changing abist_clk_sel/ckgen_clk_sel.
3. Change abist_k1/ckgen_k1 for dividing target clock (optional).
4. Change reference clock by changing clk_exec/ckgen_exec (optional).
5. Change abist_load_cnt/ckgen_load_cnt (optional).
6. Trigger frequency meter by set tri_cal/ckgen_tri_cal = 1b'1.
7. Wait until tri_cal/ckgen_tri_cal = 1'b0.
8. Read frequency meter result from cal_cnt/ckgen_cal_cnt.
    - freq(target) = (abist_k1 + 1)*[freq(reference clock)*cal_cnt]/(abist_load_cnt + 1)
    - freq(target) = (ckgen_k1 + 1)*[freq(reference clock)*ckgen_cal_cnt]/(ckgen_load_cnt + 1)

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4.2 Top Reset Generate Unit

4.2.1 Introduction

The top reset generator unit (TOPRGU) generates reset signals and distributes to each system. A watchdog timer is also included in this module.

4.2.2 Features

- Hardware reset signals for the whole chip
- Software controllable reset for each system (except for infrastructure and apmixedsys system)
- Watchdog timer
- Reset output signals for companion chips

4.2.3 Block Diagram

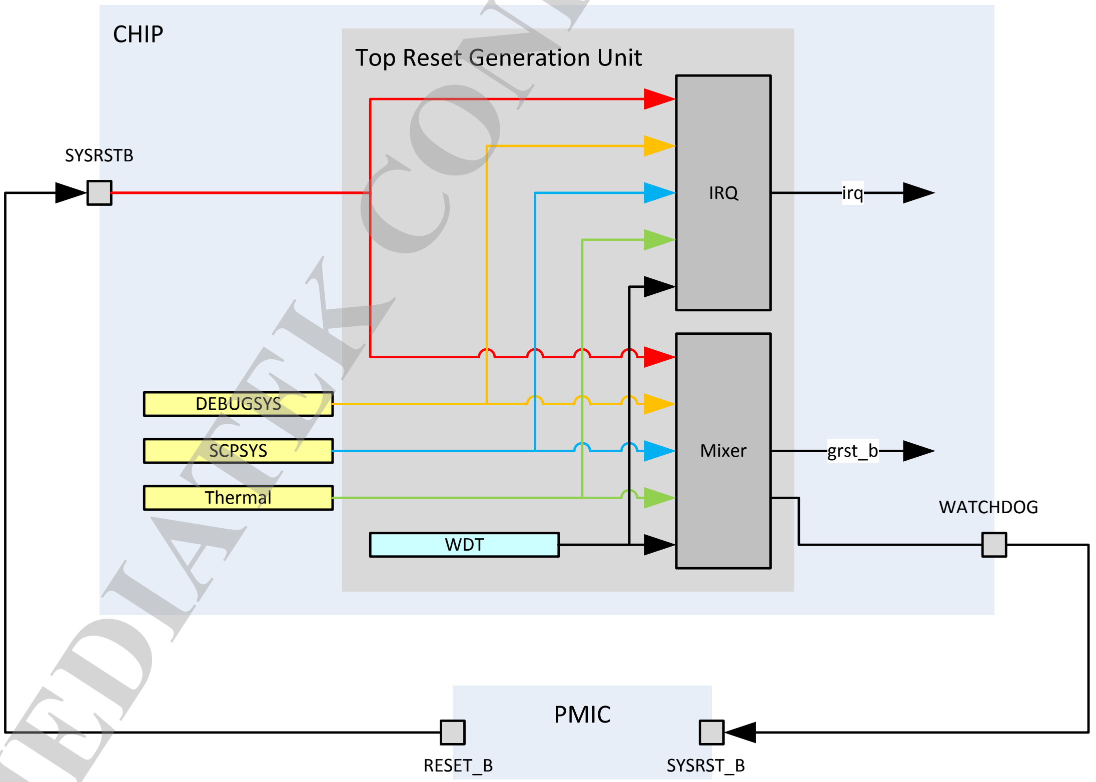

Figure 4-6. Block diagram of top reset generation unit

4.2.4 Register Definition

Module name: TOPRGU Base address: (+10007000h)

Address	Name	Width	Register Function

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Address	Name	Width	Register Function
10007000	TOPRGU_WDT_MODE	32	**Watchdog Mode Register** Will not be reset.
10007004	TOPRGU_WDT_LENGTH	32	Watchdog Counter Setting Register
10007008	TOPRGU_WDT_RESTART	32	Watchdog Counter Restart Register
1000700C	TOPRGU_WDT_STA	32	**Watchdog Status Register** Will not be reset.
10007010	TOPRGU_WDT_INTERVAL	32	**Watchdog Reset Pulse Width Register**
10007014	TOPRGU_WDT_SWRST	32	**Software Watchdog Reset Register**
10007018	TOPRGU_WDT_SWSYSRST	32	**System Software Reset Register**
10007020	TOPRGU_WDT_NONRST_REG	32	**Watchdog Non-Reset Register** Will not be reset.
10007024	TOPRGU_WDT_NONRST_REG2	32	**Watchdog Non-Reset Register** Will not be reset.
10007030	TOPRGU_WDT_REQ_MODE	32	**Reset Request Mode Register** Will not be reset.
10007034	TOPRGU_WDT_REQ_IRQ_EN	32	**Reset Request IRQ Enable Register** Will not be reset.
10007040	TOPRGU_WDT_DEBUG_CTL	32	**Debug Control Register** Will not be reset.
10007050	TOPRGU_WDT_INTERCORE_SYNC	32	Intercore Sync Register
10007054	TOPRGU_WDT_INTERCORE_SYNC_SET	32	Set Control of Intercore Sync Register
10007058	TOPRGU_WDT_INTERCORE_SYNC_CLR	32	Clear Control of Intercore Sync Register
10007500	TOPRGU_DEBUG_0_REG	32	Shadow Register of WDT_MODE
10007504	TOPRGU_DEBUG_1_REG	32	Shadow Register of WDT_STA
10007508	TOPRGU_DEBUG_2_REG	32	Shadow Register of WDT_DEBUG_CTL
1000750C	TOPRGU_DEBUG_3_REG	32	Shadow Register of WDT_REQ_MODE
10007510	TOPRGU_DEBUG_4_REG	32	Shadow Register of WDT_REG_IRQ_EN

10007000 TOPRGU_WDT_MODE Watchdog Mode Register 2200004D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key															
Type	WO															
Reset	0	0	1	0	0	0	1	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								wdt_c	ddr_r	dual_	irq_lv		wdt_i	exten	extpo	wdt_

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								nt_reset_sel	eserve_mode	mode	l_en		rq		l	en
Type								RW	RW	RW	RW		RW	RW	RW	RW
Reset								0	0	1	0		1	1	0	1

Bit(s)	Name	Description
31:24	unlock_key	**Write 0x22 to unlock the write protection of this register**
8	wdt_cnt_reset_sel	**Selects reset source of watchdog timer** 0: Reset only by external reset 1: Reset by TOPRGU
7	ddr_reserve_mode	**Enables ddr_reserve_mode** 0: Disable 1: Enable
6	dual_mode	**Enables dual_mode** Turns on watchdog timer and enables the corresponding irq_en and wdt_en if dual_mode is used 0: Disable 1: Enable
5	irq_lvl_en	**Selects IRQ type** 0: Edge (32K) 1: Level
3	wdt_irq	**Enables watchdog timer IRQ** 0: Trigger reset 1: Trigger IRQ
2	exten	**Enables watchdog output reset signal** 0: Disable 1: Enable
1	extpol	**Watchdog output reset signal polarity** 0: Active low 1: Active high
0	wdt_en	**Enables watchdog timer** 0: Disable 1: Enable

10007004 **TOPRGU_WDT_LENGTH** **Watchdog Counter Setting Register** **0000FFE8**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	wdt_length											unlock_key				
Type	RW											WO				
Reset	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	0

Bit(s)	Name	Description
15:5	wdt_length	**Watchdog time-out counter setting** The counter is restarted with {wdt_length [10:0], 1_1111_1111b}, and therefore the watchdog timer time-out period is a multiple of 512*T32k=15.6ms
4:0	unlock_key	**Write 0x8 to unlock the write protection of this register**

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10007008 TOPRGU_WDT_RESTART Watchdog Counter Restart Register 00001971

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	**wdt_restart**															
Type	WO															
Reset	0	0	0	1	1	0	0	1	0	1	1	1	0	0	0	1

Bit(s)	Name	Description
15:0	wdt_restart	Write 0x1971 to reset the watchdog time-out counter

1000700C TOPRGU_WDT_STA Watchdog Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**hw_wdt_rst**	**sw_wdt_rst**	**irq_assert**	**security_rst**									**debug_rst**	**thermal_ctl_rst**		
Type	RO	RO	RO	RO									RO	RO		
Reset	0	0	0	0									0	0		
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name															**spm_rst**	**spm_thermal_rst**
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
31	hw_wdt_rst	Indicates hardware watchdog generated reset is asserted
30	sw_wdt_rst	Indicates software watchdog generated reset is asserted
29	irq_assert	Indicates IRQ is asserted instead of reset
28	security_rst	Indicates security reset is asserted
19	debug_rst	Indicates debug generated reset is asserted
18	thermal_ctl_rst	Indicates thermal reset generated by thermal controller is asserted
1	spm_rst	Indicates scpsys time-out generated reset is asserted
0	spm_thermal_rst	Indicates thermal reset generated by scpsys reset is asserted

10007010 TOPRGU_WDT_INTERVAL Watchdog Reset Pulse Width Register 00000FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					**wdt_reset_interval**											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

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Bit(s)	Name	Description
11:0	wdt_reset_interval	**Resets pulse width generated by watchdog** 2T 32K duration is required for TD modem. Unit: 1T=1x32kHz

10007014 TOPRGU_WDT_SWRST Software Watchdog Reset Register 00001209

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	**unlock_key**															
Type	WO															
Reset	0	0	0	1	0	0	1	0	0	0	0	0	1	0	0	1

Bit(s)	Name	Description
15:0	unlock_key	Write 0x1209 to generate a software watchdog reset.

10007018 TOPRGU_WDT_SWSYSRST System Software Reset Register 88008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**unlock_key**															
Type	WO															
Reset	1	0	0	0	1	0	0	0								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	**c2k_rst**	**c2k_sw_rst**					**conn_rst**		**md_rst**		**img_rst**	**vdec_rst**	**venc_rst**	**mfg_rst**	**mm_rst**	
Type	RW	RW					RW		RW		RW	RW	RW	RW	RW	
Reset	1	0					0		0		0	0	0	0	0	

Bit(s)	Name	Description
31:24	unlock_key	**Write 0x88 to unlock the write protection of this register.**
15	c2k_rst	**Write 1 to reset the MODEM C2K system.** 2T 32K duration is required for TD modem
14	c2k_sw_rst	**Write 1 to reset the MODEM C2K system when C2K WDT is asserted.** 2T 32K duration is required for TD modem
9	conn_rst	**Write 1 to reset CONNSYS.**
7	md_rst	**Write 1 to reset the MODEM system** 2T 32K duration is required for TD modem
5	img_rst	**Write 1 to reset VENC & IMG and its related pad macro (cam, mipi_rx)**
4	vdec_rst	**Write 1 to reset VDEC.**
3	venc_rst	**Write 1 to reset VENC.**
2	mfg_rst	**Write 1 to reset MFG.**
1	mm_rst	**Write 1 to reset MM and its related pad macro (SPI, DPI, MIPI_CFG, MIPI_TX).**

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10007020 **TOPRGU_WDT_NONRST_REG** **Watchdog Non-Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	non_reset_register[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	non_reset_register[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	non_reset_register	**This register will not be reset by WDT and will only be reset by external system reset.** Used for SW to record the status of the pervious boot.

10007024 **TOPRGU_WDT_NONRST_REG2** **Watchdog Non-Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	non_reset_register2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	non_reset_register2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	non_reset_register2	**This register will not be reset by WDT and will only be reset by external system reset.** Used for SW to record the status of the pervious boot.

10007030 **TOPRGU_WDT_REQ_MODE** **Reset Request Mode Register** **333C0003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key												debug_en	thermal_ctl_en		
Type	WO												RW	RW		
Reset	0	0	1	1	0	0	1	1					1	1		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															spm_en	spm_thermal_en
Type															RW	RW
Reset															1	1

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Bit(s)	Name	Description
31:24	unlock_key	**Write 0x33 to unlock the write protection of this register.**
19	debug_en	**Enables debugsys reset** 0: Disable 1: Enable
18	thermal_ctl_en	**Enables thermal controller reset** 0: Disable 1: Enable
1	spm_en	**Enables scpsys reset** 0: Disable 1: Enable
0	spm_thermal_en	**Enables scpsys thermal reset** 0: Disable 1: Enable

10007034 **TOPRGU_WDT_REQ_IRQ_EN** **Reset Request IRQ Enable Register** **443C0003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key												debug_irq	thermal_ctl_irq		
Type	WO												RW	RW		
Reset	0	1	0	0	0	1	0	0					1	1		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															scpsys_irq	thermal_irq
Type															RW	RW
Reset															1	1

Bit(s)	Name	Description
31:24	unlock_key	**Write 0x44 to unlock the write protection of this register.**
19	debug_irq	**Triggers IRQ instead of reset when debugsys reset is enabled** 0: Trigger reset 1: Trigger IRQ
18	thermal_ctl_irq	**Triggers IRQ instead of reset when thermal controller reset is enabled** 0: Trigger reset 1: Trigger IRQ
1	scpsys_irq	**Triggers IRQ instead of reset when scpsys reset is enabled** 0: Trigger reset 1: Trigger IRQ
		Triggers IRQ instead of reset when scpsys thermal reset is enabled 0: Trigger reset 1: Trigger IRQ

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10007040 TOPRGU_WDT_DEBUG_CTL Debug Control Register FFFE00F1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key														ddr_sref_sta	ddr_reserve_sta
Type	WO														RU	RO
Reset	0	1	0	1	1	0	0	1							z	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						rg_dramc_conf_iso	rg_dramc_iso	rg_dramc_sref	rg_dramc_timeout						rg_mcu_lath_en	rg_ddr_protect_en
Type						RW	RW	RW	RW						RW	RW
Reset						0	0	0	1	1	1	1			0	1

Bit(s)	Name	Description
31:24	unlock_key	**Write 0x59 to unlock the write protection of this register**
17	ddr_sref_sta	**Indicates the current DDR status** 0: Currently not in self-refresh mode 1: Currently in self-refresh mode
16	ddr_reserve_sta	**Indicates ddr_reserve_mode is successful** 0: Failed 1: Succeed
10	rg_dramc_conf_iso	**ddr_reserve_mode related register**
9	rg_dramc_iso	**ddr_reserve_mode related register**
8	rg_dramc_sref	**ddr_reserve_mode related register**
7:4	rg_dramc_timeout	**ddr_reserve_mode related register**
1	rg_mcu_lath_en	
0	rg_ddr_protect_en	**Enables ddr_protect_mode** When ddr_reserve_mode is enabled, ddr_protect_en will be over-ridden automatically. 0: Disable 1: Enable

10007050 TOPRGU_WDT_INTERCORE_SYNC Intercore Sync Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_intercore_sync[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_intercore_sync[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	rg_intercore_sync	Register for using intercore sync

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10007054 **TOPRGU_WDT_INTERCORE_SYNC_SET** **Set Control of Intercore Sync Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_intercore_sync_set[31:16]															
Type	Other															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_intercore_sync_set[15:0]															
Type	Other															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	rg_intercore_sync_set	Sets 1'b1 to the corresponding bit of rg_intercore_sync

10007058 **TOPRGU_WDT_INTERCORE_SYNC_CLR** **Clear Control of Intercore Sync Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_intercore_sync_clr[31:16]															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_intercore_sync_clr[15:0]															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	rg_intercore_sync_clr	Sets 1'b0 to the corresponding bit of rg_intercore_sync

10007500 **TOPRGU_DEBUG_0_REG** **Shadow Register of WDT_MODE** **0000004D**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								shadow_wdt_cnt_reset_sel	shadow_ddr_reserve_mode	shadow_dual_mode	shadow_irq_lvl_en	shadow_wdt_restart_dummy_en	shadow_wdt_irq	shadow_ext_en	shadow_ext_pol	shadow_wdt_en
Type								RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset								0	0	1	0	0	1	1	0	1

Bit(s)	Name	Description
8	shadow_wdt_cnt_reset_sel	

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Bit(s)	Name	Description
7	shadow_ddr_reserve_mode	
6	shadow_dual_mode	
5	shadow_irq_lvl_en	
4	shadow_wdt_restart_dummy_en	
3	shadow_wdt_irq	
2	shadow_exten	
1	shadow_extpol	
0	shadow_wdt_en	

10007504 TOPRGU_DEBUG_1_REG Shadow Register of WDT_STA 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	shadow_hw_wdt_rst	shadow_sw_wdt_rst	shadow_irq_assert	shadow_security_rst									shadow_debug_rst			
Type	RO	RO	RO	RO									RO			
Reset	0	0	0	0									0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															shadow_spm_wdt_rst	shadow_thermal_rst
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
31	shadow_hw_wdt_rst	
30	shadow_sw_wdt_rst	
29	shadow_irq_assert	
28	shadow_security_rst	
19	shadow_debug_rst	
1	shadow_spm_wdt_rst	
0	shadow_thermal_rst	

10007508 TOPRGU_DEBUG_2_REG Shadow Register of WDT_DEBUG_CTL FFFE00F1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															shadow_ddr_sref_sta	shadow_ddr_reserve_sta
Type															RO	RO
Reset															z	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						rg_shadow	rg_shadow	rg_shadow	rg_shadow_dramc_timeout						rg_shadow	rg_shadow

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						_dramc_conf_iso	_dramc_iso	_dramc_sref							_mcu_lath_en	_ddr_protect_en
Type						RO	RO	RO	RO						RO	RO
Reset						0	0	0	1	1	1	1			0	1

Bit(s)	Name	Description
17	shadow_ddr_sref_sta	
16	shadow_ddr_reserve_sta	
10	rg_shadow_dramc_conf_iso	
9	rg_shadow_dramc_iso	
8	rg_shadow_dramc_sref	
7:4	rg_shadow_dramc_timeout	
1	rg_shadow_mcu_lath_en	
0	rg_shadow_ddr_protect_en	

1000750C **TOPRGU_DEBUG_3_REG** **Shadow Register of WDT_REQ_MODE** **003C0003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													shadow_debug_en	shadow_thermal_ctl_en		
Type													RO	RO		
Reset													1	1		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															shadow_scpsys_en	shadow_thermal_en
Type															RO	RO
Reset															1	1

Bit(s)	Name	Description
19	shadow_debug_en	
18	shadow_thermal_ctl_en	
1	shadow_scpsys_en	
0	shadow_thermal_en	

10007510 **TOPRGU_DEBUG_4_REG** **Shadow Register of WDT_REG_IRQ_EN** **003C0003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name													shadow_debug_irq	shadow_thermal_ctl_irq		
Type													RO	RO		
Reset													1	1		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															shadow_scpsys_irq	shadow_thermal_irq
Type															RO	RO
Reset															1	1

Bit(s)	Name	Description
19	shadow_debug_irq	
18	shadow_thermal_ctl_irq	
1	shadow_scpsys_irq	
0	shadow_thermal_irq	

Module name: TOPCKGEN Base address: (+10000000h)

Address	Name	Width	Register Function
10000310	TOPCKGEN_RESET_DEGLITCH_KEY	32	Reset Deglitch Enable Key Register

10000310 TOPCKGEN_RESET_DEGLITCH_KEY Reset Deglitch Enable Key Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dgrst_en_key[31:16]															
Type	RW															
Reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dgrst_en_key[15:0]															
Type	RW															
Reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit(s)	Name	Description
31:0	dgrst_en_key	Writes 0x67D2_A357 to enable reset deglitch

4.2.5 Programming Guide

4.2.5.1 TOPRGU Initial

Enable dual mode reset when TOPRGU is first initialized. Because WDT_MODE will not be reset and the dual mode will be disabled if system reset is triggered through WDT_SWRST, these registers will only be reset by SYSRSTB.

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The following registers will not be reset by TOPRGU.

- WDT_MODE
- WDT_STA
- WDT_NONRST_REG
- WDT_NONRST_REG2
- WDT_REQ_MODE
- WDT_REQ_IRQ_EN
- WDT_DEBUG_CTL

4.2.5.2 Watchdog Timer

- Trigger WDT_RESTART right after WDT_LENGTH is updated.
- WDT_SWRST can be triggered without wdt_en set to 1'b1.
- It is recommended to trigger WDT_RESTART before setting wdt_en to 1'b1.

4.2.5.3 IRQ Mode

Dual mode reset is default on. Therefore, all reset requests are default with IRQ mode enabled. This means the interrupt is triggered instead of triggering system reset immediately. If you would like to trigger system reset instead of interrupt, change the corresponding configuration of each reset request.

Each reset request can be configured as reset or IRQ separately.

4.2.5.4 MDSYS and CONNSYS Watchdog Timout

MDSYS and CONNSYS have their own watchdog timer. When their watchdog timers expire, they notify AP through interrupts. AP then asserts software reset to MDSYS or CONNSYS.

- MDSYS
  - Enable bus protection to/from MDSYS.
  - Set md_rst = 1'b1.
  - Wait for 2T 32kHz then set md_rst = 1'b0.
  - Disable bus protection to/from MDSYS.
  - Set up MDSYS boot slave.
  - Inform MDSYS abnormal reset via CCIF after MDSYS is ready.

- CONSYS
  - conn_rst = 1'b1
  - Wait for 2T 32kHz then set conn_rst = 1'b0.

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4.2.5.5 Dual Mode Reset

Dual mode reset is system reset after TOPRGU triggers interrupt. The watchdog timer needs to be enabled to complete this function.

In this mode, the watchdog timer will be ***AUTO-RESTART*** after interrupt is triggered. AP needs to clear WDT_STA after receiving interrupt from TOPRGU, or system reset will be triggered after watchdog timer expires.

- Set wdt_en = 1'b1.
- Set dual_mode = 1'b1.
- Set wdt_irq, thermal_irq, scpsys_irq or debug_irq to 1'b1.

4.2.5.6 DDR Protect

DDR protect (rg_ddr_protect_en) is useless when DDR reserved mode is enabled.

4.2.5.7 DDR Reserved Mode Reset

DDR reserved mode keeps data in DDR during system reset. In order to complete this function, DRAMC, DRMC_CONF, DDRPHY_CONF and EMI_CONF (optional) will not be reset.

- Enable DDR reserved mode when initializing TOPRGU.
- Wait for system reset to be triggered.
- [Optional] Check DDR reserved mode status (ddr_reserve_sta).
- After system reset, release DRAMC_CONF protect (set rg_dramc_conf_iso = 1'b0).
- Ensure related clocks of EMI, DRAMC, DDRPHY are ready (including PLL).
- Wait for dramc_sref_sta = 1'b1.
- Release DRAMC protect (set rg_dramc_iso = 1'b0).
- Release DRAMC self-refresh control (set rg_dramc_sref = 1'b0).
- Wait for dramc_sref_sta = 1'b0.

4.2.5.8 History

- EXT RESET is for NAND and PMIC, but there is exception.
  - MT6329 needs to disable WDT_MODE[2].
- WDT_LENGTH needs to be reset, or SYSTEM will enter RESET loop if WDT_LENGTH has been set to very short before reset trigger.

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4.3 PMIC Wrapper

4.3.1 Introduction

The PMIC wrapper is the bridge for communication between AP and PMIC.

4.3.2 Features

- Fast auto SPI format generator for PMIC register read/write
- APB3.0 bus lock scheme when SPI is busy
- Manual SPI format generator
- Supports access to dual PMICs
- Single and dual I/O SPI mode support for PMIC
- Single IO mode support only for Switching Charger
- Separated frequency between controller and SPI

4.3.3 Block Diagram

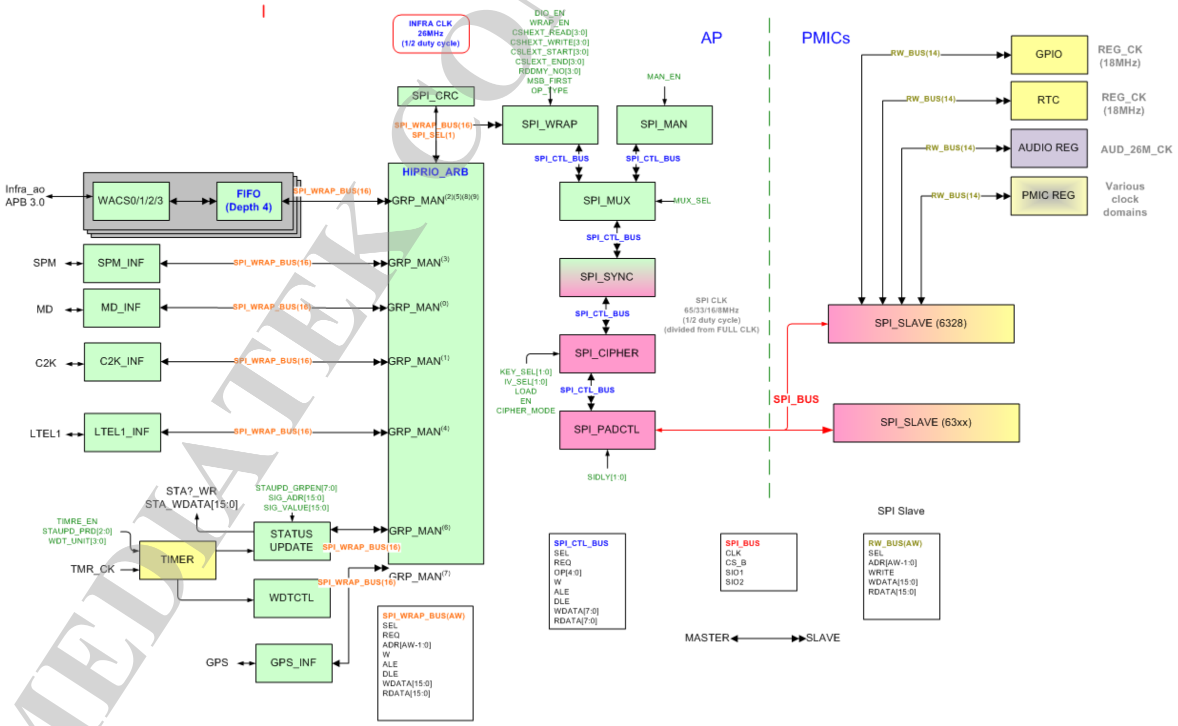

Figure 4-7. PMIC_WRAP architecture

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4.3.4 Register Definition

Module name: PMIC_WRAP Base address: (+10001000h)

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Address	Name	Width	Register Function
10001000	MUX_SEL	8	SPI MUX Selection
10001004	WRAP_EN	8	SPI Wrapper Enable
10001008	DIO_EN	8	Dual I/O Mode Enable of MT63xx
1000100C	SIDLY	8	Serial Input Delay
10001010	RDDMY	8	Read Dummy Cycle Number of MT63xx
10001014	SI_CK_CON	8	SI Enable Delay
10001018	CSHEXT_WRITE	8	CS High Extension - Write
1000101C	CSHEXT_READ	8	CS High Extension - Read
10001020	CSLEXT_START	8	CS Low Extension - Start
10001024	CSLEXT_END	8	CS Low Extension - End
10001028	STAUPD_PRD	8	Status Update Control Register
1000102C	STAUPD_GRPEN	8	Status Update Group Enable
10001030	EINT_STA0_ADR	16	Address of External Interrupt Status Register 0
10001034	EINT_STA1_ADR	16	Address of External Interrupt Status Register 1
10001038	EINT_STA	8	External Interrupt Status Register
1000103C	EINT_CLR	8	EINT Status Clear
10001040	STAUPD_MAN_TRIG	8	Status Update Manual Trigger
10001044	STAUPD_STA	16	Status Update Status
10001048	WRAP_STA	16	Wrapper Status
1000104C	HARB_INIT	8	Arbiter Initialization
10001050	HARB_HPRIO	32	Arbiter Priority Setting
10001054	HIPRIO_ARB_EN	32	Arbiter Source Enables
10001058	HARB_STA0	32	High Priority Arbiter Status 0
1000105C	HARB_STA1	32	High Priority Arbiter Status 1
10001060	MAN_EN	8	SPI Manual Mode Enable
10001064	MAN_CMD	16	Manual Command
10001068	MAN_RDATA	16	Manual Read Data
1000106C	MAN_VLDCLR	8	Manual Valid Clear
10001070	WACS0_EN	8	Wrapper Access (#0) Enable
10001074	INIT_DONE0	8	Initialization Done
10001078	WACS0_CMD	32	Wrapper Access (#0) Command
1000107C	WACS0_RDATA	32	Wrapper Access (#0) Read Data
10001080	WACS0_VLDCLR	8	Wrapper Access (#0) Valid Clear
10001084	WACS1_EN	8	Wrapper Access (#1) Enable
10001088	INIT_DONE1	8	Initialization Done
1000108C	WACS1_CMD	32	Wrapper Access (#1) Command
10001090	WACS1_RDATA	32	Wrapper Access (#1) Read Data
10001094	WACS1_VLDCLR	8	Wrapper Access (#1) Valid Clear
10001098	WACS2_EN	8	Wrapper Access (#2) Enable
1000109C	INIT_DONE2	8	Initialization Done
100010A0	WACS2_CMD	32	Wrapper Access (#2) Command
100010A4	WACS2_RDATA	32	Wrapper Access (#2) Read Data
100010A8	WACS2_VLDCLR	8	Wrapper Access (#2) Valid Clear
100010AC	WACS3_EN	8	Wrapper Access (#3) Enable
100010B0	INIT_DONE3	8	Initialization Done

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Address	Name	Width	Register Function
100010B4	WACS3_CMD	32	Wrapper Access (#3) Command
100010B8	WACS3_RDATA	32	Wrapper Access (#3) Read Data
100010BC	WACS3_VLDCLR	8	Wrapper Access (#3) Valid Clear
100010C0	INT_EN	32	Interrupt Enable
100010C4	INT_FLG_RAW	32	Interrupt Flags - Raw
100010C8	INT_FLG	32	Interrupt Flags
100010CC	INT_CLR	32	Interrupt Clear
100010D0	SIG_ADR	32	Signature Address in MT6332
100010D4	SIG_MODE	8	Signature Checking Mode in MT6332
100010D8	SIG_VALUE	32	Signature Value in MT6332
100010DC	SIG_ERRVAL	32	Error Signature Value in MT6332
100010E0	CRC_EN	8	CRC Enable
100010E4	TIMER_EN	16	Timer Enable
100010E8	TIMER_STA	32	Timer Status
100010EC	WDT_UNIT	8	Watchdog Timer Unit
100010F0	WDT_SRC_EN	32	Watchdog Timer Source Enable
100010F4	WDT_FLG	32	Watchdog Flag
100010F8	DEBUG_INT_SEL	8	Debug Interrupt Selection
100010FC	DVFS_ADR0	16	DVFS Command #0 - Address
10001100	DVFS_WDATA0	16	DVFS Command #0 - Write Data
10001104	DVFS_ADR1	16	DVFS Command #1 - Address
10001108	DVFS_WDATA1	16	DVFS Command #1 - Write Data
1000110C	DVFS_ADR2	16	DVFS Command #2 - Address
10001110	DVFS_WDATA2	16	DVFS Command #2 - Write Data
10001114	DVFS_ADR3	16	DVFS Command #3 - Address
10001118	DVFS_WDATA3	16	DVFS Command #3 - Write Data
1000111C	DVFS_ADR4	16	DVFS Command #4 - Address
10001120	DVFS_WDATA4	16	DVFS Command #4 - Write Data
10001124	DVFS_ADR5	16	DVFS Command #5 - Address
10001128	DVFS_WDATA5	16	DVFS Command #5 - Write Data
1000112C	DVFS_ADR6	16	DVFS Command #6 - Address
10001130	DVFS_WDATA6	16	DVFS Command #6 - Write Data
10001134	DVFS_ADR7	16	DVFS Command #7 - Address
10001138	DVFS_WDATA7	16	DVFS Command #7 - Write Data
1000113C	DVFS_ADR8	16	DVFS Command #8 - Address
10001140	DVFS_WDATA8	16	DVFS Command #8 - Write Data
10001144	DVFS_ADR9	16	DVFS Command #9 - Address
10001148	DVFS_WDATA9	16	DVFS Command #9 - Write Data
1000114C	DVFS_ADR10	16	DVFS Command #10 - Address
10001150	DVFS_WDATA10	16	DVFS Command #10 - Write Data
10001154	DVFS_ADR11	16	DVFS Command #11 - Address
10001158	DVFS_WDATA11	16	DVFS Command #11 - Write Data
1000115C	DVFS_ADR12	16	DVFS Command #12 - Address
10001160	DVFS_WDATA12	16	DVFS Command #12 - Write Data
10001164	DVFS_ADR13	16	DVFS Command #13 - Address
10001168	DVFS_WDATA13	16	DVFS Command #13 - Write Data

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Address	Name	Width	Register Function
1000116C	DVFS_ADR14	16	DVFS Command #14 - Address
10001170	DVFS_WDATA14	16	DVFS Command #14 - Write Data
10001174	DVFS_ADR15	16	DVFS Command #15 - Address
10001178	DVFS_WDATA15	16	DVFS Command #15 - Write Data
1000117C	SPMINF_STA	16	SPM Interface Status Register
10001180	CIPHER_KEY_SEL	8	CIPHER Key Selection
10001184	CIPHER_IV_SEL	8	CIPHER Initial Vector Selection
10001188	CIPHER_EN	8	CIPHER Engine Enable
1000118C	CIPHER_RDY	8	CIPHER Data Ready
10001190	CIPHER_MODE	8	CIPHER Mode Enable
10001194	CIPHER_SWRST	8	CIPHER Soft Reset
10001198	DCM_EN	8	Internal DCM Enable
1000119C	DCM_DBC_PRD	8	Debounce Period at Entering DCM Mode
100011A0	EXT_CK	8	Extra Clock Number
100011A4	ADC_CMD_ADDR	16	AUXADC Command Register Address
100011A8	PWRAP_ADC_CMD	16	Command to AUXADC
100011AC	ADC_RDATA_ADDR	16	Address of Thermal Data [15:0] Register in AUXADC
100011B0	GPS_STA	32	GPS Interface Status (Debug)
100011B4	SWRST	8	Software Reset
100011B8	MD_ADC_RDATA_ADDR_LATEST	16	Address of the Latest Thermal Data [15:0] Register in AUXADC
100011BC	MD_ADC_RDATA_ADDR_WP	16	Address of the Latest Buffer Thermal Data Pointer
100011C0	MD_ADC_RDATA_ADDR0	16	Address of the Buffer Thermal Data 0
100011C4	MD_ADC_RDATA_ADDR1	16	Address of the Buffer Thermal Data 1
100011C8	MD_ADC_RDATA_ADDR2	16	Address of the Buffer Thermal Data 2
100011CC	MD_ADC_RDATA_ADDR3	16	Address of the Buffer Thermal Data 3
100011D0	MD_ADC_RDATA_ADDR4	16	Address of the Buffer Thermal Data 4
100011D4	MD_ADC_RDATA_ADDR5	16	Address of the Buffer Thermal Data 5
100011D8	MD_ADC_RDATA_ADDR6	16	Address of the Buffer Thermal Data 6
100011DC	MD_ADC_RDATA_ADDR7	16	Address of the Buffer Thermal Data 7
100011E0	MD_ADC_RDATA_ADDR8	16	Address of the Buffer Thermal Data 8
100011E4	MD_ADC_RDATA_ADDR9	16	Address of the Buffer Thermal Data 9
100011E8	MD_ADC_RDATA_ADDR10	16	Address of the Buffer Thermal Data 10
100011EC	MD_ADC_RDATA_ADDR11	16	Address of the Buffer Thermal Data 11
100011F0	MD_ADC_RDATA_ADDR12	16	Address of the Buffer Thermal Data 12

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Address	Name	Width	Register Function
100011F4	MD_ADC_RDATA_ADDR13	16	Address of the Buffer Thermal Data 13
100011F8	MD_ADC_RDATA_ADDR14	16	Address of the Buffer Thermal Data 14
100011FC	MD_ADC_RDATA_ADDR15	16	Address of the Buffer Thermal Data 15
10001200	MD_ADC_RDATA_ADDR16	16	Address of the Buffer Thermal Data 16
10001204	MD_ADC_RDATA_ADDR17	16	Address of the Buffer Thermal Data 17
10001208	MD_ADC_RDATA_ADDR18	16	Address of the Buffer Thermal Data 18
1000120C	MD_ADC_RDATA_ADDR19	16	Address of the Buffer Thermal Data 19
10001210	MD_ADC_RDATA_ADDR20	16	Address of the Buffer Thermal Data 20
10001214	MD_ADC_RDATA_ADDR21	16	Address of the Buffer Thermal Data 21
10001218	MD_ADC_RDATA_ADDR22	16	Address of the Buffer Thermal Data 22
1000121C	MD_ADC_RDATA_ADDR23	16	Address of the Buffer Thermal Data 23
10001220	MD_ADC_RDATA_ADDR24	16	Address of the Buffer Thermal Data 24
10001224	MD_ADC_RDATA_ADDR25	16	Address of the Buffer Thermal Data 25
10001228	MD_ADC_RDATA_ADDR26	16	Address of the Buffer Thermal Data 26
1000122C	MD_ADC_RDATA_ADDR27	16	Address of the Buffer Thermal Data 27
10001230	MD_ADC_RDATA_ADDR28	16	Address of the Buffer Thermal Data 28
10001234	MD_ADC_RDATA_ADDR29	16	Address of the Buffer Thermal Data 29
10001238	MD_ADC_RDATA_ADDR30	16	Address of the Buffer Thermal Data 30
1000123C	MD_ADC_RDATA_ADDR31	16	Address of the Buffer Thermal Data 31
10001240	MD_ADC_STA0	32	MD_AUXADC Interface Status 0 (Debug)
10001244	MD_ADC_STA1	32	MD_AUXADC Interface Status 1 (Debug)
10001248	MD_ADC_STA2	32	MD_AUXADC Interface Status 2 (Debug)

10001000 MUX_SEL SPI MUX Selection 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MUX_SEL
Type																RW
Reset																0

Bit(s)	Name	Description
0	MUX_SEL	**Selects SPI controller source**

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Bit(s)	Name	Description
		0: SPI is controlled by automatic wrapper 1: SPI is controlled in manual mode.

10001004 WRAP_EN SPI Wrapper Enable 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																WRAP_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	WRAP_EN	**Automatic wrapper circuit enabling switch.** 0: Wrapper circuit is disabled, but the current transaction will be finished. 1: Wrapper circuit is enabled, and new request can be accepted once wrapper is available

10001008 DIO_EN Dual I/O Mode Enable of MT63xx 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															DIO_EN1	DIO_EN0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	DIO_EN1	**SPI dual I/O mode feature enabling switch for PMIC1** 0: Disable SPI dual I/O mode 1: Enable SPI dual I/O mode
0	DIO_EN0	**SPI dual I/O mode feature enabling switch for PMIC0** 0: Disable SPI dual I/O mode 1: Enable SPI dual I/O mode

1000100C SIDLY Serial Input Delay 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SIDLY	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	SIDLY	**Controls SPI input data strobe timing** The default setting (0ns) corresponds to the strobing at rising edge of SPI CLK. 0: Delay 0ns 1: Delay 2ns 2: Delay 4ns 3: Delay 6ns

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10001010 RDDMY Read Dummy Cycle Number of MT63xx FF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RDDMY1				RDDMY0			
Type									RW				RW			
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:4	RDDMY1	**Applies (1+RDDMY1[3:0])T of dummy read cycles before read data phase** This setting should be in accordance with the one in slave. The max dummy cycle is 16T.
3:0	RDDMY0	**Applies (1+RDDMY0[3:0])T of dummy read cycles before read data phase** This setting should be in accordance with the one in slave. The max. dummy cycle is 16T.

10001014 SI_CK_CON SI Enable Delay 01

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														SI_EN_SEL		SI_CK_SEL
Type														RW		RW
Reset														0	0	1

Bit(s)	Name	Description
2:1	SI_EN_SEL	**Controls SI enabling timing** T is the period of SPI CLK. 00: Delay 0T 01: Delay 1T 10: Delay 2T 11: Disable SI_EN
0	SI_CK_SEL	0: Choose inverted SPI CLK 1: Choose SPI CLK

10001018 CSHEXT_WRITE CS High Extension - Write 0F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CSHEXT_WRITE							
Type									RW							
Reset									0	0	0	0	1	1	1	1

Bit(s)	Name	Description
7:0	CSHEXT_WRITE	**After finishing a write transaction, extends CS high time to be at least (1+CSHEXT_WRITE[3:0])T of SPI CLK** Applied to the CS high time between ADR and DATA of a write transaction.

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1000101C CSHEXT_READ CS High Extension - Read 0F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CSHEXT_READ							
Type									RW							
Reset									0	0	0	0	1	1	1	1

Bit(s)	Name	Description
7:0	CSHEXT_READ	**After finishing a read transaction, extends CS high time to be at least (1+CSHEXT_READ[3:0])T of SPI CLK** Applied to the CS high time between ADR and DATA of a read transaction.

10001020 CSLEXT_START CS Low Extension - Start 0F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CSLEXT_START			
Type													RW			
Reset													1	1	1	1

Bit(s)	Name	Description
3:0	CSLEXT_START	Extends CS low time after CSL command to be at least (1.5+CSLEXT_START[3:0])T of SPI CLK

10001024 CSLEXT_END CS Low Extension - End 0F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CSLEXT_END			
Type													RW			
Reset													1	1	1	1

Bit(s)	Name	Description
3:0	CSLEXT_END	Extends CS low time before CSH command to be at least (1.5+CSLEXT_END[3:0])T of SPI CLK

10001028 STAUPD_PRD Status Update Control Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													STAUPD_PRD			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	STAUPD_PRD	**Selects periodic status update timing (period)** This status will be updated every selected time period. Unit: 19.7us 0: Disable 1: 19.7us

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Bit(s)	Name	Description
		2: 39.4us 5: 98.5us 15: 295.5us

1000102C STAUPD_GRPEN Status Update Group Enable 0C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									STAUPD_GRPEN							
Type									RW							
Reset									0	0	0	0	1	1	0	0

Bit(s)	Name	Description
7:0	STAUPD_GRPEN	**Enables switch for each status update group** [0]: Signature from MT6328 [1]: Signature from MT63xx [2]: Interrupt Status from MT6328 [3]: Interrupt Status from MT63xx [4]: read data from MT6328 for MD [5]: read data from MT6328 for GPS

10001030 EINT_STA0_ADR Address of External Interrupt Status Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_STA0_ADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	EINT_STA0_ADR	Specifies address of interrupt status in MT6328

10001034 EINT_STA1_ADR Address of External Interrupt Status Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_STA1_ADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	EINT_STA1_ADR	Specifies address of interrupt status in MT63xx

10001038 EINT_STA External Interrupt Status Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													EINT_STA			
Type													RO			
Reset													0	0	0	0

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Bit(s)	Name	Description
3:0	EINT_STA	**Records external interrupt status** [0]: CPU IRQ status in MT6328 [1]: MD32 IRQ status in MT6328 [2]: CPU IRQ status in MT63xx [3]: RESERVED

1000103C EINT_CLR EINT Status Clear 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													EINT_CLR			
Type													WO			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	EINT_CLR	**Write 1 to the corresponding bit to clear the EINT status flag.** For example, write 4'b0100 to clear bit 2 (CPU IRQ status in MT6332).

10001040 STAUPD_MAN_TRIG Status Update Manual Trigger 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STAUPD_MAN_TRIG
Type																WO
Reset																0

Bit(s)	Name	Description
0	STAUPD_MAN_TRIG	Set to 1 to manually trigger the status update circuit

10001044 STAUPD_STA Status Update Status 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								STAUPD_FSM			STAUPD_ALE_CNT			STAUPD_DLE_CNT		
Type								RU			RU			RU		
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:6	STAUPD_FSM	**Current STAUPD FSM state** 0: IDLE 2: REQ 4: WFDLE
5:3	STAUPD_ALE_CNT	**Request count every time STAUPD is triggered.** For every period of STAUPD_PRD, 4 status update request will be triggered.

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Bit(s)	Name	Description
2:0	STAUPD_DLE_CNT	**Read data count every time STAUPD is triggered.** For every period of STAUPD_PRD, 4 status will be received after requests have been sent.

10001048 WRAP_STA Wrapper Status 0280

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		WRAP_FSM				AG_WRAP_REQ	AG_WRAP_W	WRAP_CH_REQ	WRAP_CH_W	WRAP_AG_DLE_RESTCNT		WRAP_CH_ALE_RESTCNT		WRAP_CH_DLE_RESTCNT		
Type		RU				RU	RU	RU	RU	RU		RU		RU		
Reset		0	0	0	0	0	1	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:11	WRAP_FSM	**Current wrapper FSM states** 0x0: IDLE 0x2: CSL_ADR_START 0x4: ADR 0x6: CSL_ADR_END 0x8: CSH_ADR 0xA: CSL_DATA_START 0xC: DATA 0xE: CSL_DATA_END 0xF: CSH_DATA Others: Reserved
10	AG_WRAP_REQ	**Current WRAP request indicator**
9	AG_WRAP_W	**Current WRAP read/write direction**
8	WRAP_CH_REQ	**Current SPI request indicator**
7	WRAP_CH_W	**Current SPI read/write direction** 0: Read 1: Write
6:5	WRAP_AG_DLE_RESTCNT	**Remaining WRAP request counter for wrapper**
4:3	WRAP_CH_ALE_RESTCNT	**Remaining SPI request counter for wrapper**
2:0	WRAP_CH_DLE_RESTCNT	**Remaining SPI read data counter for wrapper**

1000104C HARB_INIT Arbiter Initialization 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																HARB_INIT
Type																RW
Reset																0

Bit(s)	Name	Description
0	HARB_INIT	**Clears high-priority arbiter internal registers to initial value** 0: Normal state. 1: Set up arbiter in initialized state.

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10001050 **HARB_HPRIO** **Arbiter Priority Setting** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							HARB_HPRIO									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	HARB_HPRIO	**Sets high priority to the corresponding request** The pre-defined priority is 0 > 1 > 2, ..., i.e. request from agent 0 has the highest priority. However, by setting up the corresponding bit of HARB_HPRIO[5:0] to 1, the priority can be raised higher. Request with the corresponding HARB_HPRIO bit being 1 has higher priority than other requests with the corresponding HARB_HPRIO=0. For requests with the HARB_HPRIO bits set to 1, the priority is still 0 > 1 > 2 >, ... [9]: WACS3 (C2K SW) [8]: STAUPD [7]: MD_ADCINF [6]: GPSINF [5]: WACS1 (reserved) [4]: WACS2 (AP SW) [3]: DVFSINF (SPMINF) [2]: WACS0 (MDSW) [1]: C2kINF [0]: MDINF

10001054 **HIPRIO_ARB_EN** **Arbiter Source Enables** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							HIPRIO_ARB_EN									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	HIPRIO_ARB_EN	**Enables HIPRIO_ARB for each source** [9]: WACS3 (C2K SW) [8]: STAUPD [7]: MD_ADCINF [6]: GPSINF [5]: WACS1 (reserved) [4]: WACS2 (AP SW) [3]: DVFSINF (SPMINF) [2]: WACS0 (MDSW) [1]: C2kINF [0]: MDINF 0: Disable

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Bit(s)	Name	Description
		1: Enable

10001058 HARB_STA0 High Priority Arbiter Status 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HARB_WRAP_REQ	HARB_WRAP_ADR														
Type	RU	RU														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HARB_WRAP_WDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	HARB_WRAP_REQ	
30:16	HARB_WRAP_ADR	
15:0	HARB_WRAP_WDATA	

1000105C HARB_STA1 High Priority Arbiter Status 1 02000005

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HARB_WRAP_REQ0	HARB_WRAP_W	AG_HARB_REQ[9:1]								
Type						RU	RU	RU								
Reset						0	1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AG_HARB_REQ[0:0]	HARB_DLE_RESTCNT				HARB_OWN				HARB_DLE_OWN				HARB_VLD	HARB_DLE_FULL	HARB_DLE_EMPTY
Type	RU	RU				RU				RU				RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit(s)	Name	Description
26	HARB_WRAP_REQ0	
25	HARB_WRAP_W	0: Read 1: Write
24:15	AG_HARB_REQ	
14:11	HARB_DLE_RESTCNT	
10:7	HARB_OWN	
6:3	HARB_DLE_OWN	
2	HARB_VLD	

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Bit(s)	Name	Description
1	HARB_DLE_FULL	
0	HARB_DLE_EMPTY	

10001060 MAN_EN SPI Manual Mode Enable 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MAN_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	MAN_EN	**Manual mode circuit enabling switch.** 0: Disable Manual mode circuit 1: Enable Manual mode circuit

10001064 MAN_CMD Manual Command 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			SPI_W	SPI_OP					SPI_WDATA							
Type			RW	RW					RW							
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13	SPI_W	**SPI command: Read/write direction** 0: Read 1: Write
12:8	SPI_OP	**SPI command: Operation code** 0x0: OP_CSH 0x1: OP_CSL 0x8: OP_OUTS 0x9: OP_OUTD 0xC: OP_INS 0xE: OP_IND
7:0	SPI_WDATA	**SPI command: Write data**

10001068 MAN_RDATA Manual Read Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					MAN_REQ	MAN_FSM			MAN_RDATA							
Type					RU	RU			RU							
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	MAN_REQ	**Manual request indicator.**

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Bit(s)	Name	Description
		0: No MAN request is awaiting grant. 1: One MAN Request is still awaiting grant.
10:8	MAN_FSM	**Current MAN FSM states.** 0x0: IDLE 0x2: REQ. Request in process 0x4: WFDLE. Wait for read data 0x6: WFVLDCLR. Wait for valid flag clearing Others: Reserved
7:0	MAN_RDATA	**Received read data in buffer.** SW must check if MAN_FSM equals to WFVLDCLR before reads MAN_RDATA.

1000106C **MAN_VLDCLR** **Manual Valid Clear** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MAN_VLDCLR
Type																WO
Reset																0

Bit(s)	Name	Description
0	MAN_VLDCLR	**Write 1 to clear valid flag.** 0: Disable 1: Enable

10001070 **WACS0_EN** **Wrapper Access (#0) Enable** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																WACS0_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	WACS0_EN	**Enables wrapper access** Set to disable will reset the FSM. 0: Disable 1: Enable

10001074 **INIT_DONE0** **Initialization Done** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INIT_DONE0
Type																RW
Reset																0

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Bit(s)	Name	Description
0	INIT_DONE0	**Indicates initialization is finished** During SPI transactions, if this bit is detected low, then current transaction may fail, which requires re-do or debugging. 0: Initialization is not yet finished. 1: Initialization is finished.

10001078 **WACS0_CMD** **Wrapper Access (#0) Command** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WACS0_WRITE	WACS0_ADR														
Type	RW	RW														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WACS0_WDATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	WACS0_WRITE	**Wrapper access: Read/write direction** 0: Read 1: Write
30:16	WACS0_ADR	**Wrapper access: Address[15:1]**
15:0	WACS0_WDATA	**Wrapper access: Write data[15:0]**

1000107C **WACS0_RDATA** **Wrapper Access (#0) Read Data** **80500000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WACS0_FIFO_FREECNT				WACS0_FIFO_FILLCNT					SYS_IDLE0	INIT_DONE0	SYNC_IDLE0	WACS0_REQ	WACS0_FSM		
Type	RU				RU					RU	RU	RU	RU	RU		
Reset	1	0	0	0	0	0	0	0		1	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WACS0_RDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	WACS0_FIFO_FREECNT	**Records the number of data can be filled into FIFO**
27:24	WACS0_FIFO_FILLCNT	**Records the number of data filled into FIFO**
22	SYS_IDLE0	**PMIC_WRAP busy status indicator** 1: WACS 0/1/2 idle 2: No arbiter request 3: No spi_wrap to mux request 4: No waiting read data

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Bit(s)	Name	Description
		5: spi_man is idle. 6: spi_sync is idle. 0: PMIC_WRAP is busy 1: PMIC_WRAP is IDLE
21	INIT_DONE0	**Indicates initialization is finished** During SPI transactions, if this bit is detected low, then current transaction may fail, which requires re-do or debugging. (This is equivalent to INIT_DONE) 0: Initialization is not yet finished 1: Initialization is finished.
20	SYNC_IDLE0	**SYNC module busy status** It is used to judge if the request has reached SYNC module. 0: SYNC module is busy 1: SYNC module is IDLE
19	WACS0_REQ	**Wrapper access request indicator** 0: No WACS request is awaiting grant. 1: One WACS Request is still awaiting grant.
18:16	WACS0_FSM	**Current WACS FSM states** 0x0: IDLE 0x2: REQ. Request in process 0x4: WFDLE. Wait for read data 0x6: WFVLDCLR. Wait for valid flag clearing Others: Reserved
15:0	WACS0_RDATA	**Wrapper Access: read data** SW must check if valid flag equals to 1 before using this read data.

10001080 **WACS0_VLDCLR** **Wrapper Access (#0) Valid Clear** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																WACS0_VLDCLR
Type																WO
Reset																0

Bit(s)	Name	Description
0	WACS0_VLDCLR	Write 1 to clear valid flag.

10001084 **WACS1_EN** **Wrapper Access (#1) Enable** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																WACS1_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	WACS1_EN	**Enables wrapper access** Set to disable will reset the FSM.

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Bit(s)	Name	Description
		0: Disable 1: Enable

10001088 INIT_DONE1 Initialization Done 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INIT_DONE1
Type																RW
Reset																0

Bit(s)	Name	Description
0	INIT_DONE1	**Indicates initialization is finished** During SPI transactions, if this bit is detected low, then current transaction may fail, which requires re-do or debugging. 0: Initialization is not yet finished. 1: Initialization is finished.

1000108C WACS1_CMD Wrapper Access (#1) Command 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WACS1_WRITE	WACS1_ADR														
Type	RW	RW														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WACS1_WDATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	WACS1_WRITE	**Wrapper access: Read/write direction** 0: Read 1: Write
30:16	WACS1_ADR	**Wrapper access: Address[15:1]**
15:0	WACS1_WDATA	**Wrapper access: Write data[15:0]**

10001090 WACS1_RDATA Wrapper Access (#1) Read Data 80500000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WACS1_FIFO_FREECNT				WACS1_FIFO_FILLCNT					SYS_IDLE1	INIT_DONE1	SYNC_IDLE1	WACS1_REQ	WACS1_FSM		
Type	RU				RU					RU	RU	RU	RU	RU		
Reset	1	0	0	0	0	0	0	0		1	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WACS1_RDATA															

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Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	WACS1_FIFO_FRECNT	**Records the number of data can be filled into FIFO**
27:24	WACS1_FIFO_FILLCNT	**Records the number of data filled into FIFO**
22	SYS_IDLE1	**PMIC_WRAP busy status indicator** 1: WACS 0/1/2 idle 2: No arbiter request 3: No spi_wrap to mux request 4: No waiting read data 5: spi_man is idle. 6: spi_sync is idle. 0: PMIC_WRAP is busy 1: PMIC_WRAP is IDLE
21	INIT_DONE1	**Indicates initialization is finished.** During SPI transactions, if this bit is detected low, then current transaction may fail, which requires re-do or debugging. (This is equivalent to INIT_DONE) 0: Initialization is not yet finished 1: Initialization is finished.
20	SYNC_IDLE1	**SYNC module busy status.** It is used to judge if the request has reached SYNC module. 0: SYNC module is busy 1: SYNC module is IDLE
19	WACS1_REQ	**Wrapper access request indicator.** 0: No WACS request is awaiting grant. 1: One WACS Request is still awaiting grant.
18:16	WACS1_FSM	**Current WACS FSM states.** 0x0: IDLE 0x2: REQ. Request in process 0x4: WFDLE. Wait for read data 0x6: WFVLDCLR. Wait for valid flag clearing Others: Reserved
15:0	WACS1_RDATA	**Wrapper Access: read data.** SW must check if valid flag equals to 1 before using this read data.

10001094 **WACS1_VLDCLR** **Wrapper Access (#1) Valid Clear** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**WACS1_VLDCLR**
Type																WO
Reset																0

Bit(s)	Name	Description
0	WACS1_VLDCLR	Write 1 to clear valid flag.

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10001098 WACS2_EN Wrapper Access (#2) Enable 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																WACS2_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	WACS2_EN	**Enables wrapper access** Set to disable will reset the FSM. 0: Disable 1: Enable

1000109C INIT_DONE2 Initialization Done 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INIT_DONE2
Type																RW
Reset																0

Bit(s)	Name	Description
0	INIT_DONE2	**Indicates initialization is finished** During SPI transactions, if this bit is detected low, then current transaction may fail, which requires re-do or debugging. 0: Initialization is not yet finished. 1: Initialization is finished.

100010A0 WACS2_CMD Wrapper Access (#2) Command 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WACS2_WRITE	WACS2_ADR														
Type	RW	RW														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WACS2_WDATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	WACS2_WRITE	**Wrapper access: Read/write direction** 0: Read 1: Write
30:16	WACS2_ADR	**Wrapper access: Address[15:1]**
15:0	WACS2_WDATA	**Wrapper access: Write data[15:0]**

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100010A4 **WACS2_RDATA** **Wrapper Access (#2) Read Data** **80500000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WACS2_FIFO_FREECNT				WACS2_FIFO_FILLCNT					SYS_IDLE2	INIT_DONE2	SYNC_IDLE2	WACS2_REQ	WACS2_FSM		
Type	RU				RU					RU	RU	RU	RU	RU		
Reset	1	0	0	0	0	0	0	0		1	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WACS2_RDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	WACS2_FIFO_FREECNT	**Records the number of data can be filled into FIFO**
27:24	WACS2_FIFO_FILLCNT	**Records the number of data filled into FIFO**
22	SYS_IDLE2	**PMIC_WRAP busy status indicator** 1: WACS 0/1/2 idle 2: No arbiter request 3: No spi_wrap to mux request 4: no waiting read data 5: spi_man is idle. 6: spi_sync is idle. 0: PMIC_WRAP is busy 1: PMIC_WRAP is IDLE
21	INIT_DONE2	**Indicates initialization is finished** During SPI transactions, if this bit is detected low, then current transaction may fail, which requires re-do or debugging. (This is equivalent to INIT_DONE) 0: Initialization is not yet finished 1: Initialization is finished.
20	SYNC_IDLE2	**SYNC module busy status** It is used to judge if the request has reached SYNC module. 0: SYNC module is busy 1: SYNC module is IDLE
19	WACS2_REQ	**Wrapper access request indicator** 0: No WACS request is awaiting grant. 1: One WACS Request is still awaiting grant.
18:16	WACS2_FSM	**Current WACS FSM states** 0x0: IDLE 0x2: REQ. Request in process 0x4: WFDLE. Wait for read data 0x6: WFVLDCLR. Wait for valid flag clearing Others: Reserved
15:0	WACS2_RDATA	**Wrapper Access: read data** SW must check if valid flag equals to 1 before using this read data.

100010A8 **WACS2_VLDCLR** **Wrapper Access (#2) Valid Clear** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name																WACS2_VLDCLR
Type																WO
Reset																0

Bit(s)	Name	Description
0	WACS2_VLDCLR	Write 1 to clear valid flag.

100010AC **WACS3_EN** **Wrapper Access (#3) Enable** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																WACS3_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	WACS3_EN	**Enables wrapper access** Set to disable will reset the FSM. 0: Disable 1: Enable

100010B0 **INIT_DONE3** **Initialization Done** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INIT_DONE3
Type																RW
Reset																0

Bit(s)	Name	Description
0	INIT_DONE3	**Indicates initialization is finished.** During SPI transactions, if this bit is detected low, then current transaction may fail, which requires re-do or debugging. 0: Initialization is not yet finished. 1: Initialization is finished.

100010B4 **WACS3_CMD** **Wrapper Access (#3) Command** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WACS3_WRITE	WACS3_ADR														
Type	RW	RW														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	WACS3_WDATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	WACS3_WRITE	**Wrapper access: Read/write direction** 0: Read 1: Write
30:16	WACS3_ADR	**Wrapper access: Address[15:1]**
15:0	WACS3_WDATA	**Wrapper access: Write data[15:0]**

100010B8 WACS3_RDATA Wrapper Access (#3) Read Data 80500000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WACS3_FIFO_FREECNT				WACS3_FIFO_FILLCNT					SYS_IDLE3	INIT_DONE3	SYNC_IDLE3	WACS3_REQ	WACS3_FSM		
Type	RU				RU					RU	RU	RU	RU	RU		
Reset	1	0	0	0	0	0	0	0		1	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WACS3_RDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	WACS3_FIFO_FREECNT	**Records the number of data can be filled into FIFO**
27:24	WACS3_FIFO_FILLCNT	**Records the number of data filled into FIFO**
22	SYS_IDLE3	**PMIC_WRAP busy status indicator** 1: WACS 0/1/2 idle 2: No arbiter request 3: No spi_wrap to mux request 4: No waiting read data 5: spi_man is idle. 6: spi_sync is idle. 0: PMIC_WRAP is busy 1: PMIC_WRAP is IDLE
21	INIT_DONE3	**Indicates initialization is finished** During SPI transactions, if this bit is detected low, then current transaction may fail, which requires re-do or debugging. (This is equivalent to INIT_DONE) 0: Initialization is not yet finished 1: Initialization is finished.
20	SYNC_IDLE3	**SYNC module busy status** It is used to judge if the request has reached SYNC module. 0: SYNC module is busy 1: SYNC module is IDLE
19	WACS3_REQ	**Wrapper access request indicator** 0: No WACS request is awaiting grant. 1: One WACS Request is still awaiting grant.
18:16	WACS3_FSM	**Current WACS FSM states** 0x0: IDLE 0x2: REQ. Request in process

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Bit(s)	Name	Description
		0x4: WFDLE. Wait for read data 0x6: WFVLDCLR. Wait for valid flag clearing Others: Reserved
15:0	WACS3_RDATA	**Wrapper Access: read data** SW must check if valid flag equals to 1 before using this read data.

100010BC **WACS3_VLD CLR** **Wrapper Access (#3) Valid Clear** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																WACS3_VLDCLR
Type																WO
Reset																0

Bit(s)	Name	Description
0	WACS3_VLDCLR	Write 1 to clear valid flag.

100010C0 **INT_EN** **Interrupt Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_EN[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT_EN[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT_EN	**Enables interrupt for each source** [31]: INIT_DATA_REQ_ERR: LTECO_CLOCK initial data request error [30]: INIT_FLOW_REQ_ERR: LTE CO_CLOCK initial flow request error [29]: WACS3_CMD_MISS: A WACS3 CMD is written while WACS3 is disabled [28]: WACS3_UNEXP_DLE: WACS3 unexpected DLE [27]: WACS3_UNEXP_VLDCLR: WACS3 unexpected VLDCLR [26]: C2K request errors occurs [25]: MD_ADC_DLE_CNT_OVF: MD_ADC DLE counter is overflowed [24]: MD_ADC_ALE_CNT_OVF: MD_ADC ALE counter is overflowed [23]: STAUPD_DLE_CNT_OVF: STAUPD DLE counter is overflowed. [22]: STAUPD_ALE_CNT_OVF: STAUPD ALE counter is overflowed. [21]: MDINF_REQ_ERR: Modem request error occurs [20]: WACS2_CMD_MISS: A WACS2 CMD is written while WACS2 is disabled. [19]: WACS2_UNEXP_DLE: WACS2 unexpected DLE [18]: WACS2_UNEXP_VLDCLR: WACS2 unexpected VLDCLR [17]: WACS1_CMD_MISS: A WACS1 CMD is written while WACS1 is disabled. [16]: WACS1_UNEXP_DLE: WACS1 unexpected DLE [15]: WACS1_UNEXP_VLDCLR: WACS1 unexpected VLDCLR [14]: WACS0_CMD_MISS: A WACS0 CMD is written while WACS0 is disabled.

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Bit(s)	Name	Description
		[13]: WACS0_UNEXP_DLE: WACS0 unexpected DLE [12]: WACS0_UNEXP_VLDCLR: WACS0 unexpected VLDCLR [11]: HARB_DLE_OVF: High priority arbiter DLE is overflowed. [10]: HARB_DLE_UNF: High priority arbiter DLE is underflowed. [9]: WRAP_AGDLE_OVF: WRAP agent DLE counter is overflowed. [8]: WRAP_AGDLE_UNF: WRAP agent DLE counter is underflowed. [7]: WRAP_CHDLE_OVF: WRAP channel DLE counter is overflowed. [6]: WRAP_CHDLE_UNF: WRAP channel DLE counter is underflowed. [5]: MAN_CMD_MISS: A MAN CMD is written while MAN is disabled. [4]: MAN_UNEXP_DLE: MAN unexpected DLE [3]: MAN_UNEXP_VLDCLR: MAN unexpected VLDCLR [2]: SIG_ERR1: Signature 1 check fails. [1]: SIG_ERR: Signature check fails. [0]: WDT_INT: Watchdog timeout

100010C4 **INT_FLG_RAW** **Interrupt Flags - Raw** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_FLG_RAW[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT_FLG_RAW[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT_FLG_RAW	Interrupt flags (not gated with INT_EN)

100010C8 **INT_FLG** **Interrupt Flags** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_FLG[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT_FLG[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT_FLG	[31]: DEBUG_INT: Selected DEBUG source is asserted. [30:24]: Reserved [23]: STAUPD_DLE_CNT_OVF: STAUPD DLE counter is overflowed. [22]: STAUPD_ALE_CNT_OVF: STAUPD ALE counter is overflowed. [21]: Modem request error occurs [20]: WACS2_CMD_MISS: A WACS2 CMD is written while WACS2 is disabled. [19]: WACS2_UNEXP_DLE: WACS2 unexpected DLE [18]: WACS2_UNEXP_VLDCLR: WACS2 unexpected VLDCLR [17]: WACS1_CMD_MISS: A WACS1 CMD is written while WACS1 is disabled. [16]: WACS1_UNEXP_DLE: WACS1 unexpected DLE [15]: WACS1_UNEXP_VLDCLR: WACS1 unexpected VLDCLR

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Bit(s)	Name	Description
		[14]: WACS0_CMD_MISS: A WACS0 CMD is written while WACS0 is disabled. [13]: WACS0_UNEXP_DLE: WACS0 unexpected DLE [12]: WACS0_UNEXP_VLDCLR: WACS0 unexpected VLDCLR [11]: HARB_DLE_OVF: High priority arbiter DLE is overflowed. [10]: HARB_DLE_UNF: High priority arbiter DLE is underflowed. [9]: WRAP_AGDLE_OVF: WRAP agent DLE counter is overflowed. [8]: WRAP_AGDLE_UNF: WRAP agent DLE counter is underflowed. [7]: WRAP_CHDLE_OVF: WRAP channel DLE counter is overflowed. [6]: WRAP_CHDLE_UNF: WRAP channel DLE counter is underflowed. [5]: MAN_CMD_MISS: A MAN CMD is written while MAN is disabled. [4]: MAN_UNEXP_DLE: MAN unexpected DLE [3]: MAN_UNEXP_VLDCLR: MAN unexpected VLDCLR [2]: SIG_ERR1: Signature 1 check fails. [1]: SIG_ERR: Signature check fails. [0]: WDT_INT: Watchdog timeout

100010CC **INT_CLR** **Interrupt Clear** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_CLR[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT_CLR[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT_CLR	Clear interrupt flags by writing 1 to the corresponding bit.

100010D0 **SIG_ADR** **Signature Address in MT6332** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SIG_ADR1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIG_ADR0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SIG_ADR1	**Checks signature address at PMIC side automatically** The STAUPD circuit fetches data from address every STAUPD_PRD time.
15:0	SIG_ADR0	**Checks signature address at PMIC side automatically** The STAUPD circuit is fetches data from address every STAUPD_PRD time.

100010D4 **SIG_MODE** **Signature Checking Mode in MT6332** **00**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**SIG_MODE1**	**SIG_MODE0**
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	SIG_MODE1	**Selects signature check mode** 0: Check CRC value 1: Check SIG_VALUE.
0	SIG_MODE0	**Selects signature check mode** 0: Check CRC value 1: Check SIG_VALUE.

100010D8 **SIG_VALUE** **Signature Value in MT6332** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SIG_VALUE1**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SIG_VALUE0**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SIG_VALUE1	**Checks signature value at PMIC side to automatically** If data fetched by STAUPD circuit do not match SIG_VALUE, an error interrupt (SIG_ERR) will be asserted.
15:0	SIG_VALUE0	**Checks signature value at PMIC side automatically** If data fetched by STAUPD circuit do not match SIG_VALUE, an error interrupt (SIG_ERR) will be asserted.

100010DC **SIG_ERRVAL** **Error Signature Value in MT6332** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SIG_ERRVAL1**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SIG_ERRVAL0**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SIG_ERRVAL1	When SIG_ERR occurs, the erroneous signature will be latched and can be read out from this.
15:0	SIG_ERRVAL0	When SIG_ERR occurs, the erroneous signature will be latched and can be read out from this.

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100010E0 CRC_EN CRC Enable 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CRC_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	CRC_EN	**Set to 1 to enable CRC calculation of ADR[15:0], RDATA[15:0] and WDATA[15:0].** 0: Disable 1: Enable

100010E4 TIMER_EN Timer Enable 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TIMER_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	TIMER_EN	**Enables timer clock** Disable the timer clock before modifying timer-related settings to avoid asynchronous issues. 0: Disable 1: Enable

100010E8 TIMER_STA Timer Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				STAUPD_TIMER												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDT_TIMER															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	STAUPD_TIMER	**STAUPD timer status** Unit: 38ns.
15:0	WDT_TIMER	**Watchdog timer status** Unit: 38ns.

100010EC WDT_UNIT Watchdog Timer Unit 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													WDT_UNIT			

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Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	WDT_UNIT	**Selects watchdog timer unit** The watchdog time-out occurs in 2~3 units. The unit is selected in WDT_TIMER[WDT_UNIT] which is a counter by 26MHz. For example, if WDT_UNIT = 0x8, the watchdog time-out will occur in (2~3)*(2^9)*38ns = 38.9us ~ 58.4us 0: Disable 8: 38.9us ~ 58.4us 15: 5ms ~ 7.5ms

100010F0 **WDT_SRC_EN** **Watch Dog Timer Source Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDT_SRC_EN[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDT_SRC_EN[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WDT_SRC_EN	**Enables watchdog timer source** [31]: RESERVED [30]: RESERVED [29]: RESERVED [28]: RESERVED [27]: RESERVED [26]: PREADY: APB PREADY timeout monitor [25]: STAUPD_TRIG: STAUPD trigger signal timeout monitor [24]: MSTCTL_SYNC_DLE: MSTCTL to SYNC DLE timeout monitor [23]: MUX_MAN_DLE: MUX to MAN DLE timeout monitor [22]: MUX_WRAP_DLE: MUX to WRAP DLE timeout monitor [21]: HARB_WACS3_DLE: HARB to WACS3 DLE timeout monitor [20]: HARB_STAUPD_DLE: HARB to STAUPD DLE timeout monitor [19]: HARB_SPMINF_DLE: HARB to SPMINF DLE timeout monitor [18]: HARB_WACS2_DLE: HARB to WACS2 DLE timeout monitor [17]: HARB_WACS1_DLE: HARB to WACS1 DLE timeout monitor [16]: HARB_WACS0_DLE: HARB to WACS0 DLE timeout monitor [15]: SYNC_MUX_ALE: SYNC to MUX ALE timeout monitor [14]: MUX_MAN_ALE: MUX to MAN ALE timeout monitor [13]: MUX_WRAP_ALE: MUX to WRAP ALE timeout monitor [12]: WRAP_HARB_ALE: WRAP to HARB ALE timeout monitor [11]: RESERVED [10]: HARB_MA_ADC_DLE: HARB to MD_ADC DLE timeout monitor [9]: HARB_WACS3_ALE: HARB to WACS3 ALE timeout monitor [8]: HARB_STAUPD_ALE: HARB to STAUPD ALE timeout monitor [7]: HARB_GPSINF_ALE: HARB to GPSINF ALE timeout monitor [6]: HARB_WACS1_ALE: HARB to WACS1 ALE timeout monitor [5]: HARB_MD_ADC_ALE: HARB to MD_ADC ALE timeout monitor [4]: HARB_WACS2_ALE: HARB to WACS2 ALE timeout monitor [3]: HARB_SPMINF_ALE: HARB to SPMINF ALE timeout monitor [2]: HARB_WACS0_ALE: HARB to WACS0 ALE timeout monitor [1]: HARB_C2KINF_ALE: HARB to C2KINF ALE timeout monitor [0]: HARB_MDINF_ALE: HARB to MDINF ALE timeout monitor

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100010F4 **WDT_FLG** **Watchdog Flag** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDT_FLG[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDT_FLG[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WDT_FLG	[31]: Reserved [30]: Reserved [29]: Reserved [28]: Reserved [27]: Reserved [26]: PREADY: APB PREADY timeout monitor [25]: STAUPD_TRIG: STAUPD trigger signal timeout monitor [24]: MSTCTL_SYNC_DLE: MSTCTL to SYNC DLE timeout monitor [23]: MUX_MAN_DLE: MUX to MAN DLE timeout monitor [22]: MUX_WRAP_DLE: MUX to WRAP DLE timeout monitor [21]: HARB_WACS3_DLE: HARB to WACS3 DLE timeout monitor [20]: HARB_STAUPD_DLE: HARB to STAUPD DLE timeout monitor [19]: HARB_SPMINF_DLE: HARB to SPMINF DLE timeout monitor [18]: HARB_WACS2_DLE: HARB to WACS2 DLE timeout monitor [17]: HARB_WACS1_DLE: HARB to WACS1 DLE timeout monitor [16]: HARB_WACS0_DLE: HARB to WACS0 DLE timeout monitor [15]: SYNC_MUX_ALE: SYNC to MUX ALE timeout monitor [14]: MUX_MAN_ALE: MUX to MAN ALE timeout monitor [13]: MUX_WRAP_ALE: MUX to WRAP ALE timeout monitor [12]: WRAP_HARB_ALE: WRAP to HARB ALE timeout monitor [11]: Reserved [10]: HARB_MA_ADC_DLE: HARB to MD_ADC DLE timeout monitor [9]: HARB_WACS3_ALE: HARB to WACS3 ALE timeout monitor [8]: HARB_STAUPD_ALE: HARB to STAUPD ALE timeout monitor [7]: HARB_GPSINF_ALE: HARB to GPSINF ALE timeout monitor [6]: HARB_WACS1_ALE: HARB to WACS1 ALE timeout monitor [5]: HARB_MD_ADC_ALE: HARB to MD_ADC ALE timeout monitor [4]: HARB_WACS2_ALE: HARB to WACS2 ALE timeout monitor [3]: HARB_SPMINF_ALE: HARB to SPMINF ALE timeout monitor [2]: HARB_WACS0_ALE: HARB to WACS0 ALE timeout monitor [1]: HARB_C2KINF_ALE: HARB to C2KINF ALE timeout monitor [0]: HARB_MDINF_ALE: HARB to MDINF ALE timeout monitor

100010F8 **DEBUG_INT_SEL** **Debug Interrupt Selection** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														DEBUG_INT_SEL		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	DEBUG_INT_SEL	**Debug flag as interrupt source selection**

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Bit(s)	Name	Description
		Select which bit of debug_out3[7:0] is used as interrupt source.

100010FC DVFS_ADR0 DVFS Command #0 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR0	DVFS Command #0 - Address

10001100 DVFS_WDATA0 DVFS Command #0 - Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA0	DVFS Command #0 - Write Data

10001104 DVFS_ADR1 DVFS Command #1 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR1	DVFS Command #1 - Address

10001108 DVFS_WDATA1 DVFS Command #1 - Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA1	DVFS Command #1 - Write Data

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1000110C DVFS_ADR2 DVFS Command #2 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR2	DVFS Command #2 - Address

10001110 DVFS_WDATA2 DVFS Command #2 - Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA2	DVFS Command #2 - Write Data

10001114 DVFS_ADR3 DVFS Command #3 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR3	DVFS Command #3 - Address

10001118 DVFS_WDATA3 DVFS Command #3 - Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA3	DVFS Command #3 - Write Data

1000111C DVFS_ADR4 DVFS Command #4 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	DVFS_ADR4	DVFS Command #4 - Address

10001120 DVFS_WDATA4 DVFS Command #4 - Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA4	DVFS Command #4 - Write Data

10001124 DVFS_ADR5 DVFS Command #5 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR5	DVFS Command #5 - Address

10001128 DVFS_WDATA5 DVFS Command #5 - Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA5	DVFS Command #5 - Write Data

1000112C DVFS_ADR6 DVFS Command #6 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR6	DVFS Command #6 - Address

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10001130 **DVFS_WDATA6** **DVFS Command #6 - Write Data** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA6	DVFS Command #6 - Write Data

10001134 **DVFS_ADR7** **DVFS Command #7 - Address** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR7	DVFS Command #7 - Address

10001138 **DVFS_WDATA7** **DVFS Command #7 - Write Data** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA7	DVFS Command #7 - Write Data

1000113C **DVFS_ADR8** **DVFS Command #8 - Address** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR8															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR8	DVFS Command #8 - Address

10001140 **DVFS_WDATA8** **DVFS Command #8 - Write Data** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA8															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	DVFS_WDATA8	DVFS Command #8 - Write Data

10001144 DVFS_ADR9 DVFS Command #9 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR9															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR9	DVFS Command #9 - Address

10001148 DVFS_WDATA9 DVFS Command #9 - Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA9															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA9	DVFS Command #9 - Write Data

1000114C DVFS_ADR10 DVFS Command #10 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR10															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR10	DVFS Command #10 - Address

10001150 DVFS_WDATA10 DVFS Command #10 - Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA10															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA10	DVFS Command #10 - Write Data

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10001154 **DVFS_ADR11** **DVFS Command #11 - Address** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR11															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR11	DVFS Command #11 - Address

10001158 **DVFS_WDATA11** **DVFS Command #11 - Write Data** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA11															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA11	DVFS Command #11 - Write Data

1000115C **DVFS_ADR12** **DVFS Command #12 - Address** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR12															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR12	DVFS Command #12 - Address

10001160 **DVFS_WDATA12** **DVFS Command #12 - Write Data** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA12															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA12	DVFS Command #12 - Write Data

10001164 **DVFS_ADR13** **DVFS Command #13 - Address** **0000**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR13															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR13	DVFS Command #13 - Address

10001168 **DVFS_WDATA13** **DVFS Command #13 - Write Data** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA13															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA13	DVFS Command #13 - Write Data

1000116C **DVFS_ADR14** **DVFS Command #14 - Address** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR14															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR14	DVFS Command #14 - Address

10001170 **DVFS_WDATA14** **DVFS Command #14 - Write Data** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA14															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA14	DVFS Command #14 - Write Data

10001174 **DVFS_ADR15** **DVFS Command #15 - Address** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	DVFS_ADR15	DVFS Command #15 - Address

10001178 **DVFS_WDATA15** **DVFS Command #15 - Write Data** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA15	DVFS Command #15 - Write Data

1000117C **SPMINF_STA** **SPM Interface Status Register** **001C**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					SPMINF_STA											
Type					RU											
Reset					0	0	0	0	0	0	0	1	1	1	0	0

Bit(s)	Name	Description
11:0	SPMINF_STA	**SPM interface status** The statuses of DVFS control, sleep handshake interface and PMIC_IRQ interface are involved. [11]: SYS_IDLE [10]: SLEEP_ACK [9]: SLEEP_REQ [8]: PMIC_SCP_IRQ [7]: PMIC_IRQ_ACK [6]: PMIC_IRQ_REQ [5: 2] DVFS_CTRL [1]: DVFS_CTRL_ACK [0]: DVFS_CTRL_RDY

10001180 **CIPHER_KEY_SEL** **CIPHER Key Selection** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CIPHER_KEY_SEL	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	CIPHER_KEY_SEL	**Selects cipher key** All keys are hard-wired.

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10001184 **CIPHER_IV_SEL** **CIPHER Initial Vector Selection** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CIPHER_IV_SEL	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	CIPHER_IV_SEL	**Selects cipher initial vector** Set to 0 to select manual initial vector; otherwise, other hard-wired initial vectors will be selected.

10001188 **CIPHER_EN** **CIPHER Engine Enable** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CIPHER_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	CIPHER_EN	Starts cipher engine

1000118C **CIPHER_RDY** **CIPHER Data Ready** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CIPHER_RDY	
Type															RU	
Reset															0	0

Bit(s)	Name	Description
1:0	CIPHER_RDY	**Cipher data ready** Bit 0 is for cipher 0; bit 1 is for cipher 1. The data should be ready before CIPHER_MODE is enabled. 0: Not ready 1: Ready

10001190 **CIPHER_MODE** **CIPHER Mode Enable** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CIPHER_MODE
Type																RW
Reset																0

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Bit(s)	Name	Description
0	CIPHER_MODE	**Enables cipher mode** 0: Disable 1: Enable

10001194 **CIPHER_SWRST** **CIPHER Soft Reset** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CIPHER_SWRST
Type																RW
Reset																0

Bit(s)	Name	Description
0	CIPHER_SWRST	Cipher soft reset

10001198 **DCM_EN** **Internal DCM Enable** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														TOP_DCM_EN	CRC_CK_SEL	DCM_EN
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	TOP_DCM_EN	**Enables top spi_ck DCM** 0: Disable top DCM for spi_ck 1: Enable top DCM for spi_ck. When PMIC_WRAP is in idle state, the clock will be gated.
1	CRC_CK_SEL	**Selects CRC clock** 0: Choose non-DCM clock 1: Choose DCM clock
0	DCM_EN	**Enables internal DCM** 0: Disable internal DCM 1: Enable internal DCM. When PMIC_WRAP is in idle state, the clock will be gated.

1000119C **DCM_DBC_PRD** **Debounce Period at Entering DCM Mode** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DCM_DBC_PRD							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
7:0	DCM_DBC_PRD	**Debounce period before entering DCM mode** 0: Disable debounce

100011A0 EXT_CK Extra Clock Number 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EXT_CK
Type																RW
Reset																0

Bit(s)	Name	Description
0	EXT_CK	Extra Clock number = (1 + EXT_CK)

100011A4 ADC_CMD_ADDR AUXADC Command Register Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_CMD_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	ADC_CMD_ADDR	AUXDC command register address

100011A8 PWRAP_ADC_CMD Command to AUXADC 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PWRAP_ADC_CMD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PWRAP_ADC_CMD	Command to AUXADC

100011AC ADC_RDATA_ADDR Address of Thermal Data [15:0] Register in AUXADC 0004

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_RDATA_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
15:0	ADC_RDATA_ADDR	Address of thermal data [15:0] register in AUXADC

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100011B0 GPS_STA GPS Interface Status (Debug) 00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PWRAP_GPS_WDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						GPS_INF_FSM			GPSINF_ALE_CNT		GPSINF_DLE_CNT				GPS_PWRAP_REQ	PWRAP_GPS_ACK
Type						RU			RU		RU				RU	RU
Reset						0	0	1	0	0	0	0			0	0

Bit(s)	Name	Description
31:17	PWRAP_GPS_WDATA	**AUXADC thermal data for GPS**
10:8	GPS_INF_FSM	**Current GPSINF FSM state** 1: IDLE 2: REQ 4: WFRDY
7:6	GPSINF_ALE_CNT	**GPS interface ale count**
5:4	GPSINF_DLE_CNT	**GPS interface dle count**
1	GPS_PWRAP_REQ	**GPS request**
0	PWRAP_GPS_ACK	**AUXADC data ready bit for GPS**

100011B4 SWRST Software Reset 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SWRST
Type																RW
Reset																0

Bit(s)	Name	Description
0	SWRST	Not used

100011B8 MD_ADC_RDATA_ADDR_LATEST Address of the Latest Thermal Data [15:0] Register in AUXADC 0008

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR_LATEST															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR_LATEST	Address of the latest thermal data [15:0] register in AUXADC

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100011BC	**MD_ADC_RDATA_ADDR_WP**	**Address of the Latest Buffer Thermal Data Pointer**	**000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR_WP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR_WP	Address of the latest buffer thermal data pointer

100011C0	**MD_ADC_RDATA_ADDR0**	**Address of the Buffer Thermal Data 0**	**000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR0	Address of buffer thermal data 0

100011C4	**MD_ADC_RDATA_ADDR1**	**Address of the Buffer Thermal Data 1**	**000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR1	Address of buffer thermal data 1

100011C8	**MD_ADC_RDATA_ADDR2**	**Address of the Buffer Thermal Data 2**	**000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

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Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR2	Address of buffer thermal data 2

100011CC **MD_ADC_RDATA_ADDR3** **Address of the Buffer Thermal Data 3** **000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR3	Address of buffer thermal data 3

100011D0 **MD_ADC_RDATA_ADDR4** **Address of the Buffer Thermal Data 4** **000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR4	Address of buffer thermal data 4

100011D4 **MD_ADC_RDATA_ADDR5** **Address of the Buffer Thermal Data 5** **000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR5	Address of buffer thermal data 5

100011D8 **MD_ADC_RDATA_ADDR6** **Address of the Buffer Thermal Data 6** **000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR6															

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Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR6	Address of buffer thermal data 6

100011DC MD_ADC_RDATA_ADDR7 Address of the Buffer Thermal Data 7 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR7	Address of buffer thermal data 7

100011E0 MD_ADC_RDATA_ADDR8 Address of the Buffer Thermal Data 8 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR8															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR8	Address of buffer thermal data 8

100011E4 MD_ADC_RDATA_ADDR9 Address of the Buffer Thermal Data 9 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR9															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR9	Address of buffer thermal data 9

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100011E8 **MD_ADC_RDATA_ADDR10** **Address of the Buffer Thermal Data 10** **000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR10															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR10	Address of buffer thermal data 10

100011EC **MD_ADC_RDATA_ADDR11** **Address of the Buffer Thermal Data 11** **000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR11															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR11	Address of buffer thermal data 11

100011F0 **MD_ADC_RDATA_ADDR12** **Address of the Buffer Thermal Data 12** **000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR12															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR12	Address of buffer thermal data 12

100011F4 **MD_ADC_RDATA_ADDR13** **Address of the Buffer Thermal Data 13** **000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR13															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_	Address of buffer thermal data 13

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Bit(s)	Name	Description
	ADDR13	

100011F8 **MD_ADC_RDATA_ADDR14** **Address of the Buffer Thermal Data 14** **000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR14															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR14	Address of buffer thermal data 14

100011FC **MD_ADC_RDATA_ADDR15** **Address of the Buffer Thermal Data 15** **000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR15	Address of buffer thermal data 15

10001200 **MD_ADC_RDATA_ADDR16** **Address of the Buffer Thermal Data 16** **000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR16															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR16	Address of buffer thermal data 16

10001204 **MD_ADC_RDATA_ADDR17** **Address of the Buffer Thermal Data 17** **000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR17															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR17	Address of buffer thermal data 17

10001208 **MD_ADC_RDATA_ADDR18** **Address of the Buffer Thermal Data 18** **000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR18															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR18	Address of buffer thermal data 18

1000120C **MD_ADC_RDATA_ADDR19** **Address of the Buffer Thermal Data 19** **000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR19															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR19	Address of buffer thermal data 19

10001210 **MD_ADC_RDATA_ADDR20** **Address of the Buffer Thermal Data 20** **000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR20															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR20	Address of buffer thermal data 20

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10001214 **MD_ADC_RDATA_ADDR21** **Address of the Buffer Thermal Data 21** **000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR21															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR21	Address of buffer thermal data 21

10001218 **MD_ADC_RDATA_ADDR22** **Address of the Buffer Thermal Data 22** **000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR22															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR22	Address of buffer thermal data 22

1000121C **MD_ADC_RDATA_ADDR23** **Address of the Buffer Thermal Data 23** **000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR23															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR23	Address of buffer thermal data 23

10001220 **MD_ADC_RDATA_ADDR24** **Address of the Buffer Thermal Data 24** **000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR24															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_	Address of buffer thermal data 24

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Bit(s)	Name	Description
	ADDR24	

10001224 **MD_ADC_RDATA_ADDR25** **Address of the Buffer Thermal Data 25** **000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR25															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR25	Address of buffer thermal data 25

10001228 **MD_ADC_RDATA_ADDR26** **Address of the Buffer Thermal Data 26** **000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR26															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR26	Address of buffer thermal data 26

1000122C **MD_ADC_RDATA_ADDR27** **Address of the Buffer Thermal Data 27** **000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR27															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR27	Address of buffer thermal data 27

10001230 **MD_ADC_RDATA_ADDR28** **Address of the Buffer Thermal Data 28** **000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR28															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR28	Address of buffer thermal data 28

10001234 MD_ADC_RDATA_ADDR29 Address of the Buffer Thermal Data 29 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR29															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR29	Address of buffer thermal data 29

10001238 MD_ADC_RDATA_ADDR30 Address of the Buffer Thermal Data 30 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR30															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR30	Address of buffer thermal data 30

1000123C MD_ADC_RDATA_ADDR31 Address of the Buffer Thermal Data 31 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR31															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR31	Address of buffer thermal data 31

10001240 MD_ADC_STA0 MD_AUXADC Interface Status 0 (Debug) 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PWRAP_MD_ADC_INIT_DATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PWRAP_MD_ADC_NORM_DATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PWRAP_MD_ADC_INIT_DATA	AUXADC thermal data for MD in init mode
15:0	PWRAP_MD_ADC_NORM_DATA	AUXADC thermal data for MD in normal mode

10001244 **MD_ADC_STA1** **MD_AUXADC Interface Status 1 (Debug)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MD_ADC_BUF_WDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF_MD_ADC_RDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MD_ADC_BUF_WDATA	Thermal data of init mode for writing into FIFO
15:0	BUF_MD_ADC_RDATA	Thermal data of init mode for reading out from FIFO

10001248 **MD_ADC_STA2** **MD_AUXADC Interface Status2 (Debug)** **00004400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						MD_ADC_DLE_CNT_REAL						MD_ADC_ALE_CNT[5:1]				
Type						RU						RU				
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_ALE_CNT[0:0]	MD_ADC_FIFO_FREECNT						MD_ADC_FIFO_FILLCNT						MD_ADC_FSM		
Type	RU	RU						RU						RU		
Reset	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:21	MD_ADC_DLE_CNT_REAL	**MD co-clock interface dle count**
20:15	MD_ADC_ALE_CN	**GPS interface ale count**

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Bit(s)	Name	Description
	T	
14:9	MD_ADC_FIFO_FREECNT	**Records the number of data can be filled into FIFO**
8:3	MD_ADC_FIFO_FILLCNT	**Records the number of data filled into FIFO**
2:0	MD_ADC_FSM	**Current MD_ADCINF FSM State** 1: IDLE 2: REQ 4: WFRDY

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4.4 Frequency Hopping Controller

4.4.1 Introduction

The frequency hopping controller helps AP resolve de-sense issues. The RF victims are 2G/3G/BT/FM/WiFi/GPS, etc. The aggressors in AP is the clock generated from PLL in ABB. The harmonic of all clock frequencies may de-sense the band of RF system.

4.4.2 Features

The frequency hopping controller receives the command from CPU to trigger two mechanisms:

- Spread spectrum clocking
- Frequency hopping

In MT6735, there are 7 hopping PLLs:

NAME	Capability	Range
ARMPLL	hopping, SSC	{-8%,0}
MAINPLL	hopping, SSC	{-8%,0}
MEMPLL	hopping, SSC	{-8%,0}
MMPLL	hopping, SSC	{-8%,0}
VENCPLL	SSC	{-4%,0}
MSDCPLL	hopping, SSC	{-8%,0}
TVDPLL	SSC	{-8%,0}

4.4.3 Block Diagram

Whenever MCUSYS enters sleep mode, SRCLKENA from the sleep controller is de-asserted. SRCLKENA from MCUSYS controls the power supply for the 13MHz/26MHz TCVCXO via the on-chip PMU. When the signal is de-asserted, LDO for TCVCXO in the PMU will be turned off, and 13MHz/26MHz clock will stop.

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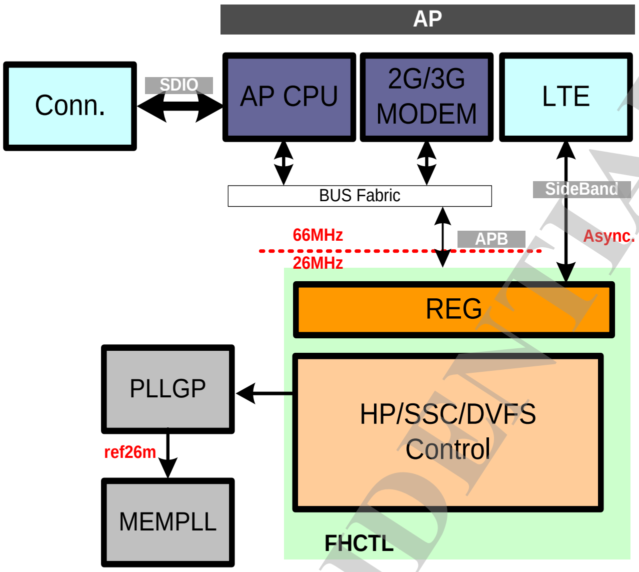

Figure 4-8. Block diagram of frequency hopping controller

4.4.4 Register Definition

Module name: FHCTL Base address: (+10209F00h)

Address	Name	Width	Register Function
10209F00	FHCTL_HP_EN	32	FHCTL Hopping Enable
10209F04	FHCTL_CLK_CON	32	FHCTL Clock Control
10209F08	FHCTL_RST_CON	32	FHCTL Software Reset Control
10209F0C	FHCTL_SLOPE0	32	**FHCTL PLL SLOPE GROUP0 Setting** (ARMPLL MAINPLL MMPLL VENCPLL MSDCPLL TVDPLL)
10209F10	FHCTL_SLOPE1	32	**FHCTL PLL SLOPE GROUP1 Setting** (MEMPLL)
10209F14	FHCTL_DSSC_CFG	32	FHCTL Dynamic SSC Config (RF number = 0 ~ 7)
10209F18	FHCTL_DSSC0_CON	32	FHCTL Dynamic SSC RF0 Control (RF0 = 2G1)
10209F1C	FHCTL_DSSC1_CON	32	FHCTL Dynamic SSC RF1 Control (RF1 = 2G2)
10209F20	FHCTL_DSSC2_CON	32	FHCTL Dynamic SSC RF2 Control (RF2 = 3G)
10209F24	FHCTL_DSSC3_CON	32	FHCTL Dynamic SSC RF3 Control (RF3 = LTE)
10209F28	FHCTL_DSSC4_CON	32	FHCTL Dynamic SSC RF4 Control (RF4 = BT)
10209F2C	FHCTL_DSSC5_CON	32	FHCTL Dynamic SSC RF5 Control (RF5 = WiFi)
10209F30	FHCTL_DSSC6_CON	32	FHCTL Dynamic SSC RF6 Control (RF6 = FM)
10209F34	FHCTL_DSSC7_CON	32	FHCTL Dynamic SSC RF7 Control (RF7 = GPS)
10209F38	FHCTL0_CFG	32	FHCTL0 (ARMPLL) Config
10209F3C	FHCTL0_UPDNLMT	32	FHCTL0 (ARMPLL) Up/Down Limit

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Address	Name	Width	Register Function
10209F40	FHCTL0_DDS	32	FHCTL0 (ARMPLL) DDS
10209F44	FHCTL0_DVFS	32	FHCTL0 (ARMPLL) DVFS
10209F48	FHCTL0_MON	32	FHCTL0 (ARMPLL) Monitor
10209F4C	FHCTL1_CFG	32	FHCTL1 (MAINPLL) Config
10209F50	FHCTL1_UPDN LMT	32	FHCTL1 (MAINPLL) Up/Down Limit
10209F54	FHCTL1_DDS	32	FHCTL1 (MAINPLL) DDS
10209F58	FHCTL1_DVFS	32	FHCTL1 (MAINPLL) DVFS
10209F5C	FHCTL1_MON	32	FHCTL1 (MAINPLL) Monitor
10209F60	FHCTL2_CFG	32	FHCTL2 (MEMPLL) Config
10209F64	FHCTL2_UPDN LMT	32	FHCTL2 (MEMPLL) Up/Down Limit
10209F68	FHCTL2_DDS	32	FHCTL2 (MEMPLL) DDS
10209F6C	FHCTL2_DVFS	32	FHCTL2 (MEMPLL) DVFS
10209F70	FHCTL2_MON	32	FHCTL2 (MEMPLL) Monitor
10209F74	FHCTL3_CFG	32	FHCTL3 (MMPLL) Config
10209F78	FHCTL3_UPDN LMT	32	FHCTL3 (MMPLL) Up/Down Limit
10209F7C	FHCTL3_DDS	32	FHCTL3 (MMPLL) DDS
10209F80	FHCTL3_DVFS	32	FHCTL3 (MMPLL) DVFS
10209F84	FHCTL3_MON	32	FHCTL3 (MMPLL) Monitor
10209F88	FHCTL4_CFG	32	FHCTL4 (VENCPLL) Config
10209F8C	FHCTL4_UPDN LMT	32	FHCTL4 (VENCPLL) Up/Down Limit
10209F90	FHCTL4_DDS	32	FHCTL4 (VENCPLL) DDS
10209F94	FHCTL4_DVFS	32	FHCTL4 (VENCPLL) DVFS
10209F98	FHCTL4_MON	32	FHCTL4 (VENCPLL) Monitor
10209F9C	FHCTL5_CFG	32	FHCTL5 (MSDCPLL) Config
10209FA0	FHCTL5_UPDN LMT	32	FHCTL5 (MSDCPLL) Up/Down Limit
10209FA4	FHCTL5_DDS	32	FHCTL5 (MSDCPLL) DDS
10209FA8	FHCTL5_DVFS	32	FHCTL5 (MSDCPLL) DVFS
10209FAC	FHCTL5_MON	32	FHCTL5 (MSDCPLL) Monitor
10209FB0	FHCTL6_CFG	32	FHCTL6 (TVDPLL) Config
10209FB4	FHCTL6_UPDN LMT	32	FHCTL6 (TVDPLL) Up/Down Limit
10209FB8	FHCTL6_DDS	32	FHCTL6 (TVDPLL) DDS
10209FBC	FHCTL6_DVFS	32	FHCTL6 (TVDPLL) DVFS
10209FC0	FHCTL6_MON	32	FHCTL6 (TVDPLL) Monitor

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10209F00 FHCTL_HP_EN FHCTL Hopping Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LTE_SIDEBAND_EN															
Type	RW															
Reset	0															

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										TVDPLL_HP_EN	MSDCPLL_HP_EN	VENCPLL_HP_EN	MMPLL_HP_EN	MEMPLL_HP_EN	MAINPLL_HP_EN	ARMPLL_HP_EN
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		LTE_SIDEBAND_EN	**Controls sideband signal from LTE DSP** 0: Off 1: On
6		TVDPLL_HP_EN	**TVDPLL divider (SDM_PCW) source control** 0: APMIXEDSYS control 1: FHCTL control
5		MSDCPLL_HP_EN	**MSDCPLL divider (SDM_PCW) source control** 0: APMIXEDSYS control 1: FHCTL control
4		VENCPLL_HP_EN	**VENCPLL divider (SDM_PCW) source control** 0: APMIXEDSYS control 1: FHCTL control
3		MMPLL_HP_EN	**MMPLL divider (SDM_PCW) source control** 0: APMIXEDSYS control 1: FHCTL control
2		MEMPLL_HP_EN	**MEMPLL divider (SDM_PCW) source control** 0: APMIXEDSYS control 1: FHCTL control
1		MAINPLL_HP_EN	**MAINPLL divider (SDM_PCW) source control** 0: APMIXEDSYS control 1: FHCTL control
0		ARMPLL_HP_EN	**ARMPLL divider (SDM_PCW) source control** 0: APMIXEDSYS control 1: FHCTL control

10209F04 **FHCTL_CLK_CON** **FHCTL Clock Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										TVDPLL_HP_CLKEN	MSDCPLL_HP_CLKEN	VENCPLL_HP_CLKEN	MMPLL_HP_CLKEN	MEMPLL_HP_CLKEN	MAINPLL_HP_CLKEN	ARMPLL_HP_CLKEN
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6		TVDPLL_HP_CLKEN	**Enables TVDPLL hopping controller CLK (high active)** 0: Disable clock 1: Enable clock
5		MSDCPLL_HP_CL	**Enables MSDCPLL hopping controller CLK (high active)**

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Bit(s)	Mnemonic	Name	Description
		KEN	0: Disable clock 1: Enable clock
4		VENCPLL_HP_CLKEN	**Enables VENCPLL hopping controller CLK (high active)** 0: Disable clock 1: Enable clock
3		MMPLL_HP_CLKEN	**Enables MMPLL hopping controller CLK (high active)** 0: Disable clock 1: Enable clock
2		MEMPLL_HP_CLKEN	**Enables MEMPLL hopping controller CLK (high active)** 0: Disable clock 1: Enable clock
1		MAINPLL_HP_CLKEN	**Enables MAINPLL hopping controller CLK (high active)** 0: Disable clock 1: Enable clock
0		ARMPLL_HP_CLKEN	**Enables ARMPLL hopping controller CLK (high active)** 0: Disable clock 1: Enable clock

10209F08 **FHCTL_RST_CON** **FHCTL Software Reset Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**TVDPLL_HP_SWRSTB**	**MSDCPLL_HP_SWRSTB**	**VENCPLL_HP_SWRSTB**	**MMPLL_HP_SWRSTB**	**MEMPLL_HP_SWRSTB**	**MAINPLL_HP_SWRSTB**	**ARMPLL_HP_SWRSTB**
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6		TVDPLL_HP_SWRSTB	**TVDPLL hopping controller software resetb (low active)** 0: Reset 1: No reset
5		MSDCPLL_HP_SWRSTB	**MSDCPLL hopping controller software resetb (low active)** 0: Reset 1: No reset
4		VENCPLL_HP_SWRSTB	**VENCPLL hopping controller software resetb (low active)** 0: Reset 1: No reset
3		MMPLL_HP_SWRSTB	**MMPLL hopping controller software resetb (low active)** 0: Reset 1: No reset
2		MEMPLL_HP_SWRSTB	**MEMPLL hopping controller software resetb (low active)** 0: Reset 1: No reset
1		MAINPLL_HP_SWRSTB	**MAINPLL hopping controller software resetb (low active)** 0: Reset 1: No reset

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Bit(s)	Mnemonic	Name	Description
0		ARMPLL_HP_SW RSTB	**ARMPLL hopping controller software resetb (low active)** 0: Reset 1: No reset

10209F0C **FHCTL_SLOPE0** **FHCTL PLL SLOPE GROUP0 Setting (ARMPLL MAINPLL MMPLL VENCPLL MSDCPLL TVDPLL)** **06003C97**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FHCTL_SFDT0											FHCTL_SFDY0[20:16]				
Type	RW											RW				
Reset	0	0	0	0	0	1	1	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FHCTL_SFDY0[15:0]															
Type	RW															
Reset	0	0	1	1	1	1	0	0	1	0	0	1	0	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		FHCTL_SFDT0	**(ARMPLL MAINPLL MMPLL VENCPLL MSDCPLL TVDPLL)** T step for each delta-freq T = (fhctl_sfdt + 2)*(1/26MHz)
20:0		FHCTL_SFDY0	**(ARMPLL MAINPLL MMPLL VENCPLL MSDCPLL TVDPLL)** Ncpo step for delta-freq > 310MHz Frequency step = (fhctl_sfdy[20:0] >> 14)*26MHz 1. If < 10MHz, Ncpo step = fhctl_sfdy >> 2^4 2. If < 30MHz, Ncpo step = fhctl_sfdy >> 2^3 3. If < 70MHz, Ncpo step = fhctl_sfdy >> 2^2 4. If < 150MHz, Ncpo step = fhctl_sfdy >> 2^1 5. If < 310MHz, Ncpo step = fhctl_sfdy >> 2^0

10209F10 **FHCTL_SLOPE1** **FHCTL PLL SLOPE GROUP1 Setting (MEMPLL)** **06003C97**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FHCTL_SFDT1											FHCTL_SFDY1[20:16]				
Type	RW											RW				
Reset	0	0	0	0	0	1	1	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FHCTL_SFDY1[15:0]															
Type	RW															
Reset	0	0	1	1	1	1	0	0	1	0	0	1	0	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		FHCTL_SFDT1	**(MEMPLL)** T step for each delta-freq T = (fhctl_sfdt + 2)*(1/26MHz)
20:0		FHCTL_SFDY1	**(MEMPLL)** Ncpo step for delta-freq > 310MHz Frequency step = (fhctl_sfdy[20:0] >> 14)*26MHz 1. If < 10MHz, Ncpo step = fhctl_sfdy >> 2^4 2. If < 30MHz, Ncpo step = fhctl_sfdy >> 2^3

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Bit(s)	Mnemonic	Name	Description
			3. If < 70MHz, Ncpo step = fhctl_sfdy >> 2^2 4. If < 150MHz, Ncpo step = fhctl_sfdy >> 2^1 5. If < 310MHz, Ncpo step = fhctl_sfdy >> 2^0

10209F14 **FHCTL_DSSC_CFG** **FHCTL Dynamic SSC Config (RF number = 0 ~ 7)** **00FF00FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									DYSSC_BAN_MASK							
Type									RW							
Reset									1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DYSSC_SSC_MASK							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
23:16		DYSSC_BAN_MASK	**Decides whether to mask this feature for every RF** To turn on BAN feature from a certain RF, set this bit to 1'b0. bit [0]: RF0(2G1) BAN control bit [1]: RF1(2G2) BAN control bit [2]: RF2(3G) BAN control bit [3]: RF3(LTE) BAN control bit [4]: RF4(BT) BAN control bit [5]: RF5(WiFi) BAN control bit [6]: RF6(FM) BAN control bit [7]: RF7(GPS) BAN control
7:0		DYSSC_SSC_MASK	**Decides whether to mask this feature for every RF** To turn on SSC feature from a certain RF, set this bit to 1'b0. bit [0]: RF0(2G1) SSC control bit [1]: RF1(2G2) SSC control bit [2]: RF2(3G) SSC control bit [3]: RF3(LTE) SSC control bit [4]: RF4(BT) SSC control bit [5]: RF5(WiFi) SSC control bit [6]: RF6(FM) SSC control bit [7]: RF7(GPS) SSC control

10209F18 **FHCTL_DSSC0_CON** **FHCTL Dynamic SSC RF0 Control (RF0 = 2G1)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										DYSSC_RF0_BAN						
Type										RW						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										DYSSC_RF0_SSC						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
22:16		DYSSC_RF0_BAN	**Enables RF0 (2G1) BAN for each PLL** bit [0]: Enable ARMPLL BAN bit [1]: Enable MAINPLL BAN bit [2]: Enable MEMPLL BAN

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Bit(s)	Mnemonic	Name	Description
			bit [3]: Enable MMPLL BAN bit [4]: Enable VENCPLL BAN bit [5]: Enable MSDCPLL BAN bit [6]: Enable TVDPLL BAN
6:0		DYSSC_RF0_SSC	**Enables RF0 (2G1) SSC for each PLL** bit [0]: Enable ARMPLL SSC bit [1]: Enable MAINPLL SSC bit [2]: Enable MEMPLL SSC bit [3]: Enable MMPLL SSC bit [4]: Enable VENCPLL SSC bit [5]: Enable MSDCPLL SSC bit [6]: Enable TVDPLL SSC

10209F1C **FHCTL_DSSC1_CON** **FHCTL Dynamic SSC RF1 Control (RF1 = 2G2)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										DYSSC_RF1_BAN						
Type										RW						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										DYSSC_RF1_SSC						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
22:16		DYSSC_RF1_BAN	**Enables RF1 (2G2) BAN for each PLL** bit [0]: Enable ARMPLL BAN bit [1]: Enable MAINPLL BAN bit [2]: Enable MEMPLL BAN bit [3]: Enable MMPLL BAN bit [4]: Enable VENCPLL BAN bit [5]: Enable MSDCPLL BAN bit [6]: Enable TVDPLL BAN
6:0		DYSSC_RF1_SSC	**Enables RF1 (2G2) SSC for each PLL** bit [0]: Enable ARMPLL SSC bit [1]: Enable MAINPLL SSC bit [2]: Enable MEMPLL SSC bit [3]: Enable MMPLL SSC bit [4]: Enable VENCPLL SSC bit [5]: Enable MSDCPLL SSC bit [6]: Enable TVDPLL SSC

10209F20 **FHCTL_DSSC2_CON** **FHCTL Dynamic SSC RF2 Control (RF2 = 3G)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										DYSSC_RF2_BAN						
Type										RW						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										DYSSC_RF2_SSC						
Type										RW						
Reset										0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
22:16		DYSSC_RF2_BAN	**Enables RF2 (3G) BAN for each PLL** bit [0]: Enable ARMPLL BAN bit [1]: Enable MAINPLL BAN bit [2]: Enable MEMPLL BAN bit [3]: Enable MMPLL BAN bit [4]: Enable VENCPLL BAN bit [5]: Enable MSDCPLL BAN bit [6]: Enable TVDPLL BAN
6:0		DYSSC_RF2_SSC	**Enables RF2 (3G) SSC for each PLL** bit [0]: Enable ARMPLL SSC bit [1]: Enable MAINPLL SSC bit [2]: Enable MEMPLL SSC bit [3]: Enable MMPLL SSC bit [4]: Enable VENCPLL SSC bit [5]: Enable MSDCPLL SSC bit [6]: Enable TVDPLL SSC

10209F24 **FHCTL_DSSC3_CON** **FHCTL Dynamic SSC RF3 Control (RF3 = LTE)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										DYSSC_RF3_BAN						
Type										RW						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										DYSSC_RF3_SSC						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
22:16		DYSSC_RF3_BAN	**Enables RF3 (LTE) BAN for each PLL** bit [0]: Enable ARMPLL BAN bit [1]: Enable MAINPLL BAN bit [2]: Enable MEMPLL BAN bit [3]: Enable MMPLL BAN bit [4]: Enable VENCPLL BAN bit [5]: Enable MSDCPLL BAN bit [6]: Enable TVDPLL BAN
6:0		DYSSC_RF3_SSC	**Enables RF3 (LTE) SSC for each PLL** bit [0]: Enable ARMPLL SSC bit [1]: Enable MAINPLL SSC bit [2]: Enable MEMPLL SSC bit [3]: Enable MMPLL SSC bit [4]: Enable VENCPLL SSC bit [5]: Enable MSDCPLL SSC bit [6]: Enable TVDPLL SSC

10209F28 **FHCTL_DSSC4_CON** **FHCTL Dynamic SSC RF4 Control (RF4 = BT)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										DYSSC_RF4_BAN						
Type										RW						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name										DYSSC_RF4_SSC						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
22:16		DYSSC_RF4_BAN	**Enables RF4 (BT) BAN for each PLL** bit [0]: Enable ARMPLL BAN bit [1]: Enable MAINPLL BAN bit [2]: Enable MEMPLL BAN bit [3]: Enable MMPLL BAN bit [4]: Enable VENCPLL BAN bit [5]: Enable MSDCPLL BAN bit [6]: Enable TVDPLL BAN
6:0		DYSSC_RF4_SSC	**Enables RF4 (BT) SSC for each PLL** bit [0]: Enable ARMPLL SSC bit [1]: Enable MAINPLL SSC bit [2]: Enable MEMPLL SSC bit [3]: Enable MMPLL SSC bit [4]: Enable VENCPLL SSC bit [5]: Enable MSDCPLL SSC bit [6]: Enable TVDPLL SSC

10209F2C **FHCTL_DSSC5_CON** **FHCTL Dynamic SSC RF5 Control (RF5 = WiFi)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										DYSSC_RF5_BAN						
Type										RW						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										DYSSC_RF5_SSC						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
22:16		DYSSC_RF5_BAN	**Enables RF5 (WiFi) BAN for each PLL** bit [0]: Enable ARMPLL BAN bit [1]: Enable MAINPLL BAN bit [2]: Enable MEMPLL BAN bit [3]: Enable MMPLL BAN bit [4]: Enable VENCPLL BAN bit [5]: Enable MSDCPLL BAN bit [6]: Enable TVDPLL BAN
6:0		DYSSC_RF5_SSC	**Enables RF5 (WiFi) SSC for each PLL** bit [0]: Enable ARMPLL SSC bit [1]: Enable MAINPLL SSC bit [2]: Enable MEMPLL SSC bit [3]: Enable MMPLL SSC bit [4]: Enable VENCPLL SSC bit [5]: Enable MSDCPLL SSC bit [6]: Enable TVDPLL SSC

10209F30 **FHCTL_DSSC6_CON** **FHCTL Dynamic SSC RF6 Control (RF6 = FM)** **00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										DYSSC_RF6_BAN						
Type										RW						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										DYSSC_RF6_SSC						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
22:16		DYSSC_RF6_BAN	**Enables RF6 (FM) BAN for each PLL** bit [0]: Enable ARMPLL BAN bit [1]: Enable MAINPLL BAN bit [2]: Enable MEMPLL BAN bit [3]: Enable MMPLL BAN bit [4]: Enable VENCPLL BAN bit [5]: Enable MSDCPLL BAN bit [6]: Enable TVDPLL BAN
6:0		DYSSC_RF6_SSC	**Enables RF6 (FM) SSC for each PLL** bit [0]: Enable ARMPLL SSC bit [1]: Enable MAINPLL SSC bit [2]: Enable MEMPLL SSC bit [3]: Enable MMPLL SSC bit [4]: Enable VENCPLL SSC bit [5]: Enable MSDCPLL SSC bit [6]: Enable TVDPLL SSC

10209F34 **FHCTL_DSSC7_CON** **FHCTL Dynamic SSC RF7 Control (RF7 = GPS)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										DYSSC_RF7_BAN						
Type										RW						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										DYSSC_RF7_SSC						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
22:16		DYSSC_RF7_BAN	**Enables RF7 (GPS) BAN for each PLL** bit [0]: Enable ARMPLL BAN bit [1]: Enable MAINPLL BAN bit [2]: Enable MEMPLL BAN bit [3]: Enable MMPLL BAN bit [4]: Enable VENCPLL BAN bit [5]: Enable MSDCPLL BAN bit [6]: Enable TVDPLL BAN
6:0		DYSSC_RF7_SSC	**Enables RF7 (GPS) SSC for each PLL** bit [0]: Enable ARMPLL SSC bit [1]: Enable MAINPLL SSC bit [2]: Enable MEMPLL SSC bit [3]: Enable MMPLL SSC bit [4]: Enable VENCPLL SSC bit [5]: Enable MSDCPLL SSC bit [6]: Enable TVDPLL SSC

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10209F38 FHCTL0_CFG FHCTL0 (ARMPLL) Config 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FRDDS0_DYS				FRDDS0_DTS			
Type									RW				RW			
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FHCTL0_MON_SEL		SFSTR0_MODE	FHCTL0_PAUSE	DYSSC0_EN	SFSTR0_EN	FRDDS0_EN	FHCTL0_EN
Type									RW		RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:20		FRDDS0_DYS	**FHCTL0 (ARMPLL) free-run mode (SSC) delta freq. of each step** Frequency step (PLL OUTPUT Freq.) = (deltaY)*26MHz (REF_CLK) 4'd00: + 0.000061035 4'd01: + 0.000122070 4'd02: + 0.000244141 4'd03: + 0.000488281 4'd04: + 0.000976562 4'd05: + 0.001953125 4'd06: + 0.003906250 4'd07: + 0.007812500 4'd08: + 0.015625000 4'd09: + 0.023437500 4'd10: + 0.031250000 4'd11: + 0.046875000 4'd12: + 0.062500000 4'd13: + 0.093750000 4'd14: + 0.125000000 4'd15 + 0.250000000
19:16		FRDDS0_DTS	**FHCTL0 (ARMPLL) free-run mode (SSC) delta time of each step (T = 26MHz clock period)** 4'd00: 0.3077us (8T) 4'd01: 0.5385us (14T) 4'd02: 0.8077us (21T) 4'd03: 1.038us (27T) 4'd04: 1.308us (34T) 4'd05: 1.538us (40T) 4'd06: 1.808us (47T) 4'd07: 2.038us (53T) 4'd08: 2.308us (60T) 4'd09: 2.538us (66T) 4'd10: 2.808us (73T) 4'd11: 3.038us (79T) 4'd12: 4.038us (105T) 4'd13: 8.038us (209T) 4'd14: 10.038us (261T) 4'd15: 20.038us (521T)
7:6		FHCTL0_MON_SEL	**FHCTL0 (ARMPLL) monitor select of MON[20:0]** 0: FHCTL_PLL_DDS[20:0] 1: FHCTL_PLL_DDS[20:0] 2: FHCTL_UPLMT[20:0] 3: FHCTL_DNLMT[20:0]
5		SFSTR0_MODE	**FHCTL0 (ARMPLL) soft-start slope mode** 0: Multi-slope 1: Uni-slope

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Bit(s)	Mnemonic	Name	Description
4		FHCTL0_PAUSE	**FHCTL0 (ARMPLL) pause hopping FSM** 0: No pause 1: Pause
3		DYSSC0_EN	**FHCTL0 (ARMPLL) dynamic SSC on** 0: No dynamic SSC 1: Dynamic SSC
2		SFSTR0_EN	**FHCTL0 (ARMPLL) soft-start mode (hopping) on/off** 0: Disable 1: Enable
1		FRDDS0_EN	**FHCTL0 (ARMPLL) free-run mode (SSC) on/off** 0: Disable 1: Enable
0		FHCTL0_EN	**FHCTL0 (ARMPLL) hopping controller on/off** 0: Disable hopping & SSC 1: Enable hopping & SSC

10209F3C **FHCTL0_UPD NLMT** **FHCTL0 (ARMPLL) Up/Down Limit** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FRDDS0_DNLMT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FRDDS0_UPLMT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		FRDDS0_DNLMT	**FHCTL0 (ARMPLL) down-limit setting for free-run DDS** The down limit of DDS = current_DDS[20:0] - {FRDDS1_DNLMT[15:0],5'b0} current_DDS[20:14]: Integer current_DDS[13:0]: Fraction 0: Down limit = Current DDS - 0 1: Down limit = Current DDS - 32 ... 4094: Down limit = Current DDS - 4094*32 4095: Down limit = Current DDS - 4095*32
15:0		FRDDS0_UPLMT	**FHCTL0 (ARMPLL) upper-limit setting for free-run DDS** The upper limit of DDS = current_DDS[20:0] + {FRDDS1_UPLMT[15:0], 5'b0} current_DDS[20:14]: Integer current_DDS[13:0]: Fraction 0: Down limit = Current DDS + 0 1: Down limit = Current DDS + 32 ... 4094: Down limit = Current DDS + 4094*32 4095: Down limit = Current DDS + 4095*32

10209F40 **FHCTL0_DDS** **FHCTL0 (ARMPLL) DDS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	**FHCTLo_PLL_TGL_ORG**											**FHCTLo_PLL_ORG[20:16]**				
Type	A1											RW				
Reset	0											0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**FHCTLo_PLL_ORG[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		FHCTLo_PLL_TGL_ORG	**FHCTLo (ARMPLL)** PLL TOGGLE, write 1 to trigger SW setting NCPO
20:0		FHCTLo_PLL_ORG	**FHCTLo (ARMPLL)** PLL DDS value, 8 bit integer + 14 bit fraction

10209F44 FHCTLo_DVFS FHCTLo (ARMPLL) DVFS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**FHCTLo_PLL_DVFS_TRI**											**FHCTLo_PLL_DVFS[20:16]**				
Type	A1											RW				
Reset	0											0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**FHCTLo_PLL_DVFS[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		FHCTLo_PLL_DVFS_TRI	**FHCTLo (ARMPLL)** PLL DVFS trigger Write 1 to trigger DVFS setting NCPO.
20:0		FHCTLo_PLL_DVFS	**FHCTLo (ARMPLL)** DVFS target NCPO It changes the NCPO of FHCTLo_PLL_ORG.

10209F48 FHCTLo_MON FHCTLo (ARMPLL) Monitor 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**FHCTLo_PAUSE**	**FHCTLo_PRD**	**SFSTRo_PRD**	**FRDDSo_PRD**	**FHCTLo_STATE**						**FHCTLo_PLL_CHG**	**FHCTLo_PLL_DDS[20:16]**				
Type	RO	RO	RO	RO	RO						RO	RO				
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**FHCTLo_PLL_DDS[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31		FHCTL0_PAUSE	FHCTL0 (ARMPLL) pause status
30		FHCTL0_PRD	FHCTL0 (ARMPLL) hopping period
29		SFSTR0_PRD	FHCTL0 (ARMPLL) soft-start (DVFS) period
28		FRDDS0_PRD	FHCTL0 (ARMPLL) free-run (DDS) period
27:24		FHCTL0_STATE	FHCTL0 (ARMPLL) multi-slope stage
21		FHCTL0_PLL_CHG	FHCTL0 (ARMPLL) PLL_CHG of ANALOG I/F
20:0		FHCTL0_PLL_DDS	FHCTL0 (ARMPLL) PLL_DDS of ANALOG I/F

10209F4C **FHCTL1_CFG** **FHCTL1(MAINPLL) Config** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FRDDS1_DYS				FRDDS1_DTS			
Type									RW				RW			
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FHCTL1_MON_SEL		SFSTR1_MODE	FHCTL1_PAUSE	DYSSC1_EN	SFSTR1_EN	FRDDS1_EN	FHCTL1_EN
Type									RW		RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:20		FRDDS1_DYS	**FHCTL1 (MAINPLL) free-run mode (SSC) delta freq. of each step** Frequency step (PLL OUTPUT Freq.) = (deltaY)*26MHz (REF_CLK) 4'd00: + 0.000061035 4'd01: + 0.000122070 4'd02: + 0.000244141 4'd03: + 0.000488281 4'd04: + 0.000976562 4'd05: + 0.001953125 4'd06: + 0.003906250 4'd07: + 0.007812500 4'd08: + 0.015625000 4'd09: + 0.023437500 4'd10: + 0.031250000 4'd11: + 0.046875000 4'd12: + 0.062500000 4'd13: + 0.093750000 4'd14: + 0.125000000 4'd15: + 0.250000000
19:16		FRDDS1_DTS	**FHCTL1 (MAINPLL) free-run mode (SSC) delta time of each step (T = 26MHz clock period)** 4'd00: 0.3077us (8T) 4'd01: 0.5385us (14T) 4'd02: 0.8077us (21T) 4'd03: 1.038us (27T) 4'd04: 1.308us (34T) 4'd05: 1.538us (40T) 4'd06: 1.808us (47T) 4'd07: 2.038us (53T) 4'd08: 2.308us (60T) 4'd09: 2.538us (66T) 4'd10: 2.808us (73T)

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Bit(s)	Mnemonic	Name	Description
			4'd11: 3.038us (79T) 4'd12: 4.038us (105T) 4'd13: 8.038us (209T) 4'd14: 10.038us (261T) 4'd15: 20.038us (521T)
7:6		FHCTL1_MON_SEL	**FHCTL1 (MAINPLL) monitor select of MON[20:0]** 0: FHCTL_PLL_DDS[20:0] 1: FHCTL_PLL_DDS[20:0] 2: FHCTL_UPLMT[20:0] 3: FHCTL_DNLMT[20:0]
5		SFSTR1_MODE	**FHCTL1 (MAINPLL) soft-start slope mode** 0: Multi-slope 1: Uni-slope
4		FHCTL1_PAUSE	**FHCTL1 (MAINPLL) pause hopping FSM** 0: No pause 1: Pause
3		DYSSC1_EN	**FHCTL1 (MAINPLL) dynamic SSC on** 0: No Dynamic SSC 1: Dynamic SSC
2		SFSTR1_EN	**FHCTL1 (MAINPLL) soft-start mode (hopping) on/off** 0: Disable 1: Enable
1		FRDDS1_EN	**FHCTL1 (MAINPLL) free-run mode (SSC) on/off** 0: Disable 1: Enable
0		FHCTL1_EN	**FHCTL1 (MAINPLL) hopping controller on/off** 0: Disable hopping & SSC 1: Enable hopping & SSC

10209F50 **FHCTL1_UPDNLMT** **FHCTL1 (MAINPLL) Up/Down Limit** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FRDDS1_DNLMT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FRDDS1_UPLMT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		FRDDS1_DNLMT	**FHCTL1 (MAINPLL) down-limit setting for free-run DDS** The down limit of DDS = Current_DDS[20:0] - {FRDDS1_DNLMT[15:0],5'b0} current_DDS[20:14]: Integer current_DDS[13:0]: Fraction 0: Down limit = Current DDS - 0 1: Down limit = Current DDS - 32 ... 4094: Down limit = Current DDS - 4094*32 4095: Down limit = Current DDS - 4095*32
15:0		FRDDS1_UPLMT	**FHCTL1 (MAINPLL) upper-limit setting for free-run DDS** The upper limit of DDS = current_DDS[20:0] +

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Bit(s)	Mnemonic	Name	Description
			{FRDDS1_UPLMT[15:0], 5'b0} current_DDS[20:14]: Integer current_DDS[13:0]: Fraction 0: Down limit = Current DDS + 0 1: Down limit = Current DDS + 32 ... 4094: Down limit = Current DDS + 4094*32 4095: Down limit = Current DDS + 4095*32

10209F54 FHCTL1_DDS FHCTL1 (MAINPLL) DDS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FHCTL1_PLL_TGL_ORG											FHCTL1_PLL_ORG[20:16]				
Type	A1											RW				
Reset	0											0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FHCTL1_PLL_ORG[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		FHCTL1_PLL_TGL_ORG	**FHCTL1 (MAINPLL)** PLL TOGGLE Write 1 to trigger SW setting NCPO.
20:0		FHCTL1_PLL_ORG	**FHCTL1 (MAINPLL)** PLL DDS value, 8 bit integer + 14 bit fraction

10209F58 FHCTL1_DVFS FHCTL1 (MAINPLL) DVFS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FHCTL1_PLL_DVFS_TRI											FHCTL1_PLL_DVFS[20:16]				
Type	A1											RW				
Reset	0											0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FHCTL1_PLL_DVFS[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		FHCTL1_PLL_DVFS_TRI	**FHCTL1 (MAINPLL)** PLL DVFS trigger Write 1 to trigger DVFS setting NCPO.
20:0		FHCTL1_PLL_DVFS	**FHCTL1 (MAINPLL)** DVFS target NCPO It changes the NCPO of FHCTL1_PLL_ORG.

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10209F5C FHCTL1_MON FHCTL1 (MAINPLL) Monitor 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FHCTL1_PAUSE	FHCTL1_PRD	SFSTR1_PRD	FRDDS1_PRD	FHCTL1_STATE						FHCTL1_PLL_CHG	FHCTL1_PLL_DDS[20:16]				
Type	RO	RO	RO	RO	RO						RO	RO				
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FHCTL1_PLL_DDS[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		FHCTL1_PAUSE	FHCTL1 (MAINPLL) pause status
30		FHCTL1_PRD	FHCTL1 (MAINPLL) hopping period
29		SFSTR1_PRD	FHCTL1 (MAINPLL) soft-start (DVFS) period
28		FRDDS1_PRD	FHCTL1 (MAINPLL) free-run (DDS) period
27:24		FHCTL1_STATE	FHCTL1 (MAINPLL) multi-slope stage
21		FHCTL1_PLL_CHG	FHCTL1 (MAINPLL) PLL_CHG of ANALOG I/F
20:0		FHCTL1_PLL_DDS	FHCTL1 (MAINPLL) PLL_DDS of ANALOG I/F

10209F60 FHCTL2_CFG FHCTL2 (MEMPLL) Config 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FRDDS2_DYS				FRDDS2_DTS			
Type									RW				RW			
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FHCTL2_MON_SEL		SFSTR2_MODE	FHCTL2_PAUSE	DYSSC2_EN	SFSTR2_EN	FRDDS2_EN	FHCTL2_EN
Type									RW		RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:20		FRDDS2_DYS	**FHCTL2 (MEMPLL) free-run mode (SSC) delta freq. of each step** Frequency step (PLL OUTPUT Freq.) = (deltaY)*26MHz (REF_CLK) 4'd00: + 0.000061035 4'd01: + 0.000122070 4'd02: + 0.000244141 4'd03: + 0.000488281 4'd04: + 0.000976562 4'd05: + 0.001953125 4'd06: + 0.003906250 4'd07: + 0.007812500 4'd08: + 0.015625000 4'd09: + 0.023437500 4'd10: + 0.031250000 4'd11: + 0.046875000 4'd12: + 0.062500000 4'd13: + 0.093750000 4'd14: + 0.125000000 4'd15: + 0.250000000

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Bit(s)	Mnemonic	Name	Description
19:16		FRDDS2_DTS	**FHCTL2 (MEMPLL) free-run mode (SSC) delta time of each step (T = 26MHz clock period)** 4'd00: 0.3077us (8T) 4'd01: 0.5385us (14T) 4'd02: 0.8077us (21T) 4'd03: 1.038us (27T) 4'd04: 1.308us (34T) 4'd05: 1.538us (40T) 4'd06: 1.808us (47T) 4'd07: 2.038us (53T) 4'd08: 2.308us (60T) 4'd09: 2.538us (66T) 4'd10: 2.808us (73T) 4'd11: 3.038us (79T) 4'd12: 4.038us (105T) 4'd13: 8.038us (209T) 4'd14:10.038us (261T) 4'd15:20.038us (521T)
7:6		FHCTL2_MON_SEL	**FHCTL2 (MEMPLL) monitor select of MON[20:0]** 0: FHCTL_PLL_DDS[20:0] 1: FHCTL_PLL_DDS[20:0] 2: FHCTL_UPLMT[20:0] 3: FHCTL_DNLMT[20:0]
5		SFSTR2_MODE	**FHCTL2 (MEMPLL) soft-start slope mode** 0: Multi-slope 1: Uni-slope
4		FHCTL2_PAUSE	**FHCTL2 (MEMPLL) pause hopping FSM** 0: No pause 1: Pause
3		DYSSC2_EN	**FHCTL2 (MEMPLL) dynamic SSC on** 0: No dynamic SSC 1: Dynamic SSC
2		SFSTR2_EN	**FHCTL2 (MEMPLL) soft-start mode (hopping) on/off** 0: Disable 1: Enable
1		FRDDS2_EN	**FHCTL2 (MEMPLL) free-run mode (SSC) on/off** 0: Disable 1: Enable
0		FHCTL2_EN	**FHCTL2 (MEMPLL) hopping controller on/off** 0: Disable hopping & SSC 1: Enable hopping & SSC

10209F64 **FHCTL2_UPD NLMT** **FHCTL2 (MEMPLL) Up/Down Limit** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FRDDS2_DNLMT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FRDDS2_UPLMT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
31:16		FRDDS2_DNLMT	**FHCTL2 (MEMPLL) down-limit setting for free-run DDS** The down limit of DDS = current_DDS[20:0] - {FRDDS1_DNLMT[15:0],5'b0} current_DDS[20:14]: Integer current_DDS[13:0]: Fraction 0: Down limit = Current DDS - 0 1: Down limit = Current DDS - 32 ... 4094: Down limit = Current DDS - 4094*32 4095 : Down limit = Current DDS - 4095*32
15:0		FRDDS2_UPLMT	**FHCTL2 (MEMPLL) upper-limit setting for free-run DDS** The upper limit of DDS = current_DDS[20:0] + {FRDDS1_UPLMT[15:0], 5'b0} current_DDS[20:14]: Integer current_DDS[13:0]: Fraction 0: Down limit = Current DDS + 0 1: Down limit = Current DDS + 32 ... 4094: Down limit = Current DDS + 4094*32 4095: Down limit = Current DDS + 4095*32

10209F68 **FHCTL2_DDS** **FHCTL2 (MEMPLL) DDS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FHCTL2_PLL_TGL_ORG											FHCTL2_PLL_ORG[20:16]				
Type	A1											RW				
Reset	0											0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FHCTL2_PLL_ORG[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		FHCTL2_PLL_TGL_ORG	**FHCTL2 (MEMPLL)** PLL toggle Write 1 to trigger SW setting NCPO.
20:0		FHCTL2_PLL_ORG	**FHCTL2 (MEMPLL)** PLL DDS value, 8 bit integer + 14 bit fraction

10209F6C **FHCTL2_DVFS** **FHCTL2 (MEMPLL) DVFS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FHCTL2_PLL_DVFS_TRI											FHCTL2_PLL_DVFS[20:16]				
Type	A1											RW				
Reset	0											0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FHCTL2_PLL_DVFS[15:0]															

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Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		FHCTL2_PLL_DVFS_TRI	**FHCTL2 (MEMPLL)** PLL DVFS trigger Write 1 to trigger DVFS setting NCPO.
20:0		FHCTL2_PLL_DVFS	**FHCTL2 (MEMPLL)** DVFS target NCPO It changes the NCPO of FHCTL2_PLL_ORG.

10209F70 FHCTL2_MON FHCTL2 (MEMPLL) Monitor 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**FHCTL2_PAUSE**	**FHCTL2_PRD**	**SFSTR2_PRD**	**FRDDS2_PRD**	**FHCTL2_STATE**						**FHCTL2_PLL_CHG**	**FHCTL2_PLL_DDS[20:16]**				
Type	RO	RO	RO	RO	RO						RO	RO				
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**FHCTL2_PLL_DDS[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		FHCTL2_PAUSE	FHCTL2 (MEMPLL) pause status
30		FHCTL2_PRD	FHCTL2 (MEMPLL) hopping period
29		SFSTR2_PRD	FHCTL2 (MEMPLL) soft-start (DVFS) period
28		FRDDS2_PRD	FHCTL2 (MEMPLL) free-run (DDS) period
27:24		FHCTL2_STATE	FHCTL2 (MEMPLL) multi-slope stage
21		FHCTL2_PLL_CHG	FHCTL2 (MEMPLL) PLL_CHG of ANALOG I/F
20:0		FHCTL2_PLL_DDS	FHCTL2 (MEMPLL) PLL_DDS of ANALOG I/F

10209F74 FHCTL3_CFG FHCTL3 (MMPLL) Config 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									**FRDDS3_DYS**				**FRDDS3_DTS**			
Type									RW				RW			
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**FHCTL3_MON_SEL**		**SFSTR3_MODE**	**FHCTL3_PAUSE**	**DYSSC3_EN**	**SFSTR3_EN**	**FRDDS3_EN**	**FHCTL3_EN**
Type									RW		RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:20		FRDDS3_DYS	**FHCTL3 (MMPLL) free-run mode (SSC) delta freq. of each step** Frequency step (PLL OUTPUT Freq.) = (deltaY)*26MHz (REF_CLK) 4'd00: + 0.000061035

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Bit(s)	Mnemonic	Name	Description
			4'd01: + 0.000122070 4'd02: + 0.000244141 4'd03: + 0.000488281 4'd04: + 0.000976562 4'd05: + 0.001953125 4'd06: + 0.003906250 4'd07: + 0.007812500 4'd08: + 0.015625000 4'd09: + 0.023437500 4'd10: + 0.031250000 4'd11: + 0.046875000 4'd12: + 0.062500000 4'd13: + 0.093750000 4'd14: + 0.125000000 4'd15: + 0.250000000
19:16		FRDDS3_DTS	**FHCTL3 (MMPLL) free-run mode (SSC) delta time of each step (T = 26MHz clock period)** 4'd00: 0.3077us (8T) 4'd01: 0.5385us (14T) 4'd02: 0.8077us (21T) 4'd03: 1.038us (27T) 4'd04: 1.308us (34T) 4'd05: 1.538us (40T) 4'd06: 1.808us (47T) 4'd07: 2.038us (53T) 4'd08: 2.308us (60T) 4'd09: 2.538us (66T) 4'd10: 2.808us (73T) 4'd11: 3.038us (79T) 4'd12: 4.038us (105T) 4'd13: 8.038us (209T) 4'd14: 10.038us (261T) 4'd15: 20.038us (521T)
7:6		FHCTL3_MON_SEL	**FHCTL3 (MMPLL) monitor select of MON[20:0]** 0: FHCTL_PLL_DDS[20:0] 1: FHCTL_PLL_DDS[20:0] 2: FHCTL_UPLMT[20:0] 3: FHCTL_DNLMT[20:0]
5		SFSTR3_MODE	**FHCTL3 (MMPLL) soft-start slope mode** 0: Multi-slope 1: Uni-slope
4		FHCTL3_PAUSE	**FHCTL3 (MMPLL) pause hopping FSM** 0: No pause 1: Pause
3		DYSSC3_EN	**FHCTL3 (MMPLL) dynamic SSC on** 0: No dynamic SSC 1: Dynamic SSC
2		SFSTR3_EN	**FHCTL3 (MMPLL) soft-start mode (hopping) on/off** 0: Disable 1: Enable
1		FRDDS3_EN	**FHCTL3 (MMPLL) free-run mode (SSC) on/off** 0: Disable 1: Enable
0		FHCTL3_EN	**FHCTL3 (MMPLL) hopping controller on/off** 0: Disable hopping & SSC 1: Enable hopping & SSC

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10209F78 FHCTL3_UPDNLMT FHCTL3 (MMPLL) Up/Down Limit 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FRDDS3_DNLMT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FRDDS3_UPLMT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		FRDDS3_DNLMT	**FHCTL3 (MMPLL) down-limit setting for free-run DDS** The down limit of DDS = current_DDS[20:0] - {FRDDS1_DNLMT[15:0],5'b0} current_DDS[20:14]: Integer current_DDS[13:0]: Fraction 0: Down limit = Current DDS - 0 1: Down limit = Current DDS - 32 ... 4094: Down limit = Current DDS - 4094*32 4095: Down limit = Current DDS - 4095*32
15:0		FRDDS3_UPLMT	**FHCTL3 (MMPLL) upper-limit setting for free-run DDS** The upper limit of DDS = current_DDS[20:0] + {FRDDS1_UPLMT[15:0], 5'b0} current_DDS[20:14]: Integer current_DDS[13:0]: Fraction 0: Down limit = Current DDS + 0 1: Down limit = Current DDS + 32 ... 4094: Down limit = Current DDS + 4094*32 4095: Down limit = Current DDS + 4095*32

10209F7C FHCTL3_DDS FHCTL3 (MMPLL) DDS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FHCTL3_PLL_TGL_ORG											FHCTL3_PLL_ORG[20:16]				
Type	A1											RW				
Reset	0											0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FHCTL3_PLL_ORG[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		FHCTL3_PLL_TGL_ORG	**FHCTL3 (MMPLL)** PLL toggle Write 1 to trigger SW setting NCPO.
20:0		FHCTL3_PLL_ORG	**FHCTL3 (MMPLL)** PLL DDS value, 8 bit integer + 14 bit fraction

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10209F80 FHCTL3_DVFS FHCTL3 (MMPLL) DVFS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FHCTL3_PLL_DVFS_TRI											FHCTL3_PLL_DVFS[20:16]				
Type	A1											RW				
Reset	0											0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FHCTL3_PLL_DVFS[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		FHCTL3_PLL_DVFS_TRI	**FHCTL3 (MMPLL)** PLL DVFS trigger Write 1 to trigger DVFS setting NCPO.
20:0		FHCTL3_PLL_DVFS	**FHCTL3 (MMPLL)** DVFS target NCPO It changes the NCPO of FHCTL3_PLL_ORG.

10209F84 FHCTL3_MON FHCTL3 (MMPLL) Monitor 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FHCTL3_PAUSE	FHCTL3_PRD	SFSTR3_PRD	FRDDS3_PRD	FHCTL3_STATE						FHCTL3_PLL_CHG	FHCTL3_PLL_DDS[20:16]				
Type	RO	RO	RO	RO	RO						RO	RO				
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FHCTL3_PLL_DDS[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		FHCTL3_PAUSE	FHCTL3 (MMPLL) pause status
30		FHCTL3_PRD	FHCTL3 (MMPLL) hopping period
29		SFSTR3_PRD	FHCTL3 (MMPLL) soft-start (DVFS) period
28		FRDDS3_PRD	FHCTL3 (MMPLL) free-run (DDS) period
27:24		FHCTL3_STATE	FHCTL3 (MMPLL) multi-slope stage
21		FHCTL3_PLL_CHG	FHCTL3 (MMPLL) PLL_CHG of ANALOG I/F
20:0		FHCTL3_PLL_DDS	FHCTL3 (MMPLL) PLL_DDS of ANALOG I/F

10209F88 FHCTL4_CFG FHCTL4 (VENCPLL) Config 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FRDDS4_DYS				FRDDS4_DTS			
Type									RW				RW			
Reset									0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FHCTL4_MON_SEL		SFSTR4_MODE	FHCTL4_PAUSE	DYSSC4_EN	SFSTR4_EN	FRDDS4_EN	FHCTL4_EN
Type									RW		RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:20		FRDDS4_DYS	**FHCTL4 (VENCPLL) free-run mode (SSC) delta freq. of each step** Frequency step (PLL OUTPUT Freq.) = (deltaY)*26MHz (REF_CLK) 4'd00: + 0.000061035 4'd01: + 0.000122070 4'd02: + 0.000244141 4'd03: + 0.000488281 4'd04: + 0.000976562 4'd05: + 0.001953125 4'd06: + 0.003906250 4'd07: + 0.007812500 4'd08: + 0.015625000 4'd09: + 0.023437500 4'd10: + 0.031250000 4'd11: + 0.046875000 4'd12: + 0.062500000 4'd13: + 0.093750000 4'd14: + 0.125000000 4'd15: + 0.250000000
19:16		FRDDS4_DTS	**FHCTL4 (VENCPLL) free-run mode (SSC) delta time of each step (T = 26MHz clock period)** 4'd00: 0.3077us (8T) 4'd01: 0.5385us (14T) 4'd02: 0.8077us (21T) 4'd03: 1.038us (27T) 4'd04: 1.308us (34T) 4'd05: 1.538us (40T) 4'd06: 1.808us (47T) 4'd07: 2.038us (53T) 4'd08: 2.308us (60T) 4'd09: 2.538us (66T) 4'd10: 2.808us (73T) 4'd11: 3.038us (79T) 4'd12: 4.038us (105T) 4'd13: 8.038us (209T) 4'd14: 10.038us (261T) 4'd15: 20.038us (521T)
7:6		FHCTL4_MON_SEL	**FHCTL4 (VENCPLL) monitor select of MON[20:0]** 0: FHCTL_PLL_DDS[20:0] 1: FHCTL_PLL_DDS[20:0] 2: FHCTL_UPLMT[20:0] 3: FHCTL_DNLMT[20:0]
5		SFSTR4_MODE	**FHCTL4 (VENCPLL) soft-start slope mode** 0: Multi-slope 1: Uni-slope
4		FHCTL4_PAUSE	**FHCTL4 (VENCPLL) pause hopping FSM** 0: No pause 1: Pause
3		DYSSC4_EN	**FHCTL4 (VENCPLL) dynamic SSC on** 0: No dynamic SSC 1: Dynamic SSC
2		SFSTR4_EN	**FHCTL4 (VENCPLL) soft-start mode (hopping) on/off**

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Bit(s)	Mnemonic	Name	Description
			0: Disable 1: Enable
1		FRDDS4_EN	**FHCTL4 (VENCPLL) free-run mode (SSC) on/off** 0: Disable 1: Enable
0		FHCTL4_EN	**FHCTL4 (VENCPLL) hopping controller on/off** 0: Disable hopping & SSC 1: Enable hopping & SSC

10209F8C **FHCTL4_UPDNLMT** **FHCTL4 (VENCPLL) Up/Down Limit** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FRDDS4_DNLMT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FRDDS4_UPLMT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		FRDDS4_DNLMT	**FHCTL4 (VENCPLL) down-limit setting for free-run DDS** The down limit of DDS = current_DDS[20:0] - {FRDDS1_DNLMT[15:0],5'b0} current_DDS[20:14]: Integer current_DDS[13:0]: Fraction 0: Down limit = Current DDS - 0 1: Down limit = Current DDS - 32 ... 4094: Down limit = Current DDS - 4094*32 4095: Down limit = Current DDS - 4095*32
15:0		FRDDS4_UPLMT	**FHCTL4 (VENCPLL) upper-limit setting for free-run DDS** The upper limit of DDS = current_DDS[20:0] + {FRDDS1_UPLMT[15:0], 5'b0} current_DDS[20:14]: Integer current_DDS[13:0]: Fraction 0: Down limit = Current DDS + 0 1: Down limit = Current DDS + 32 ... 4094: Down limit = Current DDS + 4094*32 4095: Down limit = Current DDS + 4095*32

10209F90 **FHCTL4_DDS** **FHCTL4 (VENCPLL) DDS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FHCTL4_PLL_TGL_ORG											FHCTL4_PLL_ORG[20:16]				
Type	A1											RW				
Reset	0											0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FHCTL4_PLL_ORG[15:0]															

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Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		FHCTL4_PLL_TGL_ORG	**FHCTL4 (VENCPLL)** PLL toggle Write 1 to trigger SW setting NCPO.
20:0		FHCTL4_PLL_ORG	**FHCTL4 (VENCPLL)** PLL DDS value, 8 bit integer + 14 bit fraction

10209F94 **FHCTL4_DVFS** **FHCTL4 (VENCPLL) DVFS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FHCTL4_PLL_DVFS_TRI											FHCTL4_PLL_DVFS[20:16]				
Type	A1											RW				
Reset	0											0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FHCTL4_PLL_DVFS[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		FHCTL4_PLL_DVFS_TRI	**FHCTL4 (VENCPLL)** PLL DVFS trigger Write 1 to trigger DVFS setting NCPO.
20:0		FHCTL4_PLL_DVFS	**FHCTL4 (VENCPLL)** DVFS target NCPO It changes the NCPO of FHCTL4_PLL_ORG.

10209F98 **FHCTL4_MON** **FHCTL4 (VENCPLL) Monitor** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FHCTL4_PAUSE	FHCTL4_PRD	SFSTR4_PRD	FRDDS4_PRD	FHCTL4_STATE						FHCTL4_PLL_CHG	FHCTL4_PLL_DDS[20:16]				
Type	RO	RO	RO	RO	RO						RO	RO				
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FHCTL4_PLL_DDS[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		FHCTL4_PAUSE	FHCTL4 (VENCPLL) pause status
30		FHCTL4_PRD	FHCTL4 (VENCPLL) hopping period
29		SFSTR4_PRD	FHCTL4 (VENCPLL) soft-start (DVFS) period
28		FRDDS4_PRD	FHCTL4 (VENCPLL) free-run (DDS) period

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Bit(s)	Mnemonic	Name	Description
27:24		FHCTL4_STATE	FHCTL4 (VENCPLL) multi-slope stage
21		FHCTL4_PLL_CHG	FHCTL4 (VENCPLL) PLL_CHG of ANALOG I/F
20:0		FHCTL4_PLL_DDS	FHCTL4 (VENCPLL) PLL_DDS of ANALOG I/F

10209F9C FHCTL5_CFG FHCTL5 (MSDCPLL) Config 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FRDDS5_DYS				FRDDS5_DTS			
Type									RW				RW			
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FHCTL5_MON_SEL		SFSTR5_MODE	FHCTL5_PAUSE	DYSSC5_EN	SFSTR5_EN	FRDDS5_EN	FHCTL5_EN
Type									RW		RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:20		FRDDS5_DYS	**FHCTL5 (MSDCPLL) free-run mode (SSC) delta freq. of each step** Frequency step (PLL OUTPUT Freq.) = (deltaY)*26MHz (REF_CLK) 4'd00 : + 0.000061035 4'd01 : + 0.000122070 4'd02: + 0.000244141 4'd03: + 0.000488281 4'd04: + 0.000976562 4'd05: + 0.001953125 4'd06: + 0.003906250 4'd07: + 0.007812500 4'd08: + 0.015625000 4'd09: + 0.023437500 4'd10: + 0.031250000 4'd11: + 0.046875000 4'd12: + 0.062500000 4'd13: + 0.093750000 4'd14: + 0.125000000 4'd15: + 0.250000000
19:16		FRDDS5_DTS	**FHCTL5 (MSDCPLL) free-run mode (SSC) delta time of each step (T = 26MHz clock period)** 4'd00: 0.3077us (8T) 4'd01: 0.5385us (14T) 4'd02: 0.8077us (21T) 4'd03: 1.038us (27T) 4'd04: 1.308us (34T) 4'd05: 1.538us (40T) 4'd06: 1.808us (47T) 4'd07: 2.038us (53T) 4'd08: 2.308us (60T) 4'd09: 2.538us (66T) 4'd10: 2.808us (73T) 4'd11: 3.038us (79T) 4'd12: 4.038us (105T) 4'd13: 8.038us (209T) 4'd14: 10.038us (261T) 4'd15: 20.038us (521T)
7:6		FHCTL5_MON_SE	**FHCTL5 (MSDCPLL) monitor select of MON[20:0]**

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Bit(s)	Mnemonic	Name	Description
		L	0: FHCTL_PLL_DDS[20:0] 1: FHCTL_PLL_DDS[20:0] 2: FHCTL_UPLMT[20:0] 3: FHCTL_DNLMT[20:0]
5		SFSTR5_MODE	**FHCTL5 (MSDCPLL) soft-start slope mode** 0: Multi-slope 1: Uni-slope
4		FHCTL5_PAUSE	**FHCTL5 (MSDCPLL) pause hopping FSM** 0: No pause 1: Pause
3		DYSSC5_EN	**FHCTL5 (MSDCPLL) dynamic SSC on** 0: No dynamic SSC 1: Dynamic SSC
2		SFSTR5_EN	**FHCTL5 (MSDCPLL) soft-start mode (hopping) on/off** 0: Disable 1: Enable
1		FRDDS5_EN	**FHCTL5 (MSDCPLL) free-run mode (SSC) on/off** 0: Disable 1: Enable
0		FHCTL5_EN	**FHCTL5 (MSDCPLL) hopping controller on/off** 0: Disable hopping & SSC 1: Enable hopping & SSC

10209FA0 **FHCTL5_UPDNLMT** **FHCTL5 (MSDCPLL) Up/Down Limit** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FRDDS5_DNLMT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FRDDS5_UPLMT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		FRDDS5_DNLMT	**FHCTL5 (MSDCPLL) down-limit setting for free-run DDS** The down limit of DDS = current_DDS[20:0] - {FRDDS1_DNLMT[15:0],5'b0} current_DDS[20:14] : integer current_DDS[13:0] : fraction 0 : down limit = current dds - 0 1 : down limit = current dds - 32 ... 4094 : down limit = current dds - 4094*32 4095 : down limit = current dds - 4095*32
15:0		FRDDS5_UPLMT	**FHCTL5 (MSDCPLL) upper-limit setting for free-run DDS** The upper limit of DDS = current_DDS[20:0] + {FRDDS1_UPLMT[15:0], 5'b0} current_DDS[20:14]: Integer current_DDS[13:0]: Fraction 0: Down limit = Current DDS + 0 1: Down limit = Current DDS + 32 ... 4094: Down limit = Current DDS + 4094*32

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Bit(s)	Mnemonic	Name	Description
			4095: Down limit = Current DDS + 4095*32

10209FA4 FHCTL5_DDS FHCTL5 (MSDCPLL) DDS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FHCTL5_PLL_TGL_ORG											FHCTL5_PLL_ORG[20:16]				
Type	A1											RW				
Reset	0											0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FHCTL5_PLL_ORG[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		FHCTL5_PLL_TGL_ORG	**FHCTL5 (MSDCPLL)** PLL toggle Write 1 to trigger SW setting NCPO.
20:0		FHCTL5_PLL_ORG	**FHCTL5 (MSDCPLL)** PLL DDS value, 8 bit integer + 14 bit fraction

10209FA8 FHCTL5_DVFS FHCTL5 (MSDCPLL) DVFS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FHCTL5_PLL_DVFS_TRI											FHCTL5_PLL_DVFS[20:16]				
Type	A1											RW				
Reset	0											0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FHCTL5_PLL_DVFS[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		FHCTL5_PLL_DVFS_TRI	**FHCTL5 (MSDCPLL)** PLL DVFS trigger Write 1 to trigger DVFS setting NCPO.
20:0		FHCTL5_PLL_DVFS	**FHCTL5 (MSDCPLL)** DVFS target NCPO It changes the NCPO of FHCTL5_PLL_ORG.

10209FAC FHCTL5_MON FHCTL5 (MSDCPLL) Monitor 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FHCT	FHCT	SFST	FRDD	FHCTL5_STATE						FHCT	FHCTL5_PLL_DDS[20:16]				

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	L5_PAUSE	L5_PRD	R5_PRD	S5_PRD							L5_PLL_CHG					
Type	RO	RO	RO	RO	RO						RO	RO				
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**FHCTL5_PLL_DDS[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		FHCTL5_PAUSE	FHCTL5 (MSDCPLL) pause status
30		FHCTL5_PRD	FHCTL5 (MSDCPLL) hopping period
29		SFSTR5_PRD	FHCTL5 (MSDCPLL) soft-start (DVFS) period
28		FRDDS5_PRD	FHCTL5 (MSDCPLL) free-run (DDS) period
27:24		FHCTL5_STATE	FHCTL5 (MSDCPLL) multi-slope stage
21		FHCTL5_PLL_CHG	FHCTL5 (MSDCPLL) PLL_CHG of ANALOG I/F
20:0		FHCTL5_PLL_DDS	FHCTL5 (MSDCPLL) PLL_DDS of ANALOG I/F

10209FB0 FHCTL6_CFG FHCTL6 (TVDPLL) Config 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									**FRDDS6_DYS**				**FRDDS6_DTS**			
Type									RW				RW			
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**FHCTL6_MON_SEL**		**SFSTR6_MODE**	**FHCTL6_PAUSE**	**DYSSC6_EN**	**SFSTR6_EN**	**FRDDS6_EN**	**FHCTL6_EN**
Type									RW		RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:20		FRDDS6_DYS	**FHCTL6 (TVDPLL) free-run mode (SSC) delta freq. of each step** Frequency step (PLL OUTPUT Freq.) = (deltaY)*26MHz (REF_CLK) 4'd00: + 0.000061035 4'd01: + 0.000122070 4'd02: + 0.000244141 4'd03: + 0.000488281 4'd04: + 0.000976562 4'd05: + 0.001953125 4'd06: + 0.003906250 4'd07: + 0.007812500 4'd08: + 0.015625000 4'd09: + 0.023437500 4'd10: + 0.031250000 4'd11: + 0.046875000 4'd12: + 0.062500000 4'd13: + 0.093750000 4'd14: + 0.125000000 4'd15: + 0.250000000
19:16		FRDDS6_DTS	**FHCTL6 (TVDPLL) free-run mode (SSC) delta time of each step (T = 26MHz clock period)** 4'd00: 0.3077us (8T) 4'd01: 0.5385us (14T)

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Bit(s)	Mnemonic	Name	Description
			4'd02: 0.8077us (21T) 4'd03: 1.038us (27T) 4'd04: 1.308us (34T) 4'd05: 1.538us (40T) 4'd06: 1.808us (47T) 4'd07: 2.038us (53T) 4'd08: 2.308us (60T) 4'd09: 2.538us (66T) 4'd10: 2.808us (73T) 4'd11: 3.038us (79T) 4'd12: 4.038us (105T) 4'd13: 8.038us (209T) 4'd14: 10.038us (261T) 4'd15: 20.038us (521T)
7:6		FHCTL6_MON_SEL	**FHCTL6 (TVDPLL) monitor select of MON[20:0]** 0: FHCTL_PLL_DDS[20:0] 1: FHCTL_PLL_DDS[20:0] 2: FHCTL_UPLMT[20:0] 3: FHCTL_DNLMT[20:0]
5		SFSTR6_MODE	**FHCTL6 (TVDPLL) soft-start slope mode** 0: Multi-slope 1: Uni-slope
4		FHCTL6_PAUSE	**FHCTL6 (TVDPLL) pause hopping FSM** 0: No pause 1: Pause
3		DYSSC6_EN	**FHCTL6 (TVDPLL) dynamic SSC on** 0: No dynamic SSC 1: Dynamic SSC
2		SFSTR6_EN	**FHCTL6 (TVDPLL) soft-start mode (hopping) on/off** 0: Disable 1: Enable
1		FRDDS6_EN	**FHCTL6 (TVDPLL) free-run mode (SSC) on/off** 0: Disable 1: Enable
0		FHCTL6_EN	**FHCTL6 (TVDPLL) hopping controller on/off** 0: Disable hopping & SSC 1: Enable hopping & SSC

10209FB4 **FHCTL6_UPDNLMT** **FHCTL6 (TVDPLL) Up/Down Limit** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FRDDS6_DNLMT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FRDDS6_UPLMT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		FRDDS6_DNLMT	**FHCTL6 (TVDPLL) down-limit setting for free-run DDS** The down limit of DDS = current_DDS[20:0] - {FRDDS1_DNLMT[15:0],5'b0} current_DDS[20:14]: Integer

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Bit(s)	Mnemonic	Name	Description
			current_DDS[13:0]: Fraction 0: Down limit = Current DDS - 0 1: Down limit = Current DDS - 32 ... 4094: Down limit = Current DDS - 4094*32 4095: Down limit = Current DDS - 4095*32
15:0		FRDDS6_UPLMT	**FHCTL6 (TVDPLL) upper-limit setting for free-run DDS** The upper limit of DDS = current_DDS[20:0] + {FRDDS1_UPLMT[15:0], 5'b0} current_DDS[20:14]: Integer current_DDS[13:0]: Fraction 0: Down limit = Current DDS + 0 1: Down limit = Current DDS + 32 ... 4094: Down limit = Current DDS + 4094*32 4095: Down limit = Current DDS + 4095*32

10209FB8 FHCTL6_DDS FHCTL6 (TVDPLL) DDS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FHCTL6_PLL_TGL_ORG											FHCTL6_PLL_ORG[20:16]				
Type	A1											RW				
Reset	0											0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FHCTL6_PLL_ORG[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		FHCTL6_PLL_TGL_ORG	**FHCTL6 (TVDPLL)** PLL toggle Write 1 to trigger SW setting NCPO.
20:0		FHCTL6_PLL_ORG	**FHCTL6 (TVDPLL)** PLL DDS value, 8 bit integer + 14 bit fraction

10209FBC FHCTL6_DVFS FHCTL6 (TVDPLL) DVFS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FHCTL6_PLL_DVFS_TRI											FHCTL6_PLL_DVFS[20:16]				
Type	A1											RW				
Reset	0											0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FHCTL6_PLL_DVFS[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31		FHCTL6_PLL_DVFS_TRI	**FHCTL6 (TVDPLL)** PLL DVFS trigger Write 1 to trigger DVFS setting NCPO.
20:0		FHCTL6_PLL_DVFS	**FHCTL6 (TVDPLL)** DVFS target NCPO It changes the NCPO of FHCTL6_PLL_ORG.

10209FC0 FHCTL6_MON FHCTL6 (TVDPLL) Monitor 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FHCTL6_PAUSE	FHCTL6_PRD	SFSTR6_PRD	FRDDS6_PRD	FHCTL6_STATE						FHCTL6_PLL_CHG	FHCTL6_PLL_DDS[20:16]				
Type	RO	RO	RO	RO	RO						RO	RO				
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FHCTL6_PLL_DDS[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		FHCTL6_PAUSE	FHCTL6 (TVDPLL) pause status
30		FHCTL6_PRD	FHCTL6 (TVDPLL) hopping period
29		SFSTR6_PRD	FHCTL6 (TVDPLL) soft-start (DVFS) period
28		FRDDS6_PRD	FHCTL6 (TVDPLL) free-run (DDS) period
27:24		FHCTL6_STATE	FHCTL6 (TVDPLL) multi-slope stage
21		FHCTL6_PLL_CHG	FHCTL6 (TVDPLL) PLL_CHG of ANALOG I/F
20:0		FHCTL6_PLL_DDS	FHCTL6 (TVDPLL) PLL_DDS of ANALOG I/F

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5 Peripherals

5.1 Pericfg Controller

5.1.1 Introduction

The pericfg controller is used to control the reset, clock and bus setting of peripheral subsys. Each module inside the peripheral subsys has its own software reset and clock gated control (power-down control). The hardware DCM (Dynamic Clock Management) of the peripheral subsys is also controlled in the pericfg controller. Beside AP MCU, the modem MCU can also use this pericfg controller to control specific modules clock gated control (power-down control).

5.1.2 Features

- Supports software reset control of each module inside peripheral subsys
- Supports clock gated control of the modules insider peripheral subsys by AP MCU
- Supports clock gated control of the modules insider peripheral subsys by Modem1 MCU
- Supports clock gated control of the modules insider peripheral subsys by Modem2 MCU
- Supports DCM control of peripheral subsys
- Supports bus setting (bandwidth limit/way enable/...) of peripheral subsys

5.1.3 Block Diagram

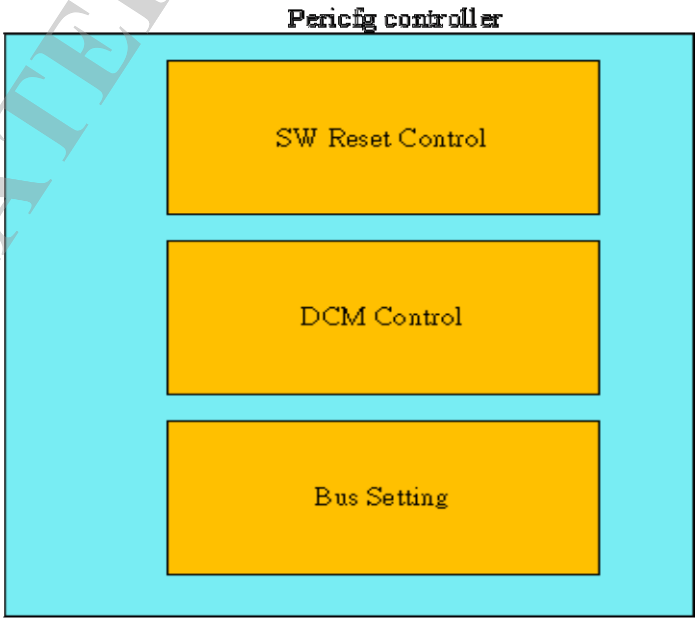

Figure 5-1. Block diagram of pericfg controller

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5.1.4 Register Definition

Module name: PERICFG Base address: (+10002000h)

Address	Name	Width	Register Function
10002000	PERI_GLOBALCON_RST0	32	Peripheral Software Reset Register 0
10002004	PERI_GLOBALCON_RST1	32	Peripheral Software Reset Register 1
10002008	PERI_GLOBALCON_PDN0_SET	32	Peripheral Power Down 0 Register Set
10002010	PERI_GLOBALCON_PDN0_CLR	32	Peripheral Power Down 0 Register Clear
10002018	PERI_GLOBALCON_PDN0_STA	32	Peripheral Power Down 0 Register Status
10002020	PERI_GLOBALCON_PDN_MD1_SET	32	Peripheral MD1 Power Down 0 Register Set
10002024	PERI_GLOBALCON_PDN_MD2_SET	32	Peripheral MD2 Power Down 0 Register Set
10002028	PERI_GLOBALCON_PDN_MD1_CLR	32	Peripheral MD1 Power Down 0 Register Clear
1000202C	PERI_GLOBALCON_PDN_MD2_CLR	32	Peripheral MD2 Power Down 0 Register Clear
10002030	PERI_GLOBALCON_PDN_MD1_STA	32	Peripheral MD1 Power Down 0 Register Status
10002034	PERI_GLOBALCON_PDN_MD2_STA	32	Peripheral MD2 Power Down 0 Register Status
10002038	PERI_GLOBALCON_PDN_MD_MASK	32	Peripheral MD Power Down Register MASK
10002050	PERI_GLOBALCON_DCMCTL	32	Peripheral DCM Control Register
10002054	PERI_GLOBALCON_DCMDBC	32	Peripheral DCM Debounce Counter
10002058	PERI_GLOBALCON_DCMFSEL	32	Peripheral DCM Frequency Selection
1000205C	PERI_GLOBALCON_CKSEL	32	Peripheral Clock Selection
100021F8	PERIAXI_BUS_CTL	32	Peripheral AXI Bus Control
100021FC	PERIAXI_BUS_CTL0	32	Peripheral AXI Bus Control 0
10002200	PERIAXI_BUS_CTL1	32	Peripheral AXI Bus Control 1
10002204	PERIAXI_BUS_CTL2	32	Peripheral AXI Bus Control 2
10002208	PERIAXI_SI0_CTL	32	Peripheral AXI SI0 Control
1000220C	PERIAXI_SI1_CTL	32	Peripheral AXI SI1 Control

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Address	Name	Width	Register Function
10002210	PERIAXI_MI_STA	32	Peripheral AXI MI Status
10002300	PERIAXI_AHB_LMT_CON1	32	Peripheral AHB Bus 0 Bandwidth Limiter
10002304	PERIAXI_AHB_LMT_CON2	32	Peripheral AHB Bus 0 Bandwidth Limiter
10002308	PERIAXI_AHB_LMT_CON3	32	Peripheral AHB Bus 1 Bandwidth Limiter
1000230C	PERIAXI_AHB_LMT_CON4	32	Peripheral AHB Bus 1 Bandwidth Limiter
10002310	PERIAXI_AHB_LMT_CON5	32	Peripheral AHB Bus 2 Bandwidth Limiter
10002314	PERIAXI_AHB_LMT_CON6	32	Peripheral AHB Bus 2 Bandwidth Limiter
10002320	PERIAXI_AXI_LMT_CON1	32	Peripheral AXI MST0 Bandwidth Limiter
10002324	PERIAXI_AXI_LMT_CON2	32	Peripheral AXI MST1 Bandwidth Limiter
10002328	PERIAXI_AXI_LMT_CON3	32	Peripheral AXI MST2 Bandwidth Limiter
1000232C	PERIAXI_AXI_LMT_CON4	32	Peripheral AP DMA Bandwidth Limiter
10002400	PERI_USB_WAKEUP_DEC_CON0	32	Peripheral USB Wakeup Control0
1000240C	PERI_UART_CK_SOURCE_SEL	32	Peripheral UART Clock Source Selection

10002000 **PERI_GLOBALCON_RST0** **Peripheral Software Reset Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				USB_SW_RST			I2C3_SW_RST	I2C2_SW_RST	I2C1_SW_RST	I2C0_SW_RST		MSDC1_SW_RST	MSDC0_SW_RST	MSDC3_SW_RST	MSDC2_SW_RST	THERM_SW_RST
Type				RW			RW	RW	RW	RW		RW	RW	RW	RW	RW
Reset				0			0	0	0	0		0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRTX_SW_RST	IRDA_SW_RST	DMA_SW_RST	AUXADC_SW_RST		PWM_SW_RST	DISP_PWM_SW_RST	BTIF_SW_RST		UART4_SW_RST	UART3_SW_RST	UART2_SW_RST	UART1_SW_RST	UART0_SW_RST
Type			RW	RW	RW	RW		RW	RW	RW		RW	RW	RW	RW	RW
Reset			0	0	0	0		0	0	0		0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28	**USB_SW_RST**	USB_SW_RST	**USB software-reset** 0: Does not reset USB 1: Reset USB
25	**I2C3_SW_RST**	I2C3_SW_RST	**I2C3 software-reset** 0: Does not reset I2C3 1: Reset I2C3
24	**I2C2_SW_**	I2C2_SW_RST	**I2C2 software-reset**

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Bit(s)	Mnemonic	Name	Description
	RST		0: Does not reset I2C2 1: Reset I2C2
23	I2C1_SW_RST	I2C1_SW_RST	**I2C1 software-reset** 0: Does not reset I2C1 1: Reset I2C1
22	I2C0_SW_RST	I2C0_SW_RST	**I2C0 software-reset** 0: Does not reset I2C0 1: Reset I2C0
20	MSDC1_SW_RST	MSDC1_SW_RST	**MSDC1 software-reset** 0: Does not reset MSDC1 1: Reset MSDC1
19	MSDC0_SW_RST	MSDC0_SW_RST	**MSDC0 software-reset** 0: Does not reset MSDC0 1: Reset MSDC0
18	MSDC3_SW_RST	MSDC3_SW_RST	**MSDC3 software-reset** 0: Does not reset MSDC3 1: Reset MSDC3
17	MSDC2_SW_RST	MSDC2_SW_RST	**MSDC2 software-reset** 0: Does not reset MSDC2 1: Reset MSDC2
16	THERM_SW_RST	THERM_SW_RST	**THERM software-reset** 0: Does not reset THERM 1: Reset THERM
13	IRTX_SW_RST	IRTX_SW_RST	**IRTX software-reset** 0: Does not reset IRTX 1: Reset IRTX
12	IRDA_SW_RST	IRDA_SW_RST	**IRDA software-reset** 0: Does not reset IRDA 1: Reset IRDA
11	DMA_SW_RST	DMA_SW_RST	**DMA software-reset** 0: Does not reset DMA 1: Reset DMA
10	AUXADC_SW_RST	AUXADC_SW_RST	**AUXADC software-reset** 0: Does not reset AUXADC 1: Reset AUXADC
8	PWM_SW_RST	PWM_SW_RST	**PWM software-reset** 0: Does not reset PWM 1: Reset PWM
7	DISP_PWM_SW_RST	DISP_PWM_SW_RST	**DISP_PWM software-reset** 0: Does not reset DISP_PWM 1: Reset DISP_PWM
6	BTIF_SW_RST	BTIF_SW_RST	**BTIF software-reset** 0: Does not reset BTIF 1: Reset BTIF
4	UART4_SW_RST	UART4_SW_RST	**UART4 software-reset** 0: Does not reset UART4 1: Reset UART4
3	UART3_SW_RST	UART3_SW_RST	**UART3 software-reset** 0: Does not reset UART3 1: Reset UART3
2	UART2_SW_RST	UART2_SW_RST	**UART2 software-reset** 0: Does not reset UART2 1: Reset UART2

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Bit(s)	Mnemonic	Name	Description
1	**UART1_SW_RST**	UART1_SW_RST	**UART1 software-reset** 0: Does not reset UART1 1: Reset UART1
0	**UART0_SW_RST**	UART0_SW_RST	**UART0 software-reset** 0: Does not reset UART0 1: Reset UART0

10002004 **PERI_GLOBALCON_RST1** **Peripheral Software Reset Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**SPI0_SW_RST**	
Type															RW	
Reset															0	

Bit(s)	Mnemonic	Name	Description
1	**SPI0_SW_RST**	SPI0_SW_RST	**SPI0 software-reset** 0: Does not reset SPI0 1: Reset SPI0

10002008 **PERI_GLOBALCON_PDN0_SET** **Peripheral Power Down 0 Register Set** **08000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			**IRTX_PDN**	**SPI0_PDN**	**AUXADC_PDN**	**I2C3_PDN**	**I2C2_PDN**	**I2C1_PDN**	**I2C0_PDN**	**BTIF_PDN**	**UART4_PDN**	**UART3_PDN**	**UART2_PDN**	**UART1_PDN**	**UART0_PDN**	**MSDC30_3_PDN**
Type			WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset			0	0	1	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MSDC30_2_PDN**	**MSDC30_1_PDN**	**MSDC30_0_PDN**	**AP_DMA_PDN**	**IRDA_PDN**	**USB0_PDN**	**PWM_PDN**	**PWM7_PDN**	**PWM6_PDN**	**PWM5_PDN**	**PWM4_PDN**	**PWM3_PDN**	**PWM2_PDN**	**PWM1_PDN**	**THERM_PDN**	**DISP_PWM_PDN**
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29	**IRTX_PDN**	IRTX_PDN_SET	**IRTX power-down** 0: Keep original value 1: Power down IRTX
28	**SPI0_PDN**	SPI0_PDN	**SPI0 power-down** 0: Keep original value 1: Power down SPI0
27	**AUXADC_PDN**	AUXADC_PDN	**AUXADC power-down** 0: Keep original value

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Bit(s)	Mnemonic	Name	Description
			1: Power down AUXADC
26	**I2C3_PDN**	I2C3_PDN	**I2C3 power-down** 0: Keep original value 1: Power down I2C2
25	**I2C2_PDN**	I2C2_PDN	**I2C2 power-down** 0: Keep original value 1: Power down I2C2
24	**I2C1_PDN**	I2C1_PDN	**I2C1 power-down** 0: Keep original value 1: Power down I2C1
23	**I2C0_PDN**	I2C0_PDN	**I2C0 power-down** 0: Keep original value 1: Power down I2C0
22	**BTIF_PDN**	BTIF_PDN	**BTIF power-down** 0: Keep original value 1: Power down BTIF
21	**UART4_PDN**	UART4_PDN	**UART4 power-down** 0: Keep original value 1: Power down UART4
20	**UART3_PDN**	UART3_PDN	**UART3 power-down** 0: Keep original value 1: Power down UART3
19	**UART2_PDN**	UART2_PDN	**UART2 power-down** 0: Keep original value 1: Power down UART2
18	**UART1_PDN**	UART1_PDN	**UART1 power-down** 0: Keep original value 1: Power down UART1
17	**UART0_PDN**	UART0_PDN	**UART0 power-down** 0: Keep original value 1: Power down UART0
16	**MSDC30_3_PDN**	MSDC30_3_PDN	**MSDC30_3 power-down** 0: Keep original value 1: Power down MSDC30_3
15	**MSDC30_2_PDN**	MSDC30_2_PDN	**MSDC30_2 power-down** 0: Keep original value 1: Power down MSDC30_2
14	**MSDC30_1_PDN**	MSDC30_1_PDN	**MSDC30_1 power-down** 0: Keep original value 1: Power down MSDC30_1
13	**MSDC30_0_PDN**	MSDC30_0_PDN	**MSDC30_0 power-down** 0: Keep original value 1: Power down MSDC30_0
12	**AP_DMA_PDN**	AP_DMA_PDN	**AP_DMA power-down** 0: Keep original value 1: Power down AP_DMA
11	**IRDA_PDN**	IRDA_PDN	**IRDA power-down** 0: Keep original value 1: Power down IRDA
10	**USB0_PDN**	USB0_PDN	**USB0 power-down** 0: Keep original value 1: Power down USB0

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Bit(s)	Mnemonic	Name	Description
9	**PWM_PDN**	PWM_PDN	**PWM power-down** 0: Keep original value 1: Power down PWM common logic
8	**PWM7_PDN**	PWM7_PDN	**PWM7 power-down** 0: Keep original value 1: Power down PWM7
7	**PWM6_PDN**	PWM6_PDN	**PWM6 power-down** 0: Keep original value 1: Power down PWM6
6	**PWM5_PDN**	PWM5_PDN	**PWM5 power-down** 0: Keep original value 1: Power down PWM5
5	**PWM4_PDN**	PWM4_PDN	**PWM4 power-down** 0: Keep original value 1: Power down PWM4
4	**PWM3_PDN**	PWM3_PDN	**PWM3 power-down** 0: Keep original value 1: Power down PWM3
3	**PWM2_PDN**	PWM2_PDN	**PWM2 power-down** 0: Keep original value 1: Power down PWM2
2	**PWM1_PDN**	PWM1_PDN	**PWM1 power-down** 0: Keep original value 1: Power down PWM1
1	**THERM_PDN**	THERM_PDN	**THERM power-down** 0: Keep original value 1: Power down THERM
0	**DISP_PWM_PDN**	DISP_PWM_PDN	**DISP_PWM power-down** 0: Keep original value 1: Power down DISP_PWM

10002010 **PERI_GLOBALCON_PDN0_CLR** **Peripheral Power Down 0 Register Clear** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRTX_PDN	SPI0_PDN	AUXADC_PDN	I2C3_PDN	I2C2_PDN	I2C1_PDN	I2C0_PDN	BTIF_PDN	UART4_PDN	UART3_PDN	UART2_PDN	UART1_PDN	UART0_PDN	MSDC30_3_PDN
Type			W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC30_2_PDN	MSDC30_1_PDN	MSDC30_0_PDN	AP_DMA_PDN	IRDA_PDN	USB0_PDN	PWM_PDN	PWM7_PDN	PWM6_PDN	PWM5_PDN	PWM4_PDN	PWM3_PDN	PWM2_PDN	PWM1_PDN	THERM_PDN	DISP_PWM_PDN
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29	**IRTX_PDN**	IRTX_PDN_SET	**IRTX_PDN clear power-down** 0: Keep original value 1: Clear power-down IRTX_PDN_SET

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Bit(s)	Mnemonic	Name	Description
28	**SPI0_PDN**	SPI0_PDN	**SPI0 clear power-down** 0: Keep original value 1: Clear power-down SPI0
27	**AUXADC_PDN**	AUXADC_PDN	**AUXADC clear power-down** 0: Keep original value 1: Clear power-down AUXADC
26	**I2C3_PDN**	I2C3_PDN	**I2C3 clear power-down** 0: Keep original value 1: Clear power-down I2C3
25	**I2C2_PDN**	I2C2_PDN	**I2C2 clear power-down** 0: Keep original value 1: Clear power-down I2C2
24	**I2C1_PDN**	I2C1_PDN	**I2C1 clear power-down** 0: Keep original value 1: Clear power-down I2C1
23	**I2C0_PDN**	I2C0_PDN	**I2C0 clear power-down** 0: Keep original value 1: Clear power-down I2C0
22	**BTIF_PDN**	BTIF_PDN	**BTIF clear power-down** 0: Keep original value 1: Clear power-down BTIF
21	**UART4_PDN**	UART4_PDN	**UART4 clear power-down** 0: Keep original value 1: Clear power-down UART4
20	**UART3_PDN**	UART3_PDN	**UART3 clear power-down** 0: Keep original value 1: Clear power-down UART3
19	**UART2_PDN**	UART2_PDN	**UART2 clear power-down** 0: Keep original value 1: Clear power-down UART2
18	**UART1_PDN**	UART1_PDN	**UART1 clear power-down** 0: Keep original value 1: Clear power-down UART1
17	**UART0_PDN**	UART0_PDN	**UART0 clear power-down** 0: Keep original value 1: Clear power-down UART0
16	**MSDC30_3_PDN**	MSDC30_3_PDN	**MSDC30_3 clear power-down** 0: Keep original value 1: Clear power-down MSDC30_3
15	**MSDC30_2_PDN**	MSDC30_2_PDN	**MSDC30_2 clear power-down** 0: Keep original value 1: Clear power-down MSDC30_2
14	**MSDC30_1_PDN**	MSDC30_1_PDN	**MSDC30_1 clear power-down** 0: Keep original value 1: Clear power-down MSDC30_1
13	**MSDC30_0_PDN**	MSDC30_0_PDN	**MSDC30_0 clear power-down** 0: Keep original value 1: Clear power-down MSDC30_0
12	**AP_DMA_PDN**	AP_DMA_PDN	**AP_DMA clear power-down** 0: Keep original value 1: Clear power-down AP_DMA
11	**IRDA_PDN**	IRDA_PDN	**IRDA clear power-down** 0: Keep original value

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Bit(s)	Mnemonic	Name	Description
			1: Clear power-down IRDA
10	**USB0_PDN**	USB0_PDN	**USB0 clear power-down** 0: Keep original value 1: Clear power-down USB0
9	**PWM_PDN**	PWM_PDN	**PWM clear power-down** 0: Keep original value 1: Clear power-down PWM7
8	**PWM7_PDN**	PWM7_PDN	**PWM7 clear power-down** 0: Keep original value 1: Clear power-down PWM7
7	**PWM6_PDN**	PWM6_PDN	**PWM6 clear power-down** 0: Keep original value 1: Clear power-down PWM6
6	**PWM5_PDN**	PWM5_PDN	**PWM5 clear power-down** 0: Keep original value 1: Clear power-down PWM5
5	**PWM4_PDN**	PWM4_PDN	**PWM4 clear power-down** 0: Keep original value 1: Clear power-down PWM4
4	**PWM3_PDN**	PWM3_PDN	**PWM3 clear power-down** 0: Keep original value 1: Clear power-down PWM3
3	**PWM2_PDN**	PWM2_PDN	**PWM2 clear power-down** 0: Keep original value 1: Clear power-down PWM2
2	**PWM1_PDN**	PWM1_PDN	**PWM1 clear power-down** 0: Keep original value 1: Clear power-down PWM1
1	**THERM_PDN**	THERM_PDN	**THERM clear power-down** 0: Keep original value 1: Clear power-down THERM
0	**DISP_PWM_PDN**	DISP_PWM_PDN	**DISP_PWM clear power-down** 0: Keep original value 1: Clear power-down DISP_PWM

10002018 **PERI_GLOBALCON_PDN0_STA** **Peripheral Power Down 0 Register Status** **08000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRTX_PDN	SPI0_PDN	AUXADC_PDN	I2C3_PDN	I2C2_PDN	I2C1_PDN	I2C0_PDN	BTIF_PDN	UART4_PDN	UART3_PDN	UART2_PDN	UART1_PDN	UART0_PDN	MSDC30_3_PDN
Type			RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset			0	0	1	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC30_2_PDN	MSDC30_1_PDN	MSDC30_0_PDN	AP_DMA_PDN	IRDA_PDN	USB0_PDN	PWM_PDN	PWM7_PDN	PWM6_PDN	PWM5_PDN	PWM4_PDN	PWM3_PDN	PWM2_PDN	PWM1_PDN	THERM_PDN	DISP_PWM_PDN
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
29	**IRTX_PDN**	IRTX_PDN_SET	**IRTX power-down** 0: Keep original value 1: Power down IRTX
28	**SPI0_PDN**	SPI0_PDN	**SPI0 power-down** 0: Keep original value 1: Power down SPI0
27	**AUXADC_PDN**	AUXADC_PDN	**AUXADC power-down** 0: Keep original value 1: Power down AUXADC
26	**I2C3_PDN**	I2C3_PDN	**I2C3 power-down** 0: Keep original value 1: Power down I2C3
25	**I2C2_PDN**	I2C2_PDN	**I2C2 power-down** 0: Keep original value 1: Power down I2C2
24	**I2C1_PDN**	I2C1_PDN	**I2C1 power-down** 0: Keep original value 1: Power down I2C1
23	**I2C0_PDN**	I2C0_PDN	**I2C0 power-down** 0: Keep original value 1: Power down I2C0
22	**BTIF_PDN**	BTIF_PDN	**BTIF power-down** 0: Keep original value 1: Power down BTIF
21	**UART4_PDN**	UART4_PDN	**UART4 power-down** 0: Keep original value 1: Power down UART4
20	**UART3_PDN**	UART3_PDN	**UART3 power-down** 0: Keep original value 1: Power down UART3
19	**UART2_PDN**	UART2_PDN	**UART2 power-down** 0: Keep original value 1: Power down UART2
18	**UART1_PDN**	UART1_PDN	**UART1 power-down** 0: Keep original value 1: Power down UART1
17	**UART0_PDN**	UART0_PDN	**UART0 power-down** 0: Keep original value 1: Power down UART0
16	**MSDC30_3_PDN**	MSDC30_3_PDN	**MSDC30_3 power-down** 0: Keep original value 1: Power down MSDC30_3
15	**MSDC30_2_PDN**	MSDC30_2_PDN	**MSDC30_2 power-down** 0: Keep original value 1: Power down MSDC30_2
14	**MSDC30_1_PDN**	MSDC30_1_PDN	**MSDC30_1 power-down** 0: Keep original value 1: Power down MSDC30_1
13	**MSDC30_0_PDN**	MSDC30_0_PDN	**MSDC30_0 power-down** 0: Keep original value 1: Power down MSDC30_0
12	**AP_DMA_PDN**	AP_DMA_PDN	**AP_DMA power-down** 0: Keep original value

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Bit(s)	Mnemonic	Name	Description
			1: Power down AP_DMA
11	IRDA_PDN	IRDA_PDN	**IRDA power-down** 0: Keep original value 1: Power down IRDA
10	USB0_PDN	USB0_PDN	**USB0 power-down** 0: Keep original value 1: Power down USB0
9	PWM_PDN	PWM_PDN	**PWM power-down** 0: Keep original value 1: Power down PWM7
8	PWM7_PDN	PWM7_PDN	**PWM7 power-down** 0: Keep original value 1: Power down PWM7
7	PWM6_PDN	PWM6_PDN	**PWM6 power-down** 0: Keep original value 1: Power down PWM6
6	PWM5_PDN	PWM5_PDN	**PWM5 power-down** 0: Keep original value 1: Power down PWM5
5	PWM4_PDN	PWM4_PDN	**PWM4 power-down** 0: Keep original value 1: Power down PWM4
4	PWM3_PDN	PWM3_PDN	**PWM3 power-down** 0: Keep original value 1: Power down PWM3
3	PWM2_PDN	PWM2_PDN	**PWM2 power-down** 0: Keep original value 1: Power down PWM2
2	PWM1_PDN	PWM1_PDN	**PWM1 power-down** 0: Keep original value 1: Power down PWM1
1	THERM_PDN	THERM_PDN	**THERM power-down** 0: Keep original value 1: Power down THERM
0	DISP_PWM_PDN	DISP_PWM_PDN	**DISP_PWM power-down** 0: Keep original value 1: Power down DISP_PWM

10002020 **PERI_GLOBALCON_PDN_MD1_SET** **Peripheral MD1 Power Down 0 Register Set** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRTX_PDN	SPI0_PDN	AUXADC_PDN	I2C3_PDN	I2C2_PDN	I2C1_PDN	I2C0_PDN	BTIF_PDN	UART4_PDN	UART3_PDN	UART2_PDN	UART1_PDN	UART0_PDN	MSDC30_3_PDN
Type			WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	MSDC30_2_PDN	MSDC30_1_PDN	MSDC30_0_PDN	AP_DMA_PDN	IRDA_PDN	USB0_PDN	PWM_PDN	PWM7_PDN	PWM6_PDN	PWM5_PDN	PWM4_PDN	PWM3_PDN	PWM2_PDN	PWM1_PDN	THERM_PDN	DISP_PWM_PDN

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Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29	**IRTX_PDN**	IRTX_PDN_SET	**IRTX power-down** 0: Keep original value 1: Power down IRTX
28	**SPI0_PDN**	SPI0_PDN	**SPI0 power-down** 0: Keep original value 1: Power down SPI0
27	**AUXADC_PDN**	AUXADC_PDN	**AUXADC power-down** 0: Keep original value 1: Power down AUXADC
26	**I2C3_PDN**	I2C3_PDN	**I2C3 power-down** 0: Keep original value 1: Power down I2C2
25	**I2C2_PDN**	I2C2_PDN	**I2C2 power-down** 0: Keep original value 1: Power down I2C2
24	**I2C1_PDN**	I2C1_PDN	**I2C1 power-down** 0: Keep original value 1: Power down I2C1
23	**I2C0_PDN**	I2C0_PDN	**I2C0 power-down** 0: Keep original value 1: Power down I2C0
22	**BTIF_PDN**	BTIF_PDN	**BTIF power-down** 0: Keep original value 1: Power down BTIF
21	**UART4_PDN**	UART4_PDN	**UART4 power-down** 0: Keep original value 1: Power down UART4
20	**UART3_PDN**	UART3_PDN	**UART3 power-down** 0: Keep original value 1: Power down UART3
19	**UART2_PDN**	UART2_PDN	**UART2 power-down** 0: Keep original value 1: Power down UART2
18	**UART1_PDN**	UART1_PDN	**UART1 power-down** 0: Keep original value 1: Power down UART1
17	**UART0_PDN**	UART0_PDN	**UART0 power-down** 0: Keep original value 1: Power down UART0
16	**MSDC30_3_PDN**	MSDC30_3_PDN	**MSDC30_3 power-down** 0: Keep original value 1: Power down MSDC30_3
15	**MSDC30_2_PDN**	MSDC30_2_PDN	**MSDC30_2 power-down** 0: Keep original value 1: Power down MSDC30_2
14	**MSDC30_1_PDN**	MSDC30_1_PDN	**MSDC30_1 power-down** 0: Keep original value 1: Power down MSDC30_1
13	**MSDC30_0_PDN**	MSDC30_0_PDN	**MSDC30_0 power-down** 0: Keep original value

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Bit(s)	Mnemonic	Name	Description
			1: Power down MSDC30_0
12	**AP_DMA_PDN**	AP_DMA_PDN	**AP_DMA power-down** 0: Keep original value 1: Power down AP_DMA
11	**IRDA_PDN**	IRDA_PDN	**IRDA power-down** 0: Keep original value 1: Power down IRDA
10	**USB0_PDN**	USB0_PDN	**USB0 power-down** 0: Keep original value 1: Power down USB0
9	**PWM_PDN**	PWM_PDN	**PWM power-down** 0: Keep original value 1: Power down PWM common logic
8	**PWM7_PDN**	PWM7_PDN	**PWM7 power-down** 0: Keep original value 1: Power down PWM7
7	**PWM6_PDN**	PWM6_PDN	**PWM6 power-down** 0: Keep original value 1: Power down PWM6
6	**PWM5_PDN**	PWM5_PDN	**PWM5 power-down** 0: Keep original value 1: Power down PWM5
5	**PWM4_PDN**	PWM4_PDN	**PWM4 power-down** 0: Keep original value 1: Power down PWM4
4	**PWM3_PDN**	PWM3_PDN	**PWM3 power-down** 0: Keep original value 1: Power down PWM3
3	**PWM2_PDN**	PWM2_PDN	**PWM2 power-down** 0: Keep original value 1: Power down PWM2
2	**PWM1_PDN**	PWM1_PDN	**PWM1 power-down** 0: Keep original value 1: Power down PWM1
1	**THERM_PDN**	THERM_PDN	**THERM power-down** 0: Keep original value 1: Power down THERM
0	**DISP_PWM_PDN**	DISP_PWM_PDN_SET	**DISP_PWM power-down** 0: Keep original value 1: Power down DISP_PWM

10002024 **PERI_GLOBALCON_PDN_MD2_SET** **Peripheral MD2 Power Down 0 Register Set** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRTX_PDN	SPI0_PDN	AUXADC_PDN	I2C3_PDN	I2C2_PDN	I2C1_PDN	I2C0_PDN	BTIF_PDN	UART4_PDN	UART3_PDN	UART2_PDN	UART1_PDN	UART0_PDN	MSDC30_3_PDN
Type			WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	MSDC30_2_PDN	MSDC30_1_PDN	MSDC30_0_PDN	AP_DMA_PDN	IRDA_PDN	USB0_PDN	PWM_PDN	PWM7_PDN	PWM6_PDN	PWM5_PDN	PWM4_PDN	PWM3_PDN	PWM2_PDN	PWM1_PDN	THERM_PDN	DISP_PWM_PDN
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29	**IRTX_PDN**	IRTX_PDN_SET	**IRTX power-down** 0: Keep original value 1: Power down IRTX
28	**SPI0_PDN**	SPI0_PDN	**SPI0 power-down** 0: Keep original value 1: Power down SPI0
27	**AUXADC_PDN**	AUXADC_PDN	**AUXADC power-down** 0: Keep original value 1: Power down AUXADC
26	**I2C3_PDN**	I2C3_PDN	**I2C3 power-down** 0: Keep original value 1: Power down I2C3
25	**I2C2_PDN**	I2C2_PDN	**I2C2 power-down** 0: Keep original value 1: Power down I2C2
24	**I2C1_PDN**	I2C1_PDN	**I2C1 power-down** 0: Keep original value 1: Power down I2C1
23	**I2C0_PDN**	I2C0_PDN	**I2C0 power-down** 0: Keep original value 1: Power down I2C0
22	**BTIF_PDN**	BTIF_PDN	**BTIF power-down** 0: Keep original value 1: Power down BTIF
21	**UART4_PDN**	UART4_PDN	**UART4 power-down** 0: Keep original value 1: Power down UART4
20	**UART3_PDN**	UART3_PDN	**UART3 power-down** 0: Keep original value 1: Power down UART3
19	**UART2_PDN**	UART2_PDN	**UART2 power-down** 0: Keep original value 1: Power down UART2
18	**UART1_PDN**	UART1_PDN	**UART1 power-down** 0: Keep original value 1: Power down UART1
17	**UART0_PDN**	UART0_PDN	**UART0 power-down** 0: Keep original value 1: Power down UART0
16	**MSDC30_3_PDN**	MSDC30_3_PDN	**MSDC30_3 power-down** 0: Keep original value 1: Power down MSDC30_3
15	**MSDC30_2_PDN**	MSDC30_2_PDN	**MSDC30_2 power-down** 0: Keep original value 1: Power down MSDC30_2
14	**MSDC30_1**	MSDC30_1_PDN	**MSDC30_1 power-down**

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Bit(s)	Mnemonic	Name	Description
	_PDN		0: Keep original value 1: Power down MSDC30_1
13	**MSDC30_0_PDN**	MSDC30_0_PDN	**MSDC30_0 power-down** 0: Keep original value 1: Power down MSDC30_0
12	**AP_DMA_PDN**	AP_DMA_PDN	**AP_DMA power-down** 0: Keep original value 1: Power down AP_DMA
11	**IRDA_PDN**	IRDA_PDN	**IRDA power-down** 0: Keep original value 1: Power down IRDA
10	**USB0_PDN**	USB0_PDN	**USB0 power-down** 0: Keep original value 1: Power down USB0
9	**PWM_PDN**	PWM_PDN	**PWM power-down** 0: Keep original value 1: Power down PWM common logic
8	**PWM7_PDN**	PWM7_PDN	**PWM7 power-down** 0: Keep original value 1: Power down PWM7
7	**PWM6_PDN**	PWM6_PDN	**PWM6 power-down** 0: Keep original value 1: Power down PWM6
6	**PWM5_PDN**	PWM5_PDN	**PWM5 power-down** 0: Keep original value 1: Power down PWM5
5	**PWM4_PDN**	PWM4_PDN	**PWM4 power-down** 0: Keep original value 1: Power down PWM4
4	**PWM3_PDN**	PWM3_PDN	**PWM3 power-down** 0: Keep original value 1: Power down PWM3
3	**PWM2_PDN**	PWM2_PDN	**PWM2 power-down** 0: Keep original value 1: Power down PWM2
2	**PWM1_PDN**	PWM1_PDN	**PWM1 power-down** 0: Keep original value 1: Power down PWM1
1	**THERM_PDN**	THERM_PDN	**THERM power-down** 0: Keep original value 1: Power down THERM
0	**DISP_PWM_PDN**	DISP_PWM_PDN_SET	**DISP_PWM power-down** 0: Keep original value 1: Power down DISP_PWM

10002028 **PERI_GLOBALCON_PDN_MD1_CLR** **Peripheral MD1 Power Down 0 Register Clear** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRTX_PDN	SPI0_PDN	AUXADC_P	I2C3_PDN	I2C2_PDN	I2C1_PDN	I2C0_PDN	BTIF_PDN	UART4_PD	UART3_PD	UART2_PD	UART1_PD	UART0_PD	MSDC30_

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					DN						N	N	N	N	N	3_PDN
Type			W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MSDC30_2_PDN**	**MSDC30_1_PDN**	**MSDC30_0_PDN**	**AP_DMA_PDN**	**IRDA_PDN**	**USB0_PDN**	**PWM_PDN**	**PWM7_PDN**	**PWM6_PDN**	**PWM5_PDN**	**PWM4_PDN**	**PWM3_PDN**	**PWM2_PDN**	**PWM1_PDN**	**THERM_PDN**	**DISP_PWM_PDN**
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29	**IRTX_PDN**	IRTX_PDN_SET	**IRTX clear power-down** 0: Keep original value 1: Clear power-down IRTX
28	**SPI0_PDN**	SPI0_PDN	**SPI0 clear power-down** 0: Keep original value 1: Clear power-down SPI0
27	**AUXADC_PDN**	AUXADC_PDN	**AUXADC clear power-down** 0: Keep original value 1: Clear power-down AUXADC
26	**I2C3_PDN**	I2C3_PDN	**I2C3 clear power-down** 0: Keep original value 1: Clear power-down I2C3
25	**I2C2_PDN**	I2C2_PDN	**I2C2 clear power-down** 0: Keep original value 1: Clear power-down I2C2
24	**I2C1_PDN**	I2C1_PDN	**I2C1 clear power-down** 0: Keep original value 1: Clear power-down I2C1
23	**I2C0_PDN**	I2C0_PDN	**I2C0 clear power-down** 0: Keep original value 1: Clear power-down I2C0
22	**BTIF_PDN**	BTIF_PDN	**BTIF clear power-down** 0: Keep original value 1: Clear power-down BTIF
21	**UART4_PDN**	UART4_PDN	**UART4 clear power-down** 0: Keep original value 1: Clear power-down UART4
20	**UART3_PDN**	UART3_PDN	**UART3 clear power-down** 0: Keep original value 1: Clear power-down UART3
19	**UART2_PDN**	UART2_PDN	**UART2 clear power-down** 0: Keep original value 1: Clear power-down UART2
18	**UART1_PDN**	UART1_PDN	**UART1 clear power-down** 0: Keep original value 1: Clear power-down UART1
17	**UART0_PDN**	UART0_PDN	**UART0 clear power-down** 0: Keep original value 1: Clear power-down UART0
16	**MSDC30_3_PDN**	MSDC30_3_PDN	**MSDC30_3 clear power-down** 0: Keep original value 1: Clear power-down MSDC30_3

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Bit(s)	Mnemonic	Name	Description
15	**MSDC30_2_PDN**	MSDC30_2_PDN	**MSDC30_2 clear power-down** 0: Keep original value 1: Clear power-down MSDC30_2
14	**MSDC30_1_PDN**	MSDC30_1_PDN	**MSDC30_1 clear power-down** 0: Keep original value 1: Clear power-down MSDC30_1
13	**MSDC30_0_PDN**	MSDC30_0_PDN	**MSDC30_0 clear power-down** 0: Keep original value 1: Clear power-down MSDC30_0
12	**AP_DMA_PDN**	AP_DMA_PDN	**AP_DMA clear power-down** 0: Keep original value 1: Clear power-down AP_DMA
11	**IRDA_PDN**	IRDA_PDN	**IRDA clear power-down** 0: Keep original value 1: Clear power-down IRDA
10	**USB0_PDN**	USB0_PDN	**USB0 clear power-down** 0: Keep original value 1: Clear power-down USB0
9	**PWM_PDN**	PWM_PDN	**PWM clear power-down** 0: Keep original value 1: Clear power-down PWM7
8	**PWM7_PDN**	PWM7_PDN	**PWM7 clear power-down** 0: Keep original value 1: Clear power-down PWM7
7	**PWM6_PDN**	PWM6_PDN	**PWM6 clear power-down** 0: Keep original value 1: Clear power-down PWM6
6	**PWM5_PDN**	PWM5_PDN	**PWM5 clear power-down** 0: Keep original value 1: Clear power-down PWM5
5	**PWM4_PDN**	PWM4_PDN	**PWM4 clear power-down** 0: Keep original value 1: Clear power-down PWM4
4	**PWM3_PDN**	PWM3_PDN	**PWM3 clear power-down** 0: Keep original value 1: Clear power-down PWM3
3	**PWM2_PDN**	PWM2_PDN	**PWM2 clear power-down** 0: Keep original value 1: Clear power-down PWM2
2	**PWM1_PDN**	PWM1_PDN	**PWM1 clear power-down** 0: Keep original value 1: Clear power-down PWM1
1	**THERM_PDN**	THERM_PDN	**THERM clear power-down** 0: Keep original value 1: Clear power-down THERM
0	**DISP_PWM_PDN**	DISP_PWM_PDN_SET	**DISP_PWM clear power-down** 0: Keep original value 1: Clear power-down DISP_PWM

1000202C	PERI_GLOBALCON_PDN_	Peripheral MD2 Power Down 0 Register	00000000

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MD2_CLR **Clear**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRTX_PDN	SPI0_PDN	AUXADC_PDN	I2C3_PDN	I2C2_PDN	I2C1_PDN	I2C0_PDN	BTIF_PDN	UART4_PDN	UART3_PDN	UART2_PDN	UART1_PDN	UART0_PDN	MSDC30_3_PDN
Type			W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC30_2_PDN	MSDC30_1_PDN	MSDC30_0_PDN	AP_DMA_PDN	IRDA_PDN	USB0_PDN	PWM_PDN	PWM7_PDN	PWM6_PDN	PWM5_PDN	PWM4_PDN	PWM3_PDN	PWM2_PDN	PWM1_PDN	THERM_PDN	DISP_PWM_PDN
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29	IRTX_PDN	IRTX_PDN_SET	**IRTX clear power-down** 0: Keep original value 1: Clear power-down IRTX
28	SPI0_PDN	SPI0_PDN	**SPI0 clear power-down** 0: Keep original value 1: Clear power-down SPI0
27	AUXADC_PDN	AUXADC_PDN	**AUXADC clear power-down** 0: Keep original value 1: Clear power-down AUXADC
26	I2C3_PDN	I2C3_PDN	**I2C3 clear power-down** 0: Keep original value 1: Clear power-down I2C3
25	I2C2_PDN	I2C2_PDN	**I2C2 clear power-down** 0: Keep original value 1: Clear power-down I2C2
24	I2C1_PDN	I2C1_PDN	**I2C1 clear power-down** 0: Keep original value 1: Clear power-down I2C1
23	I2C0_PDN	I2C0_PDN	**I2C0 clear power-down** 0: Keep original value 1: Clear power-down I2C0
22	BTIF_PDN	BTIF_PDN	**BTIF clear power-down** 0: Keep original value 1: Clear power-down BTIF
21	UART4_PDN	UART4_PDN	**UART4 clear power-down** 0: Keep original value 1: Clear power-down UART4
20	UART3_PDN	UART3_PDN	**UART3 clear power-down** 0: Keep original value 1: Clear power-down UART3
19	UART2_PDN	UART2_PDN	**UART2 clear power-down** 0: Keep original value 1: Clear power-down UART2
18	UART1_PDN	UART1_PDN	**UART1 clear power-down** 0: Keep original value 1: Clear power-down UART1
17	UART0_PDN	UART0_PDN	**UART0 clear power-down** 0: Keep original value 1: Clear power-down UART0

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Bit(s)	Mnemonic	Name	Description
16	**MSDC30_3_PDN**	MSDC30_3_PDN	**MSDC30_3 clear power-down** 0: Keep original value 1: Clear power-down MSDC30_3
15	**MSDC30_2_PDN**	MSDC30_2_PDN	**MSDC30_2 clear power-down** 0: Keep original value 1: Clear power-down MSDC30_2
14	**MSDC30_1_PDN**	MSDC30_1_PDN	**MSDC30_1 clear power-down** 0: Keep original value 1: Clear power-down MSDC30_1
13	**MSDC30_0_PDN**	MSDC30_0_PDN	**MSDC30_0 clear power-down** 0: Keep original value 1: Clear power-down MSDC30_0
12	**AP_DMA_PDN**	AP_DMA_PDN	**AP_DMA clear power-down** 0: Keep original value 1: Clear power-down AP_DMA
11	**IRDA_PDN**	IRDA_PDN	**IRDA clear power-down** 0: Keep original value 1: Clear power-down IRDA
10	**USB0_PDN**	USB0_PDN	**USB0 clear power-down** 0: Keep original value 1: Clear power-down USB0
9	**PWM_PDN**	PWM_PDN	**PWM clear power-down** 0: Keep original value 1: Clear power-down PWM7
8	**PWM7_PDN**	PWM7_PDN	**PWM7 clear power-down** 0: Keep original value 1: Clear power-down PWM7
7	**PWM6_PDN**	PWM6_PDN	**PWM6 clear power-down** 0: Keep original value 1: Clear power-down PWM6
6	**PWM5_PDN**	PWM5_PDN	**PWM5 clear power-down** 0: Keep original value 1: Clear power-down PWM5
5	**PWM4_PDN**	PWM4_PDN	**PWM4 clear power-down** 0: Keep original value 1: Clear power-down PWM4
4	**PWM3_PDN**	PWM3_PDN	**PWM3 clear power-down** 0: Keep original value 1: Clear power-down PWM3
3	**PWM2_PDN**	PWM2_PDN	**PWM2 clear power-down** 0: Keep original value 1: Clear power-down PWM2
2	**PWM1_PDN**	PWM1_PDN	**PWM1 clear power-down** 0: Keep original value 1: Clear power-down PWM1
1	**THERM_PDN**	THERM_PDN	**THERM clear power-down** 0: Keep original value 1: Clear power-down THERM
0	**DISP_PWM_PDN**	DISP_PWM_PDN_SET	**DISP_PWM clear power-down** 0: Keep original value 1: Clear power-down DISP_PWM

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10002030	PERI_GLOBALCON_PDN_MD1_STA	Peripheral MD1 Power Down 0 Register Status	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRTX_PDN	SPI0_PDN	AUXADC_PDN	I2C3_PDN	I2C2_PDN	I2C1_PDN	I2C0_PDN	BTIF_PDN	UART4_PDN	UART3_PDN	UART2_PDN	UART1_PDN	UART0_PDN	MSDC30_3_PDN
Type			RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC30_2_PDN	MSDC30_1_PDN	MSDC30_0_PDN	AP_DMA_PDN	IRDA_PDN	USB0_PDN	PWM_PDN	PWM7_PDN	PWM6_PDN	PWM5_PDN	PWM4_PDN	PWM3_PDN	PWM2_PDN	PWM1_PDN	THERM_PDN	DISP_PWM_PDN
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29	**IRTX_PDN**	IRTX_PDN_SET	**IRTX power-down** 0: Keep original value 1: Power down IRTX
28	**SPI0_PDN**	SPI0_PDN	**SPI0 power-down** 0: Keep original value 1: Power down SPI0
27	**AUXADC_PDN**	AUXADC_PDN	**AUXADC power-down** 0: Keep original value 1: Power down AUXADC
26	**I2C3_PDN**	I2C3_PDN	**I2C3 power-down** 0: Keep original value 1: Power down I2C3
25	**I2C2_PDN**	I2C2_PDN	**I2C2 power-down** 0: Keep original value 1: Power down I2C2
24	**I2C1_PDN**	I2C1_PDN	**I2C1 power-down** 0: Keep original value 1: Power down I2C1
23	**I2C0_PDN**	I2C0_PDN	**I2C0 power-down** 0: Keep original value 1: Power down I2C0
22	**BTIF_PDN**	BTIF_PDN	**BTIF power-down** 0: Keep original value 1: Power down BTIF
21	**UART4_PDN**	UART4_PDN	**UART4 power-down** 0: Keep original value 1: Power down UART4
20	**UART3_PDN**	UART3_PDN	**UART3 power-down** 0: Keep original value 1: Power down UART3
19	**UART2_PDN**	UART2_PDN	**UART2 power-down** 0: Keep original value 1: Power down UART2
18	**UART1_PDN**	UART1_PDN	**UART1 power-down** 0: Keep original value

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Bit(s)	Mnemonic	Name	Description
			1: Power down UART1
17	**UART0_PDN**	UART0_PDN	**UART0 power-down** 0: Keep original value 1: Power down UART0
16	**MSDC30_3_PDN**	MSDC30_3_PDN	**MSDC30_3 power-down** 0: Keep original value 1: Power down MSDC30_3
15	**MSDC30_2_PDN**	MSDC30_2_PDN	**MSDC30_2 power-down** 0: Keep original value 1: Power down MSDC30_2
14	**MSDC30_1_PDN**	MSDC30_1_PDN	**MSDC30_1 power-down** 0: Keep original value 1: Power down MSDC30_1
13	**MSDC30_0_PDN**	MSDC30_0_PDN	**MSDC30_0 power-down** 0: Keep original value 1: Power down MSDC30_0
12	**AP_DMA_PDN**	AP_DMA_PDN	**AP_DMA power-down** 0: Keep original value 1: Power down AP_DMA
11	**IRDA_PDN**	IRDA_PDN	**IRDA power-down** 0: Keep original value 1: Power down IRDA
10	**USB0_PDN**	USB0_PDN	**USB0 power-down** 0: Keep original value 1: Power down USB0
9	**PWM_PDN**	PWM_PDN	**PWM power-down** 0: Keep original value 1: Power down PWM7
8	**PWM7_PDN**	PWM7_PDN	**PWM7 power-down** 0: Keep original value 1: Power down PWM7
7	**PWM6_PDN**	PWM6_PDN	**PWM6 power-down** 0: Keep original value 1: Power down PWM6
6	**PWM5_PDN**	PWM5_PDN	**PWM5 power-down** 0: Keep original value 1: Power down PWM5
5	**PWM4_PDN**	PWM4_PDN	**PWM4 power-down** 0: Keep original value 1: Power down PWM4
4	**PWM3_PDN**	PWM3_PDN	**PWM3 power-down** 0: Keep original value 1: Power down PWM3
3	**PWM2_PDN**	PWM2_PDN	**PWM2 power-down** 0: Keep original value 1: Power down PWM2
2	**PWM1_PDN**	PWM1_PDN	**PWM1 power-down** 0: Keep original value 1: Power down PWM1
1	**THERM_PDN**	THERM_PDN	**THERM power-down** 0: Keep original value 1: Power down THERM

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Bit(s)	Mnemonic	Name	Description
0	**DISP_PWM_PDN**	DISP_PWM_PDN_SET	**DISP_PWM power-down** 0: Keep original value 1: Power down DISP_PWM

10002034 **PERI_GLOBALCON_PDN_MD2_STA** **Peripheral MD2 Power Down 0 Register Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRTX_PDN	SPI0_PDN	AUXADC_PDN	I2C3_PDN	I2C2_PDN	I2C1_PDN	I2C0_PDN	BTIF_PDN	UART4_PDN	UART3_PDN	UART2_PDN	UART1_PDN	UART0_PDN	MSDC30_3_PDN
Type			RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC30_2_PDN	MSDC30_1_PDN	MSDC30_0_PDN	AP_DMA_PDN	IRDA_PDN	USB0_PDN	PWM_PDN	PWM7_PDN	PWM6_PDN	PWM5_PDN	PWM4_PDN	PWM3_PDN	PWM2_PDN	PWM1_PDN	THERM_PDN	DISP_PWM_PDN
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29	**IRTX_PDN**	IRTX_PDN_SET	**IRTX power-down** 0: Keep original value 1: Power down IRTX
28	**SPI0_PDN**	SPI0_PDN	**SPI0 power-down** 0: Keep original value 1: Power down SPI0
27	**AUXADC_PDN**	AUXADC_PDN	**AUXADC power-down** 0: Keep original value 1: Power down AUXADC
26	**I2C3_PDN**	I2C3_PDN	**I2C3 power-down** 0: Keep original value 1: Power down I2C3
25	**I2C2_PDN**	I2C2_PDN	**I2C2 power-down** 0: Keep original value 1: Power down I2C2
24	**I2C1_PDN**	I2C1_PDN	**I2C1 power-down** 0: Keep original value 1: Power down I2C1
23	**I2C0_PDN**	I2C0_PDN	**I2C0 power-down** 0: Keep original value 1: Power down I2C0
22	**BTIF_PDN**	BTIF_PDN	**BTIF power-down** 0: Keep original value 1: Power down BTIF
21	**UART4_PDN**	UART4_PDN	**UART4 power-down** 0: Keep original value 1: Power down UART4
20	**UART3_PDN**	UART3_PDN	**UART3 power-down** 0: Keep original value 1: Power down UART3

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Bit(s)	Mnemonic	Name	Description
19	**UART2_PDN**	UART2_PDN	**UART2 power-down** 0: Keep original value 1: Power down UART2
18	**UART1_PDN**	UART1_PDN	**UART1 power-down** 0: Keep original value 1: Power down UART1
17	**UART0_PDN**	UART0_PDN	**UART0 power-down** 0: Keep original value 1: Power down UART0
16	**MSDC30_3_PDN**	MSDC30_3_PDN	**MSDC30_3 power-down** 0: Keep original value 1: Power down MSDC30_3
15	**MSDC30_2_PDN**	MSDC30_2_PDN	**MSDC30_2 power-down** 0: Keep original value 1: Power down MSDC30_2
14	**MSDC30_1_PDN**	MSDC30_1_PDN	**MSDC30_1 power-down** 0: Keep original value 1: Power down MSDC30_1
13	**MSDC30_0_PDN**	MSDC30_0_PDN	**MSDC30_0 power-down** 0: Keep original value 1: Power down MSDC30_0
12	**AP_DMA_PDN**	AP_DMA_PDN	**AP_DMA power-down** 0: Keep original value 1: Power down AP_DMA
11	**IRDA_PDN**	IRDA_PDN	**IRDA power-down** 0: Keep original value 1: Power down IRDA
10	**USB0_PDN**	USB0_PDN	**USB0 power-down** 0: Keep original value 1: Power down USB0
9	**PWM_PDN**	PWM_PDN	**PWM power-down** 0: Keep original value 1: Power down PWM7
8	**PWM7_PDN**	PWM7_PDN	**PWM7 power-down** 0: Keep original value 1: Power down PWM7
7	**PWM6_PDN**	PWM6_PDN	**PWM6 power-down** 0: Keep original value 1: Power down PWM6
6	**PWM5_PDN**	PWM5_PDN	**PWM5 power-down** 0: Keep original value 1: Power down PWM5
5	**PWM4_PDN**	PWM4_PDN	**PWM4 power-down** 0: Keep original value 1: Power down PWM4
4	**PWM3_PDN**	PWM3_PDN	**PWM3 power-down** 0: Keep original value 1: Power down PWM3
3	**PWM2_PDN**	PWM2_PDN	**PWM2 power-down** 0: Keep original value 1: Power down PWM2
2	**PWM1_PDN**	PWM1_PDN	**PWM1 power-down** 0: Keep original value

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Bit(s)	Mnemonic	Name	Description
			1: Power down PWM1
1	**THERM_PDN**	THERM_PDN	**THERM power-down** 0: Keep original value 1: Power down THERM
0	**DISP_PWM_PDN**	DISP_PWM_PDN_SET	**DISP_PWM power-down** 0: Keep original value 1: Power down DISP_PWM

10002038 **PERI_GLOBALCON_PDN_MD_MASK** **Peripheral MD Power Down Register MASK** **00000003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name															MD2_MASK	MD1_MASK
Type															RW	RW
Reset															1	1

Bit(s)	Mnemonic	Name	Description
1	**MD2_MASK**	MD2_MASK	**MD2 power-down mask** 0: MD2 power-down takes effect 1: MD2 power-down no effect
0	**MD1_MASK**	MD1_MASK	**MD1 power-down mask** 0: MD1 power-down takes effect 1: MD1 power-down no effect

10002050 **PERI_GLOBALCON_DCMCTL** **Peripheral DCM Control Register** **000000F0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				DCM_IDLE_BYPASS_EN					AHB_BUS_SLP_REQ						AXI_CLOCK_GATED_EN	DCM_ENABLE
Type				RW					RW						RW	RW
Reset				0	0	0	0	0	1	1	1	1			0	0

Bit(s)	Mnemonic	Name	Description
12:8	**DCM_IDLE_BYPASS_EN**	DCM_IDLE_BYPASS_EN	**Enables DCM idle bypass** bit 0: Enable ap_dma idle bypass when set to 1'b1 bit 1: Enable ap_hif idle bypass when set to 1'b1 bit 2: Enable md_hif idle bypass when set to 1'b1 bit 3: Enable usb idle bypass when set to 1'b1

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Bit(s)	Mnemonic	Name	Description
			bit 4: Enable msdc idle bypass when set to 1'b1
7:4	**AHB_BUS_SLP_REQ**	AHB_BUS_SLP_REQ	**AHB bus DCM control** bit 0: Enable AHB0_BUS sleep-request when set to 1'b1 bit 1: Enable AHB1_BUS sleep-request when set to 1'b1 bit 2: Enable AHB2_BUS sleep-request when set to 1'b1 bit 3: Enable AHB3_BUS sleep-request when set to 1'b1
1	**AXI_CLOCK_GATED_EN**	AXI_CLOCK_GATED_EN	**AXI clock gated** 0: Disable 1: Enable
0	**DCM_ENABLE**	DCM_ENABLE	**DCM control setting** 0: Disable 1: Enable

10002054 **PERI_GLOBALCON_DCMDBC** **Peripheral DCM Debounce Counter** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name									DCM_DBC_ENABLE	DCM_DBC_CNT						
Type									RW	RW						
Reset									1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
7	**DCM_DBC_ENABLE**	DCM_DBC_ENABLE	**DCM debouncing control** 0: Disable 1: Enable
6:0	**DCM_DBC_CNT**	DCM_DBC_CNT	**DCM debouncing counter**

10002058 **PERI_GLOBALCON_DCMFSEL** **Peripheral DCM Frequency Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												DCM_FULL_FSEL				
Type												RW				
Reset												0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					DCM_HALF_FSEL									DCM_QTR_FSEL		
Type					RW									RW		
Reset					0	0	0	0						0	0	0

Bit(s)	Mnemonic	Name	Description
20:16	**DCM_FULL_FSEL**	DCM_FULL_FSEL	**Selects DCM frequency for full-speed clock** FULL_FSEL[4]==1'b1: div1 FULL_FSEL[3]==1'b1: div2

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Bit(s)	Mnemonic	Name	Description
			FULL_FSEL[2]==1'b1: div4 FULL_FSEL[1]==1'b1: div8 FULL_FSEL[0]==1'b1: div16 All 0: div32
11:8	**DCM_HALF_FSEL**	DCM_HALF_FSEL	**Selects DCM frequency for half-speed clock** HALF_FSEL[3]==1'b1: div2 HALF_FSEL[2]==1'b1: div4 HALF_FSEL[1]==1'b1: div8 HALF_FSEL[0]==1'b1: div16 All: div32
2:0	**DCM_QTR_FSEL**	DCM_QTR_FSEL	**Selects DCM frequency for quarter-speed clock** QTR_FSEL[2]==1'b1: div4 QTR_FSEL[1]==1'b1: div8 QTR_FSEL[0]==1'b1: div16 All 0: div32

1000205C PERI_GLOBALCON_CKSEL Peripheral Clock Selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**PERIBUS_CK_SEL**
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**PERIBUS_CK_SEL**	PERIBUS_CK_SEL	**Peribus clock** Suggested to set to "half clock" mode when eMMC4.5 HS200 mode is enabled, which can enhance the periaxi/periahb data transfer bandwidth to improve eMMC4.5 HS200 mode data bandwidth. 0: Peribus operates at quarter clock 1: Peribus operates at half clock

100021F8 PERIAXI_BUS_CTL Peripheral AXI Bus Control 05FFF004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**PERI_X2H_BUFFER_EN**	**PERI_X2H_BURST_EN**	**PERI_X2H_ARMSK_B**	**PERI_X2H_HBURST**			**PERI_HDEC_WAY_EN[9:4]**					
Type					RW	RW	RW	RW			RW					
Reset					0	1	0	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**PERI_HDEC_WAY_EN[3:0]**				**PERI_X2S_THRES**		**peri_s2f_depth_val**					**peri_s2f_ar_fctrl_en**	**peri_s2f_aw_fctrl_en**	**peri_s2f_wthre**		
Type	RW				RW		RW					RW	RW	RW		

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Reset	1	1	1	1	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Mnemonic	Name	Description
27	PERI_X2H_BUFFER_EN	PERI_X2H_BUFFER_EN	**Enables AXI2AHB buffer attribute** 1: bvalid will be active as soon as all write data arrive at AXI2AHB bridge. 0: bvalid will be active only when all data are transferred to AHB.
26	PERI_X2H_BURST_EN	PERI_X2H_BURST_EN	**Enables AXI2AHB burst attribute** 0: The time when rvalid starts to toggle depends on arthre. 1: rvalid will start to toggle only when all AXI read data are received from AHB domain.
25	PERI_X2H_ARMSK_B	PERI_X2H_ARMSK_B	**In AXI2AHB bridge, if AXI read channel issues an INCR burst command with unaligned address, by default the bridge will use a mask circuit to make the address aligned. This will result in reading extra data from AHB slave.** If reading extra data from AHB slave will harm your application, you can set this bit to 1 to avoid this. armsk_b means the read mask circuit is low active. 1: Disable mask circuit; will not read extra data from AHB slave 0: Enable mask circuit; will result in reading extra data from AHB slave
24:22	PERI_X2H_HBURST	PERI_X2H_HBURST	**to decide the maximum burst type for AHB. Only effective when AXI issues the INCR burst type** 0: Only single transaction in AHB domain 3: Max. AHB burst will be INCR4. 5: Max. AHB burst will be INCR8. 7: Max. AHB burst will be INCR16. Otherwise: Will not take effect
21:12	PERI_HDEC_WAY_EN	PERI_HDEC_WAY_EN	**Enables slave way to bus mux**
11:10	PERI_X2S_THRES	PERI_X2S_THRES	**Configures how many data are latched before sending command on sbus.**
9:5	peri_s2f_depth_val	peri_s2f_depth_val	**Read flow control threshold setting; only valid when peri_s2f_ar_fctrl_en == 1**
4	peri_s2f_ar_fctrl_en	peri_s2f_ar_fctrl_en	**Selects read channel flow control method** 0: Threshold is pending read transaction number. 1: Threshold is pending read data number.
3	peri_s2f_aw_fctrl_en	peri_s2f_aw_fctrl_en	**Enables write channel flow control** 0: Disable write channel flow control 1: Enable write channel flow control
2:0	peri_s2f_wthre	peri_s2f_wthre	**Write flow control threshold setting** 0: Threshold is 1. 1: Threshold is 1/4 write data FIFO depth. 2: Threshold is 1/2 write data FIFO depth. 3: Threshold is 3/4 write data FIFO depth. 4: Threshold is write data FIFO depth. Otherwise: Threshold is write data FIFO depth.

100021FC **PERIAXI_BUS_CTL0** **Peripheral AXI Bus Control 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AHB0_ULTRA				AHB1_ULTRA				AHB0_PREULTRA				AHB1_PREULTRA			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AHB0_IOMMU				AHB1_IOMMU				AHB0_CACHE				AHB1_CACHE			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28	**AHB0_ULTRA**	AHB0_ULTRA	**Enables AHB bus0 ultra attribute** Bit 0: Enable NFI ultra attribute when set to 1'b1 Bit 1: Enable MSDC0 ultra attribute when set to 1'b1 Bit 2: Enable USB1 ultra attribute when set to 1'b1 Bit 3: Enable USB0 ultra attribute when set to 1'b1
27:24	**AHB1_ULTRA**	AHB1_ULTRA	**Enables AHB bus1 ultra attribute** Bit 0: Enable PWM ultra attribute when set to 1'b1 Bit 1: Enable MSDC1 ultra attribute when set to 1'b1 Bit 2: Enable MSDC2 ultra attribute when set to 1'b1 Bit 3: Enable SPI0 ultra attribute when set to 1'b1
23:20	**AHB0_PREULTRA**	AHB0_PREULTRA	**Enables AHB bus0 preultra attribute** Bit 0: Enable NFI preultra attribute when set to 1'b1 Bit 1: Enable MSDC0 preultra attribute when set to 1'b1 Bit 2: Enable USB1 preultra attribute when set to 1'b1 Bit 3: Enable USB0 preultra attribute when set to 1'b1
19:16	**AHB1_PREULTRA**	AHB1_PREULTRA	**Enables AHB bus1 preultra attribute** Bit 0: Enable PWM preultra attribute when set to 1'b1 Bit 1: Enable MSDC1 preultra attribute when set to 1'b1 Bit 2: Enable MSDC2 preultra attribute when set to 1'b1 Bit 3: Enable SPI0 preultra attribute when set to 1'b1
15:12	**AHB0_IOMMU**	AHB0_IOMMU	**Enables AHB bus0 iommu attribute** Bit 0: Enable NFI iommu attribute when set to 1'b1 Bit 1: Enable MSDC0 iommu attribute when set to 1'b1 Bit 2: Enable USB1 iommu attribute when set to 1'b1 Bit 3: Enable USB0 iommu attribute when set to 1'b1
11:8	**AHB1_IOMMU**	AHB1_IOMMU	**Enables AHB bus1 iommu attribute** Bit 0: Enable PWM iommu attribute when set to 1'b1 Bit 1: Enable MSDC1 iommu attribute when set to 1'b1 Bit 2: Enable MSDC2 iommu attribute when set to 1'b1 Bit 3: Enable SPI0 iommu attribute when set to 1'b1
7:4	**AHB0_CACHE**	AHB0_CACHE	**Enables AHB bus0 cache attribute** Bit 0: Enable NFI cache attribute when set to 1'b1 Bit 1: Enable MSDC0 cache attribute when set to 1'b1 Bit 2: Enable USB1 cache attribute when set to 1'b1 Bit 3: Enable USB0 cache attribute when set to 1'b1
3:0	**AHB1_CACHE**	AHB1_CACHE	**Enables AHB bus1 cache attribute** Bit 0: Enable PWM cache attribute when set to 1'b1 Bit 1: Enable MSDC1 cache attribute when set to 1'b1 Bit 2: Enable MSDC2 cache attribute when set to 1'b1 Bit 3: Enable SPI0 cache attribute when set to 1'b1

10002200 **PERIAXI_BUS_CTL1** **Peripheral AXI Bus Control 1** **00100000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AHB0_SHARE_EN				AHB1_SHARE_EN				AHB2_SHARE_EN				AHB2_ULTRA			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AHB2_PREULTRA				AHB2_IOMMU				AHB2_CACHE				H2X_0_RE	H2X_0_FIFO_THRESHOLD		

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													AD_AHEAD_BW			
Type	RW				RW				RW				RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28	**AHB0_SHARE_EN**	AHB0_SHARE_EN	**Enables AHB bus0 share attribute** Bit 0: Enable NFI share attribute when set to 1'b1 Bit 1: Enable MSDC0 share attribute when set to 1'b1 Bit 2: Enable USB1 share attribute when set to 1'b1 Bit 3: Enable USB0 share attribute when set to 1'b1
27:24	**AHB1_SHARE_EN**	AHB1_SHARE_EN	**Enables AHB bus1 share attribute** Bit 0: Enable PWM share attribute when set to 1'b1 Bit 1: Enable MSDC1 share attribute when set to 1'b1 Bit 2: Enable MSDC2 share attribute when set to 1'b1 Bit 3: Enable SPI0 share attribute when set to 1'b1
23:20	**AHB2_SHARE_EN**	AHB2_SHARE_EN	**Enables AHB bus2 share attribute** Bit 0: Enable MD share attribute when set to 1'b1 Bit 1: Enable SPM share attribute when set to 1'b1 Bit 2: Enable AUDIO share attribute when set to 1'b1 Bit 3: Enable THERM share attribute when set to 1'b1
19:16	**AHB2_ULTRA**	AHB2_ULTRA	**Enables AHB bus2 ultra attribute** Bit 0: Enable MD ultra attribute when set to 1'b1 Bit 1: Enable SPM ultra attribute when set to 1'b1 Bit 2: Enable AUDIO ultra attribute when set to 1'b1 Bit 3: Enable THERM ultra attribute when set to 1'b1
15:12	**AHB2_PREULTRA**	AHB2_PREULTRA	**Enables AHB bus2 preultra attribute** Bit 0: Enable MD preultra attribute when set to 1'b1 Bit 1: Enable SPM preultra attribute when set to 1'b1 Bit 2: Enable AUDIO preultra attribute when set to 1'b1 Bit 3: Enable THERM preultra attribute when set to 1'b1
11:8	**AHB2_IOMMU**	AHB2_IOMMU	**Enables AHB bus2 iommu attribute** Bit 0: Enable MD iommu attribute when set to 1'b1 Bit 1: Enable SPM iommu attribute when set to 1'b1 Bit 2: Enable AUDIO iommu attribute when set to 1'b1 Bit 3: Enable THERM iommu attribute when set to 1'b1
7:4	**AHB2_CACHE**	AHB2_CACHE	**Enables AHB bus2 cache attribute** Bit 0: Enable MD cache attribute when set to 1'b1 Bit 1: Enable SPM cache attribute when set to 1'b1 Bit 2: Enable AUDIO cache attribute when set to 1'b1 Bit 3: Enable THERM cache attribute when set to 1'b1
3	**H2X_0_READ_AHEAD_BW**	H2X_0_READ_AHEAD_BW	**Enables read ahead bufferable write option for ahb2axi_bridge_0** 0: Disable 1: Enable
2:0	**H2X_0_FIFO_THRESHOLD**	H2X_0_FIFO_THRESHOLD	**FIFO threshold control for ahb2axi_bridge_0** 000: Write command will be launched as soon as the first data are got from AHB bus. 001: Write command will be launched as soon as 1/4 of current burst len is got from AHB bus. 010: Write command will be launched as soon as 1/2 of current burst len is got from AHB bus. 011: Write command will be launched as soon as 3/4 of current burst len is got from AHB bus. 100: Write command will be launched as soon as all of current burst len is got from AHB bus.

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Bit(s)	Mnemonic	Name	Description
			Others: Same as 100

10002204 PERIAXI_BUS_CTL2 Peripheral AXI Bus Control 2 001FC07F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	H2X_1_READ_AHEAD_BW	H2X_1_FIFO_THRESHOLD			H2X_2_READ_AHEAD_BW	H2X_2_FIFO_THRESHOLD						AHB_SECURE_EN[6:2]				
Type	RW	RW			RW	RW						RW				
Reset	0	0	0	0	0	0	0	0				1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AHB_SECURE_EN[1:0]		AHB_BUFFER_EN							AHB_MERGE_EN						
Type	RW		RW							RW						
Reset	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**H2X_1_READ_AHEAD_BW**	H2X_1_READ_AHEAD_BW	**Enables read ahead bufferable write option for ahb2axi_bridge_1** 0: Disable 1: Enable
30:28	**H2X_1_FIFO_THRESHOLD**	H2X_1_FIFO_THRESHOLD	**FIFO threshold control for ahb2axi_bridge_1** 000: Write command will be launched as soon as the first data are got from AHB bus. 001: Write command will be launched as soon as 1/4 of current burst len is got from AHB bus. 010: Write command will be launched as soon as 1/2 of current burst len is got from AHB bus. 011: Write command will be launched as soon as 3/4 of current burst len is got from AHB bus. 100: Write command will be launched as soon as all of current burst len is got from AHB bus. Others: Same as 100
27	**H2X_2_READ_AHEAD_BW**	H2X_2_READ_AHEAD_BW	**Enables read ahead bufferable write option for ahb2axi_bridge_2** 0: Disable 1: Enable
26:24	**H2X_2_FIFO_THRESHOLD**	H2X_2_FIFO_THRESHOLD	**FIFO threshold control for ahb2axi_bridge_2** 000: Write command will be launched as soon as the first data are got from AHB bus. 001: Write command will be launched as soon as 1/4 of current burst len is got from AHB bus. 010: Write command will be launched as soon as 1/2 of current burst len is got from AHB bus. 011: Write command will be launched as soon as 3/4 of current burst len is got from AHB bus. 100: Write command will be launched as soon as all of current burst len is got from AHB bus. Others: Same as 100
20:14	**AHB_SECURE_EN**	AHB_SECURE_EN	**Enables AHB2AXI secure attribute** bit 0: peri_ahb2axi_bridg0 (USB2/MSDC3) bit 1: peri_ahb2axi_bridg1 (PWM/MSDC1/MSDC2/SPI) bit 2: peri_ahb2axi_bridg1 (MD/Audio/ptp_thermal/infra_ao)

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Bit(s)	Mnemonic	Name	Description
13:7	**AHB_BUFFER_EN**	AHB_BUFFER_EN	**Enables AHB2AXI buffer attribute**
6:0	**AHB_MERGE_EN**	AHB_MERGE_EN	**Enables AHB2AXI merge attribute**

10002208 **PERIAXI_SIo_CTL** **Peripheral AXI SIo Control** **00000300**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**PERIAXI_CG_DISABLE**							**PERIAXI_SIo_WR_OT_BUSY**	**PERIAXI_SIo_RD_OT_BUSY**	**PERIAXI_SIo_DFSLV_SET_RID_MISS**	**PERIAXI_SIo_DFSLV_SET_BID_MISS**	**PERIAXI_SIo_DFSLV_SET_WIRQ**	**PERIAXI_SIo_DFSLV_SET_RIRQ**	**PERIAXI_SIo_R_CHNL_SEL**		
Type	RW							RO	RO	RO	RO	RO	RO	RO		
Reset	0							0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**PERIAXI_SIo_B_CHNL_SEL**			**PERIAXI_SIo_CTRL_BYPASS**			**PERIAXI_SIo_WAY_EN**									**PERIAXI_SIo_OUSTANDING_DISABLE**
Type	RO			RW			RW									RW
Reset	0	0	0	0			1	1								0

Bit(s)	Mnemonic	Name	Description
31	**PERIAXI_CG_DISABLE**	PERIAXI_CG_DISABLE	**PERIAXI CG disable control** 0: Enable CG 1: Disable CG
24	**PERIAXI_SIo_WR_OT_BUSY**	PERIAXI_SIo_WR_OT_BUSY	**PERIAXI control bypass** 0: Disable 1: Enable
23	**PERIAXI_SIo_RD_OT_BUSY**	PERIAXI_SIo_RD_OT_BUSY	**PERIAXI control bypass** 0: Disable 1: Enable
22	**PERIAXI_SIo_DFSLV_SET_RID_MISS**	PERIAXI_SIo_DFSLV_SET_RID_MISS	**PERIAXI control bypass** 0: Disable 1: Enable
21	**PERIAXI_SIo_DFSLV_SET_BID_MISS**	PERIAXI_SIo_DFSLV_SET_BID_MISS	**PERIAXI control bypass** 0: Disable 1: Enable
20	**PERIAXI_SIo_DFSLV_SET_WIRQ**	PERIAXI_SIo_DFSLV_SET_WIRQ	**PERIAXI control bypass** 0: Disable 1: Enable
19	**PERIAXI_SIo_DFSLV_SET_RIRQ**	PERIAXI_SIo_DFSLV_SET_RIRQ	**PERIAXI control bypass** 0: Disable 1: Enable

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Bit(s)	Mnemonic	Name	Description
18:16	**PERIAXI_SI0_R_CHNL_SEL**	PERIAXI_SI0_R_CHNL_SEL	**PERIAXI control bypass** 0: Disable 1: Enable
15:13	**PERIAXI_SI0_B_CHNL_SEL**	PERIAXI_SI0_B_CHNL_SEL	**PERIAXI control bypass** 0: Disable 1: Enable
12	**PERIAXI_SI0_CTRL_BYPASS**	PERIAXI_SI0_CTRL_BYPASS	**PERIAXI control bypass** 0: Disable 1: Enable
9:8	**PERIAXI_SI0_WAY_EN**	PERIAXI_SI0_WAY_EN	**Enables PERIAXI SI0 way**
0	**PERIAXI_SI0_OUSTANDING_DISABLE**	PERIAXI_SI0_OUSTANDING_DISABLE	**Disables PERIAXI SI0 outstanding**

1000220C **PERIAXI_SI1_CTL** **Peripheral AXI SI1 Control** **00000300**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								PERIAXI_SI1_WR_OT_BUSY	PERIAXI_SI1_RD_OT_BUSY	PERIAXI_SI1_DFSLV_SET_RID_MISS	PERIAXI_SI1_DFSLV_SET_BID_MISS	PERIAXI_SI1_DFSLV_SET_WIRQ	PERIAXI_SI1_DFSLV_SET_RIRQ	PERIAXI_SI1_R_CHNL_SEL		
Type								RO	RO	RO	RO	RO	RO	RO		
Reset								0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERIAXI_SI1_B_CHNL_SEL			PERIAXI_SI1_CTRL_BYPASS			PERIAXI_SI1_WAY_EN									PERIAXI_SI1_OUSTANDING_DISABLE
Type	RO			RW			RW									RW
Reset	0	0	0	0			1	1								0

Bit(s)	Mnemonic	Name	Description
24	**PERIAXI_SI1_WR_OT_BUSY**	PERIAXI_SI1_WR_OT_BUSY	**PERIAXI control bypass** 0: Disable 1: Enable
23	**PERIAXI_SI1_RD_OT_BUSY**	PERIAXI_SI1_RD_OT_BUSY	**PERIAXI control bypass** 0: Disable 1: Enable
22	**PERIAXI_SI1_DFSLV_SET_RID_MISS**	PERIAXI_SI1_DFSLV_SET_RID_MISS	**PERIAXI control bypass** 0: Disable 1: Enable
21	**PERIAXI_SI1_DFSLV_SET_BID**	PERIAXI_SI1_DFSLV_SET_BID_MISS	**PERIAXI control bypass** 0: Disable

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Bit(s)	Mnemonic	Name	Description
	_MISS		1: Enable
20	**PERIAXI_SI1_DFSLV_SET_WIRQ**	PERIAXI_SI1_DFSLV_SET_WIRQ	**PERIAXI control bypass** 0: Disable 1: Enable
19	**PERIAXI_SI1_DFSLV_SET_RIRQ**	PERIAXI_SI1_DFSLV_SET_RIRQ	**PERIAXI control bypass** 0: Disable 1: Enable
18:16	**PERIAXI_SI1_R_CHNL_SEL**	PERIAXI_SI1_R_CHNL_SEL	**PERIAXI control bypass** 0: Disable 1: Enable
15:13	**PERIAXI_SI1_B_CHNL_SEL**	PERIAXI_SI1_B_CHNL_SEL	**PERIAXI control bypass** 0: Disable 1: Enable
12	**PERIAXI_SI1_CTRL_BYPASS**	PERIAXI_SI1_CTRL_BYPASS	**PERIAXI control bypass** 0: Disable 1: Enable
9:8	**PERIAXI_SI1_WAY_EN**	PERIAXI_SI1_WAY_EN	**Enables PERIAXI SI1 way**
0	**PERIAXI_SI1_OUSTANDING_DISABLE**	PERIAXI_SI1_OUSTANDING_DISABLE	**Disables PERIAXI SI1 outstanding**

10002210 **PERIAXI_MI_STA** **Peripheral AXI MI Status** **00000040**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MI1_W_BUSY	MI1_R_BUSY	MI1_ERRMID_SETBIRQ	MI1_ERRMID_SETRIRQ	MI0_W_BUSY	MI0_R_BUSY	MI0_ERRMID_SETBIRQ	MI0_ERRMID_SETRIRQ
Type									RO	RO	RO	RO	RO	RO	RO	RO
Reset									0	1	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7	**MI1_W_BUSY**	MI1_W_BUSY	**PERIAXI MI1 write busy** 0: MI1 not write busy 1: MI1 write busy
6	**MI1_R_BUSY**	MI1_R_BUSY	**PERIAXI MI1 read busy** 0: MI1 not read busy 1: MI1 read busy
5	**MI1_ERRMID_SET_BIRQ**	MI1_ERRMID_SET_BIRQ	**PERIAXI MI1 write error** 0: MI1 no write error MID 1: MI1 write error MID
4	**MI1_ERRMID_SET_RI**	MI1_ERRMID_SET_RIRQ	**PERIAXI MI1 read error** 0: MI1 no read error MID

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Bit(s)	Mnemonic	Name	Description
	RQ		1: MI1 read error MID
3	**MI0_W_BUSY**	MI0_W_BUSY	**PERIAXI MI0 write busy** 0: MI0 not write busy 1: MI0 write busy
2	**MI0_R_BUSY**	MI0_R_BUSY	**PERIAXI MI0 read busy** 0: MI0 not read busy 1: MI0 read busy
1	**MI0_ERRMID_SET_BIRQ**	MI0_ERRMID_SET_BIRQ	**PERIAXI MI0 write error** 0: MI0 no write error MID 1: MI0 write error MID
0	**MI0_ERRMID_SET_RIRQ**	MI0_ERRMID_SET_RIRQ	**PERIAXI MI0 read error** 0: MI0 no read error MID 1: MI0 read error MID

10002300 **PERIAXI_AHB_LMT_CON1** **Peripheral AHB Bus 0 Bandwidth Limiter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						MSDC0_EMI_ULTRA	PERI2CONN_BUFFER_MODE	PERI2CONN_BUFFER_EN	SOFT_LIMIT_EN				FILTER_CKEN	FILTER_LEN		FILTER_EN
Type						RW	RW	RW	RW				RW	RW		RW
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
10	**MSDC0_EMI_ULTRA**	MSDC0_EMI_ULTRA	**MSDC0 AHB master reads/writes CMD/data ultra attribute to EMI** Suggested to be enabled when the eMMC4.5 HS200 mode is enabled. After being enabled, every MSDC0 command will become ultra priority in the view of EMI arbitration. 0: Disable MSDC0 AHB master read/write CMD/data with ultra attribute to EMI. 1: Enable MSDC0 AHB master read/write CMD/data with ultra attribute to EMI.
9	**PERI2CONN_BUFFER_MODE**	PERI2CONN_BUFFER_MODE	**The condition of early response of per2conn_ahb_bridge_f2s depends on hprot[2] signal of AHB.** 0: Always 1: Conditional
8	**PERI2CONN_BUFFER_EN**	PERI2CONN_BUFFER_EN	**Enables early response ability of per2conn_ahb_bridge_f2s** 0: Disable 1: Enable early response
7:4	**SOFT_LIMIT_EN**	SOFT_LIMIT_EN	**Enables AHB bus 0 bandwidth soft-limiter**
3	**FILTER_CKEN**	FILTER_CKEN	**Enables AHB bus 0 bandwidth limiter filter clock**
2:1	**FILTER_L**	FILTER_LEN	**AHB bus 0 bandwidth limiter filter length**

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Bit(s)	Mnemonic	Name	Description
	EN		00: Filter length = 256 01: Filter length = 512 10: Filter length = 1024 11: Filter length = 2048
0	**FILTER_EN**	FILTER_EN	**Enables AHB bus 0 bandwidth limiter filter**

10002304 PERIAXI_AHB_LMT_CON2 Peripheral AHB Bus 0 Bandwidth Limiter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	USB0P_BUS_GNT_CNT								MSDC3_BUS_GNT_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC0_BUS_GNT_CNT								PERIAXI_MI1_FP_EN	PERIAHB_BUS2_FP_EN	APXGPT5_SWCG_EN	APXGPT4_SWCG_EN	APXGPT3_SWCG_EN	APXGPT2_SWCG_EN	APXGPT1_SWCG_EN	APXGPT0_SWCG_EN
Type	RW								RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**USB0P_BUS_GNT_CNT**	USB0P_BUS_GNT_CNT	**USB 0P bus grant count**
23:16	**MSDC3_BUS_GNT_CNT**	MSDC3_BUS_GNT_CNT	**Audio bus grant count**
15:8	**MSDC0_BUS_GNT_CNT**	MSDC0_BUS_GNT_CNT	**MSDC0 bus grant count**
7	**PERIAXI_MI1_FP_EN**	PERIAXI_MI1_FP_EN	**Enables fix priority option in MI1 to favor MD** 0: Disable 1: Enable
6	**PERIAHB_BUS2_FP_EN**	PERIAHB_BUS2_FP_EN	**Enables fix priority option in AHB_BUS2 to favor MD** 0: Disable 1: Enable
5	**APXGPT5_SWCG_EN**	APXGPT5_SWCG_EN	**Stops APXGPT5 clock** 0: Disable 1: Enable
4	**APXGPT4_SWCG_EN**	APXGPT4_SWCG_EN	**Stops APXGPT4 clock** 0: Disable 1: Enable
3	**APXGPT3_SWCG_EN**	APXGPT3_SWCG_EN	**Stops APXGPT3 clock** 0: Disable 1: Enable
2	**APXGPT2_SWCG_EN**	APXGPT2_SWCG_EN	**Stops APXGPT2 clock** 0: Disable 1: Enable
1	**APXGPT1_SWCG_EN**	APXGPT1_SWCG_EN	**Stops APXGPT1 clock** 0: Disable 1: Enable

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Bit(s)	Mnemonic	Name	Description
0	**APXGPT0_SWCG_EN**	APXGPT0_SWCG_EN	**Stops APXGPT0 clock** 0: Disable 1: Enable

10002308 PERIAXI_AHB_LMT_CON3 Peripheral AHB Bus 1 Bandwidth Limiter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SOFT_LIMIT_EN				FILTER_CKEN	FILTER_LEN		FILTER_EN
Type									RW				RW	RW		RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:4	**SOFT_LIMIT_EN**	SOFT_LIMIT_EN	**Enables AHB bus 1 bandwidth soft-limiter**
3	**FILTER_CKEN**	FILTER_CKEN	**Enables AHB bus 1 bandwidth limiter filter clock**
2:1	**FILTER_LEN**	FILTER_LEN	**AHB bus 1 bandwidth limiter filter length** 00: Fliter length = 256 01: Filter length = 512 10: Filter length = 1024 11: Filter length = 2048
0	**FILTER_EN**	FILTER_EN	**Enables AHB bus 1 bandwidth limiter filter**

1000230C PERIAXI_AHB_LMT_CON4 Peripheral AHB Bus 1 Bandwidth Limiter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI0_BUS_GNT_CNT								MSDC2_BUS_GNT_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC1_BUS_GNT_CNT								PWM_BUS_GNT_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**SPI0_BUS_GNT_CNT**	SPI0_BUS_GNT_CNT	SPI0 bus grant count
23:16	**MSDC2_BUS_GNT_CNT**	MSDC2_BUS_GNT_CNT	MSDC2 bus grant count
15:8	**MSDC1_BUS_GNT_CNT**	MSDC1_BUS_GNT_CNT	MSDC1 bus grant count
7:0	**PWM_BUS**	PWM_BUS_GNT_	PWM bus grant count

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Bit(s)	Mnemonic	Name	Description
	_GNT_CNT	CNT	

10002310 **PERIAXI_AHB_LMT_CON5** **Peripheral AHB Bus 2 Bandwidth Limiter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SOFT_LIMIT_EN				FILTER_CKEN	FILTER_LEN		FILTER_EN
Type									RW				RW	RW		RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:4	**SOFT_LIMIT_EN**	SOFT_LIMIT_EN	**Enables AHB bus 2 bandwidth soft-limiter**
3	**FILTER_CKEN**	FILTER_CKEN	**Enables AHB bus 2 bandwidth limiter filter clock**
2:1	**FILTER_LEN**	FILTER_LEN	**AHB bus 2 bandwidth limiter filter length** 00: Filter length = 256 01: Filter length = 512 10: Filter length = 1024 11: Filter length = 2048
0	**FILTER_EN**	FILTER_EN	**Enables AHB bus 2 bandwidth limiter filter**

10002314 **PERIAXI_AHB_LMT_CON6** **Peripheral AHB Bus 2 Bandwidth Limiter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PTP_BUS_GNT_CNT								AUD_BUS_GNT_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPM_BUS_GNT_CNT								MDSYS_BUS_GNT_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**PTP_BUS_GNT_CNT**	PTP_BUS_GNT_CNT	PTP bus grant count
23:16	**AUD_BUS_GNT_CNT**	AUD_BUS_GNT_CNT	DEBUGTOP bus grant count
15:8	**SPM_BUS_GNT_CNT**	SPM_BUS_GNT_CNT	FHCTL_SPM bus grant count
7:0	**MDSYS_BUS_GNT_CNT**	MDSYS_BUS_GNT_CNT	MDSYS bus grant count

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10002320 PERIAXI_AXI_LMT_CON1 Peripheral AXI MST0 Bandwidth Limiter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																SOFT_LIMIT_EN
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					FILTER_CKEN	BW_FILTER_EN	FILTER_LEN		AXI_MST0_BUS_GNT_CNT							
Type					RW	RW	RW		RW							
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	SOFT_LIMIT_EN	SOFT_LIMIT_EN	**Enables AXI MST0 soft bandwidth limiter** 0: Disable 1: Enable
11	FILTER_CKEN	FILTER_CKEN	**Enables AHB bus 0 bandwidth limiter filter clock** 0: Disable 1: Enable
10	BW_FILTER_EN	BW_FILTER_EN	**Enables AXI MST0 soft bandwidth soft-limiter** 0: Disable 1: Enable
9:8	FILTER_LEN	FILTER_LEN	**Enables AXI MST0 bandwidth limiter filter clock** 00: Filter length = 256 01: Filter length = 512 10: Filter length = 1024 11: Filter length = 2048
7:0	AXI_MST0_BUS_GNT_CNT	AXI_MST0_BUS_GNT_CNT	**Enables AXI MST0 bandwidth limiter**

10002324 PERIAXI_AXI_LMT_CON2 Peripheral AXI MST1 Bandwidth Limiter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																SOFT_LIMIT_EN
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					FILTER_CKEN	BW_FILTER_EN	FILTER_LEN		AXI_MST1_BUS_GNT_CNT							
Type					RW	RW	RW		RW							
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
16	SOFT_LIMIT_EN	SOFT_LIMIT_EN	**Enables AXI MST1 soft bandwidth soft-limiter** 0: Disable 1: Enable
11	FILTER_CKEN	FILTER_CKEN	**Enables AXI MST1 bandwidth limiter filter clock** 0: Disable 1: Enable
10	BW_FILTER_EN	BW_FILTER_EN	**Enables AXI MST1 bandwidth limiter** 0: Disable 1: Enable
9:8	FILTER_LEN	FILTER_LEN	**AXI MST1 bandwidth limiter filter length** 00: Filter length = 256 01: Filter length = 512 10: Filter length = 1024 11: Filter length = 2048
7:0	AXI_MST1_BUS_GNT_CNT	AXI_MST1_BUS_GNT_CNT	**AXI MST1 bus grant count**

10002328 **PERIAXI_AXI_LMT_CON3** **Peripheral AXI MST2 Bandwidth Limiter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																SOFT_LIMIT_EN
Type																RW
Reset																0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					FILTER_CKEN	BW_FILTER_EN	FILTER_LEN		AXI_MST2_BUS_GNT_CNT							
Type					RW	RW	RW		RW							
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	SOFT_LIMIT_EN	SOFT_LIMIT_EN	**Enables AXI MST2 soft bandwidth soft-limiter** 0: Disable 1: Enable
11	FILTER_CKEN	FILTER_CKEN	**Enables AXI MST2 bandwidth limiter filter clock** 0: Disable 1: Enable
10	BW_FILTER_EN	BW_FILTER_EN	**Enables AXI MST2 bandwidth limiter** 0: Disable 1: Enable
9:8	FILTER_LEN	FILTER_LEN	**AXI MST2 bandwidth limiter filter length** 00: Filter length = 256 01: Filter length = 512 10: Filter length = 1024 11: Filter length = 2048
7:0	AXI_MST2_BUS_GNT_CNT	AXI_MST2_BUS_GNT_CNT	**AXI MST2 bus grant count**

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1000232C **PERIAXI_AXI_LMT_CON4** **Peripheral AP DMA Bandwidth Limiter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																SOFT_LIMIT_EN
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					FILTER_CKEN	BW_FILTER_EN	FILTER_LEN		AXI_DMA_BUS_GNT_CNT							
Type					RW	RW	RW		RW							
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	SOFT_LIMIT_EN	SOFT_LIMIT_EN	**Enables AP DMA AXI soft bandwidth soft-limiter** 0: Disable 1: Enable
11	FILTER_CKEN	FILTER_CKEN	**Enables AP DMA AXI master bandwidth limiter filter clock** 0: Disable 1: Enable
10	BW_FILTER_EN	BW_FILTER_EN	**Enables AP DMA bandwidth limiter** 0: Disable 1: Enable
9:8	FILTER_LEN	FILTER_LEN	**AP DMA bandwidth limiter filter length** 00: Filter length = 256 01: Filter length = 512 10: Filter length = 1024 11: Filter length = 2048
7:0	AXI_DMA_BUS_GNT_CNT	AXI_DMA_BUS_GNT_CNT	**AP DMA bus grant count**

10002400 **PERI_USB_WAKEUP_DEC_CON0** **Peripheral USB Wakeup Control0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												USB0_CDDEBOUNCE				USB0_CDEN
Type												RW				RW
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:1	USB0_CDDEBOUNCE	USB0_CDDEBOUNCE	**USB0 debounce clock number (0~15)** 0000: 0 0001: 1

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Bit(s)	Mnemonic	Name	Description
			0010: 2 1111: 15
0	USB0_CDEN	USB0_CDEN	**Enables USB0 clock debounce** 0: Disable 1: Enable

1000240C **PERI_UART_CK_SOURCE_SEL** **Peripheral UART Clock Source Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												UART_CK_SEL				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0	UART_CK_SEL	UART_CK_SEL	**Selects clock source for UART0 through UART4** 0: 26MHz clock 1: 52MHz clock

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5.2 GPIO Control

5.2.1 General Descriptions

There are 198 I/O pins which can be programmed as multiple purpose, including GPIO, NAND, SPI, etc. By setting up the GPIO_MODE register, specific IO is selected for specific function.

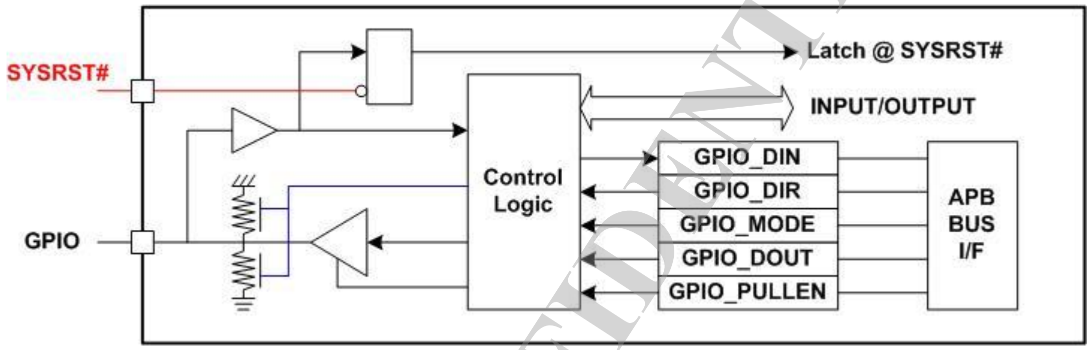

Figure 5-2. GPIO block diagram

All functions should comply with the priority rule. When there are more than one IO set as the same output function, all of the selected IOs are able to output specific signals. When there are more than one IO are set as the same input (or bi-directional) function, only the IO with the largest GPIO index works functionally.

When the MIPI function is not used, related IOs can be switched to non-MIPI input-only function, like EINT. To enable the GPI function of MIPI, there are some configurations to be done before the related GPIO_MODE is set.

5.2.2 Register Definition

Module name: GPIO Base address: (+10211000h)

Address	Name	Width	Register Function
10211000	GPIO_DIR1	32	GPIO Direction Control Register 1
10211010	GPIO_DIR2	32	GPIO Direction Control Register 2
10211020	GPIO_DIR3	32	GPIO Direction Control Register 3
10211030	GPIO_DIR4	32	GPIO Direction Control Register 4
10211040	GPIO_DIR5	32	GPIO Direction Control Register 5
10211050	GPIO_DIR6	32	GPIO Direction Control Register 6
10211060	GPIO_DIR7	32	GPIO Direction Control Register 7
10211100	GPIO_DOUT1	32	GPIO Data Output Register 1
10211110	GPIO_DOUT2	32	GPIO Data Output Register 2
10211120	GPIO_DOUT3	32	GPIO Data Output Register 3
10211130	GPIO_DOUT4	32	GPIO Data Output Register 4
10211140	GPIO_DOUT5	32	GPIO Data Output Register 5
10211150	GPIO_DOUT6	32	GPIO Data Output Register 6

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Address	Name	Width	Register Function
10211160	GPIO_DOUT7	32	GPIO Data Output Register 7
10211200	GPIO_DIN1	32	GPIO Data Input Register 1
10211210	GPIO_DIN2	32	GPIO Data Input Register 2
10211220	GPIO_DIN3	32	GPIO Data Input Register 3
10211230	GPIO_DIN4	32	GPIO Data Input Register 4
10211240	GPIO_DIN5	32	GPIO Data Input Register 5
10211250	GPIO_DIN6	32	GPIO Data Input Register 6
10211260	GPIO_DIN7	32	GPIO Data Input Register 7
10211300	GPIO_MODE1	32	GPIO Mode Control Register 1
10211310	GPIO_MODE2	32	GPIO Mode Control Register 2
10211320	GPIO_MODE3	32	GPIO Mode Control Register 3
10211330	GPIO_MODE4	32	GPIO Mode Control Register 4
10211340	GPIO_MODE5	32	GPIO Mode Control Register 5
10211350	GPIO_MODE6	32	GPIO Mode Control Register 6
10211360	GPIO_MODE7	32	GPIO Mode Control Register 7
10211370	GPIO_MODE8	32	GPIO Mode Control Register 8
10211380	GPIO_MODE9	32	GPIO Mode Control Register 9
10211390	GPIO_MODE10	32	GPIO Mode Control Register 10
102113A0	GPIO_MODE11	32	GPIO Mode Control Register 11
102113B0	GPIO_MODE12	32	GPIO Mode Control Register 12
102113C0	GPIO_MODE13	32	GPIO Mode Control Register 13
102113D0	GPIO_MODE14	32	GPIO Mode Control Register 14
102113E0	GPIO_MODE15	32	GPIO Mode Control Register 15
102113F0	GPIO_MODE16	32	GPIO Mode Control Register 16
10211400	GPIO_MODE17	32	GPIO Mode Control Register 17
10211410	GPIO_MODE18	32	GPIO Mode Control Register 18
10211420	GPIO_MODE19	32	GPIO Mode Control Register 19
10211430	GPIO_MODE20	32	GPIO Mode Control Register 20
10211440	GPIO_MODE21	32	GPIO Mode Control Register 21
102116D0	GPIO_DEBUG	32	GPIO Debug mode register
102116E0	GPIO_BACKUP	32	GPIO Reserved Control Register
102116F0	GPIO_TEST_MODE	32	GPIO Test Mode Register
10211800	GPIO_IES_G0	8	GPIO Group 0 IES Control Register
10211810	GPIO_SMT_G0	8	GPIO Group 0 SMT Control Register
10211820	GPIO_TDSEL0_G0	32	GPIO Group 0 TDSEL Control Register 0
10211828	GPIO_RDSEL0_G0	32	GPIO Group 0 RDSEL Control Register 0
10211830	GPIO_PULLEN0_G0	32	GPIO Group 0 PULLEN Control Register 0
10211850	GPIO_PULLSEL0_G0	32	GPIO Group 0 PULLSEL Control Register 0
10211870	GPIO_DRV0_G0	32	GPIO Group 0 Driving Control Register 0
10211880	GPIO_PUPD0_G0	32	GPIO Group 0 Special IO PU/PD Control Register0
10211900	GPIO_IES_G1	16	GPIO Group 1 IES Control Register
10211910	GPIO_SMT_G1	16	GPIO Group 1 SMT Control Register

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Address	Name	Width	Register Function
10211920	GPIO_TDSEL0_G1	32	GPIO Group 1 TDSEL Control Register 0
10211924	GPIO_TDSEL1_G1	32	GPIO Group 1 TDSEL Control Register 1
10211928	GPIO_RDSEL0_G1	32	GPIO Group 1 RDSEL Control Register 0
10211930	GPIO_PULLEN0_G1	32	GPIO Group 1 PULLEN Control Register 0
10211950	GPIO_PULLSEL0_G1	32	GPIO Group 1 PULLSEL Control Register 0
10211970	GPIO_DRV0_G1	32	GPIO Group 1 Driving Control Register 0
10211974	GPIO_DRV1_G1	32	GPIO Group 1 Driving Control Register 1
10211980	GPIO_PUPD0_G1	32	GPIO Group 1 Special IO PU/PD Control Register 0
10211A00	GPIO_IES_G2	16	GPIO Group 2 IES Control Register
10211A10	GPIO_SMT_G2	16	GPIO Group 2 SMT Control Register
10211A20	GPIO_TDSEL0_G2	32	GPIO Group 2 TDSEL Control Register 0
10211A24	GPIO_TDSEL1_G2	32	GPIO Group 2 TDSEL Control Register 1
10211A28	GPIO_RDSEL0_G2	32	GPIO Group 2 RDSEL Control Register 0
10211A30	GPIO_PULLEN0_G2	32	GPIO Group 2 PULLEN Control Register 0
10211A40	GPIO_PULLEN1_G2	32	GPIO Group 2 PULLEN Control Register 1
10211A50	GPIO_PULLSEL0_G2	32	GPIO Group 2 PULLSEL Control Register 0
10211A60	GPIO_PULLSEL1_G2	32	GPIO Group 2 PULLSEL Control Register 1
10211A70	GPIO_DRV0_G2	32	GPIO Group 2 Driving Control Register 0
10211A74	GPIO_DRV1_G2	32	GPIO Group 2 Driving Control Register 1
10211A80	GPIO_PUPD0_G2	32	GPIO Group 2 Special IO PU/PD Control Register 0
10211B00	GPIO_IES_G3	8	GPIO Group 3 IES Control Register
10211B10	GPIO_SMT_G3	8	GPIO Group 3 SMT Control Register
10211B20	GPIO_TDSEL0_G3	32	GPIO Group 3 TDSEL Control Register 0
10211B28	GPIO_RDSEL0_G3	32	GPIO Group 3 RDSEL Control Register 0
10211B30	GPIO_PULLEN0_G3	32	GPIO Group 3 PULLEN Control Register 0
10211B50	GPIO_PULLSEL0_G3	32	GPIO Group 3 PULLSEL Control Register 0
10211B70	GPIO_DRV0_G3	32	GPIO Group 3 Driving Control Register 0
10211C00	GPIO_IES_G4	16	GPIO Group 4 IES Control Register
10211C10	GPIO_SMT_G4	16	GPIO Group 4 SMT Control Register
10211C20	GPIO_TDSEL0_G4	32	GPIO Group 4 TDSEL Control Register 0
10211C28	GPIO_RDSEL0_G4	32	GPIO Group 4 RDSEL Control Register 0

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Address	Name	Width	Register Function
10211C70	GPIO_DRV0_G4	32	GPIO Group 4 Driving Control Register 0
10211C80	GPIO_PUPD0_G4	32	GPIO Group 4 Special IO PU/PD Control Register 0
10211C90	GPIO_PUPD1_G4	32	GPIO Group 4 Special IO PU/PD Control Register 1
10211D00	GPIO_IES_G5	16	GPIO Group 5 IES Control Register
10211D10	GPIO_SMT_G5	8	GPIO Group 5 SMT Control Register
10211D20	GPIO_TDSEL0_G5	32	GPIO Group 5 TDSEL Control Register 0
10211D28	GPIO_RDSEL0_G5	32	GPIO Group 5 RDSEL Control Register 0
10211D2C	GPIO_RDSEL1_G5	32	GPIO Group 5 RDSEL Control Register 1
10211D30	GPIO_PULLEN0_G5	32	GPIO Group 5 PULLEN Control Register 0
10211D50	GPIO_PULLSEL0_G5	32	GPIO Group 5 PULLSEL Control Register 0
10211D70	GPIO_DRV0_G5	32	GPIO Group 5 Driving Control Register 0
10211D80	GPIO_PUPD0_G5	32	GPIO Group 5 Special IO PU/PD Control Register 0
10211D90	GPIO_PUPD1_G5	32	GPIO Group 5 Special IO PU/PD Control Register 1

10211000 GPIO_DIR1 GPIO Direction Control Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mne	GPIO31_D	GPIO30_D	GPIO29_D	GPIO28_D	GPIO27_D	GPIO26_D	GPIO25_D	GPIO24_D	GPIO23_D	GPIO22_D	GPIO21_D	GPIO20_D	GPIO19_D	GPIO18_D	GPIO17_D	GPIO16_D
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	GPIO15_D	GPIO14_D	GPIO13_D	GPIO12_D	GPIO11_D	GPIO10_D	GPIO9_D	GPIO8_D	GPIO7_D	GPIO6_D	GPIO5_D	GPIO4_D	GPIO3_D	GPIO2_D	GPIO1_D	GPIO0_D
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	GPIO31_D	GPIO31_DIR	**GPIO 31 direction control** 0: Input 1: Output
30	GPIO30_D	GPIO30_DIR	**GPIO 30 direction control** 0: Input 1: Output
29	GPIO29_D	GPIO29_DIR	**GPIO 29 direction control** 0: Input 1: Output
28	GPIO28_D	GPIO28_DIR	**GPIO 28 direction control** 0: Input 1: Output
27	GPIO27_D	GPIO27_DIR	**GPIO 27 direction control** 0: Input 1: Output

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Bit(s)	Mnemonic	Name	Description
26	**GPIO26_D**	GPIO26_DIR	**GPIO 26 direction control** 0: Input 1: Output
25	**GPIO25_D**	GPIO25_DIR	**GPIO 25 direction control** 0: Input 1: Output
24	**GPIO24_D**	GPIO24_DIR	**GPIO 24 direction control** 0: Input 1: Output
23	**GPIO23_D**	GPIO23_DIR	**GPIO 23 direction control** 0: Input 1: Output
22	**GPIO22_D**	GPIO22_DIR	**GPIO 22 direction control** 0: Input 1: Output
21	**GPIO21_D**	GPIO21_DIR	**GPIO 21 direction control** 0: Input 1: Output
20	**GPIO20_D**	GPIO20_DIR	**GPIO 20 direction control** 0: Input 1: Output
19	**GPIO19_D**	GPIO19_DIR	**GPIO 19 direction control** 0: Input 1: Output
18	**GPIO18_D**	GPIO18_DIR	**GPIO 18 direction control** 0: Input 1: Output
17	**GPIO17_D**	GPIO17_DIR	**GPIO 17 direction control** 0: Input 1: Output
16	**GPIO16_D**	GPIO16_DIR	**GPIO 16 direction control** 0: Input 1: Output
15	**GPIO15_D**	GPIO15_DIR	**GPIO 15 direction control** 0: Input 1: Output
14	**GPIO14_D**	GPIO14_DIR	**GPIO 14 direction control** 0: Input 1: Output
13	**GPIO13_D**	GPIO13_DIR	**GPIO 13 direction control** 0: Input 1: Output
12	**GPIO12_D**	GPIO12_DIR	**GPIO 12 direction control** 0: Input 1: Output
11	**GPIO11_D**	GPIO11_DIR	**GPIO 11 direction control** 0: Input 1: Output
10	**GPIO10_D**	GPIO10_DIR	**GPIO 10 direction control** 0: Input 1: Output
9	**GPIO9_D**	GPIO9_DIR	**GPIO 9 direction control** 0: Input

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Bit(s)	Mnemonic	Name	Description
			1: Output
8	**GPIO8_D**	GPIO8_DIR	**GPIO 8 direction control** 0: Input 1: Output
7	**GPIO7_D**	GPIO7_DIR	**GPIO 7 direction control** 0: Input 1: Output
6	**GPIO6_D**	GPIO6_DIR	**GPIO 6 direction control** 0: Input 1: Output
5	**GPIO5_D**	GPIO5_DIR	**GPIO 5 direction control** 0: Input 1: Output
4	**GPIO4_D**	GPIO4_DIR	**GPIO 4 direction control** 0: Input 1: Output
3	**GPIO3_D**	GPIO3_DIR	**GPIO 3 direction control** 0: Input 1: Output
2	**GPIO2_D**	GPIO2_DIR	**GPIO 2 direction control** 0: Input 1: Output
1	**GPIO1_D**	GPIO1_DIR	**GPIO 1 direction control** 0: Input 1: Output
0	**GPIO0_D**	GPIO0_DIR	**GPIO 0 direction control** 0: Input 1: Output

10211010 **GPIO_DIR2** **GPIO Direction Control Register 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mne	GPIO63_D	GPIO62_D	GPIO61_D	GPIO60_D	GPIO59_D	GPIO58_D	GPIO57_D	GPIO56_D	GPIO55_D	GPIO54_D	GPIO53_D	GPIO52_D	GPIO51_D	GPIO50_D	GPIO49_D	GPIO48_D
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	GPIO47_D	GPIO46_D	GPIO45_D	GPIO44_D	GPIO43_D	GPIO42_D	GPIO41_D	GPIO40_D	GPIO39_D	GPIO38_D	GPIO37_D	GPIO36_D	GPIO35_D	GPIO34_D	GPIO33_D	GPIO32_D
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPIO63_D**	GPIO63_DIR	**GPIO 63 direction control** 0: Input 1: Output
30	**GPIO62_D**	GPIO62_DIR	**GPIO 62 direction control** 0: Input 1: Output
29	**GPIO61_D**	GPIO61_DIR	**GPIO 61 direction control** 0: Input 1: Output

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Bit(s)	Mnemonic	Name	Description
28	**GPIO60_D**	GPIO60_DIR	**GPIO 60 direction control** 0: Input 1: Output
27	**GPIO59_D**	GPIO59_DIR	**GPIO 59 direction control** 0: Input 1: Output
26	**GPIO58_D**	GPIO58_DIR	**GPIO 58 direction control** 0: Input 1: Output
25	**GPIO57_D**	GPIO57_DIR	**GPIO 57 direction control** 0: Input 1: Output
24	**GPIO56_D**	GPIO56_DIR	**GPIO 56 direction control** 0: Input 1: Output
23	**GPIO55_D**	GPIO55_DIR	**GPIO 55 direction control** 0: Input 1: Output
22	**GPIO54_D**	GPIO54_DIR	**GPIO 54 direction control** 0: Input 1: Output
21	**GPIO53_D**	GPIO53_DIR	**GPIO 53 direction control** 0: Input 1: Output
20	**GPIO52_D**	GPIO52_DIR	**GPIO 52 direction control** 0: Input 1: Output
19	**GPIO51_D**	GPIO51_DIR	**GPIO 51 direction control** 0: Input 1: Output
18	**GPIO50_D**	GPIO50_DIR	**GPIO 50 direction control** 0: Input 1: Output
17	**GPIO49_D**	GPIO49_DIR	**GPIO 49 direction control** 0: Input 1: Output
16	**GPIO48_D**	GPIO48_DIR	**GPIO 48 direction control** 0: Input 1: Output
15	**GPIO47_D**	GPIO47_DIR	**GPIO 47 direction control** 0: Input 1: Output
14	**GPIO46_D**	GPIO46_DIR	**GPIO 46 direction control** 0: Input 1: Output
13	**GPIO45_D**	GPIO45_DIR	**GPIO 45 direction control** 0: Input 1: Output
12	**GPIO44_D**	GPIO44_DIR	**GPIO 44 direction control** 0: Input 1: Output
11	**GPIO43_D**	GPIO43_DIR	**GPIO 43 direction control** 0: Input

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Bit(s)	Mnemonic	Name	Description
			1: Output
10	**GPIO42_D**	GPIO42_DIR	**GPIO 42 direction control** 0: Input 1: Output
9	**GPIO41_D**	GPIO41_DIR	**GPIO 41 direction control** 0: Input 1: Output
8	**GPIO40_D**	GPIO40_DIR	**GPIO 40 direction control** 0: Input 1: Output
7	**GPIO39_D**	GPIO39_DIR	**GPIO 39 direction control** 0: Input 1: Output
6	**GPIO38_D**	GPIO38_DIR	**GPIO 38 direction control** 0: Input 1: Output
5	**GPIO37_D**	GPIO37_DIR	**GPIO 37 direction control** 0: Input 1: Output
4	**GPIO36_D**	GPIO36_DIR	**GPIO 36 direction control** 0: Input 1: Output
3	**GPIO35_D**	GPIO35_DIR	**GPIO 35 direction control** 0: Input 1: Output
2	**GPIO34_D**	GPIO34_DIR	**GPIO 34 direction control** 0: Input 1: Output
1	**GPIO33_D**	GPIO33_DIR	**GPIO 33 direction control** 0: Input 1: Output
0	**GPIO32_D**	GPIO32_DIR	**GPIO 32 direction control** 0: Input 1: Output

10211020 **GPIO_DIR3** **GPIO Direction Control Register 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mne	GPIO95_D	GPIO94_D	GPIO93_D	GPIO92_D	GPIO91_D	GPIO90_D	GPIO89_D	GPIO88_D	GPIO87_D	GPIO86_D	GPIO85_D	GPIO84_D	GPIO83_D	GPIO82_D	GPIO81_D	GPIO80_D
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	GPIO79_D	GPIO78_D	GPIO77_D	GPIO76_D	GPIO75_D	GPIO74_D	GPIO73_D	GPIO72_D	GPIO71_D	GPIO70_D	GPIO69_D	GPIO68_D	GPIO67_D	GPIO66_D	GPIO65_D	GPIO64_D
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPIO95_D**	GPIO95_DIR	**GPIO 95 direction control** 0: Input 1: Output

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Bit(s)	Mnemonic	Name	Description
30	**GPIO94_D**	GPIO94_DIR	**GPIO 94 direction control** 0: Input 1: Output
29	**GPIO93_D**	GPIO93_DIR	**GPIO 93 direction control** 0: Input 1: Output
28	**GPIO92_D**	GPIO92_DIR	**GPIO 92 direction control** 0: Input 1: Output
27	**GPIO91_D**	GPIO91_DIR	**GPIO 91 direction control** 0: Input 1: Output
26	**GPIO90_D**	GPIO90_DIR	**GPIO 90 direction control** 0: Input 1: Output
25	**GPIO89_D**	GPIO89_DIR	**GPIO 89 direction control** 0: Input 1: Output
24	**GPIO88_D**	GPIO88_DIR	**GPIO 88 direction control** 0: Input 1: Output
23	**GPIO87_D**	GPIO87_DIR	**GPIO 87 direction control** 0: Input 1: Output
22	**GPIO86_D**	GPIO86_DIR	**GPIO 86 direction control** 0: Input 1: Output
21	**GPIO85_D**	GPIO85_DIR	**GPIO 85 direction control** 0: Input 1: Output
20	**GPIO84_D**	GPIO84_DIR	**GPIO 84 direction control** 0: Input 1: Output
19	**GPIO83_D**	GPIO83_DIR	**GPIO 83 direction control** 0: Input 1: Output
18	**GPIO82_D**	GPIO82_DIR	**GPIO 82 direction control** 0: Input 1: Output
17	**GPIO81_D**	GPIO81_DIR	**GPIO 81 direction control** 0: Input 1: Output
16	**GPIO80_D**	GPIO80_DIR	**GPIO 80 direction control** 0: Input 1: Output
15	**GPIO79_D**	GPIO79_DIR	**GPIO 79 direction control** 0: Input 1: Output
14	**GPIO78_D**	GPIO78_DIR	**GPIO 78 direction control** 0: Input 1: Output
13	**GPIO77_D**	GPIO77_DIR	**GPIO 77 direction control** 0: Input

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Bit(s)	Mnemonic	Name	Description
			1: Output
12	**GPIO76_D**	GPIO76_DIR	**GPIO 76 direction control** 0: Input 1: Output
11	**GPIO75_D**	GPIO75_DIR	**GPIO 75 direction control** 0: Input 1: Output
10	**GPIO74_D**	GPIO74_DIR	**GPIO 74 direction control** 0: Input 1: Output
9	**GPIO73_D**	GPIO73_DIR	**GPIO 73 direction control** 0: Input 1: Output
8	**GPIO72_D**	GPIO72_DIR	**GPIO 72 direction control** 0: Input 1: Output
7	**GPIO71_D**	GPIO71_DIR	**GPIO 71 direction control** 0: Input 1: Output
6	**GPIO70_D**	GPIO70_DIR	**GPIO 70 direction control** 0: Input 1: Output
5	**GPIO69_D**	GPIO69_DIR	**GPIO 69 direction control** 0: Input 1: Output
4	**GPIO68_D**	GPIO68_DIR	**GPIO 68 direction control** 0: Input 1: Output
3	**GPIO67_D**	GPIO67_DIR	**GPIO 67 direction control** 0: Input 1: Output
2	**GPIO66_D**	GPIO66_DIR	**GPIO 66 direction control** 0: Input 1: Output
1	**GPIO65_D**	GPIO65_DIR	**GPIO 65 direction control** 0: Input 1: Output
0	**GPIO64_D**	GPIO64_DIR	**GPIO 64 direction control** 0: Input 1: Output

10211030 **GPIO_DIR4** **GPIO Direction Control Register 4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mne	**GPIO127_D**	**GPIO126_D**	**GPIO125_D**	**GPIO124_D**	**GPIO123_D**	**GPIO122_D**	**GPIO121_D**	**GPIO120_D**	**GPIO119_D**	**GPIO118_D**	**GPIO117_D**	**GPIO116_D**	**GPIO115_D**	**GPIO114_D**	**GPIO113_D**	**GPIO112_D**
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	**GPIO111_D**	**GPIO110_D**	**GPIO109_D**	**GPIO108_D**	**GPIO107_D**	**GPIO106_D**	**GPIO105_D**	**GPIO104_D**	**GPIO103_D**	**GPIO102_D**	**GPIO101_D**	**GPIO100_D**	**GPIO99_D**	**GPIO98_D**	**GPIO97_D**	**GPIO96_D**

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Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPIO127_D**	GPIO127_DIR	**GPIO 127 direction control** 0: Input 1: Output
30	**GPIO126_D**	GPIO126_DIR	**GPIO 126 direction control** 0: Input 1: Output
29	**GPIO125_D**	GPIO125_DIR	**GPIO 125 direction control** 0: Input 1: Output
28	**GPIO124_D**	GPIO124_DIR	**GPIO 124 direction control** 0: Input 1: Output
27	**GPIO123_D**	GPIO123_DIR	**GPIO 123 direction control** 0: Input 1: Output
26	**GPIO122_D**	GPIO122_DIR	**GPIO 122 direction control** 0: Input 1: Output
25	**GPIO121_D**	GPIO121_DIR	**GPIO 121 direction control** 0: Input 1: Output
24	**GPIO120_D**	GPIO120_DIR	**GPIO 120 direction control** 0: Input 1: Output
23	**GPIO119_D**	GPIO119_DIR	**GPIO 119 direction control** 0: Input 1: Output
22	**GPIO118_D**	GPIO118_DIR	**GPIO 118 direction control** 0: Input 1: Output
21	**GPIO117_D**	GPIO117_DIR	**GPIO 117 direction control** 0: Input 1: Output
20	**GPIO116_D**	GPIO116_DIR	**GPIO 116 direction control** 0: Input 1: Output
19	**GPIO115_D**	GPIO115_DIR	**GPIO 115 direction control** 0: Input 1: Output
18	**GPIO114_D**	GPIO114_DIR	**GPIO 114 direction control** 0: Input 1: Output
17	**GPIO113_D**	GPIO113_DIR	**GPIO 113 direction control** 0: Input 1: Output
16	**GPIO112_D**	GPIO112_DIR	**GPIO 112 direction control** 0: Input 1: Output
15	**GPIO111_D**	GPIO111_DIR	**GPIO 111 direction control** 0: Input

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Bit(s)	Mnemonic	Name	Description
			1: Output
14	**GPIO110_D**	GPIO110_DIR	**GPIO 110 direction control** 0: Input 1: Output
13	**GPIO109_D**	GPIO109_DIR	**GPIO 109 direction control** 0: Input 1: Output
12	**GPIO108_D**	GPIO108_DIR	**GPIO 108 direction control** 0: Input 1: Output
11	**GPIO107_D**	GPIO107_DIR	**GPIO 107 direction control** 0: Input 1: Output
10	**GPIO106_D**	GPIO106_DIR	**GPIO 106 direction control** 0: Input 1: Output
9	**GPIO105_D**	GPIO105_DIR	**GPIO 105 direction control** 0: Input 1: Output
8	**GPIO104_D**	GPIO104_DIR	**GPIO 104 direction control** 0: Input 1: Output
7	**GPIO103_D**	GPIO103_DIR	**GPIO 103 direction control** 0: Input 1: Output
6	**GPIO102_D**	GPIO102_DIR	**GPIO 102 direction control** 0: Input 1: Output
5	**GPIO101_D**	GPIO101_DIR	**GPIO 101 direction control** 0: Input 1: Output
4	**GPIO100_D**	GPIO100_DIR	**GPIO 100 direction control** 0: Input 1: Output
3	**GPIO99_D**	GPIO99_DIR	**GPIO 99 direction control** 0: Input 1: Output
2	**GPIO98_D**	GPIO98_DIR	**GPIO 98 direction control** 0: Input 1: Output
1	**GPIO97_D**	GPIO97_DIR	**GPIO 97 direction control** 0: Input 1: Output
0	**GPIO96_D**	GPIO96_DIR	**GPIO 96 direction control** 0: Input 1: Output

10211040 **GPIO_DIR5** **GPIO Direction Control Register 5** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mne	GPIO159_	GPIO158_	GPIO157_D	GPIO156_	GPIO155_	GPIO154_	GPIO153_	GPIO152_	GPIO151_D	GPIO150_	GPIO149_	GPIO148_	GPIO147_	GPIO146_	GPIO145_	GPIO144_

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	D	D		D	D	D	D	D		D	D	D	D	D	D	D
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	GPIO143_D	GPIO142_D	GPIO141_D	GPIO140_D	GPIO139_D	GPIO138_D	GPIO137_D	GPIO136_D	GPIO135_D	GPIO134_D	GPIO133_D	GPIO132_D	GPIO131_D	GPIO130_D	GPIO129_D	GPIO128_D
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPIO159_D**	GPIO159_DIR	**GPIO 159 direction control** 0: Input 1: Output
30	**GPIO158_D**	GPIO158_DIR	**GPIO 158 direction control** 0: Input 1: Output
29	**GPIO157_D**	GPIO157_DIR	**GPIO 157 direction control** 0: Input 1: Output
28	**GPIO156_D**	GPIO156_DIR	**GPIO 156 direction control** 0: Input 1: Output
27	**GPIO155_D**	GPIO155_DIR	**GPIO 155 direction control** 0: Input 1: Output
26	**GPIO154_D**	GPIO154_DIR	**GPIO 154 direction control** 0: Input 1: Output
25	**GPIO153_D**	GPIO153_DIR	**GPIO 153 direction control** 0: Input 1: Output
24	**GPIO152_D**	GPIO152_DIR	**GPIO 152 direction control** 0: Input 1: Output
23	**GPIO151_D**	GPIO151_DIR	**GPIO 151 direction control** 0: Input 1: Output
22	**GPIO150_D**	GPIO150_DIR	**GPIO 150 direction control** 0: Input 1: Output
21	**GPIO149_D**	GPIO149_DIR	**GPIO 149 direction control** 0: Input 1: Output
20	**GPIO148_D**	GPIO148_DIR	**GPIO 148 direction control** 0: Input 1: Output
19	**GPIO147_D**	GPIO147_DIR	**GPIO 147 direction control** 0: Input 1: Output
18	**GPIO146_D**	GPIO146_DIR	**GPIO 146 direction control** 0: Input 1: Output
17	**GPIO145_D**	GPIO145_DIR	**GPIO 145 direction control** 0: Input

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Bit(s)	Mnemonic	Name	Description
			1: Output
16	**GPIO144_D**	GPIO144_DIR	**GPIO 144 direction control** 0: Input 1: Output
15	**GPIO143_D**	GPIO143_DIR	**GPIO 143 direction control** 0: Input 1: Output
14	**GPIO142_D**	GPIO142_DIR	**GPIO 142 direction control** 0: Input 1: Output
13	**GPIO141_D**	GPIO141_DIR	**GPIO 141 direction control** 0: Input 1: Output
12	**GPIO140_D**	GPIO140_DIR	**GPIO 140 direction control** 0: Input 1: Output
11	**GPIO139_D**	GPIO139_DIR	**GPIO 139 direction control** 0: Input 1: Output
10	**GPIO138_D**	GPIO138_DIR	**GPIO 138 direction control** 0: Input 1: Output
9	**GPIO137_D**	GPIO137_DIR	**GPIO 137 direction control** 0: Input 1: Output
8	**GPIO136_D**	GPIO136_DIR	**GPIO 136 direction control** 0: Input 1: Output
7	**GPIO135_D**	GPIO135_DIR	**GPIO 135 direction control** 0: Input 1: Output
6	**GPIO134_D**	GPIO134_DIR	**GPIO 134 direction control** 0: Input 1: Output
5	**GPIO133_D**	GPIO133_DIR	**GPIO 133 direction control** 0: Input 1: Output
4	**GPIO132_D**	GPIO132_DIR	**GPIO 132 direction control** 0: Input 1: Output
3	**GPIO131_D**	GPIO131_DIR	**GPIO 131 direction control** 0: Input 1: Output
2	**GPIO130_D**	GPIO130_DIR	**GPIO 130 direction control** 0: Input 1: Output
1	**GPIO129_D**	GPIO129_DIR	**GPIO 129 direction control** 0: Input 1: Output
0	**GPIO128_D**	GPIO128_DIR	**GPIO 128 direction control** 0: Input 1: Output

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10211050 GPIO_DIR6 GPIO Direction Control Register 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mne	GPIO191_D	GPIO190_D	GPIO189_D	GPIO188_D	GPIO187_D	GPIO186_D	GPIO185_D	GPIO184_D	GPIO183_D	GPIO182_D	GPIO181_D	GPIO180_D	GPIO179_D	GPIO178_D	GPIO177_D	GPIO176_D
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	GPIO175_D	GPIO174_D	GPIO173_D	GPIO172_D	GPIO171_D	GPIO170_D	GPIO169_D	GPIO168_D	GPIO167_D	GPIO166_D	GPIO165_D	GPIO164_D	GPIO163_D	GPIO162_D	GPIO161_D	GPIO160_D
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	GPIO191_D	GPIO191_DIR	**GPIO 191 direction control** 0: Input 1: Output
30	GPIO190_D	GPIO190_DIR	**GPIO 190 direction control** 0: Input 1: Output
29	GPIO189_D	GPIO189_DIR	**GPIO 189 direction control** 0: Input 1: Output
28	GPIO188_D	GPIO188_DIR	**GPIO 188 direction control** 0: Input 1: Output
27	GPIO187_D	GPIO187_DIR	**GPIO 187 direction control** 0: Input 1: Output
26	GPIO186_D	GPIO186_DIR	**GPIO 186 direction control** 0: Input 1: Output
25	GPIO185_D	GPIO185_DIR	**GPIO 185 direction control** 0: Input 1: Output
24	GPIO184_D	GPIO184_DIR	**GPIO 184 direction control** 0: Input 1: Output
23	GPIO183_D	GPIO183_DIR	**GPIO 183 direction control** 0: Input 1: Output
22	GPIO182_D	GPIO182_DIR	**GPIO 182 direction control** 0: Input 1: Output
21	GPIO181_D	GPIO181_DIR	**GPIO 181 direction control** 0: Input 1: Output
20	GPIO180_D	GPIO180_DIR	**GPIO 180 direction control** 0: Input 1: Output
19	GPIO179_D	GPIO179_DIR	**GPIO 179 direction control** 0: Input 1: Output

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Bit(s)	Mnemonic	Name	Description
18	GPIO178_D	GPIO178_DIR	**GPIO 178 direction control** 0: Input 1: Output
17	GPIO177_D	GPIO177_DIR	**GPIO 177 direction control** 0: Input 1: Output
16	GPIO176_D	GPIO176_DIR	**GPIO 176 direction control** 0: Input 1: Output
15	GPIO175_D	GPIO175_DIR	**GPIO 175 direction control** 0: Input 1: Output
14	GPIO174_D	GPIO174_DIR	**GPIO 174 direction control** 0: Input 1: Output
13	GPIO173_D	GPIO173_DIR	**GPIO 173 direction control** 0: Input 1: Output
12	GPIO172_D	GPIO172_DIR	**GPIO 172 direction control** 0: Input 1: Output
11	GPIO171_D	GPIO171_DIR	**GPIO 171 direction control** 0: Input 1: Output
10	GPIO170_D	GPIO170_DIR	**GPIO 170 direction control** 0: Input 1: Output
9	GPIO169_D	GPIO169_DIR	**GPIO 169 direction control** 0: Input 1: Output
8	GPIO168_D	GPIO168_DIR	**GPIO 168 direction control** 0: Input 1: Output
7	GPIO167_D	GPIO167_DIR	**GPIO 167 direction control** 0: Input 1: Output
6	GPIO166_D	GPIO166_DIR	**GPIO 166 direction control** 0: Input 1: Output
5	GPIO165_D	GPIO165_DIR	**GPIO 165 direction control** 0: Input 1: Output
4	GPIO164_D	GPIO164_DIR	**GPIO 164 direction control** 0: Input 1: Output
3	GPIO163_D	GPIO163_DIR	**GPIO 163 direction control** 0: Input 1: Output
2	GPIO162_D	GPIO162_DIR	**GPIO 162 direction control** 0: Input 1: Output
1	GPIO161_D	GPIO161_DIR	**GPIO 161 direction control** 0: Input

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Bit(s)	Mnemonic	Name	Description
			1: Output
0	GPIO160_D	GPIO160_DIR	**GPIO 160 direction control** 0: Input 1: Output

10211060 GPIO_DIR7 GPIO Direction Control Register 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					GPIO203_D	GPIO202_D	GPIO201_D	GPIO200_D	GPIO199_D	GPIO198_D	GPIO197_D	GPIO196_D	GPIO195_D	GPIO194_D	GPIO193_D	GPIO192_D
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11	GPIO203_D	GPIO203_DIR	**GPIO 203 direction control** 0: Input 1: Output
10	GPIO202_D	GPIO202_DIR	**GPIO 202 direction control** 0: Input 1: Output
9	GPIO201_D	GPIO201_DIR	**GPIO 201 direction control** 0: Input 1: Output
8	GPIO200_D	GPIO200_DIR	**GPIO 200 direction control** 0: Input 1: Output
7	GPIO199_D	GPIO199_DIR	**GPIO 199 direction control** 0: Input 1: Output
6	GPIO198_D	GPIO198_DIR	**GPIO 198 direction control** 0: Input 1: Output
5	GPIO197_D	GPIO197_DIR	**GPIO 197 direction control** 0: Input 1: Output
4	GPIO196_D	GPIO196_DIR	**GPIO 196 direction control** 0: Input 1: Output
3	GPIO195_D	GPIO195_DIR	**GPIO 195 direction control** 0: Input 1: Output
2	GPIO194_D	GPIO194_DIR	**GPIO 194 direction control** 0: Input 1: Output
1	GPIO193_D	GPIO193_DIR	**GPIO 193 direction control** 0: Input 1: Output

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Bit(s)	Mnemonic	Name	Description
0	**GPIO192_D**	GPIO192_DIR	**GPIO 192 direction control** 0: Input 1: Output

10211100 GPIO_DOUT1 GPIO Data Output Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPO31	GPO30	GPO29	GPO28	GPO27	GPO26	GPO25	GPO24	GPO23	GPO22	GPO21	GPO20	GPO19	GPO18	GPO17	GPO16
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPO15	GPO14	GPO13	GPO12	GPO11	GPO10	GPO9	GPO8	GPO7	GPO6	GPO5	GPO4	GPO3	GPO2	GPO1	GPO0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPO31**	GPIO31_DOUT	**GPIO 31 data output value** 0: Output 0 1: Output 1
30	**GPO30**	GPIO30_DOUT	**GPIO 30 data output value** 0: Output 0 1: Output 1
29	**GPO29**	GPIO29_DOUT	**GPIO 29 data output value** 0: Output 0 1: Output 1
28	**GPO28**	GPIO28_DOUT	**GPIO 28 data output value** 0: Output 0 1: Output 1
27	**GPO27**	GPIO27_DOUT	**GPIO 27 data output value** 0: Output 0 1: Output 1
26	**GPO26**	GPIO26_DOUT	**GPIO 26 data output value** 0: Output 0 1: Output 1
25	**GPO25**	GPIO25_DOUT	**GPIO 25 data output value** 0: Output 0 1: Output 1
24	**GPO24**	GPIO24_DOUT	**GPIO 24 data output value** 0: Output 0 1: Output 1
23	**GPO23**	GPIO23_DOUT	**GPIO 23 data output value** 0: Output 0 1: Output 1
22	**GPO22**	GPIO22_DOUT	**GPIO 22 data output value** 0: Output 0 1: Output 1
21	**GPO21**	GPIO21_DOUT	**GPIO 21 data output value** 0: Output 0 1: Output 1
20	**GPO20**	GPIO20_DOUT	**GPIO 20 data output value** 0: Output 0

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Bit(s)	Mnemonic	Name	Description
			1: Output 1
19	**GPO19**	GPIO19_DOUT	**GPIO 19 data output value** 0: Output 0 1: Output 1
18	**GPO18**	GPIO18_DOUT	**GPIO 18 data output value** 0: Output 0 1: Output 1
17	**GPO17**	GPIO17_DOUT	**GPIO 17 data output value** 0: Output 0 1: Output 1
16	**GPO16**	GPIO16_DOUT	**GPIO 16 data output value** 0: Output 0 1: Output 1
15	**GPO15**	GPIO15_DOUT	**GPIO 15 data output value** 0: Output 0 1: Output 1
14	**GPO14**	GPIO14_DOUT	**GPIO 14 data output value** 0: Output 0 1: Output 1
13	**GPO13**	GPIO13_DOUT	**GPIO 13 data output value** 0: Output 0 1: Output 1
12	**GPO12**	GPIO12_DOUT	**GPIO 12 data output value** 0: Output 0 1: Output 1
11	**GPO11**	GPIO11_DOUT	**GPIO 11 data output value** 0: Output 0 1: Output 1
10	**GPO10**	GPIO10_DOUT	**GPIO 10 data output value** 0: Output 0 1: Output 1
9	**GPO9**	GPIO9_DOUT	**GPIO 9 data output value** 0: Output 0 1: Output 1
8	**GPO8**	GPIO8_DOUT	**GPIO 8 data output value** 0: Output 0 1: Output 1
7	**GPO7**	GPIO7_DOUT	**GPIO 7 data output value** 0: Output 0 1: Output 1
6	**GPO6**	GPIO6_DOUT	**GPIO 6 data output value** 0: Output 0 1: Output 1
5	**GPO5**	GPIO5_DOUT	**GPIO 5 data output value** 0: Output 0 1: Output 1
4	**GPO4**	GPIO4_DOUT	**GPIO 4 data output value** 0: Output 0 1: Output 1
3	**GPO3**	GPIO3_DOUT	**GPIO 3 data output value** 0: Output 0 1: Output 1

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Bit(s)	Mnemonic	Name	Description
2	**GPO2**	GPIO2_DOUT	**GPIO 2 data output value** 0: Output 0 1: Output 1
1	**GPO1**	GPIO1_DOUT	**GPIO 1 data output value** 0: Output 0 1: Output 1
0	**GPO0**	GPIO0_DOUT	**GPIO 0 data output value** 0: Output 0 1: Output 1

10211110 **GPIO_DOUT2** **GPIO Data Output Register 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**GPO63**	**GPO62**	**GPO61**	**GPO60**	**GPO59**	**GPO58**	**GPO57**	**GPO56**	**GPO55**	**GPO54**	**GPO53**	**GPO52**	**GPO51**	**GPO50**	**GPO49**	**GPO48**
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**GPO47**	**GPO46**	**GPO45**	**GPO44**	**GPO43**	**GPO42**	**GPO41**	**GPO40**	**GPO39**	**GPO38**	**GPO37**	**GPO36**	**GPO35**	**GPO34**	**GPO33**	**GPO32**
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPO63**	GPIO63_DOUT	**GPIO 63 data output value** 0: Output 0 1: Output 1
30	**GPO62**	GPIO62_DOUT	**GPIO 62 data output value** 0: Output 0 1: Output 1
29	**GPO61**	GPIO61_DOUT	**GPIO 61 data output value** 0: Output 0 1: Output 1
28	**GPO60**	GPIO60_DOUT	**GPIO 60 data output value** 0: Output 0 1: Output 1
27	**GPO59**	GPIO59_DOUT	**GPIO 59 data output value** 0: Output 0 1: Output 1
26	**GPO58**	GPIO58_DOUT	**GPIO 58 data output value** 0: Output 0 1: Output 1
25	**GPO57**	GPIO57_DOUT	**GPIO 57 data output value** 0: Output 0 1: Output 1
24	**GPO56**	GPIO56_DOUT	**GPIO 56 data output value** 0: Output 0 1: Output 1
23	**GPO55**	GPIO55_DOUT	**GPIO 55 data output value** 0: Output 0 1: Output 1
22	**GPO54**	GPIO54_DOUT	**GPIO 54 data output value** 0: Output 0

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Bit(s)	Mnemonic	Name	Description
			1: Output 1
21	**GPO53**	GPIO53_DOUT	**GPIO 53 data output value** 0: Output 0 1: Output 1
20	**GPO52**	GPIO52_DOUT	**GPIO 52 data output value** 0: Output 0 1: Output 1
19	**GPO51**	GPIO51_DOUT	**GPIO 51 data output value** 0: Output 0 1: Output 1
18	**GPO50**	GPIO50_DOUT	**GPIO 50 data output value** 0: Output 0 1: Output 1
17	**GPO49**	GPIO49_DOUT	**GPIO 49 data output value** 0: Output 0 1: Output 1
16	**GPO48**	GPIO48_DOUT	**GPIO 48 data output value** 0: Output 0 1: Output 1
15	**GPO47**	GPIO47_DOUT	**GPIO 47 data output value** 0: Output 0 1: Output 1
14	**GPO46**	GPIO46_DOUT	**GPIO 46 data output value** 0: Output 0 1: Output 1
13	**GPO45**	GPIO45_DOUT	**GPIO 45 data output value** 0: Output 0 1: Output 1
12	**GPO44**	GPIO44_DOUT	**GPIO 44 data output value** 0: Output 0 1: Output 1
11	**GPO43**	GPIO43_DOUT	**GPIO 43 data output value** 0: Output 0 1: Output 1
10	**GPO42**	GPIO42_DOUT	**GPIO 42 data output value** 0: Output 0 1: Output 1
9	**GPO41**	GPIO41_DOUT	**GPIO 41 data output value** 0: Output 0 1: Output 1
8	**GPO40**	GPIO40_DOUT	**GPIO 40 data output value** 0: Output 0 1: Output 1
7	**GPO39**	GPIO39_DOUT	**GPIO 39 data output value** 0: Output 0 1: Output 1
6	**GPO38**	GPIO38_DOUT	**GPIO 38 data output value** 0: Output 0 1: Output 1
5	**GPO37**	GPIO37_DOUT	**GPIO 37 data output value** 0: Output 0 1: Output 1

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Bit(s)	Mnemonic	Name	Description
4	**GPO36**	GPIO36_DOUT	**GPIO 36 data output value** 0: Output 0 1: Output 1
3	**GPO35**	GPIO35_DOUT	**GPIO 35 data output value** 0: Output 0 1: Output 1
2	**GPO34**	GPIO34_DOUT	**GPIO 34 data output value** 0: Output 0 1: Output 1
1	**GPO33**	GPIO33_DOUT	**GPIO 33 data output value** 0: Output 0 1: Output 1
0	**GPO32**	GPIO32_DOUT	**GPIO 32 data output value** 0: Output 0 1: Output 1

10211120 GPIO_DOUT3 GPIO Data Output Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**GPO95**	**GPO94**	**GPO93**	**GPO92**	**GPO91**	**GPO90**	**GPO89**	**GPO88**	**GPO87**	**GPO86**	**GPO85**	**GPO84**	**GPO83**	**GPO82**	**GPO81**	**GPO80**
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**GPO79**	**GPO78**	**GPO77**	**GPO76**	**GPO75**	**GPO74**	**GPO73**	**GPO72**	**GPO71**	**GPO70**	**GPO69**	**GPO68**	**GPO67**	**GPO66**	**GPO65**	**GPO64**
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPO95**	GPIO95_DOUT	**GPIO 95 data output value** 0: Output 0 1: Output 1
30	**GPO94**	GPIO94_DOUT	**GPIO 94 data output value** 0: Output 0 1: Output 1
29	**GPO93**	GPIO93_DOUT	**GPIO 93 data output value** 0: Output 0 1: Output 1
28	**GPO92**	GPIO92_DOUT	**GPIO 92 data output value** 0: Output 0 1: Output 1
27	**GPO91**	GPIO91_DOUT	**GPIO 91 data output value** 0: Output 0 1: Output 1
26	**GPO90**	GPIO90_DOUT	**GPIO 90 data output value** 0: Output 0 1: Output 1
25	**GPO89**	GPIO89_DOUT	**GPIO 89 data output value** 0: Output 0 1: Output 1
24	**GPO88**	GPIO88_DOUT	**GPIO 88 data output value** 0: Output 0

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Bit(s)	Mnemonic	Name	Description
			1: Output 1
23	**GPO87**	GPIO87_DOUT	**GPIO 87 data output value** 0: Output 0 1: Output 1
22	**GPO86**	GPIO86_DOUT	**GPIO 86 data output value** 0: Output 0 1: Output 1
21	**GPO85**	GPIO85_DOUT	**GPIO 85 data output value** 0: Output 0 1: Output 1
20	**GPO84**	GPIO84_DOUT	**GPIO 84 data output value** 0: Output 0 1: Output 1
19	**GPO83**	GPIO83_DOUT	**GPIO 83 data output value** 0: Output 0 1: Output 1
18	**GPO82**	GPIO82_DOUT	**GPIO 82 data output value** 0: Output 0 1: Output 1
17	**GPO81**	GPIO81_DOUT	**GPIO 81 data output value** 0: Output 0 1: Output 1
16	**GPO80**	GPIO80_DOUT	**GPIO 80 data output value** 0: Output 0 1: Output 1
15	**GPO79**	GPIO79_DOUT	**GPIO 79 data output value** 0: Output 0 1: Output 1
14	**GPO78**	GPIO78_DOUT	**GPIO 78 data output value** 0: Output 0 1: Output 1
13	**GPO77**	GPIO77_DOUT	**GPIO 77 data output value** 0: Output 0 1: Output 1
12	**GPO76**	GPIO76_DOUT	**GPIO 76 data output value** 0: Output 0 1: Output 1
11	**GPO75**	GPIO75_DOUT	**GPIO 75 data output value** 0: Output 0 1: Output 1
10	**GPO74**	GPIO74_DOUT	**GPIO 74 data output value** 0: Output 0 1: Output 1
9	**GPO73**	GPIO73_DOUT	**GPIO 73 data output value** 0: Output 0 1: Output 1
8	**GPO72**	GPIO72_DOUT	**GPIO 72 data output value** 0: Output 0 1: Output 1
7	**GPO71**	GPIO71_DOUT	**GPIO 71 data output value** 0: Output 0 1: Output 1

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Bit(s)	Mnemonic	Name	Description
6	**GPO70**	GPIO70_DOUT	**GPIO 70 data output value** 0: Output 0 1: Output 1
5	**GPO69**	GPIO69_DOUT	**GPIO 69 data output value** 0: Output 0 1: Output 1
4	**GPO68**	GPIO68_DOUT	**GPIO 68 data output value** 0: Output 0 1: Output 1
3	**GPO67**	GPIO67_DOUT	**GPIO 67 data output value** 0: Output 0 1: Output 1
2	**GPO66**	GPIO66_DOUT	**GPIO 66 data output value** 0: Output 0 1: Output 1
1	**GPO65**	GPIO65_DOUT	**GPIO 65 data output value** 0: Output 0 1: Output 1
0	**GPO64**	GPIO64_DOUT	**GPIO 64 data output value** 0: Output 0 1: Output 1

10211130 **GPIO_DOUT4** **GPIO Data Output Register 4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**GPO127**	**GPO126**	**GPO125**	**GPO124**	**GPO123**	**GPO122**	**GPO121**	**GPO120**	**GPO119**	**GPO118**	**GPO117**	**GPO116**	**GPO115**	**GPO114**	**GPO113**	**GPO112**
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**GPO111**	**GPO110**	**GPO109**	**GPO108**	**GPO107**	**GPO106**	**GPO105**	**GPO104**	**GPO103**	**GPO102**	**GPO101**	**GPO100**	**GPO99**	**GPO98**	**GPO97**	**GPO96**
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPO127**	GPIO127_DOUT	**GPIO 127 data output value** 0: Output 0 1: Output 1
30	**GPO126**	GPIO126_DOUT	**GPIO 126 data output value** 0: Output 0 1: Output 1
29	**GPO125**	GPIO125_DOUT	**GPIO 125 data output value** 0: Output 0 1: Output 1
28	**GPO124**	GPIO124_DOUT	**GPIO 124 data output value** 0: Output 0 1: Output 1
27	**GPO123**	GPIO123_DOUT	**GPIO 123 data output value** 0: Output 0 1: Output 1
26	**GPO122**	GPIO122_DOUT	**GPIO 122 data output value** 0: Output 0

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Bit(s)	Mnemonic	Name	Description
			1: Output 1
25	**GPO121**	GPIO121_DOUT	**GPIO 121 data output value** 0: Output 0 1: Output 1
24	**GPO120**	GPIO120_DOUT	**GPIO 120 data output value** 0: Output 0 1: Output 1
23	**GPO119**	GPIO119_DOUT	**GPIO 119 data output value** 0: Output 0 1: Output 1
22	**GPO118**	GPIO118_DOUT	**GPIO 118 data output value** 0: Output 0 1: Output 1
21	**GPO117**	GPIO117_DOUT	**GPIO 117 data output value** 0: Output 0 1: Output 1
20	**GPO116**	GPIO116_DOUT	**GPIO 116 data output value** 0: Output 0 1: Output 1
19	**GPO115**	GPIO115_DOUT	**GPIO 115 data output value** 0: Output 0 1: Output 1
18	**GPO114**	GPIO114_DOUT	**GPIO 114 data output value** 0: Output 0 1: Output 1
17	**GPO113**	GPIO113_DOUT	**GPIO 113 data output value** 0: Output 0 1: Output 1
16	**GPO112**	GPIO112_DOUT	**GPIO 112 data output value** 0: Output 0 1: Output 1
15	**GPO111**	GPIO111_DOUT	**GPIO 111 data output value** 0: Output 0 1: Output 1
14	**GPO110**	GPIO110_DOUT	**GPIO 110 data output value** 0: Output 0 1: Output 1
13	**GPO109**	GPIO109_DOUT	**GPIO 109 data output value** 0: Output 0 1: Output 1
12	**GPO108**	GPIO108_DOUT	**GPIO 108 data output value** 0: Output 0 1: Output 1
11	**GPO107**	GPIO107_DOUT	**GPIO 107 data output value** 0: Output 0 1: Output 1
10	**GPO106**	GPIO106_DOUT	**GPIO 106 data output value** 0: Output 0 1: Output 1
9	**GPO105**	GPIO105_DOUT	**GPIO 105 data output value** 0: Output 0 1: Output 1

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Bit(s)	Mnemonic	Name	Description
8	**GPO104**	GPIO104_DOUT	**GPIO 104 data output value** 0: Output 0 1: Output 1
7	**GPO103**	GPIO103_DOUT	**GPIO 103 data output value** 0: Output 0 1: Output 1
6	**GPO102**	GPIO102_DOUT	**GPIO 102 data output value** 0: Output 0 1: Output 1
5	**GPO101**	GPIO101_DOUT	**GPIO 101 data output value** 0: Output 0 1: Output 1
4	**GPO100**	GPIO100_DOUT	**GPIO 100 data output value** 0: Output 0 1: Output 1
3	**GPO99**	GPIO99_DOUT	**GPIO 99 data output value** 0: Output 0 1: Output 1
2	**GPO98**	GPIO98_DOUT	**GPIO 98 data output value** 0: Output 0 1: Output 1
1	**GPO97**	GPIO97_DOUT	**GPIO 97 data output value** 0: Output 0 1: Output 1
0	**GPO96**	GPIO96_DOUT	**GPIO 96 data output value** 0: Output 0 1: Output 1

10211140 GPIO_DOUT5 GPIO Data Output Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**GPO159**	**GPO158**	**GPO157**	**GPO156**	**GPO155**	**GPO154**	**GPO153**	**GPO152**	**GPO151**	**GPO150**	**GPO149**	**GPO148**	**GPO147**	**GPO146**	**GPO145**	**GPO144**
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**GPO143**	**GPO142**	**GPO141**	**GPO140**	**GPO139**	**GPO138**	**GPO137**	**GPO136**	**GPO135**	**GPO134**	**GPO133**	**GPO132**	**GPO131**	**GPO130**	**GPO129**	**GPO128**
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPO159**	GPIO159_DOUT	**GPIO 159 data output value** 0: Output 0 1: Output 1
30	**GPO158**	GPIO158_DOUT	**GPIO 158 data output value** 0: Output 0 1: Output 1
29	**GPO157**	GPIO157_DOUT	**GPIO 157 data output value** 0: Output 0 1: Output 1
28	**GPO156**	GPIO156_DOUT	**GPIO 156 data output value** 0: Output 0

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Bit(s)	Mnemonic	Name	Description
			1: Output 1
27	**GPO155**	GPIO155_DOUT	**GPIO 155 data output value** 0: Output 0 1: Output 1
26	**GPO154**	GPIO154_DOUT	**GPIO 154 data output value** 0: Output 0 1: Output 1
25	**GPO153**	GPIO153_DOUT	**GPIO 153 data output value** 0: Output 0 1: Output 1
24	**GPO152**	GPIO152_DOUT	**GPIO 152 data output value** 0: Output 0 1: Output 1
23	**GPO151**	GPIO151_DOUT	**GPIO 151 data output value** 0: Output 0 1: Output 1
22	**GPO150**	GPIO150_DOUT	**GPIO 150 data output value** 0: Output 0 1: Output 1
21	**GPO149**	GPIO149_DOUT	**GPIO 149 data output value** 0: Output 0 1: Output 1
20	**GPO148**	GPIO148_DOUT	**GPIO 148 data output value** 0: Output 0 1: Output 1
19	**GPO147**	GPIO147_DOUT	**GPIO 147 data output value** 0: Output 0 1: Output 1
18	**GPO146**	GPIO146_DOUT	**GPIO 146 data output value** 0: Output 0 1: Output 1
17	**GPO145**	GPIO145_DOUT	**GPIO 145 data output value** 0: Output 0 1: Output 1
16	**GPO144**	GPIO144_DOUT	**GPIO 144 data output value** 0: Output 0 1: Output 1
15	**GPO143**	GPIO143_DOUT	**GPIO 143 data output value** 0: Output 0 1: Output 1
14	**GPO142**	GPIO142_DOUT	**GPIO 142 data output value** 0: Output 0 1: Output 1
13	**GPO141**	GPIO141_DOUT	**GPIO 141 data output value** 0: Output 0 1: Output 1
12	**GPO140**	GPIO140_DOUT	**GPIO 140 data output value** 0: Output 0 1: Output 1
11	**GPO139**	GPIO139_DOUT	**GPIO 139 data output value** 0: Output 0 1: Output 1

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Bit(s)	Mnemonic	Name	Description
10	**GPO138**	GPIO138_DOUT	**GPIO 138 data output value** 0: Output 0 1: Output 1
9	**GPO137**	GPIO137_DOUT	**GPIO 137 data output value** 0: Output 0 1: Output 1
8	**GPO136**	GPIO136_DOUT	**GPIO 136 data output value** 0: Output 0 1: Output 1
7	**GPO135**	GPIO135_DOUT	**GPIO 135 data output value** 0: Output 0 1: Output 1
6	**GPO134**	GPIO134_DOUT	**GPIO 134 data output value** 0: Output 0 1: Output 1
5	**GPO133**	GPIO133_DOUT	**GPIO 133 data output value** 0: Output 0 1: Output 1
4	**GPO132**	GPIO132_DOUT	**GPIO 132 data output value** 0: Output 0 1: Output 1
3	**GPO131**	GPIO131_DOUT	**GPIO 131 data output value** 0: Output 0 1: Output 1
2	**GPO130**	GPIO130_DOUT	**GPIO 130 data output value** 0: Output 0 1: Output 1
1	**GPO129**	GPIO129_DOUT	**GPIO 129 data output value** 0: Output 0 1: Output 1
0	**GPO128**	GPIO128_DOUT	**GPIO 128 data output value** 0: Output 0 1: Output 1

10211150 GPIO_DOUT6 GPIO Data Output Register 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**GPO191**	**GPO190**	**GPO189**	**GPO188**	**GPO187**	**GPO186**	**GPO185**	**GPO184**	**GPO183**	**GPO182**	**GPO181**	**GPO180**	**GPO179**	**GPO178**	**GPO177**	**GPO176**
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**GPO175**	**GPO174**	**GPO173**	**GPO172**	**GPO171**	**GPO170**	**GPO169**	**GPO168**	**GPO167**	**GPO166**	**GPO165**	**GPO164**	**GPO163**	**GPO162**	**GPO161**	**GPO160**
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPO191**	GPIO191_DOUT	**GPIO 191 data output value** 0: Output 0 1: Output 1
30	**GPO190**	GPIO190_DOUT	**GPIO 190 data output value** 0: Output 0

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Bit(s)	Mnemonic	Name	Description
			1: Output 1
29	**GPO189**	GPIO189_DOUT	**GPIO 189 data output value** 0: Output 0 1: Output 1
28	**GPO188**	GPIO188_DOUT	**GPIO 188 data output value** 0: Output 0 1: Output 1
27	**GPO187**	GPIO187_DOUT	**GPIO 187 data output value** 0: Output 0 1: Output 1
26	**GPO186**	GPIO186_DOUT	**GPIO 186 data output value** 0: Output 0 1: Output 1
25	**GPO185**	GPIO185_DOUT	**GPIO 185 data output value** 0: Output 0 1: Output 1
24	**GPO184**	GPIO184_DOUT	**GPIO 184 data output value** 0: Output 0 1: Output 1
23	**GPO183**	GPIO183_DOUT	**GPIO 183 data output value** 0: Output 0 1: Output 1
22	**GPO182**	GPIO182_DOUT	**GPIO 182 data output value** 0: Output 0 1: Output 1
21	**GPO181**	GPIO181_DOUT	**GPIO 181 data output value** 0: Output 0 1: Output 1
20	**GPO180**	GPIO180_DOUT	**GPIO 180 data output value** 0: Output 0 1: Output 1
19	**GPO179**	GPIO179_DOUT	**GPIO 179 data output value** 0: Output 0 1: Output 1
18	**GPO178**	GPIO178_DOUT	**GPIO 178 data output value** 0: Output 0 1: Output 1
17	**GPO177**	GPIO177_DOUT	**GPIO 177 data output value** 0: Output 0 1: Output 1
16	**GPO176**	GPIO176_DOUT	**GPIO 176 data output value** 0: Output 0 1: Output 1
15	**GPO175**	GPIO175_DOUT	**GPIO 175 data output value** 0: Output 0 1: Output 1
14	**GPO174**	GPIO174_DOUT	**GPIO 174 data output value** 0: Output 0 1: Output 1
13	**GPO173**	GPIO173_DOUT	**GPIO 173 data output value** 0: Output 0 1: Output 1

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Bit(s)	Mnemonic	Name	Description
12	**GPO172**	GPIO172_DOUT	**GPIO 172 data output value** 0: Output 0 1: Output 1
11	**GPO171**	GPIO171_DOUT	**GPIO 171 data output value** 0: Output 0 1: Output 1
10	**GPO170**	GPIO170_DOUT	**GPIO 170 data output value** 0: Output 0 1: Output 1
9	**GPO169**	GPIO169_DOUT	**GPIO 169 data output value** 0: Output 0 1: Output 1
8	**GPO168**	GPIO168_DOUT	**GPIO 168 data output value** 0: Output 0 1: Output 1
7	**GPO167**	GPIO167_DOUT	**GPIO 167 data output value** 0: Output 0 1: Output 1
6	**GPO166**	GPIO166_DOUT	**GPIO 166 data output value** 0: Output 0 1: Output 1
5	**GPO165**	GPIO165_DOUT	**GPIO 165 data output value** 0: Output 0 1: Output 1
4	**GPO164**	GPIO164_DOUT	**GPIO 164 data output value** 0: Output 0 1: Output 1
3	**GPO163**	GPIO163_DOUT	**GPIO 163 data output value** 0: Output 0 1: Output 1
2	**GPO162**	GPIO162_DOUT	**GPIO 162 data output value** 0: Output 0 1: Output 1
1	**GPO161**	GPIO161_DOUT	**GPIO 161 data output value** 0: Output 0 1: Output 1
0	**GPO160**	GPIO160_DOUT	**GPIO 160 data output value** 0: Output 0 1: Output 1

10211160 GPIO_DOUT7 GPIO Data Output Register 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**GPO203**	**GPO202**	**GPO201**	**GPO200**	**GPO199**	**GPO198**	**GPO197**	**GPO196**	**GPO195**	**GPO194**	**GPO193**	**GPO192**
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
11	**GPO203**	GPIO203_DOUT	**GPIO 203 data output value** 0: Output 0 1: Output 1
10	**GPO202**	GPIO202_DOUT	**GPIO 202 data output value** 0: Output 0 1: Output 1
9	**GPO201**	GPIO201_DOUT	**GPIO 201 data output value** 0: Output 0 1: Output 1
8	**GPO200**	GPIO200_DOUT	**GPIO 200 data output value** 0: Output 0 1: Output 1
7	**GPO199**	GPIO199_DOUT	**GPIO 199 data output value** 0: Output 0 1: Output 1
6	**GPO198**	GPIO198_DOUT	**GPIO 198 data output value** 0: Output 0 1: Output 1
5	**GPO197**	GPIO197_DOUT	**GPIO 197 data output value** 0: Output 0 1: Output 1
4	**GPO196**	GPIO196_DOUT	**GPIO 196 data output value** 0: Output 0 1: Output 1
3	**GPO195**	GPIO195_DOUT	**GPIO 195 data output value** 0: Output 0 1: Output 1
2	**GPO194**	GPIO194_DOUT	**GPIO 194 data output value** 0: Output 0 1: Output 1
1	**GPO193**	GPIO193_DOUT	**GPIO 193 data output value** 0: Output 0 1: Output 1
0	**GPO192**	GPIO192_DOUT	**GPIO 192 data output value** 0: Output 0 1: Output 1

10211200 GPIO_DIN1 GPIO Data Input Register 1 NA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPI31	GPI30	GPI29	GPI28	GPI27	GPI26	GPI25	GPI24	GPI23	GPI22	GPI21	GPI20	GPI19	GPI18	GPI17	GPI16
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPI15	GPI14	GPI13	GPI12	GPI11	GPI10	GPI9	GPI8	GPI7	GPI6	GPI5	GPI4	GPI3	GPI2	GPI1	GPI0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit(s)	Mnemonic	Name	Description
31	**GPI31**	GPIO31_DIN	GPIO 31 data input value
30	**GPI30**	GPIO30_DIN	GPIO 30 data input value

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Bit(s)	Mnemonic	Name	Description
29	**GPI29**	GPIO29_DIN	GPIO 29 data input value
28	**GPI28**	GPIO28_DIN	GPIO 28 data input value
27	**GPI27**	GPIO27_DIN	GPIO 27 data input value
26	**GPI26**	GPIO26_DIN	GPIO 26 data input value
25	**GPI25**	GPIO25_DIN	GPIO 25 data input value
24	**GPI24**	GPIO24_DIN	GPIO 24 data input value
23	**GPI23**	GPIO23_DIN	GPIO 23 data input value
22	**GPI22**	GPIO22_DIN	GPIO 22 data input value
21	**GPI21**	GPIO21_DIN	GPIO 21 data input value
20	**GPI20**	GPIO20_DIN	GPIO 20 data input value
19	**GPI19**	GPIO19_DIN	GPIO 19 data input value
18	**GPI18**	GPIO18_DIN	GPIO 18 data input value
17	**GPI17**	GPIO17_DIN	GPIO 17 data input value
16	**GPI16**	GPIO16_DIN	GPIO 16 data input value
15	**GPI15**	GPIO15_DIN	GPIO 15 data input value
14	**GPI14**	GPIO14_DIN	GPIO 14 data input value
13	**GPI13**	GPIO13_DIN	GPIO 13 data input value
12	**GPI12**	GPIO12_DIN	GPIO 12 data input value
11	**GPI11**	GPIO11_DIN	GPIO 11 data input value
10	**GPI10**	GPIO10_DIN	GPIO 10 data input value
9	**GPI9**	GPIO9_DIN	GPIO 9 data input value
8	**GPI8**	GPIO8_DIN	GPIO 8 data input value
7	**GPI7**	GPIO7_DIN	GPIO 7 data input value
6	**GPI6**	GPIO6_DIN	GPIO 6 data input value
5	**GPI5**	GPIO5_DIN	GPIO 5 data input value
4	**GPI4**	GPIO4_DIN	GPIO 4 data input value
3	**GPI3**	GPIO3_DIN	GPIO 3 data input value
2	**GPI2**	GPIO2_DIN	GPIO 2 data input value
1	**GPI1**	GPIO1_DIN	GPIO 1 data input value
0	**GPI0**	GPIO0_DIN	GPIO 0 data input value

10211210 **GPIO_DIN2** **GPIO Data Input Register 2** **NA**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**GPI63**	**GPI62**	**GPI61**	**GPI60**	**GPI59**	**GPI58**	**GPI57**	**GPI56**	**GPI55**	**GPI54**	**GPI53**	**GPI52**	**GPI51**	**GPI50**	**GPI49**	**GPI48**
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**GPI47**	**GPI46**	**GPI45**	**GPI44**	**GPI43**	**GPI42**	**GPI41**	**GPI40**	**GPI39**	**GPI38**	**GPI37**	**GPI36**	**GPI35**	**GPI34**	**GPI33**	**GPI32**
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit(s)	Mnemonic	Name	Description
31	**GPI63**	GPIO63_DIN	GPIO 63 data input value
30	**GPI62**	GPIO62_DIN	GPIO 62 data input value

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Bit(s)	Mnemonic	Name	Description
29	**GPI61**	GPIO61_DIN	GPIO 61 data input value
28	**GPI60**	GPIO60_DIN	GPIO 60 data input value
27	**GPI59**	GPIO59_DIN	GPIO 59 data input value
26	**GPI58**	GPIO58_DIN	GPIO 58 data input value
25	**GPI57**	GPIO57_DIN	GPIO 57 data input value
24	**GPI56**	GPIO56_DIN	GPIO 56 data input value
23	**GPI55**	GPIO55_DIN	GPIO 55 data input value
22	**GPI54**	GPIO54_DIN	GPIO 54 data input value
21	**GPI53**	GPIO53_DIN	GPIO 53 data input value
20	**GPI52**	GPIO52_DIN	GPIO 52 data input value
19	**GPI51**	GPIO51_DIN	GPIO 51 data input value
18	**GPI50**	GPIO50_DIN	GPIO 50 data input value
17	**GPI49**	GPIO49_DIN	GPIO 49 data input value
16	**GPI48**	GPIO48_DIN	GPIO 48 data input value
15	**GPI47**	GPIO47_DIN	GPIO 47 data input value
14	**GPI46**	GPIO46_DIN	GPIO 46 data input value
13	**GPI45**	GPIO45_DIN	GPIO 45 data input value
12	**GPI44**	GPIO44_DIN	GPIO 44 data input value
11	**GPI43**	GPIO43_DIN	GPIO 43 data input value
10	**GPI42**	GPIO42_DIN	GPIO 42 data input value
9	**GPI41**	GPIO41_DIN	GPIO 41 data input value
8	**GPI40**	GPIO40_DIN	GPIO 40 data input value
7	**GPI39**	GPIO39_DIN	GPIO 39 data input value
6	**GPI38**	GPIO38_DIN	GPIO 38 data input value
5	**GPI37**	GPIO37_DIN	GPIO 37 data input value
4	**GPI36**	GPIO36_DIN	GPIO 36 data input value
3	**GPI35**	GPIO35_DIN	GPIO 35 data input value
2	**GPI34**	GPIO34_DIN	GPIO 34 data input value
1	**GPI33**	GPIO33_DIN	GPIO 33 data input value
0	**GPI32**	GPIO32_DIN	GPIO 32 data input value

10211220 **GPIO_DIN3** **GPIO Data Input Register 3** **NA**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPI95	GPI94	GPI93	GPI92	GPI91	GPI90	GPI89	GPI88	GPI87	GPI86	GPI85	GPI84	GPI83	GPI82	GPI81	GPI80
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPI79	GPI78	GPI77	GPI76	GPI75	GPI74	GPI73	GPI72	GPI71	GPI70	GPI69	GPI68	GPI67	GPI66	GPI65	GPI64
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit(s)	Mnemonic	Name	Description
31	**GPI95**	GPIO95_DIN	GPIO 95 data input value
30	**GPI94**	GPIO94_DIN	GPIO 94 data input value

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Bit(s)	Mnemonic	Name	Description
29	**GPI93**	GPIO93_DIN	GPIO 93 data input value
28	**GPI92**	GPIO92_DIN	GPIO 92 data input value
27	**GPI91**	GPIO91_DIN	GPIO 91 data input value
26	**GPI90**	GPIO90_DIN	GPIO 90 data input value
25	**GPI89**	GPIO89_DIN	GPIO 89 data input value
24	**GPI88**	GPIO88_DIN	GPIO 88 data input value
23	**GPI87**	GPIO87_DIN	GPIO 87 data input value
22	**GPI86**	GPIO86_DIN	GPIO 86 data input value
21	**GPI85**	GPIO85_DIN	GPIO 85 data input value
20	**GPI84**	GPIO84_DIN	GPIO 84 data input value
19	**GPI83**	GPIO83_DIN	GPIO 83 data input value
18	**GPI82**	GPIO82_DIN	GPIO 82 data input value
17	**GPI81**	GPIO81_DIN	GPIO 81 data input value
16	**GPI80**	GPIO80_DIN	GPIO 80 data input value
15	**GPI79**	GPIO79_DIN	GPIO 79 data input value
14	**GPI78**	GPIO78_DIN	GPIO 78 data input value
13	**GPI77**	GPIO77_DIN	GPIO 77 data input value
12	**GPI76**	GPIO76_DIN	GPIO 76 data input value
11	**GPI75**	GPIO75_DIN	GPIO 75 data input value
10	**GPI74**	GPIO74_DIN	GPIO 74 data input value
9	**GPI73**	GPIO73_DIN	GPIO 73 data input value
8	**GPI72**	GPIO72_DIN	GPIO 72 data input value
7	**GPI71**	GPIO71_DIN	GPIO 71 data input value
6	**GPI70**	GPIO70_DIN	GPIO 70 data input value
5	**GPI69**	GPIO69_DIN	GPIO 69 data input value
4	**GPI68**	GPIO68_DIN	GPIO 68 data input value
3	**GPI67**	GPIO67_DIN	GPIO 67 data input value
2	**GPI66**	GPIO66_DIN	GPIO 66 data input value
1	**GPI65**	GPIO65_DIN	GPIO 65 data input value
0	**GPI64**	GPIO64_DIN	GPIO 64 data input value

10211230 **GPIO_DIN4** **GPIO Data Input Register 4** **NA**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**GPI127**	**GPI126**	**GPI125**	**GPI124**	**GPI123**	**GPI122**	**GPI121**	**GPI120**	**GPI119**	**GPI118**	**GPI117**	**GPI116**	**GPI115**	**GPI114**	**GPI113**	**GPI112**
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**GPI111**	**GPI110**	**GPI109**	**GPI108**	**GPI107**	**GPI106**	**GPI105**	**GPI104**	**GPI103**	**GPI102**	**GPI101**	**GPI100**	**GPI99**	**GPI98**	**GPI97**	**GPI96**
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit(s)	Mnemonic	Name	Description
31	**GPI127**	GPIO127_DIN	GPIO 127 data input value
30	**GPI126**	GPIO126_DIN	GPIO 126 data input value

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Bit(s)	Mnemonic	Name	Description
29	**GPI125**	GPIO125_DIN	GPIO 125 data input value
28	**GPI124**	GPIO124_DIN	GPIO 124 data input value
27	**GPI123**	GPIO123_DIN	GPIO 123 data input value
26	**GPI122**	GPIO122_DIN	GPIO 122 data input value
25	**GPI121**	GPIO121_DIN	GPIO 121 data input value
24	**GPI120**	GPIO120_DIN	GPIO 120 data input value
23	**GPI119**	GPIO119_DIN	GPIO 119 data input value
22	**GPI118**	GPIO118_DIN	GPIO 118 data input value
21	**GPI117**	GPIO117_DIN	GPIO 117 data input value
20	**GPI116**	GPIO116_DIN	GPIO 116 data input value
19	**GPI115**	GPIO115_DIN	GPIO 115 data input value
18	**GPI114**	GPIO114_DIN	GPIO 114 data input value
17	**GPI113**	GPIO113_DIN	GPIO 113 data input value
16	**GPI112**	GPIO112_DIN	GPIO 112 data input value
15	**GPI111**	GPIO111_DIN	GPIO 111 data input value
14	**GPI110**	GPIO110_DIN	GPIO 110 data input value
13	**GPI109**	GPIO109_DIN	GPIO 109 data input value
12	**GPI108**	GPIO108_DIN	GPIO 108 data input value
11	**GPI107**	GPIO107_DIN	GPIO 107 data input value
10	**GPI106**	GPIO106_DIN	GPIO 106 data input value
9	**GPI105**	GPIO105_DIN	GPIO 105 data input value
8	**GPI104**	GPIO104_DIN	GPIO 104 data input value
7	**GPI103**	GPIO103_DIN	GPIO 103 data input value
6	**GPI102**	GPIO102_DIN	GPIO 102 data input value
5	**GPI101**	GPIO101_DIN	GPIO 101 data input value
4	**GPI100**	GPIO100_DIN	GPIO 100 data input value
3	**GPI99**	GPIO99_DIN	GPIO 99 data input value
2	**GPI98**	GPIO98_DIN	GPIO 98 data input value
1	**GPI97**	GPIO97_DIN	GPIO 97 data input value
0	**GPI96**	GPIO96_DIN	GPIO 96 data input value

10211240 GPIO_DIN5 GPIO Data Input Register 5 NA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPI159	GPI158	GPI157	GPI156	GPI155	GPI154	GPI153	GPI152	GPI151	GPI150	GPI149	GPI148	GPI147	GPI146	GPI145	GPI144
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPI143	GPI142	GPI141	GPI140	GPI139	GPI138	GPI137	GPI136	GPI135	GPI134	GPI133	GPI132	GPI131	GPI130	GPI129	GPI128
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit(s)	Mnemonic	Name	Description
31	**GPI159**	GPIO159_DIN	GPIO 159 data input value
30	**GPI158**	GPIO158_DIN	GPIO 158 data input value

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Bit(s)	Mnemonic	Name	Description
29	**GPI157**	GPIO157_DIN	GPIO 157 data input value
28	**GPI156**	GPIO156_DIN	GPIO 156 data input value
27	**GPI155**	GPIO155_DIN	GPIO 155 data input value
26	**GPI154**	GPIO154_DIN	GPIO 154 data input value
25	**GPI153**	GPIO153_DIN	GPIO 153 data input value
24	**GPI152**	GPIO152_DIN	GPIO 152 data input value
23	**GPI151**	GPIO151_DIN	GPIO 151 data input value
22	**GPI150**	GPIO150_DIN	GPIO 150 data input value
21	**GPI149**	GPIO149_DIN	GPIO 149 data input value
20	**GPI148**	GPIO148_DIN	GPIO 148 data input value
19	**GPI147**	GPIO147_DIN	GPIO 147 data input value
18	**GPI146**	GPIO146_DIN	GPIO 146 data input value
17	**GPI145**	GPIO145_DIN	GPIO 145 data input value
16	**GPI144**	GPIO144_DIN	GPIO 144 data input value
15	**GPI143**	GPIO143_DIN	GPIO 143 data input value
14	**GPI142**	GPIO142_DIN	GPIO 142 data input value
13	**GPI141**	GPIO141_DIN	GPIO 141 data input value
12	**GPI140**	GPIO140_DIN	GPIO 140 data input value
11	**GPI139**	GPIO139_DIN	GPIO 139 data input value
10	**GPI138**	GPIO138_DIN	GPIO 138 data input value
9	**GPI137**	GPIO137_DIN	GPIO 137 data input value
8	**GPI136**	GPIO136_DIN	GPIO 136 data input value
7	**GPI135**	GPIO135_DIN	GPIO 135 data input value
6	**GPI134**	GPIO134_DIN	GPIO 134 data input value
5	**GPI133**	GPIO133_DIN	GPIO 133 data input value
4	**GPI132**	GPIO132_DIN	GPIO 132 data input value
3	**GPI131**	GPIO131_DIN	GPIO 131 data input value
2	**GPI130**	GPIO130_DIN	GPIO 130 data input value
1	**GPI129**	GPIO129_DIN	GPIO 129 data input value
0	**GPI128**	GPIO128_DIN	GPIO 128 data input value

10211250 **GPIO_DIN6** **GPIO Data Input Register 6** **NA**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPI191	GPI190	GPI189	GPI188	GPI187	GPI186	GPI185	GPI184	GPI183	GPI182	GPI181	GPI180	GPI179	GPI178	GPI177	GPI176
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPI175	GPI174	GPI173	GPI172	GPI171	GPI170	GPI169	GPI168	GPI167	GPI166	GPI165	GPI164	GPI163	GPI162	GPI161	GPI160
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit(s)	Mnemonic	Name	Description
31	**GPI191**	GPIO191_DIN	GPIO 191 data input value
30	**GPI190**	GPIO190_DIN	GPIO 190 data input value

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Bit(s)	Mnemonic	Name	Description
29	**GPI189**	GPIO189_DIN	GPIO 189 data input value
28	**GPI188**	GPIO188_DIN	GPIO 188 data input value
27	**GPI187**	GPIO187_DIN	GPIO 187 data input value
26	**GPI186**	GPIO186_DIN	GPIO 186 data input value
25	**GPI185**	GPIO185_DIN	GPIO 185 data input value
24	**GPI184**	GPIO184_DIN	GPIO 184 data input value
23	**GPI183**	GPIO183_DIN	GPIO 183 data input value
22	**GPI182**	GPIO182_DIN	GPIO 182 data input value
21	**GPI181**	GPIO181_DIN	GPIO 181 data input value
20	**GPI180**	GPIO180_DIN	GPIO 180 data input value
19	**GPI179**	GPIO179_DIN	GPIO 179 data input value
18	**GPI178**	GPIO178_DIN	GPIO 178 data input value
17	**GPI177**	GPIO177_DIN	GPIO 177 data input value
16	**GPI176**	GPIO176_DIN	GPIO 176 data input value
15	**GPI175**	GPIO175_DIN	GPIO 175 data input value
14	**GPI174**	GPIO174_DIN	GPIO 174 data input value
13	**GPI173**	GPIO173_DIN	GPIO 173 data input value
12	**GPI172**	GPIO172_DIN	GPIO 172 data input value
11	**GPI171**	GPIO171_DIN	GPIO 171 data input value
10	**GPI170**	GPIO170_DIN	GPIO 170 data input value
9	**GPI169**	GPIO169_DIN	GPIO 169 data input value
8	**GPI168**	GPIO168_DIN	GPIO 168 data input value
7	**GPI167**	GPIO167_DIN	GPIO 167 data input value
6	**GPI166**	GPIO166_DIN	GPIO 166 data input value
5	**GPI165**	GPIO165_DIN	GPIO 165 data input value
4	**GPI164**	GPIO164_DIN	GPIO 164 data input value
3	**GPI163**	GPIO163_DIN	GPIO 163 data input value
2	**GPI162**	GPIO162_DIN	GPIO 162 data input value
1	**GPI161**	GPIO161_DIN	GPIO 161 data input value
0	**GPI160**	GPIO160_DIN	GPIO 160 data input value

10211260 **GPIO_DIN7** **GPIO Data Input Register 7** **NA**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					GPI203	GPI202	GPI201	GPI200	GPI199	GPI198	GPI197	GPI196	GPI195	GPI194	GPI193	GPI192
Type					RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset					X	X	X	X	X	X	X	X	X	X	X	X

Bit(s)	Mnemonic	Name	Description
11	**GPI203**	GPIO203_DIN	GPIO 203 data input value
10	**GPI202**	GPIO202_DIN	GPIO 202 data input value
9	**GPI201**	GPIO201_DIN	GPIO 201 data input value

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Bit(s)	Mnemonic	Name	Description
8	**GPI200**	GPIO200_DIN	GPIO 200 data input value
7	**GPI199**	GPIO199_DIN	GPIO 199 data input value
6	**GPI198**	GPIO198_DIN	GPIO 198 data input value
5	**GPI197**	GPIO197_DIN	GPIO 197 data input value
4	**GPI196**	GPIO196_DIN	GPIO 196 data input value
3	**GPI195**	GPIO195_DIN	GPIO 195 data input value
2	**GPI194**	GPIO194_DIN	GPIO 194 data input value
1	**GPI193**	GPIO193_DIN	GPIO 193 data input value
0	**GPI192**	GPIO192_DIN	GPIO 192 data input value

10211300 GPIO_MODE1 GPIO Mode Control Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**GPIO9_M**			**GPIO8_M**			**GPIO7_M**			**GPIO6_M**			**GPIO5_M**		
Type		RW			RW			RW			RW			RW		
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**GPIO4_M**			**GPIO3_M**			**GPIO2_M**			**GPIO1_M**			**GPIO0_M**		
Type		RW			RW			RW			RW			RW		
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:28	**GPIO9_M**	GPIO9_MODE	**Selects GPIO 9 mode** 0: GPIO9 (IO) 1: C2K_UIM1_HOT_PLUG_IN (I) 2: PCM1_DO0 (O) 3: I2S3_MCK (O) 4: MD_EINT2 (I) 5: CLKM2 (O) 6: I2S1_MCK (O) 7: DBG_MON_A29 (IO)
27:25	**GPIO8_M**	GPIO8_MODE	**Selects GPIO 8 mode** 0: GPIO8 (IO) 1: URTS3 (O) 2: C2K_UIM0_HOT_PLUG_IN (I) 3: SCL1 (IO) 4: PCM1_DO1 (O) 5: MD_EINT1 (I) 6: KCOL4 (IO) 7: UTXD0 (O)
24:22	**GPIO7_M**	GPIO7_MODE	**Selects GPIO 7 mode** 0: GPIO7 (IO) 1: UCTS3 (I) 2: DPI_D11 (O) 3: SDA1 (IO) 4: TDD_TMS (I) 5: CONN_MCU_TMS (I) 6: I2S1_BCK (O) 7: TDD_TXD (O)
21:19	**GPIO6_M**	GPIO6_MODE	**Selects GPIO 6 mode** 0: GPIO6 (IO) 1: URTS2 (O) 2: DPI_D10 (O) 3: SPI_CKB (O)

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Bit(s)	Mnemonic	Name	Description
			4: TDD_TRSTN (I) 5: CONN_MCU_TRST_B (I) 6: I2S1_LRCK (O) 7: MD_UTXD (O)
18:16	**GPIO5_M**	GPIO5_MODE	**Selects GPIO 5 mode** 0: GPIO5 (IO) 1: UCTS2 (I) 2: DPI_D9 (O) 3: SPI_CSB (O) 4: TDD_TDI (I) 5: CONN_MCU_TDI (I) 6: I2S1_DO (O) 7: MD_URXD (I)
14:12	**GPIO4_M**	GPIO4_MODE	**Selects GPIO 4 mode** 0: GPIO4 (IO) 1: CLKM2 (O) 2: DPI_D8 (O) 3: SPI_MOB (O) 4: TDD_TCK (I) 5: CONN_MCU_TCK (I) 6: CONN_MCU_AICE_TCKC (I) 7: C2K_DM_EINT0 (IO)
11:9	**GPIO3_M**	GPIO3_MODE	**Selects GPIO 3 mode** 0: GPIO3 (IO) 1: CLKM1 (O) 2: DPI_D7 (O) 3: SPI_MIB (I) 4: MD_EINT0 (I) 5: CONN_MCU_DBGI_N (I) 6: CONN_MCU_AICE_TMSC (IO) 7: C2K_ARM_EINT3 (IO)
8:6	**GPIO2_M**	GPIO2_MODE	**Selects GPIO 2 mode** 0: GPIO2 (IO) 1: CLKM0 (O) 2: DPI_D6 (O) 3: MD_EINT0 (I) 4: USB_DRVVBUS (O) 5: CONN_MCU_DBGACK_N (O) 6: PTA_TXD (O) 7: C2K_ARM_EINT2 (IO)
5:3	**GPIO1_M**	GPIO1_MODE	**Selects GPIO 1 mode** 0: GPIO1 (IO) 1: PWM2 (O) 2: DPI_D5 (O) 3: MD_EINT0 (I) 4: TDD_TDO (IO) 5: CONN_MCU_TDO (O) 6: PTA_RXD (I) 7: C2K_ARM_EINT1 (IO)
2:0	**GPIO0_M**	GPIO0_MODE	**Selects GPIO 0 mode** 0: GPIO0 (IO) 1: IDDIG (I) 2: DPI_D4 (O) 3: Reserved 4: EXT_FRAME_SYNC (I) 5: PWM3 (O) 6: KCOL2 (IO) 7: C2K_ARM_EINT0 (IO)

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10211310 GPIO_MODE2 GPIO Mode Control Register 2 02491200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**GPIO19_M**			**GPIO18_M**			**GPIO17_M**			**GPIO16_M**			**GPIO15_M**		
Type		RW			RW			RW			RW			RW		
Reset		0	0	0	0	0	1	0	0	1	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**GPIO14_M**			**GPIO13_M**			**GPIO12_M**			**GPIO11_M**			**GPIO10_M**		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:28	**GPIO19_M**	GPIO19_MODE	**Selects GPIO 19 mode** 0: GPIO19 (IO) 1: ANT_SEL0 (O) 2: IRTX_OUT (O) 3: IRDA_TX (O) 4: C2K_UART0_TXD (O) 5: GPS_FRAME_SYNC (O) 6: LTE_UTXD (O) 7: DBG_MON_A6 (IO)
27:25	**GPIO18_M**	GPIO18_MODE	**Selects GPIO 18 mode** 0: GPIO18 (IO) 1: WB_CTRL5 (IO) 2: Reserved 3: C2K_DM_EINT1 (IO) 4: Reserved 5: Reserved 6: Reserved 7: DBG_MON_A5 (IO)
24:22	**GPIO17_M**	GPIO17_MODE	**Selects GPIO 17 mode** 0: GPIO17 (IO) 1: WB_CTRL4 (IO) 2: Reserved 3: C2K_DM_EINT0 (IO) 4: WATCHDOG (O) 5: Reserved 6: Reserved 7: DBG_MON_A4 (IO)
21:19	**GPIO16_M**	GPIO16_MODE	**Selects GPIO 16 mode** 0: GPIO16 (IO) 1: WB_CTRL3 (IO) 2: Reserved 3: C2K_ARM_EINT3 (IO) 4: Reserved 5: Reserved 6: Reserved 7: DBG_MON_A3 (IO)
18:16	**GPIO15_M**	GPIO15_MODE	**Selects GPIO 15 mode** 0: GPIO15 (IO) 1: WB_CTRL2 (IO) 2: Reserved 3: C2K_ARM_EINT2 (IO) 4: Reserved 5: Reserved 6: Reserved 7: DBG_MON_A2 (IO)
14:12	**GPIO14_M**	GPIO14_MODE	**Selects GPIO 14 mode** 0: GPIO14 (IO)

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Bit(s)	Mnemonic	Name	Description
			1: WB_CTRL1 (IO) 2: Reserved 3: C2K_ARM_EINT1 (IO) 4: Reserved 5: Reserved 6: Reserved 7: DBG_MON_A1 (IO)
11:9	**GPIO13_M**	GPIO13_MODE	**Selects GPIO 13 mode** 0: GPIO13 (IO) 1: WB_CTRL0 (IO) 2: Reserved 3: C2K_ARM_EINT0 (IO) 4: Reserved 5: Reserved 6: Reserved 7: DBG_MON_A0 (IO)
8:6	**GPIO12_M**	GPIO12_MODE	**Selects GPIO 12 mode** 0: GPIO12 (IO) 1: I2S0_MCK (O) 2: C2K_UIM1_HOT_PLUG_IN (I) 3: KCOL2 (IO) 4: MD_EINT2 (I) 5: IRTX_OUT (O) 6: SRCLKENAI2 (I) 7: PCM1_DO1 (O)
5:3	**GPIO11_M**	GPIO11_MODE	**Selects GPIO 11 mode** 0: GPIO11 (IO) 1: MD_EINT1 (I) 2: IRTX_OUT (O) 3: C2K_UIM0_HOT_PLUG_IN (I) 4: CLKM0 (O) 5: I2S2_MCK (O) 6: SCL3 (IO) 7: URXD0 (I)
2:0	**GPIO10_M**	GPIO10_MODE	**Selects GPIO 10 mode** 0: GPIO10 (IO) 1: PWM1 (O) 2: CLKM1 (O) 3: KROW2 (IO) 4: MD_EINT0 (I) 5: I2S1_MCK (O) 6: SDA3 (IO) 7: DBG_MON_A30 (IO)

10211320 **GPIO_MODE3 GPIO Mode Control Register 3** **12491240**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**GPIO29_M**			**GPIO28_M**			**GPIO27_M**			**GPIO26_M**			**GPIO25_M**		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	1	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**GPIO24_M**			**GPIO23_M**			**GPIO22_M**			**GPIO21_M**			**GPIO20_M**		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	1	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:28	**GPIO29_M**	GPIO29_MODE	**Selects GPIO 29 mode**

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Bit(s)	Mnemonic	Name	Description
			0: GPIO29 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
27:25	**GPIO28_M**	GPIO28_MODE	**Selects GPIO 28 mode** 0: GPIO28 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
24:22	**GPIO27_M**	GPIO27_MODE	**Selects GPIO 27 mode** 0: GPIO27 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
21:19	**GPIO26_M**	GPIO26_MODE	**Selects GPIO 26 mode** 0: GPIO26 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
18:16	**GPIO25_M**	GPIO25_MODE	**Selects GPIO 25 mode** 0: GPIO25 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
14:12	**GPIO24_M**	GPIO24_MODE	**Selects GPIO 24 mode** 0: GPIO24 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
11:9	**GPIO23_M**	GPIO23_MODE	**Selects GPIO 23 mode** 0: GPIO23 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved

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Bit(s)	Mnemonic	Name	Description
			6: Reserved 7: Reserved
8:6	**GPIO22_M**	GPIO22_MODE	**Selects GPIO 22 mode** 0: GPIO22 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
5:3	**GPIO21_M**	GPIO21_MODE	**Selects GPIO 21 mode** 0: GPIO21 (IO) 1: ANT_SEL2 (O) 2: PWM2 (O) 3: IRDA_PDN (O) 4: CORESONIC_SWCK (I) 5: MD_EINT1 (I) 6: C2K_UIM0_HOT_PLUG_IN (I) 7: DBG_MON_A8 (IO)
2:0	**GPIO20_M**	GPIO20_MODE	**Selects GPIO 20 mode** 0: GPIO20 (IO) 1: ANT_SEL1 (O) 2: C2K_UIM1_HOT_PLUG_IN (I) 3: IRDA_RX (I) 4: C2K_UART0_RXD (I) 5: MD_EINT2 (I) 6: LTE_URXD (I) 7: DBG_MON_A7 (IO)

10211330 GPIO_MODE4 GPIO Mode Control Register 4 12491249

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO39_M			GPIO38_M			GPIO37_M			GPIO36_M			GPIO35_M		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	1	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO34_M			GPIO33_M			GPIO32_M			GPIO31_M			GPIO30_M		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	1	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
30:28	**GPIO39_M**	GPIO39_MODE	**Selects GPIO 39 mode** 0: GPIO39 (IO) 1: Reserved 2: CMDAT4 (I) 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
27:25	**GPIO38_M**	GPIO38_MODE	**Selects GPIO 38 mode** 0: GPIO38 (IO) 1: Reserved 2: CMDAT5 (I) 3: Reserved 4: Reserved

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Bit(s)	Mnemonic	Name	Description
			5: Reserved 6: Reserved 7: Reserved
24:22	**GPIO37_M**	GPIO37_MODE	**Selects GPIO 37 mode** 0: GPIO37 (IO) 1: Reserved 2: CMDAT6 (I) 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
21:19	**GPIO36_M**	GPIO36_MODE	**Selects GPIO 36 mode** 0: GPIO36 (IO) 1: Reserved 2: CMDAT7 (I) 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
18:16	**GPIO35_M**	GPIO35_MODE	**Selects GPIO 35 mode** 0: GPIO35 (IO) 1: Reserved 2: CMDAT8 (I) 3: CMCSD3 (I) 4: Reserved 5: Reserved 6: Reserved 7: Reserved
14:12	**GPIO34_M**	GPIO34_MODE	**Selects GPIO 34 mode** 0: GPIO34 (IO) 1: Reserved 2: CMDAT9 (I) 3: CMCSD2 (I) 4: Reserved 5: Reserved 6: Reserved 7: Reserved
11:9	**GPIO33_M**	GPIO33_MODE	**Selects GPIO 33 mode** 0: GPIO33 (IO) 1: Reserved 2: CMVSYNC (I) 3: CMCSD1 (I) 4: Reserved 5: Reserved 6: Reserved 7: Reserved
8:6	**GPIO32_M**	GPIO32_MODE	**Selects GPIO 32 mode** 0: GPIO32 (IO) 1: Reserved 2: CMHSYNC (I) 3: CMCSD0 (I) 4: Reserved 5: Reserved 6: Reserved 7: Reserved
5:3	**GPIO31_M**	GPIO31_MODE	**Selects GPIO 31 mode** 0: GPIO31 (IO)

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Bit(s)	Mnemonic	Name	Description
			1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
2:0	**GPIO30_M**	GPIO30_MODE	**Selects GPIO 30 mode** 0: GPIO30 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved

10211340 GPIO_MODE5 GPIO Mode Control Register 5 12490009

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**GPIO49_M**			**GPIO48_M**			**GPIO47_M**			**GPIO46_M**			**GPIO45_M**		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	1	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**GPIO44_M**			**GPIO43_M**			**GPIO42_M**			**GPIO41_M**			**GPIO40_M**		
Type		RW			RW			RW			RW			RW		
Reset		0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
30:28	**GPIO49_M**	GPIO49_MODE	**Selects GPIO 49 mode** 0: GPIO49 (IO) 1: SDA1 (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
27:25	**GPIO48_M**	GPIO48_MODE	**Selects GPIO 48 mode** 0: GPIO48 (IO) 1: SCL0 (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
24:22	**GPIO47_M**	GPIO47_MODE	**Selects GPIO 47 mode** 0: GPIO47 (IO) 1: SDA0 (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
21:19	**GPIO46_M**	GPIO46_MODE	**Selects GPIO 46 mode**

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Bit(s)	Mnemonic	Name	Description
			0: GPIO46 (IO) 1: CMMCLK1 (O) 2: IDDIG (I) 3: LTE_MD32_JTAG_TRST (I) 4: TDD_TRSTN (I) 5: DM_JTINTP (O) 6: KCOL6 (IO) 7: DBG_MON_A13 (IO)
18:16	**GPIO45_M**	GPIO45_MODE	**Selects GPIO 45 mode** 0: GPIO45 (IO) 1: CMMCLK0 (O) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: DBG_MON_A12 (IO)
14:12	**GPIO44_M**	GPIO44_MODE	**Selects GPIO 44 mode** 0: GPIO44 (IO) 1: CMPCLK (I) 2: CMCSK (I) 3: CMCSD2 (I) 4: KCOL3 (IO) 5: SRCLKENAI2 (I) 6: PWM0 (O) 7: DBG_MON_A11 (IO)
11:9	**GPIO43_M**	GPIO43_MODE	**Selects GPIO 43 mode** 0: GPIO43 (IO) 1: CMDAT1 (I) 2: CMCSD1 (I) 3: CMFLASH (O) 4: MD_EINT0 (I) 5: CMMCLK1 (O) 6: Reserved 7: DBG_MON_A10 (IO)
8:6	**GPIO42_M**	GPIO42_MODE	**Selects GPIO 42 mode** 0: GPIO42 (IO) 1: CMDAT0 (I) 2: CMCSD0 (I) 3: CMMCLK1 (O) 4: Reserved 5: ANT_SEL5 (O) 6: Reserved 7: DBG_MON_A9 (IO)
5:3	**GPIO41_M**	GPIO41_MODE	**Selects GPIO 41 mode** 0: GPIO41 (IO) 1: Reserved 2: CMDAT2 (I) 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
2:0	**GPIO40_M**	GPIO40_MODE	**Selects GPIO 40 mode** 0: GPIO40 (IO) 1: Reserved 2: CMDAT3 (I) 3: Reserved 4: Reserved

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Bit(s)	Mnemonic	Name	Description
			5: Reserved 6: Reserved 7: Reserved

10211350 **GPIO_MODE6 GPIO Mode Control Register 6** **00090049**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**GPIO59_M**			**GPIO58_M**			**GPIO57_M**			**GPIO56_M**			**GPIO55_M**		
Type		RW			RW			RW			RW			RW		
Reset		0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**GPIO54_M**			**GPIO53_M**			**GPIO52_M**			**GPIO51_M**			**GPIO50_M**		
Type		RW			RW			RW			RW			RW		
Reset		0	0	0	0	0	0	0	0	1	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
30:28	**GPIO59_M**	GPIO59_MODE	**Selects GPIO 59 mode** 0: GPIO59 (IO) 1: URXD3 (I) 2: DPI_CK0 (O) 3: UTXD3 (O) 4: UCTS2 (I) 5: PWM3 (O) 6: KROW6 (IO) 7: DBG_MON_A16 (IO)
27:25	**GPIO58_M**	GPIO58_MODE	**Selects GPIO 58 mode** 0: GPIO58 (IO) 1: UTXD2 (O) 2: DPI_VSYNC0 (O) 3: URXD2 (I) 4: MD_UTXD (O) 5: TDD_TXD (O) 6: KROW5 (IO) 7: DBG_MON_A15 (IO)
24:22	**GPIO57_M**	GPIO57_MODE	**Selects GPIO 57 mode** 0: GPIO57 (IO) 1: URXD2 (I) 2: DPI_HSYNC0 (O) 3: UTXD2 (O) 4: MD_URXD (I) 5: SRCLKENAI1 (I) 6: KROW4 (IO) 7: DBG_MON_A14 (IO)
21:19	**GPIO56_M**	GPIO56_MODE	**Selects GPIO 56 mode** 0: GPIO56 (IO) 1: SRCLKENA1 (O) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
18:16	**GPIO55_M**	GPIO55_MODE	**Selects GPIO 55 mode** 0: GPIO55 (IO) 1: SRCLKENAI0 (I) 2: PWM2 (O) 3: Reserved

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Bit(s)	Mnemonic	Name	Description
			4: CORESONIC_SWD (IO) 5: ANT_SEL6 (O) 6: KROW5 (IO) 7: DISP_PWM (O)
14:12	**GPIO54_M**	GPIO54_MODE	**Selects GPIO 54 mode** 0: GPIO54 (IO) 1: SCL3 (IO) 2: Reserved 3: IDDIG (I) 4: Reserved 5: MD_EINT1 (I) 6: C2K_UIM0_HOT_PLUG_IN (I) 7: Reserved
11:9	**GPIO53_M**	GPIO53_MODE	**Selects GPIO 53 mode** 0: GPIO53 (IO) 1: SDA3 (IO) 2: Reserved 3: IDDIG (I) 4: Reserved 5: MD_EINT2 (I) 6: C2K_UIM1_HOT_PLUG_IN (I) 7: Reserved
8:6	**GPIO52_M**	GPIO52_MODE	**Selects GPIO 52 mode** 0: GPIO52 (IO) 1: SCL2 (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
5:3	**GPIO51_M**	GPIO51_MODE	**Selects GPIO 51 mode** 0: GPIO51 (IO) 1: SDA2 (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
2:0	**GPIO50_M**	GPIO50_MODE	**Selects GPIO 50 mode** 0: GPIO50 (IO) 1: SCL1 (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved

10211360 GPIO_MODE7 GPIO Mode Control Register 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO69_M			GPIO68_M			GPIO67_M			GPIO66_M			GPIO65_M		
Type		RW			RW			RW			RW			RW		
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO64_M			GPIO63_M			GPIO62_M			GPIO61_M			GPIO60_M		

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Type		RW			RW			RW			RW			RW		
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:28	**GPIO69_M**	GPIO69_MODE	**Selects GPIO 69 mode** 0: GPIO69 (IO) 1: DISP_PWM (O) 2: PWM1 (O) 3: LTE_MD32_JTAG_TRST (I) 4: TDD_TRSTN (I) 5: ANT_SEL7 (O) 6: DM_JTINTP (O) 7: Reserved
27:25	**GPIO68_M**	GPIO68_MODE	**Selects GPIO 68 mode** 0: GPIO68 (IO) 1: SPI_MOA (O) 2: SPI_MIA (I) 3: I2S3_LRCK (O) 4: PTA_TXD (O) 5: ANT_SEL4 (O) 6: URTS1 (O) 7: DBG_MON_A25 (IO)
24:22	**GPIO67_M**	GPIO67_MODE	**Selects GPIO 67 mode** 0: GPIO67 (IO) 1: SPI_MIA (I) 2: SPI_MOA (O) 3: I2S3_DO (O) 4: PTA_RXD (I) 5: IDDIG (I) 6: UCTS1 (I) 7: DBG_MON_A24 (IO)
21:19	**GPIO66_M**	GPIO66_MODE	**Selects GPIO 66 mode** 0: GPIO66 (IO) 1: SPI_CKA (O) 2: USB_DRVVBUS (O) 3: I2S3_BCK (O) 4: KCOL2 (IO) 5: Reserved 6: PTA_TXD (O) 7: DBG_MON_A23 (IO)
18:16	**GPIO65_M**	GPIO65_MODE	**Selects GPIO 65 mode** 0: GPIO65 (IO) 1: SPI_CSA (O) 2: EXT_FRAME_SYNC (I) 3: I2S3_MCK (O) 4: KROW2 (IO) 5: GPS_FRAME_SYNC (O) 6: PTA_RXD (I) 7: DBG_MON_A22 (IO)
14:12	**GPIO64_M**	GPIO64_MODE	**Selects GPIO 64 mode** 0: GPIO64 (IO) 1: PCM1_DO0 (O) 2: DPI_D3 (O) 3: I2S0_MCK (O) 4: PCM1_DI (I) 5: SRCLKENAI2 (I) 6: KCOL5 (IO) 7: DBG_MON_A21 (IO)
11:9	**GPIO63_M**	GPIO63_MODE	**Selects GPIO 63 mode** 0: GPIO63 (IO)

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Bit(s)	Mnemonic	Name	Description
			1: PCM1_DI (I) 2: DPI_D2 (O) 3: I2S0_DI (I) 4: PCM1_DO0 (O) 5: Reserved 6: KROW3 (IO) 7: DBG_MON_A20 (IO)
8:6	**GPIO62_M**	GPIO62_MODE	**Selects GPIO 62 mode** 0: GPIO62 (IO) 1: PCM1_SYNC (IO) 2: DPI_D1 (O) 3: I2S0_LRCK (IO) 4: KCOL7 (IO) 5: CLKM3 (O) 6: CMFLASH (O) 7: DBG_MON_A19 (IO)
5:3	**GPIO61_M**	GPIO61_MODE	**Selects GPIO 61 mode** 0: GPIO61 (IO) 1: PCM1_CLK (IO) 2: DPI_D0 (O) 3: I2S0_BCK (IO) 4: KROW4 (IO) 5: ANT_SEL3 (O) 6: IRTX_OUT (O) 7: DBG_MON_A18 (IO)
2:0	**GPIO60_M**	GPIO60_MODE	**Selects GPIO 60 mode** 0: GPIO60 (IO) 1: UTXD3 (O) 2: DPI_DE0 (O) 3: URXD3 (I) 4: URTS2 (O) 5: PWM4 (O) 6: KROW7 (IO) 7: DBG_MON_A17 (IO)

10211370 GPIO_MODE8 GPIO Mode Control Register 8 00011249

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO79_M			GPIO78_M			GPIO77_M			GPIO76_M			GPIO75_M		
Type		RW			RW			RW			RW			RW		
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO74_M			GPIO73_M			GPIO72_M			GPIO71_M			GPIO70_M		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	1	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
30:28	**GPIO79_M**	GPIO79_MODE	**Selects GPIO 79 mode** 0: GPIO79 (IO) 1: I2S0_LRCK (IO) 2: PCM1_SYNC (IO) 3: I2S3_LRCK (O) 4: I2S1_LRCK (O) 5: PWM3 (O) 6: I2S2_LRCK (O) 7: DBG_MON_A27 (IO)
27:25	**GPIO78_M**	GPIO78_MODE	**Selects GPIO 78 mode**

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Bit(s)	Mnemonic	Name	Description
			0: GPIO78 (IO) 1: I2S0_DI (I) 2: PCM1_DI (I) 3: I2S3_DO (O) 4: I2S1_DO (O) 5: PWM0 (O) 6: I2S2_DI (I) 7: DBG_MON_A26 (IO)
24:22	**GPIO77_M**	GPIO77_MODE	**Selects GPIO 77 mode** 0: GPIO77 (IO) 1: UTXD1 (O) 2: URXD1 (I) 3: MD_UTXD (O) 4: TDD_TXD (O) 5: LTE_UTXD (O) 6: C2K_UART0_TXD (O) 7: Reserved
21:19	**GPIO76_M**	GPIO76_MODE	**Selects GPIO 76 mode** 0: GPIO76 (IO) 1: URXD1 (I) 2: UTXD1 (O) 3: MD_URXD (I) 4: SCL3 (IO) 5: LTE_URXD (I) 6: C2K_UART0_RXD (I) 7: AUXIF_CLK (O)
18:16	**GPIO75_M**	GPIO75_MODE	**Selects GPIO 75 mode** 0: GPIO75 (IO) 1: UTXD0 (O) 2: URXD0 (I) 3: MD_UTXD (O) 4: TDD_TXD (O) 5: C2K_UART0_TXD (O) 6: LTE_UTXD (O) 7: Reserved
14:12	**GPIO74_M**	GPIO74_MODE	**Selects GPIO 74 mode** 0: GPIO74 (IO) 1: URXD0 (I) 2: UTXD0 (O) 3: MD_URXD (I) 4: SDA3 (IO) 5: C2K_UART0_RXD (I) 6: LTE_URXD (I) 7: AUXIF_ST (O)
11:9	**GPIO73_M**	GPIO73_MODE	**Selects GPIO 73 mode** 0: GPIO73 (IO) 1: JTDO (O) 2: CONN_MCU_TDO (O) 3: LTE_MD32_JTAG_TDO (IO) 4: TDD_TDO (IO) 5: Reserved 6: DM_OTDO (IO) 7: DFD_TDO (O)
8:6	**GPIO72_M**	GPIO72_MODE	**Selects GPIO 72 mode** 0: GPIO72 (IO) 1: JTDI (I) 2: CONN_MCU_TDI (I) 3: LTE_MD32_JTAG_TDI (I) 4: TDD_TDI (I) 5: Reserved

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Bit(s)	Mnemonic	Name	Description
			6: DM_OTDI (I) 7: DFD_TDI (I)
5:3	**GPIO71_M**	GPIO71_MODE	**Selects GPIO 71 mode** 0: GPIO71 (IO) 1: JTCK (I) 2: CONN_MCU_TCK (I) 3: LTE_MD32_JTAG_TCK (I) 4: TDD_TCK (I) 5: CORESONIC_SWCK (I) 6: DM_OTCK (I) 7: DFD_TCK_XI (I)
2:0	**GPIO70_M**	GPIO70_MODE	**Selects GPIO 70 mode** 0: GPIO70 (IO) 1: JTMS (IO) 2: CONN_MCU_TMS (I) 3: LTE_MD32_JTAG_TMS (I) 4: TDD_TMS (I) 5: CORESONIC_SWD (IO) 6: DM_OTMS (I) 7: DFD_TMS (I)

10211380 GPIO_MODE9 GPIO Mode Control Register 9 12401008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**GPIO89_M**			**GPIO88_M**			**GPIO87_M**			**GPIO86_M**			**GPIO85_M**		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**GPIO84_M**			**GPIO83_M**			**GPIO82_M**			**GPIO81_M**			**GPIO80_M**		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	0	0	0	0	0	0	1	0	0	0

Bit(s)	Mnemonic	Name	Description
30:28	**GPIO89_M**	GPIO89_MODE	**Selects GPIO 89 mode** 0: GPIO89 (IO) 1: BPI_BUS7 (O) 2: LTE_C2K_BPI_BUS7 (O) 3: CLKM0 (O) 4: Reserved 5: C2K_BPI_BUS7 (O) 6: Reserved 7: DBG_MON_B2 (IO)
27:25	**GPIO88_M**	GPIO88_MODE	**Selects GPIO 88 mode** 0: GPIO88 (IO) 1: BPI_BUS6 (O) 2: LTE_C2K_BPI_BUS6 (O) 3: Reserved 4: Reserved 5: C2K_BPI_BUS6 (O) 6: Reserved 7: DBG_MON_B1 (IO)
24:22	**GPIO87_M**	GPIO87_MODE	**Selects GPIO 87 mode** 0: GPIO87 (IO) 1: BPI_BUS5 (O) 2: LTE_C2K_BPI_BUS5 (O) 3: Reserved 4: Reserved

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Bit(s)	Mnemonic	Name	Description
			5: C2K_BPI_BUS5 (O) 6: Reserved 7: DBG_MON_B0 (IO)
21:19	**GPIO86_M**	GPIO86_MODE	**Selects GPIO 86 mode** 0: GPIO86 (IO) 1: KCOL2 (IO) 2: Reserved 3: URTS1 (O) 4: Reserved 5: C2K_RTCK (O) 6: Reserved 7: DBG_MON_A32 (IO)
18:16	**GPIO85_M**	GPIO85_MODE	**Selects GPIO 85 mode** 0: GPIO85 (IO) 1: KCOL1 (IO) 2: UCTS0 (I) 3: UCTS1 (I) 4: SDA2 (IO) 5: C2K_TMS (I) 6: AUXIF_ST (O) 7: DBG_MON_A31 (IO)
14:12	**GPIO84_M**	GPIO84_MODE	**Selects GPIO 84 mode** 0: GPIO84 (IO) 1: KCOL0 (IO) 2: URTS0 (O) 3: CONN_MCU_DBGACK_N (O) 4: SCL2 (IO) 5: C2K_TDO (IO) 6: AUXIF_CLK (O) 7: Reserved
11:9	**GPIO83_M**	GPIO83_MODE	**Selects GPIO 83 mode** 0: GPIO83 (IO) 1: KROW2 (IO) 2: USB_DRVVBUS (O) 3: Reserved 4: Reserved 5: C2K_TDI (I) 6: Reserved 7: C2K_DM_EINT3 (IO)
8:6	**GPIO82_M**	GPIO82_MODE	**Selects GPIO 82 mode** 0: GPIO82 (IO) 1: KROW1 (IO) 2: Reserved 3: CONN_MCU_TRST_B (I) 4: CORESONIC_SWD (IO) 5: C2K_NTRST (I) 6: USB_DRVVBUS (O) 7: C2K_DM_EINT2 (IO)
5:3	**GPIO81_M**	GPIO81_MODE	**Selects GPIO 81 mode** 0: GPIO81 (IO) 1: KROW0 (IO) 2: Reserved 3: CONN_MCU_DBGI_N (I) 4: CORESONIC_SWCK (I) 5: C2K_TCK (I) 6: Reserved 7: C2K_DM_EINT1 (IO)
2:0	**GPIO80_M**	GPIO80_MODE	**Selects GPIO 80 mode** 0: GPIO80 (IO)

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Bit(s)	Mnemonic	Name	Description
			1: I2S0_BCK (IO) 2: PCM1_CLK (IO) 3: I2S3_BCK (O) 4: I2S1_BCK (O) 5: PWM4 (O) 6: I2S2_BCK (O) 7: DBG_MON_A28 (IO)

10211390 **GPIO_MODE10** **GPIO Mode Control Register 10** **12491249**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**GPIO99_M**			**GPIO98_M**			**GPIO97_M**			**GPIO96_M**			**GPIO95_M**		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	1	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**GPIO94_M**			**GPIO93_M**			**GPIO92_M**			**GPIO91_M**			**GPIO90_M**		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	1	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
30:28	**GPIO99_M**	GPIO99_MODE	**Selects GPIO 99 mode** 0: GPIO99 (IO) 1: BPI_BUS17 (O) 2: LTE_C2K_BPI_BUS17 (O) 3: Reserved 4: Reserved 5: C2K_BPI_BUS17 (O) 6: Reserved 7: DBG_MON_B12 (IO)
27:25	**GPIO98_M**	GPIO98_MODE	**Selects GPIO 98 mode** 0: GPIO98 (IO) 1: BPI_BUS16 (O) 2: LTE_C2K_BPI_BUS16 (O) 3: Reserved 4: Reserved 5: C2K_BPI_BUS16 (O) 6: Reserved 7: DBG_MON_B11 (IO)
24:22	**GPIO97_M**	GPIO97_MODE	**Selects GPIO 97 mode** 0: GPIO97 (IO) 1: BPI_BUS15 (O) 2: LTE_C2K_BPI_BUS15 (O) 3: Reserved 4: Reserved 5: C2K_BPI_BUS15 (O) 6: Reserved 7: DBG_MON_B10 (IO)
21:19	**GPIO96_M**	GPIO96_MODE	**Selects GPIO 96 mode** 0: GPIO96 (IO) 1: BPI_BUS14 (O) 2: LTE_C2K_BPI_BUS14 (O) 3: Reserved 4: Reserved 5: C2K_BPI_BUS14 (O) 6: Reserved 7: DBG_MON_B9 (IO)

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Bit(s)	Mnemonic	Name	Description
18:16	**GPIO95_M**	GPIO95_MODE	**Selects GPIO 95 mode** 0: GPIO95 (IO) 1: BPI_BUS13 (O) 2: LTE_C2K_BPI_BUS13 (O) 3: Reserved 4: Reserved 5: C2K_BPI_BUS13 (O) 6: Reserved 7: DBG_MON_B8 (IO)
14:12	**GPIO94_M**	GPIO94_MODE	**Selects GPIO 94 mode** 0: GPIO94 (IO) 1: BPI_BUS12 (O) 2: LTE_C2K_BPI_BUS12 (O) 3: Reserved 4: Reserved 5: C2K_BPI_BUS12 (O) 6: Reserved 7: DBG_MON_B7 (IO)
11:9	**GPIO93_M**	GPIO93_MODE	**Selects GPIO 93 mode** 0: GPIO93 (IO) 1: BPI_BUS11 (O) 2: LTE_C2K_BPI_BUS11 (O) 3: Reserved 4: Reserved 5: C2K_BPI_BUS11 (O) 6: Reserved 7: DBG_MON_B6 (IO)
8:6	**GPIO92_M**	GPIO92_MODE	**Selects GPIO 92 mode** 0: GPIO92 (IO) 1: BPI_BUS10 (O) 2: LTE_C2K_BPI_BUS10 (O) 3: CLKM3 (O) 4: Reserved 5: C2K_BPI_BUS10 (O) 6: Reserved 7: DBG_MON_B5 (IO)
5:3	**GPIO91_M**	GPIO91_MODE	**Selects GPIO 91 mode** 0: GPIO91 (IO) 1: BPI_BUS9 (O) 2: LTE_C2K_BPI_BUS9 (O) 3: CLKM2 (O) 4: Reserved 5: C2K_BPI_BUS9 (O) 6: Reserved 7: DBG_MON_B4 (IO)
2:0	**GPIO90_M**	GPIO90_MODE	**Selects GPIO 90 mode** 0: GPIO90 (IO) 1: BPI_BUS8 (O) 2: LTE_C2K_BPI_BUS8 (O) 3: CLKM1 (O) 4: Reserved 5: C2K_BPI_BUS8 (O) 6: Reserved 7: DBG_MON_B3 (IO)

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102113A0 **GPIO_MODE11** **GPIO Mode Control Register 11** **5B6D5249**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**GPIO109_M**			**GPIO108_M**			**GPIO107_M**			**GPIO106_M**			**GPIO105_M**		
Type		RW			RW			RW			RW			RW		
Reset		1	0	1	1	0	1	1	0	1	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**GPIO104_M**			**GPIO103_M**			**GPIO102_M**			**GPIO101_M**			**GPIO100_M**		
Type		RW			RW			RW			RW			RW		
Reset		1	0	1	0	0	1	0	0	1	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
30:28	**GPIO109_M**	GPIO109_MODE	**Selects GPIO 109 mode** 0: GPIO109 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: C2K_TX_BSI_DATA (IO) 6: Reserved 7: DBG_MON_B22 (IO)
27:25	**GPIO108_M**	GPIO108_MODE	**Selects GPIO 108 mode** 0: GPIO108 (IO) 1: RFIC1_BSI_D2 (IO) 2: Reserved 3: Reserved 4: Reserved 5: C2K_TX_BSI_CLK (O) 6: Reserved 7: DBG_MON_B21 (IO)
24:22	**GPIO107_M**	GPIO107_MODE	**Selects GPIO 107 mode** 0: GPIO107 (IO) 1: RFIC1_BSI_D1 (IO) 2: Reserved 3: Reserved 4: Reserved 5: C2K_TX_BSI_EN (O) 6: Reserved 7: DBG_MON_B20 (IO)
21:19	**GPIO106_M**	GPIO106_MODE	**Selects GPIO 106 mode** 0: GPIO106 (IO) 1: RFIC1_BSI_D0 (IO) 2: Reserved 3: Reserved 4: Reserved 5: C2K_RX_BSI_DATA (IO) 6: Reserved 7: DBG_MON_B19 (IO)
18:16	**GPIO105_M**	GPIO105_MODE	**Selects GPIO 105 mode** 0: GPIO105 (IO) 1: RFIC1_BSI_CK (O) 2: Reserved 3: Reserved 4: Reserved 5: C2K_RX_BSI_CLK (O) 6: Reserved 7: DBG_MON_B18 (IO)
14:12	**GPIO104_M**	GPIO104_MODE	**Selects GPIO 104 mode** 0: GPIO104 (IO) 1: RFIC1_BSI_EN (O) 2: Reserved

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Bit(s)	Mnemonic	Name	Description
			3: Reserved 4: Reserved 5: C2K_RX_BSI_EN (O) 6: Reserved 7: DBG_MON_B17 (IO)
11:9	**GPIO103_M**	GPIO103_MODE	**Selects GPIO 103 mode** 0: GPIO103 (IO) 1: C2K_TXBPI (I) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: DBG_MON_B16 (IO)
8:6	**GPIO102_M**	GPIO102_MODE	**Selects GPIO 102 mode** 0: GPIO102 (IO) 1: BPI_BUS20 (O) 2: LTE_C2K_BPI_BUS20 (O) 3: Reserved 4: Reserved 5: C2K_BPI_BUS20 (O) 6: Reserved 7: DBG_MON_B15 (IO)
5:3	**GPIO101_M**	GPIO101_MODE	**Selects GPIO 101 mode** 0: GPIO101 (IO) 1: BPI_BUS19 (O) 2: LTE_C2K_BPI_BUS19 (O) 3: Reserved 4: Reserved 5: C2K_BPI_BUS19 (O) 6: Reserved 7: DBG_MON_B14 (IO)
2:0	**GPIO100_M**	GPIO100_MODE	**Selects GPIO 100 mode** 0: GPIO100 (IO) 1: BPI_BUS18 (O) 2: LTE_C2K_BPI_BUS18 (O) 3: Reserved 4: Reserved 5: C2K_BPI_BUS18 (O) 6: Reserved 7: DBG_MON_B13 (IO)

102113B0 **GPIO_MODE12** **GPIO Mode Control Register 12** **12491249**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**GPIO119_M**			**GPIO118_M**			**GPIO117_M**			**GPIO116_M**			**GPIO115_M**		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	1	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**GPIO114_M**			**GPIO113_M**			**GPIO112_M**			**GPIO111_M**			**GPIO110_M**		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	1	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
30:28	**GPIO119_M**	GPIO119_MODE	**Selects GPIO 119 mode** 0: GPIO119 (IO)

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Bit(s)	Mnemonic	Name	Description
			1: BPI_BUS0 (O) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: DBG_MON_B28 (IO)
27:25	**GPIO118_M**	GPIO118_MODE	**Selects GPIO 118 mode** 0: GPIO118 (IO) 1: TXBPI (I) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
24:22	**GPIO117_M**	GPIO117_MODE	**Selects GPIO 117 mode** 0: GPIO117 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
21:19	**GPIO116_M**	GPIO116_MODE	**Selects GPIO 116 mode** 0: GPIO116 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
18:16	**GPIO115_M**	GPIO115_MODE	**Selects GPIO 115 mode** 0: GPIO115 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
14:12	**GPIO114_M**	GPIO114_MODE	**Selects GPIO 114 mode** 0: GPIO114 (IO) 1: RFIC0_BSI_D0 (IO) 2: Reserved 3: Reserved 4: SPM_BSI_D0 (O) 5: Reserved 6: Reserved 7: DBG_MON_B27 (IO)
11:9	**GPIO113_M**	GPIO113_MODE	**Selects GPIO 113 mode** 0: GPIO113 (IO) 1: RFIC0_BSI_D1 (IO) 2: Reserved 3: Reserved 4: SPM_BSI_D1 (O) 5: Reserved 6: Reserved

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Bit(s)	Mnemonic	Name	Description
			7: DBG_MON_B26 (IO)
8:6	**GPIO112_M**	GPIO112_MODE	**Selects GPIO 112 mode** 0: GPIO112 (IO) 1: RFIC0_BSI_D2 (IO) 2: Reserved 3: Reserved 4: SPM_BSI_D2 (O) 5: Reserved 6: Reserved 7: DBG_MON_B25 (IO)
5:3	**GPIO111_M**	GPIO111_MODE	**Selects GPIO 111 mode** 0: GPIO111 (IO) 1: RFIC0_BSI_CK (O) 2: Reserved 3: Reserved 4: SPM_BSI_CLK (O) 5: Reserved 6: Reserved 7: DBG_MON_B24 (IO)
2:0	**GPIO110_M**	GPIO110_MODE	**Selects GPIO 110 mode** 0: GPIO110 (IO) 1: RFIC0_BSI_EN (O) 2: Reserved 3: Reserved 4: SPM_BSI_EN (O) 5: Reserved 6: Reserved 7: DBG_MON_B23 (IO)

102113C0 **GPIO_MODE13** **GPIO Mode Control Register 13** **12491249**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO129_M			GPIO128_M			GPIO127_M			GPIO126_M			GPIO125_M		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	1	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO124_M			GPIO123_M			GPIO122_M			GPIO121_M			GPIO120_M		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	1	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
30:28	**GPIO129_M**	GPIO129_MODE	**Selects GPIO 129 mode** 0: GPIO129 (IO) 1: BPI_BUS26 (O) 2: DISP_PWM (O) 3: Reserved 4: Reserved 5: I2S2_LRCK (O) 6: PTA_TXD (O) 7: LTE_URXD (I)
27:25	**GPIO128_M**	GPIO128_MODE	**Selects GPIO 128 mode** 0: GPIO128 (IO) 1: BPI_BUS25 (O) 2: Reserved 3: GPS_FRAME_SYNC (O) 4: Reserved

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Bit(s)	Mnemonic	Name	Description
			5: I2S2_DI (I) 6: PTA_RXD (I) 7: UTXD0 (O)
24:22	**GPIO127_M**	GPIO127_MODE	**Selects GPIO 127 mode** 0: GPIO127 (IO) 1: BPI_BUS24 (O) 2: Reserved 3: CONN_MCU_DBGI_N (I) 4: EXT_FRAME_SYNC (I) 5: DPI_DE1 (O) 6: SRCLKENAI1 (I) 7: URXD0 (I)
21:19	**GPIO126_M**	GPIO126_MODE	**Selects GPIO 126 mode** 0: GPIO126 (IO) 1: BPI_BUS23 (O) 2: Reserved 3: Reserved 4: Reserved 5: DPI_CK1 (O) 6: I2S2_MCK (O) 7: MD_UTXD (O)
18:16	**GPIO125_M**	GPIO125_MODE	**Selects GPIO 125 mode** 0: GPIO125 (IO) 1: BPI_BUS22 (O) 2: Reserved 3: Reserved 4: Reserved 5: DPI_VSYNC1 (O) 6: KROW2 (IO) 7: MD_URXD (I)
14:12	**GPIO124_M**	GPIO124_MODE	**Selects GPIO 124 mode** 0: GPIO124 (IO) 1: BPI_BUS21 (O) 2: Reserved 3: Reserved 4: Reserved 5: DPI_HSYNC1 (O) 6: KCOL2 (IO) 7: TDD_TXD (O)
11:9	**GPIO123_M**	GPIO123_MODE	**Selects GPIO 123 mode** 0: GPIO123 (IO) 1: BPI_BUS4 (O) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: DBG_MON_B32 (IO)
8:6	**GPIO122_M**	GPIO122_MODE	**Selects GPIO 122 mode** 0: GPIO122 (IO) 1: BPI_BUS3 (O) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: DBG_MON_B31 (IO)
5:3	**GPIO121_M**	GPIO121_MODE	**Selects GPIO 121 mode** 0: GPIO121 (IO)

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Bit(s)	Mnemonic	Name	Description
			1: BPI_BUS2 (O) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: DBG_MON_B30 (IO)
2:0	**GPIO120_M**	GPIO120_MODE	**Selects GPIO 120 mode** 0: GPIO120 (IO) 1: BPI_BUS1 (O) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: DBG_MON_B29 (IO)

102113D0 **GPIO_MODE14** **GPIO Mode Control Register 14** **12491249**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO139_M			GPIO138_M			GPIO137_M			GPIO136_M			GPIO135_M		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	1	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO134_M			GPIO133_M			GPIO132_M			GPIO131_M			GPIO130_M		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	1	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
30:28	**GPIO139_M**	GPIO139_MODE	**Selects GPIO 139 mode** 0: GPIO139 (IO) 1: PWRAP_SPIDI (IO) 2: PWRAP_SPIDO (IO) 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
27:25	**GPIO138_M**	GPIO138_MODE	**Selects GPIO 138 mode** 0: GPIO138 (IO) 1: PWRAP_SPIDO (IO) 2: PWRAP_SPIDI (IO) 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
24:22	**GPIO137_M**	GPIO137_MODE	**Selects GPIO 137 mode** 0: GPIO137 (IO) 1: RTC32K_CK (I) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved

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Bit(s)	Mnemonic	Name	Description
21:19	**GPIO136_M**	GPIO136_MODE	**Selects GPIO 136 mode** 0: GPIO136 (IO) 1: MIPI0_SDATA (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
18:16	**GPIO135_M**	GPIO135_MODE	**Selects GPIO 135 mode** 0: GPIO135 (IO) 1: MIPI0_SCLK (O) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
14:12	**GPIO134_M**	GPIO134_MODE	**Selects GPIO 134 mode** 0: GPIO134 (IO) 1: MIPI1_SDATA (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
11:9	**GPIO133_M**	GPIO133_MODE	**Selects GPIO 133 mode** 0: GPIO133 (IO) 1: MIPI1_SCLK (O) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
8:6	**GPIO132_M**	GPIO132_MODE	**Selects GPIO 132 mode** 0: GPIO132 (IO) 1: LTE_PAVM1 (O) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
5:3	**GPIO131_M**	GPIO131_MODE	**Selects GPIO 131 mode** 0: GPIO131 (IO) 1: LTE_PAVM0 (O) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
2:0	**GPIO130_M**	GPIO130_MODE	**Selects GPIO 130 mode** 0: GPIO130 (IO) 1: BPI_BUS27 (O) 2: Reserved 3: Reserved

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Bit(s)	Mnemonic	Name	Description
			4: Reserved 5: I2S2_BCK (O) 6: IRTX_OUT (O) 7: LTE_UTXD (O)

102113E0 **GPIO_MODE15** **GPIO Mode Control Register 15** **12011248**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO149_M			GPIO148_M			GPIO147_M			GPIO146_M			GPIO145_M		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO144_M			GPIO143_M			GPIO142_M			GPIO141_M			GPIO140_M		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	1	0	0	1	0	0	0

Bit(s)	Mnemonic	Name	Description
30:28	**GPIO149_M**	GPIO149_MODE	**Selects GPIO 149 mode** 0: GPIO149 (IO) 1: WATCHDOG (O) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
27:25	**GPIO148_M**	GPIO148_MODE	**Selects GPIO 148 mode** 0: GPIO148 (IO) 1: SRCLKENA (O) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
24:22	**GPIO147_M**	GPIO147_MODE	**Selects GPIO 147 mode** 0: GPIO147 (IO) 1: DSI_TE (I) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
21:19	**GPIO146_M**	GPIO146_MODE	**Selects GPIO 146 mode** 0: GPIO146 (IO) 1: LCM_RST (O) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
18:16	**GPIO145_M**	GPIO145_MODE	**Selects GPIO 145 mode** 0: GPIO145 (IO) 1: AUD_DAT_MOSI (O)

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Bit(s)	Mnemonic	Name	Description
			2: Reserved 3: AUD_DAT_MISO (I) 4: Reserved 5: Reserved 6: Reserved 7: Reserved
14:12	**GPIO144_M**	GPIO144_MODE	**Selects GPIO 144 mode** 0: GPIO144 (IO) 1: AUD_DAT_MISO (I) 2: Reserved 3: AUD_DAT_MOSI (O) 4: Reserved 5: Reserved 6: Reserved 7: Reserved
11:9	**GPIO143_M**	GPIO143_MODE	**Selects GPIO 143 mode** 0: GPIO143 (IO) 1: AUD_CLK_MOSI (O) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
8:6	**GPIO142_M**	GPIO142_MODE	**Selects GPIO 142 mode** 0: GPIO142 (IO) 1: PWRAP_SPICS_B_I (O) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
5:3	**GPIO141_M**	GPIO141_MODE	**Selects GPIO 141 mode** 0: GPIO141 (IO) 1: PWRAP_SPICK_I (O) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
2:0	**GPIO140_M**	GPIO140_MODE	**Selects GPIO 140 mode** 0: GPIO140 (IO) 1: Reserved 2: Reserved 3: LTE_MD32_JTAG_TRST (I) 4: TDD_TRSTN (I) 5: DM_JTINTP (O) 6: Reserved 7: Reserved

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102113F0 **GPIO_MODE16** **GPIO Mode Control Register 16** **12491249**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**GPIO159_M**			**GPIO158_M**			**GPIO157_M**			**GPIO156_M**			**GPIO155_M**		
Type		RW			RW			RW			RW			RW		

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Reset		0	0	1	0	0	1	0	0	1	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO154_M			GPIO153_M			GPIO152_M			GPIO151_M			GPIO150_M		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	1	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
30:28	**GPIO159_M**	GPIO159_MODE	**Selects GPIO 159 mode** 0: GPIO159 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
27:25	**GPIO158_M**	GPIO158_MODE	**Selects GPIO 158 mode** 0: GPIO158 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
24:22	**GPIO157_M**	GPIO157_MODE	**Selects GPIO 157 mode** 0: GPIO157 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
21:19	**GPIO156_M**	GPIO156_MODE	**Selects GPIO 156 mode** 0: GPIO156 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
18:16	**GPIO155_M**	GPIO155_MODE	**Selects GPIO 155 mode** 0: GPIO155 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
14:12	**GPIO154_M**	GPIO154_MODE	**Selects GPIO 154 mode** 0: GPIO154 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved

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Bit(s)	Mnemonic	Name	Description
			7: Reserved
11:9	**GPIO153_M**	GPIO153_MODE	**Selects GPIO 153 mode** 0: GPIO153 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
8:6	**GPIO152_M**	GPIO152_MODE	**Selects GPIO 152 mode** 0: GPIO152 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
5:3	**GPIO151_M**	GPIO151_MODE	**Selects GPIO 151 mode** 0: GPIO151 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
2:0	**GPIO150_M**	GPIO150_MODE	**Selects GPIO 150 mode** 0: GPIO150 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved

10211400 **GPIO_MODE17** **GPIO Mode Control Register 17** **12491249**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO169_M			GPIO168_M			GPIO167_M			GPIO166_M			GPIO165_M		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	1	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO164_M			GPIO163_M			GPIO162_M			GPIO161_M			GPIO160_M		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	1	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
30:28	**GPIO169_M**	GPIO169_MODE	**Selects GPIO 169 mode** 0: GPIO169 (IO) 1: MSDC1_DAT1 (IO) 2: LTE_MD32_JTAG_TDO (IO) 3: C2K_TDO (IO) 4: TDD_TDO (IO)

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Bit(s)	Mnemonic	Name	Description
			5: CONN_DSP_JDO (O) 6: JTDO (O) 7: Reserved
27:25	**GPIO168_M**	GPIO168_MODE	**Selects GPIO 168 mode** 0: GPIO168 (IO) 1: MSDC1_DAT0 (IO) 2: LTE_MD32_JTAG_TDI (I) 3: C2K_TDI (I) 4: TDD_TDI (I) 5: CONN_DSP_JDI (I) 6: JTDI (I) 7: Reserved
24:22	**GPIO167_M**	GPIO167_MODE	**Selects GPIO 167 mode** 0: GPIO167 (IO) 1: MSDC1_CLK (O) 2: LTE_MD32_JTAG_TCK (I) 3: C2K_TCK (I) 4: TDD_TCK (I) 5: CONN_DSP_JCK (I) 6: JTCK (I) 7: CONN_MCU_AICE_TCKC (I)
21:19	**GPIO166_M**	GPIO166_MODE	**Selects GPIO 166 mode** 0: GPIO166 (IO) 1: MSDC1_CMD (IO) 2: LTE_MD32_JTAG_TMS (I) 3: C2K_TMS (I) 4: TDD_TMS (I) 5: CONN_DSP_JMS (I) 6: JTMS (IO) 7: CONN_MCU_AICE_TMSC (IO)
18:16	**GPIO165_M**	GPIO165_MODE	**Selects GPIO 165 mode** 0: GPIO165 (IO) 1: MD_SIM1_SDAT (IO) 2: MD_SIM2_SDAT (IO) 3: UIM1_IO (IO) 4: UIM0_IO (IO) 5: Reserved 6: Reserved 7: Reserved
14:12	**GPIO164_M**	GPIO164_MODE	**Selects GPIO 164 mode** 0: GPIO164 (IO) 1: MD_SIM1_SRST (O) 2: MD_SIM2_SRST (O) 3: UIM1_RST (O) 4: UIM0_RST (O) 5: Reserved 6: Reserved 7: Reserved
11:9	**GPIO163_M**	GPIO163_MODE	**Selects GPIO 163 mode** 0: GPIO163 (IO) 1: MD_SIM1_SCLK (O) 2: MD_SIM2_SCLK (O) 3: UIM1_CLK (O) 4: UIM0_CLK (O) 5: Reserved 6: Reserved 7: Reserved
8:6	**GPIO162_M**	GPIO162_MODE	**Selects GPIO 162 mode** 0: GPIO162 (IO)

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Bit(s)	Mnemonic	Name	Description
			1: MD_SIM2_SDAT (IO) 2: MD_SIM1_SDAT (IO) 3: UIM0_IO (IO) 4: UIM1_IO (IO) 5: Reserved 6: Reserved 7: Reserved
5:3	**GPIO161_M**	GPIO161_MODE	**Selects GPIO 161 mode** 0: GPIO161 (IO) 1: MD_SIM2_SRST (O) 2: MD_SIM1_SRST (O) 3: UIM0_RST (O) 4: UIM1_RST (O) 5: Reserved 6: Reserved 7: Reserved
2:0	**GPIO160_M**	GPIO160_MODE	**Selects GPIO 160 mode** 0: GPIO160 (IO) 1: MD_SIM2_SCLK (O) 2: MD_SIM1_SCLK (O) 3: UIM0_CLK (O) 4: UIM1_CLK (O) 5: Reserved 6: Reserved 7: Reserved

10211410 **GPIO_MODE18** **GPIO Mode Control Register 18** **12491249**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**GPIO179_M**			**GPIO178_M**			**GPIO177_M**			**GPIO176_M**			**GPIO175_M**		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	1	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**GPIO174_M**			**GPIO173_M**			**GPIO172_M**			**GPIO171_M**			**GPIO170_M**		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	1	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
30:28	**GPIO179_M**	GPIO179_MODE	**Selects GPIO 179 mode** 0: GPIO179 (IO) 1: MSDC0_DAT4 (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
27:25	**GPIO178_M**	GPIO178_MODE	**Selects GPIO 178 mode** 0: GPIO178 (IO) 1: MSDC0_DAT3 (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved

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Bit(s)	Mnemonic	Name	Description
24:22	**GPIO177_M**	GPIO177_MODE	**Selects GPIO 177 mode** 0: GPIO177 (IO) 1: MSDC0_DAT2 (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
21:19	**GPIO176_M**	GPIO176_MODE	**Selects GPIO 176 mode** 0: GPIO176 (IO) 1: MSDC0_DAT1 (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
18:16	**GPIO175_M**	GPIO175_MODE	**Selects GPIO 175 mode** 0: GPIO175 (IO) 1: MSDC0_DAT0 (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
14:12	**GPIO174_M**	GPIO174_MODE	**Selects GPIO 174 mode** 0: GPIO174 (IO) 1: MSDC0_CLK (O) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
11:9	**GPIO173_M**	GPIO173_MODE	**Selects GPIO 173 mode** 0: GPIO173 (IO) 1: MSDC0_DSL (I) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
8:6	**GPIO172_M**	GPIO172_MODE	**Selects GPIO 172 mode** 0: GPIO172 (IO) 1: MSDC0_CMD (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
5:3	**GPIO171_M**	GPIO171_MODE	**Selects GPIO 171 mode** 0: GPIO171 (IO) 1: MSDC1_DAT3 (IO) 2: Reserved 3: C2K_RTCK (O)

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Bit(s)	Mnemonic	Name	Description
			4: Reserved 5: Reserved 6: Reserved 7: Reserved
2:0	**GPIO170_M**	GPIO170_MODE	**Selects GPIO 170 mode** 0: GPIO170 (IO) 1: MSDC1_DAT2 (IO) 2: LTE_MD32_JTAG_TRST (I) 3: C2K_NTRST (I) 4: TDD_TRSTN (I) 5: CONN_DSP_JINTP (O) 6: DM_JTINTP (O) 7: Reserved

10211420 **GPIO_MODE19** **GPIO Mode Control Register 19** **12491249**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO189_M			GPIO188_M			GPIO187_M			GPIO186_M			GPIO185_M		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	1	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO184_M			GPIO183_M			GPIO182_M			GPIO181_M			GPIO180_M		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	1	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
30:28	**GPIO189_M**	GPIO189_MODE	**Selects GPIO 189 mode** 0: GPIO189 (IO) 1: WB_SEN (O) 2: Reserved 3: Reserved 4: UTXD3 (O) 5: URXD3 (I) 6: Reserved 7: Reserved
27:25	**GPIO188_M**	GPIO188_MODE	**Selects GPIO 188 mode** 0: GPIO188 (IO) 1: WB_SDATA (IO) 2: MRG_SYNC (O) 3: Reserved 4: PCM0_SYNC (O) 5: Reserved 6: Reserved 7: Reserved
24:22	**GPIO187_M**	GPIO187_MODE	**Selects GPIO 187 mode** 0: GPIO187 (IO) 1: WB_SCLK (O) 2: MRG_DO (O) 3: Reserved 4: PCM0_DO (O) 5: Reserved 6: Reserved 7: Reserved
21:19	**GPIO186_M**	GPIO186_MODE	**Selects GPIO 186 mode** 0: GPIO186 (IO) 1: WB_RSTB (O)

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Bit(s)	Mnemonic	Name	Description
			2: Reserved 3: Reserved 4: URXD3 (I) 5: UTXD3 (O) 6: Reserved 7: Reserved
18:16	**GPIO185_M**	GPIO185_MODE	**Selects GPIO 185 mode** 0: GPIO185 (IO) 1: F2W_CK (I) 2: MRG_DI (I) 3: C2K_DM_EINT3 (IO) 4: PCM0_DI (I) 5: Reserved 6: Reserved 7: Reserved
14:12	**GPIO184_M**	GPIO184_MODE	**Selects GPIO 184 mode** 0: GPIO184 (IO) 1: F2W_DATA (I) 2: MRG_CLK (O) 3: C2K_DM_EINT2 (IO) 4: PCM0_CLK (O) 5: Reserved 6: Reserved 7: Reserved
11:9	**GPIO183_M**	GPIO183_MODE	**Selects GPIO 183 mode** 0: GPIO183 (IO) 1: MSDC0_RSTB (O) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
8:6	**GPIO182_M**	GPIO182_MODE	**Selects GPIO 182 mode** 0: GPIO182 (IO) 1: MSDC0_DAT7 (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
5:3	**GPIO181_M**	GPIO181_MODE	**Selects GPIO 181 mode** 0: GPIO181 (IO) 1: MSDC0_DAT6 (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
2:0	**GPIO180_M**	GPIO180_MODE	**Selects GPIO 180 mode** 0: GPIO180 (IO) 1: MSDC0_DAT5 (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved

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Bit(s)	Mnemonic	Name	Description
			7: Reserved

10211430 **GPIO_MODE20** **GPIO Mode Control Register 20** **00491249**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**GPIO199_M**			**GPIO198_M**			**GPIO197_M**			**GPIO196_M**			**GPIO195_M**		
Type		RW			RW			RW			RW			RW		
Reset		0	0	0	0	0	0	0	0	1	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**GPIO194_M**			**GPIO193_M**			**GPIO192_M**			**GPIO191_M**			**GPIO190_M**		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	1	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
30:28	**GPIO199_M**	GPIO199_MODE	**Selects GPIO 199 mode** 0: GPIO199 (IO) 1: MSDC2_CLK (O) 2: SCL1 (IO) 3: C2K_UART0_TXD (O) 4: C2K_TCK (I) 5: ANT_SEL7 (O) 6: TDD_TXD (O) 7: DM_OTCK (I)
27:25	**GPIO198_M**	GPIO198_MODE	**Selects GPIO 198 mode** 0: GPIO198 (IO) 1: MSDC2_CMD (IO) 2: SDA1 (IO) 3: C2K_UART0_RXD (I) 4: C2K_TMS (I) 5: ANT_SEL6 (O) 6: Reserved 7: DM_OTMS (I)
24:22	**GPIO197_M**	GPIO197_MODE	**Selects GPIO 197 mode** 0: GPIO197 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
21:19	**GPIO196_M**	GPIO196_MODE	**Selects GPIO 196 mode** 0: GPIO196 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
18:16	**GPIO195_M**	GPIO195_MODE	**Selects GPIO 195 mode** 0: GPIO195 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved

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Bit(s)	Mnemonic	Name	Description
			5: Reserved 6: Reserved 7: Reserved
14:12	**GPIO194_M**	GPIO194_MODE	**Selects GPIO 194 mode** 0: GPIO194 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
11:9	**GPIO193_M**	GPIO193_MODE	**Selects GPIO 193 mode** 0: GPIO193 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
8:6	**GPIO192_M**	GPIO192_MODE	**Selects GPIO 192 mode** 0: GPIO192 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
5:3	**GPIO191_M**	GPIO191_MODE	**Selects GPIO 191 mode** 0: GPIO191 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
2:0	**GPIO190_M**	GPIO190_MODE	**Selects GPIO 190 mode** 0: GPIO190 (IO) 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved

10211440 **GPIO_MODE21** **GPIO Mode Control Register 21** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name					GPIO203_M			GPIO202_M			GPIO201_M			GPIO200_M		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:9	GPIO203_M	GPIO203_MODE	**Selects GPIO 203 mode** 0: GPIO203 (IO) 1: MSDC2_DAT3 (IO) 2: ANT_SEL5 (O) 3: SCL2 (IO) 4: C2K_RTCK (O) 5: URXD1 (I) 6: KCOL6 (IO) 7: Reserved
8:6	GPIO202_M	GPIO202_MODE	**Selects GPIO 202 mode** 0: GPIO202 (IO) 1: MSDC2_DAT2 (IO) 2: ANT_SEL4 (O) 3: SDA2 (IO) 4: C2K_NTRST (I) 5: UTXD1 (O) 6: KCOL3 (IO) 7: DM_JTINTP (O)
5:3	GPIO201_M	GPIO201_MODE	**Selects GPIO 201 mode** 0: GPIO201 (IO) 1: MSDC2_DAT1 (IO) 2: ANT_SEL3 (O) 3: PWM0 (O) 4: C2K_TDO (IO) 5: URXD0 (I) 6: Reserved 7: DM_OTDO (IO)
2:0	GPIO200_M	GPIO200_MODE	**Selects GPIO 200 mode** 0: GPIO200 (IO) 1: MSDC2_DAT0 (IO) 2: ANT_SEL6 (O) 3: GPS_FRAME_SYNC (O) 4: C2K_TDI (I) 5: UTXD0 (O) 6: Reserved 7: DM_OTDI (I)

102116D0 GPIO_DEBUG GPIO Debug mode register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													MDPLL_IN_SEL	MDABB_IN_SEL	USB_IN_SEL	AUXADC_IN_SEL
Type													RW	RW	RW	RW
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DEBUG_B_SEL								DEBUG_A_SEL				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19		MDPLL_IN_SEL	**Selects MDPLL debug in**

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Bit(s)	Mnemonic	Name	Description
			0: Disable 1: Enable
18		MDABB_IN_SEL	**Selects MD ADD debug in** 0: Disable 1: Enable
17		USB_IN_SEL	**Selects USB debug in** 0: Disable 1: Enable
16		AUXADC_IN_SEL	**Selects AUXADC debug in** 0: Disable 1: Enable
12:8		DEBUG_B_SEL	**Selects debug monitor bus B** 0: cksys 1: mcusys 2: infra_ao 3: mmsys 4: mipi_tx 5: mipi_rx 6: Reserved 7: mfgsys 8: apmixsys 9: mdsys A: subsys_mbist_result B: conn_test C: infra_ao (AUXADC IN) D: USB E: USB_IN F: md_add 10: md_pll merge in mdsys 11: USB 12: md2_abb Others: Reserved
4:0		DEBUG_A_SEL	**Selects debug monitor bus A** 0: cksys 1: mcusys 2: Infra_ao 3: mmsys 4: mipi_tx 5: mipi_rx 6: Reserved 7: mfgsys 8: apmixsys 9: mdsys A: subsys_mbist_result B: conn_test C: infra_ao (AUXADC IN) D: USB E: USB_IN F: md_add 10: md_pll merge in mdsys 11: USB 12: md2_abb Others: Reserved

102116E0 **GPIO_BACKUP** **GPIO Reserved Control Register** **0000F801**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name														ROSC_RDSEL		ROSC_EN
Type														RW		RW
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BACKUP_REG													C2K_GPS_SYNC_SEL	GPS_SYNC_SEL	GPIO_BACKUP
Type	RW													RW	RW	RW
Reset	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
18:17		ROSC_RDSEL	**IO RING OSC RDSEL[1:0]** IORING OSC RDSEL[1: 0]
16		ROSC_EN	**Enables IO RING OSC** 0: Disable IORING OSC 1: Enable IORING OSC
15:3		BACKUP_REG	**GPIO reserved control register** 0: Reserved 1: Reserved
2		C2K_GPS_SYNC_SEL	**Selects GPS sync source** 0: Internal frame sync from modem 1: Internal frame sync from C2K
1		GPS_SYNC_SEL	**Selects GPS sync source** 0: Internal frame sync 1: External frame sync
0		GPIO_BACKUP	**GPIO reserved control register** 0: Reserved 1: Reserved

102116F0 **GPIO_TEST_MODE** **GPIO Test Mode Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TM_DIR
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0		TM_DIR	**Selects test mode** 0: Return GPIO_DIR on GPIO_DIR register 1: Return GPIO_OE on GPIO_DIR register

10211800 **GPIO_IES_G0** **GPIO Group 0 IES Control Register** **FF**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RESERVE			IES_G0_4	IES_G0_3	IES_G0_2	IES_G0_1	IES_G0_0

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Type									RW			RW	RW	RW	RW	RW
Reset									1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
7:5		RESERVE	**Reserved register**
4		IES_G0_4	**MSDC2 DATA PADs input enable control** 0: Disable 1: Enable
3		IES_G0_3	**MSDC2 CLK PAD input enable control** 0: Disable 1: Enable
2		IES_G0_2	**MSDC2 CMD PAD input enable control** 0: Disable 1: Enable
1		IES_G0_1	**ANTSEL PADs input enable control** 0: Disable 1: Enable
0		IES_G0_0	**WBCTRL PADs input enable control** 0: Disable 1: Enable

10211810 **GPIO_SMT_G0** **GPIO Group 0 SMT Control Register** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												SMT_G0_5	SMT_G0_4	SMT_G0_3	SMT_G0_1	SMT_G0_0
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4		SMT_G0_5	**Controls MSDC2 DATA PADs Schmitt trigger** 0: Disable 1: Enable
3		SMT_G0_4	**Controls MSDC2 CLK PAD Schmitt trigger** 0: Disable 1: Enable
2		SMT_G0_3	**Controls MSDC2 CMD PAD Schmitt trigger** 0: Disable 1: Enable
1		SMT_G0_1	**Controls ANTSEL PADs Schmitt trigger** 0: Disable 1: Enable
0		SMT_G0_0	**Controls WBCTRL PADs Schmitt trigger** 0: Disable 1: Enable

10211820 **GPIO_TDSEL0_G0** **GPIO Group 0 TDSEL Control Register 0** **000AAA00**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name													TDSEL0_G0_5			
Type													RW			
Reset													1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDSEL0_G0_4				TDSEL0_G0_3				TDSEL0_G0_1				TDSEL0_G0_0			
Type	RW				RW				RW				RW			
Reset	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:16		TDSEL0_G0_5	Controls MSDC2 DATA PADs Tx delay selection
15:12		TDSEL0_G0_4	Controls MSDC2 CLK PAD Tx delay selection
11:8		TDSEL0_G0_3	Controls MSDC2 CMD PAD Tx delay selection
7:4		TDSEL0_G0_1	Controls ANTSEL PADs Tx delay selection
3:0		TDSEL0_G0_0	Controls WBCTRL PADs Tx delay selection

10211828 **GPIO_RDSEL0_G0** **GPIO Group 0 RDSEL Control Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											RDSEL0_G0_5					
Type											RW					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDSEL0_G0_4						RDSEL0_G0_3						RDSEL0_G0_1		RDSEL0_G0_0	
Type	RW						RW						RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:16		RDSEL0_G0_5	Controls MSDC2 DATA PADs Rx delay selection
15:10		RDSEL0_G0_4	Controls MSDC2 CLK PAD Rx delay selection
9:4		RDSEL0_G0_3	Controls MSDC2 CMD PAD Rx delay selection
3:2		RDSEL0_G0_1	Controls ANTSEL PADs Rx delay selection
1:0		RDSEL0_G0_0	Controls WBCTRL PADs Rx delay selection

10211830 **GPIO_PULLEN0_G0** **GPIO Group 0 PULLEN Control Register 0** **000001FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								PULLEN0_G0_8	PULLEN0_G0_7	PULLEN0_G0_6	PULLEN0_G0_5	PULLEN0_G0_4	PULLEN0_G0_3	PULLEN0_G0_2	PULLEN0_G0_1	PULLEN0_G0_0
Type								RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset								1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
8		PULLEN0_G0_8	**Controls GPIO21 PULLEN** 0: Disable pull control 1: Enable pull control

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Bit(s)	Mnemonic	Name	Description
7		PULLEN0_G0_7	**Controls GPIO20 PULLEN** 0: Disable pull control 1: Enable pull control
6		PULLEN0_G0_6	**Controls GPIO19 PULLEN** 0: Disable pull control 1: Enable pull control
5		PULLEN0_G0_5	**Controls GPIO18 PULLEN** 0: Disable pull control 1: Enable pull control
4		PULLEN0_G0_4	**Controls GPIO17 PULLEN** 0: Disable pull control 1: Enable pull control
3		PULLEN0_G0_3	**Controls GPIO16 PULLEN** 0: Disable pull control 1: Enable pull control
2		PULLEN0_G0_2	**Controls GPIO15 PULLEN** 0: Disable pull control 1: Enable pull control
1		PULLEN0_G0_1	**Controls GPIO14 PULLEN** 0: Disable pull control 1: Enable pull control
0		PULLEN0_G0_0	**Controls GPIO13 PULLEN** 0: Disable pull control 1: Enable pull control

10211850 **GPIO_PULLSEL0_G0** **GPIO Group 0 PULLSEL Control Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**PULLSEL0_G0_8**	**PULLSEL0_G0_7**	**PULLSEL0_G0_6**	**PULLSEL0_G0_5**	**PULLSEL0_G0_4**	**PULLSEL0_G0_3**	**PULLSEL0_G0_2**	**PULLSEL0_G0_1**	**PULLSEL0_G0_0**
Type								RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8		PULLSEL0_G0_8	**Controls GPIO21 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
7		PULLSEL0_G0_7	**Controls GPIO20 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
6		PULLSEL0_G0_6	**Controls GPIO19 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
5		PULLSEL0_G0_5	**Controls GPIO18 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1

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Bit(s)	Mnemonic	Name	Description
4		PULLSEL0_G0_4	**Controls GPIO17 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
3		PULLSEL0_G0_3	**Controls GPIO16 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
2		PULLSEL0_G0_2	**Controls GPIO15 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
1		PULLSEL0_G0_1	**Controls GPIO14 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
0		PULLSEL0_G0_0	**Controls GPIO13 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1

10211870 **GPIO_DRV0_G0** **GPIO Group 0 Driving Control Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													**DRV0_G0_4**			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DRV0_G0_3**				**DRV0_G0_2**				**DRV0_G0_1**				**DRV0_G0_0**			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:16		DRV0_G0_4	**Controls MSDC2 DATA PADs driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:0]: 000: 2mA 100: 4mA 010: 6mA 110: 8mA 001: 10mA 101: 12mA 011: 14mA 111: 16mA
15:12		DRV0_G0_3	**Controls MSDC2 CLK PAD driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:0]: 000: 2mA 100: 4mA 010: 6mA 110: 8mA 001: 10mA 101: 12mA 011: 14mA 111: 16mA

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Bit(s)	Mnemonic	Name	Description
11:8		DRV0_G0_2	**Controls MSDC2 CMD PAD driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:0]: 000: 2mA 100: 4mA 010: 6mA 110: 8mA 001: 10mA 101: 12mA 011: 14mA 111: 16mA
7:4		DRV0_G0_1	**Controls ANTSEL PADs driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:1]: 00: 2mA 01: 4mA 10: 6mA 11: 8mA [0]: Reserved
3:0		DRV0_G0_0	**Controls WBCTRL PADs driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:1]: 00: 2mA 01: 4mA 10: 6mA 11 : 8mA [0]: Reserved

10211880 **GPIO_PUPD0_G0** **GPIO Group 0 Special IO PU/PD Control Register0** **05666666**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					PUPD1_G0_6					PUPD0_G0_5				PUPD0_G0_4		
Type					RW					RW				RW		
Reset					0	1	0	1		1	1	0		1	1	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name		PUPD0_G0_3				PUPD0_G0_2				PUPD0_G0_1				PUPD0_G0_0		
Type		RW				RW				RW				RW		
Reset		1	1	0		1	1	0		1	1	0		1	1	0

Bit(s)	Mnemonic	Name	Description
27:24		PUPD1_G0_6	**Controls MSDC2 BIAS TUNE** TUNE[3:0]
22:20		PUPD0_G0_5	**Controls MSDC2_DATA3 PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K
18:16		PUPD0_G0_4	**Controls MSDC2_DATA2 PUPD** [2]: 0: Pull up; 1: Pull down

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Bit(s)	Mnemonic	Name	Description
			[1]: 50K [0]: 10K
14:12		PUPD0_G0_3	**Controls MSDC2_DATA1 PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K
10:8		PUPD0_G0_2	**Controls MSDC2_DATA0 PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K
6:4		PUPD0_G0_1	**Controls MSDC2_CLK PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K0
2:0		PUPD0_G0_0	**Controls MSDC2_CMD PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K

10211900 GPIO_IES_G1 GPIO Group 1 IES Control Register FFFF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESERVE					IES_G1_10	IES_G1_9	IES_G1_8	IES_G1_7	IES_G1_6	IES_G1_5	IES_G1_4	IES_G1_3	IES_G1_2	IES_G1_1	IES_G1_0
Type	RW					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
15:11		RESERVE	**Reserved register**
10		IES_G1_10	**EINT0~4 PADs input enable control** 0: Disable 1: Enable
9		IES_G1_9	**PCM PADs input enable control** 0: Disable 1: Enable
8		IES_G1_8	**UART2/3 PADs input enable control** 0: Disable 1: Enable
7		IES_G1_7	**SRCLKENA1 PADs input enable control** 0: Disable 1: Enable
6		IES_G1_6	**SRCLKENAI PAD input enable control** 0: Disable 1: Enable
5		IES_G1_5	**I2C3 PADs input enable control** 0: Disable 1: Enable
4		IES_G1_4	**I2C2 PADs input enable control** 0: Disable 1: Enable
3		IES_G1_3	**I2C1 PADs input enable control** 0: Disable

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Bit(s)	Mnemonic	Name	Description
			1: Enable
2		IES_G1_2	**I2C0 PADs input enable control** 0: Disable 1: Enable
1		IES_G1_1	**CMMCLK PAD input enable control** 0: Disable 1: Enable
0		IES_G1_0	**DCAM PADs input enable control** 0: Disable 1: Enable

10211910 **GPIO_SMT_G1** **GPIO Group 1 SMT Control Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						SMT_G1_10	SMT_G1_9	SMT_G1_8	SMT_G1_7	SMT_G1_6	SMT_G1_5	SMT_G1_4	SMT_G1_3	SMT_G1_2	SMT_G1_1	SMT_G1_0
Type						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
10		SMT_G1_10	**Controls EINT0~4 PADs Schmitt trigger** 0: Disable 1: Enable
9		SMT_G1_9	**Controls PCM PADs Schmitt trigger** 0: Disable 1: Enable
8		SMT_G1_8	**Controls UART2/3 PADs Schmitt trigger** 0: Disable 1: Enable
7		SMT_G1_7	**Controls SRCLKENA1 PADs Schmitt trigger** 0: Disable 1: Enable
6		SMT_G1_6	**Controls SRCLKENAI PAD Schmitt trigger** 0: Disable 1: Enable
5		SMT_G1_5	**Controls I2C3 PADs Schmitt trigger** 0: Disable 1: Enable
4		SMT_G1_4	**Controls I2C2 PADs Schmitt trigger** 0: Disable 1: Enable
3		SMT_G1_3	**Controls I2C1 PADs Schmitt trigger** 0: Disable 1: Enable
2		SMT_G1_2	**Controls I2C0 PADs Schmitt trigger** 0: Disable 1: Enable
1		SMT_G1_1	**Controls CMMCLK PAD Schmitt trigger** 0: Disable 1: Enable

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Bit(s)	Mnemonic	Name	Description
0		SMT_G1_0	**Controls DCAM PADs Schmitt trigger** 0: Disable 1: Enable

10211920 **GPIO_TDSEL0_G1** **GPIO Group 1 TDSEL Control Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**TDSEL0_G1_7**				**TDSEL0_G1_6**				**TDSEL0_G1_5**				**TDSEL0_G1_4**			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TDSEL0_G1_3**				**TDSEL0_G1_2**				**TDSEL0_G1_1**				**TDSEL0_G1_0**			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		TDSEL0_G1_7	Controls SRCLKENA1 PADs Tx delay selectionl
27:24		TDSEL0_G1_6	Controls SRCLKENAI PAD Tx delay selection
23:20		TDSEL0_G1_5	Controls I2C3 PADs Tx delay selection
19:16		TDSEL0_G1_4	Controls I2C2 PADs Tx delay selection
15:12		TDSEL0_G1_3	Controls I2C1 PADs Tx delay selection
11:8		TDSEL0_G1_2	Controls I2C0 PADs Tx delay selection
7:4		TDSEL0_G1_1	Controls CMMCLK PAD Tx delay selection
3:0		TDSEL0_G1_0	Controls DCAM PADs Tx delay selection

10211924 **GPIO_TDSEL1_G1** **GPIO Group 1 TDSEL Control Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**TDSEL0_G1_10**				**TDSEL0_G1_9**				**TDSEL0_G1_8**			
Type					RW				RW				RW			
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:8		TDSEL0_G1_10	Controls EINT0~4 PADs Tx delay selection
7:4		TDSEL0_G1_9	Controls PCM PADs Tx delay selection
3:0		TDSEL0_G1_8	Controls UART2/3 PADs Tx delay selection

10211928 **GPIO_RDSEL0_G1** **GPIO Group 1 RDSEL Control Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							**RDSEL0_G1_10**		**RDSEL0_G1_9**		**RDSEL0_G1_8**		**RDSEL0_G1_7**		**RDSEL0_G1_6**	

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Type							RW		RW		RW		RW		RW	
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDSEL0_G1_5		RDSEL0_G1_4		RDSEL0_G1_3		RDSEL0_G1_2		RDSEL0_G1_1						RDSEL0_G1_0	
Type	RW		RW		RW		RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
25:24		RDSEL0_G1_10	Controls EINT0~4 PADs Rx delay selection
23:22		RDSEL0_G1_9	Controls PCM PADs Rx delay selection
21:20		RDSEL0_G1_8	Controls UART2/3 PADs Rx delay selection
19:18		RDSEL0_G1_7	Controls SRCLKENA1 PADs Rx delay selection
17:16		RDSEL0_G1_6	Controls SRCLKENAI PAD Rx delay selection
15:14		RDSEL0_G1_5	Controls I2C3 PADs Rx delay selection
13:12		RDSEL0_G1_4	Controls I2C2 PADs Rx delay selection
11:10		RDSEL0_G1_3	Controls I2C1 PADs Rx delay selection
9:8		RDSEL0_G1_2	Controls I2C0 PADs Rx delay selection
7:2		RDSEL0_G1_1	Controls CMMCLK PAD Rx delay selection
1:0		RDSEL0_G1_0	Controls DCAM PADs Rx delay selection

10211930 **GPIO_PULLEN0_G1** **GPIO Group 1 PULLEN Control Register 0** **0FFFFFE7**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					PULLEN0_G1_27	PULLEN0_G1_26	PULLEN0_G1_25	PULLEN0_G1_24	PULLEN0_G1_23	PULLEN0_G1_22	PULLEN0_G1_21	PULLEN0_G1_20	PULLEN0_G1_19	PULLEN0_G1_18	PULLEN0_G1_17	PULLEN0_G1_16
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PULLEN0_G1_15	PULLEN0_G1_14	PULLEN0_G1_13	PULLEN0_G1_12	PULLEN0_G1_11	PULLEN0_G1_10	PULLEN0_G1_9	PULLEN0_G1_8	PULLEN0_G1_7	PULLEN0_G1_6	PULLEN0_G1_5			PULLEN0_G1_2	PULLEN0_G1_1	PULLEN0_G1_0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW			RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1			1	1	1

Bit(s)	Mnemonic	Name	Description
27		PULLEN0_G1_27	**Controls GPIO4 PULLEN** 0: Disable pull control 1: Enable pull control
26		PULLEN0_G1_26	**Controls GPIO3 PULLEN** 0: Disable pull control 1: Enable pull control
25		PULLEN0_G1_25	**Controls GPIO2 PULLEN** 0: Disable pull control 1: Enable pull control
24		PULLEN0_G1_24	**Controls GPIO1 PULLEN** 0: Disable pull control 1: Enable pull control
23		PULLEN0_G1_23	**Controls GPIO0 PULLEN** 0: Disable pull control

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Bit(s)	Mnemonic	Name	Description
			1: Enable pull control
22		PULLEN0_G1_22	**Controls GPIO64 PULLEN** 0: Disable pull control 1: Enable pull control
21		PULLEN0_G1_21	**Controls GPIO63 PULLEN** 0: Disable pull control 1: Enable pull control
20		PULLEN0_G1_20	**Controls GPIO62 PULLEN** 0: Disable pull control 1: Enable pull control
19		PULLEN0_G1_19	**Controls GPIO61 PULLEN** 0: Disable pull control 1: Enable pull control
18		PULLEN0_G1_18	**Controls GPIO60 PULLEN** 0: Disable pull control 1: Enable pull control
17		PULLEN0_G1_17	**Controls GPIO59 PULLEN** 0: Disable pull control 1: Enable pull control
16		PULLEN0_G1_16	**Controls GPIO58 PULLEN** 0: Disable pull control 1: Enable pull control
15		PULLEN0_G1_15	**Controls GPIO57 PULLEN** 0: Disable pull control 1: Enable pull control
14		PULLEN0_G1_14	**Controls GPIO56 PULLEN** 0: Disable pull control 1: Enable pull control
13		PULLEN0_G1_13	**Controls GPIO55 PULLEN** 0: Disable pull control 1: Enable pull control
12		PULLEN0_G1_12	**Controls GPIO54 PULLEN** 0: Disable pull control 1: Enable pull control
11		PULLEN0_G1_11	**Controls GPIO53 PULLEN** 0: Disable pull control 1: Enable pull control
10		PULLEN0_G1_10	**Controls GPIO52 PULLEN** 0: Disable pull control 1: Enable pull control
9		PULLEN0_G1_9	**Controls GPIO51 PULLEN** 0: Disable pull control 1: Enable pull control
8		PULLEN0_G1_8	**Controls GPIO50 PULLEN** 0: Disable pull control 1: Enable pull control
7		PULLEN0_G1_7	**Controls GPIO49 PULLEN** 0: Disable pull control 1: Enable pull control
6		PULLEN0_G1_6	**Controls GPIO48 PULLEN** 0: Disable pull control 1: Enable pull control

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Bit(s)	Mnemonic	Name	Description
5		PULLEN0_G1_5	**Controls GPIO47 PULLEN** 0: Disable pull control 1: Enable pull control
2		PULLEN0_G1_2	**Controls GPIO44 PULLEN** 0: Disable pull control 1: Enable pull control
1		PULLEN0_G1_1	**Controls GPIO43 PULLEN** 0: Disable pull control 1: Enable pull control
0		PULLEN0_G1_0	**Controls GPIO42 PULLEN** 0: Disable pull control 1: Enable pull control

10211950 **GPIO_PULLSEL0_G1** **GPIO Group 1 PULLSEL Control Register 0** **00005FE0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					PULLSEL0_G1_27	PULLSEL0_G1_26	PULLSEL0_G1_25	PULLSEL0_G1_24	PULLSEL0_G1_23	PULLSEL0_G1_22	PULLSEL0_G1_21	PULLSEL0_G1_20	PULLSEL0_G1_19	PULLSEL0_G1_18	PULLSEL0_G1_17	PULLSEL0_G1_16
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PULLSEL0_G1_15	PULLSEL0_G1_14	PULLSEL0_G1_13	PULLSEL0_G1_12	PULLSEL0_G1_11	PULLSEL0_G1_10	PULLSEL0_G1_9	PULLSEL0_G1_8	PULLSEL0_G1_7	PULLSEL0_G1_6	PULLSEL0_G1_5			PULLSEL0_G1_2	PULLSEL0_G1_1	PULLSEL0_G1_0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW			RW	RW	RW
Reset	0	1	0	1	1	1	1	1	1	1	1			0	0	0

Bit(s)	Mnemonic	Name	Description
27		PULLSEL0_G1_27	**Controls GPIO4 PULLSEL** 0: Disable pull control 1: Enable pull control
26		PULLSEL0_G1_26	**Controls GPIO3 PULLSEL** 0: Disable pull control 1: Enable pull control
25		PULLSEL0_G1_25	**Controls GPIO2 PULLSEL** 0: Disable pull control 1: Enable pull control
24		PULLSEL0_G1_24	**Controls GPIO1 PULLSEL** 0: Disable pull control 1: Enable pull control
23		PULLSEL0_G1_23	**Controls GPIO0 PULLSEL** 0: Disable pull control 1: Enable pull control
22		PULLSEL0_G1_22	**Controls GPIO64 PULLSEL** 0: Disable pull control 1: Enable pull control
21		PULLSEL0_G1_21	**Controls GPIO63 PULLSEL** 0: Disable pull control 1: Enable pull control

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Bit(s)	Mnemonic	Name	Description
20		PULLSEL0_G1_20	**Controls GPIO62 PULLSEL** 0: Disable pull control 1: Enable pull control
19		PULLSEL0_G1_19	**Controls GPIO61 PULLSEL** 0: Disable pull control 1: Enable pull control
18		PULLSEL0_G1_18	**Controls GPIO60 PULLSEL** 0: Disable pull control 1: Enable pull control
17		PULLSEL0_G1_17	**Controls GPIO59 PULLSEL** 0: Disable pull control 1: Enable pull control
16		PULLSEL0_G1_16	**Controls GPIO58 PULLSEL** 0: Disable pull control 1: Enable pull control
15		PULLSEL0_G1_15	**Controls GPIO57 PULLSEL** 0: Disable pull control 1: Enable pull control
14		PULLSEL0_G1_14	**Controls GPIO56 PULLSEL** 0: Disable pull control 1: Enable pull control
13		PULLSEL0_G1_13	**Controls GPIO55 PULLSEL** 0: Disable pull control 1: Enable pull control
12		PULLSEL0_G1_12	**Controls GPIO54 PULLSEL** 0: Disable pull control 1: Enable pull control
11		PULLSEL0_G1_11	**Controls GPIO53 PULLSEL** 0: Disable pull control 1: Enable pull control
10		PULLSEL0_G1_10	**Controls GPIO52 PULLSEL** 0: Disable pull control 1: Enable pull control
9		PULLSEL0_G1_9	**Controls GPIO51 PULLSEL** 0: Disable pull control 1: Enable pull control
8		PULLSEL0_G1_8	**Controls GPIO50 PULLSEL** 0: Disable pull control 1: Enable pull control
7		PULLSEL0_G1_7	**Controls GPIO49 PULLSEL** 0: Disable pull control 1: Enable pull control
6		PULLSEL0_G1_6	**Controls GPIO48 PULLSEL** 0: Disable pull control 1: Enable pull control
5		PULLSEL0_G1_5	**Controls GPIO47 PULLSEL** 0: Disable pull control 1: Enable pull control
2		PULLSEL0_G1_2	**Controls GPIO44 PULLSEL** 0: Disable pull control 1: Enable pull control
1		PULLSEL0_G1_1	**Controls GPIO43 PULLSEL** 0: Disable pull control

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Bit(s)	Mnemonic	Name	Description
			1: Enable pull control
0		PULLSEL0_G1_0	**Controls GPIO42 PULLSEL** 0: Disable pull control 1: Enable pull control

10211970 **GPIO_DRV0_G1** **GPIO Group 1 Driving Control Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DRV0_G1_7				DRV0_G1_6				DRV0_G1_5				DRV0_G1_4			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DRV0_G1_3				DRV0_G1_2				DRV0_G1_1				DRV0_G1_0			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		DRV0_G1_7	**Controls SRCLKENA1 PADs driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:1]: 00: 2mA 01: 4mA 10: 6mA 11: 8mA [0]: Reserved
27:24		DRV0_G1_6	**Controls SRCLKENAI PADs driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:1]: 00: 2mA 01: 4mA 10: 6mA 11: 8mA [0]: Reserved
23:20		DRV0_G1_5	**Controls I2C3 PADs driving selection** [0]: EA
19:16		DRV0_G1_4	**Controls I2C2 PADs driving selection** [0]: EA
15:12		DRV0_G1_3	**Controls I2C1 PADs driving selection** [0]: EA
11:8		DRV0_G1_2	**Controls I2C0 PADs driving selection** [0]: EA
7:4		DRV0_G1_1	**Controls CMMCLK PAD driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:0]: 000: 2mA 100: 4mA 010: 6mA

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Bit(s)	Mnemonic	Name	Description
			110: 8mA 001: 10mA 101: 12mA 011: 14mA 111: 16mA
3:0		DRV0_G1_0	**Controls DCAM PADs driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:1]: 00: 2mA 01: 4mA 10: 6mA 11: 8mA [0]: Reserved

10211974 **GPIO_DRV1_G1** **GPIO Group 1 Driving Control Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DRV0_G1_10				DRV0_G1_9				DRV0_G1_8			
Type					RW				RW				RW			
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:8		DRV0_G1_10	**Controls EINT0~4 PADs driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled. [2:1]: 00: 2mA 01: 4mA 10: 6mA 11: 8mA [0]: Reserved
7:4		DRV0_G1_9	**Controls PCM PADs driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:1]: 00: 2mA 01: 4mA 10: 6mA 11: 8mA [0]: Reserved
3:0		DRV0_G1_8	**Controls UART2/3 PADs driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:1]: 00: 2mA 01: 4mA

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Bit(s)	Mnemonic	Name	Description
			10: 6mA 11: 8mA [0]: Reserved

10211980 **GPIO_PUPD0_G1** **GPIO Group 1 Special IO PU/PD Control Register 0** **00000066**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										PUPD0_G1_1				PUPD0_G1_0		
Type										RW				RW		
Reset										1	1	0		1	1	0

Bit(s)	Mnemonic	Name	Description
6:4		PUPD0_G1_1	**Controls CMMCLK1 PAD PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K
2:0		PUPD0_G1_0	**Controls CMMCLK PAD PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K

10211A00 **GPIO_IES_G2** **GPIO Group 2 IES Control Register** **FFFF**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESERVE						IES_G2_9	IES_G2_8	IES_G2_7	IES_G2_6	IES_G2_5	IES_G2_4	IES_G2_3	IES_G2_2	IES_G2_1	IES_G2_0
Type	RW						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
15:10		RESERVE	**Reserved register**
9		IES_G2_9	**RFIC0/1 PADs input enable control** 0: Disable 1: Enable
8		IES_G2_8	**BPI5~20, C2KTXBPI PADs input enable control** 0: Disable 1: Enable
7		IES_G2_7	**KEYPAD PAD input enable control** 0: Disable 1: Enable
6		IES_G2_6	**EINT9~12 PADs input enable control** 0: Disable 1: Enable
5		IES_G2_5	**I2S PADs input enable control** 0: Disable 1: Enable

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Bit(s)	Mnemonic	Name	Description
4		IES_G2_4	**UART0/1 PADs input enable control** 0: Disable 1: Enable
3		IES_G2_3	**EINT5~8 PADs input enable control** 0: Disable 1: Enable
2		IES_G2_2	**JTAG PADs input enable control** 0: Disable 1: Enable
1		IES_G2_1	**DISP_PWM PAD input enable control** 0: Disable 1: Enable
0		IES_G2_0	**SPI PADs input enable control** 0: Disable 1: Enable

10211A10 **GPIO_SMT_G2** **GPIO Group 2 SMT Control Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SMT_G2_9	SMT_G2_8	SMT_G2_7	SMT_G2_6	SMT_G2_5	SMT_G2_4	SMT_G2_3	SMT_G2_2	SMT_G2_1	SMT_G2_0
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
9		SMT_G2_9	**Controls RFIC0/1 PADs Schmitt trigger** 0: Disable 1: Enable
8		SMT_G2_8	**Controls BPI5~20, C2KTXBPI PADs Schmitt trigger** 0: Disable 1: Enable
7		SMT_G2_7	**Controls KEYPAD PAD Schmitt trigger** 0: Disable 1: Enable
6		SMT_G2_6	**Controls EINT9~12 PADs Schmitt trigger** 0: Disable 1: Enable
5		SMT_G2_5	**Controls I2S PADs Schmitt trigger** 0: Disable 1: Enable
4		SMT_G2_4	**Controls UART0/1 PADs Schmitt trigger** 0: Disable 1: Enable
3		SMT_G2_3	**Controls EINT5~8 PADs Schmitt trigger** 0: Disable 1: Enable
2		SMT_G2_2	**Controls JTAG PADs Schmitt trigger** 0: Disable 1: Enable
1		SMT_G2_1	**Controls DISP_PWM PAD Schmitt trigger** 0: Disable

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Bit(s)	Mnemonic	Name	Description
			1: Enable
0		SMT_G2_0	**Controls SPI PADs Schmitt trigger** 0: Disable 1: Enable

10211A20 **GPIO_TDSEL0_G2** **GPIO Group 2 TDSEL Control Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDSEL0_G2_7				TDSEL0_G2_6				TDSEL0_G2_5				TDSEL0_G2_4			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDSEL0_G2_3				TDSEL0_G2_2				TDSEL0_G2_1				TDSEL0_G2_0			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		TDSEL0_G2_7	Controls KEYPAD PAD Tx delay selection
27:24		TDSEL0_G2_6	Controls EINT9~12 PADs Tx delay selection
23:20		TDSEL0_G2_5	Controls I2S PADs Tx delay selection
19:16		TDSEL0_G2_4	Controls UART0/1 PADs Tx delay selection
15:12		TDSEL0_G2_3	Controls EINT5~8 PADs Tx delay selection
11:8		TDSEL0_G2_2	Controls JTAG PADs Tx delay selection
7:4		TDSEL0_G2_1	Controls DISP_PWM PAD Tx delay selection
3:0		TDSEL0_G2_0	Controls SPI PADs Tx delay selection

10211A24 **GPIO_TDSEL1_G2** **GPIO Group 2 TDSEL Control Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TDSEL1_G2_1				TDSEL1_G2_0			
Type									RW				RW			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:4		TDSEL1_G2_1	Controls RFIC0/1 PADs Tx delay selection
3:0		TDSEL1_G2_0	Controls BPI5~20, C2KTXBPI PADs Tx delay selection

10211A28 **GPIO_RDSEL0_G2** **GPIO Group 2 RDSEL Control Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													RDSEL0_G2_9		RDSEL0_G2_8	

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Type													RW		RW	
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDSELo_G2_7		RDSELo_G2_6		RDSELo_G2_5		RDSELo_G2_4		RDSELo_G2_3		RDSELo_G2_2		RDSELo_G2_1		RDSELo_G2_0	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:18		RDSELo_G2_9	Controls RFIC0/1 PADs Rx delay selection
17:16		RDSELo_G2_8	Controls BPI5~20, C2KTXBPI PADs Rx delay selection
15:14		RDSELo_G2_7	Controls KEYPAD PAD Rx delay selection
13:12		RDSELo_G2_6	Controls EINT9~12 PADs Rx delay selection
11:10		RDSELo_G2_5	Controls I2S PADs Rx delay selection
9:8		RDSELo_G2_4	Controls UART0/1 PADs Rx delay selection
7:6		RDSELo_G2_3	Controls EINT5~8 PADs Rx delay selection
5:4		RDSELo_G2_2	Controls JTAG PADs Rx delay selection
3:2		RDSELo_G2_1	Controls DISP_PWM PAD Rx delay selection
1:0		RDSELo_G2_0	Controls SPI PADs Rx delay selection

10211A30 **GPIO_PULLENo_G2** **GPIO Group 2 PULLEN Control Register 0** **C0FFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PULLENo_G2_31	PULLENo_G2_30							PULLENo_G2_23	PULLENo_G2_22	PULLENo_G2_21	PULLENo_G2_20	PULLENo_G2_19	PULLENo_G2_18	PULLENo_G2_17	PULLENo_G2_16
Type	RW	RW							RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1							1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PULLENo_G2_15	PULLENo_G2_14	PULLENo_G2_13	PULLENo_G2_12	PULLENo_G2_11	PULLENo_G2_10	PULLENo_G2_9	PULLENo_G2_8	PULLENo_G2_7	PULLENo_G2_6	PULLENo_G2_5	PULLENo_G2_4	PULLENo_G2_3	PULLENo_G2_2	PULLENo_G2_1	PULLENo_G2_0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31		PULLENo_G2_31	**Controls GPIO88 PULLEN** 0: Disable pull control 1: Enable pull control
30		PULLENo_G2_30	**Controls GPIO87 PULLEN** 0: Disable pull control 1: Enable pull control
23		PULLENo_G2_23	**Controls GPIO12 PULLEN** 0: Disable pull control 1: Enable pull control
22		PULLENo_G2_22	**Controls GPIO11 PULLEN** 0: Disable pull control 1: Enable pull control
21		PULLENo_G2_21	**Controls GPIO10 PULLEN** 0: Disable pull control 1: Enable pull control

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Bit(s)	Mnemonic	Name	Description
20		PULLEN0_G2_20	**Controls GPIO9 PULLEN** 0: Disable pull control 1: Enable pull control
19		PULLEN0_G2_19	**Controls GPIO80 PULLEN** 0: Disable pull control 1: Enable pull control
18		PULLEN0_G2_18	**Controls GPIO79 PULLEN** 0: Disable pull control 1: Enable pull control
17		PULLEN0_G2_17	**Controls GPIO78 PULLEN** 0: Disable pull control 1: Enable pull control
16		PULLEN0_G2_16	**Controls GPIO77 PULLEN** 0: Disable pull control 1: Enable pull control
15		PULLEN0_G2_15	**Controls GPIO76 PULLEN** 0: Disable pull control 1: Enable pull control
14		PULLEN0_G2_14	**Controls GPIO75 PULLEN** 0: Disable pull control 1: Enable pull control
13		PULLEN0_G2_13	**Controls GPIO74 PULLEN** 0: Disable pull control 1: Enable pull control
12		PULLEN0_G2_12	**Controls GPIO8 PULLEN** 0: Disable pull control 1: Enable pull control
11		PULLEN0_G2_11	**Controls GPIO7 PULLEN** 0: Disable pull control 1: Enable pull control
10		PULLEN0_G2_10	**Controls GPIO6 PULLEN** 0: Disable pull control 1: Enable pull control
9		PULLEN0_G2_9	**Controls GPIO5 PULLEN** 0: Disable pull control 1: Enable pull control
8		PULLEN0_G2_8	**Controls GPIO73 PULLEN** 0: Disable pull control 1: Enable pull control
7		PULLEN0_G2_7	**Controls GPIO72 PULLEN** 0: Disable pull control 1: Enable pull control
6		PULLEN0_G2_6	**Controls GPIO71 PULLEN** 0: Disable pull control 1: Enable pull control
5		PULLEN0_G2_5	**Controls GPIO70 PULLEN** 0: Disable pull control 1: Enable pull control
4		PULLEN0_G2_4	**Controls GPIO69 PULLEN** 0: Disable pull control 1: Enable pull control
3		PULLEN0_G2_3	**Controls GPIO68 PULLEN** 0: Disable pull control

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Bit(s)	Mnemonic	Name	Description
			1: Enable pull control
2		PULLEN0_G2_2	**Controls GPIO67 PULLEN** 0: Disable pull control 1: Enable pull control
1		PULLEN0_G2_1	**Controls GPIO66 PULLEN** 0: Disable pull control 1: Enable pull control
0		PULLEN0_G2_0	**Controls GPIO65 PULLEN** 0: Disable pull control 1: Enable pull control

10211A40 **GPIO_PULLEN1_G2** **GPIO Group 2 PULLEN Control Register 1** **03FFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							PULLEN1_G2_25	PULLEN1_G2_24	PULLEN1_G2_23	PULLEN1_G2_22	PULLEN1_G2_21	PULLEN1_G2_20	PULLEN1_G2_19	PULLEN1_G2_18	PULLEN1_G2_17	PULLEN1_G2_16
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							1	1	1	1	1	1	1	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PULLEN1_G2_15	PULLEN1_G2_14	PULLEN1_G2_13	PULLEN1_G2_12	PULLEN1_G2_11	PULLEN1_G2_10	PULLEN1_G2_9	PULLEN1_G2_8	PULLEN1_G2_7	PULLEN1_G2_6	PULLEN1_G2_5	PULLEN1_G2_4	PULLEN1_G2_3	PULLEN1_G2_2	PULLEN1_G2_1	PULLEN1_G2_0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
25		PULLEN1_G2_25	**Controls GPIO114 PULLEN** 0: Disable pull control 1: Enable pull control
24		PULLEN1_G2_24	**Controls GPIO113 PULLEN** 0: Disable pull control 1: Enable pull control
23		PULLEN1_G2_23	**Controls GPIO112 PULLEN** 0: Disable pull control 1: Enable pull control
22		PULLEN1_G2_22	**Controls GPIO111 PULLEN** 0: Disable pull control 1: Enable pull control
21		PULLEN1_G2_21	**Controls GPIO110 PULLEN** 0: Disable pull control 1: Enable pull control
20		PULLEN1_G2_20	**Controls GPIO109 PULLEN** 0: Disable pull control 1: Enable pull control
19		PULLEN1_G2_19	**Controls GPIO108 PULLEN** 0: Disable pull control 1: Enable pull control
18		PULLEN1_G2_18	**Controls GPIO107 PULLEN** 0: Disable pull control 1: Enable pull control

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Bit(s)	Mnemonic	Name	Description
17		PULLEN1_G2_17	**Controls GPIO106 PULLEN** 0: Disable pull control 1: Enable pull control
16		PULLEN1_G2_16	**Controls GPIO105 PULLEN** 0: Disable pull control 1: Enable pull control
15		PULLEN1_G2_15	**Controls GPIO104 PULLEN** 0: Disable pull control 1: Enable pull control
14		PULLEN1_G2_14	**Controls GPIO103 PULLEN** 0: Disable pull control 1: Enable pull control
13		PULLEN1_G2_13	**Controls GPIO102 PULLEN** 0: Disable pull control 1: Enable pull control
12		PULLEN1_G2_12	**Controls GPIO101 PULLEN** 0: Disable pull control 1: Enable pull control
11		PULLEN1_G2_11	**Controls GPIO100 PULLEN** 0: Disable pull control 1: Enable pull control
10		PULLEN1_G2_10	**Controls GPIO99 PULLEN** 0: Disable pull control 1: Enable pull control
9		PULLEN1_G2_9	**Controls GPIO98 PULLEN** 0: Disable pull control 1: Enable pull control
8		PULLEN1_G2_8	**Controls GPIO97 PULLEN** 0: Disable pull control 1: Enable pull control
7		PULLEN1_G2_7	**Controls GPIO96 PULLEN** 0: Disable pull control 1: Enable pull control
6		PULLEN1_G2_6	**Controls GPIO95 PULLEN** 0: Disable pull control 1: Enable pull control
5		PULLEN1_G2_5	**Controls GPIO94 PULLEN** 0: Disable pull control 1: Enable pull control
4		PULLEN1_G2_4	**Controls GPIO93 PULLEN** 0: Disable pull control 1: Enable pull control
3		PULLEN1_G2_3	**Controls GPIO92 PULLEN** 0: Disable pull control 1: Enable pull control
2		PULLEN1_G2_2	**Controls GPIO91 PULLEN** 0: Disable pull control 1: Enable pull control
1		PULLEN1_G2_1	**Controls GPIO90 PULLEN** 0: Disable pull control 1: Enable pull control
0		PULLEN1_G2_0	**Controls GPIO89 PULLEN**

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Bit(s)	Mnemonic	Name	Description
			0: Disable pull control 1: Enable pull control

10211A50 **GPIO_PULLSEL0_G2** **GPIO Group 2 PULLSEL Control Register 0** **000061E0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PULLSEL0_G2_31	PULLSEL0_G2_30							PULLSEL0_G2_23	PULLSEL0_G2_22	PULLSEL0_G2_21	PULLSEL0_G2_20	PULLSEL0_G2_19	PULLSEL0_G2_18	PULLSEL0_G2_17	PULLSEL0_G2_16
Type	RW	RW							RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0							0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PULLSEL0_G2_15	PULLSEL0_G2_14	PULLSEL0_G2_13	PULLSEL0_G2_12	PULLSEL0_G2_11	PULLSEL0_G2_10	PULLSEL0_G2_9	PULLSEL0_G2_8	PULLSEL0_G2_7	PULLSEL0_G2_6	PULLSEL0_G2_5	PULLSEL0_G2_4	PULLSEL0_G2_3	PULLSEL0_G2_2	PULLSEL0_G2_1	PULLSEL0_G2_0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	1	1	0	0	0	0	1	1	1	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		PULLSEL0_G2_31	**Controls GPIO88 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
30		PULLSEL0_G2_30	**Controls GPIO87 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
23		PULLSEL0_G2_23	**Controls GPIO12 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
22		PULLSEL0_G2_22	**Controls GPIO11 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
21		PULLSEL0_G2_21	**Controls GPIO10 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
20		PULLSEL0_G2_20	**Controls GPIO9 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
19		PULLSEL0_G2_19	**Controls GPIO80 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
18		PULLSEL0_G2_18	**Controls GPIO79 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
17		PULLSEL0_G2_17	**Controls GPIO78 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
16		PULLSEL0_G2_16	**Controls GPIO77 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
15		PULLSEL0_G2_15	**Controls GPIO76 PULLSEL** 0: Pull down if PULLEN = 1

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Bit(s)	Mnemonic	Name	Description
			1: Pull up if PULLEN = 1
14		PULLSEL0_G2_14	**Controls GPIO75 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
13		PULLSEL0_G2_13	**Controls GPIO74 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
12		PULLSEL0_G2_12	**Controls GPIO8 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
11		PULLSEL0_G2_11	**Controls GPIO7 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
10		PULLSEL0_G2_10	**Controls GPIO6 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
9		PULLSEL0_G2_9	**Controls GPIO5 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
8		PULLSEL0_G2_8	**Controls GPIO73 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
7		PULLSEL0_G2_7	**Controls GPIO72 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
6		PULLSEL0_G2_6	**Controls GPIO71 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
5		PULLSEL0_G2_5	**Controls GPIO70 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
4		PULLSEL0_G2_4	**Controls GPIO69 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
3		PULLSEL0_G2_3	**Controls GPIO68 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
2		PULLSEL0_G2_2	**Controls GPIO67 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
1		PULLSEL0_G2_1	**Controls GPIO66 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
0		PULLSEL0_G2_0	**Controls GPIO65 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1

10211A60 **GPIO_PULLSEL1_G2** **GPIO Group 2 PULLSEL Control Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name							PULL SEL1 _G2_ 25	PULL SEL1 _G2_ 24	PULL SEL1 _G2_ 23	PULL SEL1 _G2_ 22	PULL SEL1 _G2_ 21	PULL SEL1 _G2_ 20	PULL SEL1 _G2_ 19	PULL SEL1 _G2_ 18	PULL SEL1 _G2_ 17	PULL SEL1 _G2_ 16
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PULL SEL1 _G2_ 15	PULL SEL1 _G2_ 14	PULL SEL1 _G2_ 13	PULL SEL1 _G2_ 12	PULL SEL1 _G2_ 11	PULL SEL1 _G2_ 10	PULL SEL1 _G2_ 9	PULL SEL1 _G2_ 8	PULL SEL1 _G2_ 7	PULL SEL1 _G2_ 6	PULL SEL1 _G2_ 5	PULL SEL1 _G2_ 4	PULL SEL1 _G2_ 3	PULL SEL1 _G2_ 2	PULL SEL1 _G2_ 1	PULL SEL1 _G2_ 0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
25		PULLSEL1_G2_25	**Controls GPIO114 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
24		PULLSEL1_G2_24	**Controls GPIO113 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
23		PULLSEL1_G2_23	**Controls GPIO112 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
22		PULLSEL1_G2_22	**Controls GPIO111 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
21		PULLSEL1_G2_21	**Controls GPIO110 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
20		PULLSEL1_G2_20	**Controls GPIO109 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
19		PULLSEL1_G2_19	**Controls GPIO108 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
18		PULLSEL1_G2_18	**Controls GPIO107 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
17		PULLSEL1_G2_17	**Controls GPIO106 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
16		PULLSEL1_G2_16	**Controls GPIO105 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
15		PULLSEL1_G2_15	**Controls GPIO104 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
14		PULLSEL1_G2_14	**Controls GPIO103 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
13		PULLSEL1_G2_13	**Controls GPIO102 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
12		PULLSEL1_G2_12	**Controls GPIO101 PULLSEL** 0: Pull down if PULLEN = 1

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Bit(s)	Mnemonic	Name	Description
			1: Pull up if PULLEN = 1
11		PULLSEL1_G2_11	**Controls GPIO100 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
10		PULLSEL1_G2_10	**Controls GPIO99 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
9		PULLSEL1_G2_9	**Controls GPIO98 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
8		PULLSEL1_G2_8	**Controls GPIO97 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
7		PULLSEL1_G2_7	**Controls GPIO96 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
6		PULLSEL1_G2_6	**Controls GPIO95 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
5		PULLSEL1_G2_5	**Controls GPIO94 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
4		PULLSEL1_G2_4	**Controls GPIO93 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
3		PULLSEL1_G2_3	**Controls GPIO92 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
2		PULLSEL1_G2_2	**Controls GPIO91 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
1		PULLSEL1_G2_1	**Controls GPIO90 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
0		PULLSEL1_G2_0	**Controls GPIO89 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1

10211A70 **GPIO_DRV0_G2** **GPIO Group 2 Driving Control Register 0** **00000600**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DRV0_G2_7				DRV0_G2_6				DRV0_G2_5				DRV0_G2_4			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DRV0_G2_3				DRV0_G2_2				DRV0_G2_1				DRV0_G2_0			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		DRV0_G2_7	**Controls KEYPAD PAD driving selection**

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Bit(s)	Mnemonic	Name	Description
			[3]: Output slew rate control 1: Slower slew 0: N slew rate controlled [2:1]: 00: 2mA 01: 4mA 10: 6mA 11: 8mA [0]: Reserved
27:24		DRV0_G2_6	**Controls EINT9~12 PADs driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:1]: 00: 2mA 01: 4mA 10: 6mA 11: 8mA [0]: Reserved
23:20		DRV0_G2_5	**Controls I2S PADs driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:1]: 00: 2mA 01 : 4mA 10 : 6mA 11 : 8mA [0]: Reserved
19:16		DRV0_G2_4	**Controls UART0/1 PAD driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:1]: 00: 4mA 01: 8mA 10: 12mA 11: 16mA [0]: Reserved
15:12		DRV0_G2_3	**Controls EINT5~8 PADs driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:1]: 00: 4mA 01: 8mA 10: 12mA 11: 16mA [0]: Reserved
11:8		DRV0_G2_2	**Controls JTAG PADs driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:1]: 00: 4mA 01: 8mA 10: 12mA 11: 16mA

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Bit(s)	Mnemonic	Name	Description
			[0]: Reserved
7:4		DRV0_G2_1	**Controls DISP_PWM PADs driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:1]: 00: 4mA 01: 8mA 10: 12mA 11: 16mA [0]: Reserved
3:0		DRV0_G2_0	**Controls SPI PADs driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:1]: 00: 4mA 01: 8mA 10: 12mA 11: 16mA [0]: Reserved

10211A74 **GPIO_DRV1_G2** **GPIO Group 2 Driving Control Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**DRV1_G2_1**				**DRV1_G2_0**			
Type									RW				RW			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:4		DRV1_G2_1	**Controls RFIC0/1 PADs driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:1]: 00: 2mA 01: 4mA 10: 6mA 11: 8mA [0]: Reserved
3:0		DRV1_G2_0	**Controls BPI5~20, C2KTXBPI PADs driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:1]: 00: 4mA 01: 8mA 10: 12mA 11: 16mA [0]: Reserved

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10211A80 **GPIO_PUPD0_G2** **GPIO Group 2 Special IO PU/PD Control Register 0** **06620666**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						PUPD0_G2_5				PUPD0_G2_4				PUPD0_G2_3		
Type						RW				RW				RW		
Reset						1	1	0		1	1	0		0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						PUPD0_G2_2				PUPD0_G2_1				PUPD0_G2_0		
Type						RW				RW				RW		
Reset						1	1	0		1	1	0		1	1	0

Bit(s)	Mnemonic	Name	Description
26:24		PUPD0_G2_5	**Controls KPCOL2 PAD PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K
22:20		PUPD0_G2_4	**Controls KPCOL1 PAD PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K
18:16		PUPD0_G2_3	**Controls KPCOL0 PAD PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K
10:8		PUPD0_G2_2	**Controls KPROW2 PAD PUPD** [2] : PUPD [1] : R1 [0] : R0
6:4		PUPD0_G2_1	**Controls KPROW1 PAD PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K
2:0		PUPD0_G2_0	**Controls KPROW0 PAD PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K

10211B00 **GPIO_IES_G3** **GPIO Group 3 IES Control Register** **FF**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RESERVE		IES_G3_5	IES_G3_4	IES_G3_3	IES_G3_2	IES_G3_1	IES_G3_0
Type									RW		RW	RW	RW	RW	RW	RW
Reset									1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
7:6		RESERVE	**Reserved register**
5		IES_G3_5	**SRCLKENA0 PADs input enable control** 0: Disable 1: Enable
4		IES_G3_4	**LCM_RST, DSI_TE PADs input enable control**

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Bit(s)	Mnemonic	Name	Description
			0: Disable 1: Enable
3		IES_G3_3	**Audio PADs input enable control** 0: Disable 1: Enable
2		IES_G3_2	**PWRAP PADs input enable control** 0: Disable 1: Enable
1		IES_G3_1	**RTC32K, WATCHDOG PADs input enable control** 0: Disable 1: Enable
0		IES_G3_0	**LTE_TXBPI, BPI0~4, 21~27, PAVM, RFIC_MIPI PADs input enable control** 0: Disable 1: Enable

10211B10 **GPIO_SMT_G3** **GPIO Group 3 SMT Control Register** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											SMT_G3_5	SMT_G3_4	SMT_G3_3	SMT_G3_2	SMT_G3_1	SMT_G3_0
Type											RW	RW	RW	RW	RW	RW
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5		SMT_G3_5	**Controls SRCLKENA0 PADs Schmitt trigger** 0: Disable 1: Enable
4		SMT_G3_4	**Controls LCM_RST, DSI_TE PADs Schmitt trigger** 0: Disable 1: Enable
3		SMT_G3_3	**Controls audio PADs Schmitt trigger** 0: Disable 1: Enable
2		SMT_G3_2	**Controls PWRAP PADs Schmitt trigger** 0: Disable 1: Enable
1		SMT_G3_1	**Controls RTC32K, WATCHDOG PADs Schmitt trigger** 0: Disable 1: Enable
0		SMT_G3_0	**Controls LTE_TXBPI, BPI0~4, 21~27, PAVM, RFIC_MIPI PADs Schmitt trigger** 0: Disable 1: Enable

10211B20 **GPIO_TDSEL0_G3** **GPIO Group 3 TDSEL Control Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									TDSEL0_G3_5				TDSEL0_G3_4			

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Type									RW				RW			
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TDSEL0_G3_3**				**TDSEL0_G3_2**				**TDSEL0_G3_1**				**TDSEL0_G3_0**			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:20		TDSEL0_G3_5	Controls SRCLKENA0 PADsTx delay selection
19:16		TDSEL0_G3_4	Controls LCM_RST, DSI_TE PADs Tx delay selection
15:12		TDSEL0_G3_3	Controls audio PADsTx delay selection
11:8		TDSEL0_G3_2	Controls PWRAP PADsTx delay selection
7:4		TDSEL0_G3_1	Controls RTC32K, WATCHDOG PADsTx delay selection
3:0		TDSEL0_G3_0	Controls LTE_TXBPI, BPI0~4, 21~27, PAVM, RFIC_MIPI PADsTx delay selection

10211B28 GPIO_RDSEL0_G3 GPIO Group 3 RDSEL Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RDSEL0_G3_5**		**RDSEL0_G3_4**		**RDSEL0_G3_3**		**RDSEL0_G3_2**		**RDSEL0_G3_1**		**RDSEL0_G3_0**	
Type					RW		RW		RW		RW		RW		RW	
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:10		RDSEL0_G3_5	Controls SRCLKENA0 PADsRx delay selection
9:8		RDSEL0_G3_4	Controls LCM_RST, DSI_TE PADs Rx delay selection
7:6		RDSEL0_G3_3	Controls audio PADsRx delay selection
5:4		RDSEL0_G3_2	Controls PWRAP PADsRx delay selection
3:2		RDSEL0_G3_1	Controls RTC32K, WATCHDOG PADsRx delay selection
1:0		RDSEL0_G3_0	Controls LTE_TXBPI, BPI0~4, 21~27, PAVM, RFIC_MIPI PADsRx delay selection

10211B30 GPIO_PULLEN0_G3 GPIO Group 3 PULLEN Control Register 0 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**PULLEN0_G3_31**	**PULLEN0_G3_30**	**PULLEN0_G3_29**	**PULLEN0_G3_28**	**PULLEN0_G3_27**	**PULLEN0_G3_26**	**PULLEN0_G3_25**	**PULLEN0_G3_24**	**PULLEN0_G3_23**	**PULLEN0_G3_22**	**PULLEN0_G3_21**	**PULLEN0_G3_20**	**PULLEN0_G3_19**	**PULLEN0_G3_18**	**PULLEN0_G3_17**	**PULLEN0_G3_16**
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**PULLEN0_G3_15**	**PULLEN0_G3_14**	**PULLEN0_G3_13**	**PULLEN0_G3_12**	**PULLEN0_G3_11**	**PULLEN0_G3_10**	**PULLEN0_G3_9**	**PULLEN0_G3_8**	**PULLEN0_G3_7**	**PULLEN0_G3_6**	**PULLEN0_G3_5**	**PULLEN0_G3_4**	**PULLEN0_G3_3**	**PULLEN0_G3_2**	**PULLEN0_G3_1**	**PULLEN0_G3_0**
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

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Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31		PULLEN0_G3_31	**Controls GPIO149 PULLEN** 0: Disable pull control 1: Enable pull control
30		PULLEN0_G3_30	**Controls GPIO148 PULLEN** 0: Disable pull control 1: Enable pull control
29		PULLEN0_G3_29	**Controls GPIO147 PULLEN** 0: Disable pull control 1: Enable pull control
28		PULLEN0_G3_28	**Controls GPIO146 PULLEN** 0: Disable pull control 1: Enable pull control
27		PULLEN0_G3_27	**Controls GPIO145 PULLEN** 0: Disable pull control 1: Enable pull control
26		PULLEN0_G3_26	**Controls GPIO144 PULLEN** 0: Disable pull control 1: Enable pull control
25		PULLEN0_G3_25	**Controls GPIO143 PULLEN** 0: Disable pull control 1: Enable pull control
24		PULLEN0_G3_24	**Controls GPIO142 PULLEN** 0: Disable pull control 1: Enable pull control
23		PULLEN0_G3_23	**Controls GPIO141 PULLEN** 0: Disable pull control 1: Enable pull control
22		PULLEN0_G3_22	**Controls GPIO140 PULLEN** 0: Disable pull control 1: Enable pull control
21		PULLEN0_G3_21	**Controls GPIO139 PULLEN** 0: Disable pull control 1: Enable pull control
20		PULLEN0_G3_20	**Controls GPIO138 PULLEN** 0: Disable pull control 1: Enable pull control
19		PULLEN0_G3_19	**Controls GPIO137 PULLEN** 0: Disable pull control 1: Enable pull control
18		PULLEN0_G3_18	**Controls GPIO136 PULLEN** 0: Disable pull control 1: Enable pull control
17		PULLEN0_G3_17	**Controls GPIO135 PULLEN** 0: Disable pull control 1: Enable pull control
16		PULLEN0_G3_16	**Controls GPIO134 PULLEN** 0: Disable pull control 1: Enable pull control
15		PULLEN0_G3_15	**Controls GPIO133 PULLEN** 0: Disable pull control

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Bit(s)	Mnemonic	Name	Description
			1: Enable pull control
14		PULLEN0_G3_14	**Controls GPIO132 PULLEN** 0: Disable pull control 1: Enable pull control
13		PULLEN0_G3_13	**Controls GPIO131 PULLEN** 0: Disable pull control 1: Enable pull control
12		PULLEN0_G3_12	**Controls GPIO130 PULLEN** 0: Disable pull control 1: Enable pull control
11		PULLEN0_G3_11	**Controls GPIO129 PULLEN** 0: Disable pull control 1: Enable pull control
10		PULLEN0_G3_10	**Controls GPIO128 PULLEN** 0: Disable pull control 1: Enable pull control
9		PULLEN0_G3_9	**Controls GPIO127 PULLEN** 0: Disable pull control 1: Enable pull control
8		PULLEN0_G3_8	**Controls GPIO126 PULLEN** 0: Disable pull control 1: Enable pull control
7		PULLEN0_G3_7	**Controls GPIO125 PULLEN** 0: Disable pull control 1: Enable pull control
6		PULLEN0_G3_6	**Controls GPIO124 PULLEN** 0: Disable pull control 1: Enable pull control
5		PULLEN0_G3_5	**Controls GPIO123 PULLEN** 0: Disable pull control 1: Enable pull control
4		PULLEN0_G3_4	**Controls GPIO122 PULLEN** 0: Disable pull control 1: Enable pull control
3		PULLEN0_G3_3	**Controls GPIO121 PULLEN** 0: Disable pull control 1: Enable pull control
2		PULLEN0_G3_2	**Controls GPIO120 PULLEN** 0: Disable pull control 1: Enable pull control
1		PULLEN0_G3_1	**Controls GPIO119 PULLEN** 0: Disable pull control 1: Enable pull control
0		PULLEN0_G3_0	**Controls GPIO118 PULLEN** 0: Disable pull control 1: Enable pull control

10211B50 **GPIO_PULLSEL0_G3** **GPIO Group 3 PULLSEL Control Register0** **41000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	PULLSEL0_G3_31	PULLSEL0_G3_30	PULLSEL0_G3_29	PULLSEL0_G3_28	PULLSEL0_G3_27	PULLSEL0_G3_26	PULLSEL0_G3_25	PULLSEL0_G3_24	PULLSEL0_G3_23	PULLSEL0_G3_22	PULLSEL0_G3_21	PULLSEL0_G3_20	PULLSEL0_G3_19	PULLSEL0_G3_18	PULLSEL0_G3_17	PULLSEL0_G3_16
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PULLSEL0_G3_15	PULLSEL0_G3_14	PULLSEL0_G3_13	PULLSEL0_G3_12	PULLSEL0_G3_11	PULLSEL0_G3_10	PULLSEL0_G3_9	PULLSEL0_G3_8	PULLSEL0_G3_7	PULLSEL0_G3_6	PULLSEL0_G3_5	PULLSEL0_G3_4	PULLSEL0_G3_3	PULLSEL0_G3_2	PULLSEL0_G3_1	PULLSEL0_G3_0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		PULLSEL0_G3_31	**Controls GPIO149 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
30		PULLSEL0_G3_30	**Controls GPIO148 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
29		PULLSEL0_G3_29	**Controls GPIO147 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
28		PULLSEL0_G3_28	**Controls GPIO146 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
27		PULLSEL0_G3_27	**Controls GPIO145 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
26		PULLSEL0_G3_26	**Controls GPIO144 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
25		PULLSEL0_G3_25	**Controls GPIO143 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
24		PULLSEL0_G3_24	**Controls GPIO142 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
23		PULLSEL0_G3_23	**Controls GPIO141 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
22		PULLSEL0_G3_22	**Controls GPIO140 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
21		PULLSEL0_G3_21	**Controls GPIO139 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
20		PULLSEL0_G3_20	**Controls GPIO138 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
19		PULLSEL0_G3_19	**Controls GPIO137 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
18		PULLSEL0_G3_18	**Controls GPIO136 PULLSEL** 0: Pull down if PULLEN = 1

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Bit(s)	Mnemonic	Name	Description
			1: Pull up if PULLEN = 1
17		PULLSEL0_G3_17	**Controls GPIO135 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
16		PULLSEL0_G3_16	**Controls GPIO134 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
15		PULLSEL0_G3_15	**Controls GPIO133 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
14		PULLSEL0_G3_14	**Controls GPIO132 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
13		PULLSEL0_G3_13	**Controls GPIO131 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
12		PULLSEL0_G3_12	**Controls GPIO130 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
11		PULLSEL0_G3_11	**Controls GPIO129 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
10		PULLSEL0_G3_10	**Controls GPIO128 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
9		PULLSEL0_G3_9	**Controls GPIO127 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
8		PULLSEL0_G3_8	**Controls GPIO126 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
7		PULLSEL0_G3_7	**Controls GPIO125 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
6		PULLSEL0_G3_6	**Controls GPIO124 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
5		PULLSEL0_G3_5	**Controls GPIO123 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
4		PULLSEL0_G3_4	**Controls GPIO122 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
3		PULLSEL0_G3_3	**Controls GPIO121 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
2		PULLSEL0_G3_2	**Controls GPIO120 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1
1		PULLSEL0_G3_1	**Controls GPIO119 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1

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Bit(s)	Mnemonic	Name	Description
0		PULLSEL0_G3_0	**Controls GPIO118 PULLSEL** 0: Pull down if PULLEN = 1 1: Pull up if PULLEN = 1

10211B70 **GPIO_DRV0_G3** **GPIO Group 3 Driving Control Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									SRCLKENA0 PADs Input Enable Control				LCM_RST, DSI_TE PADs Input Enable Control			
Type									RW				RW			
Reset									0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Audio PADs Input Enable Control				PWRAP PADs Input Enable Control				RTC32K, WATCHDOG PADs Input Enable Control				LTE_TXBPI, BPI0~4, 21~27, PAVM, RFIC_MIPI PADs Input Enable Control			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:20	**SRCLKENA0 PADs Input Enable Control**	DRV0_G3_5	**Controls SRCLKENA0 PADs driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:1]: 00: 2mA 01: 4mA 10: 6mA 11: 8mA [0]: Reserved
19:16	**LCM_RST, DSI_TE PADs Input Enable Control**	DRV0_G3_4	**Controls LCM_RST, DSI_TE PADs driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:1]: 00: 2mA 01: 4mA 10: 6mA 11: 8mA [0]: Reserved
15:12	**Audio PADs Input Enable Control**	DRV0_G3_3	**Controls audio PADs driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:1]: 00: 2mA 01: 4mA 10: 6mA 11: 8mA [0]: Reserved
11:8	**PWRAP PADs Input Enable Control**	DRV0_G3_2	**Controls PWRAP PADs driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled

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Bit(s)	Mnemonic	Name	Description
			[2:1]: 00: 2mA 01: 4mA 10: 6mA 11: 8mA [0]: Reserved
7:4	**RTC32K, WATCHDOG PADs Input Enable Control**	DRV0_G3_1	**Controls RTC32K, WATCHDOG PADs driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:1]: 00: 2mA 01: 4mA 10: 6mA 11: 8mA [0]: Reserved
3:0	**LTE_TXBPI, BPI0~4, 21~27, PAVM, RFIC_MIPI PADs Input Enable Control**	DRV0_G3_0	**Controls LTE_TXBPI, BPI0~4, 21~27, PAVM, RFIC_MIPI PADs driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:1]: 00: 2mA 01: 4mA 10: 6mA 11: 8mA [0]: Reserved

10211C00 GPIO_IES_G4 GPIO Group 4 IES Control Register 00FF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RESERVE			IES_G4_4	IES_G4_3	IES_G4_2	IES_G4_1	IES_G4_0
Type									RW			RW	RW	RW	RW	RW
Reset									1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
7:5		RESERVE	**Reserved register**
4		IES_G4_4	**MSDC1 DATA PADs input enable control** 0: Disable 1: Enable
3		IES_G4_3	**MSDC1 CLK PADs input enable control** 0: Disable 1: Enable
2		IES_G4_2	**MSDC1 CMD PADs input enable control** 0: Disable 1: Enable
1		IES_G4_1	**SIM1 PADs input enable control** 0: Disable 1: Enable
0		IES_G4_0	**SIM2 PADs input enable control** 0: Disable 1: Enable

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10211C10 **GPIO_SMT_G4** **GPIO Group 4 SMT Control Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												SMT_G4_4	SMT_G4_3	SMT_G4_2	SMT_G4_1	SMT_G4_0
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4		SMT_G4_4	**MSDC1 DATA PADs Schmitt Trigger Control** 0: Disable 1: Enable
3		SMT_G4_3	**MSDC1 CLK PADs Schmitt Trigger Control** 0: Disable 1: Enable
2		SMT_G4_2	**MSDC1 CMD PADs Schmitt Trigger Control** 0: Disable 1: Enable
1		SMT_G4_1	**SIM1 PADs Schmitt Trigger Control** 0: Disable 1: Enable
0		SMT_G4_0	**SIM2 PADs Schmitt Trigger Control** 0: Disable 1: Enable

10211C20 **GPIO_TDSEL0_G4** **GPIO Group 4 TDSEL Control Register 0** **000AAAAA**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													TDSEL0_G4_4			
Type													RW			
Reset													1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDSEL0_G4_3				TDSEL0_G4_2				TDSEL0_G4_1				TDSEL0_G4_0			
Type	RW				RW				RW				RW			
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
19:16		TDSEL0_G4_4	Controls MSDC1 DATA PADsTx delay selection
15:12		TDSEL0_G4_3	Controls MSDC1 CLK PADsTx delay selection
11:8		TDSEL0_G4_2	Controls MSDC1 CMD PADsTx delay selection
7:4		TDSEL0_G4_1	Controls SIM1 PADsTx delay selection
3:0		TDSEL0_G4_0	Controls SIM2 PADsTx delay selection

10211C28 **GPIO_RDSEL0_G4** **GPIO Group 4 RDSEL Control Register 0** **0C30C000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RDSEL0_G4_4						RDSEL0_G4_3						RDSEL0_G4_2[5:4]	

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Type			RW						RW						RW	
Reset			0	0	1	1	0	0	0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDSEL0_G4_2[3:0]				RDSEL0_G4_1						RDSEL0_G4_0					
Type	RW				RW						RW					
Reset	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:24		RDSEL0_G4_4	Controls MSDC1 DATA PADsRx delay selection
23:18		RDSEL0_G4_3	Controls MSDC1 CLK PADsRx delay selection
17:12		RDSEL0_G4_2	Controls MSDC1 CMD PADsRx delay selection
11:6		RDSEL0_G4_1	Controls SIM1 PADsRx delay selection
5:0		RDSEL0_G4_0	Controls SIM2 PADsRx delay selection

10211C70 **GPIO_DRV0_G4** **GPIO Group 4 Driving Control Register 0** **00077711**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													MSDC1 DATA PADs Input Enable Control			
Type													RW			
Reset													0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC1 CLK PADs Input Enable Control				MSDC1 CMD PADs Input Enable Control				SIM1 PADs Input Enable Control				SIM2 PADs Input Enable Control			
Type	RW				RW				RW				RW			
Reset	0	1	1	1	0	1	1	1	0	0	0	1	0	0	0	1

Bit(s)	Mnemonic	Name	Description
19:16	**MSDC1 DATA PADs Input Enable Control**	DRV0_G4_4	**Controls MSDC1 DATA PADs Driving Selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:0]: 000: 2mA 100: 4mA 010: 6mA 110: 8mA 001: 10mA 101: 12mA 011: 14mA 111: 16mA
15:12	**MSDC1 CLK PADs Input Enable Control**	DRV0_G4_3	**Controls MSDC1 CLK PADs Driving Selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:0]: 000: 2mA 100: 4mA 010: 6mA 110: 8mA 001: 10mA 101: 12mA 011: 14mA 111: 16mA
11:8	**MSDC1**	DRV0_G4_2	**Controls MSDC1 CMD PADs Driving Selection**

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Bit(s)	Mnemonic	Name	Description
	CMD PADs Input Enable Control		[3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:0]: 000: 2mA 100: 4mA 010: 6mA 110: 8mA 001: 10mA 101: 12mA 011: 14mA 111: 16mA
7:4	**SIM1 PADs Input Enable Control**	DRV0_G4_1	**Controls SIM1 PADs Driving Selection** [3]: SR[0]; SIM Mode: SR[1:0]=[10] or [11] GPIO Mode: SR[1:0]=[01] or [00] [2:1]: 00: 1.5mA 01: 3mA 10: 4.5mA 11: 6mA [0]: SR[1]
3:0	**SIM2 PADs Input Enable Control**	DRV0_G4_0	**Controls SIM2 PADs Driving Selection** [3]: SR[0]; SIM Mode: SR[1:0]=[10] or [11] GPIO Mode: SR[1:0]=[01] or [00] [2:1]: 00: 1.5mA 01: 3mA 10: 4.5mA 11: 6mA [0]: SR[1]

10211C80 **GPIO_PUPD0_G4** **GPIO Group 4 Special IO PU/PD Control Register 0** **05222262**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**PUPD0_G4_6**					**PUPD0_G4_5**				**PUPD0_G4_4**		
Type					RW					RW				RW		
Reset					0	1	0	1		0	1	0		0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**PUPD0_G4_3**				**PUPD0_G4_2**				**PUPD0_G4_1**				**PUPD0_G4_0**		
Type		RW				RW				RW				RW		
Reset		0	1	0		0	1	0		1	1	0		0	1	0

Bit(s)	Mnemonic	Name	Description
27:24		PUPD0_G4_6	**Controls MSDC1 BIAS PAD TUNE** TUNE[3:0]
22:20		PUPD0_G4_5	**Controls MSDC1 DATA3 PAD PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K
18:16		PUPD0_G4_4	**Controls MSDC1 DATA2 PAD PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K
14:12		PUPD0_G4_3	**Controls MSDC1 DATA1 PAD PUPD** [2]: 0: Pull up; 1: Pull down

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Bit(s)	Mnemonic	Name	Description
			[1]: 50K [0]: 10K
10:8		PUPD0_G4_2	**Controls MSDC1 DATA0 PAD PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K
6:4		PUPD0_G4_1	**Controls MSDC1 CLK PAD PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K
2:0		PUPD0_G4_0	**Controls MSDC1 CMD PAD PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K

10211C90 **GPIO_PUPD1_G4** **GPIO Group 4 Special IO PU/PD Control Register 1** **56665666**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PUPD1_G4_7				PUPD1_G4_6				PUPD1_G4_5				PUPD1_G4_4			
Type	RW				RW				RW				RW			
Reset	0	1	0	1	0	1	1	0	0	1	1	0	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PUPD1_G4_3				PUPD1_G4_2				PUPD1_G4_1				PUPD1_G4_0			
Type	RW				RW				RW				RW			
Reset	0	1	0	1	0	1	1	0	0	1	1	0	0	1	1	0

Bit(s)	Mnemonic	Name	Description
31:28		PUPD1_G4_7	**Controls SIM1 BIAS PAD TUNE** TUNE[3:0]
27:24		PUPD1_G4_6	**Controls SIM1 SIO PAD PUPD** [3]: INS [2:0] : 001 : Pull up 45K 010 : Pull up 5K 011 : Pull up 5K/45K 100 : Pull down 75K 110 : pull down 75K
23:20		PUPD1_G4_5	**Controls SIM1 SRST PAD PUPD** [3]: INS [2:0] : 001 : Pull up 45K 010 : Pull up 5K 011 : Pull up 5K/45K 100 : Pull down 75K 110 : pull down 75K
19:16		PUPD1_G4_4	**Controls SIM1 SCLK PAD PUPD** [3]: INS [2:0] : 001 : Pull up 45K 010 : Pull up 5K 011 : Pull up 5K/45K 100 : Pull down 75K 110 : pull down 75K
15:12		PUPD1_G4_3	**Controls SIM2 BIAS PAD TUNE**

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Bit(s)	Mnemonic	Name	Description
			TUNE[3:0]
11:8		PUPD1_G4_2	**Controls SIM2 SIO PAD PUPD** [3]: INS [2:0] : 001 : Pull up 45K 010 : Pull up 5K 011 : Pull up 5K/45K 100 : Pull down 75K 110 : pull down 75K
7:4		PUPD1_G4_1	**Controls SIM2 SRST PAD PUPD** [3]: INS [2:0] : 001 : Pull up 45K 010 : Pull up 5K 011 : Pull up 5K/45K 100 : Pull down 75K 110 : pull down 75K
3:0		PUPD1_G4_0	**Controls SIM2 SCLK PAD PUPD** [3]: INS [2:0] : 001 : Pull up 45K 010 : Pull up 5K 011 : Pull up 5K/45K 100 : Pull down 75K 110 : pull down 75K 111 : pull down 75K/75K

10211D00 GPIO_IES_G5 GPIO Group 5 IES Control Register FFFF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESERVE									IES_G5_6	IES_G5_5	IES_G5_4	IES_G5_3	IES_G5_2	IES_G5_1	IES_G5_0
Type	RW									RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
15:7		RESERVE	**Reserved register**
6		IES_G5_6	**WB SPI PADs input enable control** 0: Disable 1: Enable
5		IES_G5_5	**FM PADs input enable control** 0: Disable 1: Enable
4		IES_G5_4	**MSDC0 RSTB PAD input enable control** 0: Disable 1: Enable
3		IES_G5_3	**MSDC0 DAT PAD input enable control** 0: Disable 1: Enable
2		IES_G5_2	**MSDC0 CLK PAD input enable control** 0: Disable 1: Enable
1		IES_G5_1	**MSDC0 DSL PAD input enable control** 0: Disable

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Bit(s)	Mnemonic	Name	Description
			1: Enable
0		IES_G5_0	**MSDC0 CMD PAD input enable control** 0: Disable 1: Enable

10211D10 **GPIO_SMT_G5** **GPIO Group 5 SMT Control Register** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SMT_G5_6	SMT_G5_5	SMT_G5_4	SMT_G5_3	SMT_G5_2	SMT_G5_1	SMT_G5_0
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6		SMT_G5_6	**Controls WB SPI PADs Schmitt trigger** 0: Disable 1: Enable
5		SMT_G5_5	**Controls FM PADs Schmitt trigger** 0: Disable 1: Enable
4		SMT_G5_4	**Controls MSDC0 RSTB PAD Schmitt trigger** 0: Disable 1: Enable
3		SMT_G5_3	**Controls MSDC0 DAT PAD Schmitt trigger** 0: Disable 1: Enable
2		SMT_G5_2	**Controls MSDC0 CLK PAD Schmitt trigger** 0: Disable 1: Enable
1		SMT_G5_1	**Controls MSDC0 DSL PAD Schmitt trigger** 0: Disable 1: Enable
0		SMT_G5_0	**Controls MSDC0 CMD PAD Schmitt trigger** 0: Disable 1: Enable

10211D20 **GPIO_TDSEL0_G5** **GPIO Group 5 TDSEL Control Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					TDSEL0_G5_6				TDSEL0_G5_5				TDSEL0_G5_4			
Type					RW				RW				RW			
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDSEL0_G5_3				TDSEL0_G5_2				TDSEL0_G5_1				TDSEL0_G5_0			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:24		TDSEL0_G5_6	Controls WB SPI PADs Tx delay selection

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Bit(s)	Mnemonic	Name	Description
23:20		TDSEL0_G5_5	Controls FM PADs Tx delay selection
19:16		TDSEL0_G5_4	Controls MSDC0 RSTB PAD Tx delay selection
15:12		TDSEL0_G5_3	Controls MSDC0 DAT PAD Tx delay selection
11:8		TDSEL0_G5_2	Controls MSDC0 CLK PAD Tx delay selection
7:4		TDSEL0_G5_1	Controls MSDC0 DSL PAD Tx delay selection
3:0		TDSEL0_G5_0	Controls MSDC0 CMD PAD Tx delay selection

10211D28 GPIO_RDSEL0_G5 GPIO Group 5 RDSEL Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDSEL0_G5_5		RDSEL0_G5_4						RDSEL0_G5_3						RDSEL0_G5_2[5:4]	
Type	RW		RW						RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDSEL0_G5_2[3:0]				RDSEL0_G5_1						RDSEL0_G5_0					
Type	RW				RW						RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:30		RDSEL0_G5_5	Controls FM PADs Rx delay selection
29:24		RDSEL0_G5_4	Controls MSDC0 RSTB PAD Rx delay selection
23:18		RDSEL0_G5_3	Controls MSDC0 DAT PAD Rx delay selection
17:12		RDSEL0_G5_2	Controls MSDC0 CLK PAD Rx delay selection
11:6		RDSEL0_G5_1	Controls MSDC0 DSL PAD Rx delay selection
5:0		RDSEL0_G5_0	Controls MSDC0 CMD PAD Rx delay selection

10211D2C GPIO_RDSEL1_G5 GPIO Group 5 RDSEL Control Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RDSEL0_G5_6	
Type															RW	
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1:0		RDSEL0_G5_6	Controls WB SPI PADs Rx delay selection

10211D30 GPIO_PULLEN0_G5 GPIO Group 5 PULLEN Control Register 0 0003F000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															PULL	PULL

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															EN0_G5_17	EN0_G5_16
Type															RW	RW
Reset															1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PULLEN0_G5_15	PULLEN0_G5_14	PULLEN0_G5_13	PULLEN0_G5_12												
Type	RW	RW	RW	RW												
Reset	1	1	1	1												

Bit(s)	Mnemonic	Name	Description
17		PULLEN0_G5_17	Controls GPIO189 PULLEN
16		PULLEN0_G5_16	Controls GPIO188 PULLEN
15		PULLEN0_G5_15	Controls GPIO187 PULLEN
14		PULLEN0_G5_14	Controls GPIO186 PULLEN
13		PULLEN0_G5_13	Controls GPIO185 PULLEN
12		PULLEN0_G5_12	Controls GPIO184 PULLEN

10211D50 **GPIO_PULLSEL0_G5** **GPIO Group 5 PULLSEL Control Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															PULLSEL0_G5_17	PULLSEL0_G5_16
Type															RW	RW
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PULLSEL0_G5_15	PULLSEL0_G5_14	PULLSEL0_G5_13	PULLSEL0_G5_12												
Type	RW	RW	RW	RW												
Reset	0	0	0	0												

Bit(s)	Mnemonic	Name	Description
17		PULLSEL0_G5_17	Controls GPIO189 PULLSEL
16		PULLSEL0_G5_16	Controls GPIO188 PULLSEL
15		PULLSEL0_G5_15	Controls GPIO187 PULLSEL
14		PULLSEL0_G5_14	Controls GPIO186 PULLSEL
13		PULLSEL0_G5_13	Controls GPIO185 PULLSEL
12		PULLSEL0_G5_12	Controls GPIO184 PULLSEL

10211D70 **GPIO_DRV0_G5** **GPIO Group 5 Driving Control Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DRV0_G5_6				DRV0_G5_5				DRV0_G5_4			
Type					RW				RW				RW			
Reset					0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DRV0_G5_3				DRV0_G5_2				DRV0_G5_1				DRV0_G5_0			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:24		DRV0_G5_6	**Controls WB SPI PADs driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:1]: 00: 2mA 01: 4mA 10: 6mA 11: 8mA [0]: Reserved
23:20		DRV0_G5_5	**Controls FM PADs driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:1]: 00: 2mA 01: 4mA 10: 6mA 11: 8mA [0]: Reserved
19:16		DRV0_G5_4	**Controls MSDC0 RSTB PAD driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:0]: 000: 2mA 100: 4mA 010: 6mA 110: 8mA 001: 10mA 101: 12mA 011: 14mA 111: 16mA
15:12		DRV0_G5_3	**Controls MSDC0 DAT PAD driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:0]: 000: 2mA 100: 4mA 010: 6mA 110: 8mA 001: 10mA 101: 12mA 011: 14mA 111: 16mA
11:8		DRV0_G5_2	**Controls MSDC0 CLK PAD driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:0]: 000: 2mA 100: 4mA

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Bit(s)	Mnemonic	Name	Description
			010: 6mA 110: 8mA 001: 10mA 101: 12mA 011: 14mA 111: 16mA
7:4		DRV0_G5_1	**Controls MSDC0 DSL PAD driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:0]: 000: 2mA 100: 4mA 010: 6mA 110: 8mA 001: 10mA 101: 12mA 011: 14mA 111: 16mA
3:0		DRV0_G5_0	**Controls MSDC0 CMD PAD driving selection** [3]: Output slew rate control 1: Slower slew 0: No slew rate controlled [2:0]: 000: 2mA 100: 4mA 010: 6mA 110: 8mA 001: 10mA 101: 12mA 011: 14mA 111: 16mA

10211D80 **GPIO_PUPD0_G5** **GPIO Group 5 Special IO PU/PD Control Register 0** **22222662**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		PUPD0_G5_7				PUPD0_G5_6				PUPD0_G5_5				PUPD0_G5_4		
Type		RW				RW				RW				RW		
Reset		0	1	0		0	1	0		0	1	0		0	1	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name		PUPD0_G5_3				PUPD0_G5_2				PUPD0_G5_1				PUPD0_G5_0		
Type		RW				RW				RW				RW		
Reset		0	1	0		1	1	0		1	1	0		0	1	0

Bit(s)	Mnemonic	Name	Description
30:28		PUPD0_G5_7	**Controls MSDC0 DATA4 PAD PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K
26:24		PUPD0_G5_6	**Controls MSDC0 DATA3 PAD PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K
22:20		PUPD0_G5_5	**Controls MSDC0 DATA2 PAD PUPD** [2]: 0: Pull up; 1: Pull down

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Bit(s)	Mnemonic	Name	Description
			[1]: 50K [0]: 10K
18:16		PUPD0_G5_4	**Controls MSDC0 DATA1 PAD PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K
14:12		PUPD0_G5_3	**Controls MSDC0 DATA0 PAD PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K
10:8		PUPD0_G5_2	**Controls MSDC0 DSL PAD PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K
6:4		PUPD0_G5_1	**Controls MSDC0 CLK PAD PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K
2:0		PUPD0_G5_0	**Controls MSDC0 CMD PAD PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K

10211D90 **GPIO_PUPD1_G5** **GPIO Group 5 Special IO PU/PD Control Register 1** **00002222**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PUPD0_G5_11				PUPD0_G5_10				PUPD0_G5_9				PUPD0_G5_8		
Type			RW				RW				RW				RW	
Reset		0	1	0		0	1	0		0	1	0		0	1	0

Bit(s)	Mnemonic	Name	Description
14:12		PUPD0_G5_11	**Controls MSDC0 RSTB PAD PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K
10:8		PUPD0_G5_10	**Controls MSDC0 DATA7 PAD PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K
6:4		PUPD0_G5_9	**Controls MSDC0 DATA6 PAD PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K
2:0		PUPD0_G5_8	**Controls MSDC0 DATA5 PAD PUPD** [2]: 0: Pull up; 1: Pull down [1]: 50K [0]: 10K

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5.3 Keypad Scanner

5.3.1 General Description

The keypad supports two types of keypads: 8*8 single keys and 3*3 configurable double keys.

The 8*8 keypad can be divided into two parts: 1) The keypad interface including 8 columns and 8 rows (see Figure 5-3 and Figure 5-4). The key detection block provides key pressed, key released and de-bounce mechanisms.

Each time the key is pressed or released, i.e. something different in the 8x8 matrix, the key detection block senses the change and recognizes if a key has been pressed or released. Whenever the key status changes and is stable, a KEYPAD IRQ will be issued. The MCU can then read the key(s) pressed directly in the KP_MEM1, KP_MEM2, KP_MEM3, KP_MEM4 and KP_MEM5 registers. To ensure the key pressed information is not missed, the status register in keypad will not be read-cleared by the APB read command. The status register can only be changed by the key-pressed detection FSM.

This keypad detects one or two keys pressed simultaneously with any combination. **Figure** 5-7 shows the one key pressed condition. **Figure** 5-8 (a) and **Figure** 5-8 (b) illustrate the cases of two keys pressed. Since the key pressed detection depends on the HIGH or LOW level of the external keypad interface, if the keys are pressed at the same time, and there exists a key that is on the same column and the same row with other keys, the pressed key cannot be correctly decoded. For example, if there are three key pressed: key1 = (x1, y1), key2 = (x2, y2), and key3 = (x1, y2), both key3 and key4 = (x2, y1) will be detected, and therefore they cannot be distinguished correctly. Hence, the keypad detects only one or two keys pressed simultaneously in any combination. More than two keys pressed simultaneously in a specific pattern will retrieve the wrong information.

The 3*3 keypad supports a 3*3*2 = 18 keys matrix. The 18 keys are divided into 9 sub groups, and each group consists of 2 keys and a 20 ohm resistor. Besides the limitation of the 8*8 keypad, 3*3 keypad has another limitation, which is it cannot detect two keys pressed simultaneously when the two keys are in one group, i.e. the 3*3 keypad cannot detect key 0 and key 1 pressed simultaneously or key 14 and key 15 pressed simultaneously.

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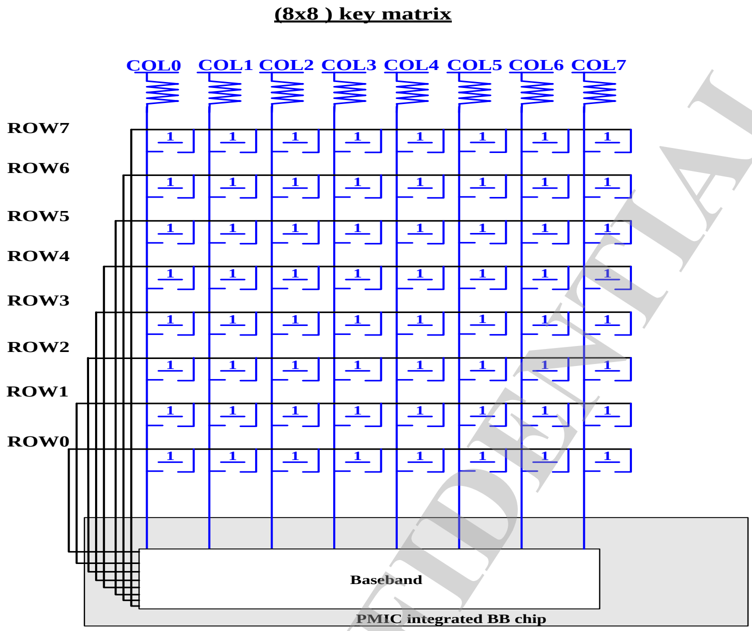

Figure 5-3. 8x8 keypad matrix (64 keys)

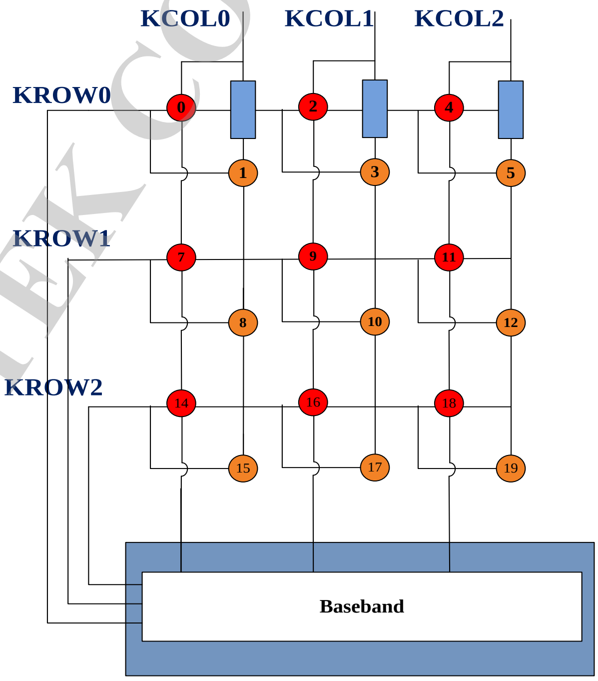

Figure 5-4. 3x3 keypad matrix (18 keys)

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5.3.2 Waveform

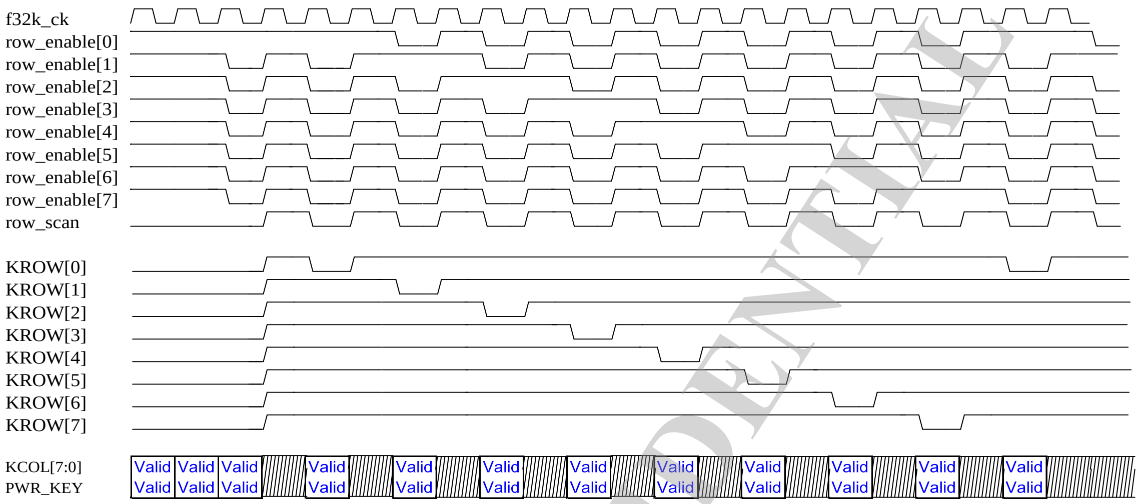

Figure 5-5. 8x8 keypad scan waveform

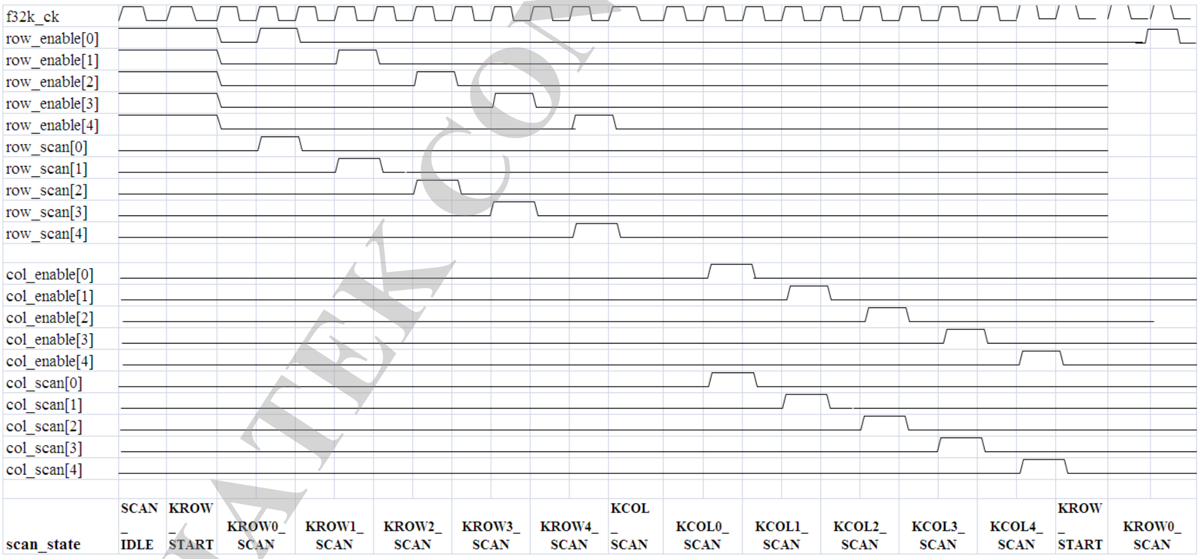

Figure 5-6. 5*5 keypad scan waveform

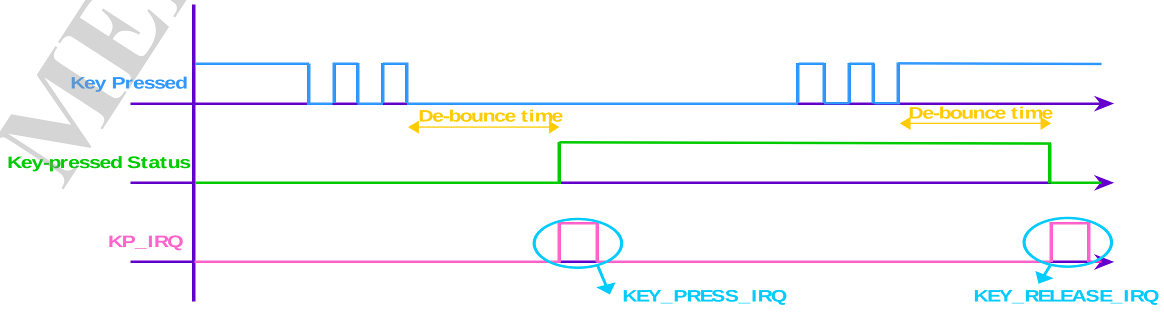

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Figure 5-7. One key pressed with de-bounce mechanism denoted

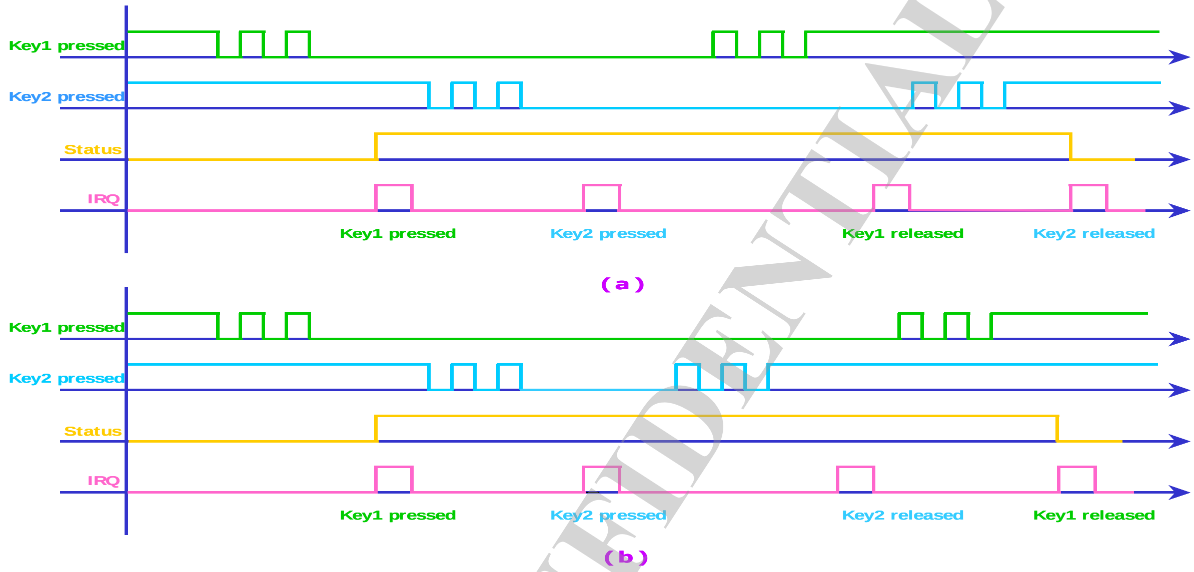

Figure 5-8. (a) Two keys pressed, case 1; (b) Two keys pressed, case 2

5.3.3 Register Definition

Module name: kp Base address: (+10003000h)

Address	Name	Width	Register Function
10003000	KP_STA	16	**Keypad Status**
10003004	KP_MEM1	16	**Keypad Scanning Output Register** Shows the key-pressed status of key 0 (LSB) ~ key 15. Refer to Table 5-1 and Table 5-2.
10003008	KP_MEM2	16	**Keypad Scanning Output Register** Shows the key-pressed status of key 16 (LSB) ~ key 31. Refer to Table 5-1 and Table 5-2.
1000300C	KP_MEM3	16	**Keypad Scanning Output Register** Shows the key-pressed status of key 32 (LSB) ~ key 47. Refer to Table 5-1 and Table 5-2.
10003010	KP_MEM4	16	**Keypad Scanning Output Register** Shows the key-pressed status of key 48 (LSB) ~ key 63. Refer to Table 5-1 and Table 5-2.
10003014	KP_MEM5	16	**Keypad Scanning Output Register** Shows the key-pressed status of key 64 (LSB) ~ key 77. Refer to Table 5-1 and Table 5-2.
10003018	KP_DEBOUNCE	16	**De-bounce Period Setting** Defines the waiting period before key pressing or release events are considered stable. If the de-bounce setting is too small, the keypad will be too sensitive and detect too many unexpected key presses. The suitable de-bounce time setting must be adjusted according to the user's habit.
1000301C	KP_SCAN_TIMING	16	**Keypad Scan Timing Adjustment Register** Sets up the 3*3 keypad scan timing. *Note: ROW_SCAN_DIV > ROW_INTERVAL_DIV and COL_SCAN_DIV > COL_INTERVAL_DIV.* ROW_INTERVAL_DIV/COL_INTERVAL_DIV are used to lower

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Address	Name	Width	Register Function
			the power consumption for it decreases the actual scan number during the de-bounce time.
10003020	KP_SEL	16	**Keypad Selection Register** Used to select: 1: Single keypad or double keypad 2: Which cols and rows are used when using double keypad
10003024	KP_EN	16	**Keypad Enable Register** Enables/Disables keypad.

10003000 KP_STA Keypad Status 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STA
Type																RO
Reset																0

Bit(s)	Mnemonic	Name	Description
0	STA	STA	**Indicates the keypad status** The register is not cleared by the read operation. 0: No key pressed 1: Key pressed

10003004 KP_MEM1 Keypad Scanning Output Register FFFF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY15	KEY14	KEY13	KEY12	KEY11	KEY10	KEY9	KEY8	KEY7	KEY6	KEY5	KEY4	KEY3	KEY2	KEY1	KEY0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Overview Shows the key-pressed status of key 0 (LSB) ~ key 15. Refer to Table 5-1 and Table 5-2.

Bit(s)	Mnemonic	Name	Description
15	KEY15	KEY15	
14	KEY14	KEY14	
13	KEY13	KEY13	
12	KEY12	KEY12	
11	KEY11	KEY11	
10	KEY10	KEY10	
9	KEY9	KEY9	
8	KEY8	KEY8	
7	KEY7	KEY7	
6	KEY6	KEY6	
5	KEY5	KEY5	
4	KEY4	KEY4	
3	KEY3	KEY3	
2	KEY2	KEY2	
1	KEY1	KEY1	

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Bit(s)	Mnemonic	Name	Description
0	**KEY0**	KEY0	

10003008 KP_MEM2 Keypad Scanning Output Register FFFF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY31	KEY30	KEY29	KEY28	KEY27	KEY26	KEY25	KEY24	KEY23	KEY22	KEY21	KEY20	KEY19	KEY18	KEY17	KEY16
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Overview Shows the key-pressed status of key 16 (LSB) ~ key 31. Refer to Table 5-1 and Table 5-2.

Bit(s)	Mnemonic	Name	Description
15	**KEY31**	KEY31	
14	**KEY30**	KEY30	
13	**KEY29**	KEY29	
12	**KEY28**	KEY28	
11	**KEY27**	KEY27	
10	**KEY26**	KEY26	
9	**KEY25**	KEY25	
8	**KEY24**	KEY24	
7	**KEY23**	KEY23	
6	**KEY22**	KEY22	
5	**KEY21**	KEY21	
4	**KEY20**	KEY20	
3	**KEY19**	KEY19	
2	**KEY18**	KEY18	
1	**KEY17**	KEY17	
0	**KEY16**	KEY16	

1000300C KP_MEM3 Keypad Scanning Output Register FFFF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY47	KEY46	KEY45	KEY44	KEY43	KEY42	KEY41	KEY40	KEY39	KEY38	KEY37	KEY36	KEY35	KEY34	KEY33	KEY32
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Overview Shows the key-pressed status of key 32 (LSB) ~ key 47. Refer to Table 5-1 and Table 5-2.

Bit(s)	Mnemonic	Name	Description
15	**KEY47**	KEY47	
14	**KEY46**	KEY46	
13	**KEY45**	KEY45	
12	**KEY44**	KEY44	
11	**KEY43**	KEY43	

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Bit(s)	Mnemonic	Name	Description
10	**KEY42**	KEY42	
9	**KEY41**	KEY41	
8	**KEY40**	KEY40	
7	**KEY39**	KEY39	
6	**KEY38**	KEY38	
5	**KEY37**	KEY37	
4	**KEY36**	KEY36	
3	**KEY35**	KEY35	
2	**KEY34**	KEY34	
1	**KEY33**	KEY33	
0	**KEY32**	KEY32	

10003010 KP_MEM4 Keypad Scanning Output Register FFFF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY63	KEY62	KEY61	KEY60	KEY59	KEY58	KEY57	KEY56	KEY55	KEY54	KEY53	KEY52	KEY51	KEY50	KEY49	KEY48
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Overview Shows the key-pressed status of key 48 (LSB) ~ key 63. Refer to Table 5-1 and Table 5-2.

Bit(s)	Mnemonic	Name	Description
15	**KEY63**	KEY63	
14	**KEY62**	KEY62	
13	**KEY61**	KEY61	
12	**KEY60**	KEY60	
11	**KEY59**	KEY59	
10	**KEY58**	KEY58	
9	**KEY57**	KEY57	
8	**KEY56**	KEY56	
7	**KEY55**	KEY55	
6	**KEY54**	KEY54	
5	**KEY53**	KEY53	
4	**KEY52**	KEY52	
3	**KEY51**	KEY51	
2	**KEY50**	KEY50	
1	**KEY49**	KEY49	
0	**KEY48**	KEY48	

10003014 KP_MEM5 Keypad Scanning Output Register 00FF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									KEY71	KEY70	KEY69	KEY68	KEY67	KEY66	KEY65	KEY64
Type									RO	RO	RO	RO	RO	RO	RO	RO

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Reset									1	1	1	1	1	1	1	1

Overview Shows the key-pressed status of key 64 (LSB) ~ key 77. Refer to Table 5-1 and Table 5-2.

Bit(s)	Mnemonic	Name	Description
7	**KEY71**	KEY71	
6	**KEY70**	KEY70	
5	**KEY69**	KEY69	
4	**KEY68**	KEY68	
3	**KEY67**	KEY67	
2	**KEY66**	KEY66	
1	**KEY65**	KEY65	
0	**KEY64**	KEY64	

10003018 KP_DEBOUNCE De-bounce Period Setting 0400

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DEBOUNCE													
Type			RW													
Reset			0	0	0	1	0	0	0	0	0	0	0	0	0	0

Overview Defines the waiting period before key pressing or release events are considered stable. If the de-bounce setting is too small, the keypad will be too sensitive and detect too many unexpected key presses. The suitable de-bounce time setting must be adjusted according to the user's habit.

Bit(s)	Mnemonic	Name	Description
13:0	**DEBOUNCE**	DEBOUNCE	De-bounce time = KP_DEBOUNCE/32 ms

1000301C KP_SCAN_TIMING Keypad Scan Timing Adjustment Register 0011

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COL_INTERVAL_DIV				ROW_INTERVAL_DIV				COL_SCAN_DIV				ROW_SCAN_DIV			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1

Overview Sets up the 3*3 keypad scan timing. Note: ROW_SCAN_DIV > ROW_INTERVAL_DIV and COL_SCAN_DIV > COL_INTERVAL_DIV. ROW_INTERVAL_DIV/COL_INTERVAL_DIV are used to lower the power consumption for it decreases the actual scan number during the de-bounce time.

Bit(s)	Mnemonic	Name	Description
15:12	**COL_INTERVAL_DIV**	COL_INTERVAL_DIV	**Sets up the COL SCAN interval cycle, i.e. cycles between two scans** Default 0 means there is 1 cycle between two high scan pulses.
11:8	**ROW_INTERVAL_DIV**	ROW_INTERVAL_DIV	**Sets up the ROW SCAN interval cycle, i.e. cycles between two scans** Default 0 means there is 1 cycle between two high scan pulses.

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Bit(s)	Mnemonic	Name	Description
7:4	COL_SCAN_DIV	COL_SCAN_DIV	**Sets up the COL SCAN cycle which includes COL_INTERVAL_DIV and the high pulse period** Default 1 means there are 2 cycles for each scan, including 1 cycle high pulse and 1 cycle interval.
3:0	ROW_SCAN_DIV	ROW_SCAN_DIV	**Sets up the ROW SCAN cycle which includes ROW_INTERVAL_DIV and the high pulse period** Default 1 means there are 2 cycles for each scan, including 1 cycle high pulse and 1 cycle interval.

10003020 KP_SEL Keypad Selection Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																KP_SEL
Type																DC
Reset																0

Overview Used to select: 1: Single keypad or double keypad 2: Which cols and rows are used when using double keypad

Bit(s)	Mnemonic	Name	Description
0	KP_SEL	KP_SEL	**Used to select whether the single keypad or double keypad is used** 0: Use single keypad 1: Use double keypad

10003024 KP_EN Keypad Enable Register 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																KP_EN
Type																RW
Reset																1

Overview Enables/Disables keypad.

Bit(s)	Mnemonic	Name	Description
0	KP_EN	KP_EN	0: Disable keypad (both single and double keypad will not work.) 1: Enable keypad (only one of single and double keypad can work.)

	COL0	COL1	COL2	COL3	COL4	COL5	COL6	COL7	PWRKEY
ROW7	63	64	65	66	67	68	69	70	71
ROW6	54	55	56	57	58	59	60	61	62
ROW5	45	46	47	48	49	50	51	52	53
ROW4	36	37	38	39	40	41	42	43	44
ROW3	27	28	29	30	31	32	33	34	35
ROW2	18	19	20	21	22	23	24	25	26

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ROW1	9	10	11	12	13	14	15	16	17
ROW0	0	1	2	3	4	5	6	7	8

Table 5-1. 8*8 single key's order number in COL/ROW matrix

	COL0	COL1	COL2	COL3	COL4	COL5	PWRKEY
ROW5	65/66	67/68	69/70	71/72	73/74	75/76	77
ROW4	52/53	54/55	56/57	58/59	60/61	62/63	64
ROW3	39/40	41/42	43/44	45/46	47/48	49/50	51
ROW2	26/27	28/29	30/31	32/33	34/35	36/37	38
ROW1	13/14	15/16	17/18	19/20	21/22	23/24	25
ROW0	0/1	2/3	4/5	6/7	8/9	10/11	12

Table 5-2. 3*3 double key's order number in COL/ROW matrix

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5.4 UART

5.4.1 Introduction

The baseband chipset houses four UARTs. UARTs provide full duplex serial communication channels between the baseband chipset and external devices.

UART has both M16C450 and M16550A modes of operation, which are compatible with a range of standard software drivers. The extensions are designed to be broadly software compatible with 16550A variants, but certain areas offer no consensus.

In common with M16550A, the UART supports word lengths from 5 to 8 bits, an optional parity bit and one or two stop bits and is fully programmable by an 8-bit CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmit and receive FIFOs. Two modem control lines and a diagnostic loop-back mode are provided. UART also includes two DMA handshake lines, indicating when the FIFOs are ready to transfer data to the CPU. Interrupts can be generated from any of the ten sources.

Note that UART is designed so that all internal operation is synchronized by the CLK signal. This synchronization results in minor timing differences between the UART and industry standard 16550A device, which means that the core is not clock for clock identical to the original device.

After hardware reset, UART will be in M16C450 mode; its FIFOs can then be enabled and UART can enter M16550A mode. UART has further additional functions beyond the M16550A mode. Each of the extended functions can be selected individually under software control.

UART provides more powerful enhancements than the industry-standard 16550:

Hardware flow control
This feature is very useful when the ISR latency is hard to predict and control in the embedded applications. The MCU is relieved of having to fetch the received data within a fixed amount of time.

Note that in order to enable the enhancements, the enhanced mode bit, EFR[4], must be set. If EFR[4] is not set, IER[7:4], FCR[5:4], cannot be written and MCR[7] cannot be read. The enhanced mode bit ensures that UART is backward compatible with the software that has been written for 16C450 and 16550A devices.

5.4.2 Features

- Provides 4 channels
- DMA, polling or interrupt operation
- Supports word lengths from 5 to 8 bits, with an optional parity bit and one or two stop bits
- 4 UART ports for hardware automatic flow control (UART0, UART1, UART2, UART3)
- Supports baud rates from 110bps up to 961,200bps
- Baud rate auto detection function

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5.4.3 Block Diagram

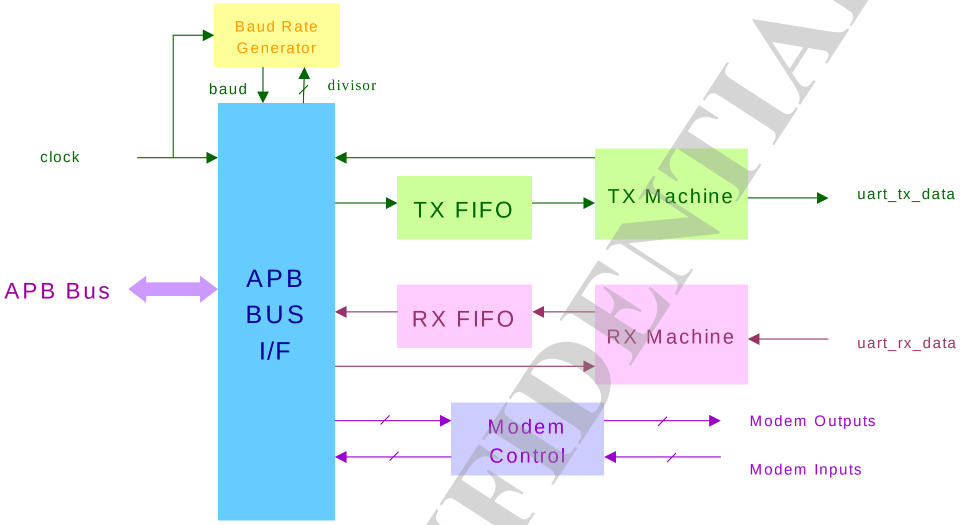

Figure 5-9. Block diagram of UART

5.4.4 Register Definition

UART number	Base address	Feature
UART0	0x11002000	Supports DMA, HW flow control
UART1	0x11003000	Supports DMA, HW flow control
UART2	0x11004000	Supports DMA, HW flow control
UART3	0x11005000	Supports DMA, HW flow control
UART4	0x1100D000	Supports DMA, HW flow control

There are five UART IPs in this SOC. The usage of the registers below are the same except that the base address must be changed to respective one.

Module name: uart1 Base address: (+11003000h)

Address	Name	Width	Register Function
11003000	**RBR**	8	RX Buffer Register
11003000	**THR**	8	TX Holding Register
11003004	**IER**	8	**Interrupt Enable Register** By storing 1 to a specific bit position, the interrupt associated with that bit is enabled. Otherwise, the interrupt is disabled. IER[7:4] are modified when EFR[4] = 1.
11003008	**IIR**	8	**Interrupt Identification Register** The priority is from high to low as the following: IIR[5:0]=0X1: No interrupt pending IIR[5:0]=0X6: Line status interrupt (under IER[2]=1) IIR[5:0]=0Xc: RX data timeout interrupt (under IER[0]=1) IIR[5:0]=0X4: RX data are placed in the RX buffer register or the RX trigger level is reached (under IER[0]=1). IIR[5:0]=0X2: TX holding register is empty or the contents of TX

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Address	Name	Width	Register Function
			FIFO have been reduced to its trigger level (under IER[1]=1). IIR[5:0]=0X0: Modem status change interrupt (under IER[3]=1) IIR[5:0]=0X10: XOFF character received (under IER[5]=1,EFR[4] = 1) IIR[5:0]=0X20: CTS or RTS rising edge (under IER[7]=1, IER[6]=1, EFR[4] = 1)
11003008	FCR	8	**FIFO Control Register** FCR is used to control the trigger levels of FIFOs or flush FIFOs. FCR[5:4] is modified when EFR[4] = 1.
1100300C	LCR	8	**Line Control Register** Determines characteristics of serial communication signals.
11003010	MCR	8	**Modem Control Register** Controls interface signals of UART. MCR[7] can be read when EFR[4] = 1.
11003014	LSR	8	**Line Status Register** Line status register
11003018	MSR	8	**Modem Status Register** Note: After a reset, D4-D7 will be inputs. A modem status interrupt can be cleared by writing 0 to D0-D3 or reading this register and set by writing 1 to D0-D3 or input has changed. D0-D3 can be modified when != BFh.
1100301C	SCR	8	**Scratch Register** General purpose read/write register After reset, its value will be un-defined.
11003020	AUTOBAUD_EN	8	Auto Baud Detect Enable Register
11003024	HIGHSPEED	8	High Speed Mode Register
11003028	SAMPLE_COUNT	8	**Sample Counter Register** When HIGHSPEED=3, sample_count is the threshold value for UART sample counter (sample_num). Count from 0 to sample_count.
1100302C	SAMPLE_POINT	8	**Sample Point Register** When HIGHSPEED=3, UART gets the input data when sample_count=sample_num. e.g. system clock = 13MHz, 921600 = 13000000/14 sample_count = 13 and sample point = 6 (sample the central point to decrease the inaccuracy) SAMPLE_POINT is usually (SAMPLE_COUNT-1)/2 with decimal removed.
11003030	AUTOBAUD_REG	8	**Auto Baud Monitor Register** Autobaud detection state Will not change until autobaud_en is enabled again.
11003034	RATEFIX_AD	8	**Clock Rate Fix Register**
11003038	AUTOBAUDSAMPLE	8	**Auto Baud Sample Register** Since the system clock may change, autobaud sample duration should change as system clock changes. When system clock = 13MHz, autobaudsample = 6; when system clock = 26MHz, autobaudsample = 13; when system clock = 52MHz, autobaudsample = 27.
1100303C	GUARD	8	Guard Time Added Register
11003040	ESCAPE_DAT	8	Escape Character Register
11003044	ESCAPE_EN	8	Escape Enable Register
11003048	SLEEP_EN	8	Sleep Enable Register
1100304C	DMA_EN	8	DMA Enable Register
11003050	RXTRI_AD	8	RX Trigger Address
11003054	FRACDIV_L	8	Fractional Divider LSB Address
11003058	FRACDIV_M	8	Fractional Divider MSB Address

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Address	Name	Width	Register Function
1100305C	FCR_RD	8	FIFO Control Register
11003090	DLL	8	**Divisor Latch (LS)** Divides bclk frequency
11003094	DLM	8	**Divisor Latch (MS)** Divides bclk frequency
11003098	EFR	8	**Enhanced Feature Register**
1100309C	FEATURE_SEL	8	**UART Feature Select Register** For AP MCU side UART If new UART register map is used, feature_sel should be kept at 1.
110030A0	XON1	8	XON1 Char Register
110030A4	XON2	8	XON2 Char Register
110030A8	XOFF1	8	XOFF1 Char Register
110030AC	XOFF2	8	XOFF2 Char Register
110030B0	USB_RX_SEL	8	UART USB RX Pin Selection Register
110030B4	SLEEP_REQ	8	UART Sleep Request Register
110030B8	SLEEP_ACK	8	UART Idle Register
110030BC	SPM_SEL	8	SPM Interface Selection Register

11003000 RBR RX Buffer Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RBR							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RBR	**Read-only** The received data can be read by accessing this register.

11003000 THR TX Holding Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									THR							
Type									WO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	THR	**TX holding register** Write-only. The data to be transmitted are written to this register then sent to PC via serial communication.

11003004 IER Interrupt Enable Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CTSI	RTSI	XOFFI		EDSSI	ELSI	ETBEI	ERBFI
Type									RW	RW	RW		RW	RW	RW	RW
Reset									0	0	0		0	0	0	0

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Bit(s)	Name	Description
7	CTSI	**Masks an interrupt that is generated when a rising edge is detected on the CTS modem control line.** *Note: This interrupt is only enabled when hardware flow control is enabled.* 0: Mask an interrupt generated when a rising edge is detected on the CTS modem control line. 1: Unmask an interrupt generated when a rising edge is detected on the CTS modem control line.
6	RTSI	**Masks an interrupt that is generated when a rising edge is detected on the RTS modem control line.** *Note: This interrupt is only enabled when hardware flow control is enabled.* 0: Mask an interrupt generated when a rising edge is detected on the RTS modem control line. 1: Unmask an interrupt generated when a rising edge is detected on the RTS modem control line.
5	XOFFI	**Masks an interrupt that is generated when an XOFF character is received.** *Note: This interrupt is only enabled when software flow control is enabled.* 0: Mask an interrupt generated when an XOFF character is received. 1: Unmask an interrupt generated when an XOFF character is received.
3	EDSSI	**When set to 1, an interrupt will be generated if DCTS (MSR[0]) becomes set.** 0: No interrupt is generated if DCTS (MSR[0]) becomes set. 1: An interrupt is generated if DCTS (MSR[0]) becomes set.
2	ELSI	**When set to 1, an interrupt will be generated if BI, FE, PE or OE (LSR[4:1]) becomes set.** 0: No interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set. 1: An interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set.
1	ETBEI	**When set to 1, an interrupt will be generated if the TX holding register is empty or the contents of TX FIFO are reduced to its trigger level.** 0: No interrupt is generated if the TX holding register is empty or the contents of TX FIFO have been reduced to its trigger level. 1: An interrupt is generated if the TX holding register is empty or the contents of TX FIFO have been reduced to its trigger level.
0	ERBFI	**When set to 1, an interrupt will be generated if RX data are placed in the RX buffer register or the RX trigger level is reached.** 0: No interrupt is generated if RX data are placed in the RX buffer register or the RX trigger level is reached. 1: An interrupt is generated if RX data are placed in the RX buffer register or the RX trigger level is reached.

11003008 IIR Interrupt Identification Register 01

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFOE		ID					
Type									RO		RU					
Reset									0	0	0	0	0	0	0	1

Bit(s)	Name	Description
7:6	FIFOE	
5:0	ID	**IIR[5:0] Priority Level Interrupt Source** 000001 - No interrupt pending 000110 1 Line Status Interrupt: BI, FE, PE or OE set in LSR. (Under IER[2]=1) 001100 2 RX Data Timeout:

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Bit(s)	Name	Description
		Timeout on character in RX FIFO. (Under IER[0]=1) 000100 3 RX Data Received: RX Data received or RX Trigger Level reached. (Under IER[0]=1) 000010 4 TX Holding Register Empty: TX Holding Register empty or TX FIFO Trigger Level reached. (Under IER[1]=1) 000000 5 Modem Status change: DDCD, TERI, DDSR or DCTS set in MSR. (Under IER[3]=1) 010000 6 Software Flow Control: XOFF Character received. (Under IER[5]=1) 100000 7 Hardware Flow Control: CTS or RTS Rising Edge. (Under IER[7]=1 or IER[6]=1) Line Status Interrupt: A RX Line Status Interrupt (IIR[5:0] == 000110b) is generated if ELSI (IER[2]) is set and any of BI, FE, PE or OE (LSR[4:1]) becomes set. The interrupt is cleared by reading the Line Status Register. RX Data Timeout Interrupt:When virtual FIFO mode is disabled, RX Data Timeout Interrupt is generated if all of the following apply: 1. FIFO contains at least one character; 2. The most recent character was received longer than four character periods ago (including all start, parity and stop bits); 3. The most recent CPU read of the FIFO was longer than four character periods ago. The timeout timer is restarted on receipt of a new byte from the RX Shift Register, or on a CPU read from the RX FIFO. The RX Data Timeout Interrupt is enabled by setting EFRBI (IER[0]) to 1, and is cleared by reading RX FIFO. When virtual FIFO mode is enabled, RX Data Timeout Interrupt is generated if all of the following apply: 1. FIFO is empty; 2. The most recent character was received longer than four character periods ago (including all start, parity and stop bits); 3. The most recent CPU read of the FIFO was longer than four character periods ago. The timeout timer is restarted on receipt of a new byte from the RX Shift Register or reading DMA_EN register. The RX Data Timeout Interrupt is enabled by setting EFRBI (IER[0]) to 1, and is cleared by reading DMA_EN register. RX Data Received Interrupt: A RX Received interrupt (IER[5:0] == 000100b) is generated if EFRBI (IER[0]) is set and either RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached. The interrupt is cleared by reading the RX Buffer Register or the RX FIFO (if enabled). TX Holding Register Empty Interrupt: A TX Holding Register Empty Interrupt (IIR[5:0] = 000010b) is generated if ETRBI (IER[1]) is set and either the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level. The interrupt is cleared by writing to the TX Holding Register or TX FIFO if FIFO enabled. Modem Status Change Interrupt: A Modem Status Change Interrupt (IIR[5:0] = 000000b) is generated if EDSSI (IER[3]) is set and either DDCD, TERI, DDSR or DCTS (MSR[3:0]) becomes set. The interrupt is cleared by reading the Modem Status Register. Software Flow Control Interrupt: A Software Flow Control Interrupt (IIR[5:0] = 010000b) is generated if Software Flow Control is enabled and XOFFI (IER[5]) becomes set, indicating that an XOFF character has been received. The interrupt is cleared by reading the Interrupt Identification Register. Hardware Flow Control Interrupt: A Hardware Flow Control Interrupt (IER[5:0] = 100000b) is generated if Hardware Flow Control is enabled and

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Bit(s)	Name	Description
		either RTSI (IER[6]) or CTSI (IER[7]) becomes set indicating that a rising edge has been detected on either the RTS/CTS Modem Control line. The interrupt is cleared by reading the Interrupt Identification Register.

11003008 FCR FIFO Control Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RFTL1_RFTL0		TFTL1_TFTL0			CLRT	CLRR	FIFOE
Type									WO		WO			WO	WO	WO
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
7:6	RFTL1_RFTL0	**RX FIFO trigger threshold** RX FIFO contains total 32 bytes. 0: 1 1: 6 2: 12 3: RXTRIG
5:4	TFTL1_TFTL0	**TX FIFO trigger threshold** TX FIFO contains total 32 bytes. 0: 1 1: 4 2: 8 3: 14
2	CLRT	**Control bit to clear TX FIFO** 0: No effect 1: Clear TX FIFO
1	CLRR	**Control bit to clear RX FIFO** 0: No effect 1: Clear RX FIFO
0	FIFOE	**Enables FIFO** This bit must be set to 1 for any of other bits in the registers to take effect. 0: Disable both RX and TX FIFO 1: Enable both RX and TX FIFO

1100300C LCR Line Control Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLAB	SB	SP	EPS	PEN	STB	WLS1_WLS0	
Type									RW	RW	RW	RW	RW	RW	RW	
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	DLAB	**Divisor latch access bit** 0: RX and TX registers are read/written at Address 0 and IER register is read/written at Address 4. 1: Divisor Latch LS is read/written at Address 0 and the Divisor Latch MS is read/written at Address 4.
6	SB	**Sets up break** 0: No effect 1: SOUT signal is forced to "0" state.

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Bit(s)	Name	Description
5	SP	**Stick parity** 0: No effect. 1: The parity bit is forced to a defined state, depending on the states of EPS and PEN: If EPS=1 & PEN=1, the parity bit will be set and checked=0. If EPS=0 & PEN=1, the Parity bit will be set and checked=1.
4	EPS	**Selects even parity** 0: When EPS=0, an odd number of ones is sent and checked. 1: When EPS=1, an even number of ones is sent and checked.
3	PEN	**Enables parity** 0: The parity is neither transmitted nor checked. 1: The parity is transmitted and checked.
2	STB	**Number of STOP bits** 0: One STOP bit is always added. 1: Two STOP bits are added after each character is sent; unless the character length is 5 when 1 STOP bit is added.
1:0	WLS1_WLS0	**Selects word length** 0: 5 bits 1: 6 bits 2: 7 bits 3: 8 bits

11003010 MCR Modem Control Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF_STATUS			Loop			RTS	
Type									RU			RW			RW	
Reset									0			0			0	

Bit(s)	Name	Description
7	XOFF_STATUS	**Read-only** 0: When an XON character is received. 1: When an XOFF character is received.
4	Loop	**Loop-back control bit** 0: No loop-back is enabled. 1: Loop-back mode is enabled.
1	RTS	**Controls the state of the output NRTS, even in loop mode** 0: RTS always outputs 1. 1: RTSs output is controlled by flow control condition.

11003014 LSR Line Status Register 60

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFOERR	TEMT	THRE	BI	FE	PE	OE	DR
Type									RU	RU	RU	RU	RU	RU	RU	RU
Reset									0	1	1	0	0	0	0	0

Bit(s)	Name	Description
7	FIFOERR	**RX FIFO error indicator** 0: No PE, FE and BI is in RX FIFO.

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Bit(s)	Name	Description
		1: Set to 1 when there is at least one PE, FE or BI in RX FIFO.
6	TEMT	**TX holding register (or TX FIFO) and TX shift register are empty.** 0: Empty conditions below are not met. 1: If FIFOs are enabled, the bit will be set whenever TX FIFO and the TX shift register are empty. If FIFOs are disabled, the bit will be set whenever TX holding register and TX shift register are empty.
5	THRE	**Indicates if there is room for TX Holding Register or TX FIFO is reduced to its trigger level** 0: Reset whenever the contents of TX FIFO are more than its trigger level (FIFOs are enabled), or whenever TX holding register is not empty (FIFOs are disabled). 1: Set whenever the contents of TX FIFO are reduced to its trigger level (FIFOs are enabled), or whenever TX holding register is empty and ready to accept new data (FIFOs are disabled).
4	BI	**Break interrupt** 0: Reset by CPU reading this register 1: If FIFOs are disabled, this bit will be set whenever SIN is held in 0 state for more than one transmission time (START bit + DATA bits + PARITY + STOP bits). If FIFOs are enabled, this error will be associated with a corresponding character in FIFO and is flagged when this byte is at top of FIFO. When a break occurs, only one zero character will be loaded to the FIFO: The next character transfer will be enabled when SIN enters the marking state and receives the next valid start bit.
3	FE	**Framing error** 0: Reset by CPU reading this register 1: If the FIFOs are disabled, this bit will be set if the received data do not have a valid STOP bit. If FIFOs are enabled, the state of this bit will be revealed when the byte it refers to is the next to be read.
2	PE	**Parity error** 0: Reset by CPU reading this register 1: If FIFOs are disabled, this bit will be set if the received data do not have a valid parity bit. If FIFOs are enabled, the state of this bit will be revealed when the referred byte is the next to be read.
1	OE	**Overrun error** 0: Reset by CPU reading this register. 1: If FIFOs are disabled, this bit will be set if RX buffer is not read by CPU before new data from RX shift register overwrites the previous contents. If FIFOs are enabled, an overrun error will occur when RX FIFO is full and RX shift register becomes full. OE is set as soon as this happens. The character in the shift register will then be overwritten but not transferred to the FIFO.
0	DR	**Data ready** 0: Cleared by CPU reading RX buffer or by reading all FIFO bytes. 1: Set by RX buffer becoming full or by FIFO becoming not empty.

11003018 MSR Modem Status Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CTS				DCTS
Type												RU				RW
Reset												0				0

Bit(s)	Name	Description
4	CTS	**Clear to send** When Loop = "0", this value is the complement of the NCTS input signal. When Loop = "1", this value is equal to the RTS bit in the modem control

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Bit(s)	Name	Description
		register.
0	DCTS	**Delta clear to send** 0: Cleared if the state of CTS has not changed since this register is last read. 1: Set if the state of CTS has changed since this register is last read.

1100301C SCR Scratch Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SCR							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SCR	**General purpose read/write register** After reset, its value will be undefined.

11003020 AUTOBAUD_EN Auto Baud Detect Enable Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														sleep_ack_sel	AUTOBAUD_SEL	AUTOBAUD_EN
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	sleep_ack_sel	0: Send sleep_ack when autobaud_en is enabled and autobaud state machine and RX are idle . 1: Cannot send sleep_ack when autobaud_en is enabled .
1	AUTOBAUD_SEL	**Selects auto-baud** 0: Support standard baud rate detection 1: Support non_standard baud rate detection (only baud from 300 to 115,200; using 52MHz to auto fix is recommended)
0	AUTOBAUD_EN	**Auto-baud enable signal** 0: Disable auto-baud function 1: Enable auto-baud function (UARTn+0024h SPEED should be set 0) *Note: When AUTOBAUD_EN is active, there should not be A*/a* char before auto baud char AT/at. If A*/a* is inevitable, autobaud will fail and please disable AUTOBAUD_EN to reset autobaud feature and autobaud_en.*

11003024 HIGHSPEED High Speed Mode Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SPEED	
Type															RW	
Reset															0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
1:0	SPEED	**UART sample counter base** 0: Based on 16*baud_pulse, baud_rate = system clock frequency/16/{DLH, DLL} 1: Based on 8*baud_pulse, baud_rate = system clock frequency/8/{DLH, DLL} 2: based on 4*baud_pulse, baud_rate = system clock frequency/4/{DLH, DLL} 3: Based on sampe_count*baud_pulse, baud_rate = system clock frequency/(sampe_count+1)/{DLM, DLL}

11003028 **SAMPLE_COUNT** **Sample Counter Register** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**SAMPLECOUNT**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SAMPLECOUNT	Only useful when HIGHSPEED mode=3

1100302C **SAMPLE_POINT** **Sample Point Register** **FF**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**SAMPLEPOINT**							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	SAMPLEPOINT	**SAMPLE_POINT is usually (SAMPLE_COUNT-1)/2 without decimal.** Sample point is effective only when HIGHSPEED=3.

11003030 **AUTOBAUD_REG** **Auto Baud Monitor Register** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**BAUD_STAT**				**BAUD_RATE**			
Type									RU				RU			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:4	BAUD_STAT	**Autobaud format** 0: Autobaud is detecting. 1: AT_7N1 2: AT_7O1 3: AT_7E1 4: AT_8N1 5: AT_8O1 6: AT_8E1

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Bit(s)	Name	Description
		7: at_7N1 8: at_7E1 9: at_7O1 10: at_8N1 11: at_8E1 12: at_8O1 13: Autobaud detection fails.
3:0	BAUD_RATE	**Autobaud baud rate** 0: 115200 1: 57600 2: 38400 3: 19200 4: 9600 5: 4800 6: 2400 7: 1200 8: 300 9: 110

11003034 RATEFIX_AD Clock Rate Fix Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**FREQ_SEL**	**AUTOBAUD_RATE_FIX**	**RATE_FIX**
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FREQ_SEL	0: System clock = UART_CLK_SRC/2 1: System clock = UART_CLK_SRC/4
1	AUTOBAUD_RATE_FIX	0: System clock = UART_CLK_SRC/1 (UART_CLK_SRC = 52MHz or 26MHz) 1: System clock = UART_CLK_SRC/2 or UART_CLK_SRC/4 (depends on FREQ_SEL)
0	RATE_FIX	0: System clock = UART_CLK_SRC/1 (UART_CLK_SRC = 52MHz or 26MHz) 1: System clock = UART_CLK_SRC/2 or UART_CLK_SRC/4 (depends on FREQ_SEL)

11003038 AUTOBAUDSAMPLE Auto Baud Sample Register 0D

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											**AUTOBAUDSAMPLE**					
Type											RW					
Reset											0	0	1	1	0	1

Bit(s)	Name	Description
5:0	AUTOBAUDSAMPLE	**CLK division for autobaud rate detection** For standard baud rate detection. system clk 52m: 'd 27

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Bit(s)	Name	Description
		system clk 26m: 'd 13 system clk 13m: 'd 6 For non-standard baud rate detection.

1100303C **GUARD** **Guard Time Added Register** **0F**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												GUARD_EN	GUARD_CNT			
Type												RW	RW			
Reset												0	1	1	1	1

Bit(s)	Name	Description
4	GUARD_EN	**Guard interval add enable signal** 0: No guard interval added 1: Add guard interval after stop bit
3:0	GUARD_CNT	**Guard interval count value** Guard interval = [1/(system clock/div_step/div)]*GUARD_CNT

11003040 **ESCAPE_DAT** **Escape Character Register** **FF**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ESCAPE_DAT							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	ESCAPE_DAT	**Escape character added before software flow control data and escape character** If TX data are xon (31h) with esc_en =1, UART transmits data as esc + CEh (~xon).

11003044 **ESCAPE_EN** **Escape Enable Register** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ESC_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	ESC_EN	**Adds escape character in transmitter and removes escape character in receiver by UART** 0: Does not deal with the escape character 1: Add escape character in transmitter and remove escape character in receiver

11003048 **SLEEP_EN** **Sleep Enable Register** **00**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SLEEP_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	SLEEP_EN	**For sleep mode issue** 0: Does not deal with sleep mode indicate signal 1: Activate hardware flow control or software control according to software initial setting when chip enters sleep mode. Release hardware flow when chip wakes up. For software control, UART sends xon when awaken and when FIFO does not reach threshold level.

1100304C DMA_EN DMA Enable Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													FIFO_lsr_sel	TO_CNT_AUTORST	TX_DMA_EN	RX_DMA_EN
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	FIFO_lsr_sel	**Selects FIFO LSR mode** 0: LSR updates automatically with read data from RX FIFO. 1: LSR holds the first line status error state until you read the LSR register.
2	TO_CNT_AUTORST	**Time-out counter auto reset register** 0: After RX time-out happens, SW shall reset the interrupt by reading UART 0x4C. 1: The time-out counter will be auto reset. Set this register when Rain's new DMA is used.
1	TX_DMA_EN	**TX_DMA mechanism enable signal** 0: Does not use DMA in TX 1: Use DMA in TX. When this register is enabled, the flow control is based on the DMA threshold and generates a time-out interrupt for DMA.
0	RX_DMA_EN	**RX_DMA mechanism enable signal** 0: Does not use DMA in RX 1: Use DMA in RX. When this register is enabled, the flow control is based on the DMA threshold and generates a time-out interrupt.

11003050 RXTRI_AD RX Trigger Address 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RXTRIG			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RXTRIG	**When {rtm,rtl}=2'b11, The RX FIFO threshold will be RXtrig.** The value is suggested to be less than half of RX FIFO size, which is 32 Bytes.

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11003054 FRACDIV_L Fractional Divider LSB Address 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FRACDIV_L							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FRACDIV_L	**Adds sampling count (+1) from State Data7 to Data 0 in order to contribute fractional divisor** Only when high_speed=3.

11003058 FRACDIV_M Fractional Divider MSB Address 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FRACDIV_M	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	FRACDIV_M	**Adds sampling count when in state stop to parity in order to contribute fractional divisor** Only when high_speed=3.

1100305C FCR_RD FIFO Control Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RFTL1_RFTLo		TFTL1_TFTLo			CLRT	CLRR	FIFOE
Type									RO		RO			RO	RO	RO
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
7:6	RFTL1_RFTLo	**RX FIFO trigger threshold** RX FIFO contains total 32 bytes. 0: 1 1: 6 2: 12 3: RXTRIG
5:4	TFTL1_TFTLo	**TX FIFO trigger threshold** TX FIFO contains total 32 bytes. 0: 1 1: 4 2: 8 3: 14
2	CLRT	0: TX FIFO is not cleared. 1: TX FIFO is cleared.
1	CLRR	0: RX FIFO is not cleared. 1: RX FIFO is cleared.
0	FIFOE	**Enables FIFO** This bit must be set to 1 for any other bits in the registers to take effect.

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Bit(s)	Name	Description
		0: RX and TX FIFOs are not enabled. 1: RX and TX FIFOs are enabled.

11003090 DLL Divisor Latch (LS) 01

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLL							
Type									RW							
Reset									0	0	0	0	0	0	0	1

Bit(s)	Name	Description
7:0	DLL	Divisor latch low 8-bit data

11003094 DLM Divisor Latch (MS) 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLM							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DLM	**Divisor latch high 8-bit data** *Note: Division by 1 generates a BAUD signal that is constantly high. DLL & DLM setting formula is {DLH,DLL}=(system clock frequency/baud_pulse/baud_rate).* When RATE_FIX(RATEFIX_AD[0])=0, system clock frequency = 52MHz. When RATE_FIX(RATEFIX_AD[0])=1 and RATE_FIX(RATEFIX_AD[2])=0, system clock frequency = 26MHz. When RATE_FIX(RATEFIX_AD[0])=1 and RATE_FIX(RATEFIX_AD[2])=1, system clock frequency = 13MHz. For baud_pulse value refer to HIGH_SPEED(offset=24H) register, e.g. when 52MHz, default speed mode and 115200 baud rate, {DLH,DLL}=52MHz/16/115200=28.

11003098 EFR Enhanced Feature Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AUTO_CTS	AUTO_RTS		ENABLE_E	SW_FLOW_CONT			
Type									RW	RW		RW	RW			
Reset									0	0		0	0	0	0	0

Bit(s)	Name	Description
7	AUTO_CTS	**Enables hardware transmission flow control** 0: Disable 1: Enable
6	AUTO_RTS	**Enables hardware reception flow control** 0: Disable 1: Enable
4	ENABLE_E	**Enables enhancement feature** 0: Disable

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Bit(s)	Name	Description
		1: Enable
3:0	SW_FLOW_CONT	**Software flow control bits** 00xx: No TX flow Control 10xx: Transmit XON1/XOFF1 as flow control bytes 01xx: Transmit XON2/XOFF2 as flow control bytes xx00: No RX Flow Control xx10: Receive XON1/XOFF1 as flow control bytes xx01: Receive XON2/XOFF2 as flow control bytes

1100309C **FEATURE_SEL** **UART Feature Select Register** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FEATURE_SEL
Type																RW
Reset																0

Bit(s)	Name	Description
0	FEATURE_SEL	**For AP MCU side UART, if new UART register map is used, feature_sel should be kept at 1.** 0: Disable new register map 1: Enable new register map

110030A0 **XON1** **XON1 Char Register** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XON1							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XON1	XON1 character for software flow control

110030A4 **XON2** **XON2 Char Register** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XON2							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XON2	XON2 character for software flow control

110030A8 **XOFF1** **XOFF1 Char Register** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF1							

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Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XOFF1	XOFF1 character for software flow control

110030AC XOFF2 XOFF2 Char Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**XOFF2**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XOFF2	XOFF2 character for software flow control

110030B0 USB_RX_SEL UART USB RX Pin Selection Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**USB_RX_SEL**
Type																RW
Reset																0

Bit(s)	Name	Description
0	USB_RX_SEL	0: Select UART RX pin 1: Select USB RX pin

110030B4 SLEEP_REQ UART Sleep Request Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**SLEEP_REQ**
Type																RW
Reset																0

Bit(s)	Name	Description
0	SLEEP_REQ	0: Cancel sleep request to UART (after wake-up sent by CPU) 1: Send sleep request to UART (before sleep sent by CPU)

110030B8 SLEEP_ACK UART Idle Register 01

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**SLEEP_ACK**
Type																RU
Reset																1

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Bit(s)	Name	Description
0	SLEEP_ACK	0: UART is not in idle state. (CPU can poll this register to get the UART state.) 1: UART is in idle state. (CPU can poll this register to get the UART state.)

110030BC SPM_SEL SPM Interface Selection Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SPM_SEL
Type																RW
Reset																0

Bit(s)	Name	Description
0	SPM_SEL	0: SPM sleep interface will not be used. 1: SPM sleep interface will be used.

5.4.5 Programming Guide

5.4.5.1 Auto Baud Rate Detection

UART can detect the baud rate used automatically. Follow the steps below:

1. Set up register autobaud_en to start detecting the data.
2. Send data of ASCII code "AT" or "at" to UART from the connected host, e.g. the PC.
3. Check if the "AT" or "at" is received. If received, the setting is now already set for further transmission.

5.4.5.2 Transmission

Follow the steps below for UART transmission:

1. Use the autobaud function to set up the baud rate or set up the parameters by yourself. The settings needed can be found in register DLL, DLM ,HIGH SPEED.
2. After setting up the baud rate, start the transmission by filling the TX FIFO and receiving data from RX FIFO.
3. Virtual FIFO can also be used for the transmission. To use the virtual FIFO, you need APDMA settings (refer to details in the APDMA section).

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5.5 USB 2.0 High Speed Dual-Role Controller

5.5.1 Introduction

The USB controller is configured for supporting 8 endpoints to receive packets and 8 endpoints to send packets except for endpoint 0. These endpoints can be individually configured in the software to handle either Bulk transfers, Interrupt transfers or Isochronous transfers. There are 8 DMA channels and the embedded RAM size is configurable size up to 8K bytes. The embedded RAM can be dynamically configured to each endpoint. As the host for point-to-point communications, the controller maintains a frame counter and automatically schedules SOF, Isochronous, Interrupt and Bulk transfers.

5.5.2 Features

The following table lists the unified USB IP features.

Feature list	Description
USB specifications	USB2.0 OTG
Enhanced feature	Generic Host QMU Generic Dev QMU
Endpoint	8 Tx 8 Rx EP0
DMA channel	8
Embedded RAM	Up to 8KB
UTMI+ interface	UTMI+ 16b
CPU slave interface	AHB asynchronous design
DMA master interface	AHB busy free asynchronous design

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5.5.3 USB Controller Block Diagram

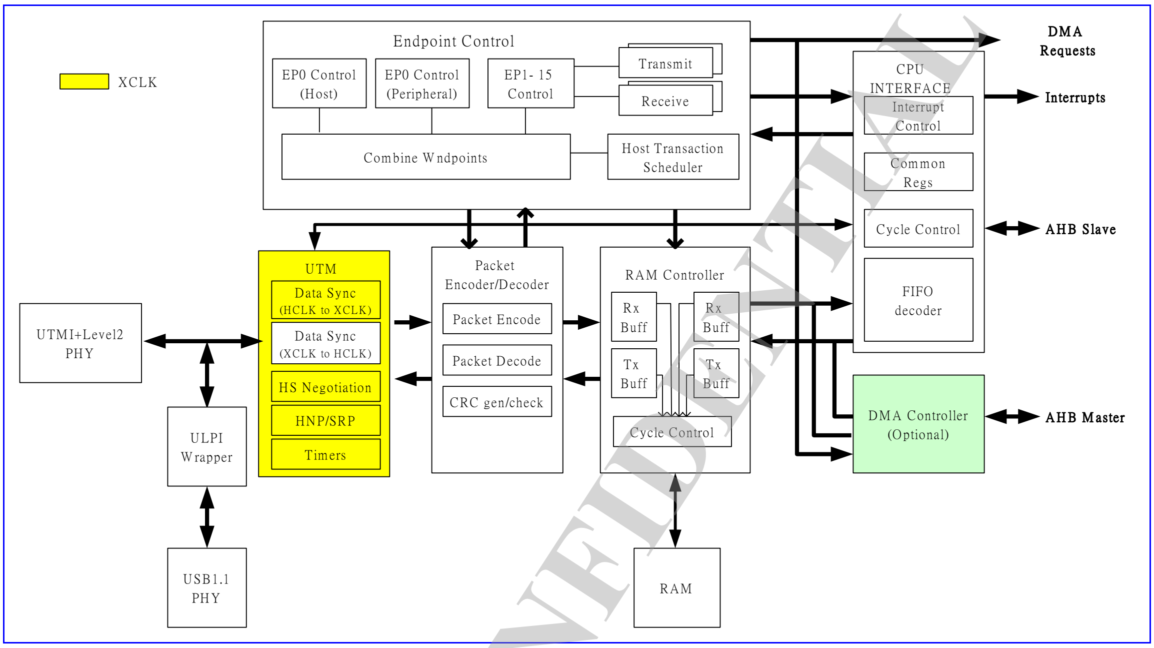

Figure 5-10. USB controller block diagram

5.5.4 Register Definition

Registers accessed using byte manipulation are marked in blue columns. Byte accessing registers can be accessed using word manipulation. Word accessing registers cannot be accessed using the byte manipulation.

Register address	Register name	Manipulation (Byte/Word)	Acronym
Common Registers			
USB + 0000h	Function address register	Byte	FADDR
USB + 0001h	Power management register	Byte	POWER
USB + 0002h	Tx interrupt status register	Byte	INTRTX
USB + 0004h	Rx interrupt status register	Byte	INTRRX
USB + 0006h	Tx interrupt enable register	Byte	INTRTXE
USB + 0008h	Rx interrupt enable register	Byte	INTRRXE
USB + 000Ah	Common USB interrupts register	Byte	INTRUSB
USB + 000Bh	Common USB interrupts enable register	Byte	INTRUSBE
USB + 000Ch	Frame number register	Byte	FRAME
USB + 000Eh	Endpoint selecting index register	Byte	INDEX
USB + 000Fh	Test mode enable register	Byte	TESTMODE
Indexed EndPoint CSR Region *n stands for endpoint number.* *For example, endpoint 1's n = 1. Valid n = 1 ~ MaxEndPoint.* *MaxEndPoint is hardware configured and the maximum is 15.*			

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Register address	Register name	Manipulation (Byte/Word)	Acronym
USB + 0010h ~ USB + 001Fh	It maps to CSR EP0 ~ EPx depending on the INDEX register. For example, if INDEX is n, address 0010h ~ 001Fh are mapped to 0x(100+10*n)h ~ 0x(100+10*n+F)h.	Byte	Indexed CSR
USB + 0020h	USB endpoint 0 FIFO register	Byte	FIFO0
USB + 0020h +(n)*4 h	USB endpoint n FIFO register	Byte	FIFOn
OTG, Dynamic FIFO, Version Registers			
USB + 0060h	OTG device control register	Byte	DEVCTL
USB + 0061h	Power up counter register	Byte	PWRUPCNT
USB + 0062h	Tx FIFO size register	Byte	TXFIFOSZ
USB + 0063h	Rx FIFO size register	Byte	RXFIFOSZ
USB + 0064h	Tx FIFO address register	Byte	TXFIFOADD
USB + 0066h	Rx FIFO address register	Byte	RXFIFOADD
USB + 006Ch	Hardware capability register	Byte	HWCAPS
USB + 006Eh	Hardware sub version register	Byte	HWSVERS
Hardware Configuration, Special Setting Registers			
USB + 0070h	USB bus performance register 1	Byte	BUSPERF1
USB + 0072h	USB bus performance register 2	Byte	BUSPERF2
USB + 0074h	USB bus performance register 3	Byte	BUSPERF3
USB + 0078h	Information about number of Tx and Rx register	Byte	EPINFO
USB + 0079h	Information about the width of RAM and the number of DMA channel register	Byte	RAMINFO
USB + 007Ah	Info. about delay to be applied register	Byte	LINKINFO
USB + 007Bh	Vbus pulsing charge register	Byte	VPLEN
USB + 007Ch	Time buffer available on HS transactions register	Byte	HS_EOF1
USB + 007Dh	Time buffer available on FS transactions register	Byte	FS_EOF1
USB + 007Eh	Time buffer available on LS transactions register	Byte	LS_EOF1
USB + 007Fh	Reset information register	Byte	RST_INFO
USB + 0080h	Rx data toggle set/status register	Word	RXTOG
USB + 0082h	Rx data toggle enable register	Word	RXTOGEN
USB + 0084h	Tx data toggle set/status register	Word	TXTOG
USB + 0086h	Tx data toggle enable register	Word	TXTOGEN
Level1 interrupt Control/Status registers			
USB + 00A0h	USB Level 1 interrupt status register	Byte	USB_L1INTS
USB + 00A4h	USB Level 1 interrupt unmask register	Byte	USB_L1INTM
USB + 00A8h	USB Level 1 interrupt polarity register	Byte	USB_L1INTP
USB + 00ACh	USB Level 1 interrupt control register	Byte	USB_L1INTC
Non-indexed EndPoint CSR Region *n stands for endpoint number.* *For example, endpoint 1's n = 1. Valid n = 1 ~ MaxEndPoint.* *MaxEndPoint is hardware configured and the maximum is 15.*			
USB + 0102h	EP0 control status register	Byte	CSR0
USB + 0108h	EP0 received bytes register	Byte	COUNT0

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Register address	Register name	Manipulation (Byte/Word)	Acronym
USB + 010Bh	NAK limit register	Byte	NAKLIMT0
USB + 010Fh	Core configuration register	Byte	CONFIGDATA
USB + 0100h +(n)*10h	TXMAP register	Byte	TXMAP(n)
USB + 0102h +(n)*10h	Tx CSR register	Byte	TXCSR(n)
USB + 0104h +(n)*10h	RXMAP register	Byte	RXMAP(n)
USB + 0106h +(n)*10h	Rx CSR register	Byte	RXCSR(n)
USB + 0108h +(n)*10h	Rx Count register	Byte	RXCOUNT(n)
USB + 010Ah +(n)*10h	TxType register	Byte	TXTYPE(n)
USB + 010Bh +(n)*10h	TxInterval register	Byte	TXINTERVAL(n)
USB + 010Ch +(n)*10h	RxType register	Byte	RXTYPE(n)
USB + 010Dh +(n)*10h	RxInterval register	Byte	RXINTERVAL(n)
USB + 010Fh +(n)*10h	Configured FIFO size register	Byte	FIFOSIZE(n)
DMA Channels Control Registers *M stands for DMA channel number.* *For example, DMA channel 1's M = 1. Valid M = 1 ~ MaxDMAChannel.* *MaxDMAChannel is hardware configured and the maximum is 8.*			
USB + 0200h	DMA interrupt status register (word access only)	Word	DMA_INTR
USB + 0210h	DMA limiter register (word access only)	Word	DMA_LIMITER
USB + 0220h	DMA configuration register (word access only)	Word	DMA_CONFIG
USB + 0204h +(M-1)*10h	DMA channel M control register (word access only)	Word	DMA_CNTL_M
USB + 0208h +(M-1)*10h	DMA channel M address register (word access only)	Word	DMA_ADDR_M
USB + 020Ch +(M-1)*10h	DMA channel M byte count register (word access only)	Word	DMA_COUNT_M
EndPoint RX Packet Count Register *n stands for endpoint number. For example, endpoint 1's n = 1. Valid n = 1 ~ MaxEndPoint.* *MaxEndPoint is hardware configured and the maximum is 15.*			
USB + 0300h +(n)*4h	EPn RxPktCount register	Word	EPnRXPKTCOUNT
Host/Hub Control Registers (Host mode only registers) *n stands for endpoint number. For example, endpoint 1's n = 1. Valid n = 1 ~ MaxEndPoint.* *MaxEndPoint is hardware configured and maximum is 15.*			
USB + 0480h +8*n h	Transmit endpoint n function address	Word	TXFUNCADDR
USB + 0482h	Transmit endpoint n hub/port address	Word	TXHUBADDR

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Register address	Register name	Manipulation (Byte/Word)	Acronym
+8*n h			
USB + 0484h +8*n h	Receive endpoint n function address	Word	RXFUNCADDR
USB + 0486h +8*n h	Receive endpoint n hub/port address	Word	RXHUBADDR
Debug Function Registers			
USB + 0600h	Debug flag selection control (byte 0, 1, 2, 3)	Word	DFC0R, DFC1R
USB + 0604h	Timing test mode	Word	TM1
USB + 0605h	No response error count	Word	TM1
USB + 0606h	Debug flag UTMI11 sub group selection	Word	DFC2R
USB + 0608h	Hardware version control register	Word	HWVER_DATE
USB + 0610h	Packet sequence record control/OpState record control	Word	PSR_CTRL/ OSR_CTRL
USB + 0611h ~ 0616h	Packet sequence record filter and trigger setting	Word	PSR_CTRL
USB + 0620h ~ 0637h	Debug register	Word	DBG_PRB
USB + 0640h ~ 065fh	Packet sequence PID data/OpState record Data	Word	PSR_DATA/ OSR_DATA
USB + 0684h	SRAM address register	Word	SRAMA
USB + 0688h	SRAM data register (word access only)	Word	SRAMD
USB + 0690h	RISC_SIZE register	Word	RISC_SIZE
USB + 0700h	Reserved register	Word	RESREG
USB + 0704h	HW TxPktRdy	Word	HWTPR
USB + 0708h	HW TxPktRdy enable register	Word	HWTPR_EN
USB + 070Ch	HW TxPktRdy error detection register	Word	HWTPR_ERR

5.5.5 Function Address Register

Module name: Unified_USB Base address: (+11200000h)

Address	Name	Width	Register Function
00	**FADDR**	8	Function Address Register (Device mode only)
01	**POWER_PERI**	8	Power Management Register
01	**POWER_HOST**	8	Power Management Register
0002	**INTRTX**	16	Tx Interrupt Status Register
0004	**INTRRX**	16	Rx Interrupt Status Register
0006	**INTRTXE**	16	Tx Interrupt Enable Register
0008	**INTRRXE**	16	Rx Interrupt Enable Register
0A	**INTRUSB**	8	Common USB Interrupt Register
0B	**INTRUSBE**	8	Common USB Interrupt Enable Register
000C	**FRAME**	16	Frame Number Register
0E	**INDEX**	8	Endpoint Selection Index Register
0F	**TESTMODE**	8	Test Mode Enable Register
0010	**TXMAP**	16	TXMAP Register

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Address	Name	Width	Register Function
0012	TXCSR_PERI	16	Tx CSR Register
0012	TXCSR_HOST	16	Tx CSR Register
0014	RXMAP	16	RXMAP Register
0016	RXCSR_PERI	16	RX CSR Register
0016	RXCSR_HOST	16	Rx CSR Register
0018	RXCOUNT	16	Rx Count Register
1A	TXTYPE	8	TxType Register
1B	TXINTERVAL	8	TxInterval Register
1C	RXTYPE	8	RxType Register
1D	RXINTERVAL	8	RxInterval Register
1F	FIFOSIZE	8	Configured FIFO Size Register
00000020	FIFO0	32	USB Endpoint 0 FIFO Register
00000024	FIFO1	32	USB Endpoint 1 FIFO Register
60	DEVCTL	8	Device Control Register
61	PWRUPCNT	8	Power Up Counter Register
62	TXFIFOSZ	8	Tx FIFO Size Register
63	RXFIFOSZ	8	Rx FIFO Size Register
0064	TXFIFOADD	16	Tx FIFO Address Register
0066	RXFIFOADD	16	Rx FIFO Address Register
006C	HWCAPS	16	Hardware Capability Register
006E	HWSVERS	16	Version Register
0070	BUSPERF1	16	USB Bus Performance Register 1
0072	BUSPERF2	16	USB Bus Performance Register 2
0074	BUSPERF3	16	USB Bus Performance Register 3
78	EPINFO	8	Number of Tx and Rx Register
79	RAMINFO	8	Width of RAM and Number of DMA Channel Register
7A	LINKINFO	8	Delay to be Applied Register
7B	VPLEN	8	Vbus Pulsing Charge Register
7C	HS_EOF1	8	Time Buffer Available on HS Transaction Register
7D	FS_EOF1	8	Time Buffer Available on FS Transaction Register
7E	LS_EOF1	8	Time Buffer Available on LS Transaction Register
7F	RST_INFO	8	Reset Information Register
0080	RXTOG	16	Rx Data Toggle Set/Status Register
0082	RXTOGEN	16	Rx Data Toggle Enable Register
0084	TXTOG	16	Tx Data Toggle Set/Status Register
0086	TXTOGEN	16	Tx Data Toggle Enable Register
000000A0	USB_L1INTS	32	USB Level 1 Interrupt Status Register
000000A4	USB_L1INTM	32	USB Level 1 Interrupt Mask Register
000000A8	USB_L1INTP	32	USB Level 1 Interrupt Polarity Register
000000AC	USB_L1INTC	32	USB Level 1 Interrupt Control Register
0102	CSR0_PERI	16	EP0 Control Status Register
0102	CSR0_HOST	16	EP0 Control Status Register
0108	COUNT0	16	EP0 Received Bytes Register
10A	Type0	8	EP0 Type Register
10B	NAKLIMT0	8	NAK Limit Register
010C	SRAMCONFIGSIZ	16	SRAM Size Register

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Address	Name	Width	Register Function
	E		
10E	HBCONFIGDATA	8	High Bind-width Configuration Register
10F	CONFIGDATA	8	Core Configuration Register
0110	TX1MAP	16	TX1MAP Register
0112	TX1CSR_PERI	16	Tx1 CSR Register
0112	TX1CSR_HOST	16	Tx1 CSR Register
0114	RX1MAP	16	RX1MAP Register
0116	RX1CSR_PERI	16	RX1 CSR Register
0116	RX1CSR_HOST	16	Rx1 CSR Register
0118	RX1COUNT	16	Rx1 Count Register
11A	TX1TYPE	8	Tx1Type Register
11B	TX1INTERVAL	8	Tx1Interval Register
11C	RX1TYPE	8	Rx1Type Register
11D	RX1INTERVAL	8	Rx1Interval Register
11F	FIFOSIZE1	8	EP1 Configured FIFO Size Register
00000200	DMA_INTR	32	DMA Interrupt Status Register
0204	DMA_CNTL_0	16	DMA Channel 0 Control Register
00000208	DMA_ADDR_0	32	DMA Channel 0 Address Register
0000020C	DMA_COUNT_0	32	DMA Channel 0 Byte Count Register
00000210	DMA_LIMITER	32	DMA Limiter Register
00000220	DMA_CONFIG	32	DMA Configuration Register
0304	EP1RXPKTCOUN T	16	EP1 RxPktCount Register
0480	T0FUNCADDR	16	T0 Function Address Register
0482	T0HUBADDR	16	T0 HUB Address Register
0488	T1FUNCADDR	16	T1 Function Address Register
048A	T1HUBADDR	16	T1 HUB Address Register
048C	R1FUNCADDR	16	R1 Function Address Register
048E	R1HUBADDR	16	R1 HUB Address Register
0604	TM1	16	Test Mode 1 Register
00000608	HWVER_DATE	32	HW Version Control Register
00000684	SRAMA	32	SRAM Address Register
00000688	SRAMD	32	SRAM Data Register
00000690	RISC_SIZE	32	RISC Size Register
00000700	RESREG	32	Reserved Register
730	OTG20_CSRL	8	OTG20 Related Control Register L
731	OTG20_CSRH	8	OTG20 Related Control Register H

11200000 FADDR Function Address Register (Device Mode Only) 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										FUNCTION_ADDRESS						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
6:0	FUNCTION_ADDRESS	FAddr is an 8-bit register that should be written with the 7-bit address of the peripheral part of the transaction. When the USB2.0 controller is used in Peripheral mode (DevCtl.bit2=0), this register should be written with the address received through a SET_ADDRESS command, which will then be used for decoding the function address in subsequent token packets. When the USB2.0 controller is used In host mode (DevCtl.bit2=1), Function address is configured by TXFUNCADDR and RXFUNCADDR.

11200001 POWER_PERI Power Management Register 20

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**ISOUPDATE**	**SOFTCONN**	**HSENAB**	**HSMODE**	**RESET**	**RESUME**	**SUSPENDMODE**	**ENABLESUSPENDM**
Type									RW	RW	RW	RU	RU	RW	RU	RW
Reset									0	0	1	0	0	0	0	0

Bit(s)	Name	Description
7	ISOUPDATE	**When set by the CPU, the USB2.0 controller will wait for an SOF token from the time TxPktRdy is set before sending the packet. If an IN token is received before an SOF token, a 0 length data packet will be sent.** Note: Only valid in Peripheral mode. Also, This bit only affects endpoints performing Isochronous transfers.
6	SOFTCONN	**If Soft Connect/Disconnect feature is enabled, the USB D+/D- lines is enabled when this bit will be set by the CPU and tri-stated when this bit is cleared by the CPU.** In Peripheral FS mode, clearing the Softcon bit may need the execution of latency until USB BUS SE0 is detected by HW. Execution Latency ~= 1ms. Such as SOF Packet EOP or RESET In Peripheral HS mode, clear Softcon bit still need execution latency until USB BUS SE0 is detected by HW. Execution Latency ~= 1us. Note: Set this bit only in Peripheral mode. For Host mode, this bit will be set if DEVCTL[0] session bit is set. This bit should also be cleared if session bit is cleared by CPU.
5	HSENAB	**When set by the CPU, the USB2.0 controller will negotiate for high-speed mode when the device is reset by the hub. If not set, the device will only operate in full-speed mode.**
4	HSMODE	**When set, This read-only bit indicates the high-speed mode is successfully negotiated during USB reset.** In Peripheral mode, it becomes valid when USB reset is completed (as indicated by USB reset interrupt). In host mode, it becomes valid when the Reset bit is cleared. Remains valid for the duration of the session. Note: Allowance is made for Tiny-J signaling in determining the transfer speed to select.
3	RESET	**Set when Reset signaling is present on the bus.** Note: This bit is read/write from the CPU in host mode but read-only in Peripheral mode.
2	RESUME	**Set by the CPU to generate Resume signaling when the function is in Suspend mode. The CPU clears this bit after 10ms (max. 15ms) to end Resume signaling. In host mode, this bit is also automatically set when Resume signaling from the target is detected while the USB2.0 controller is suspended.**

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Bit(s)	Name	Description
1	SUSPENDMODE	**In host mode, this bit is set by the CPU to enter Suspend mode.** In Peripheral mode, this bit is set on entryo into Suspend mode. It is cleared when the CPU reads the interrupt register or sets up the Resume bit above.
0	ENABLESUSPENDM	**Set by the CPU to enable the SUSPENDM output**

11200001 **POWER_HOST** **Power Management Register** **20**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											HSENAB	HSMODE	RESET	RESUME	SUSPENDMODE	ENABLESUSPENDM
Type											RW	RU	RW	RW	A0	RW
Reset											1	0	0	0	0	0

Bit(s)	Name	Description
5	HSENAB	**When set by the CPU, the USB2.0 controller will negotiate for high-speed mode when the device is reset by the hub.** If not set, the device will only operate in full-speed mode.
4	HSMODE	**When set, This read-only bit indicates the high-speed mode is successfully negotiated during USB reset.** In Peripheral mode, it becomes valid when USB reset is completed (as indicated by USB reset interrupt). In host mode, it becomes valid when the Reset bit is cleared. Remains valid for the duration of the session. Note: Allowance is made for Tiny-J signaling in determining the transfer speed to select.
3	RESET	**Set when Reset signaling is present on the bus.** Note: This bit is read/write from the CPU in host mode but read-only in Peripheral mode.
2	RESUME	**Set by the CPU to generate Resume signaling when the function is in Suspend mode.** The CPU clears this bit after 10ms (max. 15ms) to end Resume signaling. In host mode, this bit is also automatically set when Resume signaling from the target is detected while the USB2.0 controller is suspended.
1	SUSPENDMODE	**In host mode, this bit is set by the CPU to enter Suspend mode.** In Peripheral mode, this bit is set on entryo into Suspend mode. It is cleared when the CPU reads the interrupt register or sets up the Resume bit above.
0	ENABLESUSPENDM	**Set by the CPU to enable the SUSPENDM output**

11200002 **INTRTX** **Tx Interrupt Status Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															EP1_TX	EP0
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	EP1_TX	T1 Endpoint N interrupt event.
0	EP0	Endpoint0 interrupt event

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11200004 INTRRX Rx Interrupt Status Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															EP1_RX	
Type															W1C	
Reset															0	

Bit(s)	Name	Description
1	EP1_RX	

11200006 INTRTXE Tx Interrupt Enable Register FFFF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															EP1_TXE	EP0_E
Type															RW	RW
Reset															1	1

Bit(s)	Name	Description
1	EP1_TXE	1'b0: Disable Tx Endpoint N interrupt event 1'b1: Enable Tx Endpoint N interrupt event
0	EP0_E	1'b0: Disable Tx Endpoint N interrupt event 1'b1: Enable Tx Endpoint N interrupt event

11200008 INTRRXE Rx Interrupt Enable Register FFFE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															EP1_RXE	
Type															RW	
Reset															1	

Bit(s)	Name	Description
1	EP1_RXE	1'b0: Disable Rx Endpoint N interrupt event 1'b1: Enable Rx Endpoint N interrupt event

1120000A INTRUSB Common USB Interrupt Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									VBUSERROR	SESSREQ	DISCON	CONN	SOF	RESET_BABLE	RESUME	SUSPEND
Type									W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	VBUSERROR	**Set when VBus drops below the VBus Valid threshold during a session.**

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Bit(s)	Name	Description
		Only valid when USB2.0 controller is 'A' device.
6	SESSREQ	**Set when Session Request signaling has been detected.** Only valid when USB2.0 controller is 'A' device.
5	DISCON	**Set In host mode when a device disconnect is detected. Set in Peripheral mode when a session ends.** Valid at all transaction speeds.
4	CONN	**Set when a device connection is detected.** Only valid in host mode. Valid at all transaction speeds.
3	SOF	**Set when a new frame starts.**
2	RESET_BABLE	**Set in Peripheral mode when Reset signaling is detected on the bus. Set In host mode when babble is detected.** Note: Only active after the first SOF has been sent.
1	RESUME	**Set when Resume signaling is detected on the bus while the USB2.0 controller is in Suspend mode.**
0	SUSPEND	**Set when Suspend signaling is detected on the bus.** Only valid in Peripheral mode.

1120000B INTRUSBE Common USB Interrupt Enable Register 06

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									VBUSERROR_E	SESSREQ_E	DISCON_E	CONN_E	SOF_E	RESET_BABLE_E	RESEUM_E	SUSPEND_E
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	1	1	0

Bit(s)	Name	Description
7	VBUSERROR_E	Enables VBusError interrupt
6	SESSREQ_E	Enables SessReq interrupt
5	DISCON_E	Enables Discon interrupt
4	CONN_E	Enables Conn interrupt
3	SOF_E	Enables SOF interrupt
2	RESET_BABLE_E	Enables Reset/Babble interrupt
1	RESEUM_E	Enables Resume interrupt
0	SUSPEND_E	Enables Suspend interrupt

1120000C FRAME Frame Number Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						FRAME_NUMBER										
Type						RU										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	FRAME_NUMBER	Frame is an 11-bit read-only register that holds the last received frame number.

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1120000E INDEX Endpoint Selection Index Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SELECTED_ENDPOINT			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	SELECTED_ENDPOINT	**Each Tx endpoint and each Rx endpoint has its own set of control/status registers located between USB+100h - USB+1FFh.** In addition, one set of Tx control/status and one set of Rx control/status registers appear at USB+010h - USB+01Fh. Index is a 4-bit register that determines which endpoint control/status registers are accessed. Before accessing an endpoint's control/status registers at USB+010h - USB+01Fh, the endpoint number should be written to the Index register to ensure that the correct control/status registers appear in the memory map.

1120000F TESTMODE Test Mode Enable Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FORCE_HOST	FIFO_ACCESS	FORCE_FS	FORCE_HS	TEST_PACKET	TEST_K	TEST_J	TEST_SE0_NAK
Type									RW	A0	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	FORCE_HOST	**The CPU sets up this bit to instruct the core to enter Host mode when the Session bit is set, regardless of whether it is connected to any peripheral.** The state of the CID input, HostDisconnect and LineState signals are ignored. The core will then remain In host mode until the Session bit is cleared, even if a device is disconnected, and if the Force_Host bit remains set, will re-enter Host mode the next time the Session bit is set.While in this mode, the status of the HOSTDISCON signal from the PHY may be read from bit 7 of the ACTLR0.DevCtl register. The operating speed is determined from the Force_HS and Force_FS bits as follows. USB2.0 IP only Force_HS Force_FS Operating Speed 0 0 Low Speed 0 1 Full Speed 1 0 High Speed 1 1 Undefined
6	FIFO_ACCESS	**The CPU sets up this bit to transfer the packet in the Endpoint 0 Tx FIFO to the Endpoint 0 Rx FIFO.** It is cleared automatically. USB2.0 IP only.
5	FORCE_FS	**The CPU sets up this bit either in conjunction with bit 7 above or to force the USB2.0 controller into Full speed mode when it receives a USB reset**
4	FORCE_HS	**The CPU sets up this bit either in conjunction with bit 7 above or to force the USB2.0 controller into high-speed mode when it receives a USB reset.** USB2.0 IP only.
3	TEST_PACKET	**(HS_MODE) The CPU sets up this bit to enter the Test_Packet test mode. In this mode, the USB2.0 controller repetitively transmits on the bus a 53-byte test packet, the form of which is defined in the Universal Serial Bus Specification Revision 2.0, Section 7.1.20.** *Note: The test packet has a fixed format and must be loaded into the*

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Bit(s)	Name	Description
		Endpoint 0 FIFO before the test mode is entered. USB2.0 IP only.
2	TEST_K	**(HS_MODE) The CPU sets up this bit to enter the Test_K test mode.** In this mode, the USB2.0 controller transmits a continuous K on the bus. USB2.0 IP only.
1	TEST_J	**(HS_MODE) The CPU sets up this bit to enter the Test_J test mode.** In this mode, the USB2.0 controller transmits a continuous J on the bus. USB2.0 IP only.
0	TEST_SE0_NAK	**(HS_MODE) The CPU sets up this bit to enter the Test_SE0_NAK test mode.** In this mode, the USB2.0 controller remains in high-speed mode but responds to any valid IN token with a NAK. USB2.0 IP only.

11200010 TXMAP TXMAP Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				M_1		MAXIMUM_PAYLOAD_TRANSACTION										
Type				RW		RW										
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:11	M_1	**Maximum payload size for indexed TX endpoint, M-1 Packet multiplier m maximum payload transaction register**
10:0	MAXIMUM_PAYLOAD_TRANSACTION	**The TxMaxP register defines the maximum amount of data that can be transferred through the selected Tx endpoint in asingle operation.** There is a TxMaxP register for each Tx endpoint (except for Endpoint 0). Bits 10:0 define (in bytes) the maximum payload transmitted in a single transaction. The value set can be up to 1024 bytes but is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in full-speed and high-speed operations. Where the option of High-bandwidth Isochronous endpoints or of packet splitting on Bulk endpoints has been taken when the core is configured, the register includes either 2 or 5 further bits that define a multiplier m which is equal to one more than the value recorded. In the case of Bulk endpoints with the packet splitting option enabled, the multiplier m can be up to 32 and defines the maximum number of 'USB' packets (i.e. packets for transmission over the USB) of the specified payload into which a single data packet placed in the FIFO should be split, prior to transfer. (If the packet splitting option is not enabled, bit15-13 will not be implemented and bit12-11 (if included) will be ignored.) *Note: The data packet is required to be an exact multiple of the payload specified by bits 10:0, which is itself required to be either 8, 16, 32, 64 or (in the case of high-speed transfers) 512 bytes. For Isochronous endpoints operating in high-speed mode and with the high-bandwidth option enabled, m may only be either 2 or 3 (corresponding to bit 11 set or bit 12 set, respectively) and it specifies the maximum number of such transactions that can take place in a single microframe. If either bit 11 or bit 12 is non-0, the USB2.0 controller will automatically split any data packet written to the FIFO into up to 2 or 3 'USB' packets, each containing the specified payload (or less). The maximum payload for each transaction is 1024 bytes, so this allows up to 3072 bytes to be transmitted in each microframe. (For Isochronous/Interrupt transfers in Full-speed mod, bits 11 and 12 are ignored.) The value written to bits 10:0 (multiplied by m in the case of high-bandwidth Isochronous transfers) must match the value given in the wMaxPacketSize field of the Standard Endpoint Descriptor for the associated endpoint . A mismatch can cause unexpected results. The total amount of data represented by the value written to this register (specified payload * m)*

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Bit(s)	Name	Description
		must not exceed the FIFO size for the Tx endpoint and should not exceed half the FIFO size if double-buffering is required. If this register is changed after packets have been sent from the endpoint, the Tx endpoint FIFO should be completely flushed (using the FlushFIFO bit in TxCSR) after writing the new value to this register.

11200012 TXCSR_PERI Tx CSR Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOSET	ISO		DMAREQEN	FRCDATATOG	DMAREQMODE		SETTXPKTRDY_TWICE	INCOMPTX	CLRDATATOG	SENTSTALL	SENDSTALL	FLUSHFIFO	UNDERRUN	FIFONOTEMPTY	TXPKTRDY
Type	RW	RW		RW	RW	RW		A1	A1	A0	A1	RW	A0	A1	RU	A0
Reset	0	0		0	0	0		0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUTOSET	**If The CPU sets up this bit, TxPktRdy will be automatically set when data of the maximum packet size (value in TxMaxP) is loaded into the TxFIFO.** If a packet of less than the maximum packet size is loaded, TxPktRdy will have to be set manually.
14	ISO	**The CPU sets up this bit to enable the Tx endpoint for Isochronous transfers and clears it to enable the Tx endpoint for Bulk or Interrupt transfers.** *Note: This bit only has any effect in Peripheral mode. In host mode, it always returns to 0.*
12	DMAREQEN	**The CPU sets up this bit to enable the DMA request for the Tx endpoint.**
11	FRCDATATOG	**The CPU sets up this bit to force the endpoint data toggle to switch and the data packet to be cleared from the FIFO, regardless of whether an ACK was received.** This can be used by Interrupt Tx endpoints that are used to communicate rate feedback for Isochronous endpoints.
10	DMAREQMODE	**The CPU sets up this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0.** *Note: This bit must not be cleared either before or in the same cycle as the DMAReqEn bit is cleared.*
8	SETTXPKTRDY_TWICE	**Indicates TxPktRdy had been set when it is 1'b1 already Write 0 to clear it.**
7	INCOMPTX	**When the endpoint is used for high-bandwidth Isochronous/Interrupt transfers, this bit is set to indicate where a large packet has been split into 2 or 3 packets for transmission but insufficient IN tokens have been received to send all the parts.** *Note: In anything other than a high-bandwidth transfer, this bit will always return to 0.* Write 0 to clear it.
6	CLRDATATOG	**The CPU writes 1 to this bit to reset the endpoint data toggle to 0.**
5	SENTSTALL	**This bit is set when a STALL handshake is transmitted.** The FIFO is flushed, Tx interrupt is generated if enabled and the TxPktRdy bit is cleared. Cleared by CPU. Write 0 to clear it.
4	SENDSTALL	**The CPU writes 1 to this bit to issue a STALL handshake to an IN token.**

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Bit(s)	Name	Description
		The CPU clears this bit to terminate the stall condition. Note: This bit has no effect where the endpoint is used for Isochronous transfer. Otherwise, CPU should wait for SENTSTALL interrupt being generated before clearing the SENDSTALL bit.
3	FLUSHFIFO	**The CPU writes 1 to this bit to flush the latest packet from the endpoint TxFIFO.** The FIFO pointer is reset, the TxPktRdy bit is cleared and an interrupt is generated. May be set simultaneously with TxPktRdy to abort the packet that is currently being loaded into the FIFO. *Note: FlushFIFO should only be used when TxPktRdy is set. In other cases, it may cause data corruption. If the FIFO is double-buffered, FlushFIFO may need to be set twice to completely clear the FIFO.*
2	UNDERRUN	**The USB sets up this bit if an IN token is received when the TxPktRdy bit not set.** Cleared by CPU. Write 0 to clear it.
1	FIFONOTEMPTY	**The USB sets up this bit when there is at least 1 packet in TxFIFO.** This bit will be asserted automatically when TXPKTRDY is set by CPU and de-asserted when CPU flushes FIFO or sends a STALL packet.
0	TXPKTRDY	**The CPU sets up this bit after loading a data packet into FIFO.** It is cleared automatically when a data packet has been transmitted. An interrupt is also generated at this point (if enabled). TxPktRdy is also automatically cleared (interrupt is generated) prior to loading a second packet into a double-buffered FIFO.

11200012 <u>TXCSR_HOST</u> Tx CSR Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOSET			DMAREQEN	FRCDATATOG	DMAREQMODE		SETTXPKTRDY_TWICE	NAKTIMEOUT_INCOMPTX	CLRDATAOG	RXSTALL		FLUSHFIFO	ERROR	FIFONOTEMPTY	TXPKTRDY
Type	RW			RW	RW	RW		A1	A1	A0	A1		A0	A1	RU	A0
Reset	0			0	0	0		0	0	0	0		0	0	0	0

Bit(s)	Name	Description
15	AUTOSET	**If The CPU sets up this bit, TxPktRdy will be automatically set when data of the maximum packet size (value in TxMaxP) is loaded into the TxFIFO.** If a packet of less than the maximum packet size is loaded, TxPktRdy will have to be set manually.
12	DMAREQEN	**The CPU sets up this bit to enable the DMA request for the Tx endpoint.**
11	FRCDATATOG	**The CPU sets up this bit to force the endpoint data toggle to switch and the data packet to be cleared from the FIFO, regardless of whether an ACK was received.** This can be used by Interrupt Tx endpoints that are used to communicate rate feedback for Isochronous endpoints.
10	DMAREQMODE	**The CPU sets up this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0.** *Note: This bit must not be cleared either before or in the same cycle as the DMAReqEn bit is cleared.*
8	SETTXPKTRDY_TWICE	**Indicates TxPktRdy had been set when it is 1'b1 already Write 0 to clear it.**

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Bit(s)	Name	Description
7	NAKTIMEOUT_INCOMPTX	**Bulk endpoints only: This bit will be set when the Tx endpoint is halted following the receipt of NAK responses for longer than the time set as the NAK Limit by the TxInterval register.** The CPU clears this bit to allow the endpoint to continue. Write 0 to clear it.
6	CLRDATAOG	**The CPU writes 1 to this bit to reset the endpoint data toggle to 0.**
5	RXSTALL	**This bit is set when a STALL handshake is received.** When this bit is set, any DMA request that is in progress is topped, the FIFO is completely flushed, Tx interrupt is generated if enabled and the TxPktRdy bit is cleared (see below). Cleared by CPU. Write 0 to clear it.
3	FLUSHFIFO	**The CPU writes 1 to this bit to flush the latest packet from the endpoint TxFIFO.** The FIFO pointer is reset, the TxPktRdy bit is cleared and an interrupt is generated. May be set simultaneously with TxPktRdy to abort the packet that is currently being loaded into the FIFO. *Note: FlushFIFO should only be used when TxPktRdy is set. In other cases, it may cause data corruption. If the FIFO is double-buffered, FlushFIFO may need to be set twice to completely clear the FIFO.*
2	ERROR	**The USB sets up this bit when 3 attempts have been made to send a packet and no handshake packet has been received.** When the bit is set, an interrupt will be generated, TxPktRdy cleared and FIFO completely flushed. Cleared by CPU. Valid only when the endpoint is operating in Bulk or Interrupt mode. Write 0 to clear it.
1	FIFONOTEMPTY	**The USB sets up this bit when there is at least 1 packet in TxFIFO.** This bit will be asserted automatically when TXPKTRDY is set by CPU and de-asserted when CPU flushes FIFO or sends a STALL packet.
0	TXPKTRDY	**The CPU sets up this bit after loading a data packet into FIFO.** It is cleared automatically when a data packet has been transmitted. An interrupt is also generated at this point (if enabled). TxPktRdy is also automatically cleared (interrupt is generated) prior to loading a second packet into a double-buffered FIFO.

11200014 RXMAP RXMAP Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				M_1		MAXIMUM_PAYLOAD_TRANSACTION										
Type				RW		RW										
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:11	M_1	**Maximum payload size for indexed RX endpoint , M-1 Packet multiplier m**
10:0	MAXIMUM_PAYLOAD_TRANSACTION	**The RxMaxP register defines the maximum amount of data that can be transferred through the selected Rx endpoint in a single operation.** There is a RxMaxP register for each Rx endpoint (except for Endpoint 0). Bits 10:0 define (in bytes) the maximum payload transmitted in a single transaction. The value set can be up to 1024 bytes but is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full-speed and High-speed operations. Where the option of High-bandwidth Isochronous endpoints or of combining Bulk packets has been taken when the core is configured, the register includes either 2 or 5 further bits that define a multiplier m which is equal to one more

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Bit(s)	Name	Description
		than the value recorded. For Bulk endpoints with the packet combining option enabled, the multiplier m can be up to 32 and defines the number of USB packets of the specified payload which are to be combined into a single data packet within the FIFO. (If the packet splitting option is not enabled, bit15-bit13 is not implemented and bit12-bit11 (if included) is ignored.) For Isochronous endpoints operating in high-speed mode and with the high-bandwidth option enabled, m may only be either 2 or 3 (corresponding to bit 11 set or bit 12 set, respectively) and it specifies the maximum number of such transactions that can take place in a single microframe. If either bit 11 or bit 12 is non-0, the USB2.0 controller will automatically combine the separate USB packets received in any microframe into a single packet within the Rx FIFO. The maximum payload for each transaction is 1024 bytes, so this allows up to 3072 bytes to be received in each microframe. (For Isochronous/Interrupt transfers in full-speed mode or if High-bandwidth is not enabled, bits 11 and 12 are ignored.) The value written to bits 10:0 (multiplied by m in the case of high-bandwidth Isochronous transfers) must match the value given in the wMaxPacketSize field of the Standard Endpoint Descriptor for the associated endpoint . A mismatch can cause unexpected results. The total amount of data represented by the value written to this register (specified payload * m) must not exceed the FIFO size for the OUT endpoint and should not exceed half the FIFO size if double-buffering is required.

11200016 RXCSR_PERI RX CSR Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOCLEAR	ISO	DMAREQEN	DISNYET_PIDERR	DMAREQMODE		KEEPERRSTATUS	INCOMPRX	CLRDTATOG	SENTSTALL	SENDSTALL	FLUSHFIFO	DATAERR	OVERRUN	FIFOFULL	RXPKTRDY
Type	RW	RW	RW	RW	RW		RW	A1	A0	A1	RW	A0	RU	A1	RU	A1
Reset	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUTOCLEAR	**If CPU sets up this bit then the RxPktRdy bit will be automatically cleared when a packet of RxMaxP bytes has been unloaded from the RxFIFO.** When packets of less than the maximum packet size are unloaded, RxPktRdy will have to be cleared manually. *Note: The maximum packet size -3, -2, -1 is handled like the maximum packet size which is auto cleared by HW.*
14	ISO	**The CPU sets up this bit to enable the Rx endpoint for Isochronous transfers and clears it to enable the Rx endpoint for Bulk/Interrupt transfers.**
13	DMAREQEN	**The CPU sets up this bit to enable the DMA request for the Rx endpoint.**
12	DISNYET_PIDERR	**The CPU sets up this bit to disable the sending of NYET handshakes.** When set, all successfully received Rx packets are ACK'd including at the point at which the RxFIFO becomes full. Note: This bit only takes effect in high-speed mode in which it should be set for all interrupt endpoints. This bit is set when there is a PID error in the received packet. It is cleared when RxPktRdy is cleared or write 0 to clear it.
11	DMAREQMODE	**The CPU sets up this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0.** DMA Request Mode 1: Rx endpoint interrupt is generated only when DMA

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Bit(s)	Name	Description
		Request Mode 1 and received a short packet. RxDMAReq is generated when receiving a Max-Packet-size packet. DMA Request Mode 0: No Rx endpoint interrupt. RxDMAReq is generated when RxPktRdy is set.
9	KEEPERRSTATUS	**Used when endpoint works with USBQ and in Isochronous mode.** When this bit is set, the isochronous error, PIDERROR, INCOMPRX and DATAERROR will be kept and only cleared by SW.
8	INCOMPRX	**This bit will be set in an isochronous transfer if the packet in RxFIFO is incomplete because part of the data are not received.** When KeepErrorStatus = 0, it is cleared when RxPktRdy is cleared or write 0 to clear it. *Note: In anything other than an Isochronous transfer, this bit will always return to 0.* Write 0 to clear it.
7	CLRDTATOG	**The CPU writes 1 to this bit to reset the endpoint data toggle to 0.**
6	SENTSTALL	**This bit is set when a STALL handshake is transmitted.** Cleared by CPU. An interrupt will be generated when the bit is set. Write 0 to clear it.
5	SENDSTALL	**The CPU writes 1 to this bit to issue a STALL handshake.** The CPU clears this bit to terminate the stall condition. *Note: This bit has no effect where the endpoint is used for ISO transfers.*
4	FLUSHFIFO	**The CPU writes 1 to this bit to flush the next packet to be read from the endpoint RxFIFO.** The RxFIFO pointer is reset and the RxPktRdy bit is cleared. *Note: FlushFIFO should only be used when RxPktRdy is set. In other cases, it may cause data corruption. If RxFIFO is double buffered, FlushFIFO may need to be set twice to completely clear RxFIFO.*
3	DATAERR	**This bit is set when RxPktRdy is set if the data packet has a CRC or bit-stuff error.** It is cleared when RxPktRdy is cleared. *Note: This bit is only valid when the endpoint is operating in ISO mode. In Bulk mode, it always returns to 0.*
2	OVERRUN	**This bit is set if an OUT packet cannot be loaded into the RxFIFO.** Cleared by CPU (write 0 to clear it). *Note: This bit is only valid when the endpoint is operating in ISO mode. In Bulk mode, it always returns to 0. The new incoming packet will not be written to RxFIFO.* Write 0 to clear it.
1	FIFOFULL	**Set when no more packets can be loaded into RxFIFO.**
0	RXPKTRDY	**Set when a data packet has been received (to RxFIFO).** The CPU clears this bit when the packet has been unloaded from the RxFIFO. An interrupt will be generated when the bit is set. Write 0 to clear it.

11200016 RXCSR_HOST Rx CSR Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOCLEAR	AUTOREQ	DMAREQENAB	PIDERROR	DMAREQMODE	SETREQPKT_TWICE	KEEPERRSTATUS	INCOMPRX	CLRDATATOG	RXSTALL	REQPKT	FLUSHFIFO	DATAERR_NAKTIMEOUT	ERROR	FIFOFULL	RXPKTRDY
Type	RW	RW	RW	RU	RW	A1	RW	A1	A0	A1	RW	A0	A1	A1	RU	A1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15	AUTOCLEAR	**If CPU sets up this bit then the RxPktRdy bit will be automatically cleared when a packet of RxMaxP bytes has been unloaded from the RxFIFO.** When packets of less than the maximum packet size are unloaded, RxPktRdy will have to be cleared manually. *Note: The maximum packet size -3, -2, -1 is handled like the maximum packet size which is auto cleared by HW.*
14	AUTOREQ	**If CPU sets up this bit, the ReqPkt bit will be automatically set when the RxPktRdy bit is cleared.** *Note: This bit is automatically cleared when a short packet is received.*
13	DMAREQENAB	**The CPU sets up this bit to enable the DMA request for the Rx endpoint.**
12	PIDERROR	**ISO transactions only: The core sets up this bit to indicate a PID error in the received packet.** Bulk/Interrupt transactions: The setting of this bit is ignored. Write 0 to clear it. *Note: This register is read only in ISO mode but reserved for read/write access in other modes.*
11	DMAREQMODE	**The CPU sets up this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0.** DMA Request Mode 1: Rx endpoint interrupt is generated only when DMA Request Mode 1 and received a short packet. RxDMAReq is generated when receiving a Max-Packet-size packet. DMA Request Mode 0: No Rx endpoint interrupt. RxDMAReq is generated when RxPktRdy is set.
10	SETREQPKT_TWICE	**Indicates the ReqPkt had been set when it is 1 already.** Write 0 to clear it.
9	KEEPERRSTATUS	**Used when endpoint works with USBQ and in Isochronous mode.** When this bit is set, the isochronous error, PIDERROR, INCOMPRX and DATAERROR will be kept and only cleared by SW.
8	INCOMPRX	**This bit will be set in an isochronous transfer if the packet in RxFIFO is incomplete because part of the data are not received.** When KeepErrorStatus = 0, it is cleared when RxPktRdy is cleared or write 0 to clear it. *Note: In anything other than an isochronous transfer, this bit will always return to 0.* Write 0 to clear it.
7	CLRDATATOG	**The CPU writes 1 to this bit to reset the endpoint data toggle to 0.**
6	RXSTALL	**When a STALL handshake is received, this bit will be set and an interrupt generated.** Cleared by CPU. Write 0 to clear it.
5	REQPKT	**The CPU writes 1 to this bit to request an IN transaction.** Cleared when RxPktRdy is set.
4	FLUSHFIFO	**The CPU writes 1 to this bit to flush the next packet to be read from the endpoint RxFIFO.** The RxFIFO pointer is reset and the RxPktRdy bit is cleared. *Note: FlushFIFO should only be used when RxPktRdy is set. In other cases, it may cause data corruption. If RxFIFO is double buffered, FlushFIFO may need to be set twice to completely clear RxFIFO.*
3	DATAERR_NAKTIME OUT	**In Bulk mode, this bit will be set when the Rx endpoint is halted following the receipt of NAK responses for longer than the time set as the NAK Limit by the RxInterval register.** The CPU clears this bit to allow endpoint to continue. Write 0 to clear it. When operating in ISO mode, this bit is set when RxPktRdy is set if the data

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Bit(s)	Name	Description
		packet has a CRC or bit-stuff error and cleared when RxPktRdy is cleared.
2	ERROR	**The USB sets up this bit when 3 attempts have been made to receive a packet and no data packet has been received.** Cleared by CPU. An interrupt will be generated when the bit is set. *Note: This bit is only valid when the Rx endpoint is operating in Bulk or Interrupt mode. Write 0 to clear it.* In ISO mode, it always returns to 0.
1	FIFOFULL	**Set when no more packets can be loaded into RxFIFO.**
0	RXPKTRDY	**Set when a data packet has been received (to RxFIFO).** The CPU clears this bit when the packet has been unloaded from the RxFIFO. An interrupt will be generated when the bit is set. Write 0 to clear it.

11200018 RXCOUNT Rx Count Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RXCOUNT													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	RXCOUNT	**A 14-bit read-only register that holds the number of received data bytes in the packet in RxFIFO** *Note: The value returned changes as the FIFO is unloaded and is Only valid when RxPktRdy (RxCSR.D0) is set.*

1120001A TXTYPE TxType Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TX_SPEED		TX_PROTOCOL		TX_TARGET_EP_NUMBER			
Type									RW		RW		RW			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:6	TX_SPEED	**Operating speed of target device when core is configured with multipoint option** When the core is not configured with the multipoint option, these bits should not be accessed. 2'b00: Unused 2'b01: High 2'b10: Full 2'b11: Low
5:4	TX_PROTOCOL	**The CPU sets up this to select the required protocol for Tx endpoint.** 2'b00: Illegal 2'b01: Isochronous 2'b10: Bulk 2'b11: Interrupt
3:0	TX_TARGET_EP_NUMBER	**The CPU sets this value to the endpoint number contained in the Tx endpoint descriptor returned to the USB2.0 Controller during device enumeration.**

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1120001B TXINTERVAL TxInterval Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TX_POLLING_INTERVAL_NAK_LIMIT_M							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	TX_POLLING_INTERVAL_NAK_LIMIT_M	**(Host mode only) TxInterval Register TxInterval is an 8-bit register that, for Interrupt and Isochronous transfers, defines the polling interval for the currently-selected Tx endpoint.** For Bulk endpoints, this register sets the number of frames/microframes after which the endpoint should timeout on receiving a stream of NAK responses. There is a TxInterval register for each configured Tx endpoint (except for Endpoint 0). In each case the value that is set defines a number of frames/microframes (High Speed transfers), as follows: Transfer Type | Speed | Valid values (m) | Interpretation Interrupt | Low Speed or Full Speed | 1-255 | Polling interval is m frames. Interrupt | High Speed | 1-16 | Polling interval is 2^(m-1) microframes Isochronous | Full Speed or High Speed | 1-16 | Polling interval is 2^(m-1) frames/microframes Bulk | Full Speed or High Speed | 2-16 | NAK Limit is 2^(m-1) frames/microframes. *Note: Value 0 or 1 disables the NAK timeout function.*

1120001C RXTYPE RxType Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RXSPEED		RX_PROTOCOL		RX_TARGET_EP_NUMBER			
Type									RW		RW		RW			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:6	RXSPEED	**Operating speed of target device when core is configured with multipoint option** When the core is not configured with the multipoint option, these bits should not be accessed. 2'b00: Unused 2'b01: High 2'b10: Full 2'b11: Low
5:4	RX_PROTOCOL	**The CPU sets up this to select the required protocol for Tx endpoint.** 2'b00: Illegal 2'b01: Isochronous 2'b10: Bulk 2'b11: Interrupt
3:0	RX_TARGET_EP_NUMBER	**The CPU sets this value to the endpoint number contained in the Tx endpoint descriptor returned to the USB2.0 Controller during device enumeration.**

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1120001D RXINTERVAL RxInterval Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_POLLING_INTERVAL_NAK_LIMIT_M							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RX_POLLING_INTERVAL_NAK_LIMIT_M	**RxInterval Register RxInterval is an 8-bit register that, for Interrupt and Isochronous transfers, defines the polling interval for the currently-selected Rx endpoint.** For Bulk endpoints, this register sets the number of frames/microframes after which the endpoint should timeout on receiving a stream of NAK responses. There is a RxInterval register for each configured Rx endpoint (except for Endpoint 0). RX POLLING INTERVAL/NAK LIMIT (M), (Host mode only) In each case the value that is set defines a number of frames/microframes (High Speed transfers), as follows: Transfer Type Speed Valid values (m) Interpretation Interrupt Low Speed or Full Speed 1 - 255 Polling interval is m frames. High Speed 1 - 16 Polling interval is 2(m-1) microframes Isochronous Full Speed or High Speed 1 - 16 Polling interval is 2(m-1) frames/microframes Bulk Full Speed or High Speed 2 - 16 NAK Limit is 2(m-1) frames/microframes. *Note: Value 0 or 1 disables the NAK timeout function.*

1120001F FIFOSIZE Configured FIFO Size Register AA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RXFIFOSIZE				TXFIFOSIZE			
Type									DC				DC			
Reset									1	0	1	0	1	0	1	0

Bit(s)	Name	Description
7:4	RXFIFOSIZE	**Indicates RxFIFO size of 2^n bytes** Example: Value 10 means 2^10 = 1024 bytes.
3:0	TXFIFOSIZE	**Indicates TxFIFO size of 2^n bytes** Example: Value 10 means 2^10 = 1024 bytes.

11200020 FIFO0 USB Endpoint 0 FIFO Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO_DATA[31:16]															
Type	Other															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_DATA[15:0]															
Type	Other															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FIFO_DATA	**The Endpoint FIFO Registers provides 16 addresses for CPU access to the FIFOs for each endpoint.** Writing to these addresses loads data into the TxFIFO for the corresponding

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Bit(s)	Name	Description
		endpoint. Reading from these addresses unloads data from the RxFIFO for the corresponding endpoint. *Note:* *1. Transfers to and from FIFOs may be 8-bit, 16-bit or 32-bit as required, and any combination of access is allowed provided the data accessed is contiguous. However, all the transfers associated with one packet must be of the ame width so that the data is consistently byte-, word- or double-word-aligned. The last transfer may however contain fewer bytes than the previous transfers in order to complete an odd-byte or odd-word transfer. For DC/DTV projects, refer to the RISC_SIZE register to complete FIFO access.* *2. Depending on the size of the FIFO and the expected maximum packet size, the FIFOs support either single-packet or double-packet buffering. However, burst writing of multiple packets is not supported as flags need to be set after each packet is written.* *3. Following a STALL response or a Tx Strike Out error on Endpoint, the associated FIFO is completely flushed.* *(vi) Programmers don't use debug tools to monitor or read the FIFO region. The FIFO pointer will increase and cause unexpected error in MAC state machine.*

11200024 **FIFO1** **USB Endpoint 1 FIFO Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO_DATA[31:16]															
Type	Other															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_DATA[15:0]															
Type	Other															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FIFO_DATA	**The Endpoint FIFO Registers provides 16 addresses for CPU access to the FIFOs for each endpoint.** Writing to these addresses loads data into the TxFIFO for the corresponding endpoint. Reading from these addresses unloads data from the RxFIFO for the corresponding endpoint. Note: *1. Transfers to and from FIFOs may be 8-bit, 16-bit or 32-bit as required, and any combination of access is allowed provided the data accessed is contiguous. However, all the transfers associated with one packet must be of the ame width so that the data is consistently byte-, word- or double-word-aligned. The last transfer may however contain fewer bytes than the previous transfers in order to complete an odd-byte or odd-word transfer. For DC/DTV projects, refer to the RISC_SIZE register to complete FIFO access.* *2. Depending on the size of the FIFO and the expected maximum packet size, the FIFOs support either single-packet or double-packet buffering. However, burst writing of multiple packets is not supported as flags need to be set after each packet is written.* *3. Following a STALL response or a Tx Strike Out error on Endpoint, the associated FIFO is completely flushed.* *(vi) Programmers don't use debug tools to monitor or read the FIFO region. The FIFO pointer will increase and cause unexpected error in MAC state machine.*

11200060 **DEVCTL** **Device Control Register** **80**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									B_DEVICE	FSDEV	LSDEV	VBUS		HOSTMODE	HOSTREQ	SESSION
Type									RU	RU	RU	RU		RU	Other	Other
Reset									1	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	B_DEVICE	**This read-only bit indicates whether the USB2.0 controller is operating as the 'A' device or the 'B' device.** Only valid when a session is in progress. *Note: If the core is in Force_Host mode, this bit will indicate the state of the HOSTDISCON input signal from the PHY.* 1'b0: 'A' device 1'b1: 'B' device
6	FSDEV	**This read-only bit is set when a full-speed or high-speed device has been detected being connected to the port. (High-speed devices are distinguished from full-speed by checking for high-speed chirps when the device is reset.)** Only valid in host mode.
5	LSDEV	**This read-only bit is set when a low-speed device has been detected being connected to the port. Only valid in host mode.**
4:3	VBUS	**These read-only bits encode the current VBUS level; only available with OTG function enquipped; else the register value will be undefined.** 2'b00: Below SessionEnd 2'b01: Above SessionEnd, below AValid 2'b10: Above AValid, below VBusValid 2'b11: About VBusValid
2	HOSTMODE	**This read-only bit is set when the USB2.0 controller is acting as a host.**
1	HOSTREQ	**When set, the USB2.0 controller will initiate the Host Negotiation when Suspend mode is entered.** Cleared when Host Negotiation is completed ('B' device only).
0	SESSION	**When operating as an 'A' device, this bit is set or cleared by the CPU to start or end a session.** When operating as a 'B' device, this bit is set/cleared by the USB2.0 controller when a session starts/ends. It is also set by the CPU to initiate the Session Request Protocol. When the USB2.0 controller is in Suspend mode, the bit may be cleared by the CPU to perform a software disconnect. *Note: Clearing this bit when the core is not suspended will result in undefined behavior.*

11200061 PWRUPCNT Power Up Counter Register 0F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													PWRUPCNT			
Type													RW			
Reset													1	1	1	1

Bit(s)	Name	Description
3:0	PWRUPCNT	**Power-up counter limit.** The power-up counter is used to count the K state duration during suspend and when it is timed out, the resume interrupt will be issued. The register should be configured according to AHB clock speed.

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11200062 TXFIFOSZ Tx FIFO Size Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TXDPB	TXSZ			
Type												RW	RW			
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	TXDPB	**Defines whether double-packet buffering supported for TxFIFO** 0: Support only single-packet buffering 1: Support double-packet buffering
3:0	TXSZ	**Maximum packet size to be allowed for (before any splitting within the FIFO of Bulk/High-Bandwidth packets prior to transmission)** If TxDPB = 0, the FIFO will also be this size; if TxDPB = 1, the FIFO will be twice this size. TxSZ[3:0] Packet size (bytes) 4'b0000: 8 4'b0001: 16 4'b0010: 32 4'b0011: 64 4'b0100: 128 4'b0101: 256 4'b0110: 512 4'b0111: 1024 4'b1000: 2048 (Single-packet buffering only) 4'b1001: 4096 (Single-packet buffering only) Others: No support

11200063 RXFIFOSZ Rx FIFO Size Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RXDPB	RXSZ			
Type												RW	RW			
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	RXDPB	**Defines whether double-packet buffering supported for TxFIFO** 0: Support only single-packet buffering 1: Support double-packet buffering
3:0	RXSZ	**Maximum packet size to be allowed for (before any splitting within the FIFO of Bulk/High-Bandwidth packets prior to transmission)** If TxDPB = 0, the FIFO will also be this size; if TxDPB = 1, the FIFO will be twice this size RxSZ[3:0] Packet Size (bytes) 4'b0000: 8 4'b0001: 16 4'b0010: 32 4'b0011: 64 4'b0100: 128 4'b0101: 256 4'b0110: 512 4'b0111: 1024 4'b1000: 2048 (Single-packet buffering only) 4'b1001: 4096 (Single-packet buffering only) Others: No support

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11200064 TXFIFOADD Tx FIFO Address Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				TXFIFOADD												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	TXFIFOADD	**TxFIFOadd is a 13-bit register which controls the start address of the selected Tx endpoint FIFO.** TxFIFOadd[12:0] Start address 13'h0000: 0000 13'h0001: 0008 13'h0002: 0010 13'h1FFF: FFF8

11200066 RXFIFOADD Rx FIFO Address Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DataErrIntrEn	OverRUNIntrEn		RXFIFOADD												
Type	RW	RW		RW												
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	DataErrIntrEn	**Enables data error interrupt** Note: This bit is only valid when the endpoint is operating in ISO mode.
14	OverRUNIntrEn	**Enables over run interrupt** Note: this bit is only valid when the endpoint is operating in ISO mode.
12:0	RXFIFOADD	**RxFIFOadd is a 13-bit register which controls the start address of the selected Rx endpoint FIFO.** RxFIFOadd[12:0] Start address 13'h0000: 0000 13'h0001: 0008 13'h0002: 0010 13'h1FFF: FFF8

1120006C HWCAPS Hardware Capability Register 6503

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QMU_SUPPORT	HUB_SUPPORT	USB20_SUPPORT	USB11_SUPPORT	MSTR_WRAP_INTFX		SLAVE_WRAP_INTFX				USB_VERSION_CODE					
Type	RO	RO	RO	RO	DC		DC				RO					
Reset	0	1	1	0	0	1	0	1			0	0	0	0	1	1

Bit(s)	Name	Description
15	QMU_SUPPORT	**Supports QMU feature**
14	HUB_SUPPORT	**Supports HUB feature**

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Bit(s)	Name	Description
13	USB20_SUPPORT	**Supports USB2.0 feature**
12	USB11_SUPPORT	**Supports USB1.1 feature**
11:10	MSTR_WRAP_INTFX	**Configures AHB master interface** 2'b00: Mentor AHB master interface 2'b01: Asynchronous AHB master interface 2'b10: Asynchronous AXI master interface 2'b11: Asynchronous DX DRAM master interface
9:8	SLAVE_WRAP_INTFX	**Configures AHB slave interface** 2'b00: Mentor AHB slave interface 2'b01: Asynchronous AHB master interface 2'b10: Asynchronous AXI master interface 2'b11: Asynchronous DX CPU slave interface
5:0	USB_VERSION_CODE	**USB hardware version code**

1120006E HWSVERS Version Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									USB_SUB_VERSION_CODE							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	USB_SUB_VERSION_CODE	USB software version code

11200070 BUSPERF1 USB Bus Performance Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLRDMAREQEARLY_EN	SOFT_DEBOUNCE	ISO_ERR_CNT_EN	ISO_RTY_DIS		PREAMBLE_DELAY_EN	HOST_WAIT_EP0									
Type	RW	RW	RW	RW		RW	RW									
Reset	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	CLRDMAREQEARLY_EN	**If CLRDMAREQEARLY_EN = 1, DMAReq will be cleared when 8 bytes of data remain in FIFO for Rx, or TXMAXP-8 bytes will be loaded in FIFO for Tx.** If CLRDMAREQEARLY_EN = 0, DMAReq will only be cleared when Rx FIFO is read empty or TXMAXP loaded to Tx FIFO.
14	SOFT_DEBOUNCE	**If soft_debounce=0, the debounce will be implemented by HW, i.e. 120ms will be the same as before.** If soft_debounce=1, after DP/DM is stable for 1ms, connection interrupt will be generated, and SW will determine how long the delay is for debounce. This bit only affects the debounce behavior when the cable starts connection but does not affect in HNP when the cable is connected.
13	ISO_ERR_CNT_EN	**Musbhdrc has different behavior with USB spec. in HUB ISO mode.** When this bit is set, the Strike out mechanism of re-try failed will be engaged and complete the transaction.

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Bit(s)	Name	Description
12	ISO_RTY_DIS	**Musbhdrc has different behavior with USB spec. in HUB ISO mode.** This bit disables the retry of CSplit @ SOF.
10	PREAMBLE_DELAY_EN	**Host mode only and downstream port connect to hub.** This bit enables the function of host delay to issue a preamble +ack packet after receving data from LS device about 3 LS bit time.
9:0	HOST_WAIT_EP0	**Host Waiting Time of Endpoint** The written value defines the minimum cycles for controller to issue the next IN/OUT/PING token during idle state. 0: No wait. >0: In idle state, the controller must wait for at least exact cycles which are written before it issues the next IN/OUT/PING token. The cycle unit is as USB system clock cycle.

11200072 BUSPERF2 USB Bus Performance Register 2 C000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HSR_ISOICHK_DIS	HST_ISOOCHK_DIS	HOST_WAIT_EPX													
Type	RW	RW	RW													
Reset	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	HSR_ISOICHK_DIS	**Disables ISO Rx 0-packet in host mode** Optional disable selection for ISO Rx 0 packet
14	HST_ISOOCHK_DIS	**Disables ISO Tx 0-packet in host mode** Optional disable selection for ISO Rx 0 packet
13:0	HOST_WAIT_EPX	**Host Waiting Time of all Endpoints except Endpoint0** The written value defines the minimum cycles for controller to issue the next IN/OUT/PING token during idle state. 0: No wait. >0: In idle state, the controller must wait for at least exact cycles which are written before it issues the next IN/OUT/PING token. The cycle unit is as USB system clock cycle.

11200074 BUSPERF3 USB Bus Performance Register 3 0A48

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					VBUSERR_MODE		FLUSH_FIFO_EN		NOISE_STILL_SOF	BAB_CLR_EN			UNDO_SRPFIX	OTG_DEGLITCH_DISABLE	EP_SWRST	DISUSBRESET
Type					RW		RW		RW	RW			RW	RW	A0	RW
Reset					1		1		0	1			1	0	0	0

Bit(s)	Name	Description
11	VBUSERR_MODE	**Controls whether VBUS error will reset USB controller or only set up the VBUS error bit** 1'b0: Set INTRUSB.bit[7] VBUS error only 1'b1: Reset USB controller and set up INTRUSB.bit[7] VBUS error tooDataErr interrupt enable. The DataErr status bit is in RxCSR[3] and should be written

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Bit(s)	Name	Description
		0 to clear. TBD
9	FLUSH_FIFO_EN	**Enables Flush FIFO** 1'b1: Clear USBPtr0, USBPtr1 of EPx Tx by flush FIFO command. 1'b0: USBPtr0, USBPtr1 of EPx Tx cannot be cleared by flush FIFO command.
7	NOISE_STILL_SOF	**Force transmitting SOF as babble interrupt**
6	BAB_CLR_EN	**Controls babble session** 1'b0: Babble interrupt will not close session automatically. 1'b1: Babble interrupt will close session automatically.
3	UNDO_SRPFIX	**The CPU sets up this bit to recover to the original circuit of USB2.0 IP about SRP.**
2	OTG_DEGLITCH_DISABLE	**Set to 1 to disable deglitch circuit of OTG signal group VBUSVALID, AVALID and SESSEND.**
1	EP_SWRST	**SW can reset the USB MAC setting by setting this bit to 1. EP_SWRST will be cleared by HW automatically.** The MAC setting includes function address, endpoint interrupt enable/status, endpoint state and EP TX/RX CSR.
0	DISUSBRESET	**If DISUSBRESET is 0, USB MAC setting will be reset to unconfigured condition when USB bus reset is detected. SW can set this bit to 1 to disable USB MAC setting Reset by HW when USB bus reset is detected.** The HW reset MAC settings include: 1. Clear Function address register 2. Clear Index register 3. Flush all endpoint FIFO 4. Clear Control/status register a. EPN TX/RXMAXP b. EPN TX/RXCSR c. EPN TX/RXTYPE d. EPN TX/RXInterval e. EPN RXCOUNT f. EP0 CSR0 g. EP0 COUNT0 5. Enable TX/RX endpoint interrupt & Clear TX/RX interrupt status *Note: EPN TX/RX FIFOSZ/AD are not cleared.*

11200078 EPINFO Number of Tx and Rx Register 88

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RXENDPOINTS				TXENDPOINTS			
Type									RO				RO			
Reset									1	0	0	0	1	0	0	0

Bit(s)	Name	Description
7:4	RXENDPOINTS	Number of Rx endpoints implemented in the design
3:0	TXENDPOINTS	Number of Tx endpoints implemented in the design

11200079 RAMINFO Width of RAM and Number of DMA Channel Register 1B

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DMACHANS				RAMBITS			
Type									RO				DC			
Reset									0	0	0	1	1	0	1	1

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Bit(s)	Name	Description
7:4	DMACHANS	Number of DMA channels implemented in the design
3:0	RAMBITS	Width of the RAM address bus-1

1120007A LINKINFO Delay to be Applied Register 5C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									WTCON				WTID			
Type									RW				RW			
Reset									0	1	0	1	1	1	0	0

Bit(s)	Name	Description
7:4	WTCON	**Sets the wait to be applied to allow for the user's connect/disconnect filter in units of 533.3ns.** (The default setting corresponds to 2.667us.) The default value will change to be 4'h8 to meet 2.667us.
3:0	WTID	**Sets up delay to be applied from IDPULLUP being asserted to IDDIG being considered valid in units of 4.369ms.** (The default setting corresponds to 52.43ms.)

1120007B VPLEN Vbus Pulsing Charge Register 3C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									VPLEN							
Type									RW							
Reset									0	0	1	1	1	1	0	0

Bit(s)	Name	Description
7:0	VPLEN	**Sets up duration of the VBus pulsing charge in units of 136.5us.** (The default setting corresponds to 8.19ms.)

1120007C HS_EOF1 Time Buffer Available on HS Transaction Register 80

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									HS_EOF1							
Type									RW							
Reset									1	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	HS_EOF1	**Sets up high-speed transactions the time before EOF to stop beginning new transactions, in units of 133.3ns.** The default setting corresponds to 17.07us. USB2.0 IP only.

1120007D FS_EOF1 Time Buffer Available on FS Transaction Register 77

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name									FS_EOF1							
Type									RW							
Reset									0	1	1	1	0	1	1	1

Bit(s)	Name	Description
7:0	FS_EOF1	**Sets up full-speed transactions the time before EOF to stop beginning new transactions, in units of 533.3ns.** (The default setting corresponds to 63.46us.) The default value will change to be 8'hBE to meet 63.46us.

1120007E **LS_EOF1** **Time Buffer Available on LS Transaction Register** **72**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									LS_EOF1							
Type									RW							
Reset									0	1	1	1	0	0	1	0

Bit(s)	Name	Description
7:0	LS_EOF1	**Sets up Q252low-speed transactions the time before EOF to stop beginning new transactions, in units of 1.067us.** (The default setting corresponds to 121.6us.). USB2.0 IP only. The default value will change to be 8'hB6 to meet 121.6us.

1120007F **RST_INFO** **Reset Information Register** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									WTFSSE0				WTCHRP			
Type									RW				RW			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:4	WTFSSE0	**Signifies the SE0 signal duration before issuing the reset signal(for Device only).** Duration = 272.8 x WTFSSE0 + 2.5 usec. This register will only be reset when hardware is reset.
3:0	WTCHRP	**Sets up delay to be applied from detecting Reset to sending chirp K (for Device only).** The duration = 272.8 x WTCHRP + 0.1 usec. This register will only be reset when hardware is reset.

11200080 **RXTOG** **Rx Data Toggle Set/Status Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															EP1RXTOG	
Type															Other	
Reset															0	

Bit(s)	Name	Description
1	EP1RXTOG	**Receive Logical Endpoint n Data Toggle Bit Set/Status**

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Bit(s)	Name	Description
		When read, these bits indicate the current state of the Endpoint n data toggle. If enable bit is high, the bit may be written with the required setting of the data toggle. If enable is low, any value written is ignored *Note: This register is word access.* 1'b0: Logical Endpoint n RX data toggle bit = 0 1'b1: Logical Endpoint n RX data toggle bit = 1

11200082 RXTOGEN Rx Data Toggle Enable Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															EP1RXTOGEN	
Type															RW	
Reset															0	

Bit(s)	Name	Description
1	EP1RXTOGEN	**Enables Receive Logical Endpoint n Data Toggle Bit** If enable bit is set, the endpoint n data toggle can be set. *Note: This register is word access.* 1'b0: Forbid RISC writing EP n data toggle status with EP1RXTOG 1'b1: Allow RISC writing EP n data toggle status with EP1RXTOG

11200084 TXTOG Tx Data Toggle Set/Status Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															EP1TXTOG	
Type															Other	
Reset															0	

Bit(s)	Name	Description
1	EP1TXTOG	**Transmit Logical Endpoint n Data Toggle Bit Set/Status** When read, these bits indicate the current state of the Endpoint n data toggle. If enable bit is high, the bit may be written with the required setting of the data toggle. If enable is low, any value written is ignored *Note: This register is word access.* 1'b0: Logical Endpoint n TX data toggle bit = 0 1'b1: Logical Endpoint n TX data toggle bit = 1

11200086 TXTOGEN Tx Data Toggle Enable Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															EP1TXTOGEN	
Type															RW	
Reset															0	

Bit(s)	Name	Description
1	EP1TXTOGEN	**Enables Receive Logical Endpoint 1 Data Toggle Bit** If enable bit is set, the endpoint n data toggle can be set.

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Bit(s)	Name	Description
		Note: This register is word access. 1'b0: Forbid RISC writing EP n data toggle status with EP1RXTOG 1'b1: Allow RISC writing EP n data toggle status with EP1RXTOG

112000A0 **USB_L1INTS** **USB Level 1 Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**POWERDWN_INT_STATUS**	**DRVVBUS_INT_STATUS**	**IDDIG_INT_STATUS**	**VBUSVALID_INT_STATUS**	**DPDM_INT_STATUS**	**QHIF_INT_STATUS**	**QINT_STATUS**	**PSR_INT_STATUS**	**DMA_INT_STATUS**	**USBCOM_INT_STATUS**	**RX_INT_STATUS**	**TX_INT_STATUS**
Type					RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	POWERDWN_INT_STATUS	**Power-down interrupt status** When controller is in host suspend mode, VBus is valid, and DP is asserted, this bit will set. When controller is in Peripheral mode, Avalid is setting, and DP is asserted, this bit will set. When controller is in idle state, avalid is de-asserted, and linestate is in SE0, this bit will also set.
10	DRVVBUS_INT_STATUS	**DRVVBUS interrupt status** This bit shows the interrupt trigger status of DRVVBUS. The trigger polarity is determined by DRVVBUS_INT_POL. This interrupt is used in USB OTG charge pump control.
9	IDDIG_INT_STATUS	**IDDIG interrupt status** This bit shows the interrupt trigger status of IDDIG. The trigger polarity is determined by IDDIG_INT_POL. This interrupt is used in USB OTG attachment.
8	VBUSVALID_INT_STATUS	**VBUSVALID interrupt status** This bit shows the interrupt trigger status of VBUSVALID. The trigger polarity is determined by VBUSVALID_INT_POL. This interrupt is used in USB attachment to host.
7	DPDM_INT_STATUS	**DPDM interrupt status** This bit shows the interrupt trigger status of DPDM. The trigger condition is whether DP or DM goes high. This interrupt is used in USB HOST mode to detect device attachment.
6	QHIF_INT_STATUS	**USBQ HIF command interrupt status** Only valid when WiMAX Q is available.
5	QINT_STATUS	**USBQ interrupt status** Only valid when USBQ is available .
4	PSR_INT_STATUS	**Packet sequence recorder interrupt status**
3	DMA_INT_STATUS	**DMA interrupt status**
2	USBCOM_INT_STATUS	**USB common interrupt status**
1	RX_INT_STATUS	**Endpoint Rx interrupt status**
0	TX_INT_STATUS	**Endpoint Tx interrupt status**

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112000A4 USB_L1INTM USB Level 1 Interrupt Mask Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					POWERDWN_INT_UNMASK	DRVVBUS_INT_UNMASK	IDDIG_INT_UNMASK	VBUSVALID_INT_UNMASK	DPDM_INT_UNMASK	QHIF_INT_UNMASK	QINT_UNMASK	PSR_INT_UNMASK	DMA_INT_UNMASK	USBCOM_INT_UNMASK	RX_INT_UNMASK	TX_INT_UNMASK
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	POWERDWN_INT_UNMASK	**Unmasks POWERDWN interrupt** 1'b0: Mask interrupt 1'b1: Unmask interrupt
10	DRVVBUS_INT_UNMASK	**Unmasks DRVVBUS interrupt** 1'b0: Mask interrupt 1'b1: Unmask interrupt
9	IDDIG_INT_UNMASK	**Unmasks IDDIG interrupt** 1'b0: Mask interrupt 1'b1: Unmask interrupt
8	VBUSVALID_INT_UNMASK	**Unmasks VBUSVALID interrupt** 1'b0: Mask interrupt 1'b1: Unmask interrupt
7	DPDM_INT_UNMASK	**Unmasks DPDM interrupt** 1'b0: Mask interrupt 1'b1: Unmask interrupt
6	QHIF_INT_UNMASK	**Unmasks USBQ HIF command interrupt** Only valid when WiMAX Q is available. 1'b0: Mask interrupt 1'b1: Unmask interrupt
5	QINT_UNMASK	**Unmasks USBQ interrupt** Only valid when USBQ is available . 1'b0: Mask interrupt 1'b1: Unmask interrupt
4	PSR_INT_UNMASK	**Unmasks packet sequence recorder interrupt** 1'b0: Mask interrupt 1'b1: Unmask interrupt
3	DMA_INT_UNMASK	**Unmasks DMA interrupt** 1'b0: Mask interrupt 1'b1: Unmask interrupt
2	USBCOM_INT_UNMASK	**Unmasks USB common interrupt** 1'b0: Mask interrupt 1'b1: Unmask interrupt
1	RX_INT_UNMASK	**Unmasks endpoint Rx interrupt** 1'b0: Mask interrupt 1'b1: Unmask interrupt
0	TX_INT_UNMASK	**Unmasks endpoint Tx interrupt** 1'b0: Mask interrupt

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Bit(s)	Name	Description
		1'b1: Unmask interrupt

112000A8 USB_L1INTP USB Level 1 Interrupt Polarity Register 00000200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					POWERDWN_INT_POL	DRVVBUS_INT_POL	IDDIG_INT_POL	VBUSVALID_INT_POL								
Type					RW	RW	RW	RW								
Reset					0	0	1	0								

Bit(s)	Name	Description
11	POWERDWN_INT_POL	**POWERDWN interrupt polarity** 1'b0: Interrupt trigger when POWERDWN is 1. 1'b1: Interrupt trigger when POWERDWN is 0.
10	DRVVBUS_INT_POL	**DRVVBUS interrupt polarity** 1'b0: Interrupt trigger when DRVVBUS is 1. 1'b1: Interrupt trigger when DRVVBUS is 0.
9	IDDIG_INT_POL	**IDDIG interrupt polarity** 1'b0: Interrupt trigger when IDDIG is 1. 1'b1: Interrupt trigger when IDDIG is 0.
8	VBUSVALID_INT_POL	**VBUSVALID interrupt polarity** 1'b0: Interrupt trigger when VBUSVALID is 1. 1'b1: Interrupt trigger when VBUSVALID is 0.

112000AC USB_L1INTC USB Level 1 Interrupt Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																USB_INT_SYNC
Type																RW
Reset																0

Bit(s)	Name	Description
0	USB_INT_SYNC	**USB interrupt synchronization** 1'b0: USB output interrupt is output directly. 1'b1: USB output interrupt is synchronized by MCU BUS clock registers.

11200102 CSR0_PERI EP0 Control Status Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name								FLUSHFIFO	SERVICESETUPEDN	SERVICEDRXPKTRDY	SENDSTALL	SETUPEND	DATAEND	SENTSTALL	TXPKTRDY	RXPKTRDY
Type								A0	A0	A0	A0	RU	A0	RW	A0	RU
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8	FLUSHFIFO	**The CPU writes 1 to this bit to flush the next packet to be transmitted/read from the Endpoint 0 FIFO. It is cleared automatically.** The FIFO pointer is reset and the TxPktRdy/RxPktRdy bit (below) is cleared. May be set simultaneously with TxPktRdy to abort the packet that is currently being loaded into the FIFO. *Note: FlushFIFO should only be used when TxPktRdy/RxPktRdy is set. In other cases, it may cause data corruption.*
7	SERVICESETUPEDN	**The CPU writes 1 to this bit to clear the SetupEnd bit.** It is cleared automatically.
6	SERVICEDRXPKTRDY	**The CPU writes 1 to this bit to clear the RxPktRdy bit.** It is cleared automatically.
5	SENDSTALL	**The CPU writes 1 to this bit to terminate the current transaction.** The STALL handshake will be transmitted and then this bit will be cleared automatically. *Note: The FIFO should be flushed before SendStall is set.*
4	SETUPEND	**This bit will be set when a control transaction ends before the DataEnd bit has been set.** An interrupt will be generated and the FIFO flushed at this time. The bit is cleared by the CPU writing 1 to the ServicedSetupEnd bit.
3	DATAEND	**The CPU sets up this bit: When setting TxPktRdy for the last data packet.** When clearing RxPktRdy after unloading the last data packet. When setting TxPktRdy for a 0 length data packet. It is cleared automatically.
2	SENTSTALL	**This bit is set when a STALL handshake is transmitted. Cleared by CPU.** Write 0 to clear it.
1	TXPKTRDY	**The CPU sets up this bit after loading a data packet into FIFO.** It is cleared automatically when a data packet has been transmitted. An interrupt is also generated at this point (if enabled).
0	RXPKTRDY	**This bit is set when a data packet has been received.** An interrupt is generated when this bit is set. The CPU clears this bit by setting up the ServicedRxPktRdy bit.

11200102 **CSR0_HOST** **EP0 Control Status Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DISPING			FLUSHFIFO	NAKTIMEOUT	STATUSPKT	REQPKT	ERROR	SETUPPKT	RXSTALL	TXPKTRDY	RXPKTRDY
Type					RW			A0	A1	RW	RW	A1	A1	A1	A0	A1
Reset					0			0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	DISPING	**The CPU writes 1 to this bit to disable transmitting PING token.** This bit can be set together with TXPKTRDY. To clear DISPING function, SW can write 0 after each control transfer is done.

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Bit(s)	Name	Description
		The DisPing function will be cleared when the next SETUP transaction is finished or OUT transaction receive handshake token with NAK/NYET/Timeout. Read "1" only in USB11 configuration. Token PING is not supported in FS mode. USB2.0 IP for TX only.
8	FLUSHFIFO	**The CPU writes 1 to this bit to flush the next packet to be transmitted/read from the Endpoint 0 FIFO.** It is cleared automatically. The FIFO pointer is reset and the TxPktRdy/RxPktRdy bit (below) is cleared. May be set simultaneously with TxPktRdy to abort the packet that is currently being loaded into the FIFO. *Note: FlushFIFO should only be used when TxPktRdy/RxPktRdy is set. In other cases, it may cause data corruption.*
7	NAKTIMEOUT	**This bit will be set when Endpoint 0 is halted following the receipt of NAK responses for longer than the time set by the NAKLimit0 register.** The CPU clears this bit to allow the endpoint to continue. Write 0 to clear it.
6	STATUSPKT	**The CPU sets up this bit at the same time as the TxPktRdy or ReqPkt bit is set, to perform a status stage transaction.** Setting this bit ensures that the data toggle is set to 1 so that a DATA1 packet is used for the Status Stage transaction.
5	REQPKT	**The CPU writes 1 to this bit to request an IN transaction.** Cleared when RxPktRdy is set.
4	ERROR	**This bit will be set when three attempts have been made to perform a transaction with no response from the peripheral.** Cleared by CPU. An interrupt is generated when this bit is set. Write 0 to clear it.
3	SETUPPKT	**The CPU sets up this bit, at the same time as the TxPktRdy bit is set, to send a SETUP token instead of an OUT token for the transaction.** This bit will be automatically clear by HW when setup packet is transmitted. *Note: Setting this bit also clears the DataToggle.*
2	RXSTALL	**This bit is set when a STALL handshake is received.** Cleared by CPU. Write 0 to clear it.
1	TXPKTRDY	**The CPU sets up this bit after loading a data packet into FIFO.** It is cleared automatically when a data packet has been transmitted. An interrupt is also generated at this point (if enabled).
0	RXPKTRDY	**This bit is set when a data packet has been received.** An interrupt is generated when this bit is set. The CPU clears this bit by setting up the ServicedRxPktRdy bit. Write 0 to clear it.

11200108 COUNT0 EP0 Received Bytes Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										EP0_RX_COUNT						
Type										RU						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	EP0_RX_COUNT	**Count0 is a 7-bit read-only register that indicates the number of received data bytes in the Endpoint 0 FIFO.** The value returned changes as the contents of the FIFO change and is Only valid when RxPktRdy (IDXEPR0.CSR0.bit0) is set.

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1120010A Type0 EP0 Type Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EP0_Type							
Type									RW							
Reset									0	0						

Bit(s)	Name	Description
7:6	EP0_Type	**Operating speed of target device when core is configured with multipoint option.** When the core is not configured with the multipoint option, these bits should not be accessed. 2'b00: Unused 2'b01: High 2'b10: Full 2'b11: Low

1120010B NAKLIMT0 NAK Limit Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												NAKLIMIT0				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	NAKLIMIT0	**(Host mode only) NAKLimit0 is a 5-bit register that sets the number of frames/microframes (High-Speed transfers) after which Endpoint 0 should timeout on receiving a stream of NAK responses.** (Equivalent settings for other endpoints can be made through their TxInterval and RxInterval registers.). The number of frames/microframes selected is 2(m-1) (where m is the value set in the register, valid values 2 - 16). If the host receives NAK responses from the target for more frames than the number represented by the Limit set in this register, the endpoint will be halted. *Note: Value 0 or 1 disables the NAK timeout function.*

1120010C SRAMCONFIGSIZE SRAM Size Register 0800

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRAM_SIZE															
Type	RO															
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SRAM_SIZE	**Depth of SRAM with data bus width 32 bits** For example, if the SRAM is configured to 8KB, SRAM_SIZE will be 16'h800.

1120010E HBCONFIGDA High Bind-width Configuration Register 88

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									NUM_HB_EPR				NUM_HB_EPT			
Type									RO				RO			
Reset									1	0	0	0	1	0	0	0

Bit(s)	Name	Description
7:4	NUM_HB_EPR	Number of high bind-width RX endpoints
3:0	NUM_HB_EPT	Number of high bind-width TX endpoints

1120010F CONFIGDATA Core Configuration Register 1F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MPRXE	MPTXE	BIGENDIAN	HBRXE	HBTXE	DYNFIFOSIZING	SOFTCONE	UTMIDATAWIDTH
Type									RO	RO	RO	RO	RO	RO	RO	RO
Reset									0	0	0	1	1	1	1	1

Bit(s)	Name	Description
7	MPRXE	**When set to 1, automatic amalgamation of bulk packets will be selected.**
6	MPTXE	**When set to 1, automatic splitting of bulk packets will be selected.**
5	BIGENDIAN	**Set to 1 indicates Big Endian order will be selected.**
4	HBRXE	**Set to 1 indicates High-bandwidth Rx ISO Endpoint Support is selected.**
3	HBTXE	**Set to 1 indicates High-bandwidth Tx ISO Endpoint Support is selected.**
2	DYNFIFOSIZING	**Set to 1 indicates Dynamic FIFO sizing option is selected.**
1	SOFTCONE	**Set to 1 indicates Soft Connect/Disconnect option is selected.**
0	UTMIDATAWIDTH	**Indicates selected UTMI+ data width** 1'b0: 8 bits 1'b1: 16 bits

11200110 TX1MAP TX1MAP Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				M1		MAXIMUM_PAYLOAD_TRANSACTION										
Type				RW		RW										
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:11	M1	**Maximum payload size for indexed TX endpoint, M1 Packet multiplier m maximum payload transaction register**
10:0	MAXIMUM_PAYLOAD_TRANSACTION	**The TxMaxP register defines the maximum amount of data that can be transferred through the selected Tx endpoint in asingle operation.** There is a TxMaxP register for each Tx endpoint (except for Endpoint 0).Bits 10:0 define (in bytes) the maximum payload transmitted in a single transaction. The value set can be up to 1024 bytes but is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt

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Bit(s)	Name	Description
		and Isochronous transfers in full-speed and high-speed operations. Where the option of High-bandwidth Isochronous endpoints or of packet splitting on Bulk endpoints has been taken when the core is configured, the register includes either 2 or 5 further bits that define a multiplier m which is equal to one more than the value recorded. In the case of Bulk endpoints with the packet splitting option enabled, the multiplier m can be up to 32 and defines the maximum number of 'USB' packets (i.e. packets for transmission over the USB) of the specified payload into which a single data packet placed in the FIFO should be split, prior to transfer. (If the packet splitting option is not enabled, bit15-13 will not be implemented and bit12-11 (if included) will be ignored.) *Note: The data packet is required to be an exact multiple of the payload specified by bits 10:0, which is itself required to be either 8, 16, 32, 64 or (in the case of high-speed transfers) 512 bytes. For Isochronous endpoints operating in high-speed mode and with the high-bandwidth option enabled, m may only be either 2 or 3 (corresponding to bit 11 set or bit 12 set, respectively) and it specifies the maximum number of such transactions that can take place in a single microframe. If either bit 11 or bit 12 is non-0, the USB2.0 controller will automatically split any data packet written to the FIFO into up to 2 or 3 'USB' packets, each containing the specified payload (or less). The maximum payload for each transaction is 1024 bytes, so this allows up to 3072 bytes to be transmitted in each microframe. (For Isochronous/Interrupt transfers in Full-speed mod, bits 11 and 12 are ignored.) The value written to bits 10:0 (multiplied by m in the case of high-bandwidth Isochronous transfers) must match the value given in the wMaxPacketSize field of the Standard Endpoint Descriptor for the associated endpoint . A mismatch can cause unexpected results. The total amount of data represented by the value written to this register (specified payload * m) must not exceed the FIFO size for the Tx endpoint and should not exceed half the FIFO size if double-buffering is required. If this register is changed after packets have been sent from the endpoint, the Tx endpoint FIFO should be completely flushed (using the FlushFIFO bit in TxCSR) after writing the new value to this register.*

11200112 TX1CSR_PERI Tx1 CSR Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOSET	ISO		DMAREQEN	FRCDATATOG	DMAREQMODE		SETTXPKTRDY_TWICE	INCOMPTX	CLRDATATOG	SENTSTALL	SENDSTALL	FLUSHFIFO	UNDERRUN	FIFONOTEMPTY	TXPKTRDY
Type	RW	RW		RW	RW	RW		A1	A1	A0	A1	RW	A0	A1	RU	A0
Reset	0	0		0	0	0		0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUTOSET	**If The CPU sets up this bit, TxPktRdy will be automatically set when data of the maximum packet size (value in TxMaxP) is loaded into the TxFIFO.** If a packet of less than the maximum packet size is loaded, TxPktRdy will have to be set manually.
14	ISO	**The CPU sets up this bit to enable the Tx endpoint for Isochronous transfers and clears it to enable the Tx endpoint for Bulk or Interrupt transfers.** *Note: This bit only has any effect in Peripheral mode. In host mode, it always returns to 0.*
12	DMAREQEN	**The CPU sets up this bit to enable the DMA request for the Tx endpoint.**

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Bit(s)	Name	Description
11	FRCDATATOG	**The CPU sets up this bit to force the endpoint data toggle to switch and the data packet to be cleared from the FIFO, regardless of whether an ACK was received.** This can be used by Interrupt Tx endpoints that are used to communicate rate feedback for Isochronous endpoints.
10	DMAREQMODE	**The CPU sets up this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0.** *Note: This bit must not be cleared either before or in the same cycle as the DMAReqEn bit is cleared.*
8	SETTXPKTRDY_TWICE	**Indicates TxPktRdy had been set when it is 1'b1 already** Write 0 to clear it.
7	INCOMPTX	**When the endpoint is used for high-bandwidth Isochronous/Interrupt transfers, this bit is set to indicate where a large packet has been split into 2 or 3 packets for transmission but insufficient IN tokens have been received to send all the parts.** *Note: In anything other than a high-bandwidth transfer, this bit will always return to 0.* Write 0 to clear it.
6	CLRDATATOG	**The CPU writes 1 to this bit to reset the endpoint data toggle to 0.**
5	SENTSTALL	**This bit is set when a STALL handshake is transmitted.** The FIFO is flushed, Tx interrupt is generated if enabled and the TxPktRdy bit is cleared. Cleared by CPU. Write 0 to clear it.
4	SENDSTALL	**The CPU writes 1 to this bit to issue a STALL handshake to an IN token. The CPU clears this bit to terminate the stall condition.** *Note: This bit has no effect where the endpoint is used for Isochronous transfer. Otherwise, CPU should wait for SENTSTALL interrupt being generated before clearing the SENDSTALL bit.*
3	FLUSHFIFO	**The CPU writes 1 to this bit to flush the latest packet from the endpoint TxFIFO.** The FIFO pointer is reset, the TxPktRdy bit is cleared and an interrupt is generated. May be set simultaneously with TxPktRdy to abort the packet that is currently being loaded into the FIFO. *Note: FlushFIFO should only be used when TxPktRdy is set. In other cases, it may cause data corruption. If the FIFO is double-buffered, FlushFIFO may need to be set twice to completely clear the FIFO.*
2	UNDERRUN	**The USB sets up this bit if an IN token is received when the TxPktRdy bit not set.** Cleared by CPU (write 0 to clear it).
1	FIFONOTEMPTY	**The USB sets up this bit when there is at least 1 packet in TxFIFO.** This bit will be asserted automatically when TXPKTRDY is set by CPU and de-asserted when CPU flushes FIFO or sends a STALL packet.
0	TXPKTRDY	**The CPU sets up this bit after loading a data packet into FIFO.** It is cleared automatically when a data packet has been transmitted. An interrupt is also generated at this point (if enabled). TxPktRdy is also automatically cleared (interrupt is generated) prior to loading a second packet into a double-buffered FIFO.

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11200112 **<u>TX1CSR_HOST</u>** **Tx1 CSR Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTO SET			DMA REQE	FRCD ATAT	DMA REQ		SETT XPKT	NAKT IMEO	CLRD ATAO	RXST ALL		FLUS HFIF	ERRO R	FIFO NOTE	TXPK TRDY

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				N	OG	MOD E		RDY_ TWIC E	UT_I NCO MPT X	G			O		MPTY	
Type	RW			RW	RW	RW		A1	A1	A0	A1		A0	A1	RU	A0
Reset	0			0	0	0		0	0	0	0		0	0	0	0

Bit(s)	Name	Description
15	AUTOSET	**If The CPU sets up this bit, TxPktRdy will be automatically set when data of the maximum packet size (value in TxMaxP) is loaded into the TxFIFO.** If a packet of less than the maximum packet size is loaded, TxPktRdy will have to be set manually.
12	DMAREQEN	**The CPU sets up this bit to enable the DMA request for the Tx endpoint.**
11	FRCDATATOG	**The CPU sets up this bit to force the endpoint data toggle to switch and the data packet to be cleared from the FIFO, regardless of whether an ACK was received.** This can be used by Interrupt Tx endpoints that are used to communicate rate feedback for Isochronous endpoints.
10	DMAREQMODE	**The CPU sets up this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0.** *Note: This bit must not be cleared either before or in the same cycle as the DMAReqEn bit is cleared.*
8	SETTXPKTRDY_TWICE	**Indicates TxPktRdy had been set when it is 1'b1 already** Write 0 to clear it.
7	NAKTIMEOUT_INCOMPTX	**Bulk endpoints only: This bit will be set when the Tx endpoint is halted following the receipt of NAK responses for longer than the time set as the NAK Limit by the TxInterval register.** The CPU clears this bit to allow the endpoint to continue. Write 0 to clear it.
6	CLRDATAOG	**The CPU writes 1 to this bit to reset the endpoint data toggle to 0.**
5	RXSTALL	**This bit is set when a STALL handshake is received.** When this bit is set, any DMA request that is in progress is topped, the FIFO is completely flushed, Tx interrupt is generated if enabled and the TxPktRdy bit is cleared (see below). Cleared by CPU. Write 0 to clear it.
3	FLUSHFIFO	**The CPU writes 1 to this bit to flush the latest packet from the endpoint TxFIFO.** The FIFO pointer is reset, the TxPktRdy bit is cleared and an interrupt is generated. May be set simultaneously with TxPktRdy to abort the packet that is currently being loaded into the FIFO. *Note: FlushFIFO should only be used when TxPktRdy is set. In other cases, it may cause data corruption. If the FIFO is double-buffered, FlushFIFO may need to be set twice to completely clear the FIFO.*
2	ERROR	**The USB sets up this bit when 3 attempts have been made to send a packet and no handshake packet has been received.** When the bit is set, an interrupt will be generated, TxPktRdy cleared and FIFO completely flushed. Cleared by CPU. Valid only when the endpoint is operating in Bulk or Interrupt mode. Write 0 to clear it.
1	FIFONOTEMPTY	**The USB sets up this bit when there is at least 1 packet in TxFIFO.** This bit will be asserted automatically when TXPKTRDY is set by CPU and de-asserted when CPU flushes FIFO or sends a STALL packet.
0	TXPKTRDY	**The CPU sets up this bit after loading a data packet into FIFO.** It is cleared automatically when a data packet has been transmitted. An interrupt is also generated at this point (if enabled). TxPktRdy is also automatically cleared (interrupt is generated) prior to loading a second packet

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Bit(s)	Name	Description
		into a double-buffered FIFO.

11200114 RX1MAP RX1MAP Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				M1		MAXIMUM_PAYLOAD_TRANSACTION										
Type				RW		RW										
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:11	M1	**Maximum payload size for indexed RX endpoint, M1 Packet multiplier m**
10:0	MAXIMUM_PAYLOAD_TRANSACTION	**The RxMaxP register defines the maximum amount of data that can be transferred through the selected Rx endpoint in a single operation.** There is a RxMaxP register for each Rx endpoint (except for Endpoint 0). Bits 10:0 define (in bytes) the maximum payload transmitted in a single transaction. The value set can be up to 1024 bytes but is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full-speed and High-speed operations. Where the option of High-bandwidth Isochronous endpoints or of combining Bulk packets has been taken when the core is configured, the register includes either 2 or 5 further bits that define a multiplier m which is equal to one more than the value recorded. For Bulk endpoints with the packet combining option enabled, the multiplier m can be up to 32 and defines the number of USB packets of the specified payload which are to be combined into a single data packet within the FIFO. (If the packet splitting option is not enabled, bit15-bit13 is not implemented and bit12-bit11 (if included) is ignored.) For Isochronous endpoints operating in high-speed mode and with the high-bandwidth option enabled, m may only be either 2 or 3 (corresponding to bit 11 set or bit 12 set, respectively) and it specifies the maximum number of such transactions that can take place in a single microframe. If either bit 11 or bit 12 is non-0, the USB2.0 controller will automatically combine the separate USB packets received in any microframe into a single packet within the Rx FIFO. The maximum payload for each transaction is 1024 bytes, so this allows up to 3072 bytes to be received in each microframe. (For Isochronous/Interrupt transfers in full-speed mode or if High-bandwidth is not enabled, bits 11 and 12 are ignored.) The value written to bits 10:0 (multiplied by m in the case of high-bandwidth Isochronous transfers) must match the value given in the wMaxPacketSize field of the Standard Endpoint Descriptor for the associated endpoint . A mismatch can cause unexpected results. The total amount of data represented by the value written to this register (specified payload * m) must not exceed the FIFO size for the OUT endpoint and should not exceed half the FIFO size if double-buffering is required.

11200116 RX1CSR_PERI RX1 CSR Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOCLEAR	ISO	DMAREQEN	DISNYET_PIDERR	DMAREQMODE		KEEPERRSTATUS	INCOMPRX	CLRDATATOG	SENTSTALL	SENDSTALL	FLUSHFIFO	DATAERR	OVERRUN	FIFOFULL	RXPKTRDY
Type	RW	RW	RW	RW	RW		RW	A1	A0	A1	RW	A0	RU	A1	RU	A1
Reset	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15	AUTOCLEAR	**If CPU sets up this bit then the RxPktRdy bit will be automatically cleared when a packet of RxMaxP bytes has been unloaded from the RxFIFO.** When packets of less than the maximum packet size are unloaded, RxPktRdy will have to be cleared manually. *Note: The maximum packet size -3, -2, -1 is handled like the maximum packet size which is auto cleared by HW.*
14	ISO	**The CPU sets up this bit to enable the Rx endpoint for Isochronous transfers and clears it to enable the Rx endpoint for Bulk/Interrupt transfers.**
13	DMAREQEN	**The CPU sets up this bit to enable the DMA request for the Rx endpoint.**
12	DISNYET_PIDERR	**The CPU sets up this bit to disable the sending of NYET handshakes.** When set, all successfully received Rx packets are ACK'd including at the point at which the RxFIFO becomes full. Note: This bit only takes effect in high-speed mode in which it should be set for all interrupt endpoints. This bit is set when there is a PID error in the received packet. It is cleared when RxPktRdy is cleared or write 0 to clear it.
11	DMAREQMODE	**The CPU sets up this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0.** DMA Request Mode 1: Rx endpoint interrupt is generated only when DMA Request Mode 1 and received a short packet. RxDMAReq is generated when receiving a Max-Packet-size packet.DMA Request Mode 0: No Rx endpoint interrupt. RxDMAReq is generated when RxPktRdy is set.
9	KEEPERRSTATUS	**Used when endpoint works with USBQ and in Isochronous mode** When this bit is set, the isochronous error, PIDERROR, INCOMPRX and DATAERROR will be kept and only cleared by SW.
8	INCOMPRX	**This bit will be set in an isochronous transfer if the packet in RxFIFO is incomplete because part of the data are not received.** When KeepErrorStatus = 0, it is cleared when RxPktRdy is cleared or write 0 to clear it. *Note: In anything other than an isochronous transfer, this bit will always return to 0.* Write 0 to clear it.
7	CLRDTATOG	**The CPU writes 1 to this bit to reset the endpoint data toggle to 0.**
6	SENTSTALL	**This bit is set when a STALL handshake is transmitted.** Cleared by CPU. An interrupt will be generated when the bit is set. Write 0 to clear it.
5	SENDSTALL	**The CPU writes 1 to this bit to issue a STALL handshake.** The CPU clears this bit to terminate the stall condition. *Note: This bit has no effect where the endpoint is used for ISO transfers.*
4	FLUSHFIFO	**The CPU writes 1 to this bit to flush the next packet to be read from the endpoint RxFIFO.** The RxFIFO pointer is reset and the RxPktRdy bit is cleared. *Note: FlushFIFO should only be used when RxPktRdy is set. In other cases, it may cause data corruption. If RxFIFO is double buffered, FlushFIFO may need to be set twice to completely clear RxFIFO.*
3	DATAERR	**This bit is set when RxPktRdy is set if the data packet has a CRC or bit-stuff error.** It is cleared when RxPktRdy is cleared. *Note: This bit is only valid when the endpoint is operating in ISO mode. In Bulk mode, it always returns to 0.*
2	OVERRUN	**This bit is set if an OUT packet cannot be loaded into the RxFIFO.** Cleared by CPU (write 0 to clear it).

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Bit(s)	Name	Description
		Note: This bit is only valid when the endpoint is operating in ISO mode. In Bulk mode, it always returns to 0. The new incoming packet will not be written to RxFIFO.
1	FIFOFULL	**Set when no more packets can be loaded into RxFIFO.**
0	RXPKTRDY	**Set when a data packet has been received (to RxFIFO).** The CPU clears this bit when the packet has been unloaded from the RxFIFO. An interrupt will be generated when the bit is set. Write 0 to clear it.

11200116 **RX1CSR_HOST** **Rx1 CSR Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOCLEAR	AUTOREQ	DMAREQENAB	PIDERROR	DMAREQMODE	SETREQPKT_TWICE	KEEPERRSTATUS	INCOMPRX	CLRDATATOG	RXSTALL	REQPKT	FLUSHFIFO	DATAERR_NAKTIMEOUT	ERROR	FIFOFULL	RXPKTRDY
Type	RW	RW	RW	RU	RW	A1	RW	A1	A0	A1	RW	A0	A1	A1	RU	A1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUTOCLEAR	**If CPU sets up this bit then the RxPktRdy bit will be automatically cleared when a packet of RxMaxP bytes has been unloaded from the RxFIFO.** When packets of less than the maximum packet size are unloaded, RxPktRdy will have to be cleared manually. *Note: The maximum packet size -3, -2, -1 is handled like the maximum packet size which is auto cleared by HW.*
14	AUTOREQ	**If CPU sets up this bit, the ReqPkt bit will be automatically set when the RxPktRdy bit is cleared.** *Note: This bit is automatically cleared when a short packet is received.*
13	DMAREQENAB	**The CPU sets up this bit to enable the DMA request for the Rx endpoint.**
12	PIDERROR	**ISO transactions only: The core sets up this bit to indicate a PID error in the received packet. Bulk/Interrupt transactions: The setting of this bit is ignored.** Write 0 to clear it. *Note: This register is read only in ISO mode but reserved for read/write access in other modes.*
11	DMAREQMODE	**The CPU sets up this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0.** DMA Request Mode 1: Rx endpoint interrupt is generated only when DMA Request Mode 1 and received a short packet. RxDMAReq is generated when receiving a Max-Packet-size packet.DMA Request Mode 0: No Rx endpoint interrupt. RxDMAReq is generated when RxPktRdy is set.
10	SETREQPKT_TWICE	**Indicates the ReqPkt had been set when it is 1 already** Write 0 to clear it.
9	KEEPERRSTATUS	**Used when endpoint works with USBQ and in Isochronous mode.** When this bit is set, the isochronous error, PIDERROR, INCOMPRX and DATAERROR will be kept and only cleared by SW.
8	INCOMPRX	**This bit will be set in an isochronous transfer if the packet in RxFIFO is incomplete because part of the data are not received.** When KeepErrorStatus = 0, it is cleared when RxPktRdy is cleared or write 0

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Bit(s)	Name	Description
		to clear it. *Note: In anything other than an isochronous transfer, this bit will always return to 0.* Write 0 to clear it.
7	CLRDATATOG	**The CPU writes 1 to this bit to reset the endpoint data toggle to 0.**
6	RXSTALL	**When a STALL handshake is received, this bit will be set and an interrupt generated. Cleared by CPU.** Write 0 to clear it.
5	REQPKT	**The CPU writes 1 to this bit to request an IN transaction.** Cleared when RxPktRdy is set.
4	FLUSHFIFO	**The CPU writes 1 to this bit to flush the next packet to be read from the endpoint RxFIFO.** The RxFIFO pointer is reset and the RxPktRdy bit is cleared. *Note: FlushFIFO should only be used when RxPktRdy is set. In other cases, it may cause data corruption. If RxFIFO is double buffered, FlushFIFO may need to be set twice to completely clear RxFIFO.*
3	DATAERR_NAKTIMEOUT	**In Bulk mode, this bit will be set when the Rx endpoint is halted following the receipt of NAK responses for longer than the time set as the NAK Limit by the RxInterval register.** The CPU clears this bit to allow endpoint to continue. Write 0 to clear it. When operating in ISO mode, this bit is set when RxPktRdy is set if the data packet has a CRC or bit-stuff error and cleared when RxPktRdy is cleared.
2	ERROR	**The USB sets up this bit when 3 attempts have been made to receive a packet and no data packet has been received.** Cleared by CPU. An interrupt will be generated when the bit is set. Note: This bit is only valid when the Rx endpoint is operating in Bulk or Interrupt mode. In ISO mode, it always returns to 0. Write 0 to clear it.
1	FIFOFULL	**Set when no more packets can be loaded into RxFIFO.**
0	RXPKTRDY	**Set when a data packet has been received (to RxFIFO).** The CPU clears this bit when the packet has been unloaded from the RxFIFO. An interrupt will be generated when the bit is set. Write 0 to clear it.

11200118 **RX1COUNT** **Rx1 Count Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RXCOUNT													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	RXCOUNT	**A 14-bit read-only register that holds the number of received data bytes in the packet in RxFIFO** *Note: The value returned changes as FIFO is unloaded and is only valid when RxPktRdy(RxCSR.D0) is set.*

1120011A **TX1TYPE** **Tx1Type Register** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TX_SPEED		TX_PROTOCOL		TX_TARGET_EP_NUMBER			

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Type									RW		RW		RW			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:6	TX_SPEED	**Operating speed of target device when core is configured with multipoint option** When the core is not configured with the multipoint option, these bits should not be accessed. 2'b00: Unused 2'b01: High 2'b10: Full 2'b11: Low
5:4	TX_PROTOCOL	**The CPU sets up this to select the required protocol for the Tx endpoint.** 2'b00: Illegal 2'b01: Isochronous 2'b10: Bulk 2'b11: Interrupt
3:0	TX_TARGET_EP_NUMBER	**The CPU sets this value to the endpoint number contained in the Tx endpoint descriptor returned to the USB2.0 Controller during device enumeration.**

1120011B **TX1INTERVAL** **Tx1Interval Register** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TX_POLLING_INTERVAL_NAK_LIMIT_M							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	TX_POLLING_INTERVAL_NAK_LIMIT_M	**(Host mode only) TxInterval Register TxInterval is an 8-bit register that, for Interrupt and Isochronous transfers, defines the polling interval for the currently-selected Tx endpoint.** For Bulk endpoints, this register sets the number of frames/microframes after which the endpoint should timeout on receiving a stream of NAK responses. There is a TxInterval register for each configured Tx endpoint (except for Endpoint 0). In each case the value that is set defines a number of frames/microframes (High Speed transfers), as follows: Transfer Type | Speed | Valid values (m) | Interpretation Interrupt | Low Speed or Full Speed | 1-255 | Polling interval is m frames. Interrupt | High Speed | 1-16 | Polling interval is 2^(m-1) microframes Isochronous | Full Speed or High Speed | 1-16 | Polling interval is 2^(m-1) frames/microframes Bulk | Full Speed or High Speed | 2-16 | NAK Limit is 2^(m-1) frames/microframes. *Note: Value 0 or 1 disables the NAK timeout function. The register should be set before TxType for Bulk endpoint.*

1120011C **RX1TYPE** **Rx1Type Register** **00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RXSPEED		RX_PROTOCOL		RX_TARGET_EP_NUMBER			
Type									RW		RW		RW			
Reset									0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
7:6	RXSPEED	**Operating speed of target device when core is configured with multipoint option** When the core is not configured with the multipoint option, these bits should not be accessed. 2'b00: Unused 2'b01: High 2'b10: Full 2'b11: Low
5:4	RX_PROTOCOL	**The CPU sets up this to select the required protocol for the Tx endpoint.** 2'b00: Illegal 2'b01: Isochronous 2'b10: Bulk 2'b11: Interrupt
3:0	RX_TARGET_EP_NUMBER	**The CPU sets this value to the endpoint number contained in the Tx endpoint descriptor returned to the USB2.0 Controller during device enumeration.**

1120011D RX1INTERVAL Rx1Interval Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_POLLING_INTERVAL_NAK_LIMIT_M							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RX_POLLING_INTERVAL_NAK_LIMIT_M	**RxInterval Register RxInterval is an 8-bit register that, for Interrupt and Isochronous transfers, defines the polling interval for the currently-selected Rx endpoint.** For Bulk endpoints, this register sets the number of frames/microframes after which the endpoint should timeout on receiving a stream of NAK responses. There is a RxInterval register for each configured Rx endpoint (except for Endpoint 0). RX POLLING INTERVAL / NAK LIMIT (M), (Host mode only) In each case the value that is set defines a number of frames/microframes (High Speed transfers), as follows: Transfer Type Speed Valid values (m) Interpretation Interrupt Low Speed or Full Speed 1 - 255 Polling interval is m frames. High Speed 1 - 16 Polling interval is 2(m-1) microframes Isochronous Full Speed or High Speed 1 - 16 Polling interval is 2(m-1) frames/microframes Bulk Full Speed or High Speed 2 - 16 NAK Limit is 2(m-1) frames/microframes. *Note: Value 0 or 1 disables the NAK timeout function. The register should be set before RxType for Bulk endpoint.*

1120011F FIFOSIZE1 EP1 Configured FIFO Size Register AA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RXFIFOSIZE				TXFIFOSIZE			
Type									DC				DC			
Reset									1	0	1	0	1	0	1	0

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Bit(s)	Name	Description
7:4	RXFIFOSIZE	**Indicates the RxFIFO size of 2^n bytes** Example: Value 10 means 2^10 = 1024 bytes.
3:0	TXFIFOSIZE	**Indicates the TxFIFO size of 2^n bytes** Example: Value 10 means 2^10 = 1024 bytes.

11200200 DMA_INTR DMA Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA_INTR_UNMASK_SET								DMA_INTR_UNMASK_CLEAR							
Type	A0								A0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_INTR_UNMASK								DMA_INTR_STATUS							
Type	RU								W1C							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	DMA_INTR_UNMASK_SET	**Sets DMA_INTR_UNMASK to 1**
23:16	DMA_INTR_UNMASK_CLEAR	**Clears DMA_INTR_UNMASK to 0**
15:8	DMA_INTR_UNMASK	**Unmasks DMA interrupts** The DMA interrupt will be generated when DMA_INTR_UNMASK and DMA_INTR_STATUS are both 1.
7:0	DMA_INTR_STATUS	**Indicates DMA complete interrupt status, one bit per DMA channel implemented** Bit 0 is used for DMA channel 1; bit 1 is used for DMA channel 2, and so on. Write 1 to clear it. *Note: DMA interrupt will be asserted after DMA enable is disabled when a null packet is received even thought DMA_COUNT_M still does not achieve 0.*

11200204 DMA_CNTL_0 DMA Channel 0 Control Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DMAABORT		DMACHEN	BURST_MODE		BUSERR	ENDPNT				INTEN	DMAMODE	DMADIR	DMAEN
Type			A0		RU	RW		RU	RW				RW	RW	RW	Other
Reset			0		0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13	DMAABORT	**If SW needs to abort the current DMA transfer, set DMAABORT=1 & DMAEN=0. After the transfer is aborted completely, DMA interrupt will occur.**
11	DMACHEN	**DMA channel enable monitor bit**
10:9	BURST_MODE	2'b00: Burst Mode 0: Bursts of unspecified length. 2'b01: Burst Mode 1: INCR4 or unspecified length. 2'b10: Burst Mode 2: INCR8, INCR4 or unspecified length. 2'b11: Burst Mode 3: INCR16, INCR8, INCR4 or unspecified length
8	BUSERR	**Bus error**
7:4	ENDPNT	**Endpoint which DMA will transfer with**

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Bit(s)	Name	Description
3	INTEN	**Enables interrupt**
2	DMAMODE	**DMA mode** DMA mode 0: Single packet operation DMA mode 1: Multi packets operation, with the configuration of DMAReqMode in RXCSR bit 11 DMA mode 1 can support both known size or unknown size transaction.
1	DMADIR	**Direction** 0: DMA write (Rx endpoint) 1: DMA read (Tx endpoint)
0	DMAEN	**Enables DMA** The bit will be cleared when the DMA transfer is completed. Programmers should not disable the DMA_en before the transfer is completed. If programmers disable the dma_en when transferring, the DMA will not stop immediately until the last bus transfer is completed.

11200208 DMA_ADDR_0 DMA Channel 0 Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA_ADDR_0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_ADDR_0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DMA_ADDR_0	**32-bit DMA start address** Updated (increased) by USB2.0 controller automatically when multiple packet DMA (DMA Mode = 1) is used.

1120020C DMA_COUNT_0 DMA Channel 0 Byte Count Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									DMA_COUNT_0[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_COUNT_0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	DMA_COUNT_0	**24-bit DMA transfer count with byte unit** Updated (decreased) by USB2.0 controller automatically while each packet is transferred.

11200210 DMA_LIMITE DMA Limiter Register 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DMA_LIMITER							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DMA_LIMITER	**Suppresses bus utilization of DMA channel** The value is from 0 to 255. 0 means no limitation, and 255 means totally banned. The value between 0 and 255 means certain DMA can have permission to use AHB every (4 x n) AHB clock cycles. *Note: It is not recommended to limit the bus utilization of the DMA channels because this increases the latency of response to the masters, and the transfer rate decreases as well. Before using it, make sure that the bus masters have a protection mechanism to avoid entering wrong states.*

11200220 DMA_CONFIG DMA Configuration Register 00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DMA_ACTIVE_EN		AHB_HPROT_2_EN			DMAQ_CHAN_SEL					AHBWAIT_SEL	BOUNDARY_1K_CROSS_EN
Type					RW		RW			RW					RW	RW
Reset					0	0	0	0		0	0	0			0	0

Bit(s)	Name	Description
11:10	DMA_ACTIVE_EN	**The two bits control usb_active.** 2'b00: usb_active depends on all DMAEN of DMA channel control registers. 2'b01: usb_active ties to 1 2'b10: usb_active ties to 0 2'b11: usb_active depends on ep_active, dma_active and all DMAEN of DMA channel control register(OR logic)
9:8	AHB_HPROT_2_EN	**The two bits control the AHB master interface HPROT2 function operateing in non-bufferable/bufferable/last transfer non-bufferable mode.** 2'b00: All the write transfers of a burst will be accessed by bufferable mode except for the last transfer of a burst. 2'b01: AHB master HPROT2 is always accessed by non-bufferable mode. 2'b10: AHB master HPROT2 is always accessed by bufferable mode. 2'b11: reserved
6:4	DMAQ_CHAN_SEL	**Selects DMA channel used by USB_DMAQ if it is available.** It will not affect if USB_DMAQ is not available.
1	AHBWAIT_SEL	**Selects AHBWAIT behavior** Set to 1 to return to old DMA master AHB wait condition. This bit is used to test DMA FIFO overflow bug.
0	BOUNDARY_1K_CRO	**Enables 1k boundary page crossing**

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Bit(s)	Name	Description
	SS_EN	Set to 1 to force burst transfer regardless 1k boundary crossing. *Note: It will violate AHB 1k boundary specification but gain some bus performance.*

11200304 EP1RXPKTCOUNT EP1 RxPktCount Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EP1RXPKTCOUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	EP1RXPKTCOUNT	**Sets up the number of packets of Rx Endpoint n size MaxP that are to be transferred in a block transfer** Only used In host mode when AutoReq is set. Has no effect in Peripheral mode or when AutoReq is not set. RqPktCount (Host mode only) For each Rx Endpoint 1 - 15, the USB2.0 controller provides a 16-bit RqPktCount register. This read/write register is used In host mode to specify the number of packets that are to be transferred in a block transfer of one or more Bulk packets of length MaxP to Rx Endpoint n. The core uses the value recorded in this register to etermine the number of requests to issue where the AutoReq option (included in the RxCSR register) has been set. *Note: Multiple packets combined into a single bulk packet within the FIFO count as one packet.*

11200480 TOFUNCADDR To Function Address Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										ToFuncAddr						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	ToFuncAddr	**TxFuncAddr are 7-bit read/write registers that record the address of the target function that is to be accessed through the associated endpoint (Endpoint 0).** TxFuncAddr needs to be defined for each Tx endpoint that is used. *Note: TxFuncAddr must be defined for Endpoint 0.*

11200482 TOHUBADDR To HUB Address Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		ToPortAddr							ToMultiTranslator	ToHUBAddr						
Type		RW							RW	RW						
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
14:8	T0PortAddr	**TxPortAddr only needs to be written where a full or low speed device is connected to Tx Endpoint n via a high speed USB 2.0 hub which carries out the necessary transaction translation.** In such circumstances, these 7-bit read/write registers need to be used to record the port of that USB 2.0 hub through which the target associated with the endpoint is accessed. *Note: If Endpoint 0 is connected to a hub, TxHubPort must be defined. Only valid if RTL defines USB_HUB. This register is only valid @ FS/LS is plugged in at hub.*
7	T0MultiTranslator	**Bit 8 should record whether the hub has multiple transaction translator.** Only valid if RTL defines USB_HUB. This register is only valid @ FS/LS is plugged in at hub. 1'b0: Single transaction translator 1'b1: Multiple transaction translators
6:0	T0HUBAddr	**TxHUBAddr are 8-bit read/write registers only needs to be written where a full or low speed device is connected to Tx Endpoint n via a high speed USB2.0 hub which carries out the necessary transaction translation to convert between high speed transmission and full/low speed transmission.** The lower 7 bit should record the address of this USB 2.0 HUB. *Note: If Endpoint 0 is connected to a hub, TxHubAddr must be defined for EP0. Only valid if RTL defines USB_HUB. This register is only valid @ FS/LS is plugged in at hub.*

11200488 T1FUNCADDR T1 Function Address Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										T1FuncAddr						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	T1FuncAddr	**TxFuncAddr are 7-bit read/write registers that record the address of the target function that is to be accessed through the associated endpoint (Endpoint 1).** TxFuncAddr needs to be defined for each Tx endpoint that is used. *Note: TxFuncAddr must be defined for Endpoint 0.*

1120048A T1HUBADDR T1 HUB Address Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		T1PortAddr							T1MultiTranslator	T1HUBAddr						
Type		RW							RW	RW						
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:8	T1PortAddr	**TxPortAddr only needs to be written where a full or low speed device is connected to Tx Endpoint n via a high speed USB 2.0 hub which carries out the necessary transaction translation.** In such circumstances, these 7-bit read/write registers need to be used to

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Bit(s)	Name	Description
		record the port of that USB 2.0 hub through which the target associated with the endpoint is accessed. *Note: If Endpoint 1 is connected to a hub, TxHubPort must be defined. Only valid if RTL defines USB_HUB. This register is only valid @ FS/LS is plugged in at hub.*
7	T1MultiTranslator	**Bit 8 should record whether the hub has multiple transaction translator.** Only valid if RTL defines USB_HUB. This register is only valid @ FS/LS is plugged in at hub. 1'b0: Single transaction translator 1'b1: Multiple transaction translators
6:0	T1HUBAddr	**TxHUBAddr are 8-bit read/write registers only needs to be written where a full or low speed device is connected to Tx Endpoint n via a high speed USB2.0 hub which carries out the necessary transaction translation to convert between high speed transmission and full/low speed transmission.** The lower 7 bit should record the address of this USB 2.0 HUB. *Note: If Endpoint 1 is connected to a hub, TxHubAddr must be defined for EP0. Only valid if RTL defines USB_HUB. This register is only valid @ FS/LS is plugged in at hub.*

1120048C R1FUNCADDR R1 Function Address Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										R1FuncAddr						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	R1FuncAddr	**RxFuncAddr are 7-bit read/write registers that record the address of the target function that is to be accessed through the associated endpoint (Endpoint 1).** RxFuncAddr needs to be defined for each Rx endpoint that is used. *Note: RxFuncAddr does not exist on EP0.*

1120048E R1HUBADDR R1 HUB Address Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		R1PortAddr							R1MultiTranslator	R1HUBAddr						
Type		RW							RW	RW						
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:8	R1PortAddr	**RxPortAddr only needs to be written where a full or low speed device is connected to Rx Endpoint n via a high speed USB 2.0 hub which carries out the necessary transaction translation.** In such circumstances, these 7-bit read/write registers need to be used to record the port of that USB 2.0 hub through which the target associated with the endpoint is accessed. *Note: The RxPortAddr doest not exist on EP0. Only valid if RTL defines USB_HUB. This register is only valid @ FS/LS is plugged in at hub.*

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Bit(s)	Name	Description
7	R1MultiTranslator	**Bit 8 should record whether the hub has multiple transaction translator.** Only valid if RTL defines USB_HUB. This register is only valid @ FS/LS is plugged in at hub. 1'b0: Single transaction translator 1'b1: Multiple transaction translators
6:0	R1HUBAddr	**RxHUBAddr are 8-bit read/write registers only needs to be written where a full or low speed device is connected to Rx Endpoint n via a high speed USB2.0 hub which carries out the necessary transaction translation to convert between high speed transmission and full/low speed transmission.** The lower 7 bit should record the address of this USB 2.0 HUB. *Note: The RxHubAddr does not exist on EP0. Only valid if RTL defines USB_HUB. This register is only valid @ FS/LS is plugged in at hub.*

11200604 TM1 Test Mode 1 Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TM1
Type																RW
Reset																0

Bit(s)	Name	Description
0	TM1	USB IP internal TM1

11200608 HWVER_DATE HW Version Control Register 20121214

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HWVER_DATE[31:16]															
Type	DC															
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HWVER_DATE[15:0]															
Type	DC															
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	1	0	0

Bit(s)	Name	Description
31:0	HWVER_DATE	**Hardware version control register date format** 32'hYYYYMMDD

11200684 SRAMA SRAM Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															EP0_StartAd_TM6_en	SRAMDBG
Type															RW	RW
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	SRAMA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	EP0_StartAd_TM6_en	**Software can enable this bit to change the EP0 FIFO start address for test mode 6 FIFO loopback test by DMA/PIO.**
16	SRAMDBG	**SRAM_DEBUG_MODE** Software can read the data in SRAM of USB core when this bit is enabled. The related registers are SRAMA, SRAMD. After setting this bit to 1, SW can set up SRAMA (SRAM address) and read the data in register SRAMD (SRAM data). Only for debugging mode and should be disabled in normal operation. 1'b0: Software sets up this bit 0 to disable SRAM_DEBUG_MODE. 1'b1: Software sets up this bit 1 to enable SRAM_DEBUG_MODE.
15:0	SRAMA	**SRAM_ADDRESS** The register is used for RISC to read data from USB SRAM. The unit is 4-byte. For example, to check 0x400 byte address, set this register to 0x100. This register is only available when the register bit SRAM_DEBUG_MODE of the register SRAMDBG is set to 1. When SRAM ADDRESS is set, SRAM DATA will display the data in the address SRAM ADDRESS in SRAM. Only for debugging mode.

11200688 <u>SRAMD</u> SRAM Data Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRAMDATA[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRAMDATA[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRAMDATA	**SRAM_DATA** The register is used for RISC to read data from USB SRAM. This register is only available when the register bit SRAM_DEBUG_MODE of the register SRAMDBG is set to 1. When SRAM ADDRESS is set, SRAM DATA will display the data in the address SRAM ADDRESS in SRAM. Only for debugging mode.

11200690 <u>RISC_SIZE</u> RISC Size Register 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RISC_SIZE	
Type															RW	
Reset															1	0

Bit(s)	Name	Description
1:0	RISC_SIZE	**Configures RISC wrapper access size** 2'b00: 8-bit byte access

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Bit(s)	Name	Description
		2'b01: 16-bit half word access 2'b10: 32-bit word access 2'b11: Reserved

11200700 RESREG Reserved Register FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESERVEDH												MAC_CG_DIS	USB_CG_DIS	DMA_CG_DIS	MCU_CG_DIS
Type	RW												RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESERVEDL															HSTPWRDWN_OPT
Type	RW															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	MAC_CG_DIS	**Disables USB MAC clock gate to enhance dynamic power**
18	USB_CG_DIS	**Disables USB clock gate**
17	DMA_CG_DIS	**Disables DMA clock gate**
16	MCU_CG_DIS	**Disables MCU clock gate**
0	HSTPWRDWN_OPT	**Host mode device connection detection option** 0: Disable 1: Enable the detection of device connect when MAC clock is off and drive power-down wakeup signal to wake up system

11200730 OTG20_CSRL OTG20 Related Control Register L 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DIS_HSUS	EN_A_HFS_WHNP	DIS_B_WTDIS	EN_HHS_SUSP_DIS	DIS_CHARGE_VBUS	EN_HSUS_RESUME_INT	EN_HSUS_RESUME	OTG20_EN
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	DIS_HSUS	**Disables host mode entering C_OPM_HSUS state before entering suspend** Suggested: 1'b1: 0: Host mode enters C_OPM_HSUS state before entering suspend. 1: Disable host mode entering C_OPM_HSUS state before entering suspend.
6	EN_A_HFS_WHNP	**If this bit is enabled, FS idle of A device will transfer to HFS_HSUS state first.** Suggested: 1'b1 in all modes (device/host/otg) 0: FS idle of A device will not transfer to HFS_HSUS state first. 1: FS idle of A device will transfer to HFS_HSUS state first.
5	DIS_B_WTDIS	**Disables B device entering C_OPM_B_WTDIS states before switching to host mode**

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Bit(s)	Name	Description
		Suggested: 1'b1 0: B device enters C_OPM_B_WTDIS states before switching to host mode. 1: B device does not enter C_OPM_B_WTDIS states before switching to host mode.
4	EN_HHS_SUSP_DIS	**Enables host-hs-suspend entering OPM_FS_WTCON state first while receiving disconnect signal** Suggested: 1'b1 in all modes (device/host/otg). 0: The host mode enters fs_normal mode directly while the device receives the disconnect signal as suspend state in all states. 1: The host mode enters OPM_FS_WTCON mode first while the device receives the disconnect signal as suspend state in all states.
3	DIS_CHARGE_VBUS	**Disables B device charging VBUS function for OTG2.0 feature** 0: B device charges VBUS while B device initiates the SRP protocol. This mode is to make compatible the OTG1.3 related SRP flow. 1: B device does not charge VBUS while B device initiates the SRP protocol. This mode is to satisfy the OTG2.0 protocol.
2	EN_HSUS_RESUME_INT	**Enables hsus mode of host initializing resuming interrupt while receiving resume K as waiting for HNP** Suggested: 1'b1 for OTG2.0 mode 0: Suspend mode of host does not initialize resuming interrupt as receiving resume K while host is waiting for HNP protocol in OTG20 mode. 1: Suspend mode of host initializes resuming interrupt as receiving resume K while host is waiting for HNP protocol in OTG20 mode.
1	EN_HSUS_RESUME	**Enables hnpsus-mode of host entering host-normal mode as receiving resume K while waiting for HNP** Suggested: 1'b0 while USB works in OTG20 mode 0: hnpsus-mode of host stays in hnpsus-mode as receiving resume K while waiting for HNP. 1: hnpsus-mode of host enters host-normal mode as receiving resume K while waiting for HNP.
0	OTG20_EN	**Enables OTG 2.0 feature** 0: Disable OTG2.0 feature; default OTG1.3 mode. 1: Enable USB OTG20 feature

11200731 OTG20_CSRH OTG20 Related Control Register H 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															DIS_AUTORST	EN_CON_DEB_SHORT
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	DIS_AUTORST	**Informs whether HW sends bus reset automatically while B-device changes to host with HNP** 0: HW sends bus reset automatically while B-device changes to host with HNP. 1: HW does not send bus reset when B-device changes to host mode. SW must set the reset bit for sending bus reset. The bit is added for OTG20 compliance test.
0	EN_CON_DEB_SHORT	**Enable this bit to decrease A device connection denounce waiting timing** Suggested: 1'b1

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Bit(s)	Name	Description
		0: A device connection without denounce waiting timing. 1: Decrease A device connection denounce waiting timing.

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5.6 USBPHY Register File

The full features include USB2.0 PHYD and PHYA macro control registers. It also includes a frequency meter for USB2.0 PHYA monitor clock. The registers can be accessed by I2C interface (FT). The default mode is accessing registers by AHB. After 0xfe (I2C access only) is configured to 8'h01, the register file will be in the I2C mode (accessing registers by I2C).

5.6.1 Feature List

- USB2.0
  - USB2.0 PHYD control registers for PHYD macro setting
  - USB2.0 PHYA control registers for PHYA characteristic tuning
  - Force USB2.0 UTMI interface for FT tests
  - Force USB2.0 PHY analog power-down in ATPG mode
  - Frequency meter for USB2.0 PHYA monitor clock
- Accessing PHY registers by AHB slave interface
- Accessing PHY registers by I2C interface

5.6.2 USBPHY Register File Block Diagram

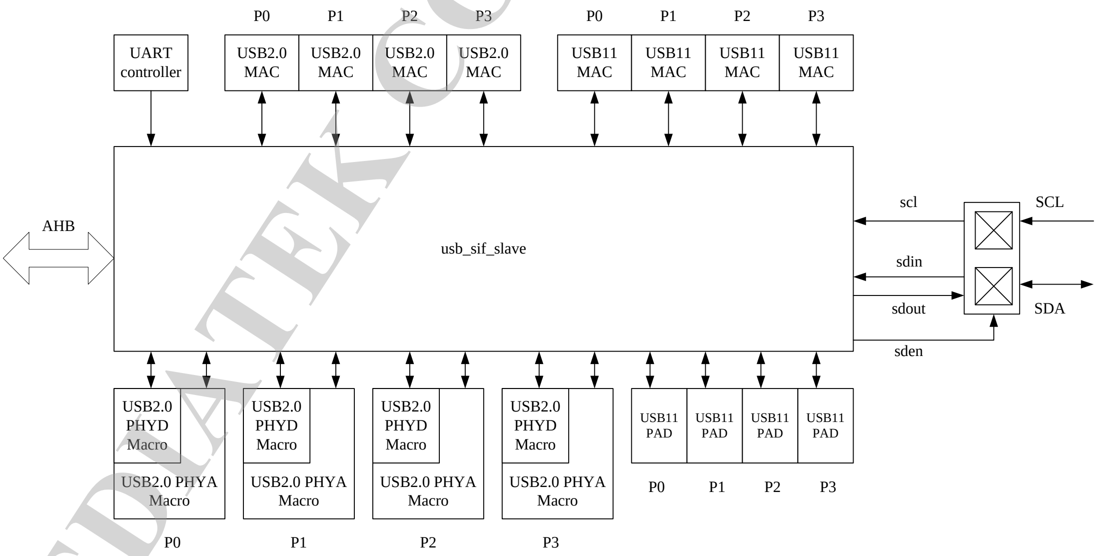

Figure 5-11. USBPHY RegFile block diagram

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5.6.3 Register Definition

- Page base
  - Every page register contains 0x00h ~ 0xefh (USB2.0+ USB1.1)
  - Frequency meter registers in one page (@ 0xff = 8'h0f)
  - 0xf0~0xff: Global register
  - 0xfe[0]: I2C mode, the default value is 0 (accessing register by AHB interface)
    - If switched to I2C mode, configuring 0xfe[0] to be 1'h1 is required.
    - I2C access only
  - 0xffh (RG_PAGE): I2C page register
    - I2C access only
- I2C
  - Accessing different pages by setting up RG_PAGE
  - Default device number: 7'h60 (*If there are more than one hier, the device number of the second hier. will be 7'h61.)
  - Accessing different pages by setting up RG_PAGE (0xff)
  - Port 0 USB PHY register page : RG_PAGE value : 8'h00
  - Port 1 USB PHY register page : RG_PAGE value : 8'h01
  - Port 2 USB PHY register page : RG_PAGE value : 8'h02
  - Port 3 USB PHY register page : RG_PAGE value : 8'h03
  - Frequency Meter register page : RG_PAGE value : 8'h0f
- AHB
  - Accessing different pages by different base addresses
  - Supporting max. four ports. Base address: 800h,900h,a00h,b00h
    - Port 0 register base address: 800h
    - Port 1 register base address: 900h
    - Port 2 register base address: a00h
    - Port 3 register base address: b00h
    - Frequency meter registers base address: f00h

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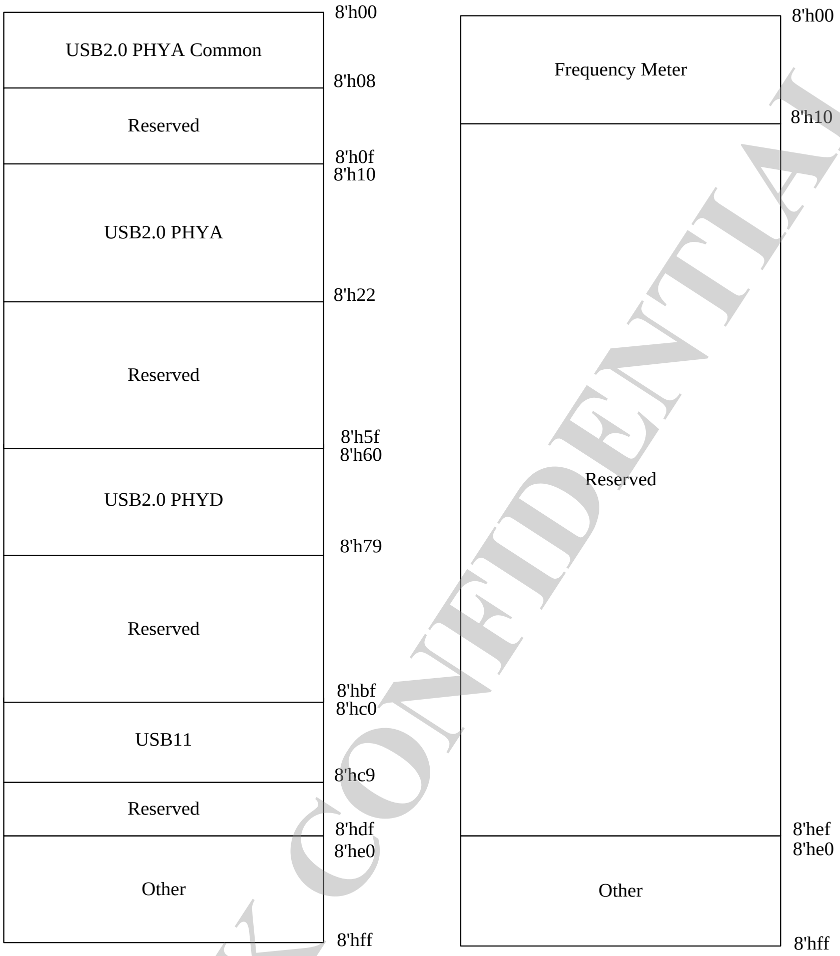

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5.6.4 Function Address Register

Module name: USBPHY Base address: (+11210000h)

Address	Name	Width	Register Function
11210000	USBPHYACR0	32	USB20 PHYA Common 0 Register
11210004	USBPHYACR1	32	
11210008	USBPHYACR2	32	
11210010	USBPHYACR4	32	
11210014	USBPHYACR5	32	
11210018	USBPHYACR6	32	
1121001C	U2PHYACR3	32	USB20 PHYA Control 3 Register
11210020	U2PHYACR4	32	USB20 PHYA Control 4 Register
11210024	U2PHYAMON0	32	USB20 PHYA Monitor 0 Register
11210060	U2PHYDCR0	32	USB20 PHYD Control 0 Register
11210064	U2PHYDCR1	32	USB20 PHYD Control 1 Register
11210068	U2PHYDTM0	32	USB20 PHYD Control UTMI 0 Register
1121006C	U2PHYDTM1	32	USB20 PHYD Control UTMI 1 Register
11210070	U2PHYDMON0	32	USB20 PHYD Monitor 0 Register
11210074	U2PHYDMON1	32	USB20 PHYD Monitor 1 Register

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Address	Name	Width	Register Function
11210078	U2PHYDMON2	32	USB20 PHYD Monitor 2 Register
1121007C	U2PHYDMON3	32	USB20 PHYD Monitor 3 Register
112100FC	REGFCOM	32	USB Common Register
11210F00	FMCR0	32	Frequency Meter Control 0 Registers
11210F04	FMCR1	32	Frequency Meter Control 1 Registers
11210F08	FMCR2	32	Frequency Meter Control 2 Registers
11210F0C	FMMONR0	32	Frequency Meter Monitor 0 Registers
11210F10	FMMONR1	32	Frequency Meter Monitor 1 Registers

11210000 USBPHYACR0 USB20 PHYA Common 0 Register 0000144E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		MPX_OUT_SEL				TX_PH_ROT_SEL				PLL_DIVEN				PLL_BR	PLL_BP	PLL_BLP
Type		RW				RW				RW				RW	RW	RW
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	USBPLL_FORCE_ON	PLL_FBDIV							PLL_PREDIV		INTR_EN	REF_EN	BGR_DIV		CHP_EN	BGR_EN
Type	RW	RW							RW		RW	RW	RW		RW	RW
Reset	0	0	0	1	0	1	0	0	0	1	0	0	1	1	1	0

Bit(s)	Mnemonic	Name	Description
30:28	MPX_OUT_SEL	RG_USB20_MPX_OUT_SEL	000: MPX output off 001: MPX output to PAD_USB_VRT (engineer verification mode) 010: MPX output to NS_USB_V (ABIST mode) 100: MPX output to PAD_USB_DP
26:24	TX_PH_ROT_SEL	RG_USB20_TX_PH_ROT_SEL	**TX clock rotation function** Clock phase of all ports will be changed at the same time. 000: Phase 0 001: Phase 1 010: Phase 2 011: Phase 3 100: Phase 4 101: Phase 5
22:20	PLL_DIVEN	RG_USB20_PLL_DIVEN	**Time domain cap multiplication ratio** 3'd0: x1 3'd1: x2 3'd6: x64
18	PLL_BR	RG_USB20_PLL_BR	**Resistance adjustment for bandwidth** 1'b0: BW = Fref/10 1'b1: BW = Fref/20
17	PLL_BP	RG_USB20_PLL_BP	**Capacitance adjustment for bandwidth** 1'b0: When RG_PLL_BR=1'b0 1'b1: When RG_PLL_BR=1'b1
16	PLL_BLP	RG_USB20_PLL_BLP	**Selects LPF bandwidth** 1'b0: 40MHz 1'b1: 20MHz
15	USBPLL_FORCE_ON	RG_USB20_USBPLL_FORCE_ON	**Power-down** 1'b0: Don't care 1'b1: Force PLL on

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Bit(s)	Mnemonic	Name	Description
14:8	**PLL_FBDIV**	RG_USB20_PLL_FBDIV	**Feedback divide ratio** 7'd0: /1 7'd1: /2 7'd127: /128
7:6	**PLL_PREDIV**	RG_USB20_PLL_PREDIV	**Pre-divider ratio** 2'b00: Fref = Fin/1 2'b01: Fref = Fin/2 2'b1X: Fref = Fin/4
5	**INTR_EN**	RG_USB20_INTR_EN	**Enables VRT internal R architecture** 0: Disable 1: Enable
4	**REF_EN**	RG_USB20_REF_EN	**Enables VRT current generator** 0: Disable 1: Enable
3:2	**BGR_DIV**	RG_USB20_BGR_DIV	**Chopper frequency divider (~3MHz)** 00: REFCLK/2 01: REFCLK/4 10: REFCLK/8 11: REFCLK/16
1	**CHP_EN**	RG_USB20_CHP_EN	**Enable signal of chopper** 0: Disable 1: Enable
0	**BGR_EN**	RG_USB20_BGR_EN	**Enable signal of BGR** 0: Disable 1: Enable

11210004 **USBPHYACR1** **45045500**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CLKREF_REV[7:0]**													**OTG_VBUSTH**		
Type	RW													RW		
Reset	0	1	0	0	0	1	0	1						1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**VRT_VREF_SEL**				**TERM_VREF_SEL**			**MPX_SEL**							
Type		RW				RW			RW							
Reset		1	0	1		1	0	1	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**CLKREF_REV[7:0]**	RG_USB20_CLKREF_REV	**RG_USB20_CLKREF_REV[2:0]** **RG_USB20_TERM_VREF_SEL_P1[2:0]** RG_USB20_CLKREF_REV[6:4] RG_USB20_TERM_VREF_SEL_P2[2:0]
18:16	**OTG_VBUSTH**	RG_USB20_OTG_VBUSTH	**Controls VBUS threshold level (shared circuit)** 000: 1.365V 001: 1.385V 010: 1.405V 011: 1.425V 100: 1.445V 101: 1.465V 110:1.485V 111: 1.505V
14:12	**VRT_VREF_SEL**	RG_USB20_VRT_VREF_SEL	**Selects VRT reference voltage (shared circuit)** 000: 700mV 001: 720mV

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Bit(s)	Mnemonic	Name	Description
			010: 740mV 011: 760mV 100: 770mV 101: 780mV 110: 800mV 111: 820mV
10:8	**TERM_VREF_SEL**	RG_USB20_TERM_VREF_SEL	**Selects HS_TX TERM reference voltage (shared circuit)** 000: 320mV 001: 340mV 010: 360mV 011: 380mV 100: 400mV 101: 420mV 110: 440mV 111:460mV
7:0	**MPX_SEL**	RG_USB20_MPX_SEL	**Selects MPX output signal** MPX_SEL[7]=1: Bypass OP to AIO, 0 off and Hi-Z MPX_SEL[6]=1: Output AIO by OP, 0 off and Hi-Z MPX_SEL[5:4]=00: Output Common part MPX_SEL[5:4]=01: Output Port0 part MPX_SEL[5:4]=10: Output Port1 part MPX_SEL[5:4]=11: Output Port2 part MPX_SEL[3]=0: Output AIO MPX_SEL[3]=1: Output DIO MPX_SEL[2:0]: (Common part) 000: OFF and Hi-Z 001: 010: 011:

11210008 USBPHYACR2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**CLKREF_REV[15:8]**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**CLKREF_REV[15:8]**	RG_USB20_CLKREF_REV	RG_USB20_CLKREF_REV[2:0] RG_USB20_TERM_VREF_SEL_P1[2:0] RG_USB20_CLKREF_REV[6:4] RG_USB20_TERM_VREF_SEL_P2[2:0]

11210010 USBPHYACR4 00004414

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DP_ABIST_SOURCE_EN**				**DP_ABIST_SELE**											**ICUSB_EN**
Type	RW				RW											RW

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Reset	0				0	0	0	0								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**LS_CR**				**FS_CR**				**LS_SR**				**FS_SR**		
Type		RW				RW				RW				RW		
Reset		1	0	0		1	0	0		0	0	1		1	0	0

Bit(s)	Mnemonic	Name	Description
31	**DP_ABIST_SOURCE_EN**	RG_USB20_DP_ABIST_SOURCE_EN	**DP ABIST source enable signal** 0: Disable ABIST source 1: Enable ABIST source
27:24	**DP_ABIST_SELE**	RG_USB20_DP_ABIST_SELE	**DP ABIST source selection signal** Porto DP ABIST source selection signal 0000: DP=0V 0001: DP=80mV 0010: DP=100mV 0011: DP=200mV 0100: DP=220mV 0101: DP=500mV 0110: DP=520mV 0111: DP=660mV 1000: DP=680mV 1001: DP=700mV 1010: DP=800mV 1011: DP=900mV 1100: DP=1900mV 1101: DP=2000mV 1110: DP=2100mV 1111: DP=VDD33
16	**ICUSB_EN**	RG_USB20_ICUSB_EN	**IC_USB mode enable signal** 0: Disable 1: Enable
14:12	**LS_CR**	RG_USB20_LS_CR	**Porto USB11 low speed mode TX slew rate control signal**
10:8	**FS_CR**	RG_USB20_FS_CR	**Porto USB11 full speed mode TX slew rate control signal**
6:4	**LS_SR**	RG_USB20_LS_SR	000: Slowest slew rate 111: Fastest slew rate
2:0	**FS_SR**	RG_USB20_FS_SR	000: Slowest slew rate 111: Fastest slew rate

11210014 **USBPHYACR5** **00801000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**DISC_FIT_EN**	**INIT_SQ_EN_DG**		**HSTX_TMODE_SEL**		**SQD**		**DISCD**		**HSTX_TMODE_EN**	**PHY D_MONE N**	**INLPBK_EN**	**CHIRP_EN**
Type				RW	RW		RW		RW		RW		RW	RW	RW	RW
Reset				0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**HSTX_SRCAL_EN**	**HSTX_SRCTRL**			**HS_100U_U3_EN**	**GBIAS_EN B**			**DM_ABIST_SOURCE_EN**				**DM_ABIST_SELE**			
Type	RW	RW			RW	RW			RW				RW			
Reset	0	0	0	1	0	0			0				0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
28	**DISC_FIT_EN**	RG_USB20_DISC_FIT_EN	**DISC deglitch enable signal** 0: Disable 1: Enable
27:26	**INIT_SQ_EN_DG**	RG_USB20_INIT_SQ_EN_DG	00: INIT_SQ_OUT_EN delay 0T 01: INIT_SQ_OUT_EN delay 2T 10: INIT_SQ_OUT_EN delay 4T 11: INIT_SQ_OUT_EN delay 5T
25:24	**HSTX_TMODE_SEL**	RG_USB20_HSTX_TMODE_SEL	**Selects HS TX test mode signal** 00: 240MHz clock 01: 60MHz clock 10: Hi 11: Lo
23:22	**SQD**	RG_USB20_SQD	**SQ deglitch** 00: Deglitch 1x 01: Deglitch 2x 10: Deglitch 3x 11: Deglitch 6x
21:20	**DISCD**	RG_USB20_DISCD	**DISC deglitch** 00: Deglitch 10n 01: Deglitch 6n 10: Deglitch 4n 11: Deglitch 2n
19	**HSTX_TMODE_EN**	RG_USB20_HSTX_TMODE_EN	**HS TX test mode enable signal** 0: Disable 1: Enable and output test pattern by TMODE_SEL
18	**PHYD_MONEN**	RG_USB20_PHYD_MONEN	**Digital PHY monitor clock enable signal** 0: Disable 1: Enable
17	**INLPBK_EN**	RG_USB20_INLPBK_EN	**High speed internal loopback enable signal** 0: Disable 1: Enable
16	**CHIRP_EN**	RG_USB20_CHIRP_EN	**Sets up chirp level to 0.8V when in chirp mode** 0: Disable 1: Enable
15	**HSTX_SRCAL_EN**	RG_USB20_HSTX_SRCAL_EN	**HS TX SR calibration enable signal** 0: Disable 1: Enable
14:12	**HSTX_SRCTRL**	RG_USB20_HSTX_SRCTRL	**Controls high speed slew rate** 000: Fastest slew rate 111: Slowest slew rate
11	**HS_100U_U3_EN**	RG_USB20_HS_100U_U3_EN	**Selects VRT 100uA source** 0: 100uA from USB2.0 1: 100uA from USB3.0
10	**GBIAS_ENB**	RG_USB20_GBIAS_ENB	**Enables overdrive 3.3V bias** 0: Enable bias 1: Disable bias (select ICUSB mode)
7	**DM_ABIST_SOURCE_EN**	RG_USB20_DM_ABIST_SOURCE_EN	**DM ABIST source enable signal** 0: Disable ABIST source 1: Enable ABIST source
3:0	**DM_ABIST_SELE**	RG_USB20_DM_ABIST_SELE	**DM ABIST source selection signal** Porto DM ABIST source selection signal 0000: DM=0V 0001: DM=80mV 0010: DM=100mV

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Bit(s)	Mnemonic	Name	Description
			0011: DM=200mV 0100: DM=220mV 0101: DM=500mV 0110: DM=520mV 0111: DM=660mV 1000: DM=680mV 1001: DM=700mV 1010: DM=800mV 1011: DM=900mV 1100: DM=1900mV 1101: DM=2000mV 1110: DM=2100mV 1111: DM=VDD33

11210018 USBPHYACR6 00900488

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PHY_REV[7:0]								BC11_SW_EN	SR_CLK_SEL		OTG_VBUSCMP_EN	OTG_ABIST_EN	OTG_ABIST_SELE		
Type	RW								RW	RW		RW	RW	RW		
Reset	0	0	0	0	0	0	0	0	1	0		1	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			HSRX_MMODE_SELE			HSRX_BIAS_EN_SEL		HSRX_TMODE_EN	DISCTH				SQTH			
Type			RW			RW		RW	RW				RW			
Reset			0	0		1	0	0	1	0	0	0	1	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**PHY_REV[7:0]**	RG_USB20_PHY_REV	**INT PHY reserved**
23	**BC11_SW_EN**	RG_USB20_BC11_SW_EN	**Controls BC1.1 switch** 0: Disable 1: Enable
22	**SR_CLK_SEL**	RG_USB20_SR_CLK_SEL	**Selects SR clock** 0: Slew rate calibration clock 1: 240MHz for ABIST clock
20	**OTG_VBUSCMP_EN**	RG_USB20_OTG_VBUSCMP_EN	**Enables OTG** 0: Disable 1: Enable
19	**OTG_ABIST_EN**	RG_USB20_OTG_ABIST_EN	**OTG ABIST mode enable signal** 0: Disable 1: Enable
18:16	**OTG_ABIST_SELE**	RG_USB20_OTG_ABIST_SELE	**Selects OTG ABIST voltage** 000: 100mV 001: 200mV 010: 350mV 011: 450mV 100: 700mV 101: 800mV 110: 1400mV 111: 1600mV
13:12	**HSRX_MMODE_SELE**	RG_USB20_HSRX_MMODE_SELE	**Selects HS_RX manual mode** 00: HS_RX in normal mode. Switch SQ/DISC function by IDLEB

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Bit(s)	Mnemonic	Name	Description
			01: Manual mode. Switch SQ (IDLEB=0)/DISC (IDLEB=1) function 10: Force HS_RX in SQ mode 11: Force HS_RX in DISC mode
10:9	**HSRX_BIAS_EN_SEL**	RG_USB20_HSRX_BIAS_EN_SEL	**Selects HS RX Bias enable signal** 00: ENPLL (always on) 01: IDLEB | RCV_EN (when TX on, RX off, device mode only) 10: !ENPLL | FS_BIAS_EN (Keep high in HS mode) 11: RG_USB20_HSRX_TMODE_EN
8	**HSRX_TMODE_EN**	RG_USB20_HSRX_TMODE_EN	**When RG_USB20_HSRX_BIAS_EN_SEL[1:0]=11, HS RX Bias will be controlled by this signal.** 0: Disable 1: Enable
7:4	**DISCTH**	RG_USB20_DISCTH	**Disconnection threshold** Shared for host disconnection and trimming control. 0000: 400mV 0001: 420mV 0010: 440mV 0011: 460mV 0100: 480mV 0101: 500mV 0110: 520mV 0111: 540mV 1000: 560mV 1001: 580mV 1010: 600mV 1011: 620mV 1100: 640mV 1101: 660mV 1110: 680mV 1111: 700mV
3:0	**SQTH**	RG_USB20_SQTH	**SQ threshold** 0000: 85mV 0001: 90mV 0010: 95mV 0011: 100mV 0100: 105mV 0101: 110mV 0110: 115mV 0111: 120mV 1000: 125mV 1001: 130mV 1010: 135mV 1011: 140mV 1100:145mV 1101: 150mV 1110: 155mV 1111: 160mV

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1121001C **U2PHYACR3** **USB20 PHYA Control 3 Register** **C0040000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**HSTX_DBIST**					**HSTX_BIST_EN**	**HSTX_I_EN_MODE**						**USB1_TMODE_EN**	**TMODE_FS_LS_TX_EN**	**TMODE_FS_LS_RCV_EN**	**TMODE_FS_LS_MODE**
Type	RW					RW	RW						RW	RW	RW	RW
Reset	1	1	0	0		0	0	0					0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name		**HS_TERM_EN_MODE**		**PUPD_BIST_EN**	**EN_PU_DM**	**EN_PD_DM**	**EN_PU_DP**	**EN_PD_DP**								
Type		RW		RW	RW	RW	RW	RW								
Reset		0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
31:28	**HSTX_DBIST**	RG_USB20_HSTX_DBIST	**HS_TX BIST output data**
26	**HSTX_BIST_EN**	RG_USB20_HSTX_BIST_EN	**High speed TX BIST enable signal** 0: Disable TX BIST 1: Enable TX BIST
25:24	**HSTX_I_EN_MODE**	RG_USB20_HSTX_I_EN_MODE	**HS_TX output current enable mode** 00: Enable TX current when EN_HS_TX_I=1 (toggle mode) 01: Enable TX current when EN_HS_TX_I=1 or EN_HS_TERM=1 10: Force to disable TX current 11: Force to enable TX current
19	**USB11_TMODE_EN**	RG_USB20_USB11_TMODE_EN	**USB11 test mode enable signal** 0: Disable test mode 1: Enable test mode
18	**TMODE_FS_LS_TX_EN**	RG_USB20_TMODE_FS_LS_TX_EN	**USB11 test mode EN_FS_LS_TX0 signal** 0: Disable USB11 TX in test mode 1: Enable USB11 TX in test mode
17	**TMODE_FS_LS_RCV_EN**	RG_USB20_TMODE_FS_LS_RCV_EN	**USB11 test mode EN_FS_LS_TX0 signal** 0: Disable USB11 receiver in test mode 1: Enable USB11 receiver in test mode
16	**TMODE_FS_LS_MODE**	RG_USB20_TMODE_FS_LS_MODE	**USB11 test mode FS_LS_MODE signal** 0: Enable USB11 into low speed mode in test mode 1: Enable USB11 into full speed mode in test mode
14:13	**HS_TERM_EN_MODE**	RG_USB20_HS_TERM_EN_MODE	**HS R45 enable mode** 00: Enable R45 when EN_HS_TERM=1 01: Enable R45 when EN_HS_TERM=1 10: Force to disable R45 11: Force to enable R45
12	**PUPD_BIST_EN**	RG_USB20_PUPD_BIST_EN	0: Disable 1: Enable PU/PD resistor ABIST
11	**EN_PU_DM**	RG_USB20_EN_PU_DM	0: Disable 1: Enable
10	**EN_PD_DM**	RG_USB20_EN_PD_DM	0: Disable 1: Enable
9	**EN_PU_DP**	RG_USB20_EN_PU_DP	0: Disable 1: Enable
8	**EN_PD_DP**	RG_USB20_EN_PD_DP	0: Disable 1: Enable

11210020 **U2PHYACR4** **USB20 PHYA Control 4 Register** **0000001A**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														**rg_usb20_dp_1ook_mode**	**DM_1ooK_EN**	**DP_1ooK_EN**
Type														RW	RW	RW
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	usb20_gpio_dm_i	usb20_gpio_dp_i	usb20_gpio_dm_oe	usb20_gpio_dp_oe			rg_usb20_gpio_ctl	usb20_gpio_mode			TX_BIAS_EN	TX_VCMPDN_EN	HS_SQ_EN_MODE		HS_RCV_EN_MODE	
Type	RW	RW	RW	RW			RW	RW			RW	RW	RW		RW	
Reset	0	0	0	0			0	0			0	1	1	0	1	0

Bit(s)	Mnemonic	Name	Description
18		rg_usb20_dp_100k_mode	0: RG_USB20_DP_100K_EN controlled by usb20_dp_100k_en register 1: RG_USB20_DP_100K_EN controlled by rg_uart_mode
17	**DM_100K_EN**	RG_USB20_DM_100K_EN	0: Disable DM 100k 1: Enable DM 100k
16	**DP_100K_EN**	usb20_dp_100k_en	**RG_USB20_DP_100K_EN = usb20_dp_100k_en when rg_usb20_dp_100k_mode =1** 0: Disable DP 100k 1: Enable DP 100k
15	**usb20_gpio_dm_i**	usb20_gpio_dm_i	**USB20 GPIO DP input**
14	**usb20_gpio_dp_i**	usb20_gpio_dp_i	**USB20 GPIO DP input**
13	**usb20_gpio_dm_oe**	usb20_gpio_dm_oe	**Enables USB20 GPIO DM output**
12	**usb20_gpio_dp_oe**	usb20_gpio_dp_oe	**Enables USB20 GPIO DP output**
9	**rg_usb20_gpio_ctl**	rg_usb20_gpio_ctl	**Controls USB20 GPIO** 0: By USB PHY register 1: System register
8	**usb20_gpio_mode**	usb20_gpio_mode	**USB20 GPIO mode enable control** 0: Disable 1: Enable
5	**TX_BIAS_EN**	RG_USB20_TX_BIAS_EN	0: Disable 1: Enable
4	**TX_VCMPDN_EN**	RG_USB20_TX_VCMPDN_EN	0: Disable 1: Enable
3:2	**HS_SQ_EN_MODE**	RG_USB20_HS_SQ_EN_MODE	00: Force DISC EN 01: Force SQ EN 10: Control by EN_HS_RCV (UTMI) 11: Control by EN_PLL
1:0	**HS_RCV_EN_MODE**	RG_USB20_HS_RCV_EN_MODE	00: Force RCV off 01: Force RCV EN 10: Control by EN_HS_RCV (UTMI) 11: Control by EN_PLL

11210024 **U2PHYAMON0** **USB20 PHYA Monitor 0 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RGO_GPIO_DM_O	RGO_GPIO_DP_O

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Type															RO	RO
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	**RGO_GPIO_DM_O**	RGO_USB20_GPIO_DM_O	USB20 GPIO DM data output to Reg
0	**RGO_GPIO_DP_O**	RGO_USB20_GPIO_DP_O	USB20 GPIO DP data output to Reg

11210060 U2PHYDCR0 USB20 PHYD Control 0 Register 00000402

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CDR_TST**		**GATED_ENB**		**TESTMODE**		**PLL_STABLE**	**PLL_FORCE_ON**	**PHYD_RESERVE[15:8]**							
Type	RW		RW		RW		RW	RW	RW							
Reset	0	0	0		0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**PHYD_RESERVE[7:0]**								**EBTHRLD**	**EARLY_HSTX_I**	**TX_TST**	**NEGEDGE_ENB**	**CDR_FILT**			
Type	RW								RW	RW	RW	RW	RW			
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0

Bit(s)	Mnemonic	Name	Description
31:30	**CDR_TST**	RG_USB20_CDR_TST	**CDR module function option, debug usage**
29	**GATED_ENB**	RG_USB20_GATED_ENB	**Enables high level clock gating** For debugging. 0: Enable 1: Disable
27:26	**TESTMODE**	RG_USB20_TESTMODE	**Selects USB test mode** 00: Normal 01: Enable loopback (set to high to initialize loopback; set to low to check LB_DONE/LB_PASS) 10: Reserved 11: Reserved
25	**PLL_STABLE**	RG_USB20_PLL_STABLE	**PHY clock enable signal** 0: PHY_CLK gated 1: PHY_CLK sent out
24	**PLL_FORCE_ON**	RG_USB20_PLL_FORCE_ON	**PLL on even when both ports are suspended** For outputting DIV_CK. 0: Normal (PLL on when not in suspend mode) 1: Force on (PLL always on)
23:8	**PHYD_RESERVE**	RG_USB20_PHYD_RESERVE	**Reserved** RG_PHYD_RESERVE[1: 0]: rg_tapctl[1:0]: tapsel optional +1/-1, 2'b00/2'b11: No change 2'b01: tap_sel -1 2'b10: tap_sel +1 RG_PHYD_RESERVE[2]: Eco option for fixing DA_USB20_HS_TERM_EN = 0 when in non-driving mode 0: Disable 1: Enable RG_PHYD_RESERVE[15: 3]: Reserved
7	**EBTHRLD**	RG_USB20_EBTHRLD	**USB20 elastic buffer tholdshold option** 0: wr_ptr = 4

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Bit(s)	Mnemonic	Name	Description
			1: wr_ptr = 3
6	**EARLY_HSTX_I**	RG_USB20_EARLY_HSTX_I	**HSTX current source turned-on timing** 0: Normal 1: Earlier
5	**TX_TST**	RG_USB20_TX_TST	**TX macro test option** For debugging
4	**NEGEDGE_ENB**	RG_USB20_NEGEDGE_ENB	**UTMI output signal aligned to negative edge for hold time issue** 0: Negedge phy_clk registered UTMI output 1: Posedge phy_clk registered UTMI output
3:0	**CDR_FILT**	RG_USB20_CDR_FILT	**Selects CDR low pass filter** For debugging.

11210064 U2PHYDCR1 USB20 PHYD Control 1 Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**PROBE_SEL**								**DRVVBUS**	**rg_debug_en**		**OTG_PROBE**	**SW_PLLMODE**		**BERTH**	
Type	RW								RW	RW		RW	RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**LBMODE**		**FORCE_TAP**	**TAPSEL**											
Type		RW		RW	RW											
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:24	**PROBE_SEL**	RG_USB20_PROBE_SEL	[4:0]: Select debugging signal [7:5]: Reserved
23	**DRVVBUS**	RG_USB20_DRVVBUS	**Controls DRVVBUS signal when force_drvvbus = 1 or utmi_muxsel = 1**
22	**rg_debug_en**	rg_debug_en	**Enables USB utmi rx_active and tx_valid debugging** 0: disable 1: enable
20	**OTG_PROBE**	RG_USB20_OTG_PROBE	**Selects OTG signals to USBSIF_PROBE_OUT[4:0]**
19:18	**SW_PLLMODE**	RG_USB20_SW_PLLMODE	**[0]: SW PLL stable mode** 0: HW PLL stable mode, 100usec PLL stable time controller by HW 1: SW PLL stable mode, 100usec PLL stable time controller by RG_PLL_STABL **[1]: PLL stable time option** 0: Stable time = 8192*free CLK period (>100usec for 60M
17:16	**BERTH**	RG_USB20_BERTH	**Loopback bit errors (BER) threshold** When BER > BERTH, loopback will fail. 00: 0 01: 16 10: 64 11: 128
14:13	**LBMODE**	RG_USB20_LBMODE	**Loop back mode** RG_LBMODE[0]: 0: When compared data are mismatched, lb_cmpok is always low. 1: When compared data are mismatched, lb_cmpok goes low until

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Bit(s)	Mnemonic	Name	Description
			compared data are matched then goes high. RG_LBMODE[1]: 0: Expected data are continuous. 1: Expected data will re-sync.
12	**FORCE_TAP**	RG_USB20_FORCE_TAP	**Forces CDR tap_sel** 0: Disable 1: Enable
11:0	**TAPSEL**	RG_USB20_TAPSEL	**When RG_FORCE_TAP=1, tap_sel = RG_TAPSEL.**

11210068 U2PHYDTM0 USB20 PHYD Control UTMI 0 Register 02040000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**rg_uart_mode**		**force_uart_i**	**force_uart_bias_en**	**force_uart_tx_oe**	**force_uart_en**	**force_usb_clken**	**force_drvvbus**	**force_datain**	**force_txvalid**	**force_dm_pulldown**	**force_dp_pulldown**	**force_xcvrsel**	**force_suspendm**	**force_termsel**	**force_opmode**
Type	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**utmi_muxsel**	**RG_RESET**	**RG_DATAIN**				**RG_TXVALIDH**	**RG_TXVALID**	**RG_DMPULLDOEN**	**RG_DPPULLDOWN**	**RG_XCVRSEL**		**RG_SUSPENDM**	**RG_TERMSEL**	**RG_OPMODE**	
Type	RW	RW	RW				RW	RW	RW	RW	RW		RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:30	**rg_uart_mode**	rg_uart_mode	**UART mode, controls RG_DP_100K_EN** 00: RG_DP_100K_EN = DA_USB_UART_EN 01: RG_DP_100K_EN = DA_USB_UART_EN & ~DA_USB_UART_TX_OE 10: RG_DP_100K_EN = 0 11: RG_DP_100K_EN = 1
29	**force_uart_i**	force_uart_i	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing UART_I to RG_UART_I value. 0: Disable 1: Enable
28	**force_uart_bias_en**	force_uart_bias_en	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing USB20_UART_BIAS_EN to RG_UART_BIAS_EN value. 0: Disable 1: Enable
27	**force_uart_tx_oe**	force_uart_tx_oe	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing USB20_UART_TX_OE to RG_UART_TX_OE value. 0: Disable 1: Enable
26	**force_uart_en**	force_uart_en	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing USB20_UART_EN to RG_UART_EN value. 0: Disable 1: Enable

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Bit(s)	Mnemonic	Name	Description
25	**force_usb_clken**	force_usb_clken	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing USB_CLKEN to RG_USB_CLKEN value. 0: Disable 1: Enable
24	**force_drvvbus**	force_drvvbus	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing USBSIF_DRVVBUS to RG_USB20_DRVVBUS value. 0: Disable 1: Enable
23	**force_datain**	force_datain	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal DATA_IN to a specific value. 0: Disable 1: Enable
22	**force_txvalid**	force_txvalid	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal TXVALID to a specific value. 0: Disable 1: Enable
21	**force_dm_pulldown**	force_dm_pulldown	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal DMPULLDOWN to a specific value. 0: Disable 1: Enable
20	**force_dp_pulldown**	force_dp_pulldown	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal DPPULLDOWN to a specific value. 0: Disable 1: Enable
19	**force_xcvrsel**	force_xcvrsel	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal XCVRSEL to a specific value. 0: Disable 1: Enable
18	**force_suspendm**	force_suspendm	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal SUSPENDM to a specific value. 0: Disable 1: Enable
17	**force_termsel**	force_termsel	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal TERMSEL to a specific value. 0: Disable 1: Enable
16	**force_opmode**	force_opmode	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal OPMODE to a specific value. 0: Disable 1: Enable
15	**utmi_muxsel**	utmi_muxsel	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing all PHY UTMI signals to specific values. 0: Disable

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Bit(s)	Mnemonic	Name	Description
			1: Enable
14	**RG_RESET**	RG_RESET	**Used for controlling PHY UTMI signal USB20_RESET = RG_RESET for software reset.**
13:10	**RG_DATAIN**	RG_DATAIN	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling PHY UTMI signal DATA_IN[31:0] = 4{RG_DATAIN} when force_datain = 1 or utmi_muxsel = 1.
9	**RG_TXVALIDH**	RG_TXVALIDH	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling PHY UTMI signal TXVALIDH when force_txvalid = 1 or utmi_muxsel = 1.
8	**RG_TXVALID**	RG_TXVALID	**When in USB PHY FT test mode, bypasses PHY UTMI signals.** Used for controlling PHY UTMI signal TXVALID when force_txvalid = 1 or utmi_muxsel = 1.
7	**RG_DMPULLDOEN**	RG_DMPULLDOWN	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling PHY UTMI signal DMPULLDOWN when force_dm_pulldown = 1 or utmi_muxsel = 1.
6	**RG_DPPULLDOWN**	RG_DPPULLDOWN	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling PHY UTMI signal DPPULLDOWN when force_dp_pulldown = 1 or utmi_muxsel = 1.
5:4	**RG_XCVRSEL**	RG_XCVRSEL	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling PHY UTMI signal XCVRSEL[1:0] when force_xcvrsel = 1 or utmi_muxsel = 1.
3	**RG_SUSPENDM**	RG_SUSPENDM	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used to control PHY UTMI signal SUSPENDM when force_suspendm = 1 or utmi_muxsel = 1.
2	**RG_TERMSEL**	RG_TERMSEL	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling PHY UTMI signal TERMSEL when force_termsel = 1 or utmi_muxsel = 1.
1:0	**RG_OPMODE**	RG_OPMODE	**When in USB PHY FT test mode, bypasses PHY UTMI** Used for controlling PHY UTMI signal OPMODE[1:0] when force_opmode = 1 or utmi_muxsel = 1.

1121006C **U2PHYDTM1** **USB20 PHYD Control UTMI 1 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**PRBS7_EN**		**PRBS7_BITCNT**						**CLK48M_EN**	**CLK60M_EN**			**RG_UART_I**	**RG_UART_BIAS_EN**	**RG_UART_TX_OE**	**RG_UART_EN**
Type	RW		RW						RW	RW			RW	RW	RW	RW
Reset	0		0	0	0	0	0	0	0	0			0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**force_vbusvalid**	**force_sessend**	**force_bvalid**	**force_avalid**	**force_iddig**	**force_idpullup**			**RG_VBUSVALID**	**RG_SESSEND**	**RG_BVALID**	**RG_AVALID**	**RG_IDDIG**	**RG_IDPULLUP**
Type			RW	RW	RW	RW	RW	RW			RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0			0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31	**PRBS7_EN**	RG_USB20_PRBS7_EN	**Enables USB20 on-chip PRBS7 decoder**
29:24	**PRBS7_BITCNT**	RG_USB20_PRBS7_BITCNT	**USB20 on-chip PRBS7 compare bit count** = (rg_prbs7_bitcnt+1)*210
23	**CLK48M_EN**	RG_USB20_CLK48M_EN	**Enables MAC 48MHz clock** 0: Disable 1: Enable
22	**CLK60M_EN**	RG_USB20_CLK60M_EN	**Enables MAC 60MHz clock** 0: Disable 1: Enable
19	**RG_UART_I**	RG_UART_I	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling DA_USB20_UART_I when force_uart_i = 1.
18	**RG_UART_BIAS_EN**	RG_UART_BIAS_EN	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling USB20_UART_BIAS_EN when force_uart_bias_en = 1.
17	**RG_UART_TX_OE**	RG_UART_TX_OE	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling USB20_UART_TX_OE when force_uart_tx_oe = 1.
16	**RG_UART_EN**	RG_UART_EN	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling USB20_UART_EN when force_uart_en = 1.
13	**force_vbusvalid**	force_vbusvalid	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal vbusvalid to a specific value. 0: Disable 1: Enable
12	**force_sessend**	force_sessend	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal sessend to a specific value. 0: Disable 1: Enable
11	**force_bvalid**	force_bvalid	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal bvalid to a specific value. 0: Disable 1: Enable
10	**force_avalid**	force_avalid	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal avalid to a specific value. 0: Disable 1: Enable
9	**force_iddig**	force_iddig	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal iddig to a specific value. 0: Disable 1: Enable
8	**force_idpullup**	force_idpullup	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal idpullup to a specific value. 0: Disable 1: Enable
5	**RG_VBUS**	RG_VBUSVALID	**When in USB PHY FT test mode, bypasses PHY UTMI**

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Bit(s)	Mnemonic	Name	Description
	VALID		**signals** Used for controlling PHY UTMI signal VBUSVALID when force_vbusvalid = 1 or utmi_muxsel = 1.
4	RG_SESSEND	RG_SESSEND	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling PHY UTMI signal SESSEND when force_sessend = 1 or utmi_muxsel = 1.
3	RG_BVALID	RG_BVALID	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling PHY UTMI signal BVALID when force_bvalid = 1 or utmi_muxsel = 1.
2	RG_AVALID	RG_AVALID	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling PHY UTMI signal AVALID when force_avalid = 1 or utmi_muxsel = 1.
1	RG_IDDIG	RG_IDDIG	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling PHY UTMI signal IDDIG when force_iddig = 1 or utmi_muxsel = 1.
0	RG_IDPULLUP	RG_IDPULLUP	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling PHY UTMI signal IDPULLUP when force_idpullup = 1 or utmi_muxsel = 1.

11210070 U2PHYDMON0 USB20 PHYD Monitor 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name									PRBS7_BERTH							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	PRBS7_BERTH	RG_USB20_PRBS7_BERTH	USB20 PRBS7 bit error rate passed/failed threshold

11210074 U2PHYDMON1 USB20 PHYD Monitor 1 Register 22200000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	USB20_UART_O	RGO_USB20_LB_PASS	RGO_USB20_LB_DONE	BVALID	IDDIG	VBUSVALID	SESSEND	AVALID	USB20_LINE_STATE		USB20_HST_DISCON	USB20_TX_READY	USB20_RX_ERROR	USB20_RX_ACTIVE	USB20_RX_VALIDH	USB20_RX_VALID
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO		RO	RO	RO	RO	RO	RO
Reset	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	USB20_DATA_OUT															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	USB20_UART_O	USB20_UART_O	**USB20_UART_O**
30	RGO_USB20_LB_PASS	RGO_USB20_LB_PASS	**Loopback passed, active high** Should be checked after loopback_en is disabled.
29	RGO_USB20_LB_DONE	RGO_USB20_LB_DONE	**Loopback done, active high** Should be checked after loopback_en is disabled.
28	BVALID	AD_USB20_BVALID	**OTG BVALID**
27	IDDIG	USB20_IDDIG	**OTG IDDIG**
26	VBUSVALID	AD_USB20_VBUSVALID	**OTG VBUSVALID**
25	SESSEND	AD_USB20_SESSEND	**OTG SESSEND**
24	AVALID	AD_USB20_AVALID	**OTG AVALID**
23:22	USB20_LINE_STATE	USB20_LINE_STATE	**Line state**
21	USB20_HST_DISCON	USB20_HST_DISCON	**Host disconnection (host only)**
20	USB20_TX_READY	USB20_TX_READY	**Data transmission is ready.**
19	USB20_RX_ERROR	USB20_RX_ERROR	**Receiving error**
18	USB20_RX_ACTIVE	USB20_RX_ACTIVE	**Receiving is active.**
17	USB20_RX_VALIDH	USB20_RX_VALIDH	**High byte of received data is valid.**
16	USB20_RX_VALID	USB20_RX_VALID	**Received data are valid.**
15:0	USB20_DATA_OUT	USB20_DATA_OUT	

11210078 **U2PHYDMON2** **USB20 PHYD Monitor 2 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rgo_txvalid_cnt								rgo_rxactive_cnt							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RGO_USB20_LB_BERCNT								USB20_PROBE_OUT							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	rgo_txvalid_cnt	rgo_txvalid_cnt	**USB PHY UTMI interface USB20_TX_VALID active count** When rg_debug_en = 1, the counter will count tx_valid active times.
23:16	rgo_rxactiv	rgo_rxactive_cnt	**USB PHY UTMI interface USB20_RX_ACTIVE active count**

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Bit(s)	Mnemonic	Name	Description
	e_cnt		When rg_debug_en = 1, the counter will count rx_active active times.
15:8	**RGO_USB20_LB_BERCNT**	RGO_USB20_LB_BERCNT	**Loopback Bit Error Counter**
7:0	**USB20_PROBE_OUT**	USB20_PROBE_OUT	**Outputs debugging signal output, selected by RG_PROBE_SEL[4:0]** Connect to GPIO in normal operation debugging mode and also connect to registers for ACD ABIST.

1121007C U2PHYDMON3 USB20 PHYD Monitor 3 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RGO_PRBS7_ERRCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RGO_PRBS7_DONE	RGO_PRBS7_LOCK	RGO_PRBS7_PASS	RGO_PRBS7_PASSTH
Type													RO	RO	RO	RO
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16	**RGO_PRBS7_ERRCNT**	RGO_USB20_PRBS7_ERRCNT	**USB20 PRBS7 bit error count indicator**
3	**RGO_PRBS7_DONE**	RGO_USB20_PRBS7_DONE	**USB20 PRBS7 done indicator** Finish compare
2	**RGO_PRBS7_LOCK**	RGO_USB20_PRBS7_LOCK	**USB20 PRBS7 locked indicator**
1	**RGO_PRBS7_PASS**	RGO_USB20_PRBS7_PASS	**USB20 PRBS7 passed indicator** Bit error free
0	**RGO_PRBS7_PASSTH**	RGO_USB20_PRBS7_PASSTH	**USB20 PRBS7 passed threshold indicator** Bit error < BERTH

112100FC REGFCOM USB Common Register 00002800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_PAGE															
Type	RW															
Reset	0	0	0	0	0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Process_code															
Type	RO															
Reset	0	0	1	0	1	0	0	0								

Bit(s)	Mnemonic	Name	Description
31:24	**RG_PAGE**	RG_PAGE	**RG_PAGE [3:0]: Port page index registers for I2C page base registers. The register is I2C access only.**

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Bit(s)	Mnemonic	Name	Description
			4'h0: Port 0 4'h1: Port 1 4'h2: Port 2 4'h3: Port 3 4'hx: 4'hf: Port f RG_PAGE[7:0]: Function page index registers for I2C page base registers. The register is I2C access only. 4'h0: USB20 4'h1: USB30 digital 4'h2: USB30 phya 4'hf: Frequency meter
15:8	**Process_code**	PROCESS_CODE	**Process code** u65: 8'h65 t55: 8'h55 t40: 8'h40

11210F00 FMCR0 Frequency Meter Control 0 Registers 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_LOCKTH				RG_MONCLK_SEL		RG_FM_MODE	RG_FREQDET_EN	CYCLECNT[23:16]							
Type	RW				RW		RW	RW	RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CYCLECNT[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28	**RG_LOCKTH**	RG_LOCKTH	**Detects PLL lock threshold**
27:26	**RG_MONCLK_SEL**	RG_MONCLK_SEL	**Selects monitor clock** 00: AD_USB_MONCLK 01: AD_USB_MONCLK1 10: AD_USB_MONCLK2 11: AD_USB_MONCLK3
25	**RG_FM_MODE**	RG_FM_MODE	**Frequency meter mode** 0: Normal mode; frequency detection only once. 1: Detect PLL lock mode
24	**RG_FREQDET_EN**	RG_FREQDET_EN	**Enables frequency meter** 0: Disable 1: Enable
23:0	**CYCLECNT**	RG_CYCLECNT	**Cycles of monclk to be measured**

11210F04 FMCR1 Frequency Meter Control 1 Registers 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_TARGET[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_TARGET[15:0]															

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Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	RG_TARGET	RG_TARGET	Adjusts capacitance

11210F08 FMCR2 Frequency Meter Control 2 Registers 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RG_OFFSET[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_OFFSET[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	RG_OFFSET	RG_OFFSET	Frequency meter out offset tolerance

11210F0C FMMONR0 Frequency Meter Monitor 0 Registers 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**USB_FM_OUT[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**USB_FM_OUT[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	USB_FM_OUT	USB_FM_OUT	Frequency meter detection result

11210F10 FMMONR1 Frequency Meter Monitor 1 Registers 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**RG_FRCK_EN**							**USBPLL_LOCK**	**USB_FM_VLD**
Type								RW							RO	RO
Reset								0							0	0

Bit(s)	Mnemonic	Name	Description
8	RG_FRCK_EN	RG_FRCK_EN	**Enables free clock** 0: Disable

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Bit(s)	Mnemonic	Name	Description
			1: Enable
1	**USBPLL_LOCK**	USBPLL_LOCK	**Monitor clock lock signal**
0	**USB_FM_VLD**	USB_FM_VLD	**Frequency meter detection done**

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5.7 SPI Interface Controller

5.7.1 Introduction

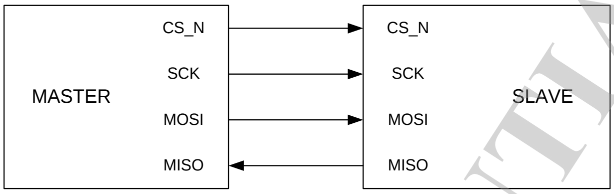

Figure 5-12. Pin connection between SPI master and SPI slave

The SPI interface is a bit-serial, four-pin transmission protocol. Figure 5-12 is an example of the connection between the SPI master and SPI slave. The SPI interface controller is a master responsible of the data transmission with the slave.

5.7.2 Pin Description

Table 5-3. SPI controller interface

Signal name	Type	Description
CS_N	O	Low active chip selection signal
SCK	O	The (bit) serial clock
MOSI	O	Data signal from master output to slave input
MISO	I	Data signal from slave output to master input

5.7.3 Transmission Formats

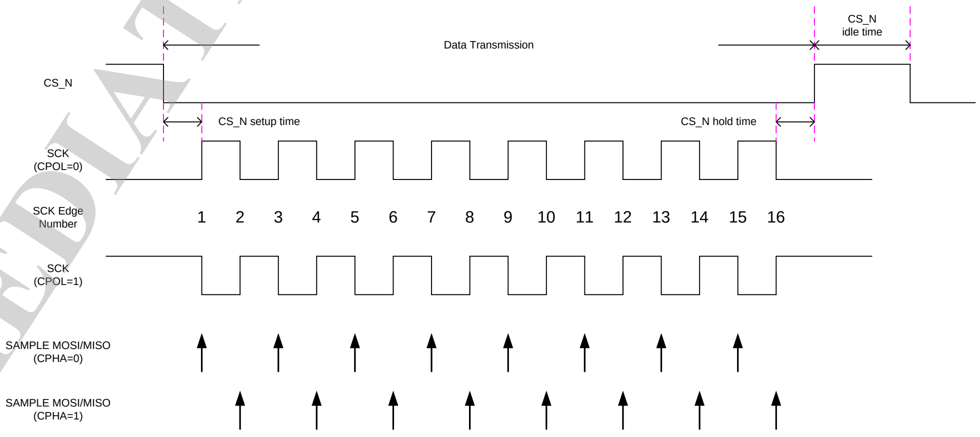

Figure 5-13. SPI transmission formats

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Figure 5-13 shows the waveform during the SPI transmission. The low active CS_N determines the start point and end point of one transaction. The CS_N setup time, hold time and idle time are also depicted.

CPOL defines the clock polarity in the transmission. Two types of polarity can be adopted, i.e. polarity 0 and polarity 1. Figure 5-13 is an example of both clock polarities (CPOL).

CPHA defines the legal timing to sample MOSI and MISO. Two different methods can be adopted.

5.7.4 Features

The features of the SPI controller (master) are:

- Configurable CS_N setup time, hold time and idle time
- Programmable SCK high time and low time
- Configurable transmitting and receiving bit order
- Two configurable modes for the source of the data to be transmitted. 1) In TX DMA mode, the SPI controller automatically fetches the transmitted data (to be put on the MOSI line) from memory; 2) In TX FIFO mode, the data to be transmitted on the MOSI line are written to FIFO before the start of the transaction.
- Two configurable modes for destination of the data to be received. 1) In RX DMA mode, the SPI controller automatically stores the received data (from MISO line) to memory; 2) In RX FIFO mode, the received data keep being in RX FIFO of the SPI controller. The processor must read back the data by itself.
- Adjustable endian order from/to memory system
- Programmable byte length for transmission
- Unlimited length for transmission. This is achieved by the operation of PAUSE mode. In PAUSE mode, the CS_N signal will keep being active (low) after the transmission. At this time, the SPI controller is in PAUSE_IDLE state, ready to receive the resume command. The state transition is shown in Figure 5-14.
- Configurable option to control CS_N de-assert between byte transfers. The controller supports a special transmission format called CS_N de-assert mode. Figure 5-15 illustrates the waveform in this transmission format.

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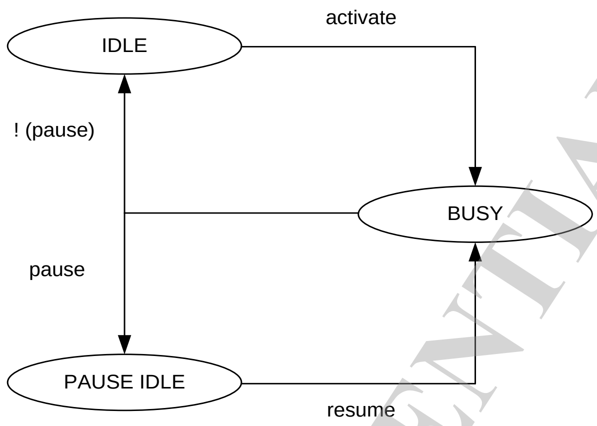

Figure 5-14. Operation flow with or without PAUSE mode

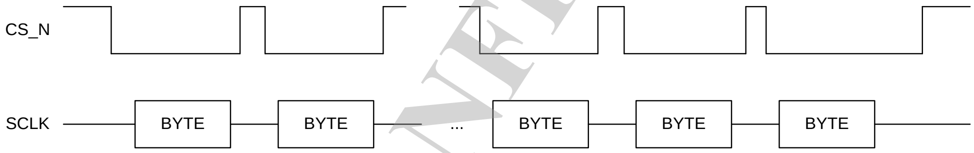

Figure 5-15. CS_N de-assert mode

5.7.5 Block Diagram

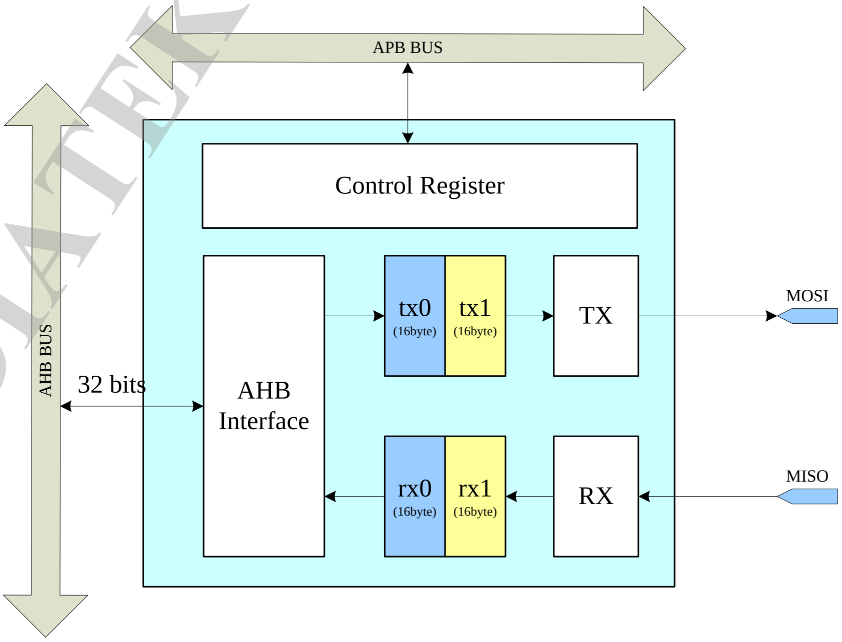

Figure-5-16. Block diagram of SPI

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5.7.6 Register Definition

Module name: SPI Base address: (+1100A000h)

Address	Name	Width	Register Function
1100A000	SPI_CFG0	32	SPI Configuration 0 Register
1100A004	SPI_CFG1	32	SPI Configuration 1 Register
1100A008	SPI_TX_SRC	32	SPI TX Source Address Register
1100A00C	SPI_RX_DST	32	SPI RX Destination Address Register
1100A010	SPI_TX_DATA	32	SPI TX Data FIFO
1100A014	SPI_RX_DATA	32	SPI RX Data FIFO
1100A018	SPI_CMD	32	SPI Command Register
1100A01C	SPI_STATUS0	32	SPI Status 0 Register
1100A020	SPI_STATUS1	32	SPI Status 1 Register
1100A024	SPI_PAD_MACRO_SEL	32	SPI pad_macro Selection Register
1100A028	SPI_CFG2	32	SPI Configuration 2 Register

1100A000 SPI_CFG0 SPI Configuration 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mne	CS_SETUP_COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	CS_HOLD_COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16	CS_SETUP_COUNT	CS_SETUP_COUNT	Chip select setup time = (CS_SETUP_COUNT + 1)*CLK_PERIOD; CLK_PERIOD is the cycle time of the clock SPI engine adopts.
15:0	CS_HOLD_COUNT	CS_HOLD_COUNT	The chip select hold time = (CS_HOLD_COUNT+1) * CLK_PERIOD.

1100A004 SPI_CFG1 SPI Configuration 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GET_TICK_DLY						PACKET_LENGTH									
Type	RW						RW									
Reset	0	0	0				0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PACKET_LOOP_CNT								CS_IDLE_COUNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:29	GET_TICK_DLY	GET_TICK_DLY	**If the speed of SPI is not fast enough, these three bits can help tolerance get_tick timing.** The timing range between get_tick is one cycle depending on the SPI system clock.
25:16	PACKET_L	PACKET_LENGTH	

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Bit(s)	Mnemonic	Name	Description
	ENGTH		
15:8	PACKET_LOOP_CNT	PACKET_LOOP_CNT	**PACKET_LENGTH[9:0] defines the number of bytes in one packet, and PACKET_LOOP_CNT[7:0] defines the number of packets within one transaction.** The number of bytes in one packet = PACKET_LENGTH + 1. The number of packets in one transaction = PACKET_LOOP_CNT + 1. Total bytes of one transaction = (PACKET_LENGTH + 1)*(PACKET_LOOP_CNT + 1).
7:0	CS_IDLE_COUNT	CS_IDLE_COUNT	**Chip select idle time between consecutive transaction = (CS_HOLD_COUNT + 1)*CLK_PERIOD**

1100A008 SPI_TX_SRC SPI TX Source Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI_TX_SRC[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_TX_SRC[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	SPI_TX_SRC	SPI_TX_SRC	**If TX_DMA_EN is set, the data to be put on the MOSI line will be kept in memory in advance, and the SPI controller will automatically read the data from memory.** SPI_TX_SRC defines the memory address from which SPI controller starts to read data.

1100A00C SPI_RX_DST SPI RX Destination Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI_RX_DST[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_RX_DST[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	SPI_RX_DST	SPI_RX_DST	**If RX_DMA_EN is set, the received data from the MISO line will be moved to memory automatically by the SPI controller.** SPI_RX_DST defines the memory address to which the SPI controller starts to store the data.

1100A010 SPI_TX_DATA SPI TX Data FIFO 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI_TX_DATA[31:16]															
Type	WO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_TX_DATA[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	SPI_TX_DATA	SPI_TX_DATA	**The depth of the TX FIFO is 32 bytes.** Write to this register will write 4 bytes to TX FIFO. The TX FIFO pointer will automatically move towards the next four bytes. Read from this register will read 4 bytes from FIFO, and TX FIFO pointer will automatically move towards the next four bytes.

1100A014 SPI_RX_DATA SPI RX Data FIFO 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI_RX_DATA[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_RX_DATA[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	SPI_RX_DATA	SPI_RX_DATA	**The depth of the RX FIFO is 32 bytes.** Read from this register will read 4 bytes from RX FIFO. The RX FIFO pointer will automatically move towards the next four bytes. Write to this register will write 4 bytes to FIFO, and the RX FIFO pointer will automatically move towards the next four bytes.

1100A018 SPI_CMD SPI Command Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															PAUSE_IE	FINISH_IE
Type															RW	RW
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_ENDIAN	RX_ENDIAN	RXMSBF	TXMSBF	TX_DMA_EN	RX_DMA_EN	CPOL	CPHA	CS_POL	SAMPLE_SEL	CS_DEASSERT_EN	PAUSE_EN		RST	RESUME	CMD_ACT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
17	PAUSE_IE	PAUSE_IE	**Interrupt enable bit of pause flag in SPI status register**
16	FINISH_IE	FINISH_IE	**Interrupt enable bit of finish flag in SPI status register**
15	TX_ENDIAN	TX_ENDIAN	**Defines whether to reverse the endian order of the data DMA from memory** 0:Does not reverse (default) Only supported in DMA mode.
14	RX_ENDIAN	RX_ENDIAN	**Defines whether to reverse the endian order of the data**

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Bit(s)	Mnemonic	Name	Description
	N		**DMA to memory** 0: Does not reverse (default)
13	**RXMSBF**	RXMSBF	**Indicates data received from MISO line is MSB first or not** Set RXMSBF to 1 for MSB first; otherwise set it to 0.
12	**TXMSBF**	TXMSBF	**Indicates data sent on MOSI line is MSB first or not** Set TXMSBF to 1 for MSB first; otherwise set it to 0.
11	**TX_DMA_EN**	TX_DMA_EN	**DMA mode enable bit of the data to be transmitted** 0: Not to enable (default)
10	**RX_DMA_EN**	RX_DMA_EN	**DMA mode enable bit of the data received** 0: Not to enable (default)
9	**CPOL**	CPOL	**Control bit of SCK polarity** 0: CPOL = 0 1: CPOL = 1
8	**CPHA**	CPHA	**Defines SPI Clock Format 0 or SPI Clock Format 1 during transmission** 0: CPHA = 0 1: CPHA = 1
7	**CS_POL**	CS_POL	**Control bit of chip select polarity** 0: Active low 1: Active high
6	**SAMPLE_SEL**	SAMPLE_SEL	**Control bit of sample edge of MISO** 0: Positive edge 1: Negative edge
5	**CS_DEASSERT_EN**	CS_DEASSERT_EN	**Enable bit of chip select de-assertion mode** Set to 1 to enable this mode.
4	**PAUSE_EN**	PAUSE_EN	**Enable bit of pause mode** Set to 1 to enable this mode.
2	**RST**	RST	**Software reset bit** When this bit is 1, software reset will be active high. Default: 0.
1	**RESUME**	RESUME	**Used when controller is in PAUSE IDLE state** Write 1 to this bit to trigger the SPI controller to resume transfer from PAUSE IDLE state.
0	**CMD_ACT**	CMD_ACT	**Command activate bit** Write 1 to this bit to trigger the SPI controller to start the transaction.

1100A01C <u>**SPI_STATUS0**</u> **SPI Status 0 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**PAUSE**	**FINISH**
Type															RC	RC
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	**PAUSE**	PAUSE	**Interrupt status bit in pause mode** Will be set by the SPI controller when it completes the transaction,

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Bit(s)	Mnemonic	Name	Description
			entering the PAUSE IDLE state.
0	FINISH	FINISH	**Interrupt status bit in non-pause mode** Will be set by the SPI controller when it completes the transaction, entering the IDLE state.

1100A020 SPI_STATUS1 SPI Status 1 Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BUSY
Type																RO
Reset																1

Bit(s)	Mnemonic	Name	Description
0	BUSY	BUSY	**Status flag reflecting SPI controller is busy or not** This bit is low active; 0 means the SPI controller is busy now. 1'b1: idle 1'b0: busy

1100A024 SPI_PAD_MACRO_SEL SPI pad_macro Selection Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PAD_MACRO_SEL		
Type														RW		
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2:0	PAD_MACRO_SEL	PAD_MACRO_SEL	Selects which PAD group SPI will use

1100A028 SPI_CFG2 SPI Configuration 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SCK_LOW_COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SCK_HIGH_COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
31:16	**SCK_LOW_COUNT**	SCK_LOW_COUNT	SCK clock low time = (SCK_LOW_COUNT + 1)*CLK_PERIOD
15:0	**SCK_HIGH_COUNT**	SCK_HIGH_COUNT	SCK clock high time = (SCK_HIGH_COUNT + 1)*CLK_PERIOD

5.7.7 Programming Guide

Follow the steps below to perform SPI transmission:

1. Prepare the data in the memory with its start address to be the "source address".
2. Set up the timing and protocol for the SPI transmission (see Figure 5-13 for detailed setup parameters).
3. Fill the "destination address", which is the start address that you would like to place the received data, and "source address", which is the start address to place the data to be transmitted, into register SPI_RX_DST and SPI_TX_SRC, respectively.
4. Write 1 the CMD_ACT to start the transfer
5. Get the data received from the buffer prepared starting from "destination address".

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5.8 MSDC Controller

5.8.1 Introduction

The MSDC (Memory Stick and SD card Controller) fully supports

- SD memory card specification version 3.0
- SDIO card specification version 3.0
- MMC/eMMC 5.0

5.8.2 Features

Each MSDC contains:

- Interface with MCU by AHB bus
- 32-bit access on AHB bus
- 32-bit access for control registers
- 8-bit/16-bit/32-bit access for FIFO in PIO mode
- Built-in 128 bytes FIFO buffers for transmit and receive
- Built-in CRC circuit
- Basic DMA mode, basic descriptor mode, and enhanced descriptor mode for SD/MMC
- Interrupt capabilities
- Does not support SPI mode for SD/MMC memory card
- Does not support suspend/resume for SD/MMC memory card
- Supports SD3.0 SDR104, data rate up to 208x4Mbps
- Supports SD3.0 DDR50, data rate up to 50x4x2Mbps(4-bit with clock dual edge)
- Supports e-MMC boot-up mode
- 256 programmable serial clock rates on SD/MMC bus from 100kHz to 208MHz
- Card detection capabilities

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5.8.3 Block Diagram

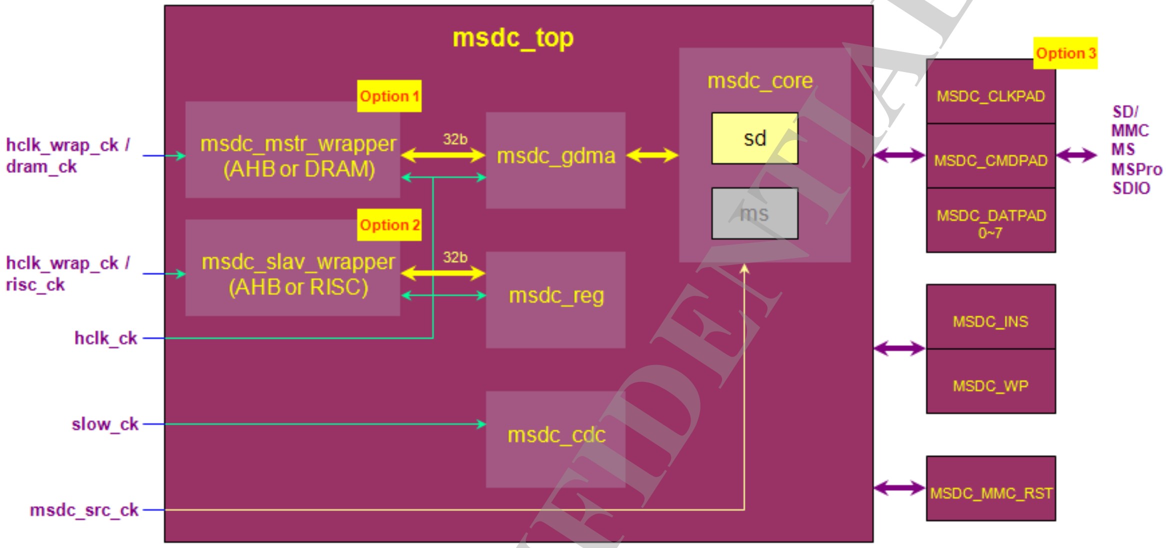

Figure 5-17. Block diagram of MSDC controller

5.8.4 Register Definition

MSDC number	Base address	Feature
MSDC0	0x11230000	EMMC4.5/5.0
MSDC1	0x11240000	SD3.0/SDIO3.0/EMMC4.5
MSDC2	0x11250000	SD3.0/SDIO3.0
MSDC3	0x11260000	SD3.0/SDIO3.0

There are 3 MSDC IPs in this SOC. Use of the registers below are the same except that the base address needs to be changed to respective one.

Module name: MSDC0 Base address: (+11230000h)

Address	Name	Width	Register Function
11230000	**MSDC_CFG**	32	**MSDC Configuration Register** For general configuration of the MS/SD controller
11230004	**MSDC_IOCON**	32	**MSDC IO Configuration Register** Contains the receiver path data latch timing control and interface control bits
11230008	**MSDC_PS**	32	**MSDC Pin Status Register** Stores card detection and write protection pin status. Card detection status can be disabled.
1123000C	**MSDC_INT**	32	**MSDC Interrupt Register** Contains the status of interrupts *Note: The register still shows the status of interrupt even though the interrupt is disabled.*
11230010	**MSDC_INTEN**	32	**MSDC Interrupt Enable Register**

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Address	Name	Width	Register Function
			Contains related enabling bit of interrupts
11230014	MSDC_FIFOCS	32	**MSDC FIFO Control and Status Register** Contains control and status of embedded 128B FIFO
11230018	MSDC_TXDATA	32	**MSDC TX Data Port Register** For PIO mode only. Used to input MSDC write data to card. The access can be AHB1B/2B/4B.
1123001C	MSDC_RXDATA	32	**MSDC RX Data Port Register** For PIO mode only. Used to read back MSDC read data from card. The access can be AHB1B/2B/4B.
11230030	SDC_CFG	32	**SD Configuration Register** Configures MS/SD memory card controller when it is configured as the host of SD memory card. If the controller is configured as the host of memory stick, the contents of the register will have no impact on the operation of the controller.
11230034	SDC_CMD	32	**SD Command Register** Defines a SD memory card command and its attributes. Before MS/SD controller issues a transaction onto SD bus, the application should specify other relative settings such as argument for command. After writing the register by the application, MS/SD controller will issue the corresponding transaction onto SD serial bus. If the command is GO_IDLE_STATE, the controller will have serial clock on SD/MMC bus running 128 cycles before issuing the command.
11230038	SDC_ARG	32	**SD Argument Register** Contains argument of SD/MMC memory card command
1123003C	SDC_STS	32	**SD Status Register** Reflects SD bus status and contains MMC stream write status
11230040	SDC_RESP0	32	**SD Response Register 0** Contains parts of the last SD/MMC memory card bus response. See description in register field SDC_RESP3.
11230044	SDC_RESP1	32	**SD Response Register 1** Contains parts of the last SD/MMC memory card bus response. See description in register field SDC_RESP3.
11230048	SDC_RESP2	32	**SD Response Register 2** Contains parts of the last SD/MMC memory card bus response. See description in register field SDC_RESP3.
1123004C	SDC_RESP3	32	**SD Response Register 3** Contains parts of the last SD/MMC memory card bus response. Register fields SDC_RESP0, SDC_RESP1, SDC_RESP2 and SDC_RESP3 are composed of the last SD/MMC memory card bus response. For response of type R2, i.e. response of the command ALL_SEND_CID, SEND_CSD and SEND_CID, only bit 127 to 0 of response token are stored in register field SDC_RESP0, SDC_RESP1, SDC_RESP2 and SDC_RESP3. SDC_RESP0 = bit 31~0 SDC_RESP1 = bit 63~32 SDC_RESP2 = bit 95~64 SDC_RESP3 = bit 127~96 For response of type R1b in auto CMD12 or R1 in auto CMD23, bit 39 to 8 of response token are stored in register field of SDC_RESP3. For the responses of other types, only bit 39 to 8 of response token are stored in the register field SDC_RESP0.
11230050	SDC_BLK_NUM	32	**SD Block Number Register** Defines block number for block transaction. For single read/write, this register should be set to 1. For multiple read/write, this register should be set to bigger than 1. Set to 0 will cause unexpected result.
11230054	SDC_VOL_CHG	32	**SD Voltage Change Wait Time Register** Defines SD voltage change check wait time.

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Address	Name	Width	Register Function
11230058	SDC_CSTS	32	**SD Card Status Register** After commands with R1 and R1b response, this register will contain the status of the SD/MMC card.
1123005C	SDC_CSTS_EN	32	**SD Card Status Enable Register** Controls which bit of SDC_CSTS will generate the MSDC_INT.SD_CSTA interrupt
11230060	SDC_DATCRC_STS	32	**SD Card Data CRC Status Register** Reflects CRC status of data line[7:0]. Only for MSDC read.
11230070	EMMC_CFG0	32	**EMMC Configuration Register 0** For boot-up mode general configuration of e-MMC version 4.3 and 4.4
11230074	EMMC_CFG1	32	**EMMC Configuration Register 1** For boot-up mode general configuration of e-MMC version 4.3 and 4.4.
11230078	EMMC_STS	32	**EMMC Status Register** Reflects status of e-MMC boot-up mode operation
1123007C	EMMC_IOCON	32	**EMMC IO Control Register** Controls H/W reset pin of e-MMC boot-up mode operation
11230080	SD_ACMD_RESP	32	**SD ACMD Response Register** Stores response of auto command from SD card
11230084	SD_ACMD19_TRG	32	**SD ACMD19 Target Register** Selects target delay line to run ACMD19 sequence
11230088	SD_ACMD19_STS	32	**SD ACMD19 Status Register** Stores result of auto command 19 from SD card
1123008C	DMA_SA_HIGH4BIT	32	**DMA Current Address Register of High 4 Bits** Contains start address high 4 bits of the 36-bit address for 64G DRAM access
11230090	DMA_SA	32	**DMA Start Address Register** Contains start address of DMA descriptor
11230094	DMA_CA	32	**DMA Current Address Register** Contains current DMA address
11230098	DMA_CTRL	32	**DMA Control Register** Controls DMA operation
1123009C	DMA_CFG	32	**DMA Configuration Register** Configures DMA operation
112300A0	SW_DBG_SEL	32	**MSDC S/W Debug Selection Register** Selects SW debugging output
112300A4	SW_DBG_OUT	32	**MSDC S/W Debug Output Register** Shows selected debugging output
112300A8	DMA_LENGTH	32	**DMA Length Register** Sets up basic DMA operation length
112300B0	PATCH_BIT0	32	**MSDC Patch Bit Register 0** Configures patch function. For normal function, this bit should be kept at default value.
112300B4	PATCH_BIT1	32	**MSDC Patch Bit Register 1** Configures patch function. For normal function, this bit should be kept at default value.
112300B8	PATCH_BIT2	32	**MSDC Patch Bit Register 2** Configures patch function. For normal function, this bit should be kept at default value.
112300F0	PAD_TUNE0	32	**MSDC Pad Tuning Register 0** Configures delay line embedded in pad macro
112300F8	DAT_RD_DLY0	32	**MSDC Data Delay Line Register 0**

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Address	Name	Width	Register Function
			Configures delay line embedded in pad macro
112300FC	DAT_RD_DLY1	32	**MSDC Data Delay Line Register 1** Configures delay line embedded in pad macro
11230110	HW_DBG_SEL	32	**MSDC H/W Debug Selection Register** Selects HW debugging output
11230114	MAIN_VER	32	**MSDC Main Version Register** Version code of MSDC IP
11230118	ECO_VER	32	**MSDC ECO Version Register** ECO version code of MSDC IP
11230180	EMMC50_PAD_CTL0	32	**MSDC eMMC5.0 CLK Pad Control Register 0** Configures eMMC5.0 SD CLK pad for duty cycle corrector
11230184	EMMC50_PAD_DS_CTL0	32	**MSDC eMMC5.0 DS Pad Control Register 0** Configures eMMC5.0 SD DS pad
11230188	EMMC50_PAD_DS_TUNE	32	**MSDC eMMC5.0 DS Pad Tuning Register** Configures delay line embedded in DS pad macro
1123018C	EMMC50_PAD_CMD_TUNE	32	MSDC eMMC5.0 CMD Pad Tuning Register
11230190	EMMC50_PAD_DAT01_TUNE	32	MSDC eMMC5.0 DAT0/1 Pad Tuning Register
11230194	EMMC50_PAD_DAT23_TUNE	32	MSDC eMMC5.0 DAT2/3 Pad Tuning Register
11230198	EMMC50_PAD_DAT45_TUNE	32	MSDC eMMC5.0 DAT4/5 Pad Tuning Register
1123019C	EMMC50_PAD_DAT67_TUNE	32	MSDC eMMC5.0 DAT6/7 Pad Tuning Register
11230204	EMMC51_CFG0	32	**eMMC51 Configuration Register 0** Configures MS/SD memory card controller when it is configured as the host of SD memory card. If the controller is configured as the host of memory stick, the contents of the register will not affect the operation of the controller.
11230208	EMMC50_CFG0	32	**eMMC50 Configuration Register0** Configures MS/SD memory card controller when it is configured as the host of SD memory card. If the controller is configured as the host of memory stick, the contents of the register will not affect the operation of the controller.
1123020C	EMMC50_CFG1	32	**eMMC50 Configuration Register 1** Configures MS/SD memory card controller when it is configured as the host of SD memory card. If the controller is configured as the host of memory stick, the contents of the register will not affect the operation of the controller.
1123021C	EMMC50_CFG2	32	**AHB2AXI Wrapper Control Register** Sets up wrapper work mode
11230220	EMMC50_CFG3	32	
11230224	EMMC50_CFG4	32	
11230228	EMMC50_BLOCK_LENGTH	32	

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11230000 MSDC_CFG MSDC Configuration Register 02400099

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SCLK STOP SEL	START_BIT		HS400CK MD	CCKMD		CCKDIV[11:8]			
Type							RW	RW		RW	RO		RW			
Reset							1	0	0	1	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CCKDIV[7:0]								CCKSB	BV18PSS	BV18SDT	CCKDRVE	PIO	RST	CCKPD	MSDC
Type	RW								RU	RU	RW	RW	RW	W1C	RW	RW
Reset	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1

Bit(s)	Mnemonic	Name	Description
25	SCLKSTOPSEL	SCLK_STOP_SEL	**In DDR mode, stops SCLK when device is idle whether checking SCLK phase or not** 1'b0: Stop sclk not checking SCLK phase 1'b1: Stop sclk checking SCLK phase; fix 1/4T sclk glitch in DDR mode
24:23	START_BIT	START_BIT	
22	HS400CKMD	HS400_CK_MODE	**Selects HS400 clock mode**
21:20	CCKMD	CARD_CK_MODE	2'b00: Use clock divider output divided by msdc_src_ck as msdc_ck. Bit[15]~bit[8] should be programmed. 2'b01: Use msdc_src_ck as msdc_ck, bit[15]~bit[8] is ignored. 2'b10: DDR mode. Also use clock divider output divided by msdc_src_ck as msdc_ck. Bit[15]~bit[8] should be programmed. 2'b11: HS400 mode. Also use clock divider output and msdc_src_ck as msdc_ck. Bit[15]~bit[8] should be programmed.
19:8	CCKDIV	CARD_CK_DIV	**MS/SD card clock divider** Controls clock frequency of serial clock on MS/SD bus. Refer to "Data Line Latching Timing Diagram" and "Response Latching Timing Diagram". For non-DDR mode, msdc_ck equals SD bus clock. (Example: For SDR25 or HS, msdc_ck and SD bus clock will be 50MHz) For DDR mode, msdc_ck denotes MSDC internal clock which will be doubled to SD bus clock. (Example: For DDR50, msdc_ck should be set to 100MHz, and bus clock will be 50MHz.) 8'b00000000: msdc_ck = (1/2)*msdc_src_ck 8'b00000001: msdc_ck = [1/(4*1)]*msdc_src_ck 8'b00000010: msdc_ck = [1/(4*2)]*msdc_src_ck 8'b00000011: msdc_ck = [1/(4*3)]*msdc_src_ck 8'b00010000: msdc_ck = [1/(4*16)]*msdc_src_ck 8'b11111111: msdc_ck = [1/(4*255)]*msdc_src_ck
7	CCKSB	CARD_CK_STABLE	**MS/SD card clock is stable or not** After programming CARD_CK_MODE or CARD_CK_DIV, this bit will immediately become 0 and return to 1 if stable. Poll this register to ensure safety control of MSDC. 1'b0: Clock output is not stable. 1'b1: Clock output is stable.
6	BV18PSS	BV_1P8_PASS	**MSDC Bus voltage 1.8V detection status** S/W should check this bit after BUS_VOL_18V_START_DET turns to 0 from 1. 1'b0: Error in voltage detection 1'b1: No error in voltage detection
5	BV18SDT	BV_1P8_START_DET	**MSDC bus voltage 1.8V detection sequence start event** SW writes 1 to this bit to trigger HW outputting 1.8V clock for 1ms and automatically detecting CMD/DAT line sequence for voltage change is passed or not. HW will clear this bit to 0 after the detection is finished. The passed or failed status is stored in bit[6] BUS_VOL_18V_PASS.
4	CCKDRVE	CARD_CK_DRV_EN	**SD/MS card bus clock drive enable bit** Set this bit to 1 to enable MSDC bus clock driver. The default bus state depends on MSDC_CFG][1] CARD_CK_PWDN bit. If MSDC_CFG[1] CARD_CK_PWDN=1, the default clock state will

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Bit(s)	Mnemonic	Name	Description
			be free running. If MSDC_CFG[1] CARD_CK_PWDN=0, the default clock state will be gated to 0. Set this bit to 0 will put the bus state into "tri-state". Default: 1 1'b0: Put the clock pad into tri-state 1'b1: Enable MSDC to drive clock pad. The state of CLK depends on MSDC_CFG[1] CARD_CK_PWDN.
3	**PIO**	PIO_MODE	**MS/SD PIO mode** Selects PIO mode. Default: PIO mode 1'b0: DMA mode 1'b1: PIO mode
2	**RST**	RST	**Software reset** Writing 1 to this register will cause internal synchronous reset of MS/SD controller, and it will not reset register settings and DMA controller. The reset sequence is done when this bit becomes 0. S/W should wait for this bit to return to 0 after writing 1. 1'b0: MS/SD controller is not in reset state. 1'b1: MS/SD controller is in reset state.
1	**CCKPD**	CARD_CK_PWDN	**MSDC bus clock power-down mode** Controls card clock power-down mode 1'b0: Clock is gated to 0 if no command or data is transmitted. 1'b1: Clock is free running even if no command or data is transmitted. (The clock may still be stopped when MSDC write data are not enough or no space for the next read data.)
0	**MSDC**	MSDC	**Selects MS/SD mode** Configures the controller to be the host of memory stick or host of SD/MMC memory card. The default value is configuring the controller as the host of memory stick. 1'b0: Configure controller to be host of memory stick 1'b1: Configure controller to be host of SD/MMC memory card

11230004 MSDC_IOCON MSDC IO Configuration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									RD7SPL	RD6SPL	RD5SPL	RD4SPL	RD3SPL	RD2SPL	RD1SPL	RD0SPL
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name			WD3SPL	WD2SPL	WD1SPL	WD0SPL	WDSPLSEL	WDSPL			RDSPLSEL	DDR50CKD	DDLSEL	RDSPL	RSPL	SDR104CKS
Type			RW	RW	RW	RW	RW	RW			RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23	**RD7SPL**	R_D7_SMPL	**Selects read data 7 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
22	**RD6SPL**	R_D6_SMPL	**Selects read data 6 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge

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Bit(s)	Mnemonic	Name	Description
21	**RD5SPL**	R_D5_SMPL	**Selects read data 5 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
20	**RD4SPL**	R_D4_SMPL	**Selects read data 4 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
19	**RD3SPL**	R_D3_SMPL	**Selects read data 3 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
18	**RD2SPL**	R_D2_SMPL	**Selects read data 2 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
17	**RD1SPL**	R_D1_SMPL	**Selects read data 1 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
16	**RD0SPL**	R_D0_SMPL	**Selects read data 0 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
13	**WD3SPL**	W_D3_SMPL	**Selects SDIO interrupt sample** Only valid when bit 9 is on. 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
12	**WD2SPL**	W_D2_SMPL	**Selects SDIO interrupt sample** Only valid when bit 9 is on. 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
11	**WD1SPL**	W_D1_SMPL	**Selects SDIO interrupt sample** Only valid when bit 9 is on. 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
10	**WD0SPL**	W_D0_SMPL	**Selects CRC status and SDIO interrupt sample** Only valid when bit 9 is on. 1'b0: Sample CRC status and SDIO interrupt by external bus clock rising edge 1'b1: Sample CRC status and SDIO interrupt by external bus clock falling edge
9	**WDSPLSEL**	W_D_SMPL_SEL	**Selects data line rising/falling latch fine-tuning in write transaction** 1'b0: All data line share one value indicated by MSDC_IOCON.W_D_SMPL 1'b1: Each data line has its own selection value indicated by Data line 0: MSDC_IOCON.W_D0_SMPL Data line 1: MSDC_IOCON.W_D1_SMPL Data line 2: MSDC_IOCON.W_D2_SMPL Data line 3: MSDC_IOCON.W_D3_SMPL
8	**WDSPL**	W_D_SMPL	**Selects CRC status and SDIO interrupt sample** 1'b0: Sample CRC status and SDIO interrupt by external bus clock rising edge 1'b1: Sample CRC status and SDIO interrupt by external bus clock falling edge

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Bit(s)	Mnemonic	Name	Description
5	**RDSPLSEL**	R_D_SMPL_SEL	**Selects data line rising/falling latch fine-tuning in read transaction** 1'b0: All data line share one value indicated by MSDC_IOCON.R_D_SMPL 1'b1: Each data line has its own selection value indicated by Data line 0: MSDC_IOCON.R_D0_SMPL Data line 1: MSDC_IOCON.R_D1_SMPL Data line 2: MSDC_IOCON.R_D2_SMPL Data line 3: MSDC_IOCON.R_D3_SMPL Data line 4: MSDC_IOCON.R_D4_SMPL Data line 5: MSDC_IOCON.R_D5_SMPL Data line 6: MSDC_IOCON.R_D6_SMPL Data line 7: MSDC_IOCON.R_D7_SMPL
4	**DDR50CKD**	DDR50_DLY_SEL	**Selects DDR50 output clock delay** 1'b0: Use default clock output 1'b1: Delay 1T msdc_src_ck for clock output
3	**DDLSEL**	D_DLYLINE_SEL	**Selects data line delay line fine-tuning** 1'b0: All data line share one delay selection value indicated by PAD_TUNE.PAD_DAT_RD_RXDLY 1'b1: Each data line has its own delay selection value indicated by Data line 0: DAT_RD_DLY0.DAT0_RD_DLY Data line 1: DAT_RD_DLY0.DAT1_RD_DLY Data line 2: DAT_RD_DLY0.DAT2_RD_DLY Data line 3: DAT_RD_DLY0.DAT3_RD_DLY Data line 4: DAT_RD_DLY1.DAT4_RD_DLY Data line 5: DAT_RD_DLY1.DAT5_RD_DLY Data line 6: DAT_RD_DLY1.DAT6_RD_DLY Data line 7: DAT_RD_DLY1.DAT7_RD_DLY
2	**RDSPL**	R_D_SMPL	**Selects read data sample** 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
1	**RSPL**	R_SMPL	**Selects command response sample** 1'b0: Sample response by external bus clock rising edge 1'b1: Sample response by external bus clock falling edge
0	**SDR104CKS**	SDR104_CLK_SEL	**SDR104 SCLK output clock control** Only used when MSDC_CFG[17:16] CARD_CK_MODE is 2'b01. 1'b0: Bus clock output equals inverted msdc_src_ck 1'b1: Bus clock output equals msdc_src_ck

11230008 **MSDC_PS** **MSDC Pin Status Register** **81FF0002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SDWP							CMD	DAT							
Type	RU							RU	RU							
Reset	1							1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDDBCE														CDSTS	CDEN
Type	RW														RU	RW
Reset	0	0	0	0											1	0

Bit(s)	Mnemonic	Name	Description
31	**SDWP**	SD_WP	**Write Protection Switch status on SD Memory Card** The register bit shows the status of Write Protection Switch on SD Memory Card. There is no default reset value. The pin WP (Write

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Bit(s)	Mnemonic	Name	Description
			Protection) is only useful while the controller is configured for SD Memory Card 1'b0: Write Protection switch on, i.e. memory card will be write-protected. 1'b1: Write Protection switch off, i.e. memory card is writable.
24	**CMD**	CMD	**Command line status** This bit reflects the command line value of MSDC bus.
23:16	**DAT**	DAT	**Data line status** This bit reflects the data line value of MSDC bus. (8-bits)
15:12	**CDDBCE**	CDDEBOUNCE	**Card detection de-bounce timer** The register field specifies the time interval for card detection de-bounce. Its default value is 0. It means that de-bounce interval is one 32KHz cycle. The interval will extend one cycle time of 32KHz by increasing the counter by 1
1	**CDSTS**	CDSTS	**Card detection status** 1'b0: Card detection pin status is logic low. 1'b1: Card detection pin status is logic high.
0	**CDEN**	CDEN	**Enables card detection** Controls the card detection circuit. 1'b0: Disable card detection 1'b1: Enable card detection

1123000C **MSDC_INT** **MSDC Interrupt Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									**AXIRSPER R**				**DMAPROT ECT**	**GPDCSERR**	**BDCSERR**	**AC19DONE**
Type									W1C				W1C	W1C	W1C	W1C
Reset									0				0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SDDCRCER R**	**SDDTO**	**DMAXFDNE**	**SDXFCPL**	**SDCSTS**	**SDRCRCER**	**SDCTO**	**SDCRDY**		**DMAQEPTY**	**SDACDRCRCER**	**SDACDCTO**	**SDACDCRDY**		**MSDCCDSC**	**MMCIRQ**
Type	W1C	W1C	W1C	W1C	RU	W1C	W1C	W1C		W1C	W1C	W1C	W1C		W1C	W1C
Reset	0	0	0	0	0	0	0	0		0	0	0	0		0	0

Bit(s)	Mnemonic	Name	Description
23	**AXIRSPERR**	AXI_RESP_ERR	**AXI BUS response error status**
19	**DMAPROTECT**	DMA_PROTECT	**There is write operation to DMA start address, length, start bit or last BUF bit.**
18	**GPDCSERR**	GPD_CS_ERR	**GPD checksum error detected**
17	**BDCSERR**	BD_CS_ERR	**BD checksum error detected**
16	**AC19DONE**	AUTOCMD19_DONE	**SD auto command 19 status register** When auto-command 19 is enabled, HW will clear this register to 0. As the tuning sequence is finished (32 times), this register will be set to 1 by HW. SW should check AUTOCMD_STS0 and SUTOCMD_STS1 only when this bit is on.
15	**SDDCRCERR**	SD_DATA_CRCERR	**SD data CRC error interrupt** Indicates that MS/SD controller detects a CRC error after reading a block of data from the DAT line or SD/MMC signals a CRC error after writing a block of data to the DAT line.

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Bit(s)	Mnemonic	Name	Description
			1'b0: Otherwise 1'b1: MS/SD controller detects a CRC error after reading a block of data from the DAT line or SD/MMC signals a CRC error after writing a block of data to the DAT line.
14	**SDDTO**	SD_DATTO	**SD data timeout interrupt** Indicates SD/MMC controller detects a timeout condition while waiting for data token on the DAT line. This bit is for both data read and data write. For SD data read, timeout will occur when the read data are not presented. For SD data write, timeout will occur when the write data CRC status is not presented if PATCH_BIT[30] DETECT_WR_CRC_TIMEOUT = 1. 1'b0: Otherwise 1'b1: SD/MMC controller detects a timeout condition while waiting for data token on the DAT line.
13	**DMAXFDNE**	DMA_XFER_DONE	**DMA transfer done interrupt** Indicates status of data block transfer. 1'b0: Otherwise 1'b1: A data block is successfully transferred.
12	**SDXFCPL**	SD_XFER_COMPLETE	**SD data transfer completed interrupt** Indicates transaction which contains data that are completed. While performing tuning procedure (Execute Tuning is set to 1), SD_XFER_COMPLETE is not set to 1.
11	**SDCSTS**	SD_CSTS	**SD CSTA update interrupt** Indicates any bit in register SDC_CSTA is active. The register bit will be set to 1. SW should clear SDC_CSTA, and this bit will be de-asserted automatically. 1'b0: No SD memory card interrupt 1'b1: SD memory card interrupt exists.
10	**SDRCRCER**	SD_RESP_CRCERR	**SD command CRC error interrupt** Indicates SD/MMC controller detects a CRC error after reading a response from the CMD line. 1'b0: Otherwise 1'b1: SD/MMC controller detects a CRC error after reading a response from the CMD line.
9	**SDCTO**	SD_CMDTO	**SD command time-out interrupt** Indicates SD/MMC controller detects a time-out condition while waiting for a response on the CMD line. 1'b0: Otherwise 1'b1: SD/MMC controller detects a time-out condition while waiting for a response on the CMD line.
8	**SDCRDY**	SD_CMDRDY	**SD command ready interrupt** For the command without response, the register bit will be 1 once the command is completed on SD/MMC bus. For command with response without busy, the register bit will be 1 whenever the command is issued onto SD/MMC bus and its corresponding response is received without CRC error. For command with response with busy in DAT0, the register bit will be 1 whenever the command is issued onto SD/MMC bus and its corresponding response is received without CRC error and the DAT0 transited from busy to idle. 1'b0: Otherwise 1'b1: Command finished successfully without CRC error.
6	**DMAQEPTY**	DMA_Q_EMPTY	**DMA queue empty interrupt** Indicates the current DMA queue is empty. Only for descriptor mode and enhance mode.
5	**SDACDRC**	SD_AUTOCMD_R	**SD auto command CRC error interrupt**

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Bit(s)	Mnemonic	Name	Description
	RCER	ESP_CRCERR	Set when detecting a CRC error in the auto command response.
4	SDACDCTO	SD_AUTOCMD_CMDTO	**SD auto command time-out interrupt** Set if no response is returned within a specified cycles (64T in spec) from the end bit of auto command.
3	SDACDCRDY	SD_AUTOCMD_CMDRDY	**SD auto command ready interrupt** Set if auto command is executed without CRC error or timeout.
1	MSDCCDSC	MSDC_CDSC	**MSDC card detection status change interrupt** Indicates if any interrupt for memory card insertion/removal exists. Whenever memory card is inserted or removed and card detection circuit is enabled, i.e. register bit CDEN in register MSDC_PS is set to 1, the register bit will be set to 1. It will be reset when the register is read. 1'b0: Otherwise 1'b1: Card is inserted or removed.
0	MMCIRQ	MMC_IRQ	**MMC card interrupt** 1'b0: Otherwise 1'b1: MMC card interrupt event occurs.

11230010 **MSDC_INTEN** **MSDC Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ENAXIRSPERR				ENDMAPROTECT	ENGPDCSERR	ENBDCSERR	ENAC19DONE
Type									RW				RW	RW	RW	RW
Reset									0				0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ENSDDCRCERR	ENSDDTO	ENDMAXFDNE	ENSDXFCPL	ENSDCSTA	ENSDRCRCER	ENSDCTO	ENSDCRDY	ENSDIOIRQ	ENDMAQEPTY	ENSDACDRCRCER	ENSDACDCTO	ENSDACDCRDY		ENMSDCCDSC	ENMMCIRQ
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0

Bit(s)	Mnemonic	Name	Description
23	ENAXIRSPERR	EN_AXI_RESP_ERR	**Enables AXI bus response error status interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
19	ENDMAPROTECT	EN_DMA_PROTECT	**Enables DMA protection interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
18	ENGPDCSERR	EN_GPD_CS_ERR	**Enables GPD checksum error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
17	ENBDCSERR	EN_BD_CS_ERR	**Enables BD checksum error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
16	ENAC19DONE	EN_AUTOCMD19_DONE	**Enables auto-command 19 completed interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
15	ENSDDCRCERR	EN_SD_DATA_CRCERR	**Enables SD data CRC error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt

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Bit(s)	Mnemonic	Name	Description
14	**ENSDDTO**	EN_SD_DATTO	**Enables SD data timeout interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
13	**ENDMAXFDNE**	EN_SD_DMA_XFER_DONE	**Enables DMA transfer done interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
12	**ENSDXFCPL**	EN_SD_XFER_COMPLETE	**Enables SD data transfer completed interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
11	**ENSDCSTA**	EN_SD_CSTA	**Enables SD CSTA update interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
10	**ENSDRCRCER**	EN_SD_RESP_CRCERR	**Enables SD command CRC error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
9	**ENSDCTO**	EN_SD_CMDTO	**Enables SD command timeout interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
8	**ENSDCRDY**	EN_SD_CMDRDY	**Enables SD command ready interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
7	**ENSDIOIRQ**	EN_SD_SDIOIRQ	**Enables SD SDIO interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
6	**ENDMAQEPTY**	EN_DMA_Q_EMPTY	**Enables DMA queue empty interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
5	**ENSDACDRCRCER**	EN_SD_AUTOCMD_RESP_CRCERR	**Enables SD auto command CRC error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
4	**ENSDACDCTO**	EN_SD_AUTOCMD_CMDTO	**Enables SD auto command time-out interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
3	**ENSDACDCRDY**	EN_AUTOCMD_CMDRDY	**Enables SD auto command ready interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
1	**ENMSDCCDSC**	EN_MSDC_CDSC	**Enables MSDC card detection status change interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
0	**ENMMCIRQ**	EN_MMC_IRQ	**Enables MMC card interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt

11230014 **MSDC_FIFOCS** **MSDC FIFO Control and Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFOCLR								TXFIFOCNT							
Type	RO								RU							
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name									**RXFIFOCNT**							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**FIFOCLR**	FIFOCLR	**Clears embedded FIFO** Write 1 to this bit to clear FIFO. It will become 0 when FIFO is cleared. SW needs to check this bit to make sure clearing FIFO sequence is done. This bit can be used when the data read/write sequence has error and needs to clean the HW FIFO.
23:16	**TXFIFOCNT**	TXFIFOCNT	**TX FIFO count for MSDC write** 8'd0: No data in FIFO 8'd1: 1 byte of data in FIFO 8'd2: 2 bytes of data in FIFO 8'd131: Maximum 131 bytes of data in FIFO Others: Reserved
7:0	**RXFIFOCNT**	RXFIFOCNT	**RX FIFO count for MSDC read** 8'd0: No data in FIFO 8'd1: 1 byte of data in FIFO 8'd2: 2 bytes of data in FIFO 8'd131: Maximum 131 bytes of data in FIFO Others: Reserved

11230018 **MSDC_TXDATA** **MSDC TX Data Port Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**PIOTXDATA[31:16]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**PIOTXDATA[15:0]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**PIOTXDATA**	PIO_TXDATA	**PIO mode TXDATA port** This register can be accessed by byte, half-word or word. This port can only be accessed in PIO mode. Otherwise, the transaction will be discarded.

1123001C **MSDC_RXDATA** **MSDC RX Data Port Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**PIORXDATA[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**PIORXDATA[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31:0	**PIORXDATA**	PIO_RXDATA	**PIO mode RXDATA port** This register can be accessed by byte, half-word or word. This port can only be accessed in PIO mode. Otherwise, the transaction will be discarded.

11230030 SDC_CFG SD Configuration Register 00100000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DTOC										INTBGP	SDIOIDE	SDIO		BUSWD	
Type	RW										RW	RW	RW		RW	
Reset	0	0	0	0	0	0	0	0			0	1	0		0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name															ENWKUPINS	ENWKUPSDIOINT
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DTOC**	DTOC	**Data timeout counter** The period from the end of the initial host read command or the last read data block in a multiple block read operation to the start bit of the next read data block requires at least two serial clock cycles. The counter is used to extend the period (Read Data Access Time) in unit of 1,048,576 serial clocks. 8'b00000000: Extend 1,048,576 more serial clock cycles 8'b00000001: Extend 1,048,576*2 more serial clock cycles 8'b00000010: Extend 1,048,576*3 more serial clock cycles 8'b11111111: Extend 1,048,576*256 more serial clock cycles
21	**INTBGP**	INT_AT_BLOCK_GAP	**Interrupt at block gap** This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Set to 1 will enable interrupt detection at the block gap for a multiple block transfer. Set to 0 will disable interrupt detection during a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0. When the host driver detects an SD card insertion, it will set up this bit according to CCCR of the SDIO card. 1'b0: Disable interrupt detection at block gap 1'b1: Enable interrupt detection at block gap
20	**SDIOIDE**	SDIO_INT_DET_EN	**Enables SDIO interrupt detection** Informs SD controller to sense SDIO interrupt. 1'b0: Disable SDIO interrupt detection 1'b1: Enable SDIO interrupt detection if SDIO bit is also on
19	**SDIO**	SDIO	**SDIO mode enable bit** Enables support to sense SDIO interrupt and disables R4 response CRC check for SDIO card. 1'b0: Disable SDIO mode 1'b1: Enable SDIO mode
17:16	**BUSWD**	BUSWIDTH	**Configures bus width** Defines SD/MMC bus width. 2'b00: 1-bit mode 2'b01: 4-bit mode 2'b10: 8-bit mode 2'b11: Reserved

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Bit(s)	Mnemonic	Name	Description
1	**ENWKUPINS**	WAKEUP_INS_EN	**Card status change wakeup event enable bit** 1'b0: Disable wakeup event for card status change 1'b1: Enable wakeup event for card status change
0	**ENWKUPSDIOINT**	WAKEUP_SDIOINT_EN	**SDIO card interrupt wakeup event enable bit** 1'b0: Disable wakeup event for SDIO card interrupt 1'b1: Enable wakeup event for SDIO card interrupt

11230034 SDC_CMD SD Command Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		VOLSWTH	ACMD		LEN											
Type		RW	RW		RW											
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GOIRQ	STOP	RW	DTYPE			RSPTYP			BREAK	CMD					
Type	RW	RW	RW	RW			RW			RW	RW					
Reset	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30	**VOLSWTH**	VOL_SWTH	**Voltage switch command** 1'b0: Disable voltage switch detection 1'b1: Enable voltage switch detection
29:28	**ACMD**	AUTO_CMD	**Enables auto command** Determines use of auto command functions. This function can be used in all modes including PIO/Basic DMA/Descriptor DMA/Enhanced Mode. There are two methods to stop multiple-block read and write operation. 1. Enabling auto CMD12 Multiple-block read and write commands for memory require CMD12 to stop the operation. When ACMD-12 is used, MSDC issues CMD12 automatically when the last block transfer is completed. Auto CMD12 error is indicated to the MSDC_INT register. The host driver shall not set up this bit if the command does not require CMD12. In particular, secure commands defined in the Part 3 File Security specification do not require CMD12. 2. Enabling auto CMD23 When ACMD-23 is used, MSDC issues a CMD23 automatically before issuing a command specified in the CMD field. The Host Controller Version 3.00 and later versions support this function. By writing the command register, MSDC issues a CMD23 first then a command specified by the CMD field in the SDC_CMD register. If response errors of CMD23 are detected, the second command will not be issued. A CMD23 error is indicated in the MSDC_INT register. 32-bit block count value for CMD23 is set to the SDC_BLOCK_NUM register. 2'b00: Disable auto command 2'b01: Enable auto CMD12 2'b10: Enable auto CMD23 2'b11: Enable re-tuning CMD19
27:16	**LEN**	LEN	**Length** Defines the length of one block (unit: byte) in a data transaction of block mode or the data length (unit: byte) in data transaction of byte mode. The maximum value of block length is 2,048 bytes. 12'b000000000000: Reserved

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Bit(s)	Mnemonic	Name	Description
			12'b000000000001: Block length is 1 byte. 12'b000000000010: Block length is 2 bytes. 12'b011111111111: Block length is 2,047 bytes. 12'b100000000000: Block length is 2,048 bytes.
15	**GOIRQ**	GO_IRQ	**GO_IRQ command** Indicates if the command is GO_IRQ_STATE (CMD40) and used only for MMC protocol. If the command is GO_IRQ_STATE, the period between command token and response token will not be limited. 1'b0: The command is not GO_IRQ_STATE. 1'b1: The command is GO_IRQ_STATE.
14	**STOP**	STOP	**Stop command** Indicates if the command is a stop transmission command. It should be set to 1 when CMD12 (SD/MMC) or CMD52 with I/O abort (SDIO) is to be issued. 1'b0: The command is not a stop transmission command. 1'b1: The command is a stop transmission command.
13	**RW**	RW	**Selects command read write** The register bit defines the command is a read command or write command. The register bit is valid only when the command causes a transaction with data token. 1'b0: The command is a read command. 1'b1: The command is a write command.
12:11	**DTYPE**	DTYPE	**Selects data block** Defines data token type for the command. 2'b00: No data token for the command 2'b01: Single block transaction (only available in block mode) 2'b10: Multiple block transaction. (only available in block mode) 2'b11: Stream operation. It should only be used in MMC protocol. (Only available in block mode)
9:7	**RSPTYP**	RSPTYP	**Command response type** 3'b000: This command has no response. 3'b001: The command has R1/R5/R6/R7 response. The response token is 48-bit with CRC check (for SD/MMC/SDIO) (not including the SDIO abort command). 3'b010: The command has R2 response. The response token is 136-bit (for SD/MMC). 3'b011: The command has R3 response. The response token is 48-bit response, no CRC check (for SD/MMC). 3'b100: The command has R4 response. The response token is 48-bit without CRC check (for SDIO). The response token is 48-bit with CRC check (for MMC). 3'b111: The command has R1b response. The response token is 48-bit (for SD/MMC/SDIO).
6	**BREAK**	BREAK	**Aborts pending MMC GO_IRQ command** Only valid for a pending GO_IRQ_MODE command waiting for MMC interrupt response. 1'b0: Not a beak command 1'b1: Break a pending MMC GO_IRQ_MODE command in the controller
5:0	**CMD**	CMD	**SD memory card command**

11230038 SDC_ARG SD Argument Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ARG[31:16]															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ARG[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ARG**	ARG	Memory card controller argument register

1123003C SDC_STS SD Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MMCSWRCPL**															**CMD_WR_BUSY**
Type	RU															W1C
Reset	0															0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**CMDBSY**	**SDCBSY**
Type															RU	RU
Reset															0	0

Bit(s)	Mnemonic	Name	Description
31	**MMCSWRCPL**	MMC_STREAM_WR_COMPL	**MMC stream mode write data are all flushed to MMC card.** SW can use this bit to confirm the last write data are flushed to MMC before issuing the STOP command. This bit is only valid when command SDC_CMD.DTYPE=2'b11. 1'b0: Last data are partially inside MSDC. 1'b1: Last data are flushed to MMC card.
16		CMD_WR_BUSY	
1	**CMDBSY**	CMDBUSY	**SD command line busy status** SW should always read this bit to make sure the command line is not busy before sending the next command. If the command is R1B or data read/write command, SW should also check the SDCBUSY bit. *Note: When auto command 12 is enabled, this bit will be asserted immediately after SDC_CMD is written and de-asserted after auto-command 12 is finished.* 1'b0: No transmission is going on CMD line on SD bus 1'b1: There exists transmission going on CMD line on SD bus
0	**SDCBSY**	SDCBUSY	**SD controller busy status** 1'b0: SD controller is idle. 1'b1: SD controller is busy.

11230040 SDC_RESP0 SD Response Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RESP0[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RESP0[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31:0	**RESP0**	RESP0	Memory card controller response register 0

11230044 **SDC_RESP1** **SD Response Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP1[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP1[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP1**	RESP1	Memory card controller response register 1

11230048 **SDC_RESP2** **SD Response Register 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP2[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP2[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP2**	RESP2	Memory card controller response register 2

1123004C **SDC_RESP3** **SD Response Register 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP3[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP3[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP3**	RESP3	Memory card controller response register 3

11230050 **SDC_BLK_NUM** **SD Block Number Register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	BLKNUM[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BLKNUM[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:0	**BLKNUM**	BLOCK_NUMBER	**Memory card controller block number** Indicates block number of data transaction. 32'd0: Reserved 32'd1: 1-data block 32'd2: 2-data block 32'd3: 3-data block 32'hffffffff: 4GB-1 data block

11230054 SDC_VOL_CHG SD Voltage Change Wait Time Register 00000145

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VCHGCNT															
Type	RW															
Reset	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	1

Bit(s)	Mnemonic	Name	Description
15:0	**VCHGCNT**	VOL_CHG_WAIT_CNT	**Defines SD voltage change check wait time** The wait time is clock frequency multiplied by VOL_WAIT_TIME.

11230058 SDC_CSTS SD Card Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSTS[31:16]															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSTS[15:0]															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CSTS**	CSTS	**CSTS** The card status field in the response R1 or R1b field. Each bit can be written 1 to clear individually.

1123005C SDC_CSTS_EN SD Card Status Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	CSTS_EN[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSTS_EN[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CSTS_EN**	CSTS_EN	**CSTS_EN** Controls which bit of CSTA will generate MSDC_INT.SDCSTA.

11230060 SDC_DATCRC_STS SD Card Data CRC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCSSN								DCSSP							
Type	RU								RU							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8	**DCSSN**	DAT_CRCSTS_NEG	**MSDC DDR mode negative edge read data CRC status** Reflects CRC status of data line[7:0] in DDR mode. The positive edge CRC status is shown in DAT_CRC_STS[7:0]. Only for MSDC read. 1'b0: No CRC error 1'b1: CRC error
7:0	**DCSSP**	DAT_CRCSTS_POS	**MSDC read data CRC status** Reflects CRC status of data line[7:0]. Only for MSDC read. 1'b0: No CRC error 1'b1: CRC error

11230070 EMMC_CFG0 EMMC Configuration Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BTSUP	BTWDLY											BTACHKDIS	BTMOD	BTSTOP	BTSTART
Type	RW	RW											RW	RW	WO	WO
Reset	0	0	0	0									0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**BTSUP**	BOOT_SUPPORT	**Supports eMMC boot-up** Indicates boot mode is supported or not. 1'b0: Does not support 1'b1: Support

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Bit(s)	Mnemonic	Name	Description
14:12	**BTWDLY**	BOOT_WAIT_DELAY	**eMMC wait delay time** Sets up delay time to wait for MMC device to exit boot-up mode after boot stop bit is set. 3'b000: 0x1,024 clock cycles 3'b001: 1x1,024 clock cycles 3'b010: 2x1,024 clock cycles 3'b111: 7x1,024 clock cycles
3	**BTACHKDIS**	BOOT_ACK_CHK_DIS	**Disables eMMC boot-up mode ACK check** 1'b0: Does ACK pattern check 1'b1: Bypass ACK pattern check
2	**BTMOD**	BOOT_MODE	**eMMC boot-up mode** There are two boot-up modes supported by eMMC 4.4. Reset CMD mode is optional for eMMC 4.3. 1'b0: Pull low CMD mode 1'b1: Reset CMD mode
1	**BTSTOP**	BOOT_STOP	**Stops eMMC boot-up** Indicates boot ACK pattern is supported or not. Read always returns to 0.
0	**BTSTART**	BOOT_START	**eMMC boot-up start signal trigger** The register bit is boot up start signal trigger. Read always returns to 0.

11230074 EMMC_CFG1 EMMC Configuration Register 1 00200003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BTATOC												BTDTOC[19:16]			
Type	RW												RW			
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BTDTOC[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
31:20	**BTATOC**	BOOT_ACK_TOC	**eMMC ack pattern timeout counter** Unit: 2^16 serial clock. SW cannot set it to 12'hFFF.
19:0	**BTDTOC**	BOOT_DAT_TOC	**eMMC read boot data timeout counter** Unit: 2^16 serial clock. SW cannot set it to 20'hFFFFF.

11230078 EMMC_STS EMMC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BTDRCV	BTARCV	BTSTS	BTATO	BTDTO	BTAERR	BTDERR
Type										RU	W1C	RU	W1C	W1C	W1C	W1C
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
6	**BTDRCV**	BOOT_DAT_RECV	**eMMC boot data are received.** This register is for SW to check the first 4-byte boot data are received or not. For other data after the first 4B data, this bit should not be referred to. SW should check RXFIFOCNT instead. 1'b0: No data in RXFIFO 1'b1: The 1st 4B data are in RXFIFO.
5	**BTARCV**	BOOT_ACK_RECV	**eMMC ack is received.** Checking BOOT_ACK_ERR to determine it is passed or failed is also required. 1'b0: No ACK pattern is received. 1'b1: ACK pattern has been received.
4	**BTSTS**	BOOT_UP_STATE	**eMMC boot-up mode status** Indicates if MMC device operates at boot-up mode state. 1'b0: Not in boot-up state 1'b1: Boot-up state is on-going.
3	**BTATO**	BOOT_ACK_TO	**eMMC ACK timeout** Indicates the controller detects a time-out condition while waiting for an ACK pattern on DAT0. 1'b0: No ACK pattern timeout error 1'b1: ACK pattern timeout error
2	**BTDTO**	BOOT_DAT_TO	**eMMC data timeout** Indicates the controller detects a timeout condition while waiting for boot data. 1'b0: No data timeout error 1'b1: Data timeout error
1	**BTAERR**	BOOT_ACK_ERR	**eMMC ACK error** Indicates the status of ACK pattern check result. The bit is set to 1 when there is ACK pattern error. 1'b0: No ACK pattern check error 1'b1: ACK pattern check error
0	**BTDERR**	BOOT_CRC_ERR	**eMMC CRC error** Indicates CRC status of boot data. The bit is set to 1 when there is data CRC error. 1'b0: No data CRC error 1'b1: Data CRC error

1123007C **EMMC_IOCON** **EMMC IO Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**BTRST**
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**BTRST**	BOOT_RST	**Resets eMMC device boot-up mode** Triggers HW reset to set eMMC device to entering pre-idle state. 1'b0: De-assert RST_n from eMMC card 1'b1: Assert RST_n to eMMC card

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11230080 **SD_ACMD_RESP** **SD ACMD Response Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ACMDRESP[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACMDRESP[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	ACMDRESP	AUTOCMD_RESP	**SD auto command response register** Stores response[39:8] of ACMD12/ACMD23/ACMD19.

11230084 **SD_ACMD19_TRG** **SD ACMD19 Target Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													ACMDFTSEL			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	ACMDFTSEL	FINE_TUNE_SEL	**Selects SD auto command 19 test target** After auto-command 19 is triggered, MSDC will only change the phase of the selected one and keep the value of other tuning registers. SW can get the result from AUTOCMD_STS. There are total 32 phases for each delay line. 4'd0: Select PAD_CLK_TXDLY[5:0] as the target to run auto-command19. 4'd1: Select PAD_CMD_RXDLY[5:0] as the target to run auto-command19. 4'd2: Select PAD_DAT_RD_RXDLY[5:0] as the target to run auto-command19. 4'd3: Select PAD_DAT_WR_RXDLY[5:0] as the target to run auto-command19. 4'd4: Select DAT0_RD_DLY[5:0] as the target to run auto-command19. 4'd5: Select DAT1_RD_DLY[5:0] as the target to run auto-command19. 4'd6: Select DAT2_RD_DLY[5:0] as the target to run auto-command19. 4'd7: Select DAT3_RD_DLY[5:0] as the target to run auto-command19. 4'd8: Select DAT4_RD_DLY[5:0] as the target to run auto-command19. 4'd9: Select DAT5_RD_DLY[5:0] as the target to run auto-command19. 4'd10: Select DAT6_RD_DLY[5:0] as the target to run auto-command19. 4'd11: Select DAT7_RD_DLY[5:0] as the target to run auto-

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Bit(s)	Mnemonic	Name	Description
			command19. 4'd12: Select CMD_RESP_RXDLY[5:0] as the target to run auto-command19. Others: Reserved

11230088 **SD_ACMD19_STS** **SD ACMD19 Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ACMD19STS[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACMD19STS[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ACMD19STS**	AUTOCMD19_STS	**SD auto command 19 test result register** When auto-command 19 is enabled, HW will automatically try 32 times of command-19 and store the result into this register. This register contains the 1st to 32rd results in bit[0:31].

1123008C **DMA_SA_HIGH4BIT** **DMA Current Address Register of High 4 Bits** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DMASAHIGH4BIT			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**DMASAHIGH4BIT**	DMA_SURR_ADDR_HIGH4BIT	Sets up the high 4-bit address of start address since the 64G DRAM needs a 36-bit address

11230090 **DMA_SA** **DMA Start Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMASA[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMASA[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DMASA**	DMA_STR_ADDR	**Start address of DMA address**

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Bit(s)	Mnemonic	Name	Description
			Sets up the start address of the DMA. In DMA basic mode, this field indicates the source or destination address of the data transfer which depends on the command. In descriptor base DMA, this is the descriptor chain start address.

11230094 DMA_CA DMA Current Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMACA[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMACA[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DMACA**	DMA_CURR_ADDR	**Current address of DMA address** Reads the current address of DMA descriptor chain.

11230098 DMA_CTRL DMA Control Register 00006008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		BSTSZ			SPLIT1K	LASTBF	DMAALIGN	DMAMOD					READYM	DMARSM	DMASTOP	DMASTART
Type		RW			RW	RW	RW	RW					RO	WO	A0	WO
Reset		1	1	0	0	0	0	0					1	0	0	0

Bit(s)	Mnemonic	Name	Description
14:12	**BSTSZ**	BURST_SIZE	**DMA burst size** Specifies the maximum transfer bytes allowed at the device per DMA burst. This field cannot be modified when the DMA status is 1. 3'd3: 8 bytes 3'd4: 16 bytes 3'd5: 32 bytes 3'd6: 64 bytes Other: Reserved
11	**SPLIT1K**	DMA_SPLIT_1K	**Specifies split burst when corssing 1K boundary address** 1'b0: 1K boundary does not split. 1'b1: 1K boundary splits.
10	**LASTBF**	LAST_BUF	**Last buffer of the basic DMA mode** Indicates the last buffer in basic DMA mode.
9	**DMAALIGN**	DMA_ALIGN	**Specifies address alignment burst size** 1'b0: No DAM burst size alignment 1'b1: DAM burst size alignment
8	**DMAMOD**	DMA_MODE	**DMA operation mode** Indicates operation mode of DMA. 1'b0: Basic DMA mode

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Bit(s)	Mnemonic	Name	Description
			1'b1: Descriptor base DMA mode
3	**READYM**	AHB_READYM	**Only for debugging when DMA hangs** SW checks if AHB bus is ok when GDMA hangs. 0: Bus is abnormal. 1: Bus is normal.
2	**DMARSM**	DMA_RESUME	**DMA resume control register** Resumes DMA transaction. Read always returns to 0.
1	**DMASTOP**	DMA_STOP	**DMA stop control register** Stops DMA transaction. When SW issues STOP command, SW must wait for this bit to be de-asserted or DMA inactive to guarantee stop is done.
0	**DMASTAR T**	DMA_START	**DMA start control register** Starts DMA transaction. Read always returns to 0.

1123009C **DMA_CFG** **DMA Configuration Register** **00000004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**DMACHKSUM12B**
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**MSDCACTIVEEN**				**AHBHPROT2EN**							**LOCKDISABLE**	**DSCPCSEN**	**DMASTS**
Type			RW				RW							RW	RW	RU
Reset			0	0			0	0						1	0	0

Bit(s)	Mnemonic	Name	Description
16	**DMACHKSUM12B**	DMA_CHK_SUM_12B	**Indicates GPD/BD checksum covers 16 bytes or 12 bytes** 1'b0: GPD/BD checksum covers 16 bytes. 1'b1: GPD/BD checksum only covers 12 bytes.
13:12	**MSDCACTIVEEN**	MSDC_ACTIVE_EN	**Indicates how to control msdc_active** 2'b00: Dynamic control msdc_active 2'b01: msdc_active = 0 2'b10: msdc_active = 1 2'b11: Reserved
9:8	**AHBHPROT2EN**	AHB_HPROT_2_EN	**Determines how to control hprot_2 pin of AHB bus** AHB_HPROT_2_EN = 2'b00, and basic DMA mode All the write transfers of a burst will be accessed by bufferable mode except for the last burst of DMA AHB_HPROT2_2_EN=2'b00, and descriptor DMA mode. All write transfers of a burst will be accessed by buffeable mode except for HW own update transfer. 2'b00: Dynamic control hprot_2 2'b01: hprot_2 = 0 2'b10: hprot_2 = 1
2	**LOCKDISABLE**	LOCK_DISABLE	**Disables lock to improve EMI efficiency** 1'b0: Enable AHB lock 1'b1: Disable AHB lock
1	**DSCPCSEN**	DMA_DSCP_CS_EN	**Enables DMA descriptor checksum** This bit is used to enable or disable the descriptor checksum validation function for the descriptor. This field cannot be modified

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Bit(s)	Mnemonic	Name	Description
			when the DMA status is 1.
0	DMASTS	DMA_STATUS	**DMA status** Indicates the status of DMA. 1'b0: DMA engine is inactive. 1'b1: DMA engine is active.

112300A0 **SW_DBG_SEL** **MSDC S/W Debug Selection Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SWDBGSEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	SWDBGSEL	DBG_SEL	**Selects MSDC debugging** Reserved.

112300A4 **SW_DBG_OUT** **MSDC S/W Debug Output Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SWDBGO[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SWDBGO[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	SWDBGO	DBG_OUT	**MSDC debugging output** 32-bit output selected by SW_DBG_SEL register

112300A8 **DMA_LENGTH** **DMA Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	XFSZ[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XFSZ[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	XFSZ	XFER_SIZE	**DMA total transfer size**

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Bit(s)	Mnemonic	Name	Description
			Specifies the number of DMA transfer byte required for the movement of source data through DMA. This field is only valid in basic DMA mode.

112300B0 PATCH_BIT0 MSDC Patch Bit Register 0 403C000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PTCH31	PTCH30	PTCH29	PTCH28	PTCH27	PTCH26	PTCH22				PTCH18				PTCH17	PTCH16
Type	RW	RW	RW	RW	RW	RW	RW				RW				RW	RW
Reset	0	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PTCH15	CKGDLYS					INTCKS			DESCUP			PTCH03	PTCH02	PTCH01	PTCH00
Type	RW	RW					RW			RW			RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0			1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**PTCH31**	EN_MMC_DRV_RESP	**Enables MSDC always driving bus when outputting wake-up response (BREAK)** 1'b0: Disable 1'b1: Enable
30	**PTCH30**	DETECT_WR_CRC_TIMEOUT	**Detects MSDC write data CRC phase time-out** 1'b0: Does not detect CRC phase timeout 1'b1: Detect CRC phase timeout
29	**PTCH29**	SPC_ALWAYS_PUSH	**SPC buffer push mechanism** 1'b0: Push the buffer only when read transfer is on-going 1'b1: Always push the buffer
28	**PTCH28**	SDIO_INT_DLY_SEL	**Selects SDIO interrupt latch time** 1'b0: Latch the data line value in internal SDIO interrupt period 1'b1: Latch the data line value in 1 clock delay of internal SDIO interrupt period
27	**PTCH27**	SDC_CMD_CMDFAIL_SEL	**Selects SDIO interrupt period recovery** 1'b0: SDIO interrupt period will re-start after a CMD12 or CMD52 command is issued 1'b1: SDIO interrupt period whenever DAT line is not busy
26	**PTCH26**	SDC_CMD_IDRT_SEL	**Selects SD identification response time** The register bit indicates if the command has a response with NID (i.e. 5 serial clock cycles as defined in SD memory card Specification Part 1 Physical Layer Specification version 1.0) response time. The register bit is valid only when the command has a response token. Thus, the register bit must be set to 1 for CMD2 (ALL_SEND_CID) and ACMD41 (SD_APP_OP_CMD). 1'b0: Otherwise 1'b1: The command has a response with NID response time.
25:22	**PTCH22**	SDC_CFG_WDOD	**SD write data output delay** The period from finish of the response for the initial host write command or the last write data block in a multiple block write operation to the start bit of the next write data block requires at least two serial clock cycles. The register field is used to extend the period (Write Data Output Delay) in unit of one serial clock. 4'b0000: No extension 4'b0001: Extend 1 more serial clock cycle 4'b0010: Extend 2 more serial clock cycles 4'b1111: Extend 15 more serial clock cycles

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Bit(s)	Mnemonic	Name	Description
21:18	**PTCH18**	SDC_CFG_BSYDLY	**SD R1B busy detection mode** Only valid for the commands with R1b response. If the command has a response of R1b type, MS/SD controller must monitor the data line 0 for card busy status from the bit time that is two serial clock cycles after the command end bit to check if operations in SD/MMC memory card are finished. The register field is used to expand the time between the command end bit and end of detection period to detect card busy status. If time is up and there is no card busy status on data line 0, the controller will abandon the detection. 4'b0000: No extension 4'b0001: Extend 1 more serial clock cycle 4'b0010: Extend 2 more serial clock cycles 4'b1111: Extend 15 more serial clock cycles
17	**PTCH17**	SDIO_CFG_INTC_SEL	**Selects SDIO interrupt model** 1'b0: When data line [1] = 0, trigger SDIO interrupt event. 1'b1: When data line [3:0] = 4'b1101, trigger SDIO interrupt event
16	**PTCH16**	MSDC_BLKNUM_SEL	**Supports ACMD23 reliable/force pro etc. features** 1'b0: Support ACMD23 reliable/force prog etc. feature 1'b1: Does not support ACMD23 reliable/force prog etc. feature
15	**PTCH15**	MSDC_FIFO_RD_DIS	**Disables MSDC RXFIFO read** 1'b0: Disable FIFO read permission to RXFIFO in PIO mode 1'b1: Enable FIFO read permission to RXFIFO in PIO mode
14:10	**CKGDLYS**	CKGEN_MSDC_DLY_SEL	**Selects CKBUF in CKGEN delay** Total 32 stages.
9:7	**INTCKS**	INT_DAT_LATCH_CK_SEL	**Selects internal MSDC clock phase** Total 8 stages, each stage can delay 1 clock period of msdc_src_ck.
6	**DESCUP**	DESC_UP_SEL	**SD transfer done interrupt should be issued when GPD are updated.** 1'b1: Enable new function to generate SD transfer done interrupt 1'b0: Use old function to generate SD transfer done interrupt
3	**PTCH03**	DIS_REFLECT	**Enables SD command register write monitor** 1'b0: Enable monitor function 1'b1: Disable monitor function
2	**PTCH02**	DIS_REFLECT_CMDWR_WHEN_BSY	**Enables SD command register write monitor** 1'b0: Enable monitor function 1'b1: Disable monitor function
1	**PTCH01**	EN_SDC_ODD_8BIT_SUP	**Enables SD odd number support for 8-bit data bus** 1'b0: Disable 1'b1: Enable
0	**PTCH00**	EN_SDC_ODD	**Enables SD odd number support for 8-bit data bus** 1'b0: Disable 1'b1: Enable

112300B4 PATCH_BIT1 MSDC Patch Bit Register 1 FFFE0009

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MSHBFCKEN	MRCTLCKEN	MWCTLCKEN	MSDCKEN	MACMDCKEN	MVOLDTCKEN	MPSCCKEN	MSPCCKEN	HGDMACKEN	AXIWRAPCKEN	DCMEN	DCMDIVSEL1	DCMDIVSEL2		FORCESTOP	SINGLEBURST
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESETGDMA		BIAS28R0	BIAS28R1	BIAS28R2				GETCRCMARGI	GETBUSYMAR	CMDTA			WRTA		

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									N	GIN						
Type	RW		RW	RW	RW				RW	RW	RW			RW		
Reset	0		0	0	0	0	0	0	0	0	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
31	**MSHBFCKEN**	MSDC_CK_SHBFF_CKEN	**msdc_src_ck clock enable bit for SHBFF** 1'b0: Disable 1'b1: Enable
30	**MRCTLCKEN**	MSDC_CK_RCTL_CKEN	**msdc_src_ck clock enable bit for RCTL** 1'b0: Disable 1'b1: Enable
29	**MWCTLCKEN**	MSDC_CK_WCTL_CKEN	**msdc_src_ck clock enable bit for WCTL** 1'b0: Disable 1'b1: Enable
28	**MSDCKEN**	MSDC_CK_SD_CKEN	**msdc_src_ck clock enable bit for SD** 1'b0: Disable 1'b1: Enable
27	**MACMDCKEN**	MSDC_CK_ACMD_CKEN	**msdc_src_ck clock enable bit for ACMD** 1'b0: Disable 1'b1: Enable
26	**MVOLDTCKEN**	MSDC_CK_VOLDET_CKEN	**msdc_src_ck clock enable bit for VOLDET** 1'b0: Disable 1'b1: Enable
25	**MPSCCKEN**	MSDC_CK_PSC_CKEN	**msdc_src_ck clock enable bit for PSC** 1'b0: Disable 1'b1: Enable
24	**MSPCCKEN**	MSDC_CK_SPC_CKEN	**msdc_src_ck clock enable bit forSPC** 1'b0: Disable 1'b1: Enable
23	**HGDMACKEN**	AHB_CK_GDMA_CKEN	**hclk_ck clock enable bit for GDMA** 1'b0: Disable 1'b1: Enable
22	**AXIWRAPCKEN**	AXI_WRAP_CKEN	**axi_ck and ahb_ck enable bit for AHB2AXI wrapper** This bit must be set to 1 when in DMA mode for eMMC50 spec, or this bit is reserverd. 1'b0: Disable 1'b1: Enable
21	**DCMEN**	DCM_EN	**Host enabling DCM for low power** When there is no transfer, ahb_ck and msdc_src_ck will be divided from source clk. 1'b1: Disable 1'b0: Enable
20	**DCMDIVSEL1**	DCM_DIV_SEL1	**For spec4.5 divider msdc_src_ck from source clk; for spec50 divider ahb_ck from source clk** 1'b1: 32 dividers from source clk 1'b0: 16 dividers from source clk
19:18	**DCMDIVSEL2**	DCM_DIV_SEL2	**Reserved for spec45** Only used for spec50. 2'b00: 64 dividers for msdc_src_ck from source clk 2'b01: 32 dividers for msdc_src_ck from source clk 2'b10: 16 dividers for msdc_src_ck from source clk 2'b11: 128 dividers for msdc_src_ck from source clk
17	**FORCESTOP**	FORCE_STOP_GDMA	**Forces state from WDMI_LAST_DATA to WDMI_IDLE with stop DMA bit** 1'b1: Enable stopping wdmi_cs when state hang in

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Bit(s)	Mnemonic	Name	Description
			WDMI_LAST_DATA with stop DMA bit 1'b0: Disable
16	**SINGLEBURST**	ENABLE_SINGLE_BURST	**AHB bus will not support incr1 burst type in the future and will only affect AHB bus MSDC design, not AXI bus design.** 1'b0: HW sends incr1 burst type. 1'b1: HW sends single burst type instead of incr1 type.
15	**RESETGDMA**	RESET_GDMA	**SW can reset GDMA when design hangs.** 1'b1: Reset GDMA 1'b0: Does not reset GDMA
13	**BIAS28R0**	BIAS_EXTBIAS_28NM	**28NM BIAS controller register 0**
12	**BIAS28R1**	BIAS_EN18IO_28NM	**28NM BIAS controller register 1**
11:8	**BIAS28R2**	BIAS_TUNE_28NM	**28NM BIAS controller register 2**
7	**GETCRCMARGIN**	GET_CRC_MARGIN	**Adds margin to get CRC status when card resp CRC does not match spec 2 cycle from endbit** 1'b0: 8 cycles reserved for getting CRC status from write data CRC endbit 1'b1: 16 cycles reserved for getting CRC status from write data CRC endbit
6	**GETBUSYMARGIN**	GET_BUSY_MARGIN	**Adds margin for getting busy state of data0** 1'b0: 1 cycle reserved for getting busy state from SRC status endbit 1'b1: 3 cycles reserved for getting busy state from SRC status endbit
5:3	**CMDTA**	CMD_RSP_TA_CNTR	**CMD response turn-around period** Turn-around cycle = CMD_RSP_TA_CNTR + 2 In USH104 mode, this register should be set to 1. In non-UHS104 mode, this register should be set to 0.
2:0	**WRTA**	WRDAT_CRCS_TA_CNTR	**Write data and CRC status turn-around period** Turn-around cycle = WRDAT_CRCS_TA_CNTR + 2 In USH104 mode, this register should be set to 1. In non-UHS104 mode, this register should be set to 0.

112300B8 <u>PATCH_BIT2</u> MSDC Patch Bit Register 2 — 14801801

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CRCSTSENSEL**			**CFGCRCSTS**	**CFGCRCSTSCNT**		**CFGCRCSTSEDGE**	**CFG_CRCSTS_SEL**	**POPENCNT**					**RESPSTSENSEL**		
Type	RW			RW	RW		RW	RW	RW					RW		
Reset	0	0	0	1	0	1	0	0	1	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CFGRESP**	**CFGRESPCNT**			**INTCRESPSEL**		**CFGRDAT**	**CFGRDATCNT**					**RESPWAITCNT**		**SUPPORT64G**	**ENHANCEGPD**
Type	RW	RW			RW		RW	RW					RW		RW	RW
Reset	0	0	0	1	1		0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:29	**CRCSTSENSEL**	CRCSTS_LATCH_EN_SEL	**Configures latch CRC status enable signal for async FIFO in eMMC45** 3'b000: Latch CRC status enable signal does not delay. 3'b001: Latch CRC status enable signal delays 1T msdc_ck. 3'b010: Latch CRC status enable signal delays 2T msdc_ck.

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Bit(s)	Mnemonic	Name	Description
			3'b011: Latch CRC status enable signal delays 3T msdc_ck. 3'b111: Latch CRC status enable signal delays 7T msdc_ck.
28	**CFGCRCSTS**	CFG_CRCSTS	**Configures CRC status path selection** The setting only uses eMMC4.5 feature. 1'b0: Latch CRC status select delay-line path 1'b1: Latch CRC status select async FIFO path
27:26	**CFGCRCSTSCNT**	CFG_CRCSTS_CNT	**Configures how many data are pushed in async FIFO before starting to pop out data from async FIFO** The min. register setting is 1. Do not set it to 0. The setting only uses eMMC4.5 feature. 2'b00: Push 0 data in async FIFO when starting to pop out data from async FIFO 2'b01: Push 1 data in async FIFO when starting to pop out data from async FIFO 2'b10: Push 2 data in async FIFO when starting to pop out data from async FIFO 2'b11: Push 3 data in async FIFO when starting to pop out data from async FIFO
25	**CFGCRCSTSEDGE**	CFG_CRCSTS_EDGE	**Uses rising async FIFO or falling async FIFO** 1'b0: Async FIFO latch CRC status uses rising async FIFO. 1'b1: Async fifo latch CRC status uses falling async FIFO.
24		CFG_CRCSTS_SEL	**Configures async FIFO path selection** 1'b0: Used normal path in async FIFO 1'b1: Use 2DFF path in async FIFO
23:20	**POPENCNT**	POP_EN_CNT	**Pop enable counter** Defines how many write pointer and read pointer margin begin to pop up data transfer.
18:16	**RESPSTSENSEL**	RESP_LATCH_EN_SEL	**Configures latch CMD response enable signal for async FIFO in eMMC45** 3'b000: Latch CMD response enable signal does not delay. 3'b001: Latch CMD response enable signal delays 1T msdc_ck. 3'b010: Latch CMD response enable signal delays 2T msdc_ck. 3'b011: Latch CMD response enable signal delays 3T msdc_ck. 3'b111: Latch CMD response enable signal delays 7T msdc_ck.
15	**CFGRESP**	CFG_RESP	**Configures CMD response path selection** The setting only used eMMC4.5 feature. 1'b0: Latch CMD response selects async FIFO path. 1'b1: Latch CMD response selects delay-line path.
14:12	**CFGRESPCNT**	CFG_RESP_CNT	**Configures how many data are pushed in async FIFO before starting to pop out data from async FIFO** The min. register setting is 1. Do not set it to 0. The setting only uses eMMC4.5 feature. 3'b000: Push 0 data in async FIFO when starting to pop out data from async FIFO 3'b001: Push 1 data in async FIFO when starting to pop out data from async FIFO 3'b111: Push 7 data in async FIFO when starting to pop out data from async FIFO.
11	**INTCRESPSEL**	INTC_RESP_SEL	**Configures BREAK command async FIFO path** 1'b0: Use normal path in async FIFO 1'b1: Use 2DFF path in async FIFO
9	**CFGRDAT**	CFG_RDAT	**Configures read data path** 1'b0: Read data path bypasses delay line. 1'b1: Read data path through delay line
8:4	**CFGRDATCNT**	CFG_RDAT_CNT	**Configures read data path delay line**

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Bit(s)	Mnemonic	Name	Description
3:2	**RESPWAITCNT**	RESP_WAIT_CNT	**Configures CMD response timeout** The timeout cycle is 65T+16*RESP_WAIT_CNT. 2'b00: CMD response timeout is 65T. 2'b01: CMD response timeout is 65T+ 16*1T. 2'b01: CMD response timeout is 65T+ 16*2T. 2'b01: CMD response timeout is 65T+ 16*3T.
1	**SUPPORT64G**	SUPPORT_64G	**Indicates which project supports high 64G DRAM space access** 1'b1: Support 64G DRAM access 1'b0: Does not support 64G DRAM access
0	**ENHANCEGPD**	ENHANCE_WAIT_GPD	**If SW clears int when GPD update has not been finished, the design will hang.** Set this bt to 1 to avoid such iuuse in enhance write mode. 1'b1: Use new HW code to update GPD in enhance mode 1'b0: Use old HW code

112300F0 **PAD_TUNE0** **MSDC Pad Tuning Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CLKTDLY					CMDRRDLY						CMDRDLY				
Type	RW					RW						RW				
Reset	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DATRRDLY					DELAYEN			DATWRDLY				
Type				RW					RW			RW				
Reset				0	0	0	0	0	0			0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:27	**CLKTDLY**	PAD_CLK_TXDLY	**Controls CLK pad TX delay** This register adds delay to CLK phase. Total 32 stages.
26:22	**CMDRRDLY**	PAD_CMD_RESP_RXDLY	**Controls CMD response internal delay line** This register fine-tunes response phase latched by MSDC internal clock. Total 32 stages.
20:16	**CMDRDLY**	PAD_CMD_RXDLY	**Controls CMD pad RX delay line** This register fine-tunes CMD pad macro response latch timing. Total 32 stages.
12:8	**DATRRDLY**	PAD_DAT_RD_RXDLY	**Controls DAT pad RX delay line (for MSDC read only)** This register fine-tunes DAT pad macro read data latch timing. Total 32 stages.
7	**DELAYEN**	DELAY_EN	**Enables all delay cell toggle when power is on** 1'b0: Disable delay cell toggle default 1'b1: Enable delay cell toggle default
4:0	**DATWRDLY**	PAD_DAT_WR_RXDLY	**Controls write data status internal delay line** This register fine-tunes write status phase latched by MSDC internal clock. Total 32 stages.

112300F8 **DAT_RD_DLY0** **MSDC Data Delay Line Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT0RDDLY								DAT1RDDLY				

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Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DAT2RDDLY								DAT3RDDLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	**DAT0RDDLY**	DAT0_RD_DLY	**Controls DAT0 pad RX delay line (for MSDC RD)** Total 32 stages.
20:16	**DAT1RDDLY**	DAT1_RD_DLY	**Controls DAT1 pad RX delay line (for MSDC RD)** Total 32 stages.
12:8	**DAT2RDDLY**	DAT2_RD_DLY	**Controls DAT2 pad RX delay line (for MSDC RD)** Total 32 stages.
4:0	**DAT3RDDLY**	DAT3_RD_DLY	**Controls DAT3 pad RX delay line (for MSDC RD)** Total 32 stages.

112300FC <u>DAT_RD_DLY1</u> MSDC Data Delay Line Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT4RDDLY								DAT5RDDLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DAT6RDDLY								DAT7RDDLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	**DAT4RDDLY**	DAT4_RD_DLY	**Controls DAT4 pad RX delay line (for MSDC RD)** Total 32 stages.
20:16	**DAT5RDDLY**	DAT5_RD_DLY	**Controls DAT5 pad RX delay line (for MSDC RD)** Total 32 stages.
12:8	**DAT6RDDLY**	DAT6_RD_DLY	**Controls DAT6 pad RX delay line (for MSDC RD)** Total 32 stages.
4:0	**DAT7RDDLY**	DAT7_RD_DLY	**Controls DAT7 pad RX delay line (for MSDC RD)** Total 32 stages.

11230110 <u>HW_DBG_SEL</u> MSDC H/W Debug Selection Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DBGWSEL	DBG3SEL						DBG2SEL							
Type		RW	RW						RW							
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DBG1SEL						DBG0SEL							
Type			RW						RW							
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
30	**DBGWSEL**	HW_DBG_WRAP_SEL	**Selects HW debug output for wrapper** 0: Select original debug pins 1: Select wrapper debug pins
29:24	**DBG3SEL**	HW_DBG3_SEL	**Selects HW debug output**
23:16	**DBG2SEL**	HW_DBG2_SEL	**Selects HW debug output**
13:8	**DBG1SEL**	HW_DBG1_SEL	**Selects HW debug output**
7:0	**DBG0SEL**	HW_DBG0_SEL	**Selects HW debug output**

11230114 MAIN_VER MSDC Main Version Register 20140512

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAINVER[31:16]															
Type	RO															
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAINVER[15:0]															
Type	RO															
Reset	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
31:0	**MAINVER**	MAIN_VER	Main version

11230118 ECO_VER MSDC ECO Version Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ECOVER[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ECOVER[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ECOVER**	ECO_VER	ECO version

11230180 EMMC50_PAD_CTL0 MSDC eMMC5.0 CLK Pad Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							DLN1		DLP1		DLN0		DLP0		HLSEL	DCCSEL
Type							RW		RW		RW		RW		RW	RW
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
9:8	**DLN1**	DLN1	**Gear to tune low duty cycle for the first duty cycle corrector** Four gears from 00 to 11
7:6	**DLP1**	DLP1	**Gear to tune high duty cycle for the second duty cycle corrector** Four gears from 00 to 11
5:4	**DLN0**	DLN0	**Gear to tune low duty cycle for the first duty cycle corrector** Four gears from 00 to 11
3:2	**DLP0**	DLP0	**Gear to tune high duty cycle for the second duty cycle corrector** Four gears from 00 to 11
1	**HLSEL**	HL_SEL	**Decides to tune low or high duty cycle** 1'b0: Tune high duty cycle 1'b1: Tune low duty cycle
0	**DCCSEL**	DCC_SEL	**Decides SCLK to pass through duty cycle corrector or not** 1'b0: Does not pass 1'b1: Pass

11230184 **EMMC50_PAD_DS_CTL0** **MSDC eMMC5.0 DS Pad Control Register 0** **0000001C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														DSDRV		
Type														RW		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DSTDSEL				DSRDSEL						DSSMT	DSIES	DSPUPD	DSR1	DSR0	DSSR
Type	RW				RW						RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0

Bit(s)	Mnemonic	Name	Description
18:16	**DSDRV**	PAD_DS_DRV	**Controls DS pad driving strength**
15:12	**DSTDSEL**	PAD_DS_TDSEL	**Selects DS pad TX duty**
11:6	**DSRDSEL**	PAD_DS_RDSEL	**Selects DS pad RX duty**
5	**DSSMT**	PAD_DS_SMT	**Enables DS pad RX input buffer Schmitt trigger hysteresis control** High asserted. SMT=1: Enable Schmitt trigger
4	**DSIES**	PAD_DS_IES	**Enables DS pad RX input buffer** High asserted. Data path from IO to O. 1'b0: Disable input buffer 1'b1: Enable input buffer
3	**DSPUPD**	PAD_DS_PUPD	**Controls DS pad pull-up/pull-down** 0: Pull-up 1: Pull-down
2	**DSR1**	PAD_DS_R1	**Controls DS pad 50K resistor**
1	**DSR0**	PAD_DS_R0	**Controls DS pad 10K resistor**
0	**DSSR**	PAD_DS_SR	**Controls DS pad output slew rate** High asserted. 1'b0: No slew rate control 1'b1: Slower slew

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11230188 **EMMC50_PAD_DS_TUNE** **MSDC eMMC5.0 DS Pad Tuning Register** **00014015**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																PAD_DS_DLY3[4:4]
Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAD_DS_DLY3[3:0]				PAD_DS_DLY2					DSDLY1					DSDLY2SEL	DSDLYSEL
Type	RW				RW					RW					RW	RW
Reset	0	1	0	0	0	0	0	0	0	0	0	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
16:12		PAD_DS_DLY3	**Gear of the second delay line for DS for input data latch in data pad macro** 32 gears from 0 to 31
11:7		PAD_DS_DLY2	**Gear of the second delay line for DS for input data latch in data pad macro** 32 gears from 0 to 31
6:2	**DSDLY1**	PAD_DS_DLY1	**Gear of the first delay line for DS for input data latch in data pad macro** 32 gears from 0 to 31
1	**DSDLY2SEL**	PAD_DS_DLY2_SEL	**Selects if DS passes through second delay macro** 1'b0: Does not pass 1'b1: Pass
0	**DSDLYSEL**	PAD_DS_DLY_SEL	**Selects if DS passes through delay macro** 1'b0: Does not pass 1'b1: Pass

1123018C **EMMC50_PAD_CMD_TUNE** **MSDC eMMC5.0 CMD Pad Tuning Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						CMDTXDLY					CMDRXDLY3					CMDRXDLY3MUXSEL
Type						RW					RW					RW
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
10:6	**CMDTXDLY**	PAD_CMD_TX_DLY	**Gear of delay line for TX data** 32 gears from 0 to 31
5:1	**CMDRXDL**	PAD_CMD_RX_D	**Gear of delay line for RX data**

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Bit(s)	Mnemonic	Name	Description
	Y3	LY3	32 gears from 0 to 31
0	CMDRXDLY3MUXSEL	PAD_CMD_RX_DLY3_MUX_SEL	**Selects if input data pass through delay line** 1'b0: Does not pass 1'b1: Pass

11230190 EMMC50_PAD_DAT01_TUNE MSDC eMMC5.0 DAT0/1 Pad Tuning Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						DAT1TXDLY					DAT1RXDLY3					DAT1RXDLY3MUXSEL
Type						RW					RW					RW
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DAT0TXDLY					DAT0RXDLY3					DAT0RXDLY3MUXSEL
Type						RW					RW					RW
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26:22	DAT1TXDLY	PAD_DAT1_TX_DLY	**Gear of delay line for TX data** 32 gears from 0 to 31
21:17	DAT1RXDLY3	PAD_DAT1_RX_DLY3	**Gear of delay line for RX data** 32 gears from 0 to 31
16	DAT1RXDLY3MUXSEL	PAD_DAT1_RX_DLY3_MUX_SEL	**Selects if input data pass through delay line** 1'b0: Does not pass 1'b1: Pass
10:6	DAT0TXDLY	PAD_DAT0_TX_DLY	**Gear of delay line for TX data** 32 gears from 0 to 31
5:1	DAT0RXDLY3	PAD_DAT0_RX_DLY3	**Gear of delay line for RX data** 32 gears from 0 to 31
0	DAT0RXDLY3MUXSEL	PAD_DAT0_RX_DLY3_MUX_SEL	**Selects if input data pass through delay line** 1'b0: Does not pass 1'b1: Pass

11230194 EMMC50_PAD_DAT23_TUNE MSDC eMMC5.0 DAT2/3 Pad Tuning Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						DAT3TXDLY					DAT3RXDLY3					DAT3RXDLY3MUXSEL
Type						RW					RW					RW
Reset						0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DAT2TXDLY					DAT2RXDLY3					DAT2RXDLY3MUXSEL
Type						RW					RW					RW
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26:22	**DAT3TXDLY**	PAD_DAT3_TX_DLY	**Gear of delay line for TX data** 32 gears from 0 to 31
21:17	**DAT3RXDLY3**	PAD_DAT3_RX_DLY3	**Gear of delay line for RX data** 32 gears from 0 to 31
16	**DAT3RXDLY3MUXSEL**	PAD_DAT3_RX_DLY3_MUX_SEL	**Selects if input data pass through delay line** 1'b0: Does not pass 1'b1: Pass
10:6	**DAT2TXDLY**	PAD_DAT2_TX_DLY	**Gear of delay line for TX data** 32 gears from 0 to 31
5:1	**DAT2RXDLY3**	PAD_DAT2_RX_DLY3	**Gear of delay line for RX data** 32 gears from 0 to 31
0	**DAT2RXDLY3MUXSEL**	PAD_DAT2_RX_DLY3_MUX_SEL	**Selects if input data pass through delay line** 1'b0: Does not pass 1'b1: Pass

11230198 **EMMC50_PAD_DAT45_TUNE** **MSDC eMMC5.0 DAT4/5 Pad Tuning Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						DAT5TXDLY					DAT5RXDLY3					DAT5RXDLY3MUXSEL
Type						RW					RW					RW
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DAT4TXDLY					DAT4RXDLY3					DAT4RXDLY3MUXSEL
Type						RW					RW					RW
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26:22	**DAT5TXDLY**	PAD_DAT5_TX_DLY	**Gear of delay line for TX data** 32 gears from 0 to 31
21:17	**DAT5RXDLY3**	PAD_DAT5_RX_DLY3	**Gear of delay line for RX data** 32 gears from 0 to 31
16	**DAT5RXDLY3MUXSEL**	PAD_DAT5_RX_DLY3_MUX_SEL	**Selects if input data pass through delay line** 1'b0: Does not pass 1'b1: Pass
10:6	**DAT4TXDL**	PAD_DAT4_TX_D	**Gear of delay line for TX data**

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Bit(s)	Mnemonic	Name	Description
	Y	LY	32 gears from 0 to 31
5:1	**DAT4RXDLY3**	PAD_DAT4_RX_DLY3	**Gear of delay line for RX data** 32 gears from 0 to 31
0	**DAT4RXDLY3MUXSEL**	PAD_DAT4_RX_DLY3_MUX_SEL	**Selects if input data pass through delay line** 1'b0: Does not pass 1'b1: Pass

1123019C **EMMC50_PAD_DAT67_TUNE** **MSDC eMMC5.0 DAT6/7 Pad Tuning Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						DAT7TXDLY					DAT7RXDLY3					DAT7RXDLY3MUXSEL
Type						RW					RW					RW
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DAT6TXDLY					DAT6RXDLY3					DAT6RXDLY3MUXSEL
Type						RW					RW					RW
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26:22	**DAT7TXDLY**	PAD_DAT7_TX_DLY	**Gear of delay line for TX data** 32 gears from 0 to 31
21:17	**DAT7RXDLY3**	PAD_DAT7_RX_DLY3	**Gear of delay line for RX data** 32 gears from 0 to 31
16	**DAT7RXDLY3MUXSEL**	PAD_DAT7_RX_DLY3_MUX_SEL	**Selects if input data pass through delay line** 1'b0: Does not pass 1'b1: Pass
10:6	**DAT6TXDLY**	PAD_DAT6_TX_DLY	**Gear of delay line for TX data** 32 gears from 0 to 31
5:1	**DAT6RXDLY3**	PAD_DAT6_RX_DLY3	**Gear of delay line for RX data** 32 gears from 0 to 31
0	**DAT6RXDLY3MUXSEL**	PAD_DAT6_RX_DLY3_MUX_SEL	**Selects if input data pass through delay line** 1'b0: Does not pass 1'b1: Pass

11230204 **EMMC51_CFG0** **eMMC51 Configuration Register 0** **000350D4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CMDQCMDEN	RDATCNT[9:5]				
Type											RW	RW				
Reset											0	0	0	0	1	1

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDATCNT[4:0]					WDATCNT										CMDQEN
Type	RW					RW										RW
Reset	0	1	0	1	0	0	0	0	1	1	0	1	0	1	0	0

Bit(s)	Mnemonic	Name	Description
21	CMDQCMDEN	CMDQ_CMD_ENABLE	**Configures CMD queue enable type** 1'b0: Enable CMD queue for CMD13, CMD44 and CMD45 1'b1: Enable CMD queue for all CMD
20:11	RDATCNT	RDAT_CNT	**Read data counter threshold for CMD queue**
10:1	WDATCNT	WDAT_CNT	**Write data counter threshold for CMD queue**
0	CMDQEN	CMDQ_EN	**Enables CMD queue**

11230208 **EMMC50_CFG0** **eMMC50 Configuration Register0** **02E889E2**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			TXSKEWSEL	RDVALIDSEL	WRVALIDSEL	MSDCRDVALID	MSDCWRVALID	EMMC50MONSEL	READDATCNT			ENDBITCNT[9:5]				
Type			RW	RW	RW	RU	RU	RW	RW			RW				
Reset			0	0	0	0	1	0	1	1	1	0	1	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ENDBITCNT[4:0]					CMDEDGESEL	CMDRESPSEL	END_BITCHKCNT				CRCSTSSEL	CRCSTSEDGE	CRCSTSCNT		PADLATCK
Type	RW					RW	RW	RW				RW	RW	RW		RW
Reset	1	0	0	0	1	0	0	1	1	1	1	0	0	0	1	0

Bit(s)	Mnemonic	Name	Description
29	TXSKEWSEL	MSDC_TXSKEW_SEL	1'b0: clk/cmd/data output is not through DFF in HS400 mode. 1'b1: clk/cmd/data output is through DFF in HS400 mode.
28	RDVALIDSEL	MSDC_RD_VALID_SEL	
27	WRVALIDSEL	MSDC_WR_VALID_SEL	
26	MSDCRDVALID	MSDC_RD_VALID	**According to eMMC50 spec, the host cannot stop pad clk in one block transfer, so it must have the whole block len data in FIFO when it is to transfer data to device.** 1'b0: SD FIFO is not valid to read for writing device. 1'b1: SD FIFO is valid to read for writing device .
25	MSDCWRVALID	MSDC_WR_VALID	**According to eMMC50 spec, the host cannot stop pad clk in one block transfer, so it must have enough space to store a block len data read from device.** 0: SD FIFO is not valid for reading data from device. 1: SD FIFO is valid for reading data from device.
24	EMMC50MONSEL	EMMC50_MON_SEL	**Set to 1 to debug eMMC50 signals** 0: Choose eMMC50 debugging signals to debug pin 1: Does not choose eMMC50 debugging signals to debug pins
23:21	READDATCNT	READ_DAT_CNT	**Sets up to latch how many data in RCLK domain switch pop condition**
20:11	ENDBITCNT	ENDBIT_CNT	**Sets up endbit check value in RCLK domain**

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Bit(s)	Mnemonic	Name	Description
10	CMDEDGESEL	CMD_EDGE_SEL	**Selects CMD response edge** 1'b0: CMD response from RCLK rising edge latch 1'b1: CMD response from RCLK falling edge latch
9	CMDRESPSEL	CMD_RESP_SEL	**Selects CMD response output** 1'b0: CMD responds from delay line; same as eMMC4.5 spec design. 1'b1: CMD responds from FIFO; design for eMMC5.0 spec.
8:5	END_BITCHKCNT	END_BIT_CHK_CNT	**Sets up how many cycles to check device busy status after CRC status**
4	CRCSTSSEL	CRC_STS_SEL	**Selects CRC status output** 1'b0: CRC status data from 2-DFF eMMC5.0 is used.(old design) 1'b1: Use CRC status data from FIFO in eMMC5.0.(new design)
3	CRCSTSEDGE	CRC_STS_EDGE	**In HS400 mode, select CRC status** dat psh 1'b0: In HS400 mode, select rising edge CRC status data psh. 1'b1: In HS400 mode, select falling edge CRC status data psh.
2:1	CRCSTSCNT	CRC_STS_CNT	
0	PADLATCK	PAD_CMD_LATCH_CK	**Selects PAD CMD latch clock in HS400 mode** 1'b0: Select internal clock as pad CMD latch clock in HS400 mode 1'b1: Select DS (RCLK) as pad CMD latch clock in HS400 mode

1123020C **EMMC50_CFG1** **eMMC50 Configuration Register 1** **0100070C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reserve0			DSCFG	PSHPSSEL	PSHCNT			EMMC50DEBUGSEL							
Type	RW			RW	RW	RW			RW							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAIT8CLKCNT				RDATSTOP	CKSWITCHCNT			WRPTRMARGIN							
Type	RW				RW	RW			RW							
Reset	0	0	0	0	0	1	1	1	0	0	0	0	1	1	0	0

Bit(s)	Mnemonic	Name	Description
31:29		reserve0	**Reserved for backup2**
28	DSCFG	DS_CFG	**Defines whether to mask redundant DS clock** 1'b0: Mask redundant DS clock 1'b1: Does not mask redundant DS clock
27	PSHPSSEL	PSH_PS_SEL	**Defines using rising or falling edge to push pulse** 1'b0: Select rising edge pulse 1'b1: Select falling edge pulse
26:24	PSHCNT	PSH_CNT	**Defines how many push cnt to start sync pop pulse to pop data**
23:16	EMMC50DEBUGSEL	EMMC50_DEBUG_SEL	**Selects eMMC50 debug signal out**
15:12	WAIT8CLKCNT	WAIT_8_CLK_CNT	**Configures 8 clock counters**
11	RDATSTOP	RD_DAT_STOP	**Selects eMMC50 read data stop signals** 1'b0: Select rising signal 1'b1: Select falling signal

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Bit(s)	Mnemonic	Name	Description
10:8	**CKSWITCHCNT**	LATCH_CK_SWITCH_CNT	**After CRC status, sets up latch clock switch counter**
7:0	**WRPTRMARGIN**	WR_PTR_MARGIN	Write pointer margin

1123021C **EMMC50_CFG2** **AHB2AXI Wrapper Control Register** **0F0C0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**AXIBUSY**	**RESPERRTYPE**		**SETLEN**				**RDOUTSTANDINGNUM**					**BOUND4K**	**BOUND2K**	**BOUND1K**
Type		RO	RO		RW				RW					RW	RW	RW
Reset		0	0	0	1	1	1	1	0	0	0	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BOUND512B**	**BOUND256B**	**BOUND128B**					**SHAREENRDEMI**	**IOMMURDEMI**	**reserved1**				**SHAREENWREMI**	**IOMMUWREMI**	
Type	RW	RW	RW					RW	RW	RW				RW	RW	
Reset	0	0	0					0	0	0	0	0	0	0	0	

Bit(s)	Mnemonic	Name	Description
30	**AXIBUSY**	AXI_BUSY	**Checks if AXI bus is busy or idle** 1'b1: AXI wrapper is busy. 1'b0: AXI wrapper is idle.
29:28	**RESPERRTYPE**	AXI_RESP_ERR_TYPE	**When SW gets AXI response error interrupt, check this bit to know which type of error occurs.** 2'b00: No error 2'b01: Do not care 2'b10: Slave error 2'b11: Decoding error
27:24	**SETLEN**	AXI_SET_LEN	**SW programs this bit to set up the transfer number in one AXI burst both for read and write.** For better performance, this bits can be set up to f 4'b0000: 1 beat per burst 4'b0001: 2 beats per burst 4'b0010: 3 beats per burst 4'b1111: 16 beats per burst
23:19	**RDOUTSTANDINGNUM**	AXI_RD_OUTSTANDING_NUM	**AXI supports outstanding transfer, i.e. when there is no response, you can still send AXI CMD.** For better performance, SW cannot set this bit up to 13, 5'b: 00001: Support 1 outstanding 5'b: 00002: Support 2 outstandings 5'b: 00003: Support 3 outstandings 5'b: 01011: Support 13 outstandings
18	**BOUND4K**	AXI_BOUND_4K	**Default: 4K in AXI spec** 1'b1: Choose 4K boundary 1'b0: Does not choose 4K boundary
17	**BOUND2K**	AXI_BOUND_2K	**For future project option** 1'b1: Choose 2K boundary 1'b0: Does not choose 2K boundary
16	**BOUND1K**	AXI_BOUND_1K	**For future project option** 1'b1: Choose 42K boundary 1'b0: Does not chose 1K boundary
15	**BOUND512**	AXI_BOUND_512B	**For future project option**

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Bit(s)	Mnemonic	Name	Description
	B		1'b1: Choose 512B boundary 1'b0: Does not choose 512B boundary
14	**BOUND256B**	AXI_BOUND_256B	**For future project option** 1'b1: Chose 256B boundary 1'b0: Does not choose 256B boundary
13	**BOUND128B**	AXI_BOUND_128B	**For future project option** 1'b1: Choose 128B boundary 1'b0: Does not choose 128B boundary
8	**SHAREENRDEMI**	AXI_SHARE_EN_RD_EMI	1'b1: Enable share 1'b0: Does not enable share
7	**IOMMURDEMI**	AXI_IOMMU_RD_EMI	1'b1: Through IOMMU 1'b0: Not through IOMMU
2	**SHAREENWREMI**	AXI_SHARE_EN_WR_EMI	1'b1: Enable share 1'b0: Does not enable share
1	**IOMMUWREMI**	AXI_IOMMU_WR_EMI	1'b1: Through IOMMU 1'b0: Not through IOMMU

11230220 **EMMC50_CFG3** **0F28A3C1**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**reserved2**			**PREULTRASETRD**						**ULTRASETRD**						**PREULTRASETWR[5:5]**
Type	RO			RW						RW						RW
Reset	0	0	0	0	1	1	1	1	0	0	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**PREULTRASETWR[4:0]**					**ULTRASETWR**						**OUTSTANDINGWR**				
Type	RW					RW						RW				
Reset	1	0	1	0	0	0	1	1	1	1	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
28:23	**PREULTRASETRD**	PREULTRA_SET_RD	**MSDC GDMA has higher priority when this bit is set to bigger value.**
22:17	**ULTRASETRD**	ULTRA_SET_RD	**MSDC GDMA has higher priority when this bit is set to bigger value.**
16:11	**PREULTRASETWR**	PREULTRA_SET_WR	**MSDC GDMA has higher priority when this bit is set to smaller value.**
10:5	**ULTRASETWR**	ULTRA_SET_WR	**MSDC GDMA has higher priority when this bit is set to smaller value.**
4:0	**OUTSTANDINGWR**	OUT_STANDING_WR	**AXI supports outstanding transfer, i.e. when there is no response, you can still send AXI CMD.** For better performance, SW cannot set this bit up to 13,

11230224 **EMMC50_CFG4** **0001281E**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**reserved3**									**WRAP_SEL**					**ULTRAEN**	
Type	RO									RW					RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IMPRULTRASETRD								IMPRULTRASETWR							
Type	RW								RW							
Reset	0	0	1	0	1	0	0	0	0	0	0	1	1	1	1	0

Bit(s)	Mnemonic	Name	Description
22:18	**WRAP_SEL**	WRAP_SEL	**For HW sel debug signal**
17:16	**ULTRAEN**	ULTRA_EN	**Cannot be set to high priority because it reduces performance of other modules.** 2'b00: Lowest priority 2'b01: Lower priority 2'b10: Middle priority 2'b11: High priority
15:8	**IMPRULTRASETRD**	IMPR_ULTRA_SET_RD	**MSDC GDMA has higher priority when this bit is set to bigger value.** The host can improve priority when ULTRA_SET_RD is set.
7:0	**IMPRULTRASETWR**	IMPR_ULTRA_SET_WR	**MSDC GDMA has higher priority when this bit is set to smaller value.** The host can improve priority when ULTRA_SET_WR is set.

11230228 **EMMC50_BLOCK_LENGTH** **00000080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								BLOCKLENGTH								
Type								RW								
Reset								0	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0	**BLOCKLENGTH**	EMMC50_BLOCK_LENGTH	**SW sets up the FIFO water level for stop clk in diff block length.** If the device block length is 512B, set this register to 9'd128. If the device block length is 256B, set this register to 9'd64. If the device block length is 128B, set this register to 9'd32. If the device block length is 64B, set this register to 9'd16. If the device block length is 32B, set this register to 9'd8. This register is used for SDIO30+. For other specs, use the default value.

Module name: MSDC1 Base address: (+11240000h)

Address	Name	Width	Register Function
11240000	MSDC_CFG	32	**MSDC Configuration Register** For general configuration of the MS/SD controller
11240004	MSDC_IOCON	32	**MSDC IO Configuration Register** Contains the receiver path data latch timing control and interface control bits
11240008	MSDC_PS	32	**MSDC Pin Status Register** Stores card detection and write protection pin status. Card

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Address	Name	Width	Register Function
			detection status can be disabled.
1124000C	**MSDC_INT**	32	**MSDC Interrupt Register** Contains the status of interrupts Note: The register still shows the status of interrupt even though the interrupt is disabled.
11240010	**MSDC_INTEN**	32	**MSDC Interrupt Enable Register** Contains related enabling bit of interrupts
11240014	**MSDC_FIFOCS**	32	**MSDC FIFO Control and Status Register** Contains control and status of embedded 128B FIFO
11240018	**MSDC_TXDATA**	32	**MSDC TX Data Port Register** For PIO mode only. Used to input MSDC write data to card. The access can be AHB1B/2B/4B.
1124001C	**MSDC_RXDATA**	32	**MSDC RX Data Port Register** For PIO mode only. Used to read back MSDC read data from card. The access can be AHB1B/2B/4B.
11240030	**SDC_CFG**	32	**SD Configuration Register** Configures MS/SD memory card controller when it is configured as the host of SD memory card. If the controller is configured as the host of memory stick, the contents of the register will have no impact on the operation of the controller.
11240034	**SDC_CMD**	32	**SD Command Register** Defines a SD memory card command and its attributes. Before MS/SD controller issues a transaction onto SD bus, the application should specify other relative settings such as argument for command. After writing the register by the application, MS/SD controller will issue the corresponding transaction onto SD serial bus. If the command is GO_IDLE_STATE, the controller will have serial clock on SD/MMC bus running 128 cycles before issuing the command.
11240038	**SDC_ARG**	32	**SD Argument Register** Contains argument of SD/MMC memory card command
1124003C	**SDC_STS**	32	**SD Status Register** Reflects SD bus status and contains MMC stream write status
11240040	**SDC_RESP0**	32	**SD Response Register 0** Contains parts of the last SD/MMC memory card bus response. See description in register field SDC_RESP3.
11240044	**SDC_RESP1**	32	**SD Response Register 1** Contains parts of the last SD/MMC memory card bus response. See description in register field SDC_RESP3.
11240048	**SDC_RESP2**	32	**SD Response Register 2** Contains parts of the last SD/MMC memory card bus response. See description in register field SDC_RESP3.
1124004C	**SDC_RESP3**	32	**SD Response Register 3** Contains parts of the last SD/MMC memory card bus response. Register fields SDC_RESP0, SDC_RESP1, SDC_RESP2 and SDC_RESP3 are composed of the last SD/MMC memory card bus response. For response of type R2, i.e. response of the command ALL_SEND_CID, SEND_CSD and SEND_CID, only bit 127 to 0 of response token are stored in register field SDC_RESP0, SDC_RESP1, SDC_RESP2 and SDC_RESP3. SDC_RESP0 = bit 31~0 SDC_RESP1 = bit 63~32 SDC_RESP2 = bit 95~64 SDC_RESP3 = bit 127~96 For response of type R1b in auto CMD12 or R1 in auto CMD23, bit 39 to 8 of response token are stored in register field of SDC_RESP3. For the responses of other types, only bit 39 to 8 of response token are stored in the register field SDC_RESP0.

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Address	Name	Width	Register Function
11240050	SDC_BLK_NUM	32	**SD Block Number Register** Defines block number for block transaction. For single read/write, this register should be set to 1. For multiple read/write, this register should be set to bigger than 1. Set to 0 will cause unexpected result.
11240054	SDC_VOL_CHG	32	**SD Voltage Change Wait Time Register** Defines SD voltage change check wait time.
11240058	SDC_CSTS	32	**SD Card Status Register** After commands with R1 and R1b response, this register will contain the status of the SD/MMC card.
1124005C	SDC_CSTS_EN	32	**SD Card Status Enable Register** Controls which bit of SDC_CSTS will generate the MSDC_INT.SD_CSTA interrupt
11240060	SDC_DATCRC_STS	32	**SD Card Data CRC Status Register** Reflects CRC status of data line[7:0]. Only for MSDC read.
11240070	EMMC_CFG0	32	**EMMC Configuration Register 0** For boot-up mode general configuration of e-MMC version 4.3 and 4.4
11240074	EMMC_CFG1	32	**EMMC Configuration Register 1** For boot-up mode general configuration of e-MMC version 4.3 and 4.4.
11240078	EMMC_STS	32	**EMMC Status Register** Reflects status of e-MMC boot-up mode operation
1124007C	EMMC_IOCON	32	**EMMC IO Control Register** Controls H/W reset pin of e-MMC boot-up mode operation
11240080	SD_ACMD_RESP	32	**SD ACMD Response Register** Stores response of auto command from SD card
11240084	SD_ACMD19_TRG	32	**SD ACMD19 Target Register** Selects target delay line to run ACMD19 sequence
11240088	SD_ACMD19_STS	32	**SD ACMD19 Status Register** Stores result of auto command 19 from SD card
1124008C	DMA_SA_HIGH4BIT	32	**DMA Current Address Register of High 4 Bits** Contains start address high 4 bits of the 36-bit address for 64G DRAM access
11240090	DMA_SA	32	**DMA Start Address Register** Contains start address of DMA descriptor
11240094	DMA_CA	32	**DMA Current Address Register** Contains current DMA address
11240098	DMA_CTRL	32	**DMA Control Register** Controls DMA operation
1124009C	DMA_CFG	32	**DMA Configuration Register** Configures DMA operation
112400A0	SW_DBG_SEL	32	**MSDC S/W Debug Selection Register** Selects SW debugging output
112400A4	SW_DBG_OUT	32	**MSDC S/W Debug Output Register** Shows selected debugging output
112400A8	DMA_LENGTH	32	**DMA Length Register** Sets up basic DMA operation length
112400B0	PATCH_BIT0	32	**MSDC Patch Bit Register 0** Configures patch function. For normal function, this bit should be kept at default value.
112400B4	PATCH_BIT1	32	**MSDC Patch Bit Register 1** Configures patch function. For normal function, this bit should be

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Address	Name	Width	Register Function
			kept at default value.
112400B8	PATCH_BIT2	32	**MSDC Patch Bit Register 2** Configures patch function. For normal function, this bit should be kept at default value.
112400C0	DAT0_TUNE_CRC	32	**DAT0 Tune Result Register** Records on-line tuning result for DAT0 line
112400C4	DAT1_TUNE_CRC	32	**DAT1 Tune Result Register** Records on-line tuning result for DAT1 line
112400C8	DAT2_TUNE_CRC	32	**DAT2 Tune Result Register** Records on-line tuning result for DAT2 line
112400CC	DAT3_TUNE_CRC	32	**DAT3 Tune Result Register** Records on-line tuning result for DAT3 line
112400D0	CMD_TUNE_CRC	32	**CMD Tune Result Register** Records on-line tuning result for CMD line
112400D4	SDIO_TUNE_WIND	32	**SDIO Tune Window Register 0** Defines tuning window size for SDIO on-line CRC tuning feature
112400F0	PAD_TUNE0	32	**MSDC Pad Tuning Register 0** Configures delay line embedded in pad macro
112400F4	PAD_TUNE1	32	**MSDC Pad Tuning Register 1** Configures delay line embedded in pad macro
112400F8	DAT_RD_DLY0	32	**MSDC Data Delay Line Register 0** Configures delay line embedded in pad macro
112400FC	DAT_RD_DLY1	32	**MSDC Data Delay Line Register 1** Configures delay line embedded in pad macro
11240100	DAT_RD_DLY2	32	**MSDC Data Delay Line Register 2** Configures delay line embedded in pad macro
11240104	DAT_RD_DLY3	32	**MSDC Data Delay Line Register 3** Configures delay line embedded in pad macro
11240110	HW_DBG_SEL	32	**MSDC H/W Debug Selection Register** Selects HW debug output
11240114	MAIN_VER	32	**MSDC Main Version Register** Shows the version code of MSDC IP
11240118	ECO_VER	32	**MSDC ECO Version Register** Shows the ECO version code of MSDC IP

11240000 MSDC_CFG MSDC Configuration Register 02000099

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SCLK STOP SEL				CCKMD		CCKDIV[11:8]			
Type							RW				W1C		RW			
Reset							1				0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CCKDIV[7:0]								CCKSB	BV18PSS	BV18SDT	CCKDRVE	PIO	RST	CCKPD	MSDC
Type	RW								RU	RU	RW	RW	RW	AO	RW	RW
Reset	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1

Bit(s)	Mnemonic	Name	Description
25	SCLKSTOPSEL	SCLK_STOP_SEL	**In DDR mode, stops SCLK when device is idle whether checking SCLK phase or not** 1'b0: Stop sclk not checking SCLK phase

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Bit(s)	Mnemonic	Name	Description
			1'b1: Stop sclk checking SCLK phase; fix 1/4T sclk glitch in DDR mode
21:20	**CCKMD**	CARD_CK_MODE	**MS/SD card clock mode** 2'b00: Use clock divider output divided by msdc_src_ck as msdc_ck. bit[15]~bit[8] should be programmed. 2'b01: Use msdc_src_ck as msdc_ck. bit[15]~bit[8] is ignored. 2'b10: DDR mode; use clock divider output divided by msdc_src_ck as msdc_ck. bit[15]~bit[8] should be programmed. 2'b11: HS400 mode; use clock divider output and use msdc_src_ck as msdc_ck. bit[15]~bit[8] should be programmed.
19:8	**CCKDIV**	CARD_CK_DIV	**MS/SD card clock divider** Controls clock frequency of serial clock on MS/SD bus. Refer to "Data Line Latching Timing Diagram" and "Response Latching Timing Diagram". For non-DDR mode, msdc_ck equals SD bus clock. (Example: For SDR25 or HS, msdc_ck and SD bus clock will be 50MHz) For DDR mode, msdc_ck denotes MSDC internal clock which will be doubled to SD bus clock. (Example: For DDR50, msdc_ck should be set to 100MHz, and bus clock will be 50MHz.) 8'b00000000: msdc_ck =(1/2)*msdc_src_ck 8'b00000001: msdc_ck = [1/(4*1)]*msdc_src_ck 8'b00000010: msdc_ck = [1/(4*2)]*msdc_src_ck 8'b00000011: msdc_ck = [1/(4*3)]*msdc_src_ck 8'b00010000: msdc_ck = [1/(4*16)]*msdc_src_ck 8'b11111111: msdc_ck = [1/(4*255)]*msdc_src_ck
7	**CCKSB**	CARD_CK_STABLE	**MS/SD card clock is stable or not** After programming CARD_CK_MODE or CARD_CK_DIV, this bit will immediately become 0 and return to 1 if stable. Poll this register to ensure safety control of MSDC. 1'b0: Clock output is not stable. 1'b1: Clock output is stable.
6	**BV18PSS**	BV_1P8_PASS	**MSDC bus voltage 1.8V detection status** SW should check this bit after BUS_VOL_18V_START_DET turns to 0 from 1. 1'b0: Error in voltage detection 1'b1: No error in voltage detection
5	**BV18SDT**	BV_1P8_START_DET	**MSDC bus voltage 1.8V detection sequence start event** SW writes 1 to this bit to trigger HW outputting 1.8V clock for 1ms and automatically detecting CMD/DAT line sequence for voltage change is passed or not. HW will clear this bit to 0 after the detection is finished. The passed or failed status is stored in bit[6] BUS_VOL_18V_PASS.
4	**CCKDRVE**	CARD_CK_DRV_EN	**SD/MS card bus clock drive enable bit** Set this bit to 1 to enable MSDC bus clock driver. The default bus state depends on MSDC_CFG][1] CARD_CK_PWDN bit. If MSDC_CFG[1] CARD_CK_PWDN=1, the default clock state will be free running. If MSDC_CFG[1] CARD_CK_PWDN=0, the default clock state will be gated to 0. Set this bit to 0 will put the bus state into "tri-state". Default: 1 1'b0: Put the clock pad into tri-state 1'b1: Enable MSDC to drive clock pad. The state of CLK depends on MSDC_CFG[1] CARD_CK_PWDN.
3	**PIO**	PIO_MODE	**MS/SD PIO mode** Selects PIO mode. Default: PIO mode
2	**RST**	RST	**Software reset** Writing 1 to this register will cause internal synchronous reset of

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Bit(s)	Mnemonic	Name	Description
			MS/SD controller, and it will not reset register settings and DMA controller. The reset sequence is done when this bit becomes 0. SW should wait for this bit to return to 0 after writing 1. 1'b0: MS/SD controller is not in reset state. 1'b1: MS/SD controller is in reset state.
1	**CCKPD**	CARD_CK_PWDN	**MSDC bus clock power-down mode** Controls card clock power-down mode 1'b0: Clock is gated to 0 if no command or data is transmitted. 1'b1: Clock is free running even if no command or data is transmitted. (The clock may still be stopped when MSDC write data are not enough or no space for the next read data.)
0	**MSDC**	MSDC	**Selects MS/SD mode** Configures the controller to be the host of memory stick or host of SD/MMC memory card. The default value is configuring the controller as the host of memory stick. 1'b0: Configure controller to be host of memory stick 1'b1: Configure controller to be host of SD/MMC memory card

11240004 MSDC_IOCON MSDC IO Configuration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									**RD7SPL**	**RD6SPL**	**RD5SPL**	**RD4SPL**	**RD3SPL**	**RD2SPL**	**RD1SPL**	**RD0SPL**
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**WD3SPL**	**WD2SPL**	**WD1SPL**	**WD0SPL**	**WDSPLSEL**	**WDSPL**			**RDSPLSEL**	**DDR50CKD**	**DDLSEL**	**RDSPL**	**RSPL**	**SDR104CKS**
Type			RW	RW	RW	RW	RW	RW			RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23	**RD7SPL**	R_D7_SMPL	**Selects read data 7 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
22	**RD6SPL**	R_D6_SMPL	**Selects read data 6 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
21	**RD5SPL**	R_D5_SMPL	**Selects read data 5 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
20	**RD4SPL**	R_D4_SMPL	**Selects read data 4 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
19	**RD3SPL**	R_D3_SMPL	**Selects read data 3 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
18	**RD2SPL**	R_D2_SMPL	**Selects read data 2 sample**

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Bit(s)	Mnemonic	Name	Description
			Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
17	**RD1SPL**	R_D1_SMPL	**Selects read data 1 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
16	**RD0SPL**	R_D0_SMPL	**Selects read data 0 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
13	**WD3SPL**	W_D3_SMPL	**Selects SDIO interrupt sample** Only valid when bit 9 is on. 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
12	**WD2SPL**	W_D2_SMPL	**Selects SDIO interrupt sample** Only valid when bit 9 is on. 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
11	**WD1SPL**	W_D1_SMPL	**Selects SDIO interrupt sample** Only valid when bit 9 is on. 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
10	**WD0SPL**	W_D0_SMPL	**Selects CRC status and SDIO interrupt sample** Only valid when bit 9 is on. 1'b0: Sample CRC Status and SDIO interrupt by external bus clock rising edge 1'b1: Sample CRC Status and SDIO interrupt by external bus clock falling edge
9	**WDSPLSEL**	W_D_SMPL_SEL	**Selects data line rising/falling latch fine-tuning in write transaction** 1'b0: All data line share one value indicated by MSDC_IOCON.W_D_SMPL 1'b1: Each data line has its own selection value indicated by Data line 0: MSDC_IOCON.W_D0_SMPL Data line 1: MSDC_IOCON.W_D1_SMPL Data line 2: MSDC_IOCON.W_D2_SMPL Data line 3: MSDC_IOCON.W_D3_SMPL
8	**WDSPL**	W_D_SMPL	**Selects CRC status and SDIO interrupt sample** 1'b0: Sample CRC Status and SDIO interrupt by external bus clock rising edge 1'b1: Sample CRC Status and SDIO interrupt by external bus clock falling edge
5	**RDSPLSEL**	R_D_SMPL_SEL	**Selects data line rising/falling latch fine-tuning in read transaction** 1'b0: All data line share one value indicated by MSDC_IOCON.R_D_SMPL 1'b1: Each data line has its own selection value indicated by Data line 0: MSDC_IOCON.R_D0_SMPL Data line 1: MSDC_IOCON.R_D1_SMPL Data line 2: MSDC_IOCON.R_D2_SMPL Data line 3: MSDC_IOCON.R_D3_SMPL Data line 4: MSDC_IOCON.R_D4_SMPL Data line 5: MSDC_IOCON.R_D5_SMPL Data line 6: MSDC_IOCON.R_D6_SMPL Data line 7: MSDC_IOCON.R_D7_SMPL
4	**DDR50CK**	DDR50_DLY_SEL	**Selects DDR50 output clock delay**

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Bit(s)	Mnemonic	Name	Description
	D		1'b0: Use default clock output 1'b1: Delay 1T msdc_src_ck for clock output
3	**DDLSEL**	D_DLYLINE_SEL	**Selects data line delay line fine-tuning** 1'b0: All data line share one delay selection value indicated by PAD_TUNE.PAD_DAT_RD_RXDLY 1'b1: Each data line has its own delay selection value indicated by Data line 0: DAT_RD_DLY0.DAT0_RD_DLY Data line 1: DAT_RD_DLY0.DAT1_RD_DLY Data line 2: DAT_RD_DLY0.DAT2_RD_DLY Data line 3: DAT_RD_DLY0.DAT3_RD_DLY Data line 4: DAT_RD_DLY1.DAT4_RD_DLY Data line 5: DAT_RD_DLY1.DAT5_RD_DLY Data line 6: DAT_RD_DLY1.DAT6_RD_DLY Data line 7: DAT_RD_DLY1.DAT7_RD_DLY
2	**RDSPL**	R_D_SMPL	**Selects read data sample** 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
1	**RSPL**	R_SMPL	**Selects command response sample** 1'b0: Sample response by external bus clock rising edge 1'b1: Sample response by external bus clock falling edge
0	**SDR104CKS**	SDR104_CLK_SEL	**SDR104 SCLK output clock control** Only used when MSDC_CFG[17:16] CARD_CK_MODE is 2'b01. 1'b0: Bus clock output equals inverted msdc_src_ck 1'b1: Bus clock output equals msdc_src_ck

11240008 **MSDC_PS** **MSDC Pin Status Register** **01FF0002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SDWP**							**CMD**	**DAT**							
Type	RU							RU	RU							
Reset	0							1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CDDBCE**														**CDSTS**	**CDEN**
Type	RW														RU	RW
Reset	0	0	0	0											1	0

Bit(s)	Mnemonic	Name	Description
31	**SDWP**	SD_WP	**Write Protection switch status on SD memory card** Shows the status of Write Protection switch on SD memory card. There is no default reset value. The pin WP (Write Protection) is only useful when the controller is configured for SD memory card. 1'b0: Write Protection switch on, i.e. memory card will be write-protected. 1'b1: Write Protection switch off, i.e. memory card is writable.
24	**CMD**	CMD	**Command line status** Reflects the command line value of MSDC bus.
23:16	**DAT**	DAT	**Data line status** Reflects the data line value of MSDC bus (8-bit).
15:12	**CDDBCE**	CDDEBOUNCE	**Card detection de-bounce timer** Specifies the time interval for card detection de-bounce. Default value: 0, meaning the de-bounce interval is one 32kHz cycle. The interval will extend one cycle time of 32kHz by increasing the counter by 1.

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Bit(s)	Mnemonic	Name	Description
1	**CDSTS**	CDSTS	**Card detection status** 1'b0: Card detection pin status is logic low. 1'b1: Card detection pin status is logic high.
0	**CDEN**	CDEN	**Enables card detection** Controls the card detection circuit. 1'b0: Disable card detection 1'b1: Enable card detection

1124000C **MSDC_INT** **MSDC Interrupt Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										**AC53 FAIL**	**AC53 DON E**	**GEAR OUTB OUN D**	**DMA PROT ECT**	**GPDC SERR**	**BDCS ERR**	**AC19 DON E**
Type										W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SDDC RCER R**	**SDDT O**	**DMA XFDN E**	**SDXF CPL**	**SDCS TS**	**SDRC RCER**	**SDCT O**	**SDCR DY**	**SDIO IRQ**	**DMA QEPT Y**	**SDAC DRCR CER**	**SDAC DCTO**	**SDAC DCRD Y**		**MSD CCDS C**	**MMC IRQ**
Type	W1C	W1C	W1C	W1C	RU	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C		W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0

Bit(s)	Mnemonic	Name	Description
22	**AC53FAIL**	AUTOCMD53_FAIL	**SD auto command 53 status register** When auto-command 53 tuning sequence fails , this register will be set to 1 by HW.
21	**AC53DONE**	AUTOCMD53_DONE	**SD auto command 53 status register** When auto-command 53 tuning sequence is finished, this register will be set to 1 by HW.
20	**GEAROUTBOUND**	GEAR_OUT_BOUND	**The gear setting of delay line is out of boundary in the process of SDIO Autocmd 53 On-Line tuning**
19	**DMAPROTECT**	DMA_PROTECT	**There is write operation to DMA start address, length, start bit or the last BUF bit.**
18	**GPDCSERR**	GPD_CS_ERR	**GPD checksum error detected**
17	**BDCSERR**	BD_CS_ERR	**BD checksum error detected**
16	**AC19DONE**	AUTOCMD19_DONE	**SD auto command 19 status register** When auto-command 19 is enabled, HW will clear this register to 0. As the tuning sequence is finished (32 times), this register will be set to 1 by HW. SW should check AUTOCMD_STS0 and SUTOCMD_STS1 only when this bit is on.
15	**SDDCRCERR**	SD_DATA_CRCERR	1'b0: Otherwise 1'b1: MS/SD controller detects a CRC error after reading a block of data from the DAT line or SD/MMC signals a CRC error after writing a block of data to the DAT line.
14	**SDDTO**	SD_DATTO	
13	**DMAXFDNE**	DMA_XFER_DONE	**DMA transfer done interrupt** Indicates status of data block transfer. 1'b0: Otherwise 1'b1: A data block is successfully transferred.
12	**SDXFCPL**	SD_XFER_COMPL	**SD data transfer completed interrupt**

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Bit(s)	Mnemonic	Name	Description
		ETE	Indicates transaction which contains data that are completed. While performing tuning procedure (Execute Tuning is set to 1), SD_XFER_COMPLETE is not set to 1.
11	**SDCSTS**	SD_CSTS	**SD CSTA update interrupt** Indicates any bit in register SDC_CSTA is active. The register bit will be set to 1. SW should clear SDC_CSTA, and this bit will be de-asserted automatically.
10	**SDRCRCER**	SD_RESP_CRCERR	**SD command CRC error interrupt** Indicates SD/MMC controller detects a CRC error after reading a response from the CMD line. 1'b0: Otherwise 1'b1: SD/MMC controller detects a CRC error after reading a response from the CMD line.
9	**SDCTO**	SD_CMDTO	**SD command time-out interrupt** Indicates SD/MMC controller detects a time-out condition while waiting for a response on the CMD line. 1'b0: Otherwise 1'b1: SD/MMC controller detects a time-out condition while waiting for a response on the CMD line.
8	**SDCRDY**	SD_CMDRDY	**SD command ready interrupt** For the command without response, the register bit will be 1 once the command is completed on SD/MMC bus. For command with response without busy, the register bit will be 1 whenever the command is issued onto SD/MMC bus and its corresponding response is received without CRC error. For command with response with busy in DAT0, the register bit will be 1 whenever the command is issued onto SD/MMC bus and its corresponding response is received without CRC error and the DAT0 transited from busy to idle. 1'b0: Otherwise 1'b1: Command finished successfully without CRC error.
7	**SDIOIRQ**	SD_SDIOIRQ	**SD SDIO interrupt** Indicates the interrupt is sensed in the SDIO bus. 1'b0: No interrupt on SDIO bus 1'b1: Interrupt on SDIO bus
6	**DMAQEPTY**	DMA_Q_EMPTY	**DMA queue empty interrupt** Indicates the current DMA queue is empty. Only for descriptor mode and enhance mode.
5	**SDACDRCRCER**	SD_AUTOCMD_RESP_CRCERR	**SD auto command CRC error interrupt** Set when detecting a CRC error in the auto command response.
4	**SDACDCTO**	SD_AUTOCMD_CMDTO	**SD auto command time-out interrupt** Set if no response is returned within a specified cycles (64T in spec) from the end bit of auto command.
3	**SDACDCRDY**	SD_AUTOCMD_CMDRDY	**SD auto command ready interrupt** Set if auto command is executed without CRC error or timeout.
1	**MSDCCDSC**	MSDC_CDSC	**MSDC card detection status change interrupt** Indicates if any interrupt for memory card insertion/removal exists. Whenever memory card is inserted or removed and card detection circuit is enabled, i.e. register bit CDEN in register MSDC_PS is set to 1, the register bit will be set to 1. It will be reset when the register is read. 1'b0: Otherwise 1'b1: Card is inserted or removed.
0	**MMCIRQ**	MMC_IRQ	**MMC card interrupt** 1'b0: Otherwise 1'b1: MMC card interrupt event occurs.

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11240010 MSDC_INTEN MSDC Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										ENAC53FAIL	ENAC53DONE	ENGEAROUTBOUND	ENDMAPROTECT	ENGPDCSERR	ENBDCSERR	ENAC19DONE
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENSDDCRCERR	ENSDDTO	ENDMAXFDNE	ENSDXFCPL	ENSDCSTA	ENSDRCRCER	ENSDCTO	ENSDCRDY	ENSDIOIRQ	ENDMAQEPTY	ENSDACDRCRCER	ENSDACDCTO	ENSDACDCRDY		ENMSDCCDSC	ENMMCIRQ
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0

Bit(s)	Mnemonic	Name	Description
22	ENAC53FAIL	EN_AUTOCMD53_FAIL	**Enables auto-command 53 failure interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
21	ENAC53DONE	EN_AUTOCMD53_DONE	**Enables auto-command 53 completed interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
20	ENGEAROUTBOUND	EN_GEAR_OUT_BOUND	**Enables gear out boundary interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
19	ENDMAPROTECT	EN_DMA_PROTECT	**Enables DMA protection interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
18	ENGPDCSERR	EN_GPD_CS_ERR	**Enables GPD checksum error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
17	ENBDCSERR	EN_BD_CS_ERR	**Enables BD checksum error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
16	ENAC19DONE	EN_AUTOCMD19_DONE	**Enables auto-command 19 completed interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
15	ENSDDCRCERR	EN_SD_DATA_CRCERR	**Enables SD data CRC error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
14	ENSDDTO	EN_SD_DATTO	**Enables SD data timeout interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
13	ENDMAXFDNE	EN_SD_DMA_XFER_DONE	**Enables DMA transfer done interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
12	ENSDXFCPL	EN_SD_XFER_COMPLETE	**Enables SD data transfer completed interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
11	ENSDCSTA	EN_SD_CSTA	**Enables SD CSTA update interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt

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Bit(s)	Mnemonic	Name	Description
10	**ENSDRCRCER**	EN_SD_RESP_CRCERR	**Enables SD command CRC error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
9	**ENSDCTO**	EN_SD_CMDTO	**Enables SD command timeout interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
8	**ENSDCRDY**	EN_SD_CMDRDY	**Enables SD command ready interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
7	**ENSDIOIRQ**	EN_SD_SDIOIRQ	**Enables SD SDIO interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
6	**ENDMAQEPTY**	EN_DMA_Q_EMPTY	**Enables DMA queue empty interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
5	**ENSDACDRCRCER**	EN_SD_AUTOCMD_RESP_CRCERR	**Enables SD auto command CRC error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
4	**ENSDACDCTO**	EN_SD_AUTOCMD_CMDTO	**Enables SD auto command time-out interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
3	**ENSDACDCRDY**	EN_AUTOCMD_CMDRDY	**Enables SD auto command ready interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
1	**ENMSDCCDSC**	EN_MSDC_CDSC	**Enables MSDC card detection status change interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
0	**ENMMCIRQ**	EN_MMC_IRQ	**Enables MMC card interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt

11240014 **MSDC_FIFOCS** **MSDC FIFO Control and Status Register** **7C000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**FIFOCLR**	**FIFO**							**TXFIFOCNT**							
Type	A0	A0							RU							
Reset	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**RXFIFOCNT**							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**FIFOCLR**	FIFOCLR	**Clears embedded FIFO** Write 1 to this bit to clear FIFO. It will become 0 when FIFO is cleared. SW needs to check this bit to make sure clearing FIFO sequence is done. This bit can be used when the data read/write sequence has error and needs to clean the HW FIFO.
30:24	**FIFO**	FIFO	

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Bit(s)	Mnemonic	Name	Description
23:16	**TXFIFOCNT**	TXFIFOCNT	**TX FIFO count for MSDC write** 8'd0: No data in FIFO 8'd1: 1 byte of data in FIFO 8'd2: 2 bytes of data in FIFO 8'd131: Maximum 131 bytes of data in FIFO Others: Reserved
7:0	**RXFIFOCNT**	RXFIFOCNT	**RX FIFO count for MSDC read** 8'd0: No data in FIFO 8'd1: 1 byte of data in FIFO 8'd2: 2 bytes of data in FIFO 8'd131: Maximum 131 bytes of data in FIFO Others: Reserved

11240018 **MSDC_TXDATA** **MSDC TX Data Port Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PIOTXDATA[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PIOTXDATA[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**PIOTXDATA**	PIO_TXDATA	**PIO mode TXDATA port** This register can be accessed by byte, half-word or word. This port can only be accessed in PIO mode. Otherwise, the transaction will be discarded.

1124001C **MSDC_RXDATA** **MSDC RX Data Port Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PIORXDATA[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PIORXDATA[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**PIORXDATA**	PIO_RXDATA	**PIO mode RXDATA port** This register can be accessed by byte, half-word or word. This port can only be accessed in PIO mode. Otherwise, the transaction will be discarded.

11240030 **SDC_CFG** **SD Configuration Register** **00100000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	DTOC										INTBGP	SDIOIDE	SDIO		BUSWD	
Type	RW										RW	RW	RW		RW	
Reset	0	0	0	0	0	0	0	0			0	1	0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															ENWKUPINS	ENWKUPSDIOINT
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DTOC**	DTOC	**Data timeout counter** The period from the end of the initial host read command or the last read data block in a multiple block read operation to the start bit of the next read data block requires at least two serial clock cycles. The counter is used to extend the period (Read Data Access Time) in unit of 1,048,576 serial clocks. 8'b00000000: Extend 1,048,576 more serial clock cycles 8'b00000001: Extend 1,048,576*2 more serial clock cycles 8'b00000010: Extend 1,048,576*3 more serial clock cycles 8'b11111111: Extend 1,048,576*256 more serial clock cycles
21	**INTBGP**	INT_AT_BLOCK_GAP	**Interrupt at block gap** This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Set to 1 will enable interrupt detection at the block gap for a multiple block transfer. Set to 0 will disable interrupt detection during a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0. When the host driver detects an SD card insertion, it will set up this bit according to CCCR of the SDIO card. 1'b0: Disable interrupt detection at block gap 1'b1: Enable interrupt detection at block gap
20	**SDIOIDE**	SDIO_INT_DET_EN	**Enables SDIO interrupt detection** Informs SD controller to sense SDIO interrupt. 1'b0: Disable SDIO interrupt detection 1'b1: Enable SDIO interrupt detection if SDIO bit is also on
19	**SDIO**	SDIO	**SDIO mode enable bit** Enables support to sense SDIO interrupt and disables R4 response CRC check for SDIO card. 1'b0: Disable SDIO mode 1'b1: Enable SDIO mode
17:16	**BUSWD**	BUSWIDTH	**Configures bus width** Defines SD/MMC bus width. 2'b00: 1-bit mode 2'b01: 4-bit mode 2'b10: 8-bit mode 2'b11: Reserved
1	**ENWKUPINS**	WAKEUP_INS_EN	**Card status change wakeup event enable bit** 1'b0: Disable wakeup event for card status change 1'b1: Enable wakeup event for card status change
0	**ENWKUPSDIOINT**	WAKEUP_SDIOINT_EN	**SDIO card interrupt wakeup event enable bit** 1'b0: Disable wakeup event for SDIO card interrupt 1'b1: Enable wakeup event for SDIO card interrupt

11240034 **SDC_CMD** **SD Command Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	ACMD53	VOLSWTH	ACMD		LEN											
Type	RW	RW	RW		RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GOIRQ	STOP	RW	DTYPE			RSPTYP			BREAK	CMD					
Type	RW	RW	RW	RW			RW			RW	RW					
Reset	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**ACMD53**	AUTO_CMD53	**Enables auto command 53** Should be used exclusively with AUTO_CMD, meaning AUTO_CMD != 2'b00. This field should be assigned to 1'b0. If this filed is assigned to 1'b1, AUTO_CMD should be set to 2'b00. 1'b0: Disable Auto Command 53 1'b1: Enable Auto Command 53
30	**VOLSWTH**	VOL_SWTH	**Voltage switch command** 1'b0: Disable voltage switch detection 1'b1: Enable voltage switch detection
29:28	**ACMD**	AUTO_CMD	**Enables auto command** Determines use of auto command functions. This function can be used in all modes including PIO/Basic DMA/Descriptor DMA/Enhanced Mode. There are two methods to stop multiple-block read and write operation. 1. Enabling auto CMD12 Multiple-block read and write commands for memory require CMD12 to stop the operation. When ACMD-12 is used, MSDC issues CMD12 automatically when the last block transfer is completed. Auto CMD12 error is indicated to the MSDC_INT register. The host driver shall not set up this bit if the command does not require CMD12. In particular, secure commands defined in the Part 3 File Security specification do not require CMD12. 2. Enabling auto CMD23 When ACMD-23 is used, MSDC issues a CMD23 automatically before issuing a command specified in the CMD field. The Host Controller Version 3.00 and later versions support this function. By writing the command register, MSDC issues a CMD23 first then a command specified by the CMD field in the SDC_CMD register. If response errors of CMD23 are detected, the second command will not be issued. A CMD23 error is indicated in the MSDC_INT register. 32-bit block count value for CMD23 is set to the SDC_BLOCK_NUM register. 2'b00: Disable Auto Command 2'b01: Enable Auto CMD12 2'b10: Enable Auto CMD23 2'b11: Enable Re-tuning CMD19
27:16	**LEN**	LEN	**Length** Defines the length of one block (unit: byte) in a data transaction of block mode or the data length (unit: byte) in data transaction of byte mode. The maximum value of block length is 2,048 bytes. 12'b000000000000: Reserved 12'b000000000001: Block length is 1 byte 12'b000000000010: Block length is 2 byte 12'b011111111111: Block length is 2047 byte 12'b100000000000: Block length is 2048 byte
15	**GOIRQ**	GO_IRQ	**GO_IRQ command** Indicates if the command is GO_IRQ_STATE (CMD40) and used only for MMC protocol. If the command is GO_IRQ_STATE, the period between command token and response token will not be

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Bit(s)	Mnemonic	Name	Description
			limited. 1'b0: The command is not GO_IRQ_STATE 1'b1: The command is GO_IRQ_STATE
14	**STOP**	STOP	**Stop command** Indicates if the command is a stop transmission command. It should be set to 1 when CMD12 (SD/MMC) or CMD52 with I/O abort (SDIO) is to be issued. 1'b0: The command is not a stop transmission command 1'b1: The command is a stop transmission command
13	**RW**	RW	**Selects command read write** The register bit defines the command is a read command or write command. The register bit is valid only when the command causes a transaction with data token. 1'b0: The command is a read command 1'b1: The command is a write command
12:11	**DTYPE**	DTYPE	**Selects data block** Defines data token type for the command. 2'b00: No data token for the command 2'b01: Single block transaction (only available in block mode) 2'b10: Multiple block transaction. (only available in block mode) 2'b11: Stream operation. It only shall be used in MMC protocol. (only available in block mode)
9:7	**RSPTYP**	RSPTYP	**Command response type** 3'b000: This command has no response. 3'b001: The command has R1/R5/R6/R7 response. The response token is 48-bit with CRC check (For SD/MMC/SDIO) (Not include the SDIO abort command) 3'b010: The command has R2 response. The response token is 136-bit (For SD/MMC) 3'b011: The command has R3 response. The response token is 48-bit response, no CRC check (For SD/MMC) 3'b100: The command has R4 response. The response token is 48-bit without CRC check (For SDIO) The response token is 48-bit with CRC check (For MMC) 3'b111: The command has R1b response. The response token is 48-bit (For SD/MMC/SDIO)
6	**BREAK**	BREAK	**Aborts pending MMC GO_IRQ command** Only valid for a pending GO_IRQ_MODE command waiting for MMC interrupt response. 1'b0: Not a beak command 1'b1: Break a pending MMC GO_IRQ_MODE command in the controller.
5:0	**CMD**	CMD	**SD Memory Card command**

11240038 **SDC_ARG** **SD Argument Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ARG[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ARG[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
31:0	**ARG**	ARG	Memory card controller argument register

1124003C SDC_STS SD Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MMCSWRCPL**															**CMD_WR_BUSY**
Type	RU															W1C
Reset	0															0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**CMDBSY**	**SDCBSY**
Type															RU	RU
Reset															0	0

Bit(s)	Mnemonic	Name	Description
31	**MMCSWRCPL**	MMC_STREAM_WR_COMPL	**MMC stream mode write data are all flushed to MMC card.** SW can use this bit to confirm the last write data are flushed to MMC before issuing the STOP command. This bit is only valid when command SDC_CMD.DTYPE=2'b11. 1'b0: Last Data are partially inside MSDC 1'b1: Last data are flushed to MMC card
16		CMD_WR_BUSY	
1	**CMDBSY**	CMDBUSY	**SD command line busy status** SW should always read this bit to make sure the command line is not busy before sending the next command. If the command is R1B or data read/write command, SW should also check the SDCBUSY bit. Note: When auto command 12 is enabled, this bit will be asserted immediately after SDC_CMD is written and de-asserted after auto-command 12 is finished. 1'b0: No transmission is going on CMD line on SD bus. 1'b1: There is transmission going on CMD line on SD bus.
0	**SDCBSY**	SDCBUSY	**SD controller busy status** 1'b0: SD controller is idle 1'b1: SD controller is busy

11240040 SDC_RESP0 SD Response Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RESP0[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RESP0[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP0**	RESP0	Memory card controller response register 0

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11240044 SDC_RESP1 SD Response Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP1[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP1[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP1**	RESP1	Memory card controller response register 1

11240048 SDC_RESP2 SD Response Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP2[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP2[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP2**	RESP2	Memory card controller response register 2

1124004C SDC_RESP3 SD Response Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP3[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP3[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP3**	RESP3	Memory card controller response register 3

11240050 SDC_BLK_NUM SD Block Number Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BLKNUM[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BLKNUM[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

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Bit(s)	Mnemonic	Name	Description
31:0	**BLKNUM**	BLOCK_NUMBER	**Memory card controller block number** Indicates block number of data transaction. 32'd0: Reserved 32'd1: 1-data block 32'd2: 2-data block 32'd3: 3-data block 32'hffffffff: 4GB-1 data block

11240054 SDC_VOL_CHG SD Voltage Change Wait Time Register 00000145

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VCHGCNT															
Type	RW															
Reset	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	1

Bit(s)	Mnemonic	Name	Description
15:0	**VCHGCNT**	VOL_CHG_WAIT_CNT	**Defines SD voltage change check wait time** The wait time is clock frequency multiplied by VOL_WAIT_TIME.

11240058 SDC_CSTS SD Card Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSTS[31:16]															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSTS[15:0]															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CSTS**	CSTS	**CSTS** The card status field in the response R1 or R1b field. Each bit can be written 1 to clear individually.

1124005C SDC_CSTS_EN SD Card Status Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSTS_EN[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSTS_EN[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31:0	**CSTS_EN**	CSTS_EN	**CSTS_EN** Controls which bit of CSTA will generate MSDC_INT.SDCSTA.

11240060 **SDC_DATCRC_STS** **SD Card Data CRC Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCSSN								DCSSP							
Type	RU								RU							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8	**DCSSN**	DAT_CRCSTS_NEG	**MSDC DDR mode negative edge read data CRC status** Reflects CRC status of data line[7:0] in DDR mode. The positive edge CRC status is shown in DAT_CRC_STS[7:0]. Only for MSDC read. 1'b0: No CRC error 1'b1: CRC error
7:0	**DCSSP**	DAT_CRCSTS_POS	**MSDC read data CRC status** Reflects CRC status of data line[7:0]. Only for MSDC read. 1'b0: No CRC error 1'b1: CRC error

11240070 **EMMC_CFG0** **EMMC Configuration Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BTSUP	BTWDLY											BTACHKDIS	BTMOD	BTSTOP	BTSTART
Type	RW	RW											RW	RW	WO	WO
Reset	0	0	0	0									0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**BTSUP**	BOOT_SUPPORT	**Supports eMMC boot-up** Indicates boot mode is supported or not. 1'b0: Does not support 1'b1: Support
14:12	**BTWDLY**	BOOT_WAIT_DELAY	**eMMC wait delay time** Sets up delay time to wait for MMC device to exit boot-up mode after boot stop bit is set. 3'b000: 0x1024 clock cycles 3'b001: 1x1024 clock cycles 3'b010: 2x1024 clock cycles

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Bit(s)	Mnemonic	Name	Description
			3'b111: 7x1024 clock cycles
3	**BTACHKDIS**	BOOT_ACK_CHK_DIS	**Disables eMMC boot-up mode ACK check** 1'b0: Does ACK pattern check 1'b1: Bypass ACK pattern check
2	**BTMOD**	BOOT_MODE	**eMMC boot-up mode** There are two boot-up modes supported by eMMC 4.4. Reset CMD mode is optional for eMMC 4.3. 1'b0: Pull low CMD mode 1'b1: Reset CMD mode
1	**BTSTOP**	BOOT_STOP	**Stops eMMC boot-up** Indicates boot ACK pattern is supported or not. Read always returns to 0.
0	**BTSTART**	BOOT_START	**eMMC boot-up start signal trigger** The register bit is boot up start signal trigger. Read always returns to 0.

11240074 EMMC_CFG1 EMMC Configuration Register 1 00200003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BTATOC												BTDTOC[19:16]			
Type	RW												RW			
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BTDTOC[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
31:20	**BTATOC**	BOOT_ACK_TOC	**eMMC ack pattern timeout counter** Unit: 2^16 serial clock. SW cannot set it to 12'hFFF.
19:0	**BTDTOC**	BOOT_DAT_TOC	**eMMC read boot data timeout counter** Unit: 2^16 serial clock. SW cannot set it to 20'hFFFFF.

11240078 EMMC_STS EMMC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BTDRCV	BTARCV	BTSTS	BTATO	BTDTO	BTAERR	BTDERR
Type										RU	W1C	RU	W1C	W1C	W1C	W1C
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6	**BTDRCV**	BOOT_DAT_RECV	**eMMC boot data are received.** This register is for SW to check the first 4-byte boot data are received or not. For other data after the first 4B data, this bit should not be referred to. SW should check RXFIFOCNT instead. 1'b0: No data in RXFIFO 1'b1: The 1st 4B data are in RXFIFO.

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Bit(s)	Mnemonic	Name	Description
5	**BTARCV**	BOOT_ACK_RECV	**eMMC ack is received.** Checking BOOT_ACK_ERR to determine it is passed or failed is also required. 1'b0: No ACK pattern is received 1'b1: ACK pattern has been received
4	**BTSTS**	BOOT_UP_STATE	**eMMC boot-up mode status** Indicates if MMC device operates at boot-up mode state. 1'b0: Not in boot-up state 1'b1: Boot-up state is on-going.
3	**BTATO**	BOOT_ACK_TO	**eMMC ACK timeout** Indicates the controller detects a time-out condition while waiting for an ACK pattern on DAT0. 1'b0: No ACK pattern timeout error 1'b1: ACK pattern timeout error
2	**BTDTO**	BOOT_DAT_TO	**eMMC data timeout** Indicates the controller detects a timeout condition while waiting for boot data. 1'b0: No Data timeout error 1'b1: Data timeout error
1	**BTAERR**	BOOT_ACK_ERR	**eMMC ACK error** Indicates the status of ACK pattern check result. The bit is set to 1 when there is ACK pattern error. 1'b0: No ACK pattern check error 1'b1: ACK pattern check error
0	**BTDERR**	BOOT_CRC_ERR	**eMMC CRC error** Indicates CRC status of boot data. The bit is set to 1 when there is data CRC error. 1'b0: No Data CRC error 1'b1: Data CRC error

1124007C **EMMC_IOCON** **EMMC IO Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**BTRST**
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**BTRST**	BOOT_RST	**Resets eMMC device boot-up mode** Triggers HW reset to set eMMC device to entering pre-idle state. 1'b0: De-assert RST_n from eMMC card 1'b1: Assert RST_n to eMMC card

11240080 **SD_ACMD_RESP** **SD ACMD Response Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	ACMDRESP[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACMDRESP[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	ACMDRESP	AUTOCMD_RESP	**SD auto command response register** Stores response[39:8] of ACMD12/ACMD23/ACMD19.

11240084 SD_ACMD19_TRG SD ACMD19 Target Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													ACMDFTSEL			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	ACMDFTSEL	FINE_TUNE_SEL	**Selects SD auto command 19 test target** After auto-command 19 is triggered, MSDC will only change the phase of the selected one and keep the value of other tuning registers. SW can get the result from AUTOCMD_STS. There are total 32 phases for each delay line. 4'd0: Select PAD_CLK_TXDLY[5:0] as the target to run auto-command19. 4'd1: Select PAD_CMD_RXDLY[5:0] as the target to run auto-command19. 4'd2: Select PAD_DAT_RD_RXDLY[5:0] as the target to run auto-command19. 4'd3: Select PAD_DAT_WR_RXDLY[5:0] as the target to run auto-command19. 4'd4: Select DAT0_RD_DLY[5:0] as the target to run auto-command19. 4'd5: Select DAT1_RD_DLY[5:0] as the target to run auto-command19. 4'd6: Select DAT2_RD_DLY[5:0] as the target to run auto-command19. 4'd7: Select DAT3_RD_DLY[5:0] as the target to run auto-command19. 4'd8: Select DAT4_RD_DLY[5:0] as the target to run auto-command19. 4'd9: Select DAT5_RD_DLY[5:0] as the target to run auto-command19. 4'd10: Select DAT6_RD_DLY[5:0] as the target to run auto-command19. 4'd11: Select DAT7_RD_DLY[5:0] as the target to run auto-command19. 4'd12: Select CMD_RESP_RXDLY[5:0] as the target to run auto-command19. Others: Reserved

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11240088 SD_ACMD19_STS SD ACMD19 Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ACMD19STS[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACMD19STS[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	ACMD19STS	AUTOCMD19_STS	**SD auto command 19 test result register** When auto-command 19 is enabled, HW will automatically try 32 times of command-19 and store the result into this register. This register contains the 1st to 32rd results in bit[0:31].

1124008C DMA_SA_HIGH4BIT DMA Current Address Register of High 4 Bits 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DMASAHIGH4BIT			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	DMASAHIGH4BIT	DMA_SURR_ADDR_HIGH4BIT	Sets up the high 4-bit address of start address since the 64G DRAM needs a 36-bit address

11240090 DMA_SA DMA Start Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMASA[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMASA[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	DMASA	DMA_STR_ADDR	**Start address of DMA address** Sets up the start address of the DMA. In DMA basic mode, this field indicates the source or destination address of the data transfer which depends on the command. In descriptor base DMA, this is the descriptor chain start address.

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11240094 DMA_CA DMA Current Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMACA[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMACA[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DMACA**	DMA_CURR_ADDR	**Current address of DMA address** Reads the current address of DMA descriptor chain.

11240098 DMA_CTRL DMA Control Register 00006008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		BSTSZ			SPLIT1K	LASTBF	DMAALIGN	DMAMOD					READYM	DMARSM	DMASTOP	DMASTART
Type		RW			RW	RW	RW	RW					RU	WO	A0	WO
Reset		1	1	0	0	0	0	0					1	0	0	0

Bit(s)	Mnemonic	Name	Description
14:12	**BSTSZ**	BURST_SIZE	**DMA burst size** Specifies the maximum transfer bytes allowed at the device per DMA burst. This field cannot be modified when the DMA status is 1. 3'd3: 8 Bytes 3'd4: 16 Bytes 3'd5: 32 Bytes 3'd6: 64 Bytes Other: Reserved
11	**SPLIT1K**	DMA_SPLIT_1K	**Specifies split burst when corssing 1K boundary address** 1'b0: 1K boundary not split 1'b1: 1K boundary split
10	**LASTBF**	LAST_BUF	**Last buffer of the basic DMA mode** Indicates the last buffer in basic DMA mode.
9	**DMAALIGN**	DMA_ALIGN	**Specifies address alignment burst size** 1'b0: do not DAM burst size alignment 1'b1: DAM burst size alignment
8	**DMAMOD**	DMA_MODE	**DMA operation mode** Indicates operation mode of DMA. 1'b0: Basic DMA mode 1'b1: Descriptor base DMA mode
3	**READYM**	AHB_READYM	**Only for debugging when DMA hangs** SW checks if AHB bus is ok when GDMA hangs. 1: bus is normal 0: bus not normal
2	**DMARSM**	DMA_RESUME	**DMA resume control register** Resumes DMA transaction. Read always returns to 0.

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Bit(s)	Mnemonic	Name	Description
1	DMASTOP	DMA_STOP	**DMA stop control register** Stops DMA transaction. When SW issues STOP command, SW must wait for this bit to be de-asserted or DMA inactive to guarantee stop is done.
0	DMASTART	DMA_START	**DMA start control register** Starts DMA transaction. Read always returns to 0.

1124009C **DMA_CFG** **DMA Configuration Register** **00000004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															OUTBOUNDSTOPDMA	DMACHKSUM12B
Type															RW	RW
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			MSDCACTIVEEN				AHBHPROT2EN							LOCKDISABLE	DSCPCSEN	DMASTS
Type			RW				RW							RW	RW	RU
Reset			0	0			0	0						1	0	0

Bit(s)	Mnemonic	Name	Description
17	OUTBOUNDSTOPDMA	OUT_BOUND_STOP_DMA	**Determines whether to stop Enhance DMA if gear setting is out of boundary when sending training data** 1'b0: Enhance DMA continues even when gear setting is out of boundary during training data sending. 1'b1: Enhance DMA stops when gear setting is out of boundary during training data sending.
16	DMACHKSUM12B	DMA_CHK_SUM_12B	**Indicates GPD/BD checksum covers 16 bytes or 12 bytes** 1'b0: GPD/BD checksum covers 16 bytes. 1'b1: GPD/BD checksum only covers 12 bytes.
13:12	MSDCACTIVEEN	MSDC_ACTIVE_EN	**Indicates how to control msdc_active** 2'b00: dynamic control msdc_active 2'b01: msdc_active = 0 2'b10: msdc_active = 1 2'b11: Reserved
9:8	AHBHPROT2EN	AHB_HPROT_2_EN	**Determines how to control hprot_2 pin of AHB bus** AHB_HPROT_2_EN = 2'b00, and basic DMA mode All the write transfers of a burst will be accessed by bufferable mode except for the last burst of DMA AHB_HPROT2_2_EN=2'b00, and descriptor DMA mode. All write transfers of a burst will be accessed by bufferable mode except for HW own update transfer. 2'b00: dynamic control hprot_2 2'b01: hprot_2 = 0 2'b10: hprot_2 = 1
2	LOCKDISABLE	LOCK_DISABLE	**Disables lock to improve EMI efficiency** 1'b0: enable ahb lock 1'b1: disable ahb lock
1	DSCPCSEN	DMA_DSCP_CS_EN	**Enables DMA descriptor checksum** This bit is used to enable or disable the descriptor checksum validation function for the descriptor. This field cannot be modified when the DMA status is 1.

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Bit(s)	Mnemonic	Name	Description
0	**DMASTS**	DMA_STATUS	**DMA status** Indicates the status of DMA. 1'b0: DMA engine is inactive 1'b1: DMA engine is active

112400A0 SW_DBG_SEL MSDC S/W Debug Selection Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SWDBGSEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**SWDBGSEL**	DBG_SEL	**Selects MSDC debugging** Reserved.

112400A4 SW_DBG_OUT MSDC S/W Debug Output Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SWDBGO[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SWDBGO[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SWDBGO**	DBG_OUT	**MSDC debugging output** 32-bit output selected by SW_DBG_SEL register

112400A8 DMA_LENGTH DMA Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	XFSZ[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	XFSZ[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**XFSZ**	XFER_SIZE	**DMA total transfer size** Specifies the number of DMA transfer byte required for the

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Bit(s)	Mnemonic	Name	Description
			movement of source data through DMA. This field is only valid in basic DMA mode.

112400B0 PATCH_BIT0 MSDC Patch Bit Register 0 403C0007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**PTCH31**	**PTCH30**	**PTCH29**	**PTCH28**	**PTCH27**	**PTCH26**	**PTCH22**				**PTCH18**				**PTCH17**	**PTCH16**
Type	RW	RW	RW	RW	RW	RW	RW				RW				RW	RW
Reset	0	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**PTCH15**	**CKGDLYS**					**INTCKS**			**DESCUP**	**PTCH5**	**PTCH4**	**PTCH3**	**PTCH02**	**PTCH01**	**PTCH00**
Type	RW	RW					RW			RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**PTCH31**	EN_MMC_DRV_RESP	**Enables MSDC always driving bus when outputting wake-up response (BREAK)** 1'b0: Disable 1'b1: Enable
30	**PTCH30**	DETECT_WR_CRC_TIMEOUT	**Detects MSDC write data CRC phase time-out** 1'b0: Does not detect CRC phase timeout 1'b1: Detect CRC phase timeout
29	**PTCH29**	SPC_ALWAYS_PUSH	**SPC buffer push mechanism** 1'b0: Push the buffer only when read transfer is on-going 1'b1: Always push the buffer
28	**PTCH28**	SDIO_INT_DLY_SEL	**Selects SDIO interrupt latch time** 1'b0: Latch the data line value in internal SDIO interrupt period 1'b1: Latch the data line value in 1 clock delay of internal SDIO interrupt period
27	**PTCH27**	SDC_CMD_CMDFAIL_SEL	**Selects SDIO interrupt period recovery** 1'b0: SDIO interrupt period will re-start after a CMD12 or CMD52 command is issued 1'b1: SDIO interrupt period whenever DAT line is not busy
26	**PTCH26**	SDC_CMD_IDRT_SEL	**Selects SD identification response time** The register bit indicates if the command has a response with NID (i.e. 5 serial clock cycles as defined in SD memory card Specification Part 1 Physical Layer Specification version 1.0) response time. The register bit is valid only when the command has a response token. Thus, the register bit must be set to 1 for CMD2 (ALL_SEND_CID) and ACMD41 (SD_APP_OP_CMD). 1'b0: Otherwise. 1'b1: The command has a response with NID response time.
25:22	**PTCH22**	SDC_CFG_WDOD	**SD Write Data Output Delay** The period from finish of the response for the initial host write command or the last write data block in a multiple block write operation to the start bit of the next write data block requires at least two serial clock cycles. The register field is used to extend the period (Write Data Output Delay) in unit of one serial clock. 4'b0000: No extension 4'b0001: Extend 1 more serial clock cycle 4'b0010: Extend 2 more serial clock cycles 4'b1111: Extend 15 more serial clock cycles
21:18	**PTCH18**	SDC_CFG_BSYDLY	**SD R1B busy detection mode**

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Bit(s)	Mnemonic	Name	Description
			Only valid for the commands with R1b response. If the command has a response of R1b type, MS/SD controller must monitor the data line 0 for card busy status from the bit time that is two serial clock cycles after the command end bit to check if operations in SD/MMC memory card are finished. The register field is used to expand the time between the command end bit and end of detection period to detect card busy status. If time is up and there is no card busy status on data line 0, the controller will abandon the detection. 4'b0000: No extension 4'b0001: Extend 1 more serial clock cycle 4'b0010: Extend 2 more serial clock cycles 4'b1111: Extend 15 more serial clock cycles
17	**PTCH17**	SDIO_CFG_INTC_SEL	**Selects SDIO interrupt model** 1'b0: When data line [1] = 0, trigger SDIO interrupt event. 1'b1: When data line [3:0] = 4'b1101, trigger SDIO interrupt event
16	**PTCH16**	MSDC_BLKNUM_SEL	**Supports ACMD23 reliable/force pro etc. features** 1'b0: Support ACMD23 reliable/force prog etc. feature 1'b1: Does not support ACMD23 reliable/force prog etc. feature
15	**PTCH15**	MSDC_FIFO_RD_DIS	**Disables MSDC RXFIFO read** 1'b0: Disable FIFO read permission to RXFIFO in PIO mode 1'b1: Enable FIFO read permission to RXFIFO in PIO mode
14:10	**CKGDLYS**	CKGEN_MSDC_DLY_SEL	**Selects CKBUF in CKGEN delay** Total 32 stages.
9:7	**INTCKS**	INT_DAT_LATCH_CK_SEL	**Selects internal MSDC clock phase** Total 8 stages, each stage can delay 1 clock period of msdc_src_ck.
6	**DESCUP**	DESC_UP_SEL	**SD transfer done interrupt should be issued when GPD are updated.** 1'b1: Enable new function to generate SD transfer done interrupt 1'b0: Use old function to generate SD transfer done interrupt
5	**PTCH5**	ACMD53_FAIL_ONE_SHOT	**Determines interrupt method of AUTOCMD53_FAIL** 1'b0: AUTOCMD53_FAIL interrupt will be asserted whenever CMD/DAT CRC error occurs. 1'b1: AUTOCMD53_FAIL interrupt will be asserted only when AUTOCMD53_DONE is asserted if there is CMD/DAT CRC error.
4	**PTCH4**	MASK_ACMD53_CRC_ERR_INTR	**Masks CMD/DAT CRC error interrupt when executing AUTOCMD53 training sequence** 1'b0: Enable CMD/DAT CRC error interrupt when executing AUTOCMD53 training sequence 1'b1: Mask CMD/DAT CRC error interrupt when executing AUTOCMD53 training sequence
3	**PTCH3**	RD_DAT_SEL	**Defines to use rising or falling buf data for SDR mode** 1'b0: Used rising buf data for SDR mode 1'b1: Used falling buf data for SDR mode
2	**PTCH02**	DIS_REFLECT_CMDWR_WHEN_BSY	**Enables SD command register write monitor** 1'b0: Enable monitor function 1'b1: Disable monitor function
1	**PTCH01**	EN_SDC_ODD_8BIT_SUP	**Enables SD odd number support for 8-bit data bus** 1'b0: Disable 1'b1: Enable
0	**PTCH00**	EN_SDC_ODD	**Enables SD odd number support for 8-bit data bus** 1'b0: Disable 1'b1: Enable

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112400B4 PATCH_BIT1 MSDC Patch Bit Register 1 FFF00009

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MSHBFCKEN	MRCTLCKEN	MWCTLCKEN	MSDCKEN	MACMDCKEN	MVOLDTCKEN	MPSCCKEN	MSPCCKEN	HGDMACKEN	HGDMACK	DCMEN	DCMDIVSEL1				SINGLEBURST
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RO	RW	RW				RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESETGDMA		BIAS28R0	BIAS28R1	BIAS28R2				GETCRCMARGIN	GETBUSYMARGIN	CMDTA			WRTA		
Type	RW		RW	RW	RW				RW	RW	RW			RW		
Reset	0		0	0	0	0	0	0	0	0	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
31	MSHBFCKEN	MSDC_CK_SHBFF_CKEN	**msdc_src_ck clock enable bit for SHBFF** 1'b0: Disable 1'b1: Enable
30	MRCTLCKEN	MSDC_CK_RCTL_CKEN	**msdc_src_ck clock enable bit for RCTL** 1'b0: Disable 1'b1: Enable
29	MWCTLCKEN	MSDC_CK_WCTL_CKEN	**msdc_src_ck clock enable bit for WCTL** 1'b0: Disable 1'b1: Enable
28	MSDCKEN	MSDC_CK_SD_CKEN	**msdc_src_ck clock enable bit for SD** 1'b0: Disable 1'b1: Enable
27	MACMDCKEN	MSDC_CK_ACMD_CKEN	**msdc_src_ck clock enable bit for ACMD** 1'b0: Disable 1'b1: Enable
26	MVOLDTCKEN	MSDC_CK_VOLDET_CKEN	**msdc_src_ck clock enable bit for VOLDET** 1'b0: Disable 1'b1: Enable
25	MPSCCKEN	MSDC_CK_PSC_CKEN	**msdc_src_ck clock enable bit for PSC** 1'b0: Disable 1'b1: Enable
24	MSPCCKEN	MSDC_CK_SPC_CKEN	**msdc_src_ck clock enable bit forSPC** 1'b0: Disable 1'b1: Enable
23	HGDMACKEN	AHB_CK_GDMA_CKEN	**hclk_ck clock enable bit for GDMA** 1'b0: Disable 1'b1: Enable
22	HGDMACK	AHB_CK	**hclk_ck clock enable bit for GDMA** 1'b0: Disable 1'b1: Enable
21	DCMEN	DCM_EN	**Host enabling DCM for low power** When there is no transfer, ahb_ck and msdc_src_ck will be divided from source clk. 1'b1: disable 1'b0: enable
20	DCMDIVSEL1	DCM_DIV_SEL1	**For spec4.5 divider msdc_src_ck from source clk; for spec50 divider ahb_ck from source clk** 1'b1: 32 divders from source clk 1'b0: 16 divders from source clk

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Bit(s)	Mnemonic	Name	Description
16	**SINGLEBURST**	ENABLE_SINGLE_BURST	**AHB bus will not support incr1 burst type in the future and will only affect AHB bus MSDC design, not AXI bus design.** 1'b0: HW sends incr1 burst type. 1'b1: HW sends single burst typr instead of incr1 type.
15	**RESETGDMA**	RESET_GDMA	**SW can reset GDMA when design hangs.** 1'b1: Reset GDMA 1'b0: Does not reset GDMA
13	**BIAS28R0**	BIAS_EXTBIAS_28NM	**28NM BIAS Controller register 0**
12	**BIAS28R1**	BIAS_EN18IO_28NM	**28NM BIAS Controller register 1**
11:8	**BIAS28R2**	BIAS_TUNE_28NM	**28NM BIAS Controller register 2**
7	**GETCRCMARGIN**	GET_CRC_MARGIN	**Adds margin to get CRC status when card resp CRC does not match spec 2 cycle from endbit** 1'b0: 8 cycles reserved for getting CRC status from write data CRC endbit 1'b1: 16 cycles reserved for getting CRC status from write data CRC endbit
6	**GETBUSYMARGIN**	GET_BUSY_MARGIN	**Adds margin for getting busy state of data0** 1'b0: 1 cycle reserved for getting busy state from SRC status endbit 1'b1: 3 cycles reserved for getting busy state from SRC status endbit
5:3	**CMDTA**	CMD_RSP_TA_CNTR	**CMD response turn-around period** Turn-around cycle = CMD_RSP_TA_CNTR + 2 In USH104 mode, this register should be set to 1. In non-UHS104 mode, this register should be set to 0.
2:0	**WRTA**	WRDAT_CRCS_TA_CNTR	**Write data and CRC status turn-around period** Turn-around cycle = WRDAT_CRCS_TA_CNTR + 2 In USH104 mode, this register should be set to 1. In non-UHS104 mode, this register should be set to 0.

112400B8 PATCH_BIT2 MSDC Patch Bit Register 2 14801803

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CRCSTSENSEL**			**CFGCRCSTS**	**CFGCRCSTSCNT**		**CFGCRCSTSEDGE**	**CFG_CRCSTS_SEL**	**POPENCNT**					**RESPSTSENSEL**		
Type	RW			RW	RW		RW	RW	RW					RW		
Reset	0	0	0	1	0	1	0	0	1	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CFGRESP**	**CFGRESPCNT**			**INTCRESPSEL**		**CFGRDAT**	**CFGRDATCNT**					**RESPWAITCNT**		**SUPPORT64G**	**ENHANCEGPD**
Type	RW	RW			RW		RW	RW					RW		RW	RW
Reset	0	0	0	1	1		0	0	0	0	0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
31:29	**CRCSTSENSEL**	CRCSTS_LATCH_EN_SEL	**Configures latch CRC status enable signal for async FIFO in eMMC45** 3'b000: Latch CRC status enable signal does not delay. 3'b001: Latch CRC status enable signal delays 1T msdc_ck. 3'b010: Latch CRC status enable signal delays 2T msdc_ck. 3'b011: Latch CRC status enable signal delays 3T msdc_ck. 3'b111: Latch CRC status enable signal delays 7T msdc_ck.

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Bit(s)	Mnemonic	Name	Description
28	**CFGCRCSTS**	CFG_CRCSTS	**Configures CRC status path selection** The setting only uses eMMC4.5 feature. 1'b0: Latch CRC Status select delay-line path 1'b1: Latch CRC Status select async fifo path
27:26	**CFGCRCSTSCNT**	CFG_CRCSTS_CNT	**Configures how many data are pushed in async FIFO before starting to pop out data from async FIFO** The min. register setting is 1. Do not set it to 0. The setting only uses eMMC4.5 feature. 2'b00: Push 0 data in async FIFO when starting to pop out data from async FIFO 2'b01: Push 1 data in async FIFO when starting to pop out data from async FIFO 2'b10: Push 2 data in async FIFO when starting to pop out data from async FIFO 2'b11: Push 3 data in async FIFO when starting to pop out data from async FIFO
25	**CFGCRCSTSEDGE**	CFG_CRCSTS_EDGE	**Uses rising async FIFO or falling async FIFO** 1'b0: Async FIFO latch CRC status uses rising async FIFO. 1'b1: Async fifo latch CRC status uses falling async FIFO.
24		CFG_CRCSTS_SEL	**Configures async FIFO path selection** 1'b0: Used normal path in async FIFO 1'b1: Use 2DFF path in async FIFO
23:20	**POPENCNT**	POP_EN_CNT	**Pop enable counter** Defines how many write pointer and read pointer margin begin to pop up data transfer.
18:16	**RESPSTSENSEL**	RESP_LATCH_EN_SEL	**Configures latch CMD response enable signal for async FIFO in eMMC45** 3'b000: Latch CMD response enable signal does not delay. 3'b001: Latch CMD response enable signal delays 1T msdc_ck. 3'b010: Latch CMD response enable signal delays 2T msdc_ck. 3'b011: Latch CMD response enable signal delays 3T msdc_ck. 3'b111: Latch CMD response enable signal delays 7T msdc_ck.
15	**CFGRESP**	CFG_RESP	**Configures CMD Response path selection** The setting only used eMMC4.5 feature. 1'b0: Latch CMD response selects async FIFO path. 1'b1: Latch CMD response selects delay-line path.
14:12	**CFGRESPCNT**	CFG_RESP_CNT	**Configures how many data are pushed in async FIFO before starting to pop out data from async FIFO** The min. register setting is 1. Do not set it to 0. The setting only uses eMMC4.5 feature. 3'b000: Push 0 data in async FIFO when starting to pop out data from async FIFO 3'b001: Push 1 data in async FIFO when starting to pop out data from async FIFO 3'b111: Push 7 data in async FIFO when starting to pop out data from async FIFO.
11	**INTCRESPSEL**	INTC_RESP_SEL	**Configures BREAK command async FIFO path** 1'b0: Use normal path in async FIFO 1'b1: Use 2DFF path in async FIFO
9	**CFGRDAT**	CFG_RDAT	**Configures read data path** 1'b0: Read data path bypasses delay line. 1'b1: Read data path through delay line
8:4	**CFGRDATCNT**	CFG_RDAT_CNT	**Configures read data path delay line**
3:2	**RESPWAITCNT**	RESP_WAIT_CNT	**Configures CMD response timeout** The timeout cycle is 65T+16*RESP_WAIT_CNT.

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Bit(s)	Mnemonic	Name	Description
			2'b00: CMD response timeout is 65T. 2'b01: CMD response timeout is 65T+ 16*1T. 2'b01: CMD response timeout is 65T+ 16*2T. 2'b01: CMD response timeout is 65T+ 16*3T.
1	**SUPPORT64G**	SUPPORT_64G	**Indicates which project supports high 64G DRAM space access** 1'b1: Support 64G DRAM access 1'b0: Does not support 64G DRAM access
0	**ENHANCEGPD**	ENHANCE_WAIT_GPD	**If SW clears int when GPD update has not been finished, the design will hang.** Set this bt to 1 to avoid such issue in enhance write mode. 1'b1: Use new HW code to update GPD in enhance mode 1'b0: Use old HW code

112400C0 DAT0_TUNE_CRC DAT0 Tune Result Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DAT0CRCSTS[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DAT0CRCSTS[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DAT0CRCSTS**	DAT0_CRC_STS	**SDIO auto command 53 test result register** When auto-command 53 is enabled, HW will automatically try TUNE_WINDOW times of command-53 and store CRC result of DAT0 into this register. This register contains the 1st to 32rd results in bit[0:31].

112400C4 DAT1_TUNE_CRC DAT1 Tune Result Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DAT1CRCSTS[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DAT1CRCSTS[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DAT1CRCSTS**	DAT1_CRC_STS	**SDIO auto command 53 test result register** When auto-command 53 is enabled, HW will automatically try TUNE_WINDOW times of command-53 and store CRC result of DAT1 into this register. This register contains the 1st to 32rd results in bit[0:31].

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112400C8 **DAT2_TUNE_CRC** **DAT2 Tune Result Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DAT2CRCSTS[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DAT2CRCSTS[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	DAT2CRCSTS	DAT2_CRC_STS	**SDIO auto command 53 test result register** When auto-command 53 is enabled, HW will automatically try TUNE_WINDOW times of command-53 and store CRC result of DAT2 into this register. This register contains the 1st to 32rd results in bit[0:31].

112400CC **DAT3_TUNE_CRC** **DAT3 Tune Result Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DAT3CRCSTS[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DAT3CRCSTS[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	DAT3CRCSTS	DAT3_CRC_STS	**SDIO auto command 53 test result register** When auto-command 53 is enabled, HW will automatically try TUNE_WINDOW times of command-53 and store CRC result of DAT3 into this register. This register contains the 1st to 32rd results in bit[0:31].

112400D0 **CMD_TUNE_CRC** **CMD Tune Result Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CMDCRCSTS[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CMDCRCSTS[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	CMDCRCSTS	CMD_CRC_STS	**SDIO auto command 53 test result register** When auto-command 53 is enabled, HW will automatically try TUNE_WINDOW times of command-53 and store CRC result of CMD into this register.

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Bit(s)	Mnemonic	Name	Description
			This register contains the 1st to 32rd results in bit[0:31].

112400D4 **SDIO_TUNE_WIND** **SDIO Tune Window Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name												TUNEWINDOW				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0	**TUNEWINDOW**	TUNE_WINDOW	**SDIO auto command 53 tuning window setting** Window range: 1. For CMD PAD Low bound: max(0, PAD_CMD_RXDLY-TUNE_WINDOW) High bound: min(31, PAD_CMD_RXDLY+TUNE_WINDOW) 2. For DAT PAD Low bound: max(0, DAT(0:3)_RD_DLY-TUNE_WINDOW) High bound:min(31: DAT(0:3)_RD_DLY+TUNE_WINDOW)

112400F0 **PAD_TUNE0** **MSDC Pad Tuning Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CLKTDLY					CMDRRDLY					CMDRRDLYSEL	CMDRDLY				
Type	RW					RW					RW	RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RXDLYSEL		DATRRDLYSEL	DATRRDLY					DELAYEN			DATWRDLY				
Type	RW		RW	RW					RW			RW				
Reset	0		0	0	0	0	0	0	0			0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:27	**CLKTDLY**	PAD_CLK_TXDLY	**Controls CLK pad TX delay** This register adds delay to CLK phase. Total 32 stages.
26:22	**CMDRRDLY**	PAD_CMD_RESP_RXDLY	**Controls CMD response internal delay line** This register fine-tunes response phase latched by MSDC internal clock. Total 32 stages.
21	**CMDRRDLYSEL**	PAD_CMD_RD_RXDLY_SEL	**Decides CMD response passes through data delay line 1 or not** 1'b0: Pass 1'b1: Does not pass
20:16	**CMDRDLY**	PAD_CMD_RXDLY	**Controls CMD pad RX delay line** This register fine-tunes CMD pad macro response latch timing. Total 32 stages.
15	**RXDLYSEL**	PAD_RXDLY_SEL	**Decides RX delay line tune data path or clock path**

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Bit(s)	Mnemonic	Name	Description
			1'b0: RX delay line tune data path 1'b1: RX delay line tune clock path
13	**DATRRDLYSEL**	PAD_DAT_RD_RXDLY_SEL	**Decide RX data pass through data delay line 1 or not** 1'b0: Pass 1'b1: Does not pass
12:8	**DATRRDLY**	PAD_DAT_RD_RXDLY	**Controls DAT pad RX delay line (for MSDC read only)** This register fine-tunes DAT pad macro read data latch timing. Total 32 stages.
7	**DELAYEN**	DELAY_EN	**Enables all delay cell toggle when power is on** 1'b0: Disable delay cell toggle default 1'b1: Enable delay cell toggle default
4:0	**DATWRDLY**	PAD_DAT_WR_RXDLY	**Controls write data status internal delay line** This register fine-tunes write status phase latched by MSDC internal clock. Total 32 stages.

112400F4 PAD_TUNE1 MSDC Pad Tuning Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CMDRRDLY2SEL	CMDRDLY2				
Type											RW	RW				
Reset											0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name			DATRRDLY2SEL	DATRRDLY2												
Type			RW	RW												
Reset			0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
21	**CMDRRDLY2SEL**	PAD_CMD_RD_RXDLY2_SEL	**Decides CMD response passes through data delay line 2 or not** 1'b0: Pass 1'b1: Does not pass
20:16	**CMDRDLY2**	PAD_CMD_RXDLY2	**Controls CMD pad RX delay line 2** This register fine-tunes CMD pad macro response latch timing in data path. Total 32 stages.
13	**DATRRDLY2SEL**	PAD_DAT_RD_RXDLY2_SEL	**Decides RX data pass through data delay line 2 or not** 1'b0: Pass 1'b1: Does not pass
12:8	**DATRRDLY2**	PAD_DAT_RD_RXDLY2	**Controls DAT pad RX delay line 2 (for MSDC read only)** This register fine-tunes DAT pad macro read data latch timing. Total 32 stages.

112400F8 DAT_RD_DLY0 MSDC Data Delay Line Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT0RDDLY								DAT1RDDLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DAT2RDDLY								DAT3RDDLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	DAT0RDDLY	DAT0_RD_DLY	**Controls DAT0 pad RX delay line (for MSDC RD)** Total 32 stages.
20:16	DAT1RDDLY	DAT1_RD_DLY	**Controls DAT1 pad RX delay line (for MSDC RD)** Total 32 stages.
12:8	DAT2RDDLY	DAT2_RD_DLY	**Controls DAT2 pad RX delay line (for MSDC RD)** Total 32 stages.
4:0	DAT3RDDLY	DAT3_RD_DLY	**Controls DAT3 pad RX delay line (for MSDC RD)** Total 32 stages.

112400FC **DAT_RD_DLY1** **MSDC Data Delay Line Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT4RDDLY								DAT5RDDLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DAT6RDDLY								DAT7RDDLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	DAT4RDDLY	DAT4_RD_DLY	**Controls DAT4 pad RX delay line (for MSDC RD)** Total 32 stages.
20:16	DAT5RDDLY	DAT5_RD_DLY	**Controls DAT5 pad RX delay line (for MSDC RD)** Total 32 stages.
12:8	DAT6RDDLY	DAT6_RD_DLY	**Controls DAT6 pad RX delay line (for MSDC RD)** Total 32 stages.
4:0	DAT7RDDLY	DAT7_RD_DLY	**Controls DAT7 pad RX delay line (for MSDC RD)** Total 32 stages.

11240100 **DAT_RD_DLY2** **MSDC Data Delay Line Register 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT0RDDLY2								DAT1RDDLY2				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DAT2RDDLY2								DAT3RDDLY2				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	DAT0RDDLY2	DAT0_RD_DLY2	**Controls DAT0 pad RX delay line 2 (for MSDC RD)**

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Bit(s)	Mnemonic	Name	Description
			Total 32 stages.
20:16	**DAT1RDDLY2**	DAT1_RD_DLY2	**Controls DAT1 pad RX delay line 2 (for MSDC RD)** Total 32 stages.
12:8	**DAT2RDDLY2**	DAT2_RD_DLY2	**Controls DAT2 pad RX delay line 2 (for MSDC RD)** Total 32 stages.
4:0	**DAT3RDDLY2**	DAT3_RD_DLY2	**Controls DAT3 pad RX delay line 2 (for MSDC RD)** Total 32 stages.

11240104 DAT_RD_DLY3 MSDC Data Delay Line Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT4RDDLY2								DAT5RDDLY2				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DAT6RDDLY2								DAT7RDDLY2				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	**DAT4RDDLY2**	DAT4_RD_DLY2	**Controls DAT4 pad RX delay line 2 (for MSDC RD)** Total 32 stages.
20:16	**DAT5RDDLY2**	DAT5_RD_DLY2	**Controls DAT5 pad RX delay line 2 (for MSDC RD)** Total 32 stages.
12:8	**DAT6RDDLY2**	DAT6_RD_DLY2	**Controls DAT6 pad RX delay line 2 (for MSDC RD)** Total 32 stages.
4:0	**DAT7RDDLY2**	DAT7_RD_DLY2	**Controls DAT7 pad RX delay line 2 (for MSDC RD)** Total 32 stages.

11240110 HW_DBG_SEL MSDC H/W Debug Selection Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DBGWSEL	DBG3SEL						DBG2SEL							
Type		RW	RW						RW							
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DBG1SEL						DBG0SEL							
Type			RW						RW							
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30	**DBGWSEL**	HW_DBG_WRAP_SEL	**Selects HW debug output for wrapper** 0: Select original debug pins 1: Select wrapper debug pins
29:24	**DBG3SEL**	HW_DBG3_SEL	**Selects HW debug output**
23:16	**DBG2SEL**	HW_DBG2_SEL	**Selects HW debug output**

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Bit(s)	Mnemonic	Name	Description
13:8	**DBG1SEL**	HW_DBG1_SEL	**Selects HW debug output**
7:0	**DBG0SEL**	HW_DBG0_SEL	**Selects HW debug output**

11240114 **MAIN_VER** **MSDC Main Version Register** **20140512**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAINVER[31:16]															
Type	RO															
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAINVER[15:0]															
Type	RO															
Reset	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
31:0	**MAINVER**	MAIN_VER	Main version

11240118 **ECO_VER** **MSDC ECO Version Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ECOVER[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ECOVER[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ECOVER**	ECO_VER	ECO version

Module name: MSDC2 Base address: (+11250000h)

Address	Name	Width	Register Function
11250000	MSDC_CFG	32	**MSDC Configuration Register** For general configuration of the MS/SD controller
11250004	MSDC_IOCON	32	**MSDC IO Configuration Register** Contains the receiver path data latch timing control and interface control bits
11250008	MSDC_PS	32	**MSDC Pin Status Register** Stores card detection and write protection pin status. Card detection status can be disabled.
1125000C	MSDC_INT	32	**MSDC Interrupt Register** Contains the status of interrupts Note: The register still shows the status of interrupt even though the interrupt is disabled.
11250010	MSDC_INTEN	32	**MSDC Interrupt Enable Register** Contains related enabling bit of interrupts
11250014	MSDC_FIFOCS	32	**MSDC FIFO Control and Status Register** Contains control and status of embedded 128B FIFO
11250018	MSDC_TXDAT	32	**MSDC TX Data Port Register**

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Address	Name	Width	Register Function
	A		For PIO mode only. Used to input MSDC write data to card. The access can be AHB1B/2B/4B.
1125001C	MSDC_RXDATA	32	**MSDC RX Data Port Register** For PIO mode only. Used to read back MSDC read data from card. The access can be AHB1B/2B/4B.
11250030	SDC_CFG	32	**SD Configuration Register** Configures MS/SD memory card controller when it is configured as the host of SD memory card. If the controller is configured as the host of memory stick, the contents of the register will have no impact on the operation of the controller.
11250034	SDC_CMD	32	**SD Command Register** Defines a SD memory card command and its attributes. Before MS/SD controller issues a transaction onto SD bus, the application should specify other relative settings such as argument for command. After writing the register by the application, MS/SD controller will issue the corresponding transaction onto SD serial bus. If the command is GO_IDLE_STATE, the controller will have serial clock on SD/MMC bus running 128 cycles before issuing the command.
11250038	SDC_ARG	32	**SD Argument Register** Contains argument of SD/MMC memory card command
1125003C	SDC_STS	32	**SD Status Register** Reflects SD bus status and contains MMC stream write status
11250040	SDC_RESP0	32	**SD Response Register 0** Contains parts of the last SD/MMC memory card bus response. See description in register field SDC_RESP3.
11250044	SDC_RESP1	32	**SD Response Register 1** Contains parts of the last SD/MMC memory card bus response. See description in register field SDC_RESP3.
11250048	SDC_RESP2	32	**SD Response Register 2** Contains parts of the last SD/MMC memory card bus response. See description in register field SDC_RESP3.
1125004C	SDC_RESP3	32	**SD Response Register 3** Contains parts of the last SD/MMC memory card bus response. Register fields SDC_RESP0, SDC_RESP1, SDC_RESP2 and SDC_RESP3 are composed of the last SD/MMC memory card bus response. For response of type R2, i.e. response of the command ALL_SEND_CID, SEND_CSD and SEND_CID, only bit 127 to 0 of response token are stored in register field SDC_RESP0, SDC_RESP1, SDC_RESP2 and SDC_RESP3. SDC_RESP0 = bit 31~0 SDC_RESP1 = bit 63~32 SDC_RESP2 = bit 95~64 SDC_RESP3 = bit 127~96 For response of type R1b in auto CMD12 or R1 in auto CMD23, bit 39 to 8 of response token are stored in register field of SDC_RESP3. For the responses of other types, only bit 39 to 8 of response token are stored in the register field SDC_RESP0.
11250050	SDC_BLK_NUM	32	**SD Block Number Register** Defines block number for block transaction. For single read/write, this register should be set to 1. For multiple read/write, this register should be set to bigger than 1. Set to 0 will cause unexpected result.
11250054	SDC_VOL_CHG	32	**SD Voltage Change Wait Time Register** Defines SD voltage change check wait time.
11250058	SDC_CSTS	32	**SD Card Status Register** After commands with R1 and R1b response, this register will contain the status of the SD/MMC card.
1125005C	SDC_CSTS_EN	32	**SD Card Status Enable Register**

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Address	Name	Width	Register Function
			Controls which bit of SDC_CSTS will generate the MSDC_INT.SD_CSTA interrupt
11250060	**SDC_DATCRC_STS**	32	**SD Card Data CRC Status Register** Reflects CRC status of data line[7:0]. Only for MSDC read.
11250080	**SD_ACMD_RESP**	32	**SD ACMD Response Register** Stores response of auto command from SD card
11250084	**SD_ACMD19_TRG**	32	**SD ACMD19 Target Register** Selects target delay line to run ACMD19 sequence
11250088	**SD_ACMD19_STS**	32	**SD ACMD19 Status Register** Stores result of auto command 19 from SD card
1125008C	**DMA_SA_HIGH4BIT**	32	**DMA Current Address Register of high 4bit** Contains start address high 4 bits of the 36-bit address for 64G DRAM access
11250090	**DMA_SA**	32	**DMA Start Address Register** Contains start address of DMA descriptor
11250094	**DMA_CA**	32	**DMA Current Address Register** Contains current DMA address
11250098	**DMA_CTRL**	32	**DMA Control Register** Controls DMA operation
1125009C	**DMA_CFG**	32	**DMA Configuration Register** Configures DMA operation
112500A0	**SW_DBG_SEL**	32	**MSDC S/W Debug Selection Register** Selects SW debugging output
112500A4	**SW_DBG_OUT**	32	**MSDC S/W Debug Output Register** Shows selected debugging output
112500A8	**DMA_LENGTH**	32	**DMA Length Register** Sets up basic DMA operation length
112500B0	**PATCH_BIT0**	32	**MSDC Patch Bit Register 0** Configures patch function. For normal function, this bit should be kept at default value.
112500B4	**PATCH_BIT1**	32	**MSDC Patch Bit Register 1** Configures patch function. For normal function, this bit should be kept at default value.
112500B8	**PATCH_BIT2**	32	**MSDC Patch Bit Register 2** Configures patch function. For normal function, this bit should be kept at default value.
112500C0	**DAT0_TUNE_CRC**	32	**DAT0 Tune Result Register** Records on-line tuning result for DAT0 line
112500C4	**DAT1_TUNE_CRC**	32	**DAT1 Tune Result Register** Records on-line tuning result for DAT1 line
112500C8	**DAT2_TUNE_CRC**	32	**DAT2 Tune Result Register** Records on-line tuning result for DAT2 line
112500CC	**DAT3_TUNE_CRC**	32	**DAT3 Tune Result Register** Records on-line tuning result for DAT3 line
112500D0	**CMD_TUNE_CRC**	32	**CMD Tune Result Register** Records on-line tuning result for CMD line
112500D4	**SDIO_TUNE_WIND**	32	**SDIO Tune Window Register 0** Defines tuning window size for SDIO on-line CRC tuning feature
112500F0	**PAD_TUNE0**	32	**MSDC Pad Tuning Register 0** Configures delay line embedded in pad macro
112500F4	**PAD_TUNE1**	32	**MSDC Pad Tuning Register 1** Configures delay line embedded in pad macro

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Address	Name	Width	Register Function
112500F8	DAT_RD_DLY0	32	**MSDC Data Delay Line Register 0** Configures delay line embedded in pad macro
112500FC	DAT_RD_DLY1	32	**MSDC Data Delay Line Register 1** Configures delay line embedded in pad macro
11250100	DAT_RD_DLY2	32	**MSDC Data Delay Line Register 2** Configures delay line embedded in pad macro
11250104	DAT_RD_DLY3	32	**MSDC Data Delay Line Register 3** Configures delay line embedded in pad macro
11250110	HW_DBG_SEL	32	**MSDC H/W Debug Selection Register** Selects HW debug output
11250114	MAIN_VER	32	**MSDC Main Version Register** Shows the version code of MSDC IP
11250118	ECO_VER	32	**MSDC ECO Version Register** Shows the ECO version code of MSDC IP

11250000 MSDC_CFG MSDC Configuration Register 02000099

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SCLK STOP SEL				CCKMD		CCKDIV[11:8]			
Type							RW				RW		RW			
Reset							1				0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CCKDIV[7:0]								CCKSB	BV18PSS	BV18SDT	CCKDRVE	PIO	RST	CCKPD	MSDC
Type	RW								RU	RU	RW	RW	RW	A0	RW	RW
Reset	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1

Bit(s)	Mnemonic	Name	Description
25	SCLKSTOP SEL	SCLK_STOP_SEL	**In DDR mode, stops SCLK when device is idle whether checking SCLK phase or not** 1'b0: Stop sclk not checking SCLK phase 1'b1: Stop sclk checking SCLK phase; fix 1/4T sclk glitch in DDR mode
21:20	CCKMD	CARD_CK_MODE	**MS/SD card clock mode** 2'b00: Use clock divider output divided by msdc_src_ck as msdc_ck. bit[15]~bit[8] should be programmed. 2'b01: Use msdc_src_ck as msdc_ck. bit[15]~bit[8] is ignored. 2'b10: DDR mode; use clock divider output divided by msdc_src_ck as msdc_ck. bit[15]~bit[8] should be programmed. 2'b11: HS400 mode; use clock divider output and use msdc_src_ck as msdc_ck. bit[15]~bit[8] should be programmed.
19:8	CCKDIV	CARD_CK_DIV	**MS/SD card clock divider** Controls clock frequency of serial clock on MS/SD bus. Refer to "Data Line Latching Timing Diagram" and "Response Latching Timing Diagram". For non-DDR mode, msdc_ck equals SD bus clock. (Example: For SDR25 or HS, msdc_ck and SD bus clock will be 50MHz) For DDR mode, msdc_ck denotes MSDC internal clock which will be doubled to SD bus clock. (Example: For DDR50, msdc_ck should be set to 100MHz, and bus clock will be 50MHz.) 8'b00000000: msdc_ck =(1/2)*msdc_src_ck 8'b00000001: msdc_ck = [1/(4*1)]*msdc_src_ck 8'b00000010: msdc_ck = [1/(4*2)]*msdc_src_ck 8'b00000011: msdc_ck = [1/(4*3)]*msdc_src_ck 8'b00010000: msdc_ck = [1/(4*16)]*msdc_src_ck

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Bit(s)	Mnemonic	Name	Description
			8'b11111111: msdc_ck = [1/(4*255)]*msdc_src_ck
7	**CCKSB**	CARD_CK_STABLE	**MS/SD card clock is stable or not** After programming CARD_CK_MODE or CARD_CK_DIV, this bit will immediately become 0 and return to 1 if stable. Poll this register to ensure safety control of MSDC. 1'b0: Clock output is not stable. 1'b1: Clock output is stable.
6	**BV18PSS**	BV_1P8_PASS	**MSDC bus voltage 1.8V detection status** SW should check this bit after BUS_VOL_18V_START_DET turns to 0 from 1. 1'b0: Error in voltage detection 1'b1: No error in voltage detection
5	**BV18SDT**	BV_1P8_START_DET	**MSDC bus voltage 1.8V detection sequence start event** SW writes 1 to this bit to trigger HW outputting 1.8V clock for 1ms and automatically detecting CMD/DAT line sequence for voltage change is passed or not. HW will clear this bit to 0 after the detection is finished. The passed or failed status is stored in bit[6] BUS_VOL_18V_PASS.
4	**CCKDRVE**	CARD_CK_DRV_EN	**SD/MS card bus clock drive enable bit** Set this bit to 1 to enable MSDC bus clock driver. The default bus state depends on MSDC_CFG][1] CARD_CK_PWDN bit. If MSDC_CFG[1] CARD_CK_PWDN=1, the default clock state will be free running. If MSDC_CFG[1] CARD_CK_PWDN=0, the default clock state will be gated to 0. Set this bit to 0 will put the bus state into "tri-state". Default: 1 1'b0: Put the clock pad into tri-state 1'b1: Enable MSDC to drive clock pad. The state of CLK depends on MSDC_CFG[1] CARD_CK_PWDN.
3	**PIO**	PIO_MODE	**MS/SD PIO mode** Selects PIO mode. Default: PIO mode
2	**RST**	RST	**Software reset** Writing 1 to this register will cause internal synchronous reset of MS/SD controller, and it will not reset register settings and DMA controller. The reset sequence is done when this bit becomes 0. SW should wait for this bit to return to 0 after writing 1. 1'b0: MS/SD controller is not in reset state. 1'b1: MS/SD controller is in reset state.
1	**CCKPD**	CARD_CK_PWDN	**MSDC bus clock power-down mode** Controls card clock power-down mode 1'b0: Clock is gated to 0 if no command or data is transmitted. 1'b1: Clock is free running even if no command or data is transmitted. (The clock may still be stopped when MSDC write data are not enough or no space for the next read data.)
0	**MSDC**	MSDC	**Selects MS/SD mode** Configures the controller to be the host of memory stick or host of SD/MMC memory card. The default value is configuring the controller as the host of memory stick. 1'b0: Configure controller to be host of memory stick 1'b1: Configure controller to be host of SD/MMC memory card

11250004 MSDC_IOCON MSDC IO Configuration Register 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									RD7SPL	RD6SPL	RD5SPL	RD4SPL	RD3SPL	RD2SPL	RD1SPL	RD0SPL
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			WD3SPL	WD2SPL	WD1SPL	WD0SPL	WDSPLSEL	WDSPL			RDSPLSEL	DDR50CKD	DDLSEL	RDSPL	RSPL	SDR104CKS
Type			RW	RW	RW	RW	RW	RW			RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23	**RD7SPL**	R_D7_SMPL	**Selects read data 7 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
22	**RD6SPL**	R_D6_SMPL	**Selects read data 6 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
21	**RD5SPL**	R_D5_SMPL	**Selects read data 5 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
20	**RD4SPL**	R_D4_SMPL	**Selects read data 4 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
19	**RD3SPL**	R_D3_SMPL	**Selects read data 3 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
18	**RD2SPL**	R_D2_SMPL	**Selects read data 2 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
17	**RD1SPL**	R_D1_SMPL	**Selects read data 1 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
16	**RD0SPL**	R_D0_SMPL	**Selects read data 0 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
13	**WD3SPL**	W_D3_SMPL	**Selects SDIO interrupt sample** Only valid when bit 9 is on. 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
12	**WD2SPL**	W_D2_SMPL	**Selects SDIO interrupt sample** Only valid when bit 9 is on. 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
11	**WD1SPL**	W_D1_SMPL	**Selects SDIO interrupt sample** Only valid when bit 9 is on. 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge

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Bit(s)	Mnemonic	Name	Description
10	**WD0SPL**	W_D0_SMPL	**Selects CRC status and SDIO interrupt sample** Only valid when bit 9 is on. 1'b0: Sample CRC Status and SDIO interrupt by external bus clock rising edge 1'b1: Sample CRC Status and SDIO interrupt by external bus clock falling edge
9	**WDSPLSEL**	W_D_SMPL_SEL	**Selects data line rising/falling latch fine-tuning in write transaction** 1'b0: All data line share one value indicated by MSDC_IOCON.W_D_SMPL 1'b1: Each data line has its own selection value indicated by Data line 0: MSDC_IOCON.W_D0_SMPL Data line 1: MSDC_IOCON.W_D1_SMPL Data line 2: MSDC_IOCON.W_D2_SMPL Data line 3: MSDC_IOCON.W_D3_SMPL
8	**WDSPL**	W_D_SMPL	**Selects CRC status and SDIO interrupt sample** 1'b0: Sample CRC Status and SDIO interrupt by external bus clock rising edge 1'b1: Sample CRC Status and SDIO interrupt by external bus clock falling edge
5	**RDSPLSEL**	R_D_SMPL_SEL	**Selects data line rising/falling latch fine-tuning in read transaction** 1'b0: All data line share one value indicated by MSDC_IOCON.R_D_SMPL 1'b1: Each data line has its own selection value indicated by Data line 0: MSDC_IOCON.R_D0_SMPL Data line 1: MSDC_IOCON.R_D1_SMPL Data line 2: MSDC_IOCON.R_D2_SMPL Data line 3: MSDC_IOCON.R_D3_SMPL Data line 4: MSDC_IOCON.R_D4_SMPL Data line 5: MSDC_IOCON.R_D5_SMPL Data line 6: MSDC_IOCON.R_D6_SMPL Data line 7: MSDC_IOCON.R_D7_SMPL
4	**DDR50CKD**	DDR50_DLY_SEL	**Selects DDR50 output clock delay** 1'b0: Use default clock output 1'b1: Delay 1T msdc_src_ck for clock output
3	**DDLSEL**	D_DLYLINE_SEL	**Selects data line delay line fine-tuning** 1'b0: All data line share one delay selection value indicated by PAD_TUNE.PAD_DAT_RD_RXDLY 1'b1: Each data line has its own delay selection value indicated by Data line 0: DAT_RD_DLY0.DAT0_RD_DLY Data line 1: DAT_RD_DLY0.DAT1_RD_DLY Data line 2: DAT_RD_DLY0.DAT2_RD_DLY Data line 3: DAT_RD_DLY0.DAT3_RD_DLY Data line 4: DAT_RD_DLY1.DAT4_RD_DLY Data line 5: DAT_RD_DLY1.DAT5_RD_DLY Data line 6: DAT_RD_DLY1.DAT6_RD_DLY Data line 7: DAT_RD_DLY1.DAT7_RD_DLY
2	**RDSPL**	R_D_SMPL	**Selects read data sample** 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
1	**RSPL**	R_SMPL	**Selects command response sample** 1'b0: Sample response by external bus clock rising edge 1'b1: Sample response by external bus clock falling edge
0	**SDR104CKS**	SDR104_CLK_SEL	**SDR104 SCLK output clock control** Only used when MSDC_CFG[17:16] CARD_CK_MODE is 2'b01. 1'b0: Bus clock output equals inverted msdc_src_ck 1'b1: Bus clock output equals msdc_src_ck

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11250008 MSDC_PS MSDC Pin Status Register 01FF0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SDWP							CMD	DAT							
Type	RU							RU	RU							
Reset	0							1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDDBCE														CDSTS	CDEN
Type	RW														RU	RW
Reset	0	0	0	0											1	0

Bit(s)	Mnemonic	Name	Description
31	**SDWP**	SD_WP	**Write Protection switch status on SD memory card** Shows the status of Write Protection switch on SD memory card. There is no default reset value. The pin WP (Write Protection) is only useful when the controller is configured for SD memory card. 1'b0: Write Protection switch on, i.e. memory card will be write-protected. 1'b1: Write Protection switch off, i.e. memory card is writable.
24	**CMD**	CMD	**Command line status** Reflects the command line value of MSDC bus.
23:16	**DAT**	DAT	**Data line status** Reflects the data line value of MSDC bus (8-bit).
15:12	**CDDBCE**	CDDEBOUNCE	**Card detection de-bounce timer** Specifies the time interval for card detection de-bounce. Default value: 0, meaning the de-bounce interval is one 32kHz cycle. The interval will extend one cycle time of 32kHz by increasing the counter by 1.
1	**CDSTS**	CDSTS	**Card detection status** 1'b0: Card detection pin status is logic low. 1'b1: Card detection pin status is logic high.
0	**CDEN**	CDEN	**Enables card detection** Controls the card detection circuit. 1'b0: Disable card detection 1'b1: Enable card detection

1125000C MSDC_INT MSDC Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										AC53FAIL	AC53DONE	GEAROUTBOUND	DMAPROTECT	GPDCSERR	BDCSERR	AC19DONE
Type										W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SDDCRCERR	SDDTO	DMAXFDNE	SDXFCPL	SDCSTS	SDRCRCERR	SDCTO	SDCRDY	SDIOIRQ	DMAQEPTY	SDACDRCRCERR	SDACDCTO	SDACDCRDY		MSDCCDSC	MMCIRQ
Type	W1C	W1C	W1C	W1C	RU	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C		W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0

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Bit(s)	Mnemonic	Name	Description
22	**AC53FAIL**	AUTOCMD53_FAIL	**SD auto command 53 status register** When auto-command 53 tuning sequence fails , this register will be set to 1 by HW.
21	**AC53DONE**	AUTOCMD53_DONE	**SD auto command 53 status register** When auto-command 53 tuning sequence is finished, this register will be set to 1 by HW.
20	**GEAROUTBOUND**	GEAR_OUT_BOUND	**The gear setting of delay line is out of boundary in the process of SDIO Autocmd 53 On-Line tuning**
19	**DMAPROTECT**	DMA_PROTECT	**There is write operation to DMA start address, length, start bit or the last BUF bit.**
18	**GPDCSERR**	GPD_CS_ERR	**GPD checksum error detected**
17	**BDCSERR**	BD_CS_ERR	**BD checksum error detected**
16	**AC19DONE**	AUTOCMD19_DONE	**SD auto command 19 status register** When auto-command 19 is enabled, HW will clear this register to 0. As the tuning sequence is finished (32 times), this register will be set to 1 by HW. SW should check AUTOCMD_STS0 and SUTOCMD_STS1 only when this bit is on.
15	**SDDCRCERR**	SD_DATA_CRCERR	1'b0: Otherwise 1'b1: MS/SD controller detects a CRC error after reading a block of data from the DAT line or SD/MMC signals a CRC error after writing a block of data to the DAT line.
14	**SDDTO**	SD_DATTO	
13	**DMAXFDNE**	DMA_XFER_DONE	**DMA transfer done interrupt** Indicates status of data block transfer. 1'b0: Otherwise 1'b1: A data block is successfully transferred.
12	**SDXFCPL**	SD_XFER_COMPLETE	**SD data transfer completed interrupt** Indicates transaction which contains data that are completed. While performing tuning procedure (Execute Tuning is set to 1), SD_XFER_COMPLETE is not set to 1.
11	**SDCSTS**	SD_CSTS	**SD CSTA update interrupt** Indicates any bit in register SDC_CSTA is active. The register bit will be set to 1. SW should clear SDC_CSTA, and this bit will be de-asserted automatically.
10	**SDRCRCER**	SD_RESP_CRCERR	**SD command CRC error interrupt** Indicates SD/MMC controller detects a CRC error after reading a response from the CMD line. 1'b0: Otherwise 1'b1: SD/MMC controller detects a CRC error after reading a response from the CMD line.
9	**SDCTO**	SD_CMDTO	**SD command time-out interrupt** Indicates SD/MMC controller detects a time-out condition while waiting for a response on the CMD line. 1'b0: Otherwise 1'b1: SD/MMC controller detects a time-out condition while waiting for a response on the CMD line.
8	**SDCRDY**	SD_CMDRDY	**SD command ready interrupt** For the command without response, the register bit will be 1 once the command is completed on SD/MMC bus. For command with response without busy, the register bit will be 1 whenever the command is issued onto SD/MMC bus and its corresponding response is received without CRC error. For command with response with busy in DAT0, the register bit will be 1 whenever the command is issued onto SD/MMC bus and its

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Bit(s)	Mnemonic	Name	Description
			corresponding response is received without CRC error and the DAT0 transited from busy to idle. 1'b0: Otherwise 1'b1: Command finished successfully without CRC error.
7	**SDIOIRQ**	SD_SDIOIRQ	**SD SDIO interrupt** Indicates the interrupt is sensed in the SDIO bus. 1'b0: No interrupt on SDIO bus 1'b1: Interrupt on SDIO bus
6	**DMAQEPTY**	DMA_Q_EMPTY	**DMA queue empty interrupt** Indicates the current DMA queue is empty. Only for descriptor mode and enhance mode.
5	**SDACDRCRCER**	SD_AUTOCMD_RESP_CRCERR	**SD auto command CRC error interrupt** Set when detecting a CRC error in the auto command response.
4	**SDACDCTO**	SD_AUTOCMD_CMDTO	**SD auto command time-out interrupt** Set if no response is returned within a specified cycles (64T in spec) from the end bit of auto command.
3	**SDACDCRDY**	SD_AUTOCMD_CMDRDY	**SD auto command ready interrupt** Set if auto command is executed without CRC error or timeout.
1	**MSDCCDSC**	MSDC_CDSC	**MSDC card detection status change interrupt** Indicates if any interrupt for memory card insertion/removal exists. Whenever memory card is inserted or removed and card detection circuit is enabled, i.e. register bit CDEN in register MSDC_PS is set to 1, the register bit will be set to 1. It will be reset when the register is read. 1'b0: Otherwise 1'b1: Card is inserted or removed.
0	**MMCIRQ**	MMC_IRQ	**MMC card interrupt** 1'b0: Otherwise 1'b1: MMC card interrupt event occurs.

11250010 **MSDC_INTEN** **MSDC Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										ENAC53FAIL	ENAC53DONE	ENGEAROUTBOUND	ENDMAPROTECT	ENGPDCSERR	ENBDCSERR	ENAC19DONE
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENSDDCRCERR	ENSDDTO	ENDMAXFDNE	ENSDXFCPL	ENSDCSTA	ENSDRCRCER	ENSDCTO	ENSDCRDY	ENSDIOIRQ	ENDMAQEPTY	ENSDACDRCRCER	ENSDACDCTO	ENSDACDCRDY		ENMSDCCDSC	ENMCIRQ
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0

Bit(s)	Mnemonic	Name	Description
22	**ENAC53FAIL**	EN_AUTOCMD53_FAIL	**Enables auto-command 53 failure interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
21	**ENAC53DONE**	EN_AUTOCMD53_DONE	**Enables auto-command 53 completed interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
20	**ENGEARO**	EN_GEAR_OUT_B	**Enables gear out boundary interrupt**

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Bit(s)	Mnemonic	Name	Description
	UTBOUND	OUND	1'b0: Disable interrupt 1'b1: Enable interrupt
19	ENDMAPROTECT	EN_DMA_PROTECT	**Enables DMA protection interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
18	ENGPDCSERR	EN_GPD_CS_ERR	**Enables GPD checksum error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
17	ENBDCSERR	EN_BD_CS_ERR	**Enables BD checksum error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
16	ENAC19DONE	EN_AUTOCMD19_DONE	**Enables auto-command 19 completed interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
15	ENSDDCRCERR	EN_SD_DATA_CRCERR	**Enables SD data CRC error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
14	ENSDDTO	EN_SD_DATTO	**Enables SD data timeout interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
13	ENDMAXFDNE	EN_SD_DMA_XFER_DONE	**Enables DMA transfer done interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
12	ENSDXFCPL	EN_SD_XFER_COMPLETE	**Enables SD data transfer completed interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
11	ENSDCSTA	EN_SD_CSTA	**Enables SD CSTA update interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
10	ENSDRCRCER	EN_SD_RESP_CRCERR	**Enables SD command CRC error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
9	ENSDCTO	EN_SD_CMDTO	**Enables SD command timeout interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
8	ENSDCRDY	EN_SD_CMDRDY	**Enables SD command ready interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
7	ENSDIOIRQ	EN_SD_SDIOIRQ	**Enables SD SDIO interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
6	ENDMAQEPTY	EN_DMA_Q_EMPTY	**Enables DMA queue empty interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
5	ENSDACDRCRCER	EN_SD_AUTOCMD_RESP_CRCERR	**Enables SD auto command CRC error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
4	ENSDACDCTO	EN_SD_AUTOCMD_CMDTO	**Enables SD auto command time-out interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
3	ENSDACDCRDY	EN_AUTOCMD_CMDRDY	**Enables SD auto command ready interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt

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Bit(s)	Mnemonic	Name	Description
1	**ENMSDCC DSC**	EN_MSDC_CDSC	**Enables MSDC card detection status change interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
0	**ENMMCIR Q**	EN_MMC_IRQ	**Enables MMC card interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt

11250014 MSDC_FIFOCS MSDC FIFO Control and Status Register 7C000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**FIFO CLR**	**FIFO**							**TXFIFOCNT**							
Type	A0	A0							RU							
Reset	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**RXFIFOCNT**							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**FIFOCLR**	FIFOCLR	**Clears embedded FIFO** Write 1 to this bit to clear FIFO. It will become 0 when FIFO is cleared. SW needs to check this bit to make sure clearing FIFO sequence is done. This bit can be used when the data read/write sequence has error and needs to clean the HW FIFO.
30:24	**FIFO**	FIFO	
23:16	**TXFIFOCN T**	TXFIFOCNT	**TX FIFO count for MSDC write** 8'd0: No data in FIFO 8'd1: 1 byte of data in FIFO 8'd2: 2 bytes of data in FIFO 8'd131: Maximum 131 bytes of data in FIFO Others: Reserved
7:0	**RXFIFOCN T**	RXFIFOCNT	**RX FIFO count for MSDC read** 8'd0: No data in FIFO 8'd1: 1 byte of data in FIFO 8'd2: 2 bytes of data in FIFO 8'd131: Maximum 131 bytes of data in FIFO Others: Reserved

11250018 MSDC_TXDATA MSDC TX Data Port Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**PIOTXDATA[31:16]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**PIOTXDATA[15:0]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31:0	**PIOTXDATA**	PIO_TXDATA	**PIO mode TXDATA port** This register can be accessed by byte, half-word or word. This port can only be accessed in PIO mode. Otherwise, the transaction will be discarded.

1125001C **MSDC_RXDATA** **MSDC RX Data Port Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**PIORXDATA[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**PIORXDATA[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**PIORXDATA**	PIO_RXDATA	**PIO mode RXDATA port** This register can be accessed by byte, half-word or word. This port can only be accessed in PIO mode. Otherwise, the transaction will be discarded.

11250030 **SDC_CFG** **SD Configuration Register** **00100000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DTOC**										**INTBGP**	**SDIOIDE**	**SDIO**		**BUSWD**	
Type	RW										RW	RW	RW		RW	
Reset	0	0	0	0	0	0	0	0			0	1	0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**ENWKUPINS**	**ENWKUPSDIOINT**
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DTOC**	DTOC	**Data timeout counter** The period from the end of the initial host read command or the last read data block in a multiple block read operation to the start bit of the next read data block requires at least two serial clock cycles. The counter is used to extend the period (Read Data Access Time) in unit of 1,048,576 serial clocks. 8'b00000000: Extend 1,048,576 more serial clock cycles 8'b00000001: Extend 1,048,576*2 more serial clock cycles 8'b00000010: Extend 1,048,576*3 more serial clock cycles 8'b11111111: Extend 1,048,576*256 more serial clock cycles
21	**INTBGP**	INT_AT_BLOCK_GAP	**Interrupt at block gap** This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Set to 1 will enable interrupt detection at the block gap for a multiple block transfer. Set to 0 will disable interrupt detection during a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this

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Bit(s)	Mnemonic	Name	Description
			bit should be set to 0. When the host driver detects an SD card insertion, it will set up this bit according to CCCR of the SDIO card. 1'b0: Disable interrupt detection at block gap 1'b1: Enable interrupt detection at block gap
20	**SDIOIDE**	SDIO_INT_DET_EN	**Enables SDIO interrupt detection** Informs SD controller to sense SDIO interrupt. 1'b0: Disable SDIO interrupt detection 1'b1: Enable SDIO interrupt detection if SDIO bit is also on
19	**SDIO**	SDIO	**SDIO mode enable bit** Enables support to sense SDIO interrupt and disables R4 response CRC check for SDIO card. 1'b0: Disable SDIO mode 1'b1: Enable SDIO mode
17:16	**BUSWD**	BUSWIDTH	**Configures bus width** Defines SD/MMC bus width. 2'b00: 1-bit mode 2'b01: 4-bit mode 2'b10: 8-bit mode 2'b11: Reserved
1	**ENWKUPINS**	WAKEUP_INS_EN	**Card status change wakeup event enable bit** 1'b0: Disable wakeup event for card status change 1'b1: Enable wakeup event for card status change
0	**ENWKUPSDIOINT**	WAKEUP_SDIOINT_EN	**SDIO card interrupt wakeup event enable bit** 1'b0: Disable wakeup event for SDIO card interrupt 1'b1: Enable wakeup event for SDIO card interrupt

11250034 SDC_CMD SD Command Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ACMD53	VOLSWTH	ACMD		LEN											
Type	RW	RW	RW		RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GOIRQ	STOP	RW	DTYPE			RSPTYP			BREAK	CMD					
Type	RW	RW	RW	RW			RW			RW	RW					
Reset	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**ACMD53**	AUTO_CMD53	**Enables auto command 53** Should be used exclusively with AUTO_CMD, meaning AUTO_CMD != 2'b00. This field should be assigned to 1'b0. If this filed is assigned to 1'b1, AUTO_CMD should be set to 2'b00. 1'b0: Disable Auto Command 53 1'b1: Enable Auto Command 53
30	**VOLSWTH**	VOL_SWTH	**Voltage switch command** 1'b0: Disable voltage switch detection 1'b1: Enable voltage switch detection
29:28	**ACMD**	AUTO_CMD	**Enables auto command** Determines use of auto command functions. This function can be used in all modes including PIO/Basic DMA/Descriptor DMA/Enhanced Mode. There are two methods to stop multiple-block read and write operation.

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Bit(s)	Mnemonic	Name	Description
			1. Enabling auto CMD12 Multiple-block read and write commands for memory require CMD12 to stop the operation. When ACMD-12 is used, MSDC issues CMD12 automatically when the last block transfer is completed. Auto CMD12 error is indicated to the MSDC_INT register. The host driver shall not set up this bit if the command does not require CMD12. In particular, secure commands defined in the Part 3 File Security specification do not require CMD12. 2. Enabling auto CMD23 When ACMD-23 is used, MSDC issues a CMD23 automatically before issuing a command specified in the CMD field. The Host Controller Version 3.00 and later versions support this function. By writing the command register, MSDC issues a CMD23 first then a command specified by the CMD field in the SDC_CMD register. If response errors of CMD23 are detected, the second command will not be issued. A CMD23 error is indicated in the MSDC_INT register. 32-bit block count value for CMD23 is set to the SDC_BLOCK_NUM register. 2'b00: Disable Auto Command 2'b01: Enable Auto CMD12 2'b10: Enable Auto CMD23 2'b11: Enable Re-tuning CMD19
27:16	**LEN**	LEN	**Length** Defines the length of one block (unit: byte) in a data transaction of block mode or the data length (unit: byte) in data transaction of byte mode. The maximum value of block length is 2,048 bytes. 12'b000000000000: Reserved 12'b000000000001: Block length is 1 byte 12'b000000000010: Block length is 2 byte 12'b011111111111: Block length is 2047 byte 12'b100000000000: Block length is 2048 byte
15	**GOIRQ**	GO_IRQ	**GO_IRQ command** Indicates if the command is GO_IRQ_STATE (CMD40) and used only for MMC protocol. If the command is GO_IRQ_STATE, the period between command token and response token will not be limited. 1'b0: The command is not GO_IRQ_STATE 1'b1: The command is GO_IRQ_STATE
14	**STOP**	STOP	**Stop command** Indicates if the command is a stop transmission command. It should be set to 1 when CMD12 (SD/MMC) or CMD52 with I/O abort (SDIO) is to be issued. 1'b0: The command is not a stop transmission command 1'b1: The command is a stop transmission command
13	**RW**	RW	**Selects command read write** The register bit defines the command is a read command or write command. The register bit is valid only when the command causes a transaction with data token. 1'b0: The command is a read command 1'b1: The command is a write command
12:11	**DTYPE**	DTYPE	**Selects data block** Defines data token type for the command. 2'b00: No data token for the command 2'b01: Single block transaction (only available in block mode) 2'b10: Multiple block transaction. (only available in block mode) 2'b11: Stream operation. It only shall be used in MMC protocol. (only available in block mode)
9:7	**RSPTYP**	RSPTYP	**Command response type** 3'b000: This command has no response. 3'b001: The command has R1/R5/R6/R7 response. The response

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Bit(s)	Mnemonic	Name	Description
			token is 48-bit with CRC check (For SD/MMC/SDIO) (Not include the SDIO abort command) 3'b010: The command has R2 response. The response token is 136-bit (For SD/MMC) 3'b011: The command has R3 response. The response token is 48-bit response, no CRC check (For SD/MMC) 3'b100: The command has R4 response. The response token is 48-bit without CRC check (For SDIO) The response token is 48-bit with CRC check (For MMC) 3'b111: The command has R1b response. The response token is 48-bit (For SD/MMC/SDIO)
6	**BREAK**	BREAK	**Aborts pending MMC GO_IRQ command** Only valid for a pending GO_IRQ_MODE command waiting for MMC interrupt response. 1'b0: Not a beak command 1'b1: Break a pending MMC GO_IRQ_MODE command in the controller.
5:0	**CMD**	CMD	**SD Memory Card command**

11250038 SDC_ARG SD Argument Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ARG[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ARG[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ARG**	ARG	Memory card controller argument register

1125003C SDC_STS SD Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMC SWR CPL															CMD_WR_BUSY
Type	RU															W1C
Reset	0															0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CMD BSY	SDCB SY
Type															RU	RU
Reset															0	0

Bit(s)	Mnemonic	Name	Description
31	**MMCSWR CPL**	MMC_STREAM_WR_COMPL	**MMC stream mode write data are all flushed to MMC card.** SW can use this bit to confirm the last write data are flushed to MMC before issuing the STOP command. This bit is only valid when command SDC_CMD.DTYPE=2'b11. 1'b0: Last Data are partially inside MSDC 1'b1: Last data are flushed to MMC card

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Bit(s)	Mnemonic	Name	Description
16		CMD_WR_BUSY	
1	**CMDBSY**	CMDBUSY	**SD command line busy status** SW should always read this bit to make sure the command line is not busy before sending the next command. If the command is R1B or data read/write command, SW should also check the SDCBUSY bit. *Note: When auto command 12 is enabled, this bit will be asserted immediately after SDC_CMD is written and de-asserted after auto-command 12 is finished.* 1'b0: No transmission is going on CMD line on SD bus. 1'b1: There is transmission going on CMD line on SD bus.
0	**SDCBSY**	SDCBUSY	**SD controller busy status** 1'b0: SD controller is idle 1'b1: SD controller is busy

11250040 SDC_RESP0 SD Response Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP0[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP0[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP0**	RESP0	Memory card controller response register 0

11250044 SDC_RESP1 SD Response Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP1[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP1[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP1**	RESP1	Memory card controller response register 1

11250048 SDC_RESP2 SD Response Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP2[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP2[15:0]															
Type	RU															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP2**	RESP2	Memory card controller response register 2

1125004C **SDC_RESP3** SD Response Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RESP3[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RESP3[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP3**	RESP3	Memory card controller response register 3

11250050 **SDC_BLK_NUM** SD Block Number Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**BLKNUM[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BLKNUM[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:0	**BLKNUM**	BLOCK_NUMBER	**Memory card controller block number** Indicates block number of data transaction. 32'd0: Reserved 32'd1: 1-data block 32'd2: 2-data block 32'd3: 3-data block 32'hffffffff: 4GB-1 data block

11250054 **SDC_VOL_CHG** SD Voltage Change Wait Time Register 00000145

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**VCHGCNT**															
Type	RW															
Reset	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	1

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Bit(s)	Mnemonic	Name	Description
15:0	**VCHGCNT**	VOL_CHG_WAIT_CNT	**Defines SD voltage change check wait time** The wait time is clock frequency multiplied by VOL_WAIT_TIME.

11250058 SDC_CSTS SD Card Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSTS[31:16]															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSTS[15:0]															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CSTS**	CSTS	**CSTS** The card status field in the response R1 or R1b field. Each bit can be written 1 to clear individually.

1125005C SDC_CSTS_EN SD Card Status Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSTS_EN[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSTS_EN[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CSTS_EN**	CSTS_EN	**CSTS_EN** Controls which bit of CSTA will generate MSDC_INT.SDCSTA.

11250060 SDC_DATCRC_STS SD Card Data CRC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCSSN								DCSSP							
Type	RU								RU							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8	**DCSSN**	DAT_CRCSTS_NEG	**MSDC DDR mode negative edge read data CRC status** Reflects CRC status of data line[7:0] in DDR mode. The positive edge CRC status is shown in DAT_CRC_STS[7:0].

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Bit(s)	Mnemonic	Name	Description
			Only for MSDC read. 1'b0: No CRC error 1'b1: CRC error
7:0	**DCSSP**	DAT_CRCSTS_POS	**MSDC read data CRC status** Reflects CRC status of data line[7:0]. Only for MSDC read. 1'b0: No CRC error 1'b1: CRC error

11250080 **SD_ACMD_RESP** **SD ACMD Response Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ACMDRESP[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACMDRESP[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ACMDRESP**	AUTOCMD_RESP	**SD auto command response register** Stores response[39:8] of ACMD12/ACMD23/ACMD19.

11250084 **SD_ACMD19_TRG** **SD ACMD19 Target Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													ACMDFTSEL			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**ACMDFTSEL**	FINE_TUNE_SEL	**Selects SD auto command 19 test target** After auto-command 19 is triggered, MSDC will only change the phase of the selected one and keep the value of other tuning registers. SW can get the result from AUTOCMD_STS. There are total 32 phases for each delay line. 4'd0: Select PAD_CLK_TXDLY[5:0] as the target to run auto-command19. 4'd1: Select PAD_CMD_RXDLY[5:0] as the target to run auto-command19. 4'd2: Select PAD_DAT_RD_RXDLY[5:0] as the target to run auto-command19. 4'd3: Select PAD_DAT_WR_RXDLY[5:0] as the target to run auto-command19. 4'd4: Select DAT0_RD_DLY[5:0] as the target to run auto-command19. 4'd5: Select DAT1_RD_DLY[5:0] as the target to run auto-command19.

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Bit(s)	Mnemonic	Name	Description
			4'd6: Select DAT2_RD_DLY[5:0] as the target to run auto-command19. 4'd7: Select DAT3_RD_DLY[5:0] as the target to run auto-command19. 4'd8: Select DAT4_RD_DLY[5:0] as the target to run auto-command19. 4'd9: Select DAT5_RD_DLY[5:0] as the target to run auto-command19. 4'd10: Select DAT6_RD_DLY[5:0] as the target to run auto-command19. 4'd11: Select DAT7_RD_DLY[5:0] as the target to run auto-command19. 4'd12: Select CMD_RESP_RXDLY[5:0] as the target to run auto-command19. Others: Reserved

11250088 SD_ACMD19_STS SD ACMD19 Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ACMD19STS[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACMD19STS[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	ACMD19STS	AUTOCMD19_STS	**SD auto command 19 test result register** When auto-command 19 is enabled, HW will automatically try 32 times of command-19 and store the result into this register. This register contains the 1st to 32rd results in bit[0:31].

1125008C DMA_SA_HIGH4BIT DMA Current Address Register of high 4bit 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DMASAHIGH4BIT			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	DMASAHIGH4BIT	DMA_SURR_ADDR_HIGH4BIT	Sets up the high 4-bit address of start address since the 64G DRAM needs a 36-bit address

11250090 DMA_SA DMA Start Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	**DMASA[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DMASA[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DMASA**	DMA_STR_ADDR	**Start address of DMA address** Sets up the start address of the DMA. In DMA basic mode, this field indicates the source or destination address of the data transfer which depends on the command. In descriptor base DMA, this is the descriptor chain start address.

11250094 **DMA_CA** **DMA Current Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DMACA[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DMACA[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DMACA**	DMA_CURR_ADDR	**Current address of DMA address** Reads the current address of DMA descriptor chain.

11250098 **DMA_CTRL** **DMA Control Register** **00006008**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**BSTSZ**			**SPLIT1K**	**LASTBF**	**DMAALIGN**	**DMAMOD**					**READYM**	**DMARSM**	**DMASTOP**	**DMASTART**
Type		RW			RW	RW	RW	RW					RU	WO	W1C	WO
Reset		1	1	0	0	0	0	0					1	0	0	0

Bit(s)	Mnemonic	Name	Description
14:12	**BSTSZ**	BURST_SIZE	**DMA burst size** Specifies the maximum transfer bytes allowed at the device per DMA burst. This field cannot be modified when the DMA status is 1. 3'd3: 8 Bytes 3'd4: 16 Bytes 3'd5: 32 Bytes 3'd6: 64 Bytes Other: Reserved
11	**SPLIT1K**	DMA_SPLIT_1K	**Specifies split burst when corssing 1K boundary address** 1'b0: 1K boundary not split 1'b1: 1K boundary split

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Bit(s)	Mnemonic	Name	Description
10	**LASTBF**	LAST_BUF	**Last buffer of the basic DMA mode** Indicates the last buffer in basic DMA mode.
9	**DMAALIGN**	DMA_ALIGN	**Specifies address alignment burst size** 1'b0: do not DAM burst size alignment 1'b1: DAM burst size alignment
8	**DMAMOD**	DMA_MODE	**DMA operation mode** Indicates operation mode of DMA. 1'b0: Basic DMA mode 1'b1: Descriptor base DMA mode
3	**READYM**	AHB_READYM	**Only for debugging when DMA hangs** SW checks if AHB bus is ok when GDMA hangs. 1: bus is normal 0: bus not normal
2	**DMARSM**	DMA_RESUME	**DMA resume control register** Resumes DMA transaction. Read always returns to 0.
1	**DMASTOP**	DMA_STOP	**DMA stop control register** Stops DMA transaction. When SW issues STOP command, SW must wait for this bit to be de-asserted or DMA inactive to guarantee stop is done.
0	**DMASTART**	DMA_START	**DMA start control register** Starts DMA transaction. Read always returns to 0.

1125009C DMA_CFG DMA Configuration Register 00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															OUTBOUNDSTOPDMA	DMACHKSUM12B
Type															RW	RW
Reset															0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name			MSDCACTIVEEN				AHBHPROT2EN							LOCKDISABLE	DSCPCSEN	DMASTS
Type			RW				RW							RW	RW	RU
Reset			0	0			0	0						1	0	0

Bit(s)	Mnemonic	Name	Description
17	**OUTBOUNDSTOPDMA**	OUT_BOUND_STOP_DMA	**Determines whether to stop Enhance DMA if gear setting is out of boundary when sending training data** 1'b0: Enhance DMA continues even when gear setting is out of boundary during training data sending. 1'b1: Enhance DMA stops when gear setting is out of boundary during training data sending.
16	**DMACHKSUM12B**	DMA_CHK_SUM_12B	**Indicates GPD/BD checksum covers 16 bytes or 12 bytes** 1'b0: GPD/BD checksum covers 16 bytes. 1'b1: GPD/BD checksum only covers 12 bytes.
13:12	**MSDCACTIVEEN**	MSDC_ACTIVE_EN	**Indicates how to control msdc_active** 2'b00: dynamic control msdc_active 2'b01: msdc_active = 0 2'b10: msdc_active = 1 2'b11: Reserved

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Bit(s)	Mnemonic	Name	Description
9:8	**AHBHPROT2EN**	AHB_HPROT_2_EN	**Determines how to control hprot_2 pin of AHB bus** AHB_HPROT_2_EN = 2'b00, and basic DMA mode All the write transfers of a burst will be accessed by bufferable mode except for the last burst of DMA AHB_HPROT2_2_EN=2'b00, and descriptor DMA mode. All write transfers of a burst will be accessed by bufferable mode except for HW own update transfer. 2'b00: dynamic control hprot_2 2'b01: hprot_2 = 0 2'b10: hprot_2 = 1
2	**LOCKDISABLE**	LOCK_DISABLE	**Disables lock to improve EMI efficiency** 1'b0: enable ahb lock 1'b1: disable ahb lock
1	**DSCPCSEN**	DMA_DSCP_CS_EN	**Enables DMA descriptor checksum** This bit is used to enable or disable the descriptor checksum validation function for the descriptor. This field cannot be modified when the DMA status is 1.
0	**DMASTS**	DMA_STATUS	**DMA status** Indicates the status of DMA. 1'b0: DMA engine is inactive 1'b1: DMA engine is active

112500A0 **SW_DBG_SEL** **MSDC S/W Debug Selection Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SWDBGSEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**SWDBGSEL**	DBG_SEL	**Selects MSDC debugging** Reserved.

112500A4 **SW_DBG_OUT** **MSDC S/W Debug Output Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SWDBGO[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SWDBGO[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SWDBGO**	DBG_OUT	**MSDC debugging output** 32-bit output selected by SW_DBG_SEL register

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112500A8 DMA_LENGTH DMA Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	XFSZ[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XFSZ[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**XFSZ**	XFER_SIZE	**DMA total transfer size** Specifies the number of DMA transfer byte required for the movement of source data through DMA. This field is only valid in basic DMA mode.

112500B0 PATCH_BIT0 MSDC Patch Bit Register 0 403C0006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PTCH31	PTCH30	PTCH29	PTCH28	PTCH27	PTCH26	PTCH22				PTCH18				PTCH17	PTCH16
Type	RW	RW	RW	RW	RW	RW	RW				RW				RW	RW
Reset	0	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PTCH15	CKGDLYS					INTCKS			DESCUP	PTCH5	PTCH4	PTCH3	PTCH02	PTCH01	
Type	RW	RW					RW			RW	RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	

Bit(s)	Mnemonic	Name	Description
31	**PTCH31**	EN_MMC_DRV_RESP	**Enables MSDC always driving bus when outputting wake-up response (BREAK)** 1'b0: Disable 1'b1: Enable
30	**PTCH30**	DETECT_WR_CRC_TIMEOUT	**Detects MSDC write data CRC phase time-out** 1'b0: Does not detect CRC phase timeout 1'b1: Detect CRC phase timeout
29	**PTCH29**	SPC_ALWAYS_PUSH	**SPC buffer push mechanism** 1'b0: Push the buffer only when read transfer is on-going 1'b1: Always push the buffer
28	**PTCH28**	SDIO_INT_DLY_SEL	**Selects SDIO interrupt latch time** 1'b0: Latch the data line value in internal SDIO interrupt period 1'b1: Latch the data line value in 1 clock delay of internal SDIO interrupt period
27	**PTCH27**	SDC_CMD_CMDFAIL_SEL	**Selects SDIO interrupt period recovery** 1'b0: SDIO interrupt period will re-start after a CMD12 or CMD52 command is issued 1'b1: SDIO interrupt period whenever DAT line is not busy
26	**PTCH26**	SDC_CMD_IDRT_SEL	**Selects SD identification response time** The register bit indicates if the command has a response with NID (i.e. 5 serial clock cycles as defined in SD memory card Specification Part 1 Physical Layer Specification version 1.0) response time. The register bit is valid only when the command has a response token.

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Bit(s)	Mnemonic	Name	Description
			Thus, the register bit must be set to 1 for CMD2 (ALL_SEND_CID) and ACMD41 (SD_APP_OP_CMD). 1'b0: Otherwise. 1'b1: The command has a response with NID response time.
25:22	**PTCH22**	SDC_CFG_WDOD	**SD Write Data Output Delay** The period from finish of the response for the initial host write command or the last write data block in a multiple block write operation to the start bit of the next write data block requires at least two serial clock cycles. The register field is used to extend the period (Write Data Output Delay) in unit of one serial clock. 4'b0000: No extension 4'b0001: Extend 1 more serial clock cycle 4'b0010: Extend 2 more serial clock cycles 4'b1111: Extend 15 more serial clock cycles
21:18	**PTCH18**	SDC_CFG_BSYDLY	**SD R1B busy detection mode** Only valid for the commands with R1b response. If the command has a response of R1b type, MS/SD controller must monitor the data line 0 for card busy status from the bit time that is two serial clock cycles after the command end bit to check if operations in SD/MMC memory card are finished. The register field is used to expand the time between the command end bit and end of detection period to detect card busy status. If time is up and there is no card busy status on data line 0, the controller will abandon the detection. 4'b0000: No extension 4'b0001: Extend 1 more serial clock cycle 4'b0010: Extend 2 more serial clock cycles 4'b1111: Extend 15 more serial clock cycles
17	**PTCH17**	SDIO_CFG_INTC_SEL	**Selects SDIO interrupt model** 1'b0: When data line [1] = 0, trigger SDIO interrupt event. 1'b1: When data line [3:0] = 4'b1101, trigger SDIO interrupt event
16	**PTCH16**	MSDC_BLKNUM_SEL	**Supports ACMD23 reliable/force pro etc. features** 1'b0: Support ACMD23 reliable/force prog etc. feature 1'b1: Does not support ACMD23 reliable/force prog etc. feature
15	**PTCH15**	MSDC_FIFO_RD_DIS	**Disables MSDC RXFIFO read** 1'b0: Disable FIFO read permission to RXFIFO in PIO mode 1'b1: Enable FIFO read permission to RXFIFO in PIO mode
14:10	**CKGDLYS**	CKGEN_MSDC_DLY_SEL	**Selects CKBUF in CKGEN delay** Total 32 stages.
9:7	**INTCKS**	INT_DAT_LATCH_CK_SEL	**Selects internal MSDC clock phase** Total 8 stages, each stage can delay 1 clock period of msdc_src_ck.
6	**DESCUP**	DESC_UP_SEL	**SD transfer done interrupt should be issued when GPD are updated.** 1'b1: Enable new function to generate SD transfer done interrupt 1'b0: Use old function to generate SD transfer done interrupt
5	**PTCH5**	ACMD53_FAIL_ONE_SHOT	**Determines interrupt method of AUTOCMD53_FAIL** 1'b0: AUTOCMD53_FAIL interrupt will be asserted whenever CMD/DAT CRC error occurs. 1'b1: AUTOCMD53_FAIL interrupt will be asserted only when AUTOCMD53_DONE is asserted if there is CMD/DAT CRC error.
4	**PTCH4**	MASK_ACMD53_CRC_ERR_INTR	**Masks CMD/DAT CRC error interrupt when executing AUTOCMD53 training sequence** 1'b0: Enable CMD/DAT CRC error interrupt when executing AUTOCMD53 training sequence 1'b1: Mask CMD/DAT CRC error interrupt when executing AUTOCMD53 training sequence
3	**PTCH3**	RD_DAT_SEL	**Defines to use rising or falling buf data for SDR mode** 1'b0: Used rising buf data for SDR mode

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Bit(s)	Mnemonic	Name	Description
			1'b1: Used falling buf data for SDR mode
2	**PTCH02**	DIS_REFLECT_CMDWR_WHEN_BSY	**Enables SD command register write monitor** 1'b0: Enable monitor function 1'b1: Disable monitor function
1	**PTCH01**	EN_SDC_ODD_8BIT_SUP	**Enables SD odd number support for 8-bit data bus** 1'b0: Disable 1'b1: Enable

112500B4 PATCH_BIT1 MSDC Patch Bit Register 1 FFB00009

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MSHBFCKEN	MRCTLCKEN	MWCTLCKEN	MSDCKEN	MACMDCKEN	MVOLDTCKEN	MPSCCKEN	MSPCCKEN	HGDMACKEN		DCMEN	DCMDIVSEL1				SINGLEBURST
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW				RW
Reset	1	1	1	1	1	1	1	1	1		1	1				0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RESETGDMA		BIAS28R0	BIAS28R1	BIAS28R2				GETCRCMARGIN	GETBUSYMARGIN	CMDTA			WRTA		
Type	RW		RW	RW	RW				RW	RW	RW			RW		
Reset	0		0	0	0	0	0	0	0	0	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
31	**MSHBFCKEN**	MSDC_CK_SHBFF_CKEN	**msdc_src_ck clock enable bit for SHBFF** 1'b0: Disable 1'b1: Enable
30	**MRCTLCKEN**	MSDC_CK_RCTL_CKEN	**msdc_src_ck clock enable bit for RCTL** 1'b0: Disable 1'b1: Enable
29	**MWCTLCKEN**	MSDC_CK_WCTL_CKEN	**msdc_src_ck clock enable bit for WCTL** 1'b0: Disable 1'b1: Enable
28	**MSDCKEN**	MSDC_CK_SD_CKEN	**msdc_src_ck clock enable bit for SD** 1'b0: Disable 1'b1: Enable
27	**MACMDCKEN**	MSDC_CK_ACMD_CKEN	**msdc_src_ck clock enable bit for ACMD** 1'b0: Disable 1'b1: Enable
26	**MVOLDTCKEN**	MSDC_CK_VOLDET_CKEN	**msdc_src_ck clock enable bit for VOLDET** 1'b0: Disable 1'b1: Enable
25	**MPSCCKEN**	MSDC_CK_PSC_CKEN	**msdc_src_ck clock enable bit for PSC** 1'b0: Disable 1'b1: Enable
24	**MSPCCKEN**	MSDC_CK_SPC_CKEN	**msdc_src_ck clock enable bit forSPC** 1'b0: Disable 1'b1: Enable
23	**HGDMACKEN**	AHB_CK_GDMA_CKEN	**hclk_ck clock enable bit for GDMA** 1'b0: Disable 1'b1: Enable
21	**DCMEN**	DCM_EN	**Host enabling DCM for low power**

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Bit(s)	Mnemonic	Name	Description
			When there is no transfer, ahb_ck and msdc_src_ck will be divided from source clk. 1'b1: disable 1'b0: enable
20	**DCMDIVSEL1**	DCM_DIV_SEL1	**For spec4.5 divider msdc_src_ck from source clk; for spec50 divider ahb_ck from source clk** 1'b1: 32 divders from source clk 1'b0: 16 divders from source clk
16	**SINGLEBURST**	ENABLE_SINGLE_BURST	**AHB bus will not support incr1 burst type in the future and will only affect AHB bus MSDC design, not AXI bus design.** 1'b0: HW sends incr1 burst type. 1'b1: HW sends single burst type instead of incr1 type.
15	**RESETGDMA**	RESET_GDMA	**SW can reset GDMA when design hangs.** 1'b1: Reset GDMA 1'b0: Does not reset GDMA
13	**BIAS28R0**	BIAS_EXTBIAS_28NM	**28NM BIAS Controller register 0**
12	**BIAS28R1**	BIAS_EN18IO_28NM	**28NM BIAS Controller register 1**
11:8	**BIAS28R2**	BIAS_TUNE_28NM	**28NM BIAS Controler register 2**
7	**GETCRCMARGIN**	GET_CRC_MARGIN	**Adds margin to get CRC status when card resp CRC does not match spec 2 cycle from endbit** 1'b0: 8 cycles reserved for getting CRC status from write data CRC endbit 1'b1: 16 cycles reserved for getting CRC status from write data CRC endbit
6	**GETBUSYMARGIN**	GET_BUSY_MARGIN	**Adds margin for getting busy state of data0** 1'b0: 1 cycle reserved for getting busy state from SRC status endbit 1'b1: 3 cycles reserved for getting busy state from SRC status endbit
5:3	**CMDTA**	CMD_RSP_TA_CNTR	**CMD response turn-around period** Turn-around cycle = CMD_RSP_TA_CNTR + 2 In USH104 mode, this register should be set to 1. In non-UHS104 mode, this register should be set to 0.
2:0	**WRTA**	WRDAT_CRCS_TA_CNTR	**Write data and CRC status turn-around period** Turn-around cycle = WRDAT_CRCS_TA_CNTR + 2 In USH104 mode, this register should be set to 1. In non-UHS104 mode, this register should be set to 0.

112500B8 **PATCH_BIT2** **MSDC Patch Bit Register 2** **14801801**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRCSTSENSEL			CFGCRCSTS	CFGCRCSTSCNT		CFGCRCSTSEDGE	CFG_CRCSTS_SEL	POPENCNT					RESPSTSENSEL		
Type	RW			RW	RW		RW	RW	RW					RW		
Reset	0	0	0	1	0	1	0	0	1	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFGRESP	CFGRESPCNT			INTCRESPSEL		CFGRDAT	CFGRDATCNT					RESPWAITCNT		SUPPORT64G	ENHANCEGPD
Type	RW	RW			RW		RW	RW					RW		RW	RW
Reset	0	0	0	1	1		0	0	0	0	0	0	0	0	0	1

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Bit(s)	Mnemonic	Name	Description
31:29	**CRCSTSENSEL**	CRCSTS_LATCH_EN_SEL	**Configures latch CRC status enable signal for async FIFO in eMMC45** 3'b000: Latch CRC status enable signal does not delay. 3'b001: Latch CRC status enable signal delays 1T msdc_ck. 3'b010: Latch CRC status enable signal delays 2T msdc_ck. 3'b011: Latch CRC status enable signal delays 3T msdc_ck. 3'b111: Latch CRC status enable signal delays 7T msdc_ck.
28	**CFGCRCSTS**	CFG_CRCSTS	**Configures CRC status path selection** The setting only uses eMMC4.5 feature. 1'b0: Latch CRC Status select delay-line path 1'b1: Latch CRC Status select async fifo path
27:26	**CFGCRCSTSCNT**	CFG_CRCSTS_CNT	**Configures how many data are pushed in async FIFO before starting to pop out data from async FIFO** The min. register setting is 1. Do not set it to 0. The setting only uses eMMC4.5 feature. 2'b00: Push 0 data in async FIFO when starting to pop out data from async FIFO 2'b01: Push 1 data in async FIFO when starting to pop out data from async FIFO 2'b10: Push 2 data in async FIFO when starting to pop out data from async FIFO 2'b11: Push 3 data in async FIFO when starting to pop out data from async FIFO
25	**CFGCRCSTSEDGE**	CFG_CRCSTS_EDGE	**Uses rising async FIFO or falling async FIFO** 1'b0: Async FIFO latch CRC status uses rising async FIFO. 1'b1: Async fifo latch CRC status uses falling async FIFO.
24		CFG_CRCSTS_SEL	**Configures async FIFO path selection** 1'b0: Used normal path in async FIFO 1'b1: Use 2DFF path in async FIFO
23:20	**POPENCNT**	POP_EN_CNT	**Pop enable counter** Defines how many write pointer and read pointer margin begin to pop up data transfer.
18:16	**RESPSTSENSEL**	RESP_LATCH_EN_SEL	**Configures latch CMD response enable signal for async FIFO in eMMC45** 3'b000: Latch CMD response enable signal does not delay. 3'b001: Latch CMD response enable signal delays 1T msdc_ck. 3'b010: Latch CMD response enable signal delays 2T msdc_ck. 3'b011: Latch CMD response enable signal delays 3T msdc_ck. 3'b111: Latch CMD response enable signal delays 7T msdc_ck.
15	**CFGRESP**	CFG_RESP	**Configures CMD Response path selection** The setting only used eMMC4.5 feature. 1'b0: Latch CMD response selects async FIFO path. 1'b1: Latch CMD response selects delay-line path.
14:12	**CFGRESPCNT**	CFG_RESP_CNT	**Configures how many data are pushed in async FIFO before starting to pop out data from async FIFO** The min. register setting is 1. Do not set it to 0. The setting only uses eMMC4.5 feature. 3'b000: Push 0 data in async FIFO when starting to pop out data from async FIFO 3'b001: Push 1 data in async FIFO when starting to pop out data from async FIFO 3'b111: Push 7 data in async FIFO when starting to pop out data from async FIFO.
11	**INTCRESPSEL**	INTC_RESP_SEL	**Configures BREAK command async FIFO path** 1'b0: Use normal path in async FIFO 1'b1: Use 2DFF path in async FIFO
9	**CFGRDAT**	CFG_RDAT	**Configures read data path**

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Bit(s)	Mnemonic	Name	Description
			1'b0: Read data path bypasses delay line. 1'b1: Read data path through delay line
8:4	**CFGRDATCNT**	CFG_RDAT_CNT	**Configures read data path delay line**
3:2	**RESPWAITCNT**	RESP_WAIT_CNT	**Configures CMD response timeout** The timeout cycle is 65T+16*RESP_WAIT_CNT. 2'b00: CMD response timeout is 65T. 2'b01: CMD response timeout is 65T+ 16*1T. 2'b01: CMD response timeout is 65T+ 16*2T. 2'b01: CMD response timeout is 65T+ 16*3T.
1	**SUPPORT64G**	SUPPORT_64G	**Indicates which project supports high 64G DRAM space access** 1'b1: Support 64G DRAM access 1'b0: Does not support 64G DRAM access
0	**ENHANCEGPD**	ENHANCE_WAIT_GPD	**If SW clears int when GPD update has not been finished, the design will hang.** Set this bt to 1 to avoid such issue in enhance write mode. 1'b1: Use new HW code to update GPD in enhance mode 1'b0: Use old HW code

112500C0 **DAT0_TUNE_CRC** **DAT0 Tune Result Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DAT0CRCSTS[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DAT0CRCSTS[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DAT0CRCSTS**	DAT0_CRC_STS	**SDIO auto command 53 test result register** When auto-command 53 is enabled, HW will automatically try TUNE_WINDOW times of command-53 and store CRC result of DAT0 into this register. This register contains the 1st to 32rd results in bit[0:31].

112500C4 **DAT1_TUNE_CRC** **DAT1 Tune Result Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DAT1CRCSTS[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DAT1CRCSTS[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DAT1CRCS**	DAT1_CRC_STS	**SDIO auto command 53 test result register**

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Bit(s)	Mnemonic	Name	Description
	TS		When auto-command 53 is enabled, HW will automatically try TUNE_WINDOW times of command-53 and store CRC result of DAT1 into this register. This register contains the 1st to 32rd results in bit[0:31].

112500C8 DAT2_TUNE_CRC DAT2 Tune Result Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DAT2CRCSTS[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DAT2CRCSTS[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	DAT2CRCSTS	DAT2_CRC_STS	**SDIO auto command 53 test result register** When auto-command 53 is enabled, HW will automatically try TUNE_WINDOW times of command-53 and store CRC result of DAT2 into this register. This register contains the 1st to 32rd results in bit[0:31].

112500CC DAT3_TUNE_CRC DAT3 Tune Result Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DAT3CRCSTS[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DAT3CRCSTS[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	DAT3CRCSTS	DAT3_CRC_STS	**SDIO auto command 53 test result register** When auto-command 53 is enabled, HW will automatically try TUNE_WINDOW times of command-53 and store CRC result of DAT3 into this register. This register contains the 1st to 32rd results in bit[0:31].

112500D0 CMD_TUNE_CRC CMD Tune Result Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CMDCRCSTS[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CMDCRCSTS[15:0]															
Type	RU															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	CMDCRCSTS	CMD_CRC_STS	**SDIO auto command 53 test result register** When auto-command 53 is enabled, HW will automatically try TUNE_WINDOW times of command-53 and store CRC result of CMD into this register. This register contains the 1st to 32rd results in bit[0:31].

112500D4 SDIO_TUNE_WIND SDIO Tune Window Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TUNEWINDOW				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0	TUNEWINDOW	TUNE_WINDOW	**SDIO auto command 53 tuning window setting** Window range: 1. For CMD PAD Low bound: max(0, PAD_CMD_RXDLY-TUNE_WINDOW) High bound: min(31, PAD_CMD_RXDLY+TUNE_WINDOW) 2. For DAT PAD Low bound: max(0, DAT(0:3)_RD_DLY-TUNE_WINDOW) High bound: min(31: DAT(0:3)_RD_DLY+TUNE_WINDOW)

112500F0 PAD_TUNE0 MSDC Pad Tuning Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CLKTDLY					CMDRRDLY					CMDRRDLYSEL	CMDRDLY				
Type	RW					RW					RW	RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RXDLYSEL		DATRRDLYSEL	DATRRDLY					DELAYEN			DATWRDLY				
Type	RW		RW	RW					RW			RW				
Reset	0		0	0	0	0	0	0	0			0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:27	CLKTDLY	PAD_CLK_TXDLY	**Controls CLK pad TX delay** This register adds delay to CLK phase. Total 32 stages.
26:22	CMDRRDLY	PAD_CMD_RESP_RXDLY	**Controls CMD response internal delay line** This register fine-tunes response phase latched by MSDC internal clock. Total 32 stages.
21	CMDRRDLYSEL	PAD_CMD_RD_RXDLY_SEL	**Decides CMD response passes through data delay line 1 or not** 1'b0: Pass

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Bit(s)	Mnemonic	Name	Description
			1'b1: Does not pass
20:16	**CMDRDLY**	PAD_CMD_RXDLY	**Controls CMD pad RX delay line** This register fine-tunes CMD pad macro response latch timing. Total 32 stages.
15	**RXDLYSEL**	PAD_RXDLY_SEL	**Decides RX delay line tune data path or clock path** 1'b0: RX delay line tune data path 1'b1: RX delay line tune clock path
13	**DATRRDLYSEL**	PAD_DAT_RD_RXDLY_SEL	**Decide RX data pass through data delay line 1 or not** 1'b0: Pass 1'b1: Does not pass
12:8	**DATRRDLY**	PAD_DAT_RD_RXDLY	**Controls DAT pad RX delay line (for MSDC read only)** This register fine-tunes DAT pad macro read data latch timing. Total 32 stages.
7	**DELAYEN**	DELAY_EN	**Enables all delay cell toggle when power is on** 1'b0: Disable delay cell toggle default 1'b1: Enable delay cell toggle default
4:0	**DATWRDLY**	PAD_DAT_WR_RXDLY	**Controls write data status internal delay line** This register fine-tunes write status phase latched by MSDC internal clock. Total 32 stages.

112500F4 PAD_TUNE1 MSDC Pad Tuning Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											**CMDRRDLY2SEL**	**CMDRDLY2**				
Type											RW	RW				
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**DATRRDLY2SEL**	**DATRRDLY2**												
Type			RW	RW												
Reset			0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
21	**CMDRRDLY2SEL**	PAD_CMD_RD_RXDLY2_SEL	**Decides CMD response passes through data delay line 2 or not** 1'b0: Pass 1'b1: Does not pass
20:16	**CMDRDLY2**	PAD_CMD_RXDLY2	**Controls CMD pad RX delay line 2** This register fine-tunes CMD pad macro response latch timing in data path. Total 32 stages.
13	**DATRRDLY2SEL**	PAD_DAT_RD_RXDLY2_SEL	**Decides RX data pass through data delay line 2 or not** 1'b0: Pass 1'b1: Does not pass
12:8	**DATRRDLY2**	PAD_DAT_RD_RXDLY2	**Controls DAT pad RX delay line 2 (for MSDC read only)** This register fine-tunes DAT pad macro read data latch timing. Total 32 stages.

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112500F8 **DAT_RD_DLY0** **MSDC Data Delay Line Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT0RDDLY								DAT1RDDLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DAT2RDDLY								DAT3RDDLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	DAT0RDDLY	DAT0_RD_DLY	**Controls DAT0 pad RX delay line (for MSDC RD)** Total 32 stages.
20:16	DAT1RDDLY	DAT1_RD_DLY	**Controls DAT1 pad RX delay line (for MSDC RD)** Total 32 stages.
12:8	DAT2RDDLY	DAT2_RD_DLY	**Controls DAT2 pad RX delay line (for MSDC RD)** Total 32 stages.
4:0	DAT3RDDLY	DAT3_RD_DLY	**Controls DAT3 pad RX delay line (for MSDC RD)** Total 32 stages.

112500FC **DAT_RD_DLY1** **MSDC Data Delay Line Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT4RDDLY								DAT5RDDLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DAT6RDDLY								DAT7RDDLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	DAT4RDDLY	DAT4_RD_DLY	**Controls DAT4 pad RX delay line (for MSDC RD)** Total 32 stages.
20:16	DAT5RDDLY	DAT5_RD_DLY	**Controls DAT5 pad RX delay line (for MSDC RD)** Total 32 stages.
12:8	DAT6RDDLY	DAT6_RD_DLY	**Controls DAT6 pad RX delay line (for MSDC RD)** Total 32 stages.
4:0	DAT7RDDLY	DAT7_RD_DLY	**Controls DAT7 pad RX delay line (for MSDC RD)** Total 32 stages.

11250100 **DAT_RD_DLY2** **MSDC Data Delay Line Register 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT0RDDLY2								DAT1RDDLY2				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DAT2RDDLY2								DAT3RDDLY2				

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Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	**DAT0RDDLY2**	DAT0_RD_DLY2	**Controls DAT0 pad RX delay line 2 (for MSDC RD)** Total 32 stages.
20:16	**DAT1RDDLY2**	DAT1_RD_DLY2	**Controls DAT1 pad RX delay line 2 (for MSDC RD)** Total 32 stages.
12:8	**DAT2RDDLY2**	DAT2_RD_DLY2	**Controls DAT2 pad RX delay line 2 (for MSDC RD)** Total 32 stages.
4:0	**DAT3RDDLY2**	DAT3_RD_DLY2	**Controls DAT3 pad RX delay line 2 (for MSDC RD)** Total 32 stages.

11250104 **DAT_RD_DLY3** **MSDC Data Delay Line Register 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**DAT4RDDLY2**								**DAT5RDDLY2**				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**DAT6RDDLY2**								**DAT7RDDLY2**				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	**DAT4RDDLY2**	DAT4_RD_DLY2	**Controls DAT4 pad RX delay line 2 (for MSDC RD)** Total 32 stages.
20:16	**DAT5RDDLY2**	DAT5_RD_DLY2	**Controls DAT5 pad RX delay line 2 (for MSDC RD)** Total 32 stages.
12:8	**DAT6RDDLY2**	DAT6_RD_DLY2	**Controls DAT6 pad RX delay line 2 (for MSDC RD)** Total 32 stages.
4:0	**DAT7RDDLY2**	DAT7_RD_DLY2	**Controls DAT7 pad RX delay line 2 (for MSDC RD)** Total 32 stages.

11250110 **HW_DBG_SEL** **MSDC H/W Debug Selection Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**DBGWSEL**	**DBG3SEL**						**DBG2SEL**							
Type		RW	RW						RW							
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**DBG1SEL**						**DBG0SEL**							
Type			RW						RW							
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30	**DBGWSEL**	HW_DBG_WRAP_SEL	**Selects HW debug output for wrapper** 0: Select original debug pins

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Bit(s)	Mnemonic	Name	Description
			1: Select wrapper debug pins
29:24	**DBG3SEL**	HW_DBG3_SEL	**Selects HW debug output**
23:16	**DBG2SEL**	HW_DBG2_SEL	**Selects HW debug output**
13:8	**DBG1SEL**	HW_DBG1_SEL	**Selects HW debug output**
7:0	**DBG0SEL**	HW_DBG0_SEL	**Selects HW debug output**

11250114 **MAIN_VER** **MSDC Main Version Register** **20140512**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAINVER[31:16]															
Type	RO															
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAINVER[15:0]															
Type	RO															
Reset	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
31:0	**MAINVER**	MAIN_VER	Main version

11250118 **ECO_VER** **MSDC ECO Version Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ECOVER[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ECOVER[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ECOVER**	ECO_VER	ECO version

Module name: MSDC3 Base address: (+11260000h)

Address	Name	Width	Register Function
11260000	MSDC_CFG	32	**MSDC Configuration Register** For general configuration of the MS/SD controller
11260004	MSDC_IOCON	32	**MSDC IO Configuration Register** Contains the receiver path data latch timing control and interface control bits
11260008	MSDC_PS	32	**MSDC Pin Status Register** Stores card detection and write protection pin status. Card detection status can be disabled.
1126000C	MSDC_INT	32	**MSDC Interrupt Register** Contains the status of interrupts Note: The register still shows the status of interrupt even though the interrupt is disabled.
11260010	MSDC_INTEN	32	**MSDC Interrupt Enable Register**

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Address	Name	Width	Register Function
			Contains related enabling bit of interrupts
11260014	MSDC_FIFOCS	32	**MSDC FIFO Control and Status Register** Contains control and status of embedded 128B FIFO
11260018	MSDC_TXDATA	32	**MSDC TX Data Port Register** For PIO mode only. Used to input MSDC write data to card. The access can be AHB1B/2B/4B.
1126001C	MSDC_RXDATA	32	**MSDC RX Data Port Register** For PIO mode only. Used to read back MSDC read data from card. The access can be AHB1B/2B/4B.
11260030	SDC_CFG	32	**SD Configuration Register** Configures MS/SD memory card controller when it is configured as the host of SD memory card. If the controller is configured as the host of memory stick, the contents of the register will have no impact on the operation of the controller.
11260034	SDC_CMD	32	**SD Command Register** Defines a SD memory card command and its attributes. Before MS/SD controller issues a transaction onto SD bus, the application should specify other relative settings such as argument for command. After writing the register by the application, MS/SD controller will issue the corresponding transaction onto SD serial bus. If the command is GO_IDLE_STATE, the controller will have serial clock on SD/MMC bus running 128 cycles before issuing the command.
11260038	SDC_ARG	32	**SD Argument Register** Contains argument of SD/MMC memory card command
1126003C	SDC_STS	32	**SD Status Register** Reflects SD bus status and contains MMC stream write status
11260040	SDC_RESP0	32	**SD Response Register 0** Contains parts of the last SD/MMC memory card bus response. See description in register field SDC_RESP3.
11260044	SDC_RESP1	32	**SD Response Register 1** Contains parts of the last SD/MMC memory card bus response. See description in register field SDC_RESP3.
11260048	SDC_RESP2	32	**SD Response Register 2** Contains parts of the last SD/MMC memory card bus response. See description in register field SDC_RESP3.
1126004C	SDC_RESP3	32	**SD Response Register 3** Contains parts of the last SD/MMC memory card bus response. Register fields SDC_RESP0, SDC_RESP1, SDC_RESP2 and SDC_RESP3 are composed of the last SD/MMC memory card bus response. For response of type R2, i.e. response of the command ALL_SEND_CID, SEND_CSD and SEND_CID, only bit 127 to 0 of response token are stored in register field SDC_RESP0, SDC_RESP1, SDC_RESP2 and SDC_RESP3. SDC_RESP0 = bit 31~0 SDC_RESP1 = bit 63~32 SDC_RESP2 = bit 95~64 SDC_RESP3 = bit 127~96 For response of type R1b in auto CMD12 or R1 in auto CMD23, bit 39 to 8 of response token are stored in register field of SDC_RESP3. For the responses of other types, only bit 39 to 8 of response token are stored in the register field SDC_RESP0.
11260050	SDC_BLK_NUM	32	**SD Block Number Register** Defines block number for block transaction. For single read/write, this register should be set to 1. For multiple read/write, this register should be set to bigger than 1. Set to 0 will cause unexpected result.
11260054	SDC_VOL_CHG	32	**SD Voltage Change Wait Time Register** Defines SD voltage change check wait time.

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Address	Name	Width	Register Function
11260058	SDC_CSTS	32	**SD Card Status Register** After commands with R1 and R1b response, this register will contain the status of the SD/MMC card.
1126005C	SDC_CSTS_EN	32	**SD Card Status Enable Register** Controls which bit of SDC_CSTS will generate the MSDC_INT.SD_CSTA interrupt
11260060	SDC_DATCRC_STS	32	**SD Card Data CRC Status Register** Reflects CRC status of data line[7:0]. Only for MSDC read.
11260080	SD_ACMD_RESP	32	**SD ACMD Response Register** Stores response of auto command from SD card
11260084	SD_ACMD19_TRG	32	**SD ACMD19 Target Register** Selects target delay line to run ACMD19 sequence
11260088	SD_ACMD19_STS	32	**SD ACMD19 Status Register** Stores result of auto command 19 from SD card
1126008C	DMA_SA_HIGH4BIT	32	**DMA Current Address Register of High 4 Bits** Contains start address high 4 bits of the 36-bit address for 64G DRAM access
11260090	DMA_SA	32	**DMA Start Address Register** Contains start address of DMA descriptor
11260094	DMA_CA	32	**DMA Current Address Register** Contains current DMA address
11260098	DMA_CTRL	32	**DMA Control Register** Controls DMA operation
1126009C	DMA_CFG	32	**DMA Configuration Register** Configures DMA operation
112600A0	SW_DBG_SEL	32	**MSDC S/W Debug Selection Register** Selects SW debugging output
112600A4	SW_DBG_OUT	32	**MSDC S/W Debug Output Register** Shows selected debugging output
112600A8	DMA_LENGTH	32	**DMA Length Register** Sets up basic DMA operation length
112600B0	PATCH_BIT0	32	**MSDC Patch Bit Register 0** Configures patch function. For normal function, this bit should be kept at default value.
112600B4	PATCH_BIT1	32	**MSDC Patch Bit Register 1** Configures patch function. For normal function, this bit should be kept at default value.
112600B8	PATCH_BIT2	32	**MSDC Patch Bit Register 2** Configures patch function. For normal function, this bit should be kept at default value.
112600C0	DAT0_TUNE_CRC	32	**DAT0 Tune Result Register** Records on-line tuning result for DAT0 line
112600C4	DAT1_TUNE_CRC	32	**DAT1 Tune Result Register** Records on-line tuning result for DAT1 line
112600C8	DAT2_TUNE_CRC	32	**DAT2 Tune Result Register** Records on-line tuning result for DAT2 line
112600CC	DAT3_TUNE_CRC	32	**DAT3 Tune Result Register** Records on-line tuning result for DAT3 line
112600D0	CMD_TUNE_CRC	32	**CMD Tune Result Register** Records on-line tuning result for CMD line
112600D4	SDIO_TUNE_WIND	32	**SDIO Tune Window Register 0** Defines tuning window size for SDIO on-line CRC tuning feature

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Address	Name	Width	Register Function
112600F0	PAD_TUNE0	32	**MSDC Pad Tuning Register 0** Configures delay line embedded in pad macro
112600F4	PAD_TUNE1	32	**MSDC Pad Tuning Register 1** Configures delay line embedded in pad macro
112600F8	DAT_RD_DLY0	32	**MSDC Data Delay Line Register 0** Configures delay line embedded in pad macro
112600FC	DAT_RD_DLY1	32	**MSDC Data Delay Line Register 1** Configures delay line embedded in pad macro
11260100	DAT_RD_DLY2	32	**MSDC Data Delay Line Register 2** Configures delay line embedded in pad macro
11260104	DAT_RD_DLY3	32	**MSDC Data Delay Line Register 3** Configures delay line embedded in pad macro
11260110	HW_DBG_SEL	32	**MSDC H/W Debug Selection Register** Selects HW debug output
11260114	MAIN_VER	32	**MSDC Main Version Register** Shows the version code of MSDC IP
11260118	ECO_VER	32	**MSDC ECO Version Register** Shows the ECO version code of MSDC IP

11260000 MSDC_CFG MSDC Configuration Register 02000099

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SCLK STOP SEL				CCKMD		CCKDIV[11:8]			
Type							RW				W1C		RW			
Reset							1				0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CCKDIV[7:0]								CCKSB	BV18PSS	BV18SDT	CCKDRVE	PIO	RST	CCKPD	MSDC
Type	RW								RU	RU	RW	RW	RW	A0	RW	RW
Reset	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1

Bit(s)	Mnemonic	Name	Description
25	SCLKSTOPSEL	SCLK_STOP_SEL	**In DDR mode, stops SCLK when device is idle whether checking SCLK phase or not** 1'b0: Stop sclk not checking SCLK phase 1'b1: Stop sclk checking SCLK phase; fix 1/4T sclk glitch in DDR mode
21:20	CCKMD	CARD_CK_MODE	**MS/SD card clock mode** 2'b00: Use clock divider output divided by msdc_src_ck as msdc_ck. bit[15]~bit[8] should be programmed. 2'b01: Use msdc_src_ck as msdc_ck. bit[15]~bit[8] is ignored. 2'b10: DDR mode; use clock divider output divided by msdc_src_ck as msdc_ck. bit[15]~bit[8] should be programmed. 2'b11: HS400 mode; use clock divider output and use msdc_src_ck as msdc_ck. bit[15]~bit[8] should be programmed.
19:8	CCKDIV	CARD_CK_DIV	**MS/SD card clock divider** Controls clock frequency of serial clock on MS/SD bus. Refer to "Data Line Latching Timing Diagram" and "Response Latching Timing Diagram". For non-DDR mode, msdc_ck equals SD bus clock. (Example: For SDR25 or HS, msdc_ck and SD bus clock will be 50MHz) For DDR mode, msdc_ck denotes MSDC internal clock which will be doubled to SD bus clock. (Example: For DDR50, msdc_ck should be set to 100MHz, and bus clock will be 50MHz.)

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Bit(s)	Mnemonic	Name	Description
			8'b00000000: msdc_ck =(1/2)*msdc_src_ck 8'b00000001: msdc_ck = [1/(4*1)]*msdc_src_ck 8'b00000010: msdc_ck = [1/(4*2)]*msdc_src_ck 8'b00000011: msdc_ck = [1/(4*3)]*msdc_src_ck 8'b00010000: msdc_ck = [1/(4*16)]*msdc_src_ck 8'b11111111: msdc_ck = [1/(4*255)]*msdc_src_ck
7	**CCKSB**	CARD_CK_STABLE	**MS/SD card clock is stable or not** After programming CARD_CK_MODE or CARD_CK_DIV, this bit will immediately become 0 and return to 1 if stable. Poll this register to ensure safety control of MSDC. 1'b0: Clock output is not stable. 1'b1: Clock output is stable.
6	**BV18PSS**	BV_1P8_PASS	**MSDC bus voltage 1.8V detection status** SW should check this bit after BUS_VOL_18V_START_DET turns to 0 from 1. 1'b0: Error in voltage detection 1'b1: No error in voltage detection
5	**BV18SDT**	BV_1P8_START_DET	**MSDC bus voltage 1.8V detection sequence start event** SW writes 1 to this bit to trigger HW outputting 1.8V clock for 1ms and automatically detecting CMD/DAT line sequence for voltage change is passed or not. HW will clear this bit to 0 after the detection is finished. The passed or failed status is stored in bit[6] BUS_VOL_18V_PASS.
4	**CCKDRVE**	CARD_CK_DRV_EN	**SD/MS card bus clock drive enable bit** Set this bit to 1 to enable MSDC bus clock driver. The default bus state depends on MSDC_CFG][1] CARD_CK_PWDN bit. If MSDC_CFG[1] CARD_CK_PWDN=1, the default clock state will be free running. If MSDC_CFG[1] CARD_CK_PWDN=0, the default clock state will be gated to 0. Set this bit to 0 will put the bus state into "tri-state". Default: 1 1'b0: Put the clock pad into tri-state 1'b1: Enable MSDC to drive clock pad. The state of CLK depends on MSDC_CFG[1] CARD_CK_PWDN.
3	**PIO**	PIO_MODE	**MS/SD PIO mode** Selects PIO mode. Default: PIO mode
2	**RST**	RST	**Software reset** Writing 1 to this register will cause internal synchronous reset of MS/SD controller, and it will not reset register settings and DMA controller. The reset sequence is done when this bit becomes 0. SW should wait for this bit to return to 0 after writing 1. 1'b0: MS/SD controller is not in reset state. 1'b1: MS/SD controller is in reset state.
1	**CCKPD**	CARD_CK_PWDN	**MSDC bus clock power-down mode** Controls card clock power-down mode 1'b0: Clock is gated to 0 if no command or data is transmitted. 1'b1: Clock is free running even if no command or data is transmitted. (The clock may still be stopped when MSDC write data are not enough or no space for the next read data.)
0	**MSDC**	MSDC	**Selects MS/SD mode** Configures the controller to be the host of memory stick or host of SD/MMC memory card. The default value is configuring the controller as the host of memory stick. 1'b0: Configure controller to be host of memory stick 1'b1: Configure controller to be host of SD/MMC memory card

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11260004 MSDC_IOCON MSDC IO Configuration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									RD7SPL	RD6SPL	RD5SPL	RD4SPL	RD3SPL	RD2SPL	RD1SPL	RD0SPL
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name			WD3SPL	WD2SPL	WD1SPL	WD0SPL	WDSPLSEL	WDSPL			RDSPLSEL	DDR50CKD	DDLSEL	RDSPL	RSPL	SDR104CKS
Type			RW	RW	RW	RW	RW	RW			RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23	**RD7SPL**	R_D7_SMPL	**Selects read data 7 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
22	**RD6SPL**	R_D6_SMPL	**Selects read data 6 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
21	**RD5SPL**	R_D5_SMPL	**Selects read data 5 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
20	**RD4SPL**	R_D4_SMPL	**Selects read data 4 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
19	**RD3SPL**	R_D3_SMPL	**Selects read data 3 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
18	**RD2SPL**	R_D2_SMPL	**Selects read data 2 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
17	**RD1SPL**	R_D1_SMPL	**Selects read data 1 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
16	**RD0SPL**	R_D0_SMPL	**Selects read data 0 sample** Only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
13	**WD3SPL**	W_D3_SMPL	**Selects SDIO interrupt sample** Only valid when bit 9 is on. 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
12	**WD2SPL**	W_D2_SMPL	**Selects SDIO interrupt sample** Only valid when bit 9 is on. 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge

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Bit(s)	Mnemonic	Name	Description
11	**WD1SPL**	W_D1_SMPL	**Selects SDIO interrupt sample** Only valid when bit 9 is on. 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
10	**WD0SPL**	W_D0_SMPL	**Selects CRC status and SDIO interrupt sample** Only valid when bit 9 is on. 1'b0: Sample CRC Status and SDIO interrupt by external bus clock rising edge 1'b1: Sample CRC Status and SDIO interrupt by external bus clock falling edge
9	**WDSPLSEL**	W_D_SMPL_SEL	**Selects data line rising/falling latch fine-tuning in write transaction** 1'b0: All data line share one value indicated by MSDC_IOCON.W_D_SMPL 1'b1: Each data line has its own selection value indicated by Data line 0: MSDC_IOCON.W_D0_SMPL Data line 1: MSDC_IOCON.W_D1_SMPL Data line 2: MSDC_IOCON.W_D2_SMPL Data line 3: MSDC_IOCON.W_D3_SMPL
8	**WDSPL**	W_D_SMPL	**Selects CRC status and SDIO interrupt sample** 1'b0: Sample CRC Status and SDIO interrupt by external bus clock rising edge 1'b1: Sample CRC Status and SDIO interrupt by external bus clock falling edge
5	**RDSPLSEL**	R_D_SMPL_SEL	**Selects data line rising/falling latch fine-tuning in read transaction** 1'b0: All data line share one value indicated by MSDC_IOCON.R_D_SMPL 1'b1: Each data line has its own selection value indicated by Data line 0: MSDC_IOCON.R_D0_SMPL Data line 1: MSDC_IOCON.R_D1_SMPL Data line 2: MSDC_IOCON.R_D2_SMPL Data line 3: MSDC_IOCON.R_D3_SMPL Data line 4: MSDC_IOCON.R_D4_SMPL Data line 5: MSDC_IOCON.R_D5_SMPL Data line 6: MSDC_IOCON.R_D6_SMPL Data line 7: MSDC_IOCON.R_D7_SMPL
4	**DDR50CKD**	DDR50_DLY_SEL	**Selects DDR50 output clock delay** 1'b0: Use default clock output 1'b1: Delay 1T msdc_src_ck for clock output
3	**DDLSEL**	D_DLYLINE_SEL	**Selects data line delay line fine-tuning** 1'b0: All data line share one delay selection value indicated by PAD_TUNE.PAD_DAT_RD_RXDLY 1'b1: Each data line has its own delay selection value indicated by Data line 0: DAT_RD_DLY0.DAT0_RD_DLY Data line 1: DAT_RD_DLY0.DAT1_RD_DLY Data line 2: DAT_RD_DLY0.DAT2_RD_DLY Data line 3: DAT_RD_DLY0.DAT3_RD_DLY Data line 4: DAT_RD_DLY1.DAT4_RD_DLY Data line 5: DAT_RD_DLY1.DAT5_RD_DLY Data line 6: DAT_RD_DLY1.DAT6_RD_DLY Data line 7: DAT_RD_DLY1.DAT7_RD_DLY
2	**RDSPL**	R_D_SMPL	**Selects read data sample** 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
1	**RSPL**	R_SMPL	**Selects command response sample** 1'b0: Sample response by external bus clock rising edge 1'b1: Sample response by external bus clock falling edge

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Bit(s)	Mnemonic	Name	Description
0	**SDR104CKS**	SDR104_CLK_SEL	**SDR104 SCLK output clock control** Only used when MSDC_CFG[17:16] CARD_CK_MODE is 2'b01. 1'b0: Bus clock output equals inverted msdc_src_ck 1'b1: Bus clock output equals msdc_src_ck

11260008 MSDC_PS MSDC Pin Status Register 01FF0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SDWP							CMD	DAT							
Type	RU							RU	RU							
Reset	0							1	1	1	1	1	1	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CDDBCE														CDSTS	CDEN
Type	RW														RU	RW
Reset	0	0	0	0											1	0

Bit(s)	Mnemonic	Name	Description
31	**SDWP**	SD_WP	**Write Protection switch status on SD memory card** Shows the status of Write Protection switch on SD memory card. There is no default reset value. The pin WP (Write Protection) is only useful when the controller is configured for SD memory card. 1'b0: Write Protection switch on, i.e. memory card will be write-protected. 1'b1: Write Protection switch off, i.e. memory card is writable.
24	**CMD**	CMD	**Command line status** Reflects the command line value of MSDC bus.
23:16	**DAT**	DAT	**Data line status** Reflects the data line value of MSDC bus (8-bit).
15:12	**CDDBCE**	CDDEBOUNCE	**Card detection de-bounce timer** Specifies the time interval for card detection de-bounce. Default value: 0, meaning the de-bounce interval is one 32kHz cycle. The interval will extend one cycle time of 32kHz by increasing the counter by 1.
1	**CDSTS**	CDSTS	**Card detection status** 1'b0: Card detection pin status is logic low. 1'b1: Card detection pin status is logic high.
0	**CDEN**	CDEN	**Enables card detection** Controls the card detection circuit. 1'b0: Disable card detection 1'b1: Enable card detection

1126000C MSDC_INT MSDC Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										AC53FAIL	AC53DONE	GEAROUTBOUND	DMAPROTECT	GPDCSERR	BDCSERR	AC19DONE
Type										W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset										0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SDDC	SDDT	DMA	SDXF	SDCS	SDRC	SDCT	SDCR	SDIO	DMA	SDAC	SDAC	SDAC		MSD	MMC

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	RCERR	O	XFDNE	CPL	TS	RCER	O	DY	IRQ	QEPTY	DRCRCER	DCTO	DCRDY		CCDSC	IRQ
Type	W1C	W1C	W1C	W1C	RU	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C		W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0

Bit(s)	Mnemonic	Name	Description
22	**AC53FAIL**	AUTOCMD53_FAIL	**SD auto command 53 status register** When auto-command 53 tuning sequence fails , this register will be set to 1 by HW.
21	**AC53DONE**	AUTOCMD53_DONE	**SD auto command 53 status register** When auto-command 53 tuning sequence is finished, this register will be set to 1 by HW.
20	**GEAROUTBOUND**	GEAR_OUT_BOUND	**The gear setting of delay line is out of boundary in the process of SDIO Autocmd 53 On-Line tuning**
19	**DMAPROTECT**	DMA_PROTECT	**There is write operation to DMA start address, length, start bit or the last BUF bit.**
18	**GPDCSERR**	GPD_CS_ERR	**GPD checksum error detected**
17	**BDCSERR**	BD_CS_ERR	**BD checksum error detected**
16	**AC19DONE**	AUTOCMD19_DONE	**SD auto command 19 status register** When auto-command 19 is enabled, HW will clear this register to 0. As the tuning sequence is finished (32 times), this register will be set to 1 by HW. SW should check AUTOCMD_STS0 and SUTOCMD_STS1 only when this bit is on.
15	**SDDCRCERR**	SD_DATA_CRCERR	1'b0: Otherwise 1'b1: MS/SD controller detects a CRC error after reading a block of data from the DAT line or SD/MMC signals a CRC error after writing a block of data to the DAT line.
14	**SDDTO**	SD_DATTO	
13	**DMAXFDNE**	DMA_XFER_DONE	**DMA transfer done interrupt** Indicates status of data block transfer. 1'b0: Otherwise 1'b1: A data block is successfully transferred.
12	**SDXFCPL**	SD_XFER_COMPLETE	**SD data transfer completed interrupt** Indicates transaction which contains data that are completed. While performing tuning procedure (Execute Tuning is set to 1), SD_XFER_COMPLETE is not set to 1.
11	**SDCSTS**	SD_CSTS	**SD CSTA update interrupt** Indicates any bit in register SDC_CSTA is active. The register bit will be set to 1. SW should clear SDC_CSTA, and this bit will be de-asserted automatically.
10	**SDRCRCER**	SD_RESP_CRCER	**SD command CRC error interrupt** Indicates SD/MMC controller detects a CRC error after reading a response from the CMD line. 1'b0: Otherwise 1'b1: SD/MMC controller detects a CRC error after reading a response from the CMD line.
9	**SDCTO**	SD_CMDTO	**SD command time-out interrupt** Indicates SD/MMC controller detects a time-out condition while waiting for a response on the CMD line. 1'b0: Otherwise 1'b1: SD/MMC controller detects a time-out condition while waiting for a response on the CMD line.
8	**SDCRDY**	SD_CMDRDY	**SD command ready interrupt** For the command without response, the register bit will be 1 once the

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Bit(s)	Mnemonic	Name	Description
			command is completed on SD/MMC bus. For command with response without busy, the register bit will be 1 whenever the command is issued onto SD/MMC bus and its corresponding response is received without CRC error. For command with response with busy in DAT0, the register bit will be 1 whenever the command is issued onto SD/MMC bus and its corresponding response is received without CRC error and the DAT0 transited from busy to idle. 1'b0: Otherwise 1'b1: Command finished successfully without CRC error.
7	**SDIOIRQ**	SD_SDIOIRQ	**SD SDIO interrupt** Indicates the interrupt is sensed in the SDIO bus. 1'b0: No interrupt on SDIO bus 1'b1: Interrupt on SDIO bus
6	**DMAQEPTY**	DMA_Q_EMPTY	**DMA queue empty interrupt** Indicates the current DMA queue is empty. Only for descriptor mode and enhance mode.
5	**SDACDRCRCER**	SD_AUTOCMD_RESP_CRCERR	**SD auto command CRC error interrupt** Set when detecting a CRC error in the auto command response.
4	**SDACDCTO**	SD_AUTOCMD_CMDTO	**SD auto command time-out interrupt** Set if no response is returned within a specified cycles (64T in spec) from the end bit of auto command.
3	**SDACDCRDY**	SD_AUTOCMD_CMDRDY	**SD auto command ready interrupt** Set if auto command is executed without CRC error or timeout.
1	**MSDCCDSC**	MSDC_CDSC	**MSDC card detection status change interrupt** Indicates if any interrupt for memory card insertion/removal exists. Whenever memory card is inserted or removed and card detection circuit is enabled, i.e. register bit CDEN in register MSDC_PS is set to 1, the register bit will be set to 1. It will be reset when the register is read. 1'b0: Otherwise 1'b1: Card is inserted or removed.
0	**MMCIRQ**	MMC_IRQ	**MMC card interrupt** 1'b0: Otherwise 1'b1: MMC card interrupt event occurs.

11260010 **MSDC_INTEN MSDC Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										**ENAC53FAIL**	**ENAC53DONE**	**ENGEAROUTBOUND**	**ENDMAPROTECT**	**ENGPDCSERR**	**ENBDCSERR**	**ENAC19DONE**
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ENSDDCRCERR**	**ENSDDTO**	**ENDMAXFDNE**	**ENSDXFCPL**	**ENSDCSTA**	**ENSDRCRCER**	**ENSDCTO**	**ENSDCRDY**	**ENSDIOIRQ**	**ENDMAQEPTY**	**ENSDACDRCRCER**	**ENSDACDCTO**	**ENSDACDCRDY**		**ENMSDCCDSC**	**ENMCIRQ**
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0

Bit(s)	Mnemonic	Name	Description
22	**ENAC53FAIL**	EN_AUTOCMD53_FAIL	**Enables auto-command 53 failure interrupt** 1'b0: Disable interrupt

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Bit(s)	Mnemonic	Name	Description
			1'b1: Enable interrupt
21	**ENAC53DONE**	EN_AUTOCMD53_DONE	**Enables auto-command 53 completed interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
20	**ENGEAROUTBOUND**	EN_GEAR_OUT_BOUND	**Enables gear out boundary interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
19	**ENDMAPROTECT**	EN_DMA_PROTECT	**Enables DMA protection interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
18	**ENGPDCSERR**	EN_GPD_CS_ERR	**Enables GPD checksum error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
17	**ENBDCSERR**	EN_BD_CS_ERR	**Enables BD checksum error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
16	**ENAC19DONE**	EN_AUTOCMD19_DONE	**Enables auto-command 19 completed interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
15	**ENSDDCRCERR**	EN_SD_DATA_CRCERR	**Enables SD data CRC error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
14	**ENSDDTO**	EN_SD_DATTO	**Enables SD data timeout interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
13	**ENDMAXFDNE**	EN_SD_DMA_XFER_DONE	**Enables DMA transfer done interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
12	**ENSDXFCPL**	EN_SD_XFER_COMPLETE	**Enables SD data transfer completed interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
11	**ENSDCSTA**	EN_SD_CSTA	**Enables SD CSTA update interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
10	**ENSDRCRCER**	EN_SD_RESP_CRCERR	**Enables SD command CRC error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
9	**ENSDCTO**	EN_SD_CMDTO	**Enables SD command timeout interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
8	**ENSDCRDY**	EN_SD_CMDRDY	**Enables SD command ready interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
7	**ENSDIOIRQ**	EN_SD_SDIOIRQ	**Enables SD SDIO interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
6	**ENDMAQEPTY**	EN_DMA_Q_EMPTY	**Enables DMA queue empty interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
5	**ENSDACDRCRCER**	EN_SD_AUTOCMD_RESP_CRCERR	**Enables SD auto command CRC error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt

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Bit(s)	Mnemonic	Name	Description
4	ENSDACDCTO	EN_SD_AUTOCMD_CMDTO	**Enables SD auto command time-out interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
3	ENSDACDCRDY	EN_AUTOCMD_CMDRDY	**Enables SD auto command ready interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
1	ENMSDCCDSC	EN_MSDC_CDSC	**Enables MSDC card detection status change interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
0	ENMMCIRQ	EN_MMC_IRQ	**Enables MMC card interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt

11260014 MSDC_FIFOCS MSDC FIFO Control and Status Register 7C000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFOCLR	FIFO							TXFIFOCNT							
Type	A0	A0							RU							
Reset	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RXFIFOCNT							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	FIFOCLR	FIFOCLR	**Clears embedded FIFO** Write 1 to this bit to clear FIFO. It will become 0 when FIFO is cleared. SW needs to check this bit to make sure clearing FIFO sequence is done. This bit can be used when the data read/write sequence has error and needs to clean the HW FIFO.
30:24	FIFO	FIFO	
23:16	TXFIFOCNT	TXFIFOCNT	**TX FIFO count for MSDC write** 8'd0: No data in FIFO 8'd1: 1 byte of data in FIFO 8'd2: 2 bytes of data in FIFO 8'd131: Maximum 131 bytes of data in FIFO Others: Reserved
7:0	RXFIFOCNT	RXFIFOCNT	**RX FIFO count for MSDC read** 8'd0: No data in FIFO 8'd1: 1 byte of data in FIFO 8'd2: 2 bytes of data in FIFO 8'd131: Maximum 131 bytes of data in FIFO Others: Reserved

11260018 MSDC_TXDATA MSDC TX Data Port Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PIOTXDATA[31:16]															

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Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**PIOTXDATA[15:0]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**PIOTXDATA**	PIO_TXDATA	**PIO mode TXDATA port** This register can be accessed by byte, half-word or word. This port can only be accessed in PIO mode. Otherwise, the transaction will be discarded.

1126001C MSDC_RXDATA MSDC RX Data Port Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**PIORXDATA[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**PIORXDATA[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**PIORXDATA**	PIO_RXDATA	**PIO mode RXDATA port** This register can be accessed by byte, half-word or word. This port can only be accessed in PIO mode. Otherwise, the transaction will be discarded.

11260030 SDC_CFG SD Configuration Register 00100000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DTOC**										**INTBGP**	**SDIOIDE**	**SDIO**		**BUSWD**	
Type	RW										RW	RW	RW		RW	
Reset	0	0	0	0	0	0	0	0			0	1	0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**ENWKUPINS**	**ENWKUPSDIOINT**
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DTOC**	DTOC	**Data timeout counter** The period from the end of the initial host read command or the last read data block in a multiple block read operation to the start bit of the next read data block requires at least two serial clock cycles. The counter is used to extend the period (Read Data Access Time) in unit of 1,048,576 serial clocks. 8'b00000000: Extend 1,048,576 more serial clock cycles 8'b00000001: Extend 1,048,576*2 more serial clock cycles 8'b00000010: Extend 1,048,576*3 more serial clock cycles

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Bit(s)	Mnemonic	Name	Description
			8'b11111111: Extend 1,048,576*256 more serial clock cycles
21	**INTBGP**	INT_AT_BLOCK_GAP	**Interrupt at block gap** This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Set to 1 will enable interrupt detection at the block gap for a multiple block transfer. Set to 0 will disable interrupt detection during a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0. When the host driver detects an SD card insertion, it will set up this bit according to CCCR of the SDIO card. 1'b0: Disable interrupt detection at block gap 1'b1: Enable interrupt detection at block gap
20	**SDIOIDE**	SDIO_INT_DET_EN	**Enables SDIO interrupt detection** Informs SD controller to sense SDIO interrupt. 1'b0: Disable SDIO interrupt detection 1'b1: Enable SDIO interrupt detection if SDIO bit is also on
19	**SDIO**	SDIO	**SDIO mode enable bit** Enables support to sense SDIO interrupt and disables R4 response CRC check for SDIO card. 1'b0: Disable SDIO mode 1'b1: Enable SDIO mode
17:16	**BUSWD**	BUSWIDTH	**Configures bus width** Defines SD/MMC bus width. 2'b00: 1-bit mode 2'b01: 4-bit mode 2'b10: 8-bit mode 2'b11: Reserved
1	**ENWKUPINS**	WAKEUP_INS_EN	**Card status change wakeup event enable bit** 1'b0: Disable wakeup event for card status change 1'b1: Enable wakeup event for card status change
0	**ENWKUPSDIOINT**	WAKEUP_SDIOINT_EN	**SDIO card interrupt wakeup event enable bit** 1'b0: Disable wakeup event for SDIO card interrupt 1'b1: Enable wakeup event for SDIO card interrupt

11260034 **SDC_CMD** **SD Command Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**ACMD53**	**VOLSWTH**	**ACMD**		**LEN**											
Type	RW	RW	RW		RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**GOIRQ**	**STOP**	**RW**	**DTYPE**			**RSPTYP**			**BREAK**	**CMD**					
Type	RW	RW	RW	RW			RW			RW	RW					
Reset	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**ACMD53**	AUTO_CMD53	**Enables auto command 53** Should be used exclusively with AUTO_CMD, meaning AUTO_CMD != 2'b00. This field should be assigned to 1'b0. If this filed is assigned to 1'b1, AUTO_CMD should be set to 2'b00. 1'b0: Disable Auto Command 53 1'b1: Enable Auto Command 53
30	**VOLSWTH**	VOL_SWTH	**Voltage switch command** 1'b0: Disable voltage switch detection

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Bit(s)	Mnemonic	Name	Description
			1'b1: Enable voltage switch detection
29:28	**ACMD**	AUTO_CMD	**Enables auto command** Determines use of auto command functions. This function can be used in all modes including PIO/Basic DMA/Descriptor DMA/Enhanced Mode. There are two methods to stop multiple-block read and write operation. 1. Enabling auto CMD12 Multiple-block read and write commands for memory require CMD12 to stop the operation. When ACMD-12 is used, MSDC issues CMD12 automatically when the last block transfer is completed. Auto CMD12 error is indicated to the MSDC_INT register. The host driver shall not set up this bit if the command does not require CMD12. In particular, secure commands defined in the Part 3 File Security specification do not require CMD12. 2. Enabling auto CMD23 When ACMD-23 is used, MSDC issues a CMD23 automatically before issuing a command specified in the CMD field. The Host Controller Version 3.00 and later versions support this function. By writing the command register, MSDC issues a CMD23 first then a command specified by the CMD field in the SDC_CMD register. If response errors of CMD23 are detected, the second command will not be issued. A CMD23 error is indicated in the MSDC_INT register. 32-bit block count value for CMD23 is set to the SDC_BLOCK_NUM register. 2'b00: Disable Auto Command 2'b01: Enable Auto CMD12 2'b10: Enable Auto CMD23 2'b11: Enable Re-tuning CMD19
27:16	**LEN**	LEN	**Length** Defines the length of one block (unit: byte) in a data transaction of block mode or the data length (unit: byte) in data transaction of byte mode. The maximum value of block length is 2,048 bytes. 12'b000000000000: Reserved 12'b000000000001: Block length is 1 byte 12'b000000000010: Block length is 2 byte 12'b011111111111: Block length is 2047 byte 12'b100000000000: Block length is 2048 byte
15	**GOIRQ**	GO_IRQ	**GO_IRQ command** Indicates if the command is GO_IRQ_STATE (CMD40) and used only for MMC protocol. If the command is GO_IRQ_STATE, the period between command token and response token will not be limited. 1'b0: The command is not GO_IRQ_STATE 1'b1: The command is GO_IRQ_STATE
14	**STOP**	STOP	**Stop command** Indicates if the command is a stop transmission command. It should be set to 1 when CMD12 (SD/MMC) or CMD52 with I/O abort (SDIO) is to be issued. 1'b0: The command is not a stop transmission command 1'b1: The command is a stop transmission command
13	**RW**	RW	**Selects command read write** The register bit defines the command is a read command or write command. The register bit is valid only when the command causes a transaction with data token. 1'b0: The command is a read command 1'b1: The command is a write command
12:11	**DTYPE**	DTYPE	**Selects data block** Defines data token type for the command. 2'b00: No data token for the command

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Bit(s)	Mnemonic	Name	Description
			2'b01: Single block transaction (only available in block mode) 2'b10: Multiple block transaction. (only available in block mode) 2'b11: Stream operation. It only shall be used in MMC protocol. (only available in block mode)
9:7	**RSPTYP**	RSPTYP	**Command response type** 3'b000: This command has no response. 3'b001: The command has R1/R5/R6/R7 response. The response token is 48-bit with CRC check (For SD/MMC/SDIO) (Not include the SDIO abort command) 3'b010: The command has R2 response. The response token is 136-bit (For SD/MMC) 3'b011: The command has R3 response. The response token is 48-bit response, no CRC check (For SD/MMC) 3'b100: The command has R4 response. The response token is 48-bit without CRC check (For SDIO) The response token is 48-bit with CRC check (For MMC) 3'b111: The command has R1b response. The response token is 48-bit (For SD/MMC/SDIO)
6	**BREAK**	BREAK	**Aborts pending MMC GO_IRQ command** Only valid for a pending GO_IRQ_MODE command waiting for MMC interrupt response. 1'b0: Not a beak command 1'b1: Break a pending MMC GO_IRQ_MODE command in the controller.
5:0	**CMD**	CMD	**SD Memory Card command**

11260038 SDC_ARG SD Argument Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ARG[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ARG[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ARG**	ARG	Memory card controller argument register

1126003C SDC_STS SD Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMC SWR CPL															CMD _WR _BUS Y
Type	RU															W1C
Reset	0															0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CMD BSY	SDCB SY
Type															RU	RU
Reset															0	0

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Bit(s)	Mnemonic	Name	Description
31	**MMCSWRCPL**	MMC_STREAM_WR_COMPL	**MMC stream mode write data are all flushed to MMC card.** SW can use this bit to confirm the last write data are flushed to MMC before issuing the STOP command. This bit is only valid when command SDC_CMD.DTYPE=2'b11. 1'b0: Last Data are partially inside MSDC 1'b1: Last data are flushed to MMC card
16		CMD_WR_BUSY	
1	**CMDBSY**	CMDBUSY	**SD command line busy status** SW should always read this bit to make sure the command line is not busy before sending the next command. If the command is R1B or data read/write command, SW should also check the SDCBUSY bit. Note: When auto command 12 is enabled, this bit will be asserted immediately after SDC_CMD is written and de-asserted after auto-command 12 is finished. 1'b0: No transmission is going on CMD line on SD bus. 1'b1: There is transmission going on CMD line on SD bus.
0	**SDCBSY**	SDCBUSY	**SD controller busy status** 1'b0: SD controller is idle 1'b1: SD controller is busy

11260040 SDC_RESP0 SD Response Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP0[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP0[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP0**	RESP0	Memory card controller response register 0

11260044 SDC_RESP1 SD Response Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP1[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP1[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP1**	RESP1	Memory card controller response register 1

11260048 SDC_RESP2 SD Response Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	**RESP2[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RESP2[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP2**	RESP2	Memory card controller response register 2

1126004C **SDC_RESP3** SD Response Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RESP3[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RESP3[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP3**	RESP3	Memory card controller response register 3

11260050 **SDC_BLK_NUM** SD Block Number Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**BLKNUM[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BLKNUM[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:0	**BLKNUM**	BLOCK_NUMBER	**Memory card controller block number** Indicates block number of data transaction. 32'd0: Reserved 32'd1: 1-data block 32'd2: 2-data block 32'd3: 3-data block 32'hffffffff: 4GB-1 data block

11260054 **SDC_VOL_CHG** SD Voltage Change Wait Time Register 00000145

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VCHGCNT															
Type	RW															
Reset	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	1

Bit(s)	Mnemonic	Name	Description
15:0	VCHGCNT	VOL_CHG_WAIT_CNT	**Defines SD voltage change check wait time** The wait time is clock frequency multiplied by VOL_WAIT_TIME.

11260058 SDC_CSTS SD Card Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSTS[31:16]															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSTS[15:0]															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	CSTS	CSTS	**CSTS** The card status field in the response R1 or R1b field. Each bit can be written 1 to clear individually.

1126005C SDC_CSTS_EN SD Card Status Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSTS_EN[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSTS_EN[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	CSTS_EN	CSTS_EN	**CSTS_EN** Controls which bit of CSTA will generate MSDC_INT.SDCSTA.

11260060 SDC_DATCRC_STS SD Card Data CRC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCSSN								DCSSP							
Type	RU								RU							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
15:8	**DCSSN**	DAT_CRCSTS_NEG	**MSDC DDR mode negative edge read data CRC status** Reflects CRC status of data line[7:0] in DDR mode. The positive edge CRC status is shown in DAT_CRC_STS[7:0]. Only for MSDC read. 1'b0: No CRC error 1'b1: CRC error
7:0	**DCSSP**	DAT_CRCSTS_POS	**MSDC read data CRC status** Reflects CRC status of data line[7:0]. Only for MSDC read. 1'b0: No CRC error 1'b1: CRC error

11260080 **SD_ACMD_RESP** **SD ACMD Response Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ACMDRESP[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACMDRESP[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ACMDRESP**	AUTOCMD_RESP	**SD auto command response register** Stores response[39:8] of ACMD12/ACMD23/ACMD19.

11260084 **SD_ACMD19_TRG** **SD ACMD19 Target Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													ACMDFTSEL			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**ACMDFTSEL**	FINE_TUNE_SEL	**Selects SD auto command 19 test target** After auto-command 19 is triggered, MSDC will only change the phase of the selected one and keep the value of other tuning registers. SW can get the result from AUTOCMD_STS. There are total 32 phases for each delay line. 4'd0: Select PAD_CLK_TXDLY[5:0] as the target to run auto-command19. 4'd1: Select PAD_CMD_RXDLY[5:0] as the target to run auto-command19. 4'd2: Select PAD_DAT_RD_RXDLY[5:0] as the target to run auto-command19. 4'd3: Select PAD_DAT_WR_RXDLY[5:0] as the target to run auto-command19.

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Bit(s)	Mnemonic	Name	Description
			4'd4: Select DAT0_RD_DLY[5:0] as the target to run auto-command19. 4'd5: Select DAT1_RD_DLY[5:0] as the target to run auto-command19. 4'd6: Select DAT2_RD_DLY[5:0] as the target to run auto-command19. 4'd7: Select DAT3_RD_DLY[5:0] as the target to run auto-command19. 4'd8: Select DAT4_RD_DLY[5:0] as the target to run auto-command19. 4'd9: Select DAT5_RD_DLY[5:0] as the target to run auto-command19. 4'd10: Select DAT6_RD_DLY[5:0] as the target to run auto-command19. 4'd11: Select DAT7_RD_DLY[5:0] as the target to run auto-command19. 4'd12: Select CMD_RESP_RXDLY[5:0] as the target to run auto-command19. Others: Reserved

11260088 **SD_ACMD19_STS** **SD ACMD19 Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ACMD19STS[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACMD19STS[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ACMD19STS**	AUTOCMD19_STS	**SD auto command 19 test result register** When auto-command 19 is enabled, HW will automatically try 32 times of command-19 and store the result into this register. This register contains the 1st to 32rd results in bit[0:31].

1126008C **DMA_SA_HIGH4BIT** **DMA Current Address Register of high 4bit** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DMASAHIGH4BIT			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**DMASAHIGH4BIT**	DMA_SURR_ADDR_HIGH4BIT	Sets up the high 4-bit address of start address since the 64G DRAM needs a 36-bit address

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11260090 DMA_SA DMA Start Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMASA[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMASA[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	DMASA	DMA_STR_ADDR	**Start address of DMA address** Sets up the start address of the DMA. In DMA basic mode, this field indicates the source or destination address of the data transfer which depends on the command. In descriptor base DMA, this is the descriptor chain start address.

11260094 DMA_CA DMA Current Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMACA[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMACA[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	DMACA	DMA_CURR_ADDR	**Current address of DMA address** Reads the current address of DMA descriptor chain.

11260098 DMA_CTRL DMA Control Register 00006008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		BSTSZ			SPLIT1K	LASTBF	DMAALIGN	DMAMOD					READYM	DMARSM	DMASTOP	DMASTART
Type		RW			RW	RW	RW	RW					RU	WO	A0	WO
Reset		1	1	0	0	0	0	0					1	0	0	0

Bit(s)	Mnemonic	Name	Description
14:12	BSTSZ	BURST_SIZE	**DMA burst size** Specifies the maximum transfer bytes allowed at the device per DMA burst. This field cannot be modified when the DMA status is 1. 3'd3: 8 Bytes 3'd4: 16 Bytes 3'd5: 32 Bytes 3'd6: 64 Bytes Other: Reserved

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Bit(s)	Mnemonic	Name	Description
11	**SPLIT1K**	DMA_SPLIT_1K	**Specifies split burst when corssing 1K boundary address** 1'b0: 1K boundary not split 1'b1: 1K boundary split
10	**LASTBF**	LAST_BUF	**Last buffer of the basic DMA mode** Indicates the last buffer in basic DMA mode.
9	**DMAALIGN**	DMA_ALIGN	**Specifies address alignment burst size** 1'b0: do not DAM burst size alignment 1'b1: DAM burst size alignment
8	**DMAMOD**	DMA_MODE	**DMA operation mode** Indicates operation mode of DMA. 1'b0: Basic DMA mode 1'b1: Descriptor base DMA mode
3	**READYM**	AHB_READYM	**Only for debugging when DMA hangs** SW checks if AHB bus is ok when GDMA hangs. 1: bus is normal 0: bus not normal
2	**DMARSM**	DMA_RESUME	**DMA resume control register** Resumes DMA transaction. Read always returns to 0.
1	**DMASTOP**	DMA_STOP	**DMA stop control register** Stops DMA transaction. When SW issues STOP command, SW must wait for this bit to be de-asserted or DMA inactive to guarantee stop is done.
0	**DMASTART**	DMA_START	**DMA start control register** Starts DMA transaction. Read always returns to 0.

1126009C **DMA_CFG** **DMA Configuration Register** **00000004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															**OUTBOUNDSTOPDMA**	**DMACHKSUM12B**
Type															RW	RW
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**MSDCACTIVEEN**				**AHBHPROT2EN**							**LOCKDISABLE**	**DSCPCSEN**	**DMASTS**
Type			RW				RW							RW	RW	RU
Reset			0	0			0	0						1	0	0

Bit(s)	Mnemonic	Name	Description
17	**OUTBOUNDSTOPDMA**	OUT_BOUND_STOP_DMA	**Determines whether to stop Enhance DMA if gear setting is out of boundary when sending training data** 1'b0: Enhance DMA continues even when gear setting is out of boundary during training data sending. 1'b1: Enhance DMA stops when gear setting is out of boundary during training data sending.
16	**DMACHKSUM12B**	DMA_CHK_SUM_12B	**Indicates GPD/BD checksum covers 16 bytes or 12 bytes** 1'b0: GPD/BD checksum covers 16 bytes. 1'b1: GPD/BD checksum only covers 12 bytes.
13:12	**MSDCACTIVEEN**	MSDC_ACTIVE_EN	**Indicates how to control msdc_active** 2'b00: dynamic control msdc_active

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Bit(s)	Mnemonic	Name	Description
			2'b01: msdc_active = 0 2'b10: msdc_active = 1 2'b11: Reserved
9:8	**AHBHPROT2EN**	AHB_HPROT_2_EN	**Determines how to control hprot_2 pin of AHB bus** AHB_HPROT_2_EN = 2'b00, and basic DMA mode All the write transfers of a burst will be accessed by bufferable mode except for the last burst of DMA AHB_HPROT2_2_EN=2'b00, and descriptor DMA mode. All write transfers of a burst will be accessed by bufferable mode except for HW own update transfer. 2'b00: dynamic control hprot_2 2'b01: hprot_2 = 0 2'b10: hprot_2 = 1
2	**LOCKDISABLE**	LOCK_DISABLE	**Disables lock to improve EMI efficiency** 1'b0: enable ahb lock 1'b1: disable ahb lock
1	**DSCPCSEN**	DMA_DSCP_CS_EN	**Enables DMA descriptor checksum** This bit is used to enable or disable the descriptor checksum validation function for the descriptor. This field cannot be modified when the DMA status is 1.
0	**DMASTS**	DMA_STATUS	**DMA status** Indicates the status of DMA. 1'b0: DMA engine is inactive 1'b1: DMA engine is active

112600A0 SW_DBG_SEL MSDC S/W Debug Selection Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SWDBGSEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**SWDBGSEL**	DBG_SEL	**Selects MSDC debugging** Reserved.

112600A4 SW_DBG_OUT MSDC S/W Debug Output Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SWDBGO[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SWDBGO[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
31:0	**SWDBGO**	DBG_OUT	**MSDC debugging output** 32-bit output selected by SW_DBG_SEL register

112600A8 DMA_LENGTH DMA Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	XFSZ[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XFSZ[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**XFSZ**	XFER_SIZE	**DMA total transfer size** Specifies the number of DMA transfer byte required for the movement of source data through DMA. This field is only valid in basic DMA mode.

112600B0 PATCH_BIT0 MSDC Patch Bit Register 0 403C0006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PTCH31	PTCH30	PTCH29	PTCH28	PTCH27	PTCH26	PTCH22				PTCH18				PTCH17	PTCH16
Type	RW	RW	RW	RW	RW	RW	RW				RW				RW	RW
Reset	0	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PTCH15	CKGDLYS					INTCKS			DESCUP	PTCH5	PTCH4	PTCH3	PTCH02	PTCH01	
Type	RW	RW					RW			RW	RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	

Bit(s)	Mnemonic	Name	Description
31	**PTCH31**	EN_MMC_DRV_RESP	**Enables MSDC always driving bus when outputting wake-up response (BREAK)** 1'b0: Disable 1'b1: Enable
30	**PTCH30**	DETECT_WR_CRC_TIMEOUT	**Detects MSDC write data CRC phase time-out** 1'b0: Does not detect CRC phase timeout 1'b1: Detect CRC phase timeout
29	**PTCH29**	SPC_ALWAYS_PUSH	**SPC buffer push mechanism** 1'b0: Push the buffer only when read transfer is on-going 1'b1: Always push the buffer
28	**PTCH28**	SDIO_INT_DLY_SEL	**Selects SDIO interrupt latch time** 1'b0: Latch the data line value in internal SDIO interrupt period 1'b1: Latch the data line value in 1 clock delay of internal SDIO interrupt period
27	**PTCH27**	SDC_CMD_CMDFAIL_SEL	**Selects SDIO interrupt period recovery** 1'b0: SDIO interrupt period will re-start after a CMD12 or CMD52 command is issued 1'b1: SDIO interrupt period whenever DAT line is not busy

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Bit(s)	Mnemonic	Name	Description
26	**PTCH26**	SDC_CMD_IDRT_SEL	**Selects SD identification response time** The register bit indicates if the command has a response with NID (i.e. 5 serial clock cycles as defined in SD memory card Specification Part 1 Physical Layer Specification version 1.0) response time. The register bit is valid only when the command has a response token. Thus, the register bit must be set to 1 for CMD2 (ALL_SEND_CID) and ACMD41 (SD_APP_OP_CMD). 1'b0: Otherwise. 1'b1: The command has a response with NID response time.
25:22	**PTCH22**	SDC_CFG_WDOD	**SD Write Data Output Delay** The period from finish of the response for the initial host write command or the last write data block in a multiple block write operation to the start bit of the next write data block requires at least two serial clock cycles. The register field is used to extend the period (Write Data Output Delay) in unit of one serial clock. 4'b0000: No extension 4'b0001: Extend 1 more serial clock cycle 4'b0010: Extend 2 more serial clock cycles 4'b1111: Extend 15 more serial clock cycles
21:18	**PTCH18**	SDC_CFG_BSYDLY	**SD R1B busy detection mode** Only valid for the commands with R1b response. If the command has a response of R1b type, MS/SD controller must monitor the data line 0 for card busy status from the bit time that is two serial clock cycles after the command end bit to check if operations in SD/MMC memory card are finished. The register field is used to expand the time between the command end bit and end of detection period to detect card busy status. If time is up and there is no card busy status on data line 0, the controller will abandon the detection. 4'b0000: No extension 4'b0001: Extend 1 more serial clock cycle 4'b0010: Extend 2 more serial clock cycles 4'b1111: Extend 15 more serial clock cycles
17	**PTCH17**	SDIO_CFG_INTC_SEL	**Selects SDIO interrupt model** 1'b0: When data line [1] = 0, trigger SDIO interrupt event. 1'b1: When data line [3:0] = 4'b1101, trigger SDIO interrupt event
16	**PTCH16**	MSDC_BLKNUM_SEL	**Supports ACMD23 reliable/force pro etc. features** 1'b0: Support ACMD23 reliable/force prog etc. feature 1'b1: Does not support ACMD23 reliable/force prog etc. feature
15	**PTCH15**	MSDC_FIFO_RD_DIS	**Disables MSDC RXFIFO read** 1'b0: Disable FIFO read permission to RXFIFO in PIO mode 1'b1: Enable FIFO read permission to RXFIFO in PIO mode
14:10	**CKGDLYS**	CKGEN_MSDC_DLY_SEL	**Selects CKBUF in CKGEN delay** Total 32 stages.
9:7	**INTCKS**	INT_DAT_LATCH_CK_SEL	**Selects internal MSDC clock phase** Total 8 stages, each stage can delay 1 clock period of msdc_src_ck.
6	**DESCUP**	DESC_UP_SEL	**SD transfer done interrupt should be issued when GPD are updated.** 1'b1: Enable new function to generate SD transfer done interrupt 1'b0: Use old function to generate SD transfer done interrupt
5	**PTCH5**	ACMD53_FAIL_ONE_SHOT	**Determines interrupt method of AUTOCMD53_FAIL** 1'b0: AUTOCMD53_FAIL interrupt will be asserted whenever CMD/DAT CRC error occurs. 1'b1: AUTOCMD53_FAIL interrupt will be asserted only when AUTOCMD53_DONE is asserted if there is CMD/DAT CRC error.
4	**PTCH4**	MASK_ACMD53_CRC_ERR_INTR	**Masks CMD/DAT CRC error interrupt when executing AUTOCMD53 training sequence** 1'b0: Enable CMD/DAT CRC error interrupt when executing

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Bit(s)	Mnemonic	Name	Description
			AUTOCMD53 training sequence 1'b1: Mask CMD/DAT CRC error interrupt when executing AUTOCMD53 training sequence
3	**PTCH3**	RD_DAT_SEL	**Defines to used rising or falling buf data for SDR mode** 1'b0: Used rising buf data for SDR mode 1'b1: Used falling buf data for SDR mode
2	**PTCH02**	DIS_REFLECT_CMDWR_WHEN_BSY	**Enables SD command register write monitor** 1'b0: Enable monitor function 1'b1: Disable monitor function
1	**PTCH01**	EN_SDC_ODD_8BIT_SUP	**Enables SD odd number support for 8-bit data bus** 1'b0: Disable 1'b1: Enable

112600B4 PATCH_BIT1 MSDC Patch Bit Register 1 FFB00009

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MSHBFCKEN	MRCTLCKEN	MWCTLCKEN	MSDCKEN	MACMDCKEN	MVOLDTCKEN	MPSCCKEN	MSPCCKEN	HGDMACKEN		DCMEN	DCMDIVSEL1				SINGLEBURST
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW				RW
Reset	1	1	1	1	1	1	1	1	1		1	1				0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RESETGDMA		BIAS28R0	BIAS28R1	BIAS28R2				GETCRCMARGIN	GETBUSYMARGIN	CMDTA			WRTA		
Type	RW		RW	RW	RW				RW	RW	RW			RW		
Reset	0		0	0	0	0	0	0	0	0	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
31	**MSHBFCKEN**	MSDC_CK_SHBFF_CKEN	**msdc_src_ck clock enable bit for SHBFF** 1'b0: Disable 1'b1: Enable
30	**MRCTLCKEN**	MSDC_CK_RCTL_CKEN	**msdc_src_ck clock enable bit for RCTL** 1'b0: Disable 1'b1: Enable
29	**MWCTLCKEN**	MSDC_CK_WCTL_CKEN	**msdc_src_ck clock enable bit for WCTL** 1'b0: Disable 1'b1: Enable
28	**MSDCKEN**	MSDC_CK_SD_CKEN	**msdc_src_ck clock enable bit for SD** 1'b0: Disable 1'b1: Enable
27	**MACMDCKEN**	MSDC_CK_ACMD_CKEN	**msdc_src_ck clock enable bit for ACMD** 1'b0: Disable 1'b1: Enable
26	**MVOLDTCKEN**	MSDC_CK_VOLDET_CKEN	**msdc_src_ck clock enable bit for VOLDET** 1'b0: Disable 1'b1: Enable
25	**MPSCCKEN**	MSDC_CK_PSC_CKEN	**msdc_src_ck clock enable bit for PSC** 1'b0: Disable 1'b1: Enable
24	**MSPCCKEN**	MSDC_CK_SPC_CKEN	**msdc_src_ck clock enable bit for SPC** 1'b0: Disable 1'b1: Enable

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Bit(s)	Mnemonic	Name	Description
23	**HGDMACKEN**	AHB_CK_GDMA_CKEN	**hclk_ck clock enable bit for GDMA** 1'b0: Disable 1'b1: Enable
21	**DCMEN**	DCM_EN	**Host enabling DCM for low power** When there is no transfer, ahb_ck and msdc_src_ck will be divided from source clk. 1'b1: disable 1'b0: enable
20	**DCMDIVSEL1**	DCM_DIV_SEL1	**For spec4.5 divider msdc_src_ck from source clk; for spec50 divider ahb_ck from source clk** 1'b1: 32 divders from source clk 1'b0: 16 divders from source clk
16	**SINGLEBURST**	ENABLE_SINGLE_BURST	**AHB bus will not support incr1 burst type in the future and will only affect AHB bus MSDC design, not AXI bus design.** 1'b0: HW sends incr1 burst type. 1'b1: HW sends single burst type instead of incr1 type.
15	**RESETGDMA**	RESET_GDMA	**SW can reset GDMA when design hangs.** 1'b1: Reset GDMA 1'b0: Does not reset GDMA
13	**BIAS28R0**	BIAS_EXTBIAS_28NM	**28NM BIAS Controller register 0**
12	**BIAS28R1**	BIAS_EN18IO_28NM	**28NM BIAS Controller register 1**
11:8	**BIAS28R2**	BIAS_TUNE_28NM	**28NM BIAS Controller register 2**
7	**GETCRCMARGIN**	GET_CRC_MARGIN	**Adds margin to get CRC status when card resp CRC does not match spec 2 cycle from endbit** 1'b0: 8 cycles reserved for getting CRC status from write data CRC endbit 1'b1: 16 cycles reserved for getting CRC status from write data CRC endbit
6	**GETBUSYMARGIN**	GET_BUSY_MARGIN	**Adds margin for getting busy state of data0** 1'b0: 1 cycle reserved for getting busy state from SRC status endbit 1'b1: 3 cycles reserved for getting busy state from SRC status endbit
5:3	**CMDTA**	CMD_RSP_TA_CNTR	**CMD response turn-around period** Turn-around cycle = CMD_RSP_TA_CNTR + 2 In USH104 mode, this register should be set to 1. In non-UHS104 mode, this register should be set to 0.
2:0	**WRTA**	WRDAT_CRCS_TA_CNTR	**Write data and CRC status turn-around period** Turn-around cycle = WRDAT_CRCS_TA_CNTR + 2 In USH104 mode, this register should be set to 1. In non-UHS104 mode, this register should be set to 0.

112600B8 **PATCH_BIT2** **MSDC Patch Bit Register 2** **14801801**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRCSTSENSEL			CFGCRCSTS	CFGCRCSTSCNT		CFGCRCSTSEDGE	CFG_CRCSTS_SEL	POPENCNT					RESPSTSENSEL		
Type	RW			RW	RW		RW	RW	RW					RW		
Reset	0	0	0	1	0	1	0	0	1	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFGRESP	CFGRESPCNT			INTCRESP		CFGRDAT	CFGRDATCNT					RESPWAITCNT		SUPPORT6	ENHANCE

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					SEL										4G	GPD
Type	RW	RW			RW		RW	RW					RW		RW	RW
Reset	0	0	0	1	1		0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:29	CRCSTSENSEL	CRCSTS_LATCH_EN_SEL	**Configures latch CRC status enable signal for async FIFO in eMMC45** 3'b000: Latch CRC status enable signal does not delay. 3'b001: Latch CRC status enable signal delays 1T msdc_ck. 3'b010: Latch CRC status enable signal delays 2T msdc_ck. 3'b011: Latch CRC status enable signal delays 3T msdc_ck. 3'b111: Latch CRC status enable signal delays 7T msdc_ck.
28	CFGCRCSTS	CFG_CRCSTS	**Configures CRC status path selection** The setting only uses eMMC4.5 feature. 1'b0: Latch CRC Status select delay-line path 1'b1: Latch CRC Status select async fifo path
27:26	CFGCRCSTSCNT	CFG_CRCSTS_CNT	**Configures how many data are pushed in async FIFO before starting to pop out data from async FIFO** The min. register setting is 1. Do not set it to 0. The setting only uses eMMC4.5 feature. 2'b00: Push 0 data in async FIFO when starting to pop out data from async FIFO 2'b01: Push 1 data in async FIFO when starting to pop out data from async FIFO 2'b10: Push 2 data in async FIFO when starting to pop out data from async FIFO 2'b11: Push 3 data in async FIFO when starting to pop out data from async FIFO
25	CFGCRCSTSEDGE	CFG_CRCSTS_EDGE	**Uses rising async FIFO or falling async FIFO** 1'b0: Async FIFO latch CRC status uses rising async FIFO. 1'b1: Async fifo latch CRC status uses falling async FIFO.
24		CFG_CRCSTS_SEL	**Configures async FIFO path selection** 1'b0: Used normal path in async FIFO 1'b1: Use 2DFF path in async FIFO
23:20	POPENCNT	POP_EN_CNT	**Pop enable counter** Defines how many write pointer and read pointer margin begin to pop up data transfer.
18:16	RESPSTSENSEL	RESP_LATCH_EN_SEL	**Configures latch CMD response enable signal for async FIFO in eMMC45** 3'b000: Latch CMD response enable signal does not delay. 3'b001: Latch CMD response enable signal delays 1T msdc_ck. 3'b010: Latch CMD response enable signal delays 2T msdc_ck. 3'b011: Latch CMD response enable signal delays 3T msdc_ck. 3'b111: Latch CMD response enable signal delays 7T msdc_ck.
15	CFGRESP	CFG_RESP	**Configures CMD Response path selection** The setting only used eMMC4.5 feature. 1'b0: Latch CMD response selects async FIFO path. 1'b1: Latch CMD response selects delay-line path.
14:12	CFGRESPCNT	CFG_RESP_CNT	**Configures how many data are pushed in async FIFO before starting to pop out data from async FIFO** The min. register setting is 1. Do not set it to 0. The setting only uses eMMC4.5 feature. 3'b000: Push 0 data in async FIFO when starting to pop out data from async FIFO 3'b001: Push 1 data in async FIFO when starting to pop out data from async FIFO 3'b111: Push 7 data in async FIFO when starting to pop out data from async FIFO.

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Bit(s)	Mnemonic	Name	Description
11	**INTCRESP SEL**	INTC_RESP_SEL	**Configures BREAK command async FIFO path** 1'b0: Use normal path in async FIFO 1'b1: Use 2DFF path in async FIFO
9	**CFGRDAT**	CFG_RDAT	**Configures read data path** 1'b0: Read data path bypasses delay line. 1'b1: Read data path through delay line
8:4	**CFGRDATCNT**	CFG_RDAT_CNT	**Configures read data path delay line**
3:2	**RESPWAITCNT**	RESP_WAIT_CNT	**Configures CMD response timeout** The timeout cycle is 65T+16*RESP_WAIT_CNT. 2'b00: CMD response timeout is 65T. 2'b01: CMD response timeout is 65T+ 16*1T. 2'b01: CMD response timeout is 65T+ 16*2T. 2'b01: CMD response timeout is 65T+ 16*3T.
1	**SUPPORT64G**	SUPPORT_64G	**Indicates which project supports high 64G DRAM space access** 1'b1: Support 64G DRAM access 1'b0: Does not support 64G DRAM access
0	**ENHANCE GPD**	ENHANCE_WAIT_GPD	**If SW clears int when GPD update has not been finished, the design will hang.** Set this bt to 1 to avoid such issue in enhance write mode. 1'b1: Use new HW code to update GPD in enhance mode 1'b0: Use old HW code

112600C0 **DAT0_TUNE_CRC** **DAT0 Tune Result Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DAT0CRCSTS[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DAT0CRCSTS[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DAT0CRCSTS**	DAT0_CRC_STS	**SDIO auto command 53 test result register** When auto-command 53 is enabled, HW will automatically try TUNE_WINDOW times of command-53 and store CRC result of DAT0 into this register. This register contains the 1st to 32rd results in bit[0:31].

112600C4 **DAT1_TUNE_CRC** **DAT1 Tune Result Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DAT1CRCSTS[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DAT1CRCSTS[15:0]															
Type	RU															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DAT1CRCSTS**	DAT1_CRC_STS	**SDIO auto command 53 test result register** When auto-command 53 is enabled, HW will automatically try TUNE_WINDOW times of command-53 and store CRC result of DAT1 into this register. This register contains the 1st to 32rd results in bit[0:31].

112600C8 DAT2_TUNE_CRC DAT2 Tune Result Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DAT2CRCSTS[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DAT2CRCSTS[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DAT2CRCSTS**	DAT2_CRC_STS	**SDIO auto command 53 test result register** When auto-command 53 is enabled, HW will automatically try TUNE_WINDOW times of command-53 and store CRC result of DAT2 into this register. This register contains the 1st to 32rd results in bit[0:31].

112600CC DAT3_TUNE_CRC DAT3 Tune Result Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DAT3CRCSTS[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DAT3CRCSTS[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DAT3CRCSTS**	DAT3_CRC_STS	**SDIO auto command 53 test result register** When auto-command 53 is enabled, HW will automatically try TUNE_WINDOW times of command-53 and store CRC result of DAT3 into this register. This register contains the 1st to 32rd results in bit[0:31].

112600D0 CMD_TUNE_CRC CMD Tune Result Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CMDCRCSTS[31:16]															
Type	RU															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CMDCRCSTS[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CMDCRCSTS**	CMD_CRC_STS	**SDIO auto command 53 test result register** When auto-command 53 is enabled, HW will automatically try TUNE_WINDOW times of command-53 and store CRC result of CMD into this register. This register contains the 1st to 32rd results in bit[0:31].

112600D4 SDIO_TUNE_WIND SDIO Tune Window Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**TUNEWINDOW**				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0	**TUNEWINDOW**	TUNE_WINDOW	**SDIO auto command 53 tuning window setting** Window range: 1. For CMD PAD Low bound: max(0, PAD_CMD_RXDLY-TUNE_WINDOW) High bound: min(31, PAD_CMD_RXDLY+TUNE_WINDOW) 2. For DAT PAD Low bound: max(0, DAT(0:3)_RD_DLY-TUNE_WINDOW) High bound: min(31: DAT(0:3)_RD_DLY+TUNE_WINDOW)

112600F0 PAD_TUNE0 MSDC Pad Tuning Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CLKTDLY**					**CMDRRDLY**					**CMDRRDLYSEL**	**CMDRDLY**				
Type	RW					RW					RW	RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RXDLYSEL**		**DATRRDLYSEL**	**DATRRDLY**					**DELAYEN**			**DATWRDLY**				
Type	RW		RW	RW					RW			RW				
Reset	0		0	0	0	0	0	0	0			0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:27	**CLKTDLY**	PAD_CLK_TXDLY	**Controls CLK pad TX delay** This register adds delay to CLK phase. Total 32 stages.
26:22	**CMDRRDLY**	PAD_CMD_RESP_RXDLY	**Controls CMD response internal delay line** This register fine-tunes response phase latched by MSDC internal

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Bit(s)	Mnemonic	Name	Description
			clock. Total 32 stages.
21	**CMDRRDLYSEL**	PAD_CMD_RD_RXDLY_SEL	**Decides CMD response passes through data delay line 1 or not** 1'b0: Pass 1'b1: Does not pass
20:16	**CMDRDLY**	PAD_CMD_RXDLY	**Controls CMD pad RX delay line** This register fine-tunes CMD pad macro response latch timing. Total 32 stages.
15	**RXDLYSEL**	PAD_RXDLY_SEL	**Decides RX delay line tune data path or clock path** 1'b0: RX delay line tune data path 1'b1: RX delay line tune clock path
13	**DATRRDLYSEL**	PAD_DAT_RD_RXDLY_SEL	**Decide RX data pass through data delay line 1 or not** 1'b0: Pass 1'b1: Does not pass
12:8	**DATRRDLY**	PAD_DAT_RD_RXDLY	**Controls DAT pad RX delay line (for MSDC read only)** This register fine-tunes DAT pad macro read data latch timing. Total 32 stages.
7	**DELAYEN**	DELAY_EN	**Enables all delay cell toggle when power is on** 1'b0: Disable delay cell toggle default 1'b1: Enable delay cell toggle default
4:0	**DATWRDLY**	PAD_DAT_WR_RXDLY	**Controls write data status internal delay line** This register fine-tunes write status phase latched by MSDC internal clock. Total 32 stages.

112600F4 **PAD_TUNE1** **MSDC Pad Tuning Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											**CMDRRDLY2SEL**	**CMDRDLY2**				
Type											RW	RW				
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**DATRRDLY2SEL**	**DATRRDLY2**												
Type			RW	RW												
Reset			0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
21	**CMDRRDLY2SEL**	PAD_CMD_RD_RXDLY2_SEL	**Decides CMD response passes through data delay line 2 or not** 1'b0: Pass 1'b1: Does not pass
20:16	**CMDRDLY2**	PAD_CMD_RXDLY2	**Controls CMD pad RX delay line 2** This register fine-tunes CMD pad macro response latch timing in data path. Total 32 stages.
13	**DATRRDLY2SEL**	PAD_DAT_RD_RXDLY2_SEL	**Decides RX data pass through data delay line 2 or not** 1'b0: Pass 1'b1: Does not pass
12:8	**DATRRDLY2**	PAD_DAT_RD_RXDLY2	**Controls DAT pad RX delay line 2 (for MSDC read only)** This register fine-tunes DAT pad macro read data latch timing. Total 32 stages.

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112600F8 DAT_RD_DLY0 MSDC Data Delay Line Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT0RDDLY								DAT1RDDLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DAT2RDDLY								DAT3RDDLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	DAT0RDDLY	DAT0_RD_DLY	**Controls DAT0 pad RX delay line (for MSDC RD)** Total 32 stages.
20:16	DAT1RDDLY	DAT1_RD_DLY	**Controls DAT1 pad RX delay line (for MSDC RD)** Total 32 stages.
12:8	DAT2RDDLY	DAT2_RD_DLY	**Controls DAT2 pad RX delay line (for MSDC RD)** Total 32 stages.
4:0	DAT3RDDLY	DAT3_RD_DLY	**Controls DAT3 pad RX delay line (for MSDC RD)** Total 32 stages.

112600FC DAT_RD_DLY1 MSDC Data Delay Line Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT4RDDLY								DAT5RDDLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DAT6RDDLY								DAT7RDDLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	DAT4RDDLY	DAT4_RD_DLY	**Controls DAT4 pad RX delay line (for MSDC RD)** Total 32 stages.
20:16	DAT5RDDLY	DAT5_RD_DLY	**Controls DAT5 pad RX delay line (for MSDC RD)** Total 32 stages.
12:8	DAT6RDDLY	DAT6_RD_DLY	**Controls DAT6 pad RX delay line (for MSDC RD)** Total 32 stages.
4:0	DAT7RDDLY	DAT7_RD_DLY	**Controls DAT7 pad RX delay line (for MSDC RD)** Total 32 stages.

11260100 DAT_RD_DLY2 MSDC Data Delay Line Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT0RDDLY2								DAT1RDDLY2				
Type				RW								RW				

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Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**DAT2RDDLY2**								**DAT3RDDLY2**				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	**DAT0RDDLY2**	DAT0_RD_DLY2	**Controls DAT0 pad RX delay line 2 (for MSDC RD)** Total 32 stages.
20:16	**DAT1RDDLY2**	DAT1_RD_DLY2	**Controls DAT1 pad RX delay line 2 (for MSDC RD)** Total 32 stages.
12:8	**DAT2RDDLY2**	DAT2_RD_DLY2	**Controls DAT2 pad RX delay line 2 (for MSDC RD)** Total 32 stages.
4:0	**DAT3RDDLY2**	DAT3_RD_DLY2	**Controls DAT3 pad RX delay line 2 (for MSDC RD)** Total 32 stages.

11260104 **DAT_RD_DLY3** **MSDC Data Delay Line Register 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**DAT4RDDLY2**								**DAT5RDDLY2**				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**DAT6RDDLY2**								**DAT7RDDLY2**				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	**DAT4RDDLY2**	DAT4_RD_DLY2	**Controls DAT4 pad RX delay line 2 (for MSDC RD)** Total 32 stages.
20:16	**DAT5RDDLY2**	DAT5_RD_DLY2	**Controls DAT5 pad RX delay line 2 (for MSDC RD)** Total 32 stages.
12:8	**DAT6RDDLY2**	DAT6_RD_DLY2	**Controls DAT6 pad RX delay line 2 (for MSDC RD)** Total 32 stages.
4:0	**DAT7RDDLY2**	DAT7_RD_DLY2	**Controls DAT7 pad RX delay line 2 (for MSDC RD)** Total 32 stages.

11260110 **HW_DBG_SEL** **MSDC H/W Debug Selection Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**DBGWSEL**	**DBG3SEL**						**DBG2SEL**							
Type		RW	RW						RW							
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**DBG1SEL**						**DBG0SEL**							
Type			RW						RW							
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
30	**DBGWSEL**	HW_DBG_WRAP_SEL	**Selects HW debug output for wrapper** 0: Select original debug pins 1: Select wrapper debug pins
29:24	**DBG3SEL**	HW_DBG3_SEL	**Selects HW debug output**
23:16	**DBG2SEL**	HW_DBG2_SEL	**Selects HW debug output**
13:8	**DBG1SEL**	HW_DBG1_SEL	**Selects HW debug output**
7:0	**DBG0SEL**	HW_DBG0_SEL	**Selects HW debug output**

11260114 **MAIN_VER** **MSDC Main Version Register** **20140512**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MAINVER[31:16]**															
Type	RO															
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MAINVER[15:0]**															
Type	RO															
Reset	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
31:0	**MAINVER**	MAIN_VER	Main version

11260118 **ECO_VER** **MSDC ECO Version Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**ECOVER[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ECOVER[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ECOVER**	ECO_VER	ECO version

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5.9 AUXADC

5.9.1 Introduction

The auxiliary ADC unit is used to identify the plugged peripheral and perform temperature measurement. There are 16 input channels allowing diverse applications, such as temperature measurement and light sensor.

Each channel only operates in the immediate mode. The time-trigger mode is removed now.
In the immediate mode, the A/D converter samples the value once only when the flag in the AUXADC_CON1 register is set. For example, if the flag IMM0 in AUXADC_CON1 is set, the A/D converter will sample the data for channel 0. The IMM flags have to be cleared and set again to initialize another sampling. The value sampled for channel 0 is stored in register AUXADC_DAT0, and the value for channel 1 is stored in register AUXADC_DAT1 and so on. If the AUTOSET(x) flag in the register AUXADC_CON0 is set, the auto-sampling function will be enabled in channel(x). The A/D converter samples the data for the channel(x) in which the corresponding data register is read. For example, in the case the AUTOSET0 flag is set. When the data register AUXADC_DAT0 is read, the A/D converter will sample the next value for channel 0 immediately.

If multiple channels are selected at the same time, the task will be performed sequentially on every selected channel from high to low channel. For example, if AUXADC_CON1 is set to 0x7f, i.e. all 7 channels are selected, the state machine in the unit will start sampling from channel 6 to channel 0 and saves the values of each input channel in respective registers. The same process also applies to the timer-triggered mode.

The PUWAIT_EN bit in register AUXADC_CON3 is used to power up the analog port in advance, ensuring that the power is ramped up to the stable state before A/D converter starts the conversion. The analog part is automatically powered down after the conversion is completed.

Besides, there are several embedded temperature sensors. The module accepts signals from module of thermal controller to measure the temperature of the embedded sensors. The measurement result is able to be read in the command registers in the module of thermal controller.

5.9.2 Features

Table 5-4 describes the features in the AUXADC module.

Table 5-4. AUXADC: feature list

Item	Main function	Description
1	Immediate analog-digital conversion	In immediate mode, it supports auto-set option. In time-trigger mode, it supports auto-clear option.
2	Background detection and interrupt	The related command registers: AUXADC_DET_VOLT, AUXADC_PERIOD, AUXADC_DEBT, AUXADC_SEL
3	Temperature measurement	

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5.9.3 Block Diagram

SW controls the AUXADC through the APB bus. Once the hardware receives the command, it will trigger AUXADC channel sampling automatically. SW polls the status register or waits for interrupts from the CPU.

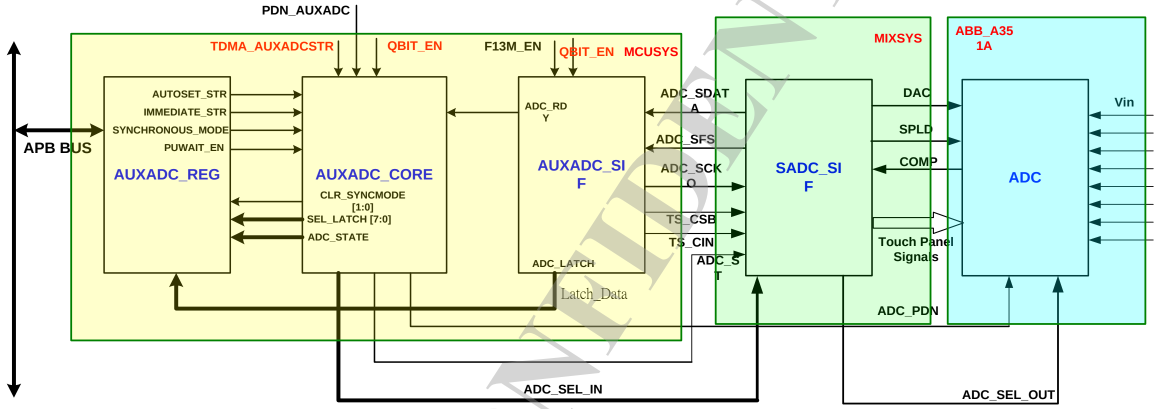

Figure 5-18. Block diagram of AUXADC

5.9.4 Theory of Operation

5.9.4.1 SAR ADC

Successive-approximation-register (SAR) ADC provides low power consumption, cost-effective and medium resolution. The AUXADC is SAR ADC architecture.

Here is an 8-bit conversion example. V_{REF} is the reference voltage of AUXADC.

The AUXADC implements a binary search algorithm. An initial register V_{DA} value compared to the input voltage V_{IN} is the mid-value between (2^8-1) and 0. The value represents V_{REF} /2. If V_{IN} is bigger than V_{DA}, the output of comparison will be 1, and the MSB-bit will be 1. On the contrary, the MSB bit will be 0. Subsequently, bit 7 will be set to 1, and another comparison is done. Bit 6 to bit 0 will be executed as the previous action. Then, the 8-bit digital value will be available.

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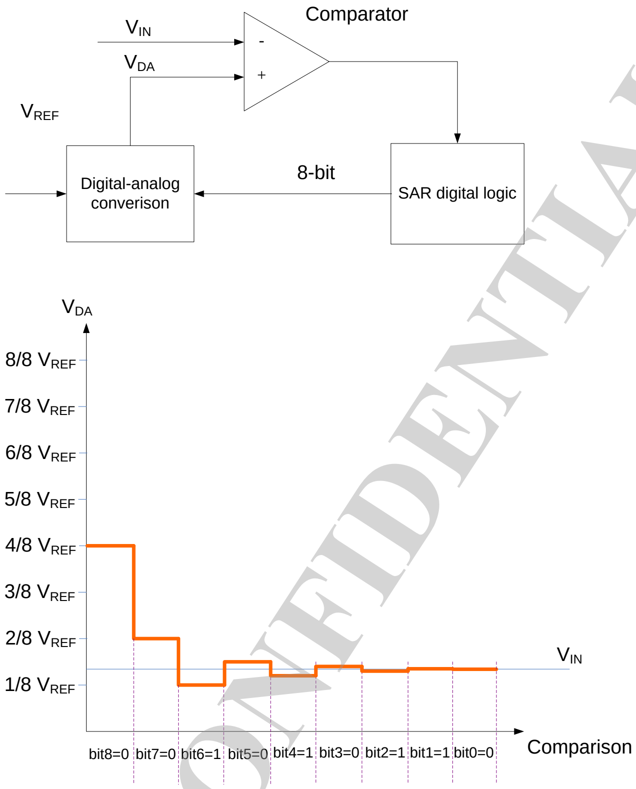

Figure 5-19. SAR ADC architecture and conversion

5.9.4.2 Design Partition

Table 5-5 shows the design partition.

Table 5-5. AUXADC: design partition

Sub module name (hier1)	Description
AUXADC	Top module
AUXADC_REG	APB command registers
AUXADC_SIF	ADC serial interface with the module SADC_SIF
AUXADC_DEBUG	Debugging signal selection
AUXADC_MONITOR	Background detection and generate interrupt
AUXADC_CORE	AUXADC state machine and handle sampling sequence
SADC_SIF	Generate signals to analog part and transfer ADC result to the module AUXADC

5.9.5 Register Definition

Module name: AUXADC Base address: (+11001000h)

Address	Name	Width	Register Function
11001000	AUXADC_CON0	32	**AUXADC Control Register 0** Defines auto-sample mode of the module

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Address	Name	Width	Register Function
			In auto-sample mode, each channel with its sample register being read can start sampling immediately once the read back channel RDY bit is asserted without configuring the control register AUXADC_CON1 again.
11001004	AUXADC_CON1	32	**AUXADC Control Register 1** Controls channel 0~12 immediate mode
11001008	AUXADC_CON1_SET	32	**AUXADC Control Set Register 1** Sets up channel 0~12 immediate mode
1100100C	AUXADC_CON1_CLR	32	**AUXADC Control Clear Register 1** Clears channel 0~12 immediate mode
11001010	AUXADC_CON2	32	**AUXADC Control Register 2** AUXADC SPL control and status
11001014 ~ 11001050	AUXADC_DAT[n] (n=0~15)	32	**AUXADC Channel n Register** Stores sampled data of AUXADC channel n
11001084	AUXADC_DET_VOLT	32	**AUXADC Background Detected Control** Controls background detection
11001088	AUXADC_DET_SEL	32	**AUXADC Background Detected Channel** Background detection channel
1100108C	AUXADC_DET_PERIOD	32	**Background Detection Period** Controls background detection period
11001090	AUXADC_DET_DEBT	32	**Background Detection Debounce** Controls background detection de-bounce
11001094	AUXADC_MISC	32	**AUXADC Misc Control** Controls ADC clock and misc
1100109C	AUXADC_SAMPLE_LIST	32	**AUXADC Sample List** For debugging
110010A0	AUXADC_ABIST_PERIOD	32	**AUXADC ABIST Control** For ABIST mode
110010A4	AUXADC_TST	32	AUXADC Test Control
110010B0	AUXADC_SPL_EN	32	AUXADC SPL Enable
110010B4	AUXADC_SPL_CFG0	32	AUXADC SPL Config0
110010B8	AUXADC_SPL_CFG1	32	AUXADC SPL Config1
110010BC	AUXADC_SPL_CFG2	32	AUXADC SPL Config2
110010C0	AUXADC_SPL_CFG3	32	AUXADC SPL Config3
110010C4	AUXADC_SPL_CFG4	32	AUXADC SPL Config4
110010C8	AUXADC_SPL_CFG5	32	AUXADC SPL Config5
110010CC	AUXADC_SPL_CFG6	32	AUXADC SPL Config6
110010D0	AUXADC_SPL_CFG7	32	AUXADC SPL Config7

11001000 AUXADC_CON0 AUXADC Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOSET15	AUTOSET14	AUTOSET13	AUTOSET12	AUTOSET11	AUTOSET10	AUTOSET9	AUTOSET8	AUTOSET7	AUTOSET6	AUTOSET5	AUTOSET4	AUTOSET3	AUTOSET2	AUTOSET1	AUTOSET0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**AUTOSET15**	AUTOSET15	**Enables auto set for CH15** 0: Not AUTOSET mode 1: AUTOSET mode
14	**AUTOSET14**	AUTOSET14	**Enables auto set for CH14** 0: Not AUTOSET mode 1: AUTOSET mode
13	**AUTOSET13**	AUTOSET13	**Enables auto set for CH13** 0: Not AUTOSET mode 1: AUTOSET mode
12	**AUTOSET12**	AUTOSET12	**Enables auto set for CH12** 0: Not AUTOSET mode 1: AUTOSET mode
11	**AUTOSET11**	AUTOSET11	**Enables auto set for CH11** 0: Not AUTOSET mode 1: AUTOSET mode
10	**AUTOSET10**	AUTOSET10	**Enables auto set for CH10** 0: Not AUTOSET mode 1: AUTOSET mode
9	**AUTOSET9**	AUTOSET9	**Enables auto set for CH09** 0: Not AUTOSET mode 1: AUTOSET mode
8	**AUTOSET8**	AUTOSET8	**Enables auto set for CH08** 0: Not AUTOSET mode 1: AUTOSET mode
7	**AUTOSET7**	AUTOSET7	**Enables auto set for CH07** 0: Not AUTOSET mode 1: AUTOSET mode
6	**AUTOSET6**	AUTOSET6	**Enables auto set for CH06** 0: Not AUTOSET mode 1: AUTOSET mode
5	**AUTOSET5**	AUTOSET5	**Enables auto set for CH05** 0: Not AUTOSET mode 1: AUTOSET mode
4	**AUTOSET4**	AUTOSET4	**Enables auto set for CH04** 0: Not AUTOSET mode 1: AUTOSET mode
3	**AUTOSET3**	AUTOSET3	**Enables auto set for CH03** 0: Not AUTOSET mode 1: AUTOSET mode
2	**AUTOSET2**	AUTOSET2	**Enables auto set for CH02** 0: Not AUTOSET mode 1: AUTOSET mode
1	**AUTOSET1**	AUTOSET1	**Enables auto set for CH01** 0: Not AUTOSET mode

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Bit(s)	Mnemonic	Name	Description
			0: AUTOSET mode
0	**AUTOSET0**	AUTOSET0	**Enables auto set for CH00** 0: Not AUTOSET mode 1: AUTOSET mode

11001004 **AUXADC_CON1** **AUXADC Control Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IMM15	IMM14	IMM13	IMM12	IMM11	IMM10	IMM9	IMM8	IMM7	IMM6	IMM5	IMM4	IMM3	IMM2	IMM1	IMM0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**IMM15**	IMM15	**Channel 15 immediate mode** 0: Channel 15 is not selected. 1: Channel 15 is selected.
14	**IMM14**	IMM14	**Channel 14 immediate mode** 0: Channel 14 is not selected. 1: Channel 14 is selected.
13	**IMM13**	IMM13	**Channel 13 immediate mode** 0: Channel 13 is not selected. 1: Channel 13 is selected.
12	**IMM12**	IMM12	**Channel 12 immediate mode** 0: Channel 12 is not selected. 1: Channel 12 is selected.
11	**IMM11**	IMM11	**Channel 11 immediate mode** 0: Channel 11 is not selected. 1: Channel 11 is selected.
10	**IMM10**	IMM10	**Channel 10 immediate mode** 0: Channel 10 is not selected. 1: Channel 10 is selected.
9	**IMM9**	IMM9	**Channel 9 immediate mode** 0: Channel 9 is not selected. 1: Channel 9 is selected.
8	**IMM8**	IMM8	**Channel 8 immediate mode** 0: Channel 8 is not selected. 1: Channel 8 is selected.
7	**IMM7**	IMM7	**Channel 7 immediate mode** 0: Channel 7 is not selected. 1: Channel 7 is selected.
6	**IMM6**	IMM6	**Channel 6 immediate mode** 0: Channel 6 is not selected. 1: Channel 6 is selected.
5	**IMM5**	IMM5	**Channel 5 immediate mode** 0: Channel 5 is not selected. 1: Channel 5 is selected.

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Bit(s)	Mnemonic	Name	Description
4	**IMM4**	IMM4	**Channel 4 immediate mode** 0: Channel 4 is not selected. 1: Channel 4 is selected.
3	**IMM3**	IMM3	**Channel 3 immediate mode** 0: Channel 3 is not selected. 1: Channel 3 is selected.
2	**IMM2**	IMM2	**Channel 2 immediate mode** 0: Channel 2 is not selected. 1: Channel 2 is selected.
1	**IMM1**	IMM1	**Channel 1 immediate mode** 0: Channel 1 is not selected. 1: Channel 1 is selected.
0	**IMM0**	IMM0	**Channel 0 immediate mode** 0: Channel 0 is not selected. 1: Channel 0 is selected.

11001008 **AUXADC_CON1_SET** **AUXADC Control Set Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				SET12	SET11	SET10	SET9	SET8	SET7	SET6	SET5	SET4	SET3	SET2	SET1	SET0
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12	**SET12**	SET12	Sets up Channel 12 immediate mode
11	**SET11**	SET11	Sets up Channel 11 immediate mode
10	**SET10**	SET10	Sets up Channel 10 immediate mode
9	**SET9**	SET9	Sets up Channel 9 immediate mode
8	**SET8**	SET8	Sets up Channel 8 immediate mode
7	**SET7**	SET7	Sets up Channel 7 immediate mode
6	**SET6**	SET6	Sets up Channel 6 immediate mode
5	**SET5**	SET5	Sets up Channel 5 immediate mode
4	**SET4**	SET4	Sets up Channel 4 immediate mode
3	**SET3**	SET3	Sets up Channel 3 immediate mode
2	**SET2**	SET2	Sets up Channel 2 immediate mode
1	**SET1**	SET1	Sets up Channel 1 immediate mode
0	**SET0**	SET0	Sets up Channel 0 immediate mode

1100100C **AUXADC_CON1_CLR** **AUXADC Control Clear Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

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Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CLR 12	CLR 11	CLR 10	CLR 9	CLR 8	CLR 7	CLR 6	CLR 5	CLR 4	CLR 3	CLR 2	CLR 1	CLR 0
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12	**CLR12**	CLR12	Clears Channel 12 immediate mode
11	**CLR11**	CLR11	Clears Channel 11 immediate mode
10	**CLR10**	CLR10	Clears Channel 10 immediate mode
9	**CLR9**	CLR9	Clears Channel 9 immediate mode
8	**CLR8**	CLR8	Clears Channel 8 immediate mode
7	**CLR7**	CLR7	Clears Channel 7 immediate mode
6	**CLR6**	CLR6	Clears Channel 6 immediate mode
5	**CLR5**	CLR5	Clears Channel 5 immediate mode
4	**CLR4**	CLR4	Clears Channel 4 immediate mode
3	**CLR3**	CLR3	Clears Channel 3 immediate mode
2	**CLR2**	CLR2	Clears Channel 2 immediate mode
1	**CLR1**	CLR1	Clears Channel 1 immediate mode
0	**CLR0**	CLR0	Clears Channel 0 immediate mode

11001014 ~ 11001050 **AUXADC_DAT[n] (n=0~15)** **AUXADC Channel n Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RDY 0	DAT0											
Type				RO	RO											
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12	**RDY0**	RDYn	**AUXADC channel n data ready** Cleared after the register is read. 0: Not ready 1: Ready
11:0	**DAT0**	DATn	**AUXADC channel n data** Stores the sampled data for channel n.

11001084 **AUXADC_DET_VOLT** **AUXADC Background Detected Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	INV				VOL											
Type	RW				RW											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**INV**	INV	**Controls background detected** When the battery voltage is higher or lower than pre-defined voltage (VOLT), the interrupt will be issued to AP. 0: Lower 1: Higher
11:0	**VOL**	VOL	

11001088 **AUXADC_DET_SEL** **AUXADC Background Detected Channel** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CHSEL			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**CHSEL**	CHSEL	**Channel to be sampled in background** 0x0: Channel 0 0x1: Channel 1 ... 0x8: Channel 8 Others: Reserved

1100108C **AUXADC_DET_PERIOD** **Background Detection Period** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			BGDET													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
13:0	**BGDET**	BG_DET_PERIOD	**Background sample period** When this value is not 0, the background detection will be activated automatically and other ADC sampling functions will be stopped. The counter counts by 32K clock. When counter value is bigger than DET_PERIOD, the detection will be activated.

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11001090 **AUXADC_DET_DEBT** **Background Detection Debounce** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			BGTIME													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
13:0	**BGTIME**	BG_DEBT_TIME	**Background de-bounce time** When the number of the detected channel is higher or lower than the pre-defined voltage and exceeds "debounce_time", the interrupt will be issued.

11001094 **AUXADC_MISC** **AUXADC Misc Control** **00000008**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DIV							
Type									RW							
Reset									0	0	0	0	1	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**DIV**	DIV	**Internal divide count value** 0x0~3: Reserved. Should not be used. 0x4: A/D clock = 26MHz clock/4 0x5: A/D clock = 26MHz clock/5 0x6: A/D clock = 26MHz clock/6 0x7: A/D clock = 26MHz clock/7 0x8: A/D clock = 26MHz clock/8 = 3.25MHz (default) 0x9 ~ 0xFF: Programmable

1100109C **AUXADC_SAMPLE_LIST** **AUXADC Sample List** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SAMPLE_LIST															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**SAMPLE_LIST**	SAMPLE_LIST	Hardware sample list for debugging

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110010A0 AUXADC_ABIST_PERIOD AUXADC ABIST Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN	MODE_EN								PERIOD						
Type	RW	RW								RW						
Reset	0	0								0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**EN**	TP_ABIST_EN	**Enables touch panel ABIST mode** TP will sample when TP_ABIST_EN=1 and ABIST_MODE_EN=1. 0: Disable 1: Enable
14	**MODE_EN**	ABIST_MODE_EN	**Enables ABIST mode** 0: Disable 1: Enable
6:0	**PERIOD**	ABIST_SPL_PERIOD	**Period of two different samples** One period is a ADC clock.

110010A4 AUXADC_TST AUXADC Test Control 00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_AUTORPT_PRD													AUXADC_AUTORPT_EN	AUXADC_TEST_SEL	AUXADC_TEST_MODE
Type	RW													RW	RW	RW
Reset	0	0	0	0	0	0	0	1						0	0	0

Bit(s)	Mnemonic	Name	Description
15:8	**AUXADC_AUTORPT_PRD**	AUXADC_AUTORPT_PRD	**Period of auto-start**
2	**AUXADC_AUTORPT_EN**	AUXADC_AUTORPT_EN	**Enables AUXADC auto start mode** 0: Disable 1: Enable
1	**AUXADC_TEST_SEL**	AUXADC_TEST_SEL	**Selects AUXADC test mode** 0: In test mode. CHSEL from GPI 1: In test mode. CHSEL from REG
0	**AUXADC_TEST_**	AUXADC_TEST_MODE	**Enables AUXADC test mode** 0: Disable. Normal mode

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Bit(s)	Mnemonic	Name	Description
	MODE		1: Enable. Use auxadc_test_in from GPI

110010B0 **AUXADC_SPL_EN** **AUXADC SPL Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPLNUM_AUX15_EN	SPLNUM_AUX14_EN	SPLNUM_AUX13_EN	SPLNUM_AUX12_EN	SPLNUM_AUX11_EN	SPLNUM_AUX10_EN	SPLNUM_AUX09_EN	SPLNUM_AUX08_EN	SPLNUM_AUX07_EN	SPLNUM_AUX06_EN	SPLNUM_AUX05_EN	SPLNUM_AUX04_EN	SPLNUM_AUX03_EN	SPLNUM_AUX02_EN	SPLNUM_AUX01_EN	SPLNUM_AUX00_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**SPLNUM_AUX15_EN**	SPLNUM_AUX15_EN	**Enables AUX15 SPL signal duration extension** 0: Disable. SPL duration will be 4T of AUXADC clock only. 1: Enable. Use SPLNUM_AUX15 for this register for SPL duration.
14	**SPLNUM_AUX14_EN**	SPLNUM_AUX14_EN	**Enables AUX14 SPL signal duration extension** 0: Disable. SPL duration will be 4T of AUXADC clock only. 1: Enable. Use SPLNUM_AUX14 for this register for SPL duration.
13	**SPLNUM_AUX13_EN**	SPLNUM_AUX13_EN	**Enables AUX13 SPL signal duration extension** 0: Disable. SPL duration will be 4T of AUXADC clock only. 1: Enable. Use SPLNUM_AUX13 for this register for SPL duration.
12	**SPLNUM_AUX12_EN**	SPLNUM_AUX12_EN	**Enables AUX12 SPL signal duration extension** 0: Disable. SPL duration will be 4T of AUXADC clock only. 1: Enable. Use SPLNUM_AUX12 for this register for SPL duration.
11	**SPLNUM_AUX11_EN**	SPLNUM_AUX11_EN	**Enables AUX11 SPL signal duration extension** 0: Disable. SPL duration will be 4T of AUXADC clock only. 1: Enable. Use SPLNUM_AUX11 for this register for SPL duration.
10	**SPLNUM_AUX10_EN**	SPLNUM_AUX10_EN	**Enables AUX10 SPL signal duration extension** 0: Disable. SPL duration will be 4T of AUXADC clock only. 1: Enable. Use SPLNUM_AUX10 for this register for SPL duration.
9	**SPLNUM_AUX09_EN**	SPLNUM_AUX09_EN	**Enables AUX09 SPL signal duration extension** 0: Disable. SPL duration will be 4T of AUXADC clock only. 1: Enable. Use SPLNUM_AUX09 for this register for SPL duration.
8	**SPLNUM_AUX08_EN**	SPLNUM_AUX08_EN	**Enables AUX08 SPL signal duration extension** 0: Disable. SPL duration will be 4T of AUXADC clock only. 1: Enable. Use SPLNUM_AUX08 for this register for SPL duration.
7	**SPLNUM_AUX07_EN**	SPLNUM_AUX07_EN	**Enables AUX07 SPL signal duration extension** 0: Disable. SPL duration will be 4T of AUXADC clock only. 1: Enable. Use SPLNUM_AUX07for this register for SPL duration.
6	**SPLNUM_AUX06_EN**	SPLNUM_AUX06_EN	**Enables AUX06 SPL signal duration extension** 0: Disable. SPL duration will be 4T of AUXADC clock only. 1: Enable. Use SPLNUM_AUX06 for this register for SPL duration.
5	**SPLNUM_AUX05_EN**	SPLNUM_AUX05_EN	**Enables AUX05 SPL signal duration extension** 0: Disable. SPL duration will be 4T of AUXADC clock only. 1: Enable. Use SPLNUM_AUX05 for this register for SPL duration.

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Bit(s)	Mnemonic	Name	Description
4	**SPLNUM_AUX04_EN**	SPLNUM_AUX04_EN	**Enables AUX04 SPL signal duration extension** 0: Disable. SPL duration will be 4T of AUXADC clock only. 1: Enable. Use SPLNUM_AUX04 for this register for SPL duration.
3	**SPLNUM_AUX03_EN**	SPLNUM_AUX03_EN	**Enables AUX03 SPL signal duration extension** 0: Disable. SPL duration will be 4T of AUXADC clock only. 1: Enable. Use SPLNUM_AUX03 for this register for SPL duration.
2	**SPLNUM_AUX02_EN**	SPLNUM_AUX02_EN	**Enables AUX02 SPL signal duration extension** 0: Disable. SPL duration will be 4T of AUXADC clock only. 1: Enable. Use SPLNUM_AUX02 for this register for SPL duration.
1	**SPLNUM_AUX01_EN**	SPLNUM_AUX01_EN	**Enables AUX01 SPL signal duration extension** 0: Disable. SPL duration will be 4T of AUXADC clock only. 1: Enable. Use SPLNUM_AUX01 for this register for SPL duration.
0	**SPLNUM_AUX00_EN**	SPLNUM_AUX00_EN	**Enables AUX00 SPL signal duration extension** 0: Disable. SPL duration will be 4T of AUXADC clock only. 1: Enable. Use SPLNUM_AUX00 for this register for SPL duration.

110010B4 **AUXADC_SPL_CFG0** **AUXADC SPL Config0** **00002020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPLNUM_AUX01								SPLNUM_AUX00							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8	**SPLNUM_AUX01**	SPLNUM_AUX01	
7:0	**SPLNUM_AUX00**	SPLNUM_AUX00	

110010B8 **AUXADC_SPL_CFG1** **AUXADC SPL Config1** **00002020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPLNUM_AUX03								SPLNUM_AUX02							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8	**SPLNUM_AUX03**	SPLNUM_AUX03	
7:0	**SPLNUM_AUX02**	SPLNUM_AUX02	

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110010BC **AUXADC_SPL_CFG2** **AUXADC SPL Config2** **00002020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPLNUM_AUX05								SPLNUM_AUX04							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8	**SPLNUM_AUX05**	SPLNUM_AUX05	
7:0	**SPLNUM_AUX04**	SPLNUM_AUX04	

110010C0 **AUXADC_SPL_CFG3** **AUXADC SPL Config3** **00002020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPLNUM_AUX07								SPLNUM_AUX06							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8	**SPLNUM_AUX07**	SPLNUM_AUX07	
7:0	**SPLNUM_AUX06**	SPLNUM_AUX06	

110010C4 **AUXADC_SPL_CFG4** **AUXADC SPL Config4** **00002020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPLNUM_AUX09								SPLNUM_AUX08							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8	**SPLNUM_AUX09**	SPLNUM_AUX09	

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Bit(s)	Mnemonic	Name	Description
7:0	**SPLNUM_AUX08**	SPLNUM_AUX08	

110010C8 **AUXADC_SPL_CFG5** **AUXADC SPL Config5** **00002020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SPLNUM_AUX11**								**SPLNUM_AUX10**							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8	**SPLNUM_AUX11**	SPLNUM_AUX11	
7:0	**SPLNUM_AUX10**	SPLNUM_AUX10	

110010CC **AUXADC_SPL_CFG6** **AUXADC SPL Config6** **00002020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SPLNUM_AUX13**								**SPLNUM_AUX12**							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8	**SPLNUM_AUX13**	SPLNUM_AUX13	
7:0	**SPLNUM_AUX12**	SPLNUM_AUX12	

110010D0 **AUXADC_SPL_CFG7** **AUXADC SPL Config7** **00002020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SPLNUM_AUX15**								**SPLNUM_AUX14**							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
15:8	**SPLNUM_AUX15**	SPLNUM_AUX15	
7:0	**SPLNUM_AUX14**	SPLNUM_AUX14	

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5.10 I2C/SCCB Controller

5.10.1 Introduction

I2C (Inter-IC)/SCCB (Serial Camera Control Bus) is a two-wire serial interface. The two signals are SCL and SDA. SCL is a clock signal that is driven by the master. SDA is a bi-directional data signal that can be driven by either the master or the slave. This generic controller supports the master role and conforms to the I2C specification.

5.10.2 Features

- I2C compliant master mode operation
- Adjustable clock speed for LS/FS mode operation
- Supports 7-bit/10-bit addressing
- Supports high-speed mode
- Supports slave clock extension
- START/STOP/REPEATED START condition
- Manual transfer mode
- Multi-write per transfer
- Multi-read per transfer
- Multi-transfer per transaction
- Combined format transfer with length change capability.
- Active drive/wired-and I/O configuration
- Repeated start multiple transfer

5.10.2.1 Manual Transfer Mode

The controller offers manual mode.

When the manual mode is selected, in addition to the slave address register, the controller has a built-in 8-byte deep FIFO which allows MCU to prepare up to 8 bytes of data for a write transfer, or read up to 8 bytes of data for a read transfer.

5.10.2.2 Transfer Format Support

This controller is designed to be as generic as possible in order to support a wide range of devices that may utilize different combinations of transfer formats. Here are the transfer format types supported through different software configurations:

Wording convention note

- Transfer = Anything encapsulated within a Start and Stop or Repeated Start.
- Transfer length = Number of bytes within the transfer
- Transaction = This is the top unit. Everything combined equals 1 transaction.

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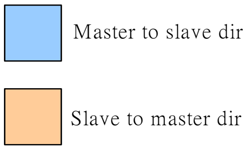
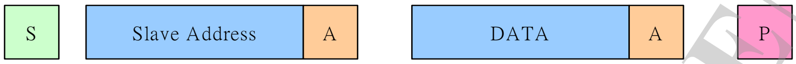
- Transaction length = Number of transfers to be conducted.

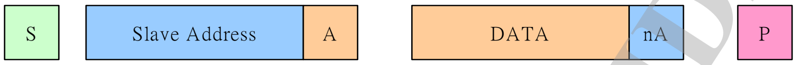


Single byte access

Single Byte Write

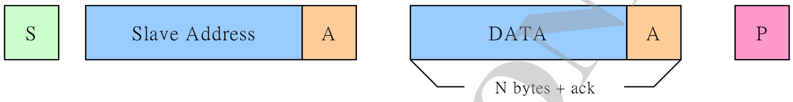


Single Byte Read

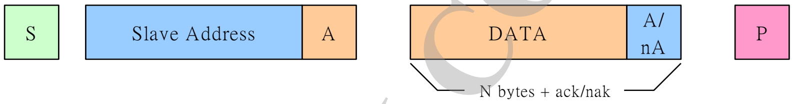


Multi byte access

Multi Byte Write

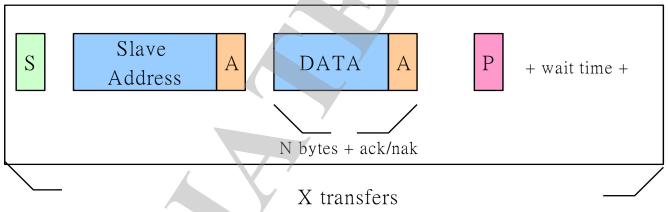


Multi Byte Read

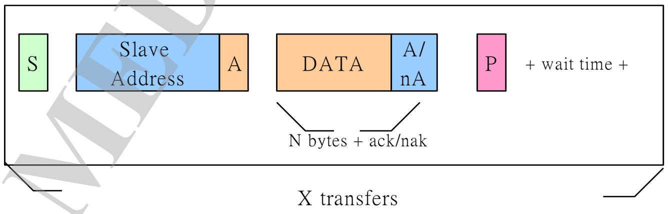


Multi-byte transfer + multi-transfer (same direction)

Multi Byte Write + Multi Transfer



Multi Byte Read + Multi Transfer



Multi-byte transfer + multi-transfer w RS (same direction)

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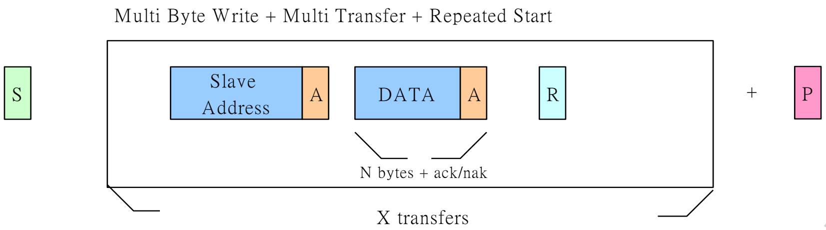
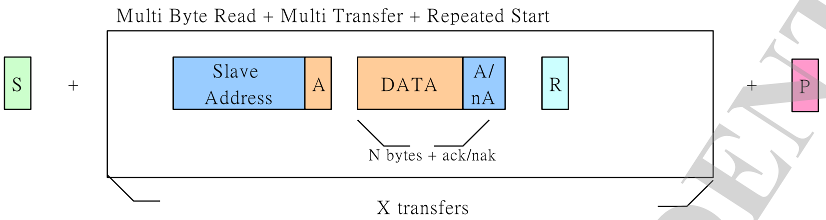
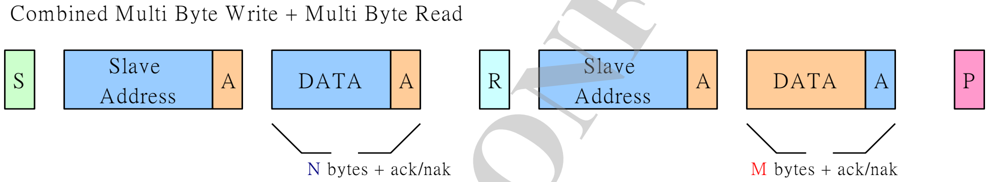


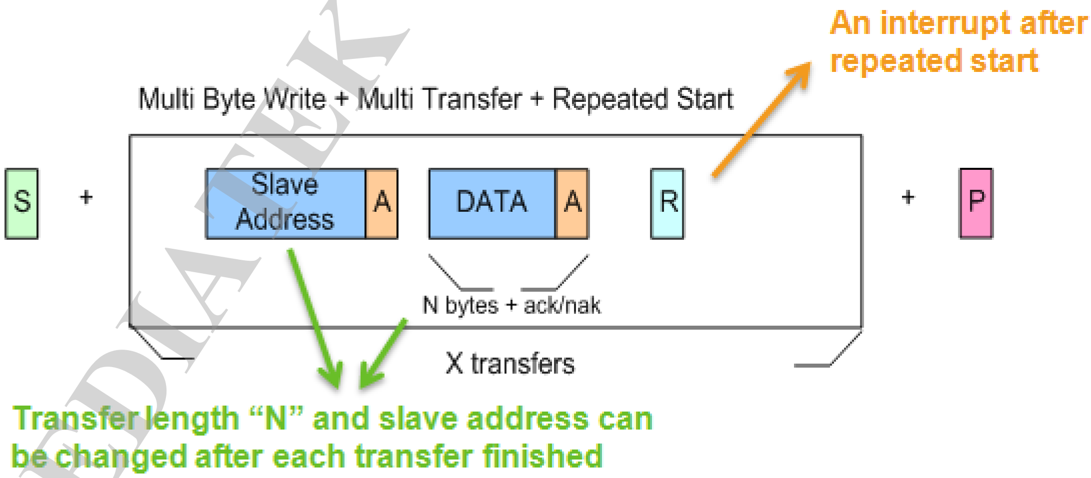


Combined write/read with Repeated Start (direction change)

Note: Only supports write and then read sequence. Read and then write is not supported.



Repeated start multiple transfer (write/read)



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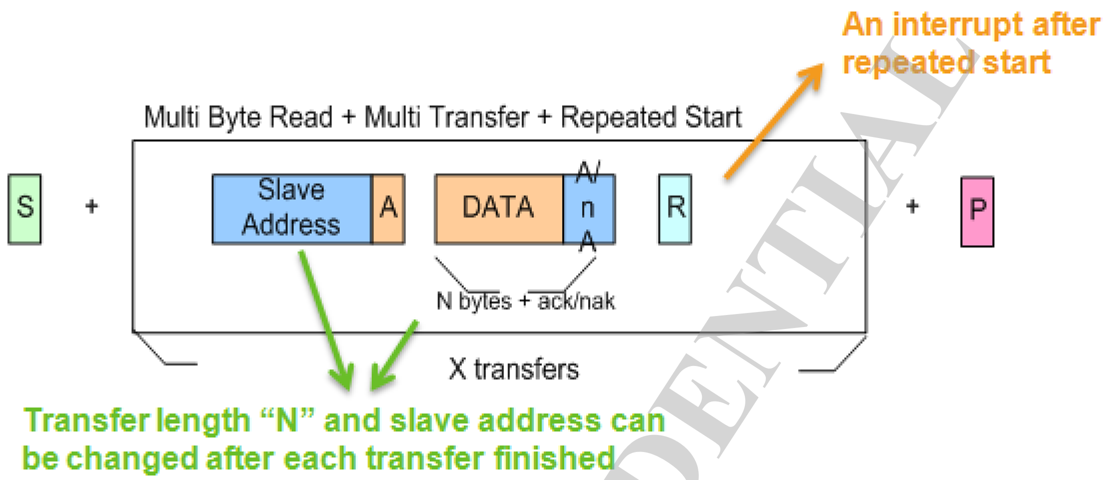

5.10.3 Block Diagram

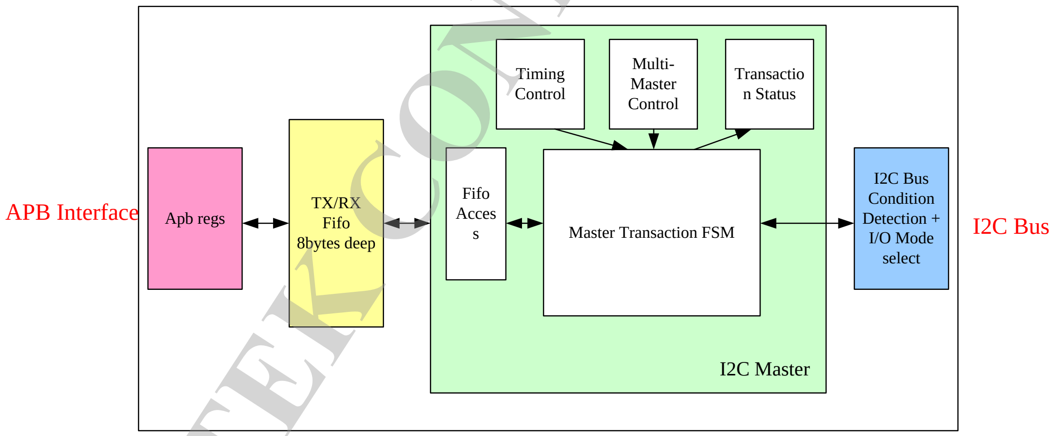

Figure 5-20. Block diagram of I2C

5.10.4 Register Definition

I2C number	Base address	Feature
I2C0	0x11007000	Supports DMA
I2C1	0x11008000	Supports DMA
I2C2	0x11009000	Supports DMA
I2C3	0x1100F000	Supports DMA

There are four I2C IPs in this SOC. The usage of the registers below is the same except that the base address must be changed to respective one.

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Module name: i2c0 Base address: (+11007000h)

Address	Name	Width	Register Function
11007000	DATA_PORT	16	Data Port Register
11007004	SLAVE_ADDR	16	Slave Address Register
11007008	INTR_MASK	16	Interrupt Mask Register
1100700C	INTR_STAT	16	Interrupt Status Register
11007010	CONTROL	16	Control Register
11007018	TRANSAC_LEN	16	Transaction Length Register (Number of Transfers per Transaction)
1100701C	DELAY_LEN	16	Inter Delay Length Register
11007020	TIMING	16	**Timing Control Register** LS/FS only. This register is used to control the output waveform timing. Each half pulse width, i.e. each high or low pulse, is equal to (step_cnt_div+1)*(sample_cnt_div +1)/13MHz
11007024	START	16	Start Register
11007028	EXT_CONF	16	Extension Configuration Register
11007030	FIFO_STAT	16	FIFO Status Register
11007034	FIFO_THRESH	16	**FIFO Thresh Register** For debugging only. By default these values do not need to be adjusted. Note that for Rx, no time-out mechanism is implemented. Therefore, RX_trig_thresh must be left at 0, or there will be data left in FIFO that is not fetched by DMA controller.
11007038	FIFO_ADDR_CLR	16	FIFO Address Clear Register
11007040	IO_CONFIG	16	**IO Config Register** Configures I/O for the SDA and SCL lines to select between normal I/O mode or open-drain mode to support wired-and bus.
11007044	DEBUG	16	**Reserved Debug Register** *Note: This register is for debugging only. The bits are R/W. Do not change the default values.*
11007048	HS	16	**High Speed Mode Register** Contains options for supporting high-speed operation features. Each HS half pulse width, i.e. each high or low pulse, is equal to (step_cnt_div+1)*(sample_cnt_div+1)/13MHz
11007050	SOFTRESET	16	Soft Reset Register
11007054	I2C0_I2CREG_HW_CG_EN	16	HW DCM Enable
11007064	DEBUGSTAT	16	Debug Status Register
11007068	DEBUGCTRL	16	Debug Control Register
1100706C	TRANSFER_LEN_AUX	16	Transfer Length Register (Number of Bytes per Transfer)

11007000 DATA_PORT Data Port Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DATA_PORT							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	DATA_PORT	DATA_PORT	**This is the FIFO access port.** During master write sequences (slave_addr[0] = 0), this port can be written by APB, and during master read sequences (slave_addr[0] =

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Bit(s)	Mnemonic	Name	Description
			1), this port can be read by APB. *Note: Slave_addr must be set correctly before accessing FIFO.* (For debugging only) If the fifo_apb_debug bit is set, the FIFO can be read and written by APB.

11007004 SLAVE_ADDR Slave Address Register 00BF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**SLAVE_ADDR**							
Type									RW							
Reset									1	0	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
7:0	**SLAVE_ADDR**	SLAVE_ADDR	**Specifies slave address of device to be accessed** Bit 0 is defined by I2C protocol as a bit that indicates the direction of transfer 0: Master write 1: Master read

11007008 INTR_MASK Interrupt Mask Register 00FF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**Spare**				**MAS_ARB_LOST**	**MAS_HS_NACKER**	**MAS_ACKERR**	**MAS_TRANSAC_COMP**
Type									RW				RW	RW	RW	RW
Reset									1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
7:4	**Spare**	SPARE	
3	**MAS_ARB_LOST**	MAS_ARB_LOST	Set to 0 to mask ARB_LOST interrupt signal.
2	**MAS_HS_NACKER**	MAS_HS_NACKER	Set to 0 to mask HS_NACKERR interrupt signal.
1	**MAS_ACKERR**	MAS_ACKERR	Set to 0 to mask ACK_ERR interrupt signal.
0	**MAS_TRANSAC_COMP**	MAS_TRANSAC_COMP	Set to 0 to mask TRANSAC_COMP interrupt signal.

1100700C INTR_STAT Interrupt Status Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**RS_MULTIPLE**	**ARB_LOST**	**HS_NACKERR**	**ACKERR**	**TRANSAC_COMP**
Type												W1C	W1C	W1C	W1C	W1C
Reset												0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
4		RS_MULTIPLE	
3	**ARB_LOST**	ARB_LOST	**This status is asserted if the I2C controller loses arbitration.**
2	**HS_NACKERR**	HS_NACKERR	**This status is asserted if HS master code NACK error detection is enabled.** If enabled, HS master code NACK ERR will cause transaction to end and stop will be issued.
1	**ACKERR**	ACKERR	**This status is asserted if ACK error detection is enabled.** If enabled, ACKERR will cause transaction to end and stop will be issued.
0	**TRANSAC_COMP**	TRANSAC_COMP	**This status is asserted when an transaction has completed successfully.**

11007010 CONTROL Control Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**TRANSFER_LEN_CHANGE**	**ACKERR_DET_EN**	**DIR_CHANGE**	**CLK_EXT_EN**	**DMA_EN**	**RS_STOP**	
Type										RW	RW	RW	RW	RW	RW	
Reset										0	0	0	0	0	0	

Bit(s)	Mnemonic	Name	Description
6	**TRANSFER_LEN_CHANGE**	TRANSFER_LEN_CHANGE	**Specifies whether or not to change the transfer length after the first transfer is completed** If enabled, the transfers after the first transfer will use the transfer_len_aux parameter.
5	**ACKERR_DET_EN**	ACKERR_DET_EN	**Enables slave ack error detection.** When enabled, if slave ack error is detected, the master shall terminate the transaction by issuing a STOP condition and then asserts ackerr interrupt. MCU shall handle this case appropriately and then resets the FIFO address before reissuing transaction again. If this option is disabled, the controller will ignore slave ack error and keep on scheduled transaction. 0: Disable 1: Enable
4	**DIR_CHANGE**	DIR_CHANGE	**For combined transfer format** The direction of transfer is to be changed from write to read after the first RS condition *Note: When set to 1, the transfers after the direction change will base on the transfer_len_aux parameter.* 0: Disable 1: Enable
3	**CLK_EXT_EN**	CLK_EXT_EN	**I2C spec allows slaves to hold the SCL line low if it is not yet ready for further processing** Therefore, if this bit is set to 1, the master controller will enter a high wait state until the slave releases the SCL line.
2	**DMA_EN**	DMA_EN	**By default, this is disabled, and FIFO data shall be manually prepared by MCU.** This default setting should be used for transfer sizes of less than 8 data bytes and no multiple transfer is configured. When enabled, DMA requests are turned on, and the FIFO data should be prepared in memory.

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Bit(s)	Mnemonic	Name	Description
1	**RS_STOP**	RS_STOP	**In LS/FS mode, this bit affects multi-transfer transaction only.** It controls whether or not REPEATED-START condition is used between transfers. The last ending transfer always ends with a STOP. In HS mode, this bit must be set to 1. 0: Use STOP 1: Use REPEATED-START

11007018 TRANSAC_LEN Transaction Length Register (Number of Transfers per Transaction) 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TRANSFER_LEN							
Type									RW							
Reset									0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
7:0	**TRANSFER_LEN**	TRANSFER_LEN	**Indicates the number of transfers to be transferred in 1 transaction unit** *Note: The value must be set to be bigger than 1; otherwise no transfer will take place.*

1100701C DELAY_LEN Inter Delay Length Register 0002

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DELAY_LEN							
Type									RW							
Reset									0	0	0	0	0	0	1	0

Bit(s)	Mnemonic	Name	Description
7:0	**DELAY_LEN**	DELAY_LEN	**Sets up wait delay between consecutive transfers when the RS_STOP bit is set to 0** The unit is the same as half pulse width.

11007020 TIMING Timing Control Register 1303

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_READ_ADJ	DATA_READ_TIME				SAMPLE_CNT_DIV					STEP_CNT_DIV					
Type	RW	RW				RW					RW					
Reset	0	0	0	1		0	1	1			0	0	0	0	1	1

Overview LS/FS only. This register is used to control the output waveform timing. Each half pulse width, i.e. each high or low pulse, is equal to (step_cnt_div+1)*(sample_cnt_div +1)/13MHz

Bit(s)	Mnemonic	Name	Description
15	**DATA_READ_ADJ**	DATA_READ_ADJ	**When set to 1, data latch in sampling time during master reads are adjusted according to DATA_READ_TIME value.** Otherwise, by default data are latched in at half of the high pulse

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Bit(s)	Mnemonic	Name	Description
			width point. This value must be set to smaller than or equal to half the high pulse width.
14:12	**DATA_READ_TIME**	DATA_READ_TIME	**Valid only when DATA_READ_ADJ is set to 1** This can be used to adjust so that data are latched in at earlier sampling points (assume data are settled by then).
10:8	**SAMPLE_CNT_DIV**	SAMPLE_CNT_DIV	**Used for LS/FS only** Adjusts the width of each sample. Sample width = sample_cnt_div*1/13MHz
5:0	**STEP_CNT_DIV**	STEP_CNT_DIV	**Specifies the number of samples per half pulse width, i.e. each high or low pulse**

11007024 START Start Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RS_STOP_MULTIPLE_CONFIG	RS_STOP_MULTIPLE_TRIG	RS_STOP_MULTIPLE_TRIG_CLR													START
Type	RW	RW	RO													RW
Reset	0	0	0													0

Bit(s)	Mnemonic	Name	Description
15	**RS_STOP_MULTIPLE_CONFIG**	RS_STOP_MULTIPLE_CONFIG	**Enables multiple r/w & length & slave address with rs_stop transfer**
14	**RS_STOP_MULTIPLE_TRIG**	RS_STOP_MULTIPLE_TRIG	**Triggers the next transfer when enabling multiple r/w & length & slave address with rs_stop transfer**
13	**RS_STOP_MULTIPLE_TRIG_CLR**	RS_STOP_MULTIPLE_TRIG_CLR	**Clears rs_stop_mul_trig for the next transfer**
0	**START**	START	**Starts transaction on bus** It is auto de-asserted at the end of transaction.

11007028 EXT_CONF Extension Configuration Register 1800

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXT_TIME															EXT_EN
Type	RW															RW
Reset	0	0	0	1	1	0	0	0								0

Bit(s)	Mnemonic	Name	Description
15:8		EXT_TIME	**Configurable extension time of start condition.** Time unit: 1/4*BASE_CLOCK_PERIOD *Note: The max. value is {0xFF-SAMPLE_CNT_DIV}.*
0	**EXT_EN**	EXT_EN	**Used for standard mode only** Baud rate is up to 100kHz. This option decides to perform the extension of start/stop condition. If enabled, perform the extension;

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Bit(s)	Mnemonic	Name	Description
			others not. 0: Disable 1: Enable

11007030 **FIFO_STAT** **FIFO Status Register** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RD_ADDR**				**WR_ADDR**				**FIFO_OFFSET**						**WR_FULL**	**RD_EMPTY**
Type	RO				RO				RO						RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0			0	1

Bit(s)	Mnemonic	Name	Description
15:12	**RD_ADDR**	RD_ADDR	**Current RD address pointer** Only bit [2:0] has physical meaning.
11:8	**WR_ADDR**	WR_ADDR	**Current WR address pointer** Only bit [2:0] has physical meaning.
7:4	**FIFO_OFFSET**	FIFO_OFFSET	
1	**WR_FULL**	WR_FULL	**Indicates FIFO is full**
0	**RD_EMPTY**	RD_EMPTY	**Indicates FIFO is empty**

11007034 **FIFO_THRESH** **FIFO Thresh Register** **0700**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**TX_TRIG_THRESH**								**RX_TRIG_THRESH**		
Type						RW								RW		
Reset						1	1	1						0	0	0

Overview For debugging only. By default these values do not need to be adjusted. Note that for Rx, no time-out mechanism is implemented. Therefore, RX_trig_thresh must be left at 0, or there will be data left in FIFO that is not fetched by DMA controller.

Bit(s)	Mnemonic	Name	Description
10:8	**TX_TRIG_THRESH**	TX_TRIG_THRESH	When Tx FIFO level is below this value, Tx DMA request will be asserted.
2:0	**RX_TRIG_THRESH**	RX_TRIG_THRESH	When Rx FIFO level is above this value, Rx DMA request will be asserted.

11007038 **FIFO_ADDR_CLR** **FIFO Address Clear Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**FIFO_ADDR_CLR**

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Type																WO
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**FIFO_ADDR_CLR**	FIFO_ADDR_CLR	When written with 1, 1 pulse fifo_addr_clr will be generated to clear the FIFO address back to 0.

11007040 IO_CONFIG IO Config Register 0003

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													IDLE_OE_EN	IO_SYNC_EN	SDA_IO_CONFIG	SCL_IO_CONFIG
Type													RW	RW	RW	RW
Reset													0	0	1	1

Overview Configures I/O for the SDA and SCL lines to select between normal I/O mode or open-drain mode to support wired-and bus.

Bit(s)	Mnemonic	Name	Description
3	**IDLE_OE_EN**	IDLE_OE_EN	0: Does not drive bus in idle state 1: Drive bus in idle state
2	**IO_SYNC_EN**	IO_SYNC_EN	**Reserved for debugging only** When set to 1, SCL and SDA inputs will be the first dual synced by bclk_ck. This should not be required.
1	**SDA_IO_CONFIG**	SDA_IO_CONFIG	0: Normal tristate I/O mode 1: Open-drain mode
0	**SCL_IO_CONFIG**	SCL_IO_CONFIG	0: Normal tristate I/O mode 1: Open-drain mode

11007044 DEBUG Reserved Debug Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														DEBUG		
Type														RW		
Reset														0	0	0

Overview Note: This register is for debugging only. The bits are R/W. Do not change the default values.

Bit(s)	Mnemonic	Name	Description
2:0	**DEBUG**	DEBUG	

11007048 HS High Speed Mode Register 0102

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		HS_SAMPLE_CNT_DIV				HS_STEP_CNT_DIV				MASTER_CODE					HS_NACKERR_DET_EN	HS_EN
Type		RW				RW				RW					RW	RW

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Reset		0	0	0		0	0	1		0	0	0			1	0

Overview Contains options for supporting high-speed operation features. Each HS half pulse width, i.e. each high or low pulse, is equal to (step_cnt_div+1)*(sample_cnt_div+1)/13MHz

Bit(s)	Mnemonic	Name	Description
14:12	**HS_SAMPLE_CNT_DIV**	HS_SAMPLE_CNT_DIV	**When high speed mode is entered after the master code transfer has been completed, the sample width will depend on this parameter.**
10:8	**HS_STEP_CNT_DIV**	HS_STEP_CNT_DIV	**When high speed mode is entered after the master code transfer has been completed, the number of samples per half pulse width will depend on this value.**
6:4	**MASTER_CODE**	MASTER_CODE	**3-bit programmable value for the master code to be transmitted**
1	**HS_NACKERR_DET_EN**	HS_NACKERR_DET_EN	**Enables NACKERR detection during the master code transmission** When enabled, if NACK is not received after master code has been transmitted, the transaction will be terminated with a STOP condition.
0	**HS_EN**	HS_EN	**Enables high speed transaction** *Note: rs_stop must be set to 1, too.*

11007050 **SOFTRESET** **Soft Reset Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**SOFT_RESET**
Type																WO
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**SOFT_RESET**	SOFT_RESET	When written with 1, 1 pulse soft reset will be used as synchronous reset to reset I2C internal hardware circuits.

11007054 **I2C0_I2CREG_HW_CG_EN** **HW DCM Enable** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**DCM_EN**
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0		DCM_EN	**Enables HW DCM function** Default: Disable 0: Disable 1: Enable

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11007064 DEBUGSTAT Debug Status Register 0020

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BUS_BUSY	MASTER_WRITE	MASTER_READ	MASTER_STATE				
Type									RU	RU	RU	RU				
Reset									0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7	**BUS_BUSY**	BUS_BUSY	**For debugging only** Valid when bus_detect_en is 1. bus_busy = 1 indicates a start transaction has been detected and no stop condition has been detected yet.
6	**MASTER_WRITE**	MASTER_WRITE	**For debugging only** 1: Current transfer is in master write dir.
5	**MASTER_READ**	MASTER_READ	**For debugging only** 1: Current transfer is in master read dir.
4:0	**MASTER_STATE**	MASTER_STATE	**For debugging only** Reads back the current master_state. 0: Idle state 1: I2C master is preparing for sending out the start bit, SCL=1, SDA=1 2: I2C master is sending out the start bit, SCL=1, SDA=0 3: I2C master/slave is preparing for transmitting data bit, SCL=0, SDA=data bit (data bit can be changed when SCL=0) 4: I2C master/slave is transmitting data bit, SCL=1, SDA=data bit (data bit is stable when SCL=1) 5: I2C master/slave is preparing for transmitting ack bit, SCL=0, SDA=ack (ack bit can be changed when SCL=0) 6: I2C master/slave is transmitting ack bit, SCL=1, SDA=0 (ack bit is stable when SCL=1) 7: I2C master is preparing for sending out stop bit or repeated-start bit, SCL=0, SDA=0/1 (0: stop bit; 1: repeated-start bit) 8: I2C master is sending out stop bit or repeated-start bit, SCL=1, SDA=1/0 (1: stop bit; 0: repeated-start bit); 9: I2C master is in delay start between two transfers, SCL=1, SDA=1 10: I2C master is in FIFO wait state. For writing transaction, it means FIFO is empty and I2C master is waiting for DMA controller to write data into FIFO. For reading transaction, it means FIFO is full and I2C master is waiting for DMA controller reading data from FIFO, SCL=0, SDA=don't care 12: I2C master is preparing for sending out data bit of master code. This state is used only in high-speed transaction, SCL=0, SDA=data bit of master code (data bit of master code can be changed when SCL=0) 13: I2C master is sending out data bit of master code. This state is used only in high-speed transaction, SCL=1, SDA=data bit of master code (data bit of master code is stable when SCL=1) 14: I2C master/slave is preparing for transmitting nack bit, SCL=0, SDA=nack bit (nack bit can be changed when SCL=0). This state is used only in high-speed transaction. 15: I2C master/slave is transmitting nack bit, SCL=1, SDA=1; This state is used only in high-speed transaction.

11007068 DEBUGCTRL Debug Control Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name															APB_DEBUG_RD	FIFO_APB_DEBUG
Type															WO	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	APB_DEBUG_RD	APB_DEBUG_RD	**Valid only when fifo_apb_debug is set to 1. Writing to this register will generate a 1 pulsed FIFO APB RD signal for reading the FIFO data.**
0	FIFO_APB_DEBUG	FIFO_APB_DEBUG	**For trace 32 debugging** When trace 32 is used and the memory map is shown, turning on this bit will block the normal APB read access. APB read access to FIFO will then be enabled by writing to apb_debug_rd. 0: Disable 1: Enable

1100706C **TRANSFER_LEN_AUX** **Transfer Length Register (Number of Bytes per Transfer)** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANSFER_LEN_AUX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
15:0	TRANSFER_LEN_AUX	TRANSFER_LEN_AUX	**Valid only when dir_change or transfer_len_change is set to 1.** Indicates the number of data bytes to be transferred in 1 transfer unit (excluding slave address byte) for the transfers following the direction change. That is, if dir_change =1, the first write transfer length will depend on transfer_len, and the second read transfer length depends on transfer_len_aux. Dir change is always after the first transfer. *Note: The value must be set to be bigger than 1; otherwise no transfer will take place.*

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5.11 Pulse-Width Modulation (PWM)

5.11.1 Introduction

Seven generic pulse-width modulators are implemented to generate pulse sequences with programmable frequency and duration for LCD backlight, charging or other purposes. Before enabling PWM, the pulse sequences must be prepared in the memory or registers. Then PWM will read the pulse sequences to generate random waveform to meet all kinds of applications (see Figure 5-21).

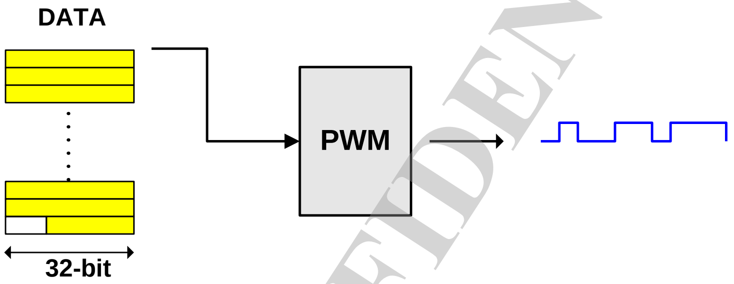
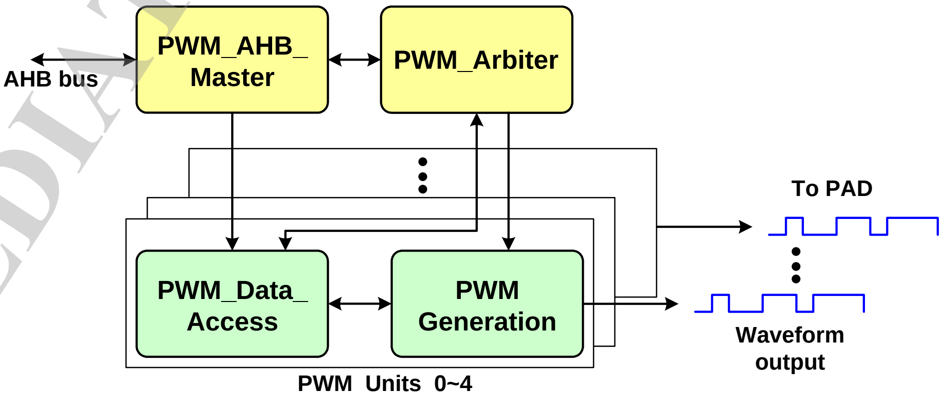


Figure 5-21. Generation procedure of PWM

5.11.2 Features

- Old mode, FIFO mode
- Periodical memory and random mode
- Sequential output mode and 3DLCM mode

5.11.3 Block Diagram



5.11.4 Register Definition

Module name: PWM Base address: (+11006000h)

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Address	Name	Width	Register Function
11006000	PWM_ENABLE	32	PWM Enable Register
11006004	PWM3_DELAY	32	PWM3 Delay Duration Register
11006008	PWM4_DELAY	32	PWM4 Delay Duration Register
11006010	PWM0_CON	32	PWM0 Control Register
11006014	PWM0_HDURATION	32	PWM0 High Duration Register
11006018	PWM0_LDURATION	32	PWM0 Low Duration Register
1100601C	PWM0_GDURATION	32	PWM0 Guard Duration Register
11006020	PWM0_BUF0_BASE_ADDR	32	
11006024	PWM0_BUF0_SIZE	32	PWM0 Buffer0 Size Register
11006028	PWM0_BUF1_BASE_ADDR	32	PWM0 Buffer1 Base Address Register
1100602C	PWM0_BUF1_SIZE	32	PWM0 Buffer1 Size Register
11006030	PWM0_SEND_DATA0	32	PWM0 Send Data 0 Register
11006034	PWM0_SEND_DATA1	32	PWM0 Send Data 1 Register
11006038	PWM0_WAVE_NUM	32	PWM0 Wave Number Register
1100603C	PWM0_DATA_WIDTH	32	PWM0 Data Width Register
11006040	PWM0_THRESH	32	PWM0 Thresh Register
11006044	PWM0_SEND_WAVENUM	32	PWM0 Send Wave Number Register
11006048	PWM0_VALID	32	PWM0 Valid Register
11006050	PWM1_CON	32	PWM1 Control Register
11006054	PWM1_HDURATION	32	PWM1 High Duration Register
11006058	PWM1_LDURATION	32	PWM1 Low Duration Register
1100605C	PWM1_GDURATION	32	PWM1 Guard Duration Register
11006060	PWM1_BUF0_BASE_ADDR	32	PWM1 Buffer 0 Base Address Register
11006064	PWM1_BUF0_SIZE	32	PWM1 Buffer 0 Size Register
11006068	PWM1_BUF1_BASE_ADDR	32	PWM1 Buffer 1 Base Address Register
1100606C	PWM1_BUF1_SIZE	32	PWM1 Buffer 1 Size Register
11006070	PWM1_SEND_DATA0	32	PWM1 Send Data 0 Register
11006074	PWM1_SEND_DATA1	32	PWM1 Send Data 1 Register
11006078	PWM1_WAVE_NUM	32	PWM1 Wave Number Register
1100607C	PWM1_DATA_WIDTH	32	PWM1 Data Width Register
11006080	PWM1_THRESH	32	PWM1 Thresh Register

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Address	Name	Width	Register Function
11006084	PWM1_SEND_WAVENUM	32	PWM1 Send Wave Number Register
11006088	PWM1_VALID	32	PWM1 Valid Register
11006090	PWM2_CON	32	PWM2 Control Register
11006094	PWM2_HDURATION	32	PWM2 High Duration Register
11006098	PWM2_LDURATION	32	PWM2 Low Duration Register
1100609C	PWM2_GDURATION	32	PWM2 Guard Duration Register
110060A0	PWM2_BUF0_BASE_ADDR	32	PWM2 Buffer 0 Base Address Register
110060A4	PWM2_BUF0_SIZE	32	PWM2 Buffer 0 Size Register
110060A8	PWM2_BUF1_BASE_ADDR	32	PWM2 Buffer 1 Base Address Register
110060AC	PWM2_BUF1_SIZE	32	PWM2 Buffer 1 Size Register
110060B0	PWM2_SEND_DATA0	32	PWM2 Send Data 0 Register
110060B4	PWM2_SEND_DATA1	32	PWM2 Send Data 1 Register
110060B8	PWM2_WAVE_NUM	32	PWM2 Wave Number Register
110060BC	PWM2_DATA_WIDTH	32	PWM2 Data Width Register
110060C0	PWM2_THRESH	32	PWM2 Thresh Register
110060C4	PWM2_SEND_WAVENUM	32	PWM2 Send Wave Number Register
110060C8	PWM2_VALID	32	PWM2 Valid Register
110060D0	PWM3_CON	32	PWM3 Control Register
110060D4	PWM3_HDURATION	32	PWM3 High Duration Register
110060D8	PWM3_LDURATION	32	PWM3 Low Duration Register
110060DC	PWM3_GDURATION	32	PWM3 Guard Duration Register
110060E0	PWM3_BUF0_BASE_ADDR	32	PWM3 Buffer 0 Base Address Register
110060E4	PWM3_BUF0_SIZE	32	PWM3 Buffer 0 Size Register
110060E8	PWM3_BUF1_BASE_ADDR	32	PWM3 Buffer 1 Base Address Register
110060EC	PWM3_BUF1_SIZE	32	PWM3 Buffer 1 Size Register
110060F0	PWM3_SEND_DATA0	32	PWM3 Send Data 0 Register
110060F4	PWM3_SEND_DATA1	32	PWM3 Send Data 1 Register
110060F8	PWM3_WAVE_NUM	32	PWM3 Wave Number Register
110060FC	PWM3_DATA_WIDTH	32	PWM3 Data Width Register
11006100	PWM3_THRESH	32	PWM3 Thresh Register
11006104	PWM3_SEND_W	32	PWM3 Send Wave Number Register

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Address	Name	Width	Register Function
	AVENUM		
11006108	PWM3_VALID	32	PWM3 Valid Register
11006110	PWM4_CON	32	PWM4 Control Register
11006114	PWM4_HDURATION	32	PWM4 High Duration Register
11006118	PWM4_LDURATION	32	PWM4 Low Duration Register
1100611C	PWM4_GDURATION	32	PWM4 Guard Duration Register
11006120	PWM4_BUF0_BASE_ADDR	32	
11006124	PWM4_BUF0_SIZE	32	PWM4 Buffer 0 Size Register
11006128	PWM4_BUF1_BASE_ADDR	32	PWM4 Buffer 1 Base Address Register
1100612C	PWM4_BUF1_SIZE	32	PWM4 Buffer 1 Size Register
11006130	PWM4_SEND_DATA0	32	PWM4 Send Data 0 Register
11006134	PWM4_SEND_DATA1	32	PWM4 Send Data 1 Register
11006138	PWM4_WAVE_NUM	32	PWM4 Wave Number Register
1100613C	PWM4_DATA_WIDTH	32	PWM4 Data Width Register
11006140	PWM4_THRESH	32	PWM4 Thresh Register
11006144	PWM4_SEND_WAVENUM	32	PWM4 Send Wave Number Register
11006148	PWM4_VALID	32	PWM4 Valid Register
110061CC	PWM_LOOP_BACK_TEST	32	PWM Loop Back Test
110061D0	PWM_3DLCM	32	PWM Support For 3D LCM
11006200	PWM_INT_ENABLE	32	PWM Interrupt Enable Register
11006204	PWM_INT_STATUS	32	PWM Interrupt Status Register
11006208	PWM_INT_ACK	32	PWM Interrupt Acknowledge Register
1100620C	PWM_EN_STATUS	32	PWM Enable Status Register
11006210	PWM_CK_26M_SEL	32	PWM BCLK Selection

11006000 **PWM_ENABLE** **PWM Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																PWM_SEQ_MODE
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												PWM4_EN	PWM3_EN	PWM2_EN	PWM1_EN	PWM0_EN

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Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
16	PWM_SEQ_MODE	**Set to 1 to enable PWM2, PWM3, PWM4 and PWM5 sequential delay mode.** In this mode, PWM2 starts first and then after PWM3_DELAY_TIME, PWM3 will start. After PWM3 starts, PWM4 will start after PWM4_DELAY_TIME.After PWM4 starts, PWM5 will start after PWM5_DELAY_TIME *Note: The output of PWM_SEQ_MODE is started after PWM2 is enabled. PWM_SEQ_MODE should be set before PWM3, PWM4 and PWM5 are enabled or at the same time. This mode does not work when PWM2 is set in OLD_PWM_MODE and CLKSEL=1.*
4	PWM4_EN	0: Disable PWM4 1: Enable PWM4
3	PWM3_EN	0: Disable PWM3 1: Enable PWM3
2	PWM2_EN	0: Disable PWM2 1: Enable PWM2
1	PWM1_EN	0: Disable PWM1 1: Enable PWM1
0	PWM0_EN	0: Disable PWM0 1: Enable PWM0

11006004 PWM3_DELAY PWM3 Delay Duration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**DELAY_CLKSEL**
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**PWM3_DELAY_DURATION**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	DELAY_CLKSEL	**Clock unit of PWM3_DELAY_DURATION** 0: CLK=CLKSRC (32k is not allowed.) 1: CLK=CLKSRC/1625
15:0	PWM3_DELAY_DURATION	**Duration between PWM2 and PWM3 start point.**

11006008 PWM4_DELAY PWM4 Delay Duration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**DELAY_CLKSEL**
Type																RW
Reset																0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PWM4_DELAY_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	DELAY_CLKSEL	**Clock unit of PWM4_DELAY_DURATION** 0: CLK=CLKSRC (32k is not allowed.) 1: CLK=CLKSRC/1625
15:0	PWM4_DELAY_DURATION	**Duration between PWM3 and PWM4 start point**

11006010 PWM0_CON PWM0 Control Register 00007E00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OLD_PWM_MODE	STOP_BITPOS						GUARD_VALUE	IDLE_VALUE	MODE	SRCSEL	CLKSEL_OLD	CLKSEL	CLKDIV		
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	OLD_PWM_MODE	**Uses old PWM mode** *Note: Using old PWM mode also means using periodical mode. Therefore, SRCSEL and MODE are ignored in this situation. Only old PWM mode with 32kHz clock however cannot work in system sleep mode.* 0: New PWM mode 1: Old PWM mode
14:9	STOP_BITPOS	**Stop bit position for source data in periodical mode** In FIFO mode, it is used to indicate the stop bit position in total 64 bits. In memory mode, it is for the stop bit position of the last 32 bits.
8	GUARD_VALUE	**PWM0 output value during guard time**
7	IDLE_VALUE	**PWM0 output value in idle state**
6	MODE	**Selects random generator mode** 0: Periodical PWM mode 1: Random PWM mode
5	SRCSEL	**Selects PWM0 data source** 0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	0: CLK=32K; CLK is not used. 1: CLK=32K; CLK can be used.
3	CLKSEL	**Selects PWM0 clock** 0: CLK=CLKSRC 1: CLK=CLKSRC/1625
2:0	CLKDIV	**Selects PWM0 clock scale** 000b: CLK Hz 001b: CLK/2 Hz 010b: CLK/4 Hz 011b: CLK/8 Hz 100b: CLK/16 Hz

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Bit(s)	Name	Description
		101b: CLK/32 Hz 110b: CLK/64 Hz 111b: CLK/128 Hz

11006014 **PWM0_HDURATION** **PWM0 High Duration Register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	HDURATION	**PWM0 pulse duration based on the current clock when PWM output is high** If duration =N, program N-1 in this register. *Note: The duration of PWM must not be 0.*

11006018 **PWM0_LDURATION** **PWM0 Low Duration Register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	LDURATION	**PWM0 pulse duration based on the current clock when PWM output is low** If duration =N, program N-1 in this register. *Note: The duration of PWM must not be 0.*

1100601C **PWM0_GDURATION** **PWM0 Guard Duration Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GUARD_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	GUARD_DURATION	**Guarding interval between individual waveforms and the output is decided by GUARD_VALUE** If it equals N, program N-1 in this register. *Note:* *1. If this duration is 0, it means there is no guarding interval.* *2: The guard duration of old mode is set by PWM_DATA_WIDTH.*

11006020 **PWM0_BUF0_BASE_ADDR** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF0_BS_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	Base address of Memory Buffer 0 for PWM0's waveform data

11006024 **PWM0_BUF0_SIZE** **PWM0 Buffer0 Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF0_SIZE	**Length of waveform data in Memory Buffer 0 PWM0 should generate** If it equals N, program N-1 in this register. *Note: The size is in unit of 32-bit data.*

11006028 **PWM0_BUF1_BASE_ADDR** **PWM0 Buffer1 Base Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	**Base address of Memory Buffer 1 for PWM0's waveform data** *Note: The Memory Buffer 1 is useless in periodical mode.*

1100602C **PWM0_BUF1_SIZE** **PWM0 Buffer1 Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF1_SIZE	**Length of waveform data in Memory Buffer 1 PWM0 should generate** If it equals N, program N-1 in this register.

11006030 **PWM0_SEND_DATA0** **PWM0 Send Data 0 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA0	**PWM0 Local Buffer 0 of pulse sequence data to be generated** *Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.*

11006034 **PWM0_SEND_DATA1** **PWM0 Send Data 1 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	**PWM0 Local Buffer 0 of pulse sequence data to be generated**

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Bit(s)	Name	Description
		Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

11006038 PWM0_WAVE_NUM PWM0 Wave Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WAVE_NUM	**Number by which PWM0 will generate from pulse data repeatedly** *Note: If WAVE_NUM=0, the waveform generation will not stop until it is disabled.*

1100603C PWM0_DATA_WIDTH PWM0 Data Width Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DATA_WIDTH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DATA_WIDTH	PWM0 pulse data width in old PWM mode

11006040 PWM0_THRESH PWM0 Thresh Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				THRESH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	THRESH	PWM0 pulse data high/low switching threshold in old PWM mode

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11006044 **PWM0_SEND_WAVENUM** **PWM0 Send Wave Number Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_WAVENUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SEND_WAVENUM	Number by which PWM0 has already generated from specified data source in periodical mode

11006048 **PWM0_VALID** **PWM0 Valid Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BUF1_VALID	BUF0_VALID
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	BUF1_VALID	0: Memory 1 is empty. 1: Memory 1 is not empty. When finishing writing data to Memory 1, write 1 to inform PWM the data in Memory 1 are ready.
0	BUF0_VALID	0: Memory 0 is empty. 1: Memory 0 is not empty. When finishing writing data to Memory 0, write 1 to inform PWM the data in Memory 0 are ready.

11006050 **PWM1_CON** **PWM1 Control Register** **00007E00**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OLD_PWM_MODE	STOP_BITPOS						GUARD_VALUE	IDLE_VALUE	MODE	SRCSEL	CLKSEL_OLD	CLKSEL	CLKDIV		
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	OLD_PWM_MODE	**Uses old PWM mode** *Note: Using old PWM mode also means using periodical mode. Therefore, SRCSEL and MODE are ignored in this situation. Only old PWM mode with 32kHz clock however cannot work in system sleep mode.*

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Bit(s)	Name	Description
14:9	STOP_BITPOS	0: New PWM mode 1: Old PWM mode *Note: Using old PWM mode also means using periodical mode. Therefore, SRCSEL and MODE are ignored in this situation. Only old PWM mode with 32kHz clock however cannot work in system sleep mode.*
8	GUARD_VALUE	**PWM1 output value during guard time**
7	IDLE_VALUE	**PWM1 output value in idle state**
6	MODE	**Selects random generator mode** 0: Periodical PWM mode 1: Random PWM mode
5	SRCSEL	**Selects PWM1 data source** 0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	0: CLK=32K; CLK is not used. 1: CLK=32K; CLK can be used.
3	CLKSEL	**Selects PWM0 clock** 0: CLK=CLKSRC 1: CLK=CLKSRC/1625
2:0	CLKDIV	**Selects PWM1 clock scale** 000b: CLK Hz 001b: CLK/2 Hz 010b: CLK/4 Hz 011b: CLK/8 Hz 100b: CLK/16 Hz 101b: CLK/32 Hz 110b: CLK/64 Hz 111b: CLK/128 Hz

11006054 PWM1_HDURATION PWM1 High Duration Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	HDURATION	**PWM1 pulse duration based on the current clock when PWM output is high** If duration =N, program N-1 in this register. *Note: The duration of PWM must not be 0.*

11006058 PWM1_LDURATION PWM1 Low Duration Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	LDURATION	**PWM1 pulse duration based on the current clock when PWM output is low** If duration =N, program N-1 in this register. *Note: The duration of PWM must not be 0.*

1100605C PWM1_GDURATION PWM1 Guard Duration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GUARD_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GUARD_DURATION	**Guarding interval between individual waveforms and the output is decided by GUARD_VALUE** If it equals N, program N-1 in this register. *Note:* *1. If this duration is 0, it means there is no guarding interval.* *2: The guard duration of old mode is set by PWM_DATA_WIDTH.*

11006060 PWM1_BUF0_BASE_ADDR PWM1 Buffer 0 Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF0_BS_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	Base address of Memory Buffer 0 for PWM1's waveform data

11006064 PWM1_BUF0_SIZE PWM1 Buffer 0 Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF0_SIZE	**Length of waveform data in Memory Buffer 0 PWM1 should generate** If it equals N, program N-1 in this register. *Note: The size is in unit of 32-bit data.*

11006068 PWM1_BUF1_BASE_ADDR PWM1 Buffer 1 Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	**Base address of Memory Buffer 1 for PWM10's waveform data** *Note: The Memory Buffer 1 is useless in periodical mode.*

1100606C PWM1_BUF1_SIZE PWM1 Buffer 1 Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF1_SIZE	**Length of waveform data in Memory Buffer 1 PWM1 should generate** If it equals N, program N-1 in this register.

11006070 PWM1_SEND_DATA0 PWM1 Send Data 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA0[15:0]															

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Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA0	**PWM1 Local Buffer 0 of pulse sequence data to be generated** *Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.*

11006074 PWM1_SEND_DATA1 PWM1 Send Data 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	**PWM1 Local Buffer 0 of pulse sequence data to be generated** *Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.*

11006078 PWM1_WAVE_NUM PWM1 Wave Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WAVE_NUM	**Number by which PWM1 will generate from pulse data repeatedly** *Note: If WAVE_NUM=0, the waveform generation will not stop until it is disabled.*

1100607C PWM1_DATA_WIDTH PWM1 Data Width Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DATA_WIDTH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
12:0	DATA_WIDTH	PWM1 pulse data width in old PWM mode

11006080 PWM1_THRESH PWM1 Thresh Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				THRESH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	THRESH	PWM1 pulse data high/low switching threshold in old PWM mode

11006084 PWM1_SEND_WAVENUM PWM1 Send Wave Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SEND_WAVENUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SEND_WAVENUM	Number by which PWM1 has already generated from specified data source in periodical mode

11006088 PWM1_VALID PWM1 Valid Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name															BUF1_VALID	BUF0_VALID
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	BUF1_VALID	0: Memory 1 is empty. 1: Memory 1 is not empty. When finishing writing data to Memory 1, write 1 to inform PWM the data in Memory 1 are ready.

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Bit(s)	Name	Description
0	BUF0_VALID	0: Memory 0 is empty. 1: Memory 0 is not empty. When finishing writing data to Memory 0, write 1 to inform PWM the data in Memory 0 are ready.

11006090 PWM2_CON PWM2 Control Register 00007E00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**OLD_PWM_MODE**	**STOP_BITPOS**						**GUARD_VALUE**	**IDLE_VALUE**	**MODE**	**SRCSEL**	**CLKSEL_OLD**	**CLKSEL**	**CLKDIV**		
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	OLD_PWM_MODE	**Uses old PWM mode** *Note: Using old PWM mode also means using periodical mode. Therefore, SRCSEL and MODE are ignored in this situation. Only old PWM mode with 32kHz clock source however cannot work in system sleep mode.* 0: New PWM mode 1: Old PWM mode
14:9	STOP_BITPOS	**Stop bit position for source data in periodical mode** In FIFO mode, it is used to indicate the stop bit position in total 64 bits. In memory mode, it is for the stop bit position of the last 32 bits.
8	GUARD_VALUE	**PWM2 output value during guard time**
7	IDLE_VALUE	**PWM2 output value in idle state**
6	MODE	**Selects random generator mode** 0: Periodical PWM mode 1: Random PWM mode
5	SRCSEL	**Selects PWM2 data source** 0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	0: CLK=32K; CLK is not used. 1: CLK=32K; CLK can be used.
3	CLKSEL	**Selects PWM0 clock** 0: CLK=CLKSRC 1: CLK=CLKSRC/1625
2:0	CLKDIV	**Selects PWM2 clock scale** 000b: CLK Hz 001b: CLK/2 Hz 010b: CLK/4 Hz 011b: CLK/8 Hz 100b: CLK/16 Hz 101b: CLK/32 Hz 110b: CLK/64 Hz 111b: CLK/128 Hz

11006094 PWM2_HDUR PWM2 High Duration Register 00000001

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	HDURATION	**PWM2 pulse duration based on the current clock when PWM output is high** If duration =N, program N-1 in this register. *Note: The duration of PWM must not be 0.*

11006098 **PWM2_LDURATION** **PWM2 Low Duration Register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	LDURATION	**PWM2 pulse duration based on the current clock when PWM output is low** If duration =N, program N-1 in this register. *Note: The duration of PWM must not be 0.*

1100609C **PWM2_GDURATION** **PWM2 Guard Duration Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GUARD_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GUARD_DURATION	**Guarding interval between individual waveforms and the output is decided by GUARD_VALUE** If it equals N, program N-1 in this register. *Note:* *1. If this duration is 0, it means there is no guarding interval.* *2: The guard duration of old mode is set by PWM_DATA_WIDTH.*

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110060A0 PWM2_BUF0_BASE_ADDR PWM2 Buffer 0 Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF0_BS_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	Base address of Memory Buffer 0 for PWM2's waveform data

110060A4 PWM2_BUF0_SIZE PWM2 Buffer 0 Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF0_SIZE	**Length of waveform data in Memory Buffer 0 PWM2 should generate** If it equals N, program N-1 in this register.

110060A8 PWM2_BUF1_BASE_ADDR PWM2 Buffer 1 Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	**Base address of Memory Buffer 1 for PWM2's waveform data** *Note: The Memory Buffer 1 is useless in periodical mode.*

110060AC PWM2_BUF1_SIZE PWM2 Buffer 1 Size Register 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF1_SIZE	**Length of waveform data in Memory Buffer 1 PWM2 should generate** If it equals N, program N-1 in this register.

110060B0 PWM2_SEND_DATA0 PWM2 Send Data 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA0	**PWM2 Local Buffer 0 of pulse sequence data to be generated** *Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.*

110060B4 PWM2_SEND_DATA1 PWM2 Send Data 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	**PWM2 Local Buffer 0 of pulse sequence data to be generated** *Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.*

110060B8 PWM2_WAVE_NUM PWM2 Wave Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

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Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WAVE_NUM	**Number by which PWM2 will generate from pulse data repeatedly** *Note: If WAVE_NUM=0, the waveform generation will not stop until it is disabled.*

110060BC PWM2_DATA_WIDTH PWM2 Data Width Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DATA_WIDTH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DATA_WIDTH	PWM2 pulse data width in old PWM mode

110060C0 PWM2_THRESH PWM2 Thresh Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				THRESH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	THRESH	PWM2 pulse data high/low switching threshold in old PWM mode

110060C4 PWM2_SEND_WAVENUM PWM2 Send Wave Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_WAVENUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	SEND_WAVENUM	Number by which PWM2 has already generated from specified data source in periodical mode

110060C8 PWM2_VALID PWM2 Valid Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BUF1_VALID	BUF0_VALID
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	BUF1_VALID	0: Memory 1 is empty. 1: Memory 1 is not empty. When finishing writing data to Memory 1, write 1 to inform PWM the data in Memory 1 are ready.
0	BUF0_VALID	0: Memory 0 is empty. 1: Memory 0 is not empty. When finishing writing data to Memory 0, write 1 to inform PWM the data in Memory 0 are ready.

110060D0 PWM3_CON PWM3 Control Register 00007E00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OLD_PWM_MODE	STOP_BITPOS						GUARD_VALUE	IDLE_VALUE	MODE	SRCSEL	CLKSEL_OLD	CLKSEL	CLKDIV		
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	OLD_PWM_MODE	**Uses old PWM mode** *Note: Using old PWM mode also means using periodical mode. Therefore, SRCSEL and MODE are ignored in this situation. Only old PWM mode with 32kHz clock source however cannot work in system sleep mode.* 0: New PWM mode 1: Old PWM mode
14:9	STOP_BITPOS	**Stop bit position for source data in periodical mode** In FIFO mode, it is used to indicate the stop bit position in total 64 bits. In memory mode, it is for the stop bit position of the last 32 bits.
8	GUARD_VALUE	**PWM3 output value during guard time**
7	IDLE_VALUE	**PWM3 output value in idle state**
6	MODE	**Selects random generator mode** 0: Periodical PWM mode

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Bit(s)	Name	Description
		1: Random PWM mode
5	SRCSEL	**Selects PWM3 data source** 0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	0: CLK=32K; CLK is not used. 1: CLK=32K; CLK can be used.
3	CLKSEL	**Selects PWM0 clock** 0: CLK=CLKSRC 1: CLK=CLKSRC/1625
2:0	CLKDIV	**Selects PWM3 clock scale** 000b: CLK Hz 001b: CLK/2 Hz 010b: CLK/4 Hz 011b: CLK/8 Hz 100b: CLK/16 Hz 101b: CLK/32 Hz 110b: CLK/64 Hz 111b: CLK/128 Hz

110060D4 **PWM3_HDURATION** **PWM3 High Duration Register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	HDURATION	**PWM3 pulse duration based on the current clock when PWM output is high** If duration =N, program N-1 in this register. *Note: The duration of PWM must not be 0.*

110060D8 **PWM3_LDURATION** **PWM3 Low Duration Register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	LDURATION	**PWM3 pulse duration based on the current clock when PWM output is low** If duration =N, program N-1 in this register.

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Bit(s)	Name	Description
		Note: The duration of PWM must not be 0.

110060DC **PWM3_GDURATION** **PWM3 Guard Duration Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GUARD_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GUARD_DURATION	**Guarding interval between individual waveforms and the output is decided by GUARD_VALUE** If it equals N, program N-1 in this register. *Note:* *1. If this duration is 0, it means there is no guarding interval.* *2: The guard duration of old mode is set by PWM_DATA_WIDTH.*

110060E0 **PWM3_BUF0_BASE_ADDR** **PWM3 Buffer 0 Base Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF0_BS_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	Base address of Memory Buffer 0 for PWM3's waveform data

110060E4 **PWM3_BUF0_SIZE** **PWM3 Buffer 0 Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF0_SIZE	**Length of waveform data in Memory Buffer 0 PWM3 should**

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Bit(s)	Name	Description
		generate If it equals N, program N-1 in this register.

110060E8 **PWM3_BUF1_BASE_ADDR** **PWM3 Buffer 1 Base Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	**Base address of Memory Buffer 1 for PWM3's waveform data** *Note: The Memory Buffer 1 is useless in periodical mode.*

110060EC **PWM3_BUF1_SIZE** **PWM3 Buffer 1 Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF1_SIZE	**Length of waveform data in Memory Buffer 1 PWM3 should generate** If it equals N, program N-1 in this register.

110060F0 **PWM3_SEND_DATA0** **PWM3 Send Data 0 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA0	**PWM3 Local Buffer 0 of pulse sequence data to be generated** *Note: This value should be written only in periodically FIFO mode. In other*

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Bit(s)	Name	Description
		modes, this buffer is for internal memory access.

110060F4 **PWM3_SEND_DATA1** **PWM3 Send Data 1 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	**PWM3 Local Buffer 0 of pulse sequence data to be generated** *Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.*

110060F8 **PWM3_WAVE_NUM** **PWM3 Wave Number Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WAVE_NUM	**Number by which PWM3 will generate from pulse data repeatedly** *Note: If WAVE_NUM=0, the waveform generation will not stop until it is disabled.*

110060FC **PWM3_DATA_WIDTH** **PWM3 Data Width Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DATA_WIDTH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DATA_WIDTH	PWM3 pulse data width in old PWM mode

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11006100 **PWM3_THRESH** **PWM3 Thresh Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				THRESH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	THRESH	PWM3 pulse data high/low switching threshold in old PWM mode

11006104 **PWM3_SEND_WAVENUM** **PWM3 Send Wave Number Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_WAVENUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SEND_WAVENUM	Number by which PWM3 has already generated from specified data source in periodical mode

11006108 **PWM3_VALID** **PWM3 Valid Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BUF1_VALID	BUF0_VALID
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	BUF1_VALID	0: Memory 1 is empty. 1: Memory 1 is not empty. When finishing writing data to Memory 1, write 1 to inform PWM the data in Memory 1 are ready.
0	BUF0_VALID	0: Memory 0 is empty. 1: Memory 0 is not empty. When finishing writing data to Memory 0, write 1 to inform PWM the data in Memory 0 are ready.

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11006110 PWM4_CON PWM4 Control Register 00007E00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OLD_PWM_MODE	STOP_BITPOS						GUARD_VALUE	IDLE_VALUE	MODE	SRCSEL	CLKSEL_OLD	CLKSEL	CLKDIV		
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	OLD_PWM_MODE	**Uses old PWM mode** *Note: Using old PWM mode also means using periodical mode. Therefore, SRCSEL and MODE are ignored in this situation. Only old PWM mode with 32kHz clock source however cannot work in system sleep mode.* 0: New PWM mode 1: Old PWM mode
14:9	STOP_BITPOS	**Stop bit position for source data in periodical mode** In FIFO mode, it is used to indicate the stop bit position in total 64 bits. In memory mode, it is for the stop bit position of the last 32 bits.
8	GUARD_VALUE	**PWM4 output value during guard time**
7	IDLE_VALUE	**PWM4 output value in idle state**
6	MODE	**Selects random generator mode** 0: Periodical PWM mode 1: Random PWM mode
5	SRCSEL	**Selects PWM4 data source** 0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	0: CLK=32K CLK IS NOT USED 1: CLK=32K CLK CAN BE USED
3	CLKSEL	**Selects PWM4 clock** 0: CLK=CLKSRC 1: CLK=CLKSRC/1625
2:0	CLKDIV	**Selects PWM4 clock scale** 000b: CLK Hz 001b: CLK/2 Hz 010b: CLK/4 Hz 011b: CLK/8 Hz 100b: CLK/16 Hz 101b: CLK/32 Hz 110b: CLK/64 Hz 111b: CLK/128 Hz

11006114 PWM4_HDURATION PWM4 High Duration Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HDURATION															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	HDURATION	**PWM4 pulse duration based on the current clock when PWM output is high** If duration =N, program N-1 in this register. *Note: The duration of PWM must not be 0.*

11006118 **PWM4_LDURATION** **PWM4 Low Duration Register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**LDURATION**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	LDURATION	**PWM4 pulse duration based on the current clock when PWM output is low** If duration =N, program N-1 in this register. *Note: The duration of PWM must not be 0.*

1100611C **PWM4_GDURATION** **PWM4 Guard Duration Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**GUARD_DURATION**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GUARD_DURATION	**Guarding interval between individual waveforms and the output is decided by GUARD_VALUE** If it equals N, program N-1 in this register. *Note:* *1. If this duration is 0, it means there is no guarding interval.* *2: The guard duration of old mode is set by PWM_DATA_WIDTH.*

11006120 **PWM4_BUF0_BASE_ADDR** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**BUF0_BS_ADDR[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	Base address of Memory Buffer 0 for PWM4's waveform data

11006124 PWM4_BUF0_SIZE PWM4 Buffer 0 Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF0_SIZE	**Length of waveform data in Memory Buffer 0 PWM4 should generate** If it equals N, program N-1 in this register.

11006128 PWM4_BUF1_BASE_ADDR PWM4 Buffer 1 Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	**Base address of Memory Buffer 1 for PWM4's waveform data** *Note: The Memory Buffer 1 is useless in periodical mode.*

1100612C PWM4_BUF1_SIZE PWM4 Buffer 1 Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	BUF1_SIZE	**Length of waveform data in Memory Buffer 1 PWM4 should generate** If it equals N, program N-1 in this register.

11006130 **PWM4_SEND_DATA0** **PWM4 Send Data 0 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SEND_DATA0[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SEND_DATA0[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA0	**PWM4 Local Buffer 0 of pulse sequence data to be generated** *Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.*

11006134 **PWM4_SEND_DATA1** **PWM4 Send Data 1 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SEND_DATA1[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SEND_DATA1[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	**PWM4 Local Buffer 0 of pulse sequence data to be generated** *Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.*

11006138 **PWM4_WAVE_NUM** **PWM4 Wave Number Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**WAVE_NUM**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
15:0	WAVE_NUM	**Number by which PWM4 will generate from pulse data repeatedly** *Note: If WAVE_NUM=0, the waveform generation will not stop until it is disabled.*

1100613C <u>PWM4_DATA_WIDTH</u> PWM4 Data Width Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DATA_WIDTH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DATA_WIDTH	PWM4 pulse data width in old PWM mode

11006140 <u>PWM4_THRESH</u> PWM4 Thresh Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				THRESH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	THRESH	PWM4 pulse data high/low switching threshold in old PWM mode

11006144 <u>PWM4_SEND_WAVENUM</u> PWM4 Send Wave Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_WAVENUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SEND_WAVENUM	Number by which PWM4 has already generated from specified data source in periodical mode

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11006148 PWM4_VALID PWM4 Valid Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BUF1_VALID	BUF0_VALID
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	BUF1_VALID	0: Memory 1 is empty. 1: Memory 1 is not empty. When finishing writing data to Memory 1, write 1 to inform PWM the data in Memory 1 are ready.
0	BUF0_VALID	0: Memory 0 is empty. 1: Memory 0 is not empty. When finishing writing data to Memory 0, write 1 to inform PWM the data in Memory 0 are ready.

110061CC PWM_LOOP_BACK_TEST PWM Loop Back Test 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												PWM4_STATUS	PWM3_STATUS	PWM2_STATUS	PWM1_STATUS	PWM0_STATUS
Type												RU	RU	RU	RU	RU
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	PWM4_STATUS	0: PWM4 output is low. 1: PWM4 output is high.
3	PWM3_STATUS	0: PWM3 output is low. 1: PWM3 output is high.
2	PWM2_STATUS	0: PWM2 output is low. 1: PWM2 output is high.
1	PWM1_STATUS	0: PWM1 output is low. 1: PWM1 output is high.
0	PWM0_STATUS	0: PWM0 output is low. 1: PWM0 output is high.

110061D0 PWM_3DLCM PWM Support For 3D LCM 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												PWM_3DLCM_5	PWM_3DLCM_4	PWM_3DLCM_3	PWM_3DLCM_2	PWM_3DLCM_1
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	PWM_3DLCM_SYNC			PWM_3DLCM_5_base	PWM_3DLCM_4_base	PWM_3DLCM_3_base	PWM_3DLCM_2_base	PWM_3DLCM_1_base			PWM_3DLCM_5_INV	PWM_3DLCM_4_INV	PWM_3DLCM_3_INV	PWM_3DLCM_2_INV	PWM_3DLCM_1_INV	PWM_3DLCM_EN
Type	RW			RW	RW	RW	RW	RW			RW	RW	RW	RW	RW	RW
Reset	0			0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
20	PWM_3DLCM_5	*Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.* 0: PWM4 is not selected as PWM auxiliary channel. 1: PWM4 is selected as PWM auxiliary channel.
19	PWM_3DLCM_4	*Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.* 0: PWM3 is not selected as PWM auxiliary channel. 1: PWM3 is selected as PWM auxiliary channel.
18	PWM_3DLCM_3	*Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.* 0: PWM2 is not selected as PWM auxiliary channel. 1: PWM2 is selected as PWM auxiliary channel.
17	PWM_3DLCM_2	*Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.* 0: PWM1 is not selected as PWM auxiliary channel. 1: PWM1 is selected as PWM auxiliary channel.
16	PWM_3DLCM_1	*Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.* 0: PWM0 is not selected as PWM auxiliary channel. 1: PWM0 is selected as PWM auxiliary channel.
15	PWM_3DLCM_SYNC	0: PWM auxiliary channel does not keep low when PWM base channel is disabled. 1: PWM auxiliary channel keeps low when PWM base channel is disabled.
12	PWM_3DLCM_5_base	*Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.* 0: PWM4 is not selected as PWM base channel. 1: PWM4 is selected as PWM base channel.
11	PWM_3DLCM_4_base	*Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.* 0: PWM3 is not selected as PWM base channel. 1: PWM3 is selected as PWM base channel.
10	PWM_3DLCM_3_base	*Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.* 0: PWM2 is not selected as PWM base channel. 1: PWM2 is selected as PWM base channel.
9	PWM_3DLCM_2_base	*Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.* 0: PWM1 is not selected as PWM base channel. 1: PWM1 is selected as PWM base channel.
8	PWM_3DLCM_1_base	*Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.* 0: PWM0 is not selected as PWM base channel. 1: PWM0 is selected as PWM base channel.
5	PWM_3DLCM_5_INV	0: PWM4 is the same as PWM base channel when PWM4 is selected as auxiliary channel. 1: PWM4 is inversion of PWM base channel when PWM4 is selected as auxiliary channel.
4	PWM_3DLCM_4_INV	0: PWM3 is the same as PWM base channel when PWM3 is selected as auxiliary channel.

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Bit(s)	Name	Description
		1: PWM3 is inversion of PWM base channel when PWM3 is selected as auxiliary channel.
3	PWM_3DLCM_3_INV	0: PWM2 is the same as PWM base channel when PWM2 is selected as auxiliary channel. 1: PWM2 is inversion of PWM base channel when PWM2 is selected as auxiliary channel.
2	PWM_3DLCM_2_INV	0: PWM1 is the same as PWM base channel when PWM1 is selected as auxiliary channel. 1: PWM1 is inversion of PWM base channel when PWM1 is selected as auxiliary channel.
1	PWM_3DLCM_1_INV	0: PWM0 is the same as PWM base channel when PWM0 is selected as auxiliary channel. 1: PWM0 is inversion of PWM base channel when PWM0 is selected as auxiliary channel.
0	PWM_3DLCM_EN	0: Disable 3D_LCM for PWM 1: Enable 3D_LCM for PWM

11006200 **PWM_INT_ENABLE** **PWM Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							PWM4_INT_UNDERFLOW_EN	PWM4_INT_FINISH_EN	PWM3_INT_UNDERFLOW_EN	PWM3_INT_FINISH_EN	PWM2_INT_UNDERFLOW_EN	PWM2_INT_FINISH_EN	PWM1_INT_UNDERFLOW_EN	PWM1_INT_FINISH_EN	PWM0_INT_UNDERFLOW_EN	PWM0_INT_FINISH_EN
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9	PWM4_INT_UNDERFLOW_EN	0: Disable underflow interrupt for PWM4 1: Enable underflow interrupt for PWM4
8	PWM4_INT_FINISH_EN	0: Disable finished interrupt for PWM4 1: Enable finished interrupt for PWM4
7	PWM3_INT_UNDERFLOW_EN	0: Disable underflow interrupt for PWM3 1: Enable underflow interrupt for PWM3
6	PWM3_INT_FINISH_EN	0: Disable finished interrupt for PWM3 1: Enable finished interrupt for PWM3
5	PWM2_INT_UNDERFLOW_EN	0: Disable underflow interrupt for PWM2 1: Enable underflow interrupt for PWM2
4	PWM2_INT_FINISH_EN	0: Disable finished interrupt for PWM2 1: Enable finished interrupt for PWM2
3	PWM1_INT_UNDERFLOW_EN	0: Disable underflow interrupt for PWM1 1: Enable underflow interrupt for PWM1
2	PWM1_INT_FINISH_EN	0: Disable finished interrupt for PWM1 1: Enable finished interrupt for PWM1
1	PWM0_INT_UNDERFLOW_EN	0: Disable underflow interrupt for PWM0 1: Enable underflow interrupt for PWM0
0	PWM0_INT_FINISH	0: Disable finished interrupt for PWM0

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Bit(s)	Name	Description
	_EN	1: Enable finished interrupt for PWM0

11006204 **PWM_INT_STATUS** **PWM Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							PWM4_INT_UNDERFLOW_ST	PWM4_INT_FINISH_ST	PWM3_INT_UNDERFLOW_ST	PWM3_INT_FINISH_ST	PWM2_INT_UNDERFLOW_ST	PWM2_INT_FINISH_ST	PWM1_INT_UNDERFLOW_ST	PWM1_INT_FINISH_ST	PWM0_INT_UNDERFLOW_ST	PWM0_INT_FINISH_ST
Type							RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9	PWM4_INT_UNDERFLOW_ST	0: PWM4 underflow interrupt has not come. 1: PWM4 underflow interrupt has come.
8	PWM4_INT_FINISH_ST	0: PWM4 finished interrupt has not come. 1: PWM4 finished interrupt has come.
7	PWM3_INT_UNDERFLOW_ST	0: PWM3 underflow interrupt has not come. 1: PWM3 underflow interrupt has come.
6	PWM3_INT_FINISH_ST	0: PWM3 finished interrupt has not come. 1: PWM3 finished interrupt has come.
5	PWM2_INT_UNDERFLOW_ST	0: PWM2 underflow interrupt has not come. 1: PWM2 underflow interrupt has come.
4	PWM2_INT_FINISH_ST	0: PWM2 finished interrupt has not come. 1: PWM2 finished interrupt has come.
3	PWM1_INT_UNDERFLOW_ST	0: PWM1 underflow interrupt has not come. 1: PWM1 underflow interrupt has come.
2	PWM1_INT_FINISH_ST	0: PWM1 finished interrupt has not come. 1: PWM1 finished interrupt has come.
1	PWM0_INT_UNDERFLOW_ST	0: PWM0 underflow interrupt has not come. 1: PWM0 underflow interrupt has come.
0	PWM0_INT_FINISH_ST	0: PWM0 finished interrupt has not come. 1: PWM0 finished interrupt has come.

11006208 **PWM_INT_ACK** **PWM Interrupt Acknowledge Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							PWM4_INT_UNDERFLOW	PWM4_INT_FINISH_ACK	PWM3_INT_UNDERFLOW	PWM3_INT_FINISH_ACK	PWM2_INT_UNDERFLOW	PWM2_INT_FINISH_ACK	PWM1_INT_UNDERFLOW_	PWM1_INT_FINISH_ACK	PWM0_INT_UNDERFLOW	PWM0_INT_FINISH_ACK

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							_ACK		_ACK		_ACK		ACK		_ACK	
Type							WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9	PWM4_INT_UNDERFLOW_ACK	0: Does not clear PWM4 underflow interrupt 1: Clear PWM4 underflow interrupt
8	PWM4_INT_FINISH_ACK	0: Does not clear PWM4 finished interrupt 1: Clear PWM4 finished interrupt
7	PWM3_INT_UNDERFLOW_ACK	0: Does not clear PWM3 underflow interrupt 1: Clear PWM3 underflow interrupt
6	PWM3_INT_FINISH_ACK	0: Does not clear PWM3 finished interrupt 1: Clear PWM3 finished interrupt
5	PWM2_INT_UNDERFLOW_ACK	0: Does not clear PWM2 underflow interrupt 1: Clear PWM2 underflow interrupt
4	PWM2_INT_FINISH_ACK	0: Does not clear PWM2 finished interrupt 1: Clear PWM2 finished interrupt
3	PWM1_INT_UNDERFLOW_ACK	0: Does not clear PWM1 underflow interrupt 1: Clear PWM1 underflow interrupt
2	PWM1_INT_FINISH_ACK	0: Does not clear PWM1 finished interrupt 1: Clear PWM1 finished interrupt
1	PWM0_INT_UNDERFLOW_ACK	0: Does not clear PWM0 underflow interrupt 1: Clear PWM0 underflow interrupt
0	PWM0_INT_FINISH_ACK	0: Does not clear PWM0 finished interrupt 1: Clear PWM0 finished interrupt

1100620C **PWM_EN_STATUS** **PWM Enable Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**PWM4_EN_ST**	**PWM3_EN_ST**	**PWM2_EN_ST**	**PWM1_EN_ST**	**PWM0_EN_ST**
Type												RO	RO	RO	RO	RO
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	PWM4_EN_ST	PWM4 enabling status
3	PWM3_EN_ST	PWM3 enabling status
2	PWM2_EN_ST	PWM2 enabling status
1	PWM1_EN_ST	PWM1 enabling status
0	PWM0_EN_ST	PWM0 enabling status

11006210 **PWM_CK_26M_SEL** **PWM BCLK Selection** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

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Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																PWM_26M_SEL
Type																RW
Reset																1

Bit(s)	Name	Description
0	PWM_26M_SEL	0: Select bus CLK as BCLK 1: Select 26M fix CLK as BCLK

5.11.5 Clock Source Selection

OLD_MODE	CLKSEL_OLD	CLKSEL	CLKSRC
1	1	0	bclk
1	1	1	32KHz (used in old mode only)
1	0	0	bclk
1	0	1	bclk/1625
0	Don't care	0	bclk
0	Don't care	1	bclk/1625

Note: bclk can be selected as 26MHz or 66MHz(bus clock) by PWM_CK_26M_SEL.

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5.12 General-Purpose Timer (GPT)

5.12.1 Introduction

The GPT includes five 32-bit timers and one 64-bit timer. Each timer has four operation modes, which are ONE-SHOT, REPEAT, KEEP-GO and FREERUN, and can operate on one of the two clock sources, RTC clock (32.768kHz) and system clock (13MHz).

5.12.2 Features

The four operation modes for GPT are ONE-SHOT, REPEAT, KEEP-GO and FREERUN. See Table 5-6. ***Operation mode of GPT*** for the functions of each mode.

Table 5-6. Operation mode of GPT

Mode	Auto Stop	Interrupt	Increases when EN=1 and …	When COUNTn equals COMPAREn	Example: Compare is set to 2 **Bold means interrupt*
ONE-SHOT	Yes	Yes	Stops when COUNTn equals to COMPAREn	EN is reset to 0.	0,1,**2**,2,2,2,2,2,2,2,2,2,…
REPEAT	No	Yes		Count is reset to 0.	0,1,**2**,0,1,**2**,0,1,**2**,0,1,**2**…
KEEP-GO	No	Yes	Reset to 0 when overflow		0,1,**2**,3,4,5,6,7,8,9,10,…
FREERUN	No	No	Reset to 0 when overflow		0,1,2,3,4,5,6,7,8,9,10,…

Each timer can be programmed to select the clock source, RTC clock (32.76kHz) or system clock (13MHz). After the clock source is determined, the division ratio of the selected clock can be programmed. The division ratio can be fine-granulated as 1, 2, 3, 4 to 13 and coarse-granulated as 16, 32 and 64.

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5.12.3 Block Diagram

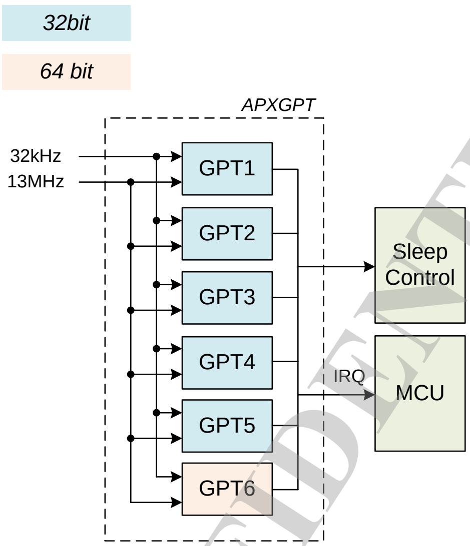

Figure 5-22. Block diagram of APXGPT

5.12.4 Register Definition

Module name: apxgpt Base address: (+10004000h)

Address	Name	Width	Register Function
10004000	GPT_IRQEN	32	**GPT IRQ Enabling** Controls the enabling/disabling of GPT interrupt.
10004004	GPT_IRQSTA	32	**GPT IRQ Status** Shows the interrupt status of each GPT.
10004008	GPT_IRQACK	32	**GPT IRQ Acknowledgement** Acknowledges the GPT interrupt.
10004010	GPT1_CON	32	**GPT1 Control** General control for GPT1.
10004014	GPT1_CLK	32	**GPT1 Clock Setting** Controls the clock source and division ratio of GPT clock.
10004018	GPT1_COUNT	32	**GPT1 Counter** Timer count of GPT1.
1000401C	GPT1_COMPARE	32	**GPT1 Compare Value** Compare value for GPT1.
10004020	GPT2_CON	32	**GPT2 Control** General control for GPT2.
10004024	GPT2_CLK	32	**GPT2 Clock Setting** Controls the clock source and division ratio of GPT clock.
10004028	GPT2_COUNT	32	**GPT2 Counter** Timer count of GPT2.
1000402C	GPT2_COMPARE	32	**GPT2 Compare Value** Compare value for GPT2.
10004030	GPT3_CON	32	**GPT3 Control** General control for GPT3.
10004034	GPT3_CLK	32	**GPT3 Clock Setting** Controls the clock source and division ratio of GPT clock.

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Address	Name	Width	Register Function
10004038	GPT3_COUNT	32	**GPT3 Counter** Timer count of GPT3.
1000403C	GPT3_COMPARE	32	**GPT3 Compare Value** Compare value for GPT3.
10004040	GPT4_CON	32	**GPT4 Control** General control for GPT4.
10004044	GPT4_CLK	32	**GPT4 Clock Setting** Controls the clock source and division ratio of GPT clock.
10004048	GPT4_COUNT	32	**GPT4 Counter** Timer count of GPT4.
1000404C	GPT4_COMPARE	32	**GPT4 Compare Value** Compare value for GPT4.
10004050	GPT5_CON	32	**GPT5 Control** General control for GPT5.
10004054	GPT5_CLK	32	**GPT5 Clock Setting** Controls the clock source and division ratio of GPT clock.
10004058	GPT5_COUNT	32	**GPT5 Counter** Timer count of GPT5.
1000405C	GPT5_COMPARE	32	**GPT5 Compare Value** Compare value for GPT5.
10004060	GPT6_CON	32	**GPT6 Control** General control for GPT6.
10004064	GPT6_CLK	32	**GPT6 Clock Setting** Controls the clock source and division ratio of GPT clock.
10004068	GPT6_COUNTL	32	**GPT6 Counter L** Lower word timer count for GPT6.
1000406C	GPT6_COMPAREL	32	**GPT6 Compare Value L** Lower word compare value for GPT6.
10004078	GPT6_COUNTH	32	**GPT6 Counter L** Higher word timer count for GPT6.
1000407C	GPT6_COMPAREH	32	**GPT6 Compare Value H** Higher word compare value for GPT6.

10004000 GPT_IRQEN GPT IRQ Enabling 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name											IRQEN					
Type											RW					
Reset											0	0	0	0	0	0

Overview Controls the enabling/disabling of GPT interrupt.

Bit(s)	Name	Description
5:0	IRQEN	**Enables interrupt of each GPT** 0: Disable associated interrupt of GPT 1: Enable associated interrupt of GPT

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10004004 GPT_IRQSTA GPT IRQ Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											IRQSTA					
Type											RO					
Reset											0	0	0	0	0	0

Overview Shows the interrupt status of each GPT.

Bit(s)	Name	Description
5:0	IRQSTA	**Interrupt status of each GPT** 0: No associated interrupt is generated 1: Associated interrupt is pending and waiting for service

10004008 GPT_IRQACK GPT IRQ Acknowledgement 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											IRQACK					
Type											WO					
Reset											0	0	0	0	0	0

Overview Acknowledges the GPT interrupt.

Bit(s)	Name	Description
5:0	IRQACK	**Interrupt acknowledgement for each GPT** 0: No effect 1: Associated interrupt request is acknowledged and should be relinquished.

10004010 GPT1_CON GPT1 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MODE1				CLR1	EN1
Type											RW				WO	RW
Reset											0	0			0	0

Overview General control for GPT1.

Bit(s)	Name	Description
5:4	MODE1	**Operation mode of GPT1** 00: ONE-SHOT mode

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Bit(s)	Name	Description
		01: REPEAT mode 10: KEEP-GO mode 11: FREERUN mode
1	CLR1	**Clears the counter of GPT1 to 0** 0: No effect 1: Clear
0	EN1	**Enables GPT1** 0: Disable 1: Enable

10004014 GPT1_CLK GPT1 Clock Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CLK1	CLKDIV1			
Type												RW	RW			
Reset												0	0	0	0	0

Overview Controls the clock source and division ratio of GPT clock.

Bit(s)	Name	Description
4	CLK1	**Sets up clock source of GPT1** 0: System clock (13MHz) 1: RTC clock (32kHz)
3:0	CLKDIV1	**Setting of GPT1 input clock frequency divider** 0000: Clock source divided by 1 0001: Clock source divided by 2 0010: Clock source divided by 3 0011: Clock source divided by 4 0100: Clock source divided by 5 0101: Clock source divided by 6 0110: Clock source divided by 7 0111: Clock source divided by 8 1000: Clock source divided by 9 1001: Clock source divided by 10 1010: Clock source divided by 11 1011: Clock source divided by 12 1100: Clock source divided by 13 1101: Clock source divided by 16 1110: Clock source divided by 32 1111: Clock source divided by 64

10004018 GPT1_COUNT GPT1 Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COUNTER1[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COUNTER1[15:0]															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview Timer count of GPT1.

Bit(s)	Name	Description
31:0	COUNTER1	Timer counter of GPT1

1000401C GPT1_COMPARE GPT1 Compare Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COMPARE1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMPARE1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview Compare value for GPT1.

Bit(s)	Name	Description
31:0	COMPARE1	Compare value of GPT1

10004020 GPT2_CON GPT2 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MODE2				CLR2	EN2
Type											RW				WO	RW
Reset											0	0			0	0

Overview General control for GPT2.

Bit(s)	Name	Description
5:4	MODE2	**Operation mode of GPT2** 00: ONE-SHOT mode 01: REPEAT mode 10: KEEP-GO mode 11: FREERUN mode
1	CLR2	**Clears the counter of GPT2 to 0** 0: No effect 1: Clear
0	EN2	**Enables GPT2** 0: Disable 1: Enable

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10004024 GPT2_CLK GPT2 Clock Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CLK2	CLKDIV2			
Type												RW	RW			
Reset												0	0	0	0	0

Overview Controls the clock source and division ratio of GPT clock.

Bit(s)	Name	Description
4	CLK2	**Sets up clock source of GPT2** 0: System clock (13MHz) 1: RTC clock (32kHz)
3:0	CLKDIV2	**Setting of GPT2 input clock frequency divider** 0000: Clock source divided by 1 0001: Clock source divided by 2 0010: Clock source divided by 3 0011: Clock source divided by 4 0100: Clock source divided by 5 0101: Clock source divided by 6 0110: Clock source divided by 7 0111: Clock source divided by 8 1000: Clock source divided by 9 1001: Clock source divided by 10 1010: Clock source divided by 11 1011: Clock source divided by 12 1100: Clock source divided by 13 1101: Clock source divided by 16 1110: Clock source divided by 32 1111: Clock source divided by 64

10004028 GPT2_COUNT GPT2 Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COUNTER2[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COUNTER2[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview Timer count of GPT2.

Bit(s)	Name	Description
31:0	COUNTER2	Timer counter of GPT2

1000402C GPT2_COMPARE GPT2 Compare Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	COMPARE2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMPARE2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview Compare value for GPT2.

Bit(s)	Name	Description
31:0	COMPARE2	Compare value of GPT2

10004030 GPT3_CON GPT3 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MODE3				CLR3	EN3
Type											RW				WO	RW
Reset											0	0			0	0

Overview General control for GPT3.

Bit(s)	Name	Description
5:4	MODE3	**Operation mode of GPT3** 00: ONE-SHOT mode 01: REPEAT mode 10: KEEP-GO mode 11: FREERUN mode
1	CLR3	**Clears the counter of GPT3 to 0** 0: No effect 1: Clear
0	EN3	**Enables GPT3** 0: Disable 1: Enable

10004034 GPT3_CLK GPT3 Clock Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CLK3	CLKDIV3			
Type												RW	RW			
Reset												0	0	0	0	0

Overview Controls the clock source and division ratio of GPT clock.

Bit(s)	Name	Description

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Bit(s)	Name	Description
4	CLK3	**Set clock source of GPT3** 0: System clock (13 MHz) 1: RTC clock (32 kHz)
3:0	CLKDIV3	**Setting of GPT3 input clock frequency divider** 0000: Clock source divided by 1 0001: Clock source divided by 2 0010: Clock source divided by 3 0011: Clock source divided by 4 0100: Clock source divided by 5 0101: Clock source divided by 6 0110: Clock source divided by 7 0111: Clock source divided by 8 1000: Clock source divided by 9 1001: Clock source divided by 10 1010: Clock source divided by 11 1011: Clock source divided by 12 1100: Clock source divided by 13 1101: Clock source divided by 16 1110: Clock source divided by 32 1111: Clock source divided by 64

10004038 GPT3_COUNT GPT3 Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COUNTER3[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COUNTER3[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview Timer count of GPT3.

Bit(s)	Name	Description
31:0	COUNTER3	Timer counter of GPT3

1000403C GPT3_COMPARE GPT3 Compare Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COMPARE3[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMPARE3[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview Compare value for GPT3.

Bit(s)	Name	Description
31:0	COMPARE3	Compare value of GPT3

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10004040 GPT4_CON GPT4 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name											MODE4				CLR4	EN4
Type											RW				WO	RW
Reset											0	0			0	0

Overview General control for GPT4.

Bit(s)	Name	Description
5:4	MODE4	**Operation mode of GPT4** 00: ONE-SHOT mode 01: REPEAT mode 10: KEEP-GO mode 11: FREERUN mode
1	CLR4	**Clears the counter of GPT4 to 0** 0: No effect 1: Clear
0	EN4	**Enables GPT4** 0: Disable 1: Enable

10004044 GPT4_CLK GPT4 Clock Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name												CLK4	CLKDIV4			
Type												RW	RW			
Reset												0	0	0	0	0

Overview Controls the clock source and division ratio of GPT clock.

Bit(s)	Name	Description
4	CLK4	**Sets up clock source of GPT4** 0: System clock (13MHz) 1: RTC clock (32kHz)
3:0	CLKDIV4	**Setting of GPT4 input clock frequency divider** 0000: Clock source divided by 1 0001: Clock source divided by 2 0010: Clock source divided by 3 0011: Clock source divided by 4 0100: Clock source divided by 5 0101: Clock source divided by 6 0110: Clock source divided by 7 0111: Clock source divided by 8 1000: Clock source divided by 9

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Bit(s)	Name	Description
		1001: Clock source divided by 10 1010: Clock source divided by 11 1011: Clock source divided by 12 1100: Clock source divided by 13 1101: Clock source divided by 16 1110: Clock source divided by 32 1111: Clock source divided by 64

10004048 GPT4_COUNT GPT4 Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COUNTER4[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COUNTER4[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview Timer count of GPT4.

Bit(s)	Name	Description
31:0	COUNTER4	Timer counter of GPT4

1000404C GPT4_COMPARE GPT4 Compare Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COMPARE4[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMPARE4[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview Compare value for GPT4.

Bit(s)	Name	Description
31:0	COMPARE4	Compare value of GPT4

10004050 GPT5_CON GPT5 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MODE5				CLR5	EN5
Type											RW				WO	RW
Reset											0	0			0	0

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Overview General control for GPT5.

Bit(s)	Name	Description
5:4	MODE5	**Operation mode of GPT5** 00: ONE-SHOT mode 01: REPEAT mode 10: KEEP-GO mode 11: FREERUN mode
1	CLR5	**Clears the counter of GPT5 to 0** 0: No effect 1: Clear
0	EN5	**Enables GPT5** 0: Disable 1: Enable

10004054 GPT5_CLK GPT5 Clock Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CLK5	CLKDIV5			
Type												RW	RW			
Reset												0	0	0	0	0

Overview Controls the clock source and division ratio of GPT clock.

Bit(s)	Name	Description
4	CLK5	**Set clock source of GPT5** 0: System clock (13 MHz) 1: RTC clock (32 kHz)
3:0	CLKDIV5	**Setting of GPT5 input clock frequency divider** 0000: Clock source divided by 1 0001: Clock source divided by 2 0010: Clock source divided by 3 0011: Clock source divided by 4 0100: Clock source divided by 5 0101: Clock source divided by 6 0110: Clock source divided by 7 0111: Clock source divided by 8 1000: Clock source divided by 9 1001: Clock source divided by 10 1010: Clock source divided by 11 1011: Clock source divided by 12 1100: Clock source divided by 13 1101: Clock source divided by 16 1110: Clock source divided by 32 1111: Clock source divided by 64

10004058 GPT5_COUNT GPT5 Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COUNTER5[31:16]															

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Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**COUNTER5[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview Timer count of GPT5.

Bit(s)	Name	Description
31:0	COUNTER5	Timer counter of GPT5

1000405C GPT5_COMPARE GPT5 Compare Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**COMPARE5[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**COMPARE5[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview Compare value for GPT5.

Bit(s)	Name	Description
31:0	COMPARE5	Compare value of GPT5

10004060 GPT6_CON GPT6 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											**MODE6**				**CLR6**	**EN6**
Type											RW				WO	RW
Reset											0	0			0	0

Overview General control for GPT6.

Bit(s)	Name	Description
5:4	MODE6	**Operation mode of GPT3** 00: ONE-SHOT mode 01: REPEAT mode 10: KEEP-GO mode 11: FREERUN mode
1	CLR6	**Clears the counter of GPT3 to 0** 0: No effect 1: Clear
0	EN6	**Enables GPT3**

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Bit(s)	Name	Description
		0: Disable 1: Enable

10004064 GPT6_CLK GPT6 Clock Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CLK6	CLKDIV6			
Type												RW	RW			
Reset												0	0	0	0	0

Overview Controls the clock source and division ratio of GPT clock.

Bit(s)	Name	Description
4	CLK6	**Set clock source of GPT3** 0: System clock (13 MHz) 1: RTC clock (32 kHz)
3:0	CLKDIV6	**Setting of GPT3 input clock frequency divider** 0000: Clock source divided by 1 0001: Clock source divided by 2 0010: Clock source divided by 3 0011: Clock source divided by 4 0100: Clock source divided by 5 0101: Clock source divided by 6 0110: Clock source divided by 7 0111: Clock source divided by 8 1000: Clock source divided by 9 1001: Clock source divided by 10 1010: Clock source divided by 11 1011: Clock source divided by 12 1100: Clock source divided by 13 1101: Clock source divided by 16 1110: Clock source divided by 32 1111: Clock source divided by 64

10004068 GPT6_COUNT L GPT6 Counter L 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COUNTER6L[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COUNTER6L[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview Lower word timer count for GPT6.

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:0	COUNTER6L	**Lower word of timer count of GPT6** A read operation of GPT6_COUNTL will make GPT6_COUNTH fixed until the next read operation of GPT6_COUNTL.

1000406C GPT6_COMPAREL GPT6 Compare Value L 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COMPARE6L[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMPARE6L[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview Lower word compare value for GPT6.

Bit(s)	Name	Description
31:0	COMPARE6L	Lower word of compare value of GPT6

10004078 GPT6_COUNTH GPT6 Counter L 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COUNTER6H[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COUNTER6H[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview Higher word timer count for GPT6.

Bit(s)	Name	Description
31:0	COUNTER6H	Higher word of timer count of GPT6

1000407C GPT6_COMPAREH GPT6 Compare Value H 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COMPARE6H[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMPARE6H[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Overview Higher word compare value for GPT6.

Bit(s)	Name	Description
31:0	COMPARE6H	Higher word of compare of GPT6

5.12.5 Programming Guide

To program and use GPT, note that:
The counter value can be read any time even when the clock source is RTC clock.

- The compare value can be programmed any time.

For the GPT6 64-bit timer, the read operation of the 64-bit timer value will be separated into two APB reads since an APB read is of 32-bit width. To perform the read of 64-bit timer value, the lower word should be read first then the higher word. The read operation of lower word freezes the “read value” of the higher word but does not freeze the timer counting. This ensures that the separated read operation acquires the correct timer value. If both two tasks, e.g. task A and task B, perform the read of 64-bit timer value, task A first reads the lower word of the value, and task B reads the lower word of the value. Either of the tasks reads the higher word of timer value, and the obtained value will be the time when task B reads the lower word of timer value. To guarantee task A reads the correct 64-bit timer value, some software procedures are required, e.g. the semaphore.

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5.13 Thermal Controller

5.13.1 Introduction

On mobile platform, thermal management is very fundamental. The thermal management controls the platform computing performance to achieve the requirement and maintain the Raven within the temperature constraints. Operation under over-high temperature for a long time will have a risk of damage for Raven reliability.

In MT6735, it embeds several temperature sensors in possible hot spots on the die. The thermal controller module executes a periodic measurement for each hot spot. The temperature readings are readable for software.

In order to minimize the software effort nf temperature monitoring, the thermal controller generates interrupts to microprocessors which informs the abnormal condition.

5.13.2 Features

- Supports up to three thermal sensors
- Periodic temperature measurement
- Temperature monitoring
- Different types of low pass filters for thermal sensor reading

5.13.3 Block Diagram

There are four microprocessors in MT6735. Their maximum frequency is up to over 1.3GHz and the transistor count is also large. The power consumed by microprocessors occupies a high percentage of the entire chip power consumption. Besides the microprocessors, EMI is also a source of power consumption because it provides high DRAM data bandwidth to other modules in MT6735.

The thermal controller is implemented for the software to operate MT6735 with a pre-defined temperature range. Or it will have function failure and reliability issues. According to temperature measurement, the system performance can be adjusted and the system design for power dissipation can also be monitored.

The hottest location in MT6735 may be different in different applications. Besides, when the thermal controller informs the software of an abnormal condition, the following power reduction action should be an efficient and low latency.

In general, there are two methods for embedded CMOS temperature sensor:

- VBE temperature sensor
- ▵ VBE temperature sensor (PTAT temperature sensor)

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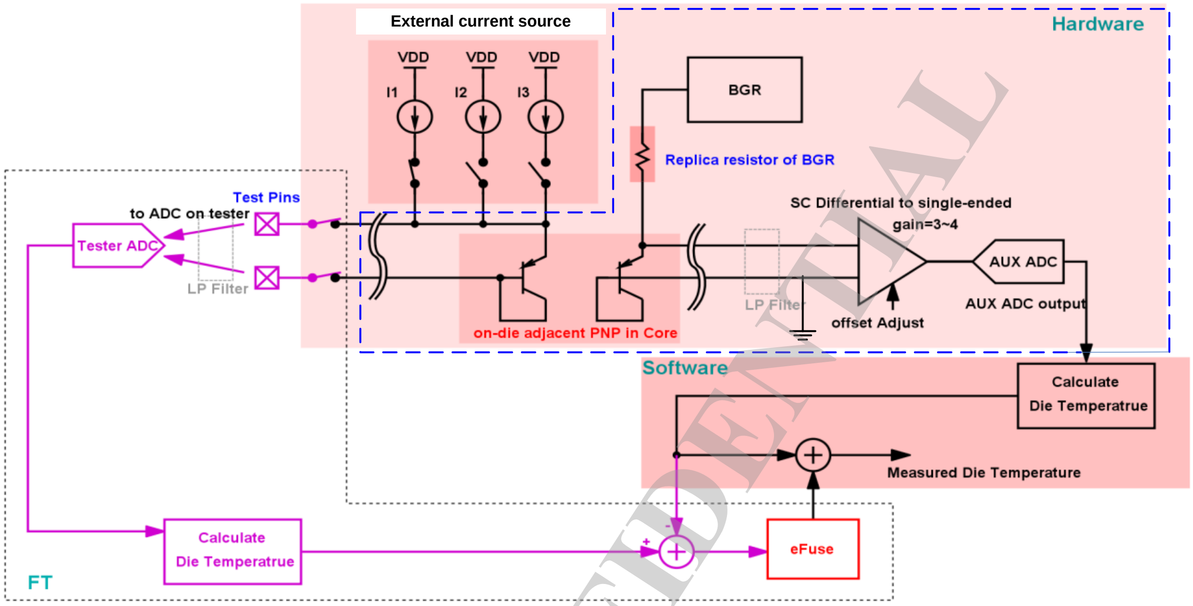

Figure 5-23. Implementation of CMOS temperature sensor

The accuracy target is 2°C when the temperature is in the range of 0 ~ 85°C. We use VBE as a CMOS sensor:

Consider

$$Ic = Is \cdot e^{\frac{V_{BE}}{\frac{nkT}{q}}}$$

$$\Rightarrow V_{BE} = \frac{nkT}{q} \cdot \ln \frac{I_C}{I_S}$$

- -1.665mV/°C in N40 process (TT, RTyp)

And use 12-bit SAR AUXADC for data conversion. The resolution of AUXADC is about $2.5V/2^{12}$= 0.6mV. But for △ VBE method,

△ VBE = nkT/q x lnN

- k/q=0.086mV/°C

The resolution of AUXADC is not enough.

Considering offset, we calibrate the offset in FT and use e-fuse to store the calibrated value.

- △ VBE based approach for die temperature offset calibration.

There is no need to wait for thermal equilibrium in FT. However, it needs unused PAD and external bias circuit in FT.

1. Consider the BJT series resistor,

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$$\Delta V_{BE} = \frac{\beta}{1+\beta} R_S (I_{C_1} - I_{C_2}) + \frac{nkT}{q} \cdot \ln \frac{I_{C_1}}{I_{C_2}} \frac{I_{S_2}}{I_{S_1}} = \frac{\beta}{1+\beta} R_S (I_{C_1} - I_{C_2}) + \frac{nkT}{q} \ln \frac{N}{M}$$

2. By applying IC1, IC2 and IC3, the three different current in FT, we can get the following equation and solve it for RS and T.

$$\Delta V_{BE1} = \frac{\beta}{1+\beta} R_S (I_{C_2} - I_{C_1}) + \frac{nkT}{q} \ln N_1$$

$$\Delta V_{BE2} = \frac{\beta}{1+\beta} R_S (I_{C_3} - I_{C_2}) + \frac{nkT}{q} \ln N_2$$

- Comparing the T measured via on chip ADC and the T got in the above equations, we can calibrate the temperature offset.

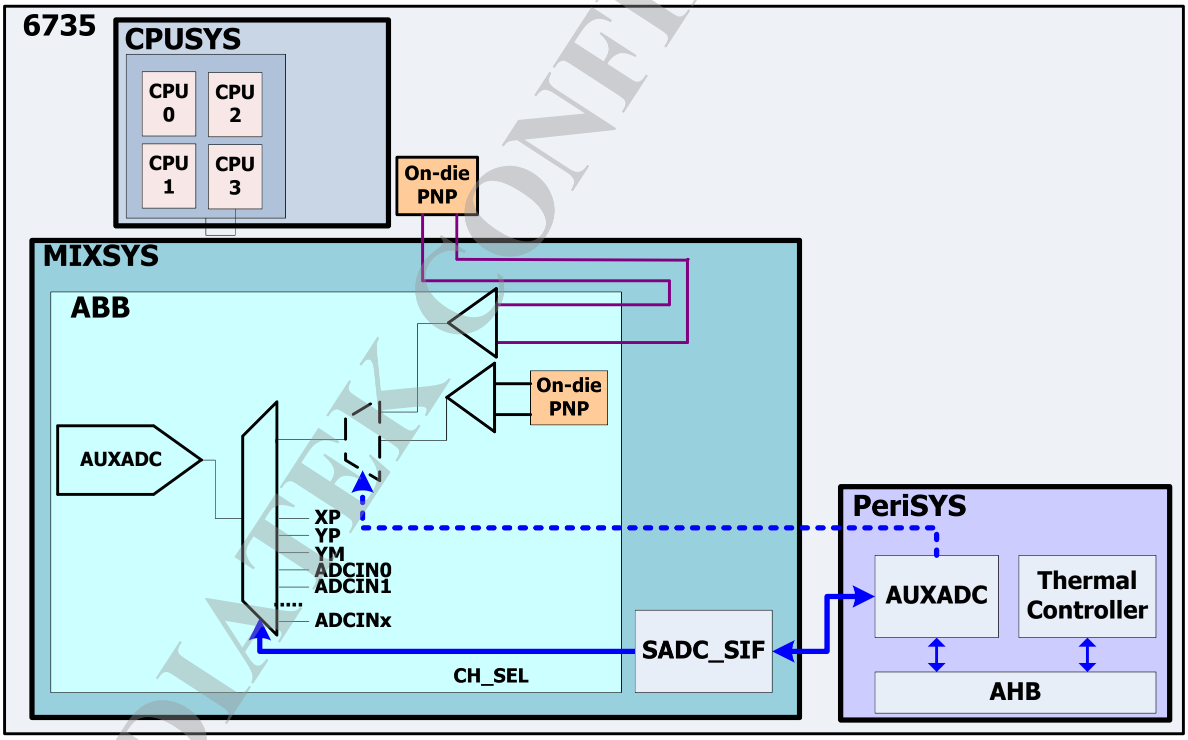

Figure 5-24. Block diagram of system temperature measurement

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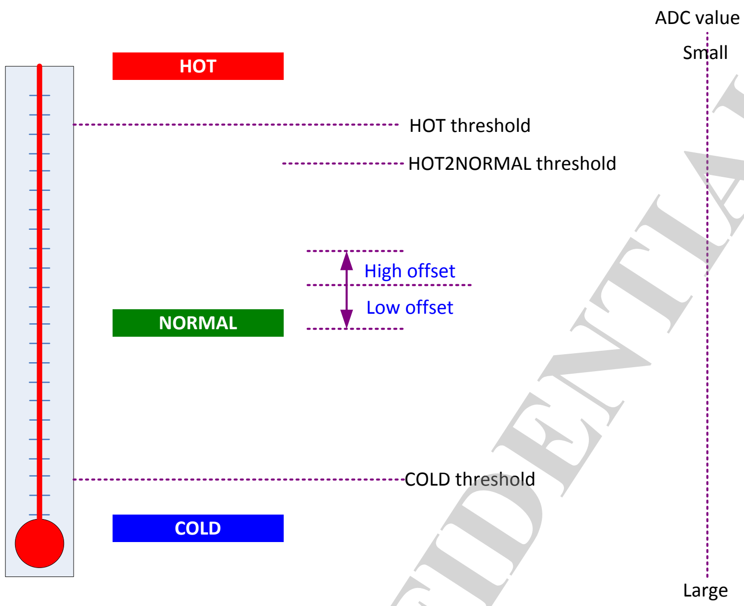

Figure 5-25. Block diagram of system temperature measurement

5.13.4 Register Definition

Module name: ptp_therm_ctrl Base address: (+1100B000h)

Address	Name	Width	Register Function
1100B000	TEMPMONCTL0	32	Temperature Monitoring Control 0
1100B004	TEMPMONCTL1	32	Temperature Monitoring Control 1
1100B008	TEMPMONCTL2	32	**Temperature Monitoring Control 2** This register is fixed to 0 when RTC_POWERKEY1 & RTC_POWERKEY2 unmatch the correct values.
1100B00C	TEMPMONINT	32	Temperature Monitoring Interrupt Enable
1100B010	TEMPMONINTSTS	32	Temperature Monitoring Interrupt Status
1100B014	TEMPMONIDET0	32	Sensing Point 0 Temperature Monitoring Detection
1100B018	TEMPMONIDET1	32	Sensing Point 1 Temperature Monitoring Detection
1100B01C	TEMPMONIDET2	32	Sensing Point 2 Temperature Monitoring Detection
1100B024	TEMPH2NTHRE	32	Temperature HOT2NORMAL Threshold
1100B028	TEMPHTHRE	32	Temperature Hot Threshold
1100B02C	TEMPCTHRE	32	Temperature Cold Threshold
1100B030	TEMPOFFSETH	32	Temperature High Offset Threshold
1100B034	TEMPOFFSETL	32	Temperature Low Offset Threshold
1100B038	TEMPMSRCTL0	32	Temperature Measure Control 0
1100B03C	TEMPMSRCTL1	32	Temperature Measure Control 1
1100B040	TEMPAHBPOLL	32	Temperature AHB Polling
1100B044	TEMPAHBTO	32	Temperature AHB Polling Timeout
1100B048	TEMPADCPNP0	32	ADC Mux Selection Value
1100B04C	TEMPADCPNP1	32	ADC Mux Selection Value

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Address	Name	Width	Register Function
1100B050	**TEMPADCPNP2**	32	ADC Mux Selection Value
1100B054	**TEMPADCMUX**	32	ADC Mux Selection
1100B058	**TEMPADCEXT**	32	ADC Extra Write
1100B05C	**TEMPADCEXT1**	32	ADC Extra Write 1
1100B060	**TEMPADCEN**	32	ADC Enable
1100B064	**TEMPPNPMUXADDR**	32	PNP Mux Selection Address
1100B068	**TEMPADCMUXADDR**	32	ADC Mux Selection Address
1100B06C	**TEMPADCEXTADDR**	32	ADC Extra Write Address
1100B070	**TEMPADCEXT1ADDR**	32	ADC Extra Write Address 1
1100B074	**TEMPADCENADDR**	32	ADC Enable Address
1100B078	**TEMPADCVALIDADDR**	32	ADC Voltage Valid Reading Address
1100B07C	**TEMPADCVOLTADDR**	32	ADC Voltage Reading Address
1100B080	**TEMPRDCTRL**	32	ADC Voltage Read Control
1100B084	**TEMPADCVALIDMASK**	32	ADC Valid Mask
1100B088	**TEMPADCVOLTAGESHIFT**	32	ADC Voltage Shift
1100B08C	**TEMPADCWRITECTRL**	32	ADC Write Control
1100B090	**TEMPMSR0**	32	Temperature Measure Reading 0
1100B094	**TEMPMSR1**	32	Temperature Measure Reading 1
1100B098	**TEMPMSR2**	32	Temperature Measure Reading 2
1100B0A0	**TEMPIMMD0**	32	Temperature IMMD Measure Reading 0
1100B0A4	**TEMPIMMD1**	32	Temperature IMMD Measure Reading 1
1100B0A8	**TEMPIMMD2**	32	Temperature IMMD Measure Reading 2
1100B0B0	**TEMPMONIDET3**	32	Sensing Point 3 Temperature Monitoring Detection
1100B0B4	**TEMPADCPNP3**	32	ADC Mux Selection Value
1100B0B8	**TEMPMSR3**	32	Temperature Measure Reading 3
1100B0BC	**TEMPIMMD3**	32	Temperature IMMD Measure Reading 3
1100B0C0	**TEMPPROTCTL**	32	Thermal Protection Sensor Selection
1100B0C4	**TEMPPROTTA**	32	Temperature Protection STAGE1
1100B0C8	**TEMPPROTTB**	32	Temperature Protection STAGE2
1100B0CC	**TEMPPROTTC**	32	Temperature Protection STAGE3
1100B0F0	**TEMPSPARE0**	32	Spare Register For Debug 0
1100B0F4	**TEMPSPARE1**	32	Spare Register For Debug 1
1100B0F8	**TEMPSPARE2**	32	Spare Register For Debug 2
1100B0FC	**TEMPSPARE3**	32	Spare Register For Debug 3
1100B400	**PTPCORESEL**	32	
1100B404	**THERMINTST**	32	
1100B408	**PTPODINTST**	32	
1100B40C	**THSTAGE0ST**	32	
1100B410	**THSTAGE1ST**	32	

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Address	Name	Width	Register Function
1100B414	THSTAGE2ST	32	
1100B418	THAHBST0	32	
1100B41C	THAHBST1	32	
1100B420	PTPSPARE0	32	
1100B424	PTPSPARE1	32	
1100B428	PTPSPARE2	32	
1100B42C	PTPSPARE3	32	
1100B430	THSLPEVEB	32	

1100B000 TEMPMONCTL0 Temperature Monitoring Control 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name													SENSE3_EN	SENSE2_EN	SENSE1_EN	SENSE0_EN
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3		SENSE3_EN	**Enable periodic temperature measurement on sensing point 2** 0: Disable 1: Enable 0: Disable 1: Enable
2	SENSE2_EN	SENSE2_EN	**Enables periodic temperature measurement on sensing point 2** 0: Disable 1: Enable 0: Disable 1: Enable
1	SENSE1_EN	SENSE1_EN	**Enables periodic temperature measurement on sensing point 1** 0: Disable 1: Enable 0: Disable 1: Enable
0	SENSE0_EN	SENSE0_EN	**Enables periodic temperature measurement on sensing point 0** 0: Disable 1: Enable 0: Disable 1: Enable

1100B004 TEMPMONCTL1 Temperature Monitoring Control 1 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																HOTINT_SEL3
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HOTINT_SEL2	HOTINT_SEL1	HOTINT_SEL0				PERIOD_UNIT									
Type	RW	RW	RW				RW									
Reset	0	0	0				0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16		HOTINT_SEL3	**Selects hot interrupt for sensing point 2** 0: All when it is normal to over hot threshold 1: Only the first time when it is normal to over hot threshold 0: All when it is normal to over hot threshold 1: Only the first time when it is normal to over hot threshold
15	**HOTINT_SEL2**	HOTINT_SEL2	**Selects hot interrupt for sensing point 2** 0: All when it is normal to over hot threshold 1: Only the first time when it is normal to over hot threshold 0: All when it is normal to over hot threshold 1: Only the first time when it is normal to over hot threshold
14	**HOTINT_SEL1**	HOTINT_SEL1	**Selects hot interrupt for sensing point 1** 0: All when it is normal to over hot threshold 1: Only the first time when it is normal to over hot threshold 0: All when it is normal to over hot threshold 1: Only the first time when it is normal to over hot threshold
13	**HOTINT_SEL0**	HOTINT_SEL0	**Selects hot interrupt for sensing point 0** 0: All when it is normal to over hot threshold 1: Only the first time when it is normal to over hot threshold 0: All when it is normal to over hot threshold 1: Only the first time when it is normal to over hot threshold
9:0	**PERIOD_UNIT**	PERIOD_UNIT	

1100B008 TEMPMONCTL2 Temperature Monitoring Control 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FILT_INTRVAL									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SEN_INTRVAL									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
25:16		FILT_INTRVAL	
9:0	**SEN_INTRVAL**	SEN_INTRVAL	

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1100B00C TEMPMONINT Temperature Monitoring Interrupt Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STAGE3_INT_EN	STAGE2_INT_EN	STAGE1_INT_EN	FILTER_INT_EN_3	IMMD_INT_EN_3	NOHOTINTEN3	HOFSINTEN3	LOFSINTEN3	HINTEN3	CINTEN3	FILTER_INT_EN_2	FILTER_INT_EN_1	FILTER_INT_EN_0	IMMD_INT_EN_2	IMMD_INT_EN_1	IMMD_INT_EN_0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TIME_OUT_INT_EN	NOHOTINTEN2	HOFSINTEN2	LOFSINTEN2	HINTEN2	CINTEN2	NOHOTINTEN1	HOFSINTEN1	LOFSINTEN1	HINTEN1	CINTEN1	NOHOTINTEN0	HOFSINTEN0	LOFSINTEN0	HINTEN0	CINTEN0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**STAGE3_INT_EN**	STAGE3_INT_EN	**Enables interrupt for thermal protection stage 3** 0: Disable 1: Enable 0: Disable 1: Enable
30	**STAGE2_INT_EN**	STAGE2_INT_EN	**Enables interrupt for thermal protection stage 2** 0: Disable 1: Enable 0: Disable 1: Enable
29	**STAGE1_INT_EN**	STAGE1_INT_EN	**Enables interrupt for thermal protection stage 1** 0: Disable 1: Enable 0: Disable 1: Enable
28	**FILTER_INT_EN_3**	FILTER_INT_EN_3	**Enables filter sense interrupt for sensing point 2** 0: Disable 1: Enable 0: Disable 1: Enable
27	**IMMD_INT_EN_3**	IMMD_INT_EN_3	**Enables immediate sense interrupt for sensing point 2** 0: Disable 1: Enable 0: Disable 1: Enable
26	**NOHOTINTEN3**	NOHOTINTEN3	**Enables hot to normal interrupt for sensing point 3** 0: Disable 1: Enable 0: Disable 1: Enable
25	**HOFSINTEN3**	HOFSINTEN3	**Enables high offset interrupt for sensing point 3** 0: Disable 1: Enable 0: Disable 1: Enable
24	**LOFSINTEN3**	LOFSINTEN3	**Enables low offset interrupt for sensing point 3** 0: Disable 1: Enable 0: Disable 1: Enable
23	**HINTEN3**	HINTEN3	**Enables hot threshold interrupt for sensing point 3**

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Bit(s)	Mnemonic	Name	Description
			0: Disable 1: Enable 0: Disable 1: Enable
22	**CINTEN3**	CINTEN3	**Enables cold threshold interrupt for sensing point 3** 0: Disable 1: Enable 0: Disable 1: Enable
21	**FILTER_INT_EN_2**	FILTER_INT_EN_2	**Enables filter sense interrupt for sensing point 2** 0: Disable 1: Enable 0: Disable 1: Enable
20	**FILTER_INT_EN_1**	FILTER_INT_EN_1	**Enables filter sense interrupt for sensing point 1** 0: Disable 1: Enable 0: Disable 1: Enable
19	**FILTER_INT_EN_0**	FILTER_INT_EN_0	**Enables filter sense interrupt for sensing point 0** 0: Disable 1: Enable 0: Disable 1: Enable
18	**IMMD_INT_EN_2**	IMMD_INT_EN_2	**Enables immediate sense interrupt for sensing point 2** 0: Disable 1: Enable 0: Disable 1: Enable
17	**IMMD_INT_EN_1**	IMMD_INT_EN_1	**Enables immediate sense interrupt for sensing point 1** 0: Disable 1: Enable 0: Disable 1: Enable
16	**IMMD_INT_EN_0**	IMMD_INT_EN_0	**Enables immediate sense interrupt for sensing point 0** 0: Disable 1: Enable 0: Disable 1: Enable
15	**TIME_OUT_INT_EN**	TIME_OUT_INT_EN	**Enables AHB polling temperature time-out interrupt** 0: Disable 1: Enable 0: Disable 1: Enable
14	**NOHOTINTEN2**	NOHOTINTEN2	**Enables hot to normal interrupt for sensing point 2** 0: Disable 1: Enable 0: Disable 1: Enable
13	**HOFSINTEN2**	HOFSINTEN2	**Enables high offset interrupt for sensing point 2** 0: Disable 1: Enable 0: Disable 1: Enable
12	**LOFSINTEN2**	LOFSINTEN2	**Enables low offset interrupt for sensing point 2** 0: Disable 1: Enable

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Bit(s)	Mnemonic	Name	Description
			0: Disable 1: Enable
11	**HINTEN2**	HINTEN2	**Enables hot threshold interrupt for sensing point 2** 0: Disable 1: Enable 0: Disable 1: Enable
10	**CINTEN2**	CINTEN2	**Enables cold threshold interrupt for sensing point 2** 0: Disable 1: Enable 0: Disable 1: Enable
9	**NOHOTINTEN1**	NOHOTINTEN1	**Enables hot to normal interrupt for sensing point 1** 0: Disable 1: Enable 0: Disable 1: Enable
8	**HOFSINTEN1**	HOFSINTEN1	**Enables high offset interrupt for sensing point 1** 0: Disable 1: Enable 0: Disable 1: Enable
7	**LOFSINTEN1**	LOFSINTEN1	**Enables low offset interrupt for sensing point 1** 0: Disable 1: Enable 0: Disable 1: Enable
6	**HINTEN1**	HINTEN1	**Enables hot threshold interrupt for sensing point 1** 0: Disable 1: Enable 0: Disable 1: Enable
5	**CINTEN1**	CINTEN1	**Enables cold threshold interrupt for sensing point 1** 0: Disable 1: Enable 0: Disable 1: Enable
4	**NOHOTINTEN0**	NOHOTINTEN0	**Enables hot to normal interrupt for sensing point 0** 0: Disable 1: Enable 0: Disable 1: Enable
3	**HOFSINTEN0**	HOFSINTEN0	**Enables high offset interrupt for sensing point 0** 0: Disable 1: Enable 0: Disable 1: Enable
2	**LOFSINTEN0**	LOFSINTEN0	**Enables low offset interrupt for sensing point 0** 0: Disable 1: Enable 0: Disable 1: Enable
1	**HINTEN0**	HINTEN0	**Enables hot threshold interrupt for sensing point 0** 0: Disable 1: Enable 0: Disable

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Bit(s)	Mnemonic	Name	Description
			1: Enable
0	**CINTEN0**	CINTEN0	**Enables cold threshold interrupt for sensing point 0** 0: Disable 1: Enable 0: Disable 1: Enable

1100B010 **TEMPMONINTSTS** **Temperature Monitoring Interrupt Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STAGE3_INT_STAT	STAGE2_INT_STAT	STAGE1_INT_STAT	FILTER_INT_STAT_3	IMMD_INT_STAT_3	NOHOTINTSTS3	HOFSINTSTS3	LOFSINTSTS3	HINTSTS3	LINTSTS3	FILTER_INT_STAT_2	FILTER_INT_STAT_1	FILTER_INT_STAT_0	IMMD_INT_STAT_2	IMMD_INT_STAT_1	IMMD_INT_STAT_0
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TIMEOUTINTSTS		HOFSINTSTS2	LOFSINTSTS2	HINTSTS2	LINTSTS2	NOHOTINTSTS1	HOFSINTSTS1	LOFSINTSTS1	HINTSTS1	LINTSTS1	NOHOTINTSTS0	HOFSINTSTS0	LOFSINTSTS0	HINTSTS0	LINTSTS0
Type	RU		RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**STAGE3_INT_STAT**	STAGE3_INT_STAT	
30	**STAGE2_INT_STAT**	STAGE2_INT_STAT	
29	**STAGE1_INT_STAT**	STAGE1_INT_STAT	
28	**FILTER_INT_STAT_3**	FILTER_INT_STAT_3	
27	**IMMD_INT_STAT_3**	IMMD_INT_STAT_3	
26	**NOHOTINTSTS3**	NOHOTINTSTS3	
25	**HOFSINTSTS3**	HOFSINTSTS3	
24	**LOFSINTSTS3**	LOFSINTSTS3	
23	**HINTSTS3**	HINTSTS3	
22	**LINTSTS3**	LINTSTS3	
21	**FILTER_INT_STAT_2**	FILTER_INT_STAT_2	
20	**FILTER_INT_STAT_1**	FILTER_INT_STAT_1	
19	**FILTER_INT_STAT_0**	FILTER_INT_STAT_0	
18	**IMMD_INT_STAT_2**	IMMD_INT_STAT_2	
17	**IMMD_INT**	IMMD_INT_STAT	

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Bit(s)	Mnemonic	Name	Description
	_STAT_1	_1	
16	**IMMD_INT_STAT_0**	IMMD_INT_STAT_0	
15	**TIMEOUTINTSTS**	TIMEOUTINTSTS	
13	**HOFSINTSTS2**	HOFSINTSTS2	
12	**LOFSINTSTS2**	LOFSINTSTS2	
11	**HINTSTS2**	HINTSTS2	
10	**LINTSTS2**	LINTSTS2	
9	**NOHOTINTSTS1**	NOHOTINTSTS1	
8	**HOFSINTSTS1**	HOFSINTSTS1	
7	**LOFSINTSTS1**	LOFSINTSTS1	
6	**HINTSTS1**	HINTSTS1	
5	**LINTSTS1**	LINTSTS1	
4	**NOHOTINTSTS0**	NOHOTINTSTS0	
3	**HOFSINTSTS0**	HOFSINTSTS0	
2	**LOFSINTSTS0**	LOFSINTSTS0	
1	**HINTSTS0**	HINTSTS0	
0	**LINTSTS0**	LINTSTS0	

1100B014 **TEMPMONIDET0** **Sensing Point 0 Temperature Monitoring Detection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**NOHOTIMES**		**HOTIMES**		**LOTIMES**		**HTIMES**		**CTIMES**	
Type							RW		RW		RW		RW		RW	
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
9:8		NOHOTIMES	**Times of hot to normal interrupt occurrence** 00: 1 01: 2 10: 3 11: 4 00: 1 01: 2 10: 3 11: 4
7:6	**HOTIMES**	HOTIMES	**Times of high offset interrupt occurrence**

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Bit(s)	Mnemonic	Name	Description
			00: 1 01: 2 10: 3 11: 4 00: 1 01: 2 10: 3 11: 4
5:4	**LOTIMES**	LOTIMES	**Times of low offset interrupt occurrence** 00: 1 01: 2 10: 3 11: 4 00: 1 01: 2 10: 3 11: 4
3:2	**HTIMES**	HTIMES	**Times of hot threshold interrupt occurrence** 00: 1 01: 2 10: 3 11: 4 00: 1 01: 2 10: 3 11: 4
1:0	**CTIMES**	CTIMES	**Times of cold threshold interrupt occurrence** 00: 1 01: 2 10: 3 11: 4 00: 1 01: 2 10: 3 11: 4

1100B018 **TEMPMONIDET1** **Sensing Point 1 Temperature Monitoring Detection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							NOHOTIMES		HOTIMES		LOTIMES		HTIMES		CTIMES	
Type							RW		RW		RW		RW		RW	
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
9:8		NOHOTIMES	**Times of hot to normal interrupt occurrence** 00: 1 01: 2 10: 3 11: 4 00: 1 01: 2

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Bit(s)	Mnemonic	Name	Description
			10: 3 11: 4
7:6	**HOTIMES**	HOTIMES	**Times of high offset interrupt occurrence** 00: 1 01: 2 10: 3 11: 4 00: 1 01: 2 10: 3 11: 4
5:4	**LOTIMES**	LOTIMES	**Times of low offset interrupt occurrence** 00: 1 01: 2 10: 3 11: 4 00: 1 01: 2 10: 3 11: 4
3:2	**HTIMES**	HTIMES	**Times of hot threshold interrupt occurrence** 00: 1 01: 2 10: 3 11: 4 00: 1 01: 2 10: 3 11: 4
1:0	**CTIMES**	CTIMES	**Times of cold threshold interrupt occurrence** 00: 1 01: 2 10: 3 11: 4 00: 1 01: 2 10: 3 11: 4

1100B01C **TEMPMONIDET2** **Sensing Point 2 Temperature Monitoring Detection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							NOHOTIMES		HOTIMES		LOTIMES		HTIMES		CTIMES	
Type							RW		RW		RW		RW		RW	
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
9:8		NOHOTIMES	**Times of hot to normal interrupt occurrence** 00: 1 01: 2 10: 3

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Bit(s)	Mnemonic	Name	Description
			11: 4 00: 1 01: 2 10: 3 11: 4
7:6	**HOTIMES**	HOTIMES	**Times of high offset interrupt occurrence** 00: 1 01: 2 10: 3 11: 4 00: 1 01: 2 10: 3 11: 4
5:4	**LOTIMES**	LOTIMES	**Times of low offset interrupt occurrence** 00: 1 01: 2 10: 3 11: 4 00: 1 01: 2 10: 3 11: 4
3:2	**HTIMES**	HTIMES	**Times of hot threshold interrupt occurrence** 00: 1 01: 2 10: 3 11: 4 00: 1 01: 2 10: 3 11: 4
1:0	**CTIMES**	CTIMES	**Times of cold threshold interrupt occurrence** 00: 1 01: 2 10: 3 11: 4 00: 1 01: 2 10: 3 11: 4

1100B024 **TEMPH2NTHRE** **Temperature HOT2NORMAL Threshold** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					HOT2NORMAL_THRE											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0		HOT2NORMAL_THRE	

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1100B028 TEMPHTHRE Temperature Hot Threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**HOT_THRE**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0		HOT_THRE	

1100B02C TEMPCTHRE Temperature Cold Threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**COLD_THRE**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0		COLD_THRE	

1100B030 TEMPOFFSETH Temperature High Offset Threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**HIGH_OFFSET**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0		HIGH_OFFSET	

1100B034 TEMPOFFSETL Temperature Low Offset Threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					LOW_OFFSET											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0		LOW_OFFSET	

1100B038 **TEMPMSRCTL0** **Temperature Measure Control 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					MSRCTL3			MSRCTL2			MSRCTL1			MSRCTL0		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:9		MSRCTL3	000: One sampling 001: Average 2 samplings 010: 4 samplings; drop max. and min. then average 2 samples 011: 6 samplings; drop max. and min. then averageg 4 samples 100: 10 sampling; drop max. and min. then average 8 samples 101: 18 samplings; drop max. and min, then average 16 samples Others: One sampling
8:6	**MSRCTL2**	MSRCTL2	000: One sampling 001: Average 2 samplings 010: 4 samplings; drop max. and min. then average 2 samples 011: 6 samplings; drop max. and min. then average 4 samples 100: 10 samplings; drop max. and min. then average 8 samples 101: 18 samplings; drop max. and min. then average 16 samples Others: One sampling
5:3	**MSRCTL1**	MSRCTL1	000: One sampling 001: Average 2 sampling 010: 4 sampling; drop max. and min. then average 2 samples 011: 6 sampling; drop max. and min. then average 4 samples 100: 10 sampling; drop max. and min. then average 8 samples 101: 18 sampling; drop max. and min. then average 16 samples Others: One sampling
2:0	**MSRCTL0**	MSRCTL0	000: One sampling 001: Average 2 samplings 010: 4 samplings; drop max. and min. then average 2 samples 011: 6 samplings; drop max. and min. then average 4 samples 100: 10 samplings; drop max. and min. then average 8 samples 101: 18 samplings; drop max. and min. then average 16 samples Others: One sampling

1100B03C **TEMPMSRCTL1** **Temperature Measure Control 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

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Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**MSR3IMM**	**PAUSE3**	**MSRSTS1**	**MSR2IMM**	**MSR1IMM**	**MSR0IMM**	**PAUSE2**	**PAUSE1**	**PAUSE0**	**MSRSTS0**
Type							RW	RW	RU	RW	RW	RW	RW	RW	RW	RU
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
9		MSR3IMM	0: Disable 1: Enable
8	**PAUSE3**	PAUSE3	0: Release pause 1: Pause
7	**MSRSTS1**	MSRSTS1	**Temperature measurement bus status[1]** 00: IDLE 01: Write transaction 10: Read transaction 11: Wait for read after write 00: IDLE 01: Write transaction 10: Read transaction 11: Waiting for read after write
6	**MSR2IMM**	MSR2IMM	0: Disable 1: Enable
5	**MSR1IMM**	MSR1IMM	0: Disable 1: Enable
4	**MSR0IMM**	MSR0IMM	0: Disable 1: Enable
3	**PAUSE2**	PAUSE2	0: Release pause 1: Pause
2	**PAUSE1**	PAUSE1	0: Release pause 1: Pause
1	**PAUSE0**	PAUSE0	0: Release pause 1: Pause
0	**MSRSTS0**	MSRSTS0	**Temperature measurement bus status[0]** 00: IDLE 01: Write transaction 10: Read transaction 11: Wait for read after write 00: IDLE 01: Write transaction 10: Read transaction 11: Waiting for read after write

1100B040 **TEMPAHBPOLL** **Temperature AHB Polling** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**ADC_POLL_INTVL[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ADC_POLL_INTVL[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
31:0	ADC_POLL_INTVL	ADC_POLL_INTVL	**Time interval for AHB polling the temperature voltage from AUXADC** Unit: 32k

1100B044 TEMPAHBTO Temperature AHB Polling Timeout FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADC_TIMEOUT[31:16]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_TIMEOUT[15:0]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0	ADC_TIMEOUT	ADC_TIMEOUT	**Timeout time for AHB polling the temperature voltage from AUXADC without getting any response** Unit: 32k

1100B048 TEMPADCPNP0 ADC Mux Selection Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TEMPADCPNP0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TEMPADCPNP0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	TEMPADCPNP0	TEMPADCPNP0	HW automatically switches the AUXADC mux with this value for PNP 0.

1100B04C TEMPADCPNP1 ADC Mux Selection Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TEMPADCPNP1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TEMPADCPNP1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	TEMPADCPNP1	TEMPADCPNP1	HW automatically switches the AUXADC mux with this value for PNP 1.

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1100B050 **TEMPADCPNP2** **ADC Mux Selection Value** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TEMPADCPNP2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TEMPADCPNP2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	TEMPADCPNP2	TEMPADCPNP2	HW automatically switches the AUXADC mux with this value for PNP 2.

1100B054 **TEMPADCMUX** **ADC Mux Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADC_MUX[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_MUX[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	ADC_MUX	ADC_MUX	

1100B058 **TEMPADCEXT** **ADC Extra Write** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADC_EXT[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_EXT[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	ADC_EXT	ADC_EXT	

1100B05C **TEMPADCEXT1** **ADC Extra Write 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADC_EXT1[31:16]															

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Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ADC_EXT1[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ADC_EXT1**	ADC_EXT1	

1100B060 **TEMPADCEN** **ADC Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**ADC_EN[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ADC_EN[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ADC_EN**	ADC_EN	**AHB value for AUXADC enabling**

1100B064 **TEMPPNPMUXADDR** **PNP Mux Selection Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**ADC_PNP_MUX_ADDR[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ADC_PNP_MUX_ADDR[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ADC_PNP_MUX_ADDR**	ADC_PNP_MUX_ADDR	

1100B068 **TEMPADCMUXADDR** **ADC Mux Selection Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**ADC_MUX_ADDR[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ADC_MUX_ADDR[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31:0	**ADC_MUX_ADDR**	ADC_MUX_ADDR	

1100B06C **TEMPADCEXTADDR** **ADC Extra Write Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADC_EXT_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_EXT_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ADC_EXT_ADDR**	ADC_EXT_ADDR	

1100B070 **TEMPADCEXT1ADDR** **ADC Extra Write Address 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADC_EXT1_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_EXT1_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ADC_EXT1_ADDR**	ADC_EXT1_ADDR	

1100B074 **TEMPADCENADDR** **ADC Enable Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADC_EN_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_EN_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ADC_EN_ADDR**	ADC_EN_ADDR	AHB address for AUXADC enabling

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1100B078 TEMPADCVALIDADDR ADC Voltage Valid Reading Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADC_VALID_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_VALID_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	ADC_VALID_ADDR	ADC_VALID_ADDR	AHB address for AUXADC valid bit

1100B07C TEMPADCVOLTADDR ADC Voltage Reading Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADC_VOLT_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_VOLT_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	ADC_VOLT_ADDR	ADC_VOLT_ADDR	AHB address for AUXADC voltage output

1100B080 TEMPRDCTRL ADC Voltage Read Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RD_CTRL_DIFF
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0		RD_CTRL_DIFF	0: Read valid and voltage are in the same register. 1: Read valid and voltage are in different registers.

1100B084 TEMPADCVALIDMASK ADC Valid Mask 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											ADC_RD_VALID_POLARITY	ADC_RD_VALID_POS				
Type											RW	RW				
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5		ADC_RD_VALID_POLARITY	0: Valid bit is active low. 1: Valid bit is active high.
4:0	**ADC_RD_VALID_POS**	ADC_RD_VALID_POS	Indicates where the valid bit is in a register

1100B088 TEMPADCVOLTAGESHIFT ADC Voltage Shift 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												ADC_VOLTAGE_SHIFT				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		ADC_VOLTAGE_SHIFT	

1100B08C TEMPADCWRITECTRL ADC Write Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													ADC_EXTRA1_WRITE	ADC_EXTRA_WRITE	ADC_MUX_WRITE	ADC_PNP_WRITE
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3		ADC_EXTRA1_WRITE	Enables adc_extra1_write address

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Bit(s)	Mnemonic	Name	Description
2	**ADC_EXTRA_WRITE**	ADC_EXTRA_WRITE	Enables adc_extra_write address
1	**ADC_MUX_WRITE**	ADC_MUX_WRITE	Enables adc_mux_write address
0	**ADC_PNP_WRITE**	ADC_PNP_WRITE	Enables adc_pnp_write address

1100B090 TEMPMSR0 Temperature Measure Reading 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSRVALID0				MSRREADING0											
Type	RC				RU											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**MSRVALID0**	MSRVALID0	
11:0		MSRREADING0	

1100B094 TEMPMSR1 Temperature Measure Reading 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSRVALID1				MSRREADING1											
Type	RC				RU											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15		MSRVALID1	
11:0		MSRREADING1	

1100B098 TEMPMSR2 Temperature Measure Reading 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSRVALI				MSRREADING2											

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	D2															
Type	RC				RU											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15		MSRVALID2	
11:0		MSRREADING2	

1100B0A0 TEMPIMMD0 Temperature IMMD Measure Reading 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IMMDMSRVALID0				IMMDMSRREADING0											
Type	RC				RU											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15		IMMDMSRVALID0	
11:0		IMMDMSRREADING0	

1100B0A4 TEMPIMMD1 Temperature IMMD Measure Reading 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IMMDMSRVALID1				IMMDMSRREADING1											
Type	RC				RU											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15		IMMDMSRVALID1	
11:0		IMMDMSRREADING1	

1100B0A8 TEMPIMMD2 Temperature IMMD Measure Reading 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	IMMDMSRVALID2				IMMDMSRREADING2											
Type	RC				RU											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15		IMMDMSRVALID2	
11:0		IMMDMSRREADING2	

1100B0B0 **TEMPMONIDET3** **Sensing Point 3 Temperature Monitoring Detection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							NOHOTIMES		HOTIMES		LOTIMES		HTIMES		CTIMES	
Type							RW		RW		RW		RW		RW	
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
9:8		NOHOTIMES	**Times of hot to normal interrupt occurrence** 00: 1 01: 2 10: 3 11: 4 00: 1 01: 2 10: 3 11: 4
7:6	**HOTIMES**	HOTIMES	**Times of high offset interrupt occurrence** 00: 1 01: 2 10: 3 11: 4 00: 1 01: 2 10: 3 11: 4
5:4	**LOTIMES**	LOTIMES	**Times of low offset interrupt occurrence** 00: 1 01: 2 10: 3 11: 4 00: 1 01: 2 10: 3 11: 4
3:2	**HTIMES**	HTIMES	**Times of hot threshold interrupt occurrence** 00: 1 01: 2 10: 3 11: 4

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Bit(s)	Mnemonic	Name	Description
			00: 1 01: 2 10: 3 11: 4
1:0	CTIMES	CTIMES	**Times of cold threshold interrupt occurrence** 00: 1 01: 2 10: 3 11: 4 00: 1 01: 2 10: 3 11: 4

1100B0B4 TEMPADCPNP3 ADC Mux Selection Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TEMPADCPNP3[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TEMPADCPNP3[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	TEMPADCPNP3	TEMPADCPNP3	HW automatically switches the AUXADC mux with this value for PNP 3.

1100B0B8 TEMPMSR3 Temperature Measure Reading 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSRVALID3				MSRREADING3											
Type	RC				RU											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15		MSRVALID3	
11:0		MSRREADING3	

1100B0BC TEMPIMMD3 Temperature IMMD Measure Reading 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IMMDMSRVALID3				IMMDMSRREADING3											
Type	RC				RU											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15		IMMDMSRVALID3	
11:0		IMMDMSRREADING3	

1100B0C0 **TEMPPROTCTL** **Thermal Protection Sensor Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													PROTSELECTION		PROTSTRATEGY	
Type													RW		RW	
Reset													0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					PROTOFFSET											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:18		PROTSELECTION	00: Sensor 0 01: Sensor 1 10: Sensor 2 11: Sensor 3
17:16	**PROTSTRATEGY**	PROTSTRATEGY	00: Average of 4 sensors 01: Maximum of 4 sensors 10: Selected sensor 11: Reserved
11:0	**PROTOFFSET**	PROTOFFSET	

1100B0C4 **TEMPPROTTA** **Temperature Protection STAGE1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					PROTSTAGE1THRES											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0		PROTSTAGE1THRES	

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1100B0C8 TEMPPROTTB Temperature Protection STAGE2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					PROTSTAGE2THRES											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0		PROTSTAGE2THRES	

1100B0CC TEMPPROTTC Temperature Protection STAGE3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					PROTSTAGE2THRES											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0		PROTSTAGE2THRES	

1100B0F0 TEMPSPARE0 Spare Register For Debug 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SPARE0**	SPARE0	Debugging register 0

1100B0F4 TEMPSPARE1 Spare Register For Debug 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31:0	**SPARE1**	SPARE1	Debugging register 1

1100B0F8 TEMPSPARE2 Spare Register For Debug 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SPARE2**	SPARE2	Debugging register 2

1100B0FC TEMPSPARE3 Spare Register For Debug 3 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE3[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE3[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit(s)	Mnemonic	Name	Description
31:0	**SPARE3**	SPARE3	Debugging register 3

1100B400 PTPCORESEL 00070000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														PTPODCORE2EN	PTPODCORE1EN	PTPODCORE0EN
Type														RW	RW	RW
Reset														1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													APBSEL			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
18	**PTPODCORE2EN**	PTPODCORE2EN	**Enables PTPOD CORE 2** 0: Disable 1: Enable
17	**PTPODCORE1EN**	PTPODCORE1EN	**Enables PTPOD CORE 1** 0: Disable

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Bit(s)	Mnemonic	Name	Description
			1: Enable
16	**PTPODCOREoEN**	PTPODCOREoEN	**Enables PTPOD CORE o** o: Disable 1: Enable
3:0	**APBSEL**	APBSEL	

1100B404 THERMINTST 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESERVE[28:13]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESERVE[12:0]													THERMINT2	THERMINT1	THERMINT0
Type	RO													RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:3	**RESERVE**	RESERVE	**Reserved**
2	**THERMINT2**	THERMINT2	
1	**THERMINT1**	THERMINT1	**Selects Core N APB** N = APBSEL
0	**THERMINT0**	THERMINT0	

1100B408 PTPODINTST 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESERVE[28:13]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESERVE[12:0]													PTPODINT2	PTPODINT1	PTPODINT0
Type	RO													RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:3	**RESERVE**	RESERVE	Reserved
2	**PTPODINT2**	PTPODINT2	
1	**PTPODINT1**	PTPODINT1	
0	**PTPODINT0**	PTPODINT0	

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1100B40C THSTAGE0ST **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														THST0C2	THST0C1	THST0C0
Type														RU	RU	RU
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2	**THST0C2**	THST0C2	
1	**THST0C1**	THST0C1	
0	**THST0C0**	THST0C0	

1100B410 THSTAGE1ST **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														THST1C2	THST1C1	THST1C0
Type														RU	RU	RU
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2	**THST1C2**	THST1C2	
1	**THST1C1**	THST1C1	
0	**THST1C0**	THST1C0	

1100B414 THSTAGE2ST **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														THST2C2	THST2C1	THST2C0
Type														RU	RU	RU
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2	**THST2C2**	THST2C2	
1	**THST2C1**	THST2C1	
0	**THST2C0**	THST2C0	

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1100B418 THAHBST0 00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																AHBVALID
Type																RU
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														AHBGNT0ON2	AHBGNT0ON1	AHBGNT0ON0
Type														RU	RU	RU
Reset														1	0	0

Bit(s)	Mnemonic	Name	Description
16	**AHBVALID**	AHBVALID	
2	**AHBGNT0ON2**	AHBGNT0ON2	
1	**AHBGNT0ON1**	AHBGNT0ON1	
0	**AHBGNT0ON0**	AHBGNT0ON0	

1100B41C THAHBST1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														AHBGNT1ON2	AHBGNT1ON1	AHBGNT1ON0
Type														RU	RU	RU
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2	**AHBGNT1ON2**	AHBGNT1ON2	
1	**AHBGNT1ON1**	AHBGNT1ON1	
0	**AHBGNT1ON0**	AHBGNT1ON0	

1100B420 PTPSPARE0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PTPSPARE0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PTPSPARE0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31:0	**PTPSPARE 0**	PTPSPARE0	PTPOD debugging register 0

1100B424 PTPSPARE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PTPSPARE1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PTPSPARE1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**PTPSPARE 1**	PTPSPARE1	PTPOD debugging register 1

1100B428 PTPSPARE2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PTPSPARE2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PTPSPARE2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**PTPSPARE 2**	PTPSPARE2	PTPOD debugging register 2

1100B42C PTPSPARE3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PTPSPARE3[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PTPSPARE3[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**PTPSPARE 3**	PTPSPARE3	PTPOD debugging register 3

1100B430 THSLPEVEB 00000007

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														THEVBC2	THEVBC1	THEVBC0
Type														RU	RU	RU
Reset														1	1	1

Bit(s)	Mnemonic	Name	Description
2	**THEVBC2**	THEVBC2	
1	**THEVBC1**	THEVBC1	
0	**THEVBC0**	THEVBC0	

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5.14 IRTX

5.14.1 Introduction

IRTX module provides the “Consumer IR” feature. According to Wikipedia, *“Consumer IR, consumer infrared, or CIR, refers to a wide variety of devices employing the infrared electromagnetic spectrum for wireless communications. Most commonly found in television remote controls, infrared ports are equally ubiquitous in consumer electronics, such as PDAs, laptops, and computers. The functionality of CIR is as broad as the consumer electronics that carry it. For instance, a television remote control can convey a "channel up" command to the television, while a computer might be able to surf the internet solely via CIR. The type, speed, bandwidth, and power of the transmitted information depends on the particular CIR protocol employed.”*

MediaTek’s IRTX provides three main stream CIR protocols: NEC, RC5 and RC6. It also supports Android IR API in which the OS version is above KitKat.

5.14.2 NEC Protocol

5.14.2.1 Introduction

The NEC protocol uses pulse distance encoding of the bits. Each pulse is a 560µs long 38kHz carrier burst (about 21 cycles). A logical "1" takes 2.25ms to transmit, while a logical "0" takes only half of that, i.e. 1.125ms, as shown in Figure 5-26. The recommended carrier duty-cycle is 1/4 or 1/3.

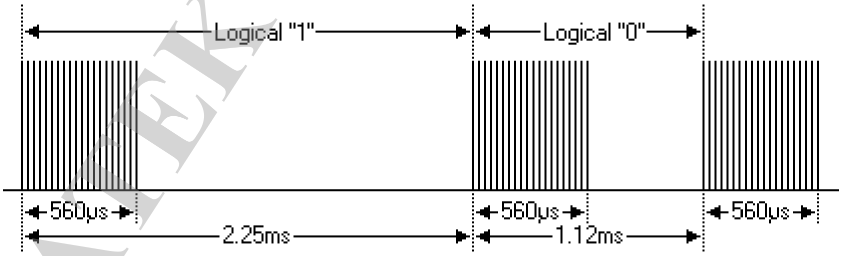

Figure 5-26. Logic representation for NEC protocol

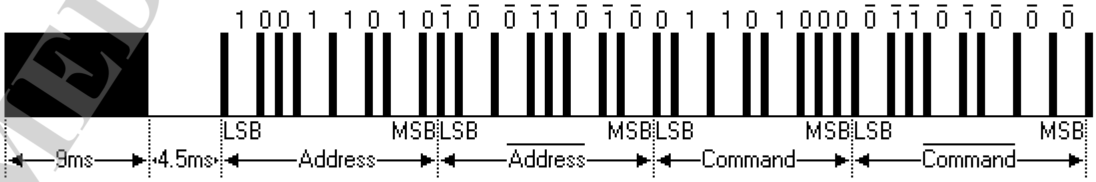

Figure 5-27. Pulse train in transmission of NEC protocol

The picture above shows the typical pulse train of the NEC protocol. With this protocol, the LSB is transmitted first. In this case Address $59 and Command $16 is transmitted. A message is started by a

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9ms AGC burst, which is used to set up the gain of the earlier IR receivers. This AGC burst is then followed by a 4.5ms space, which is then followed by the Address and Command. Address and Command are transmitted twice. In the second time, all bits are inverted and can be used for verification of the received message. The total transmission time is constant because every bit is repeated with its inverted length.

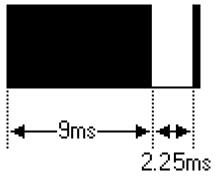

Figure 5-28. A message is started by a 9ms AGC burst

A command is transmitted only once even when the key on the remote control remains pressed. Every 110ms a repeat code is transmitted for as long as the key remains down. This repeated code is simply a 9ms AGC pulse followed by a 2.25ms space and a 560µs burst.

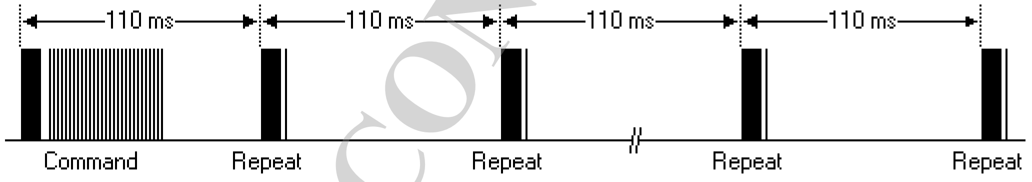

Figure 5-29. A repeat code is transmitted every 110ms

5.14.2.2 Features

- 8-bit address and 8-bit command length
- Address and command are transmitted twice for reliability.
- Pulse distance modulation
- 38kHz carrier frequency
- 1.125ms or 2.25ms bit time

5.14.3 Philips RC-5 Protocol

5.14.3.1 Introduction

The protocol uses bi-phase modulation (or so-called Manchester coding) of a 36kHz IR carrier frequency. All bits are of equal length to 1.778ms in this protocol, with half of the bit time filled with a burst of the 36kHz carrier and the other half being idle. A logical zero is represented by a burst in the first half of the bit time. A logical one is represented by a burst in the second half of the bit time. The pulse/pause ratio of the 36kHz carrier frequency is 1/3 or 1/4 to reduce power consumption.

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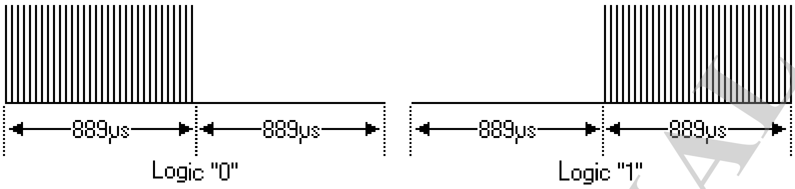

Figure 5-30. Coding method for RC5 protocol

5.14.3.2 Features

- 5-bit address and 6-bit command length (7 command bits for RC5X)
- Bi-phase coding (aka Manchester coding)
- 36kHz carrier frequency
- 1.778ms constant bit time (64 cycles of 36 kHz)
- Manufacturer Philips

5.14.4 Philips RC-6 Protocol

5.14.4.1 Introduction

RC-6 is the successor of the RC-5 protocol. Like RC-5 the new RC-6 protocol is also defined by Philips. It is a very versatile and well defined protocol. Because of this versatility its original definition is many pages long. Here we only summarize the most important properties of this protocol. RC-6 signals are modulated on a 36kHz Infra Red carrier. The duty cycle of this carrier has to be between 25% and 50%.

Data are modulated using Manchester coding; this means that each bit (or symbol) has both a mark and space in the output signal. If the symbol is a "1", the first half of the bit time will be a mark and the second half a space. If the symbol is a "0", the first half of the bit time will be a space and the second half a mark.

The main timing unit is 1t, which is 16 times the carrier period (1/36k*16 = 444µs). With RC-6, total different symbols are defined:

- The leader pulse has a 6t mark time (2.666ms) and 2t space time (0.889ms). This leader pulse is normally used to set up the gain of the IR receiver unit.

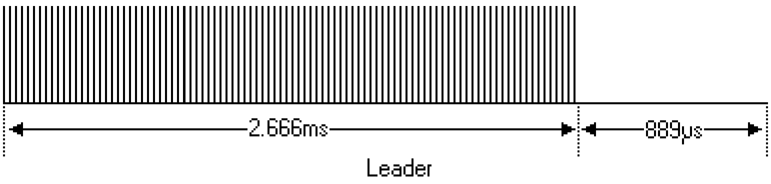

Figure 5-31. Lead pulse in RC6 protocol

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- Normal bits have 1t mark time (0.444ms) and 1t space time (0.444ms). "0" and "1" are encoded by the position of the mark and space in the bit time.

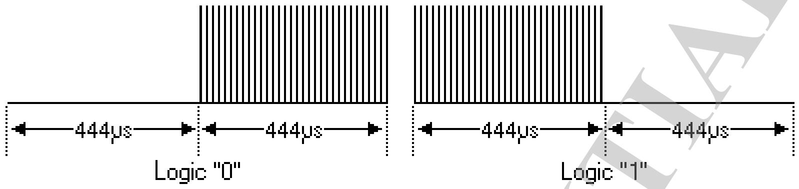

Figure 5-32. Coding method for RC6 protocol

- Trailer bits have 2t mark time (0.889ms) and 2t space time (0.889ms). "0" and "1" are encoded by the position of the mark and space in the bit time.

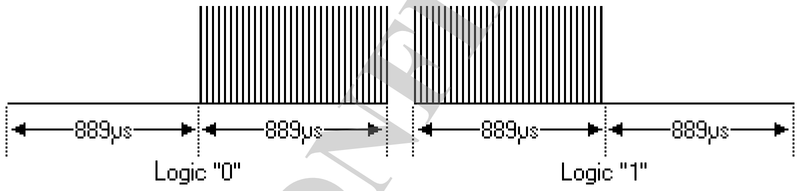

Figure 5-33. Trailer pulse in RC6 protocol

The leader and trailer symbols are only used in the header field of the messages.

5.14.4.2 Features

- Different modes of operation, depending on the intended use
- Dedicated Philips modes and OEM modes
- Variable command length, depending on the operation mode
- Bi-phase coding (aka Manchester coding)
- 35kHz carrier frequency
- Manufacturer Philips

5.14.5 Register Definition

Module name: irtx Base address: (+11011000h)

Address	Name	Width	Register Function
11011000	IRTXCFG	32	IRTX Configuration Register
11011004	IRTXD0	32	IRTX Transmission Data 0 Register
11011008	IRTXD1	32	IRTX Transmission Data 1 Register
1101100C	IRTXD2	32	IRTX Transmission Data 2 Register
11011010	IRTX_L0H	32	IRTX Logic 0 High Period Register
11011014	IRTX_L0L	32	IRTX Logic 0 Low Period Register

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Address	Name	Width	Register Function
11011018	**IRTX_L1H**	32	IRTX Logic 1 High Period Register
1101101C	**IRTX_L1L**	32	IRTX Logic 1 Low Period Register
11011020	**IRTXSYNCH**	32	IRTX Sync High Period Register
11011024	**IRTXSYNCL**	32	IRTX Sync Low Period Register
11011028	**IRTXMT**	32	IRTX Modulation Parameter Register

11011000 IRTXCFG IRTX Configuration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_INV	IRTX_BITNUM							IRTX_IRINV	IRTX_IROS	IRTX_RODR	IRTX_BODR	IRTX_SWO	IRTX_MODE		IRTX_STRT
Type	RW	RW							RW	RW	RW	RW	RW	RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15		DATA_INV	**IR N inverter** Set this bit to 1 to invert the IR data waveform only.
14:8		IRTX_BITNUM	**Bit number** Number of IR bits to be transmitted
7		IRTX_IRINV	**IR inverter** Set this bit to 1 to invert IR output.
6		IRTX_IROS	**Selects IR output** 0: IR output is IRTX baseband signal. 1: IR output is IRTX modulated signal.
5		IRTX_RODR	**Register transmission order** 0: IRTX_R0 first, IRTX_R11 last (R0, R1 ~ R11) 1: IRTX_R11 first, IRTX_R0 last (R11, R10 ~R0)
4		IRTX_BODR	**Bit transmission order** 0: MSB first, LSB last (ex. R0[7], R0[6] ~ R0[0]) 1: LSB first, MSB last (ex. R0[0], R0[1] ~ R0[7])
3		IRTX_SWO	**Software output bit** When the IRTX output protocol is set to software mode, the IR output will be the same as SWO.
2:1		IRTX_MODE	**IR output protocol** 0: Pulse-width coded protocol 1: RC5 protocol 2: RC6 protocol 3: Software mode
0		IRTX_STRT	**IR trigger bit** 0: IR code transfer completed 1: Start to transfer IR code When IRTX output protocol is set to software mode, this bit will be set as 0 to terminate IR transmission.

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11011004 IRTXD0 IRTX Transmission Data 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRTX_R3								IRTX_R2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_R1								IRTX_R0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		IRTX_R3	IRTX byte 3
23:16		IRTX_R2	IRTX byte 2
15:8		IRTX_R1	IRTX byte 1
7:0		IRTX_R0	IRTX byte 0

11011008 IRTXD1 IRTX Transmission Data 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRTX_R7								IRTX_R6							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_R5								IRTX_R4							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		IRTX_R7	IRTX byte 7
23:16		IRTX_R6	IRTX byte 6
15:8		IRTX_R5	IRTX byte 5
7:0		IRTX_R4	IRTX byte 4

1101100C IRTXD2 IRTX Transmission Data 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRTX_R11								IRTX_R10							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_R9								IRTX_R8							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		IRTX_R11	IRTX byte 11
23:16		IRTX_R10	IRTX byte 10
15:8		IRTX_R9	IRTX byte 9
7:0		IRTX_R8	IRTX byte 8

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11011010 **IRTX_L0H** **IRTX Logic 0 High Period Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									IRTX_L0H[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_L0H[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		IRTX_L0H	**Logic 0 pulse high period** The period is equal to L0H/27MHz. This register is also valid in RC5/RC6 protocol. RC5 T = 24000, so T = 24000/27MHz = 0.889ms

11011014 **IRTX_L0L** **IRTX Logic 0 Low Period Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									IRTX_L0L[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_L0L[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		IRTX_L0L	**Logic 0 pulse low period** The period is equal to L0L/27MHz. When in SWO, bit[2:0] indicates which PWM channel is selected.

11011018 **IRTX_L1H** **IRTX Logic 1 High Period Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									IRTX_L1H[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_L1H[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		IRTX_L1H	**Logic 1 pulse high period** The period is equal to L1H/27MHz.

1101101C **IRTX_L1L** **IRTX Logic 1 Low Period Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name									IRTX_L1L[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_L1L[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		IRTX_L1L	**Logic 1 pulse low period** The period is equal to L1L/27MHz.

11011020 IRTXSYNCH IRTX Sync High Period Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									IRTX_SYNCH[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_SYNCH[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		IRTX_SYNCH	**SYNCH leading pulse high period** The period is equal to SYNCH/27MHz. SYNCH will be ignored if RC5/RC6 protocol is adopted.

11011024 IRTXSYNCL IRTX Sync Low Period Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									IRTX_SYNCL[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_SYNCL[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		IRTX_SYNCL	**SYNCL leading pulse low period** The period is equal to SYNCL/27MHz. SYNCL will be ignored if RC5/RC6 protocol is adopted.

11011028 IRTXMT IRTX Modulation Parameter Register 00E602B2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRTX_CDT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	1	1	0	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_CWT															
Type	RW															

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Reset	0	0	0	0	0	0	1	0	1	0	1	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
31:16		IRTX_CDT	**Carrier waveform duty time** Duty cycle = CDT/CWT Default duty cycle = 230/690 =33%
15:0		IRTX_CWT	**Carrier waveform period**

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5.15 IrDA

5.15.1 Introduction

IrDA framer, which is shown in Figure 5-34, is implemented to reduce the CPU loading for IrDA transmission. The IrDA framer functional block can be divided into two parts: (1) the transmitting part and (2) the receiving part. The transmitter part performs BOFs addition, byte stuffing, the addition of 16-bits FCS, and EOF appendence. The receiving part executes BOFs removal, ESC character removal, CRC checking, and EOF detection. In addition, the framer will perform 3/16 modulation and demodulation to connect to the IR transceiver. The transmitter and receiver need the DMA channel.

5.15.2 Features

- The IrDA framer supports IrDA SIR, MIR and FIR modes of operation.
- SIR mode includes operation from 9600bps ~ 115200bps.
- MIR includes operation at 567000bps or 1152000bps
- FIR mode includes operation at 4Mbps.

5.15.3 Block Diagram

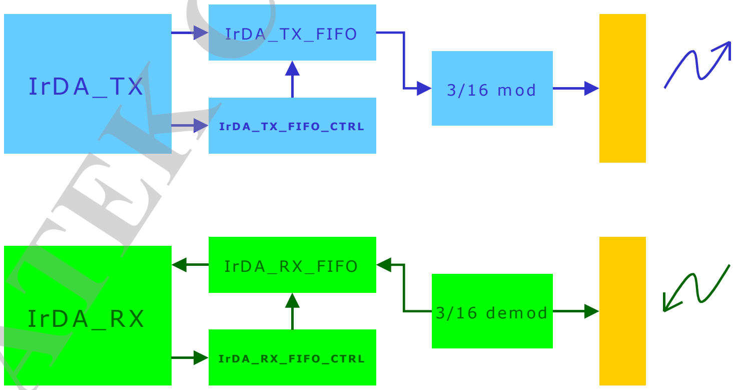

Figure 5-34. Block diagram of IrDA

5.15.4 Register Definition

Module name: irda_framer Base address: (+11010000h)

Address	Name	Width	Register Function
11010000	**BUF**	16	Tx BUF and Rx BUF
11010004	**BUF_CLEAR**	16	Tx BUF and Rx BUF Clear Signal
11010008	**MAX_T**	16	Max. Turn-around Time
1101000C	**MIN_T**	16	Min. Turn-around Time
11010010	**BOFS**	16	Number of Additional BOFs Prefixed to the Beginning of a Frame

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Address	Name	Width	Register Function
11010014	DIV	16	Baud Rate Divisor
11010018	TX_FRAME_SIZE	16	Transmit Frame Size
1101001C	RX_FRAME1_SIZE	16	Receiving Frame 1 Size
11010020	ABORT	16	Transmit Abort Indication
11010024	TX_EN	16	IrDA Framer Transmit Enable Signal
11010028	RX_EN	16	IrDA Framer Receive Enable Signal
1101002C	TRIGGER	16	FIFO Trigger Level Indication
11010030	IRQ_ENABLE	16	IRQ Enabling Signal
11010034	IRQ_STA	16	Interrupt Status
11010038	ERR_STATUS	16	Error Status Register
1101003C	TRANSCEIVER_PDN	16	**Transceiver Power On/Off Control** Selects transceiver mode
11010040	RX_FRAME_MAX	16	Max. Number of Receiving Frame Size
11010044	THRESH_T	16	Threshold Time
11010048	COUNT_ENABLE	16	Counter Enabling Signal
1101004C	CLOCK_RATE	16	Indication of System Clock Rate
11010050	RATE_FIX	16	System Clock Rate Fix
11010054	FRAME1_STATUS	16	Rx Frame 1 Status
11010058	FRAME2_STATUS	16	Rx Frame 2 Status
1101005C	RX_FRAME2_SIZE	16	Receiving Frame 2 Size
11010060	IRDA_MODE	16	IrDA Mode Selection
11010064	FIFO_STAT	16	**FIFO Status** Indicates the real-time FIFO status, for monitoring purposes.
11010068	IRDA_FIR_DIV	16	Generate FIR Sampling clk

11010000 BUF Tx BUF and Rx BUF 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BUF							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	BUF	BUF	IrDA framer transmit or receive data

11010004 BUF_CLEAR Tx BUF and Rx BUF Clear Signal 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CLEAR
Type																RO
Reset																0

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Bit(s)	Mnemonic	Name	Description
0	**CLEAR**	CLEAR	**SIR mode only** When CLEAR = 1, both Tx and Rx FIFO will be cleared. Used primarily for debugging. Normal operation does not require this. This control signal can only be issued in SIR mode.

11010008 **MAX_T** **Max. Turn-around Time** **3E80**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			MAX_T													
Type			RW													
Reset			1	1	1	1	1	0	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
13:0	**MAX_T**	MAX_T	**Max. time a station can hold the P/F bit** This parameter, along with the baud rate parameter, dictates the maximum number of bytes that a station can transmit before passing the line to another station by transmitting a frame with the P/F bit. This parameter is used by one station to indicate the maximum time the other station can send before it must turn the link around. For baud rates less than 115,200kbps, 500ms is the only valid value. Default: 500ms

1101000C **MIN_T** **Min. Turn-around Time** **FDE8**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_T															
Type	RW															
Reset	1	1	1	1	1	1	0	1	1	1	1	0	1	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**MIN_T**	MIN_T	**Min. turn-around time** Default: 10ms. The minimum turnaround time parameter deals with the time needed for a receiver to recover following saturation by transmission from the same device. This parameter corresponds to the required time delay between the last byte of the last frame sent by a station and the point at which it is ready to receive the first byte of a frame from another station, i.e. the latency for a transmit to complete and be ready to receive.

11010010 **BOFS** **Number of Additional BOFs Prefixed to the Beginning of a Frame** **000B**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TYPE	BOFS						
Type									RW	RW						
Reset									0	0	0	0	1	0	1	1

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
7	**TYPE**	TYPE	**SIR mode only. Additional BOFs type** 0: BOF = FFh 1: BOF = C0h
6:0	**BOFS**	BOFS	**For SIR mode: The additional BOFs parameter indicates the number of additional flags needed at the beginning of every frame.** The main purpose for the additional BOFs is to provide a delay at the beginning of each frame for devices with a long interrupt latency. **For MIR mode: This parameter indicates the number of double STA's to transmit in the beginning.** This value should be set to 0 (for default 2 STA's) for MIR mode, unless more are required. **For FIR mode: This parameter has no effect.**

11010014 DIV Baud Rate Divisor 0055

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIV															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
15:0	**DIV**	DIV	**Transmit or receive rate divider** SIR mode: DIV Rate = System clock frequency/DIV/16. The default value is 55h when in contention mode. MIR/FIR mode: DIV Rate = 1. This divisor is also used to determine the RX FIFO timeout threshold.

11010018 TX_FRAME_SIZE Transmit Frame Size 0040

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_FRAME_SIZE											
Type					RW											
Reset					0	0	0	0	0	1	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0	**TX_FRAME_SIZE**	TX_FRAME_SIZE	**Transmit frame size** The default value is 64 when in contention mode.

1101001C RX_FRAME1_SIZE Receiving Frame 1 Size 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_FRAME1_SIZE											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
11:0	**RX_FRAME1_SIZE**	RX_FRAME1_SIZE	**Reports the number of byte received** Includes only the A+C+I fields.

11010020 ABORT Transmit Abort Indication 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ABORT
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**ABORT**	ABORT	**SIR mode only** When set to 1, the framer transmits an abort sequence and closes the frame without an FCS field or an ending flag. *Note: Tx abort can be achieved in MIR and FIR by simply disabling the tx_en signal.*

11010024 TX_EN IrDA Framer Transmit Enable Signal 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TX_ONE	TXINVERT	MODE	TX_EN
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3	**TX_ONE**	TX_ONE	**Controls the transmit enable signal (one or not one)** 0: tx_en is not de-asserted until software programs do so. 1: tx_en is de-asserted (i.e. transmit is disabled) automatically after one frame has been sent.
2	**TXINVERT**	TXINVERT	**Inverts transmit signal** 0: Transmit signal is not inverted. 1: Transmit signal is inverted.
1	**MODE**	MODE	**SIR mode only. Selects modulation type** 0: 3/16 modulation 1: 1.61us
0	**TX_EN**	TX_EN	**Enables transmission**

11010028 RX_EN IrDA Framer Receive Enable Signal 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RX_ONE	RXINVERT	RX_EN
Type														RW	RW	RW
Reset														0	0	0

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Bit(s)	Mnemonic	Name	Description
2	**RX_ONE**	RX_ONE	**Disables receiving when one frame is acquired** 0: rx_en is not de-asserted until software programs do so. 1: rx_en is de-asserted (i.e. transmit disabled) automatically after one frame has been sent.
1	**RXINVERT**	RXINVERT	**Inverts the received signal** 0: Received signal is not inverted. 1: Received signal is inverted.
0	**RX_EN**	RX_EN	**Enables receiving**

11010002C **TRIGGER** **FIFO Trigger Level Indication** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RX_TRIG		TX_TRIG	
Type													RW		RW	
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:2	**RX_TRIG**	RX_TRIG	**Rx FIFO interrupt trigger threshold** When the amount of data in Rx FIFO is above the specified amount, DMA req is asserted. 0: 1 byte 1: 2 bytes 2: 3 bytes
1:0	**TX_TRIG**	TX_TRIG	**Tx FIFO interrupt trigger threshold** When the amount of data in the Tx FIFO is less than the specified amount, DMA req is asserted. (When TX_TRIG = 03, DMA req is always asserted as long as FIFO is not full.) 0: 0 byte 1: 1 byte 2: 8 bytes 3: 16 bytes

11010030 **IRQ_ENABLE** **IRQ Enabling Signal** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				2NDRX_COMP	RXRESTART	THRESHTIMEOUT	FIFOTIMEOUT	TXABORT	RXABORT	MAXTIMEOUT	MINTIMEOUT	RXCOMPLETE	TXCOMPLETE	ERROR	RXTHRES	TXTHRES
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12	**2NDRX_COMP**	_2NDRX_COMP	**Receives second frame and gets P/F bit** 0: No interrupt is generated 1: Interrupt is generated when receiving second frame and P/F bit is completely obtained.
11	**RXRESTART**	RXRESTART	**SIR mode only. Receives a new frame before one frame is received completely** 0: No interrupt is generated. 1: Interrupt is generated when receiving a new frame and before one

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Bit(s)	Mnemonic	Name	Description
			frame has been completely received.
10	**THRESHTIMEOUT**	THRESHTIMEOUT	**Threshold time time-out** 0: No interrupt is generated. 1: Interrupt is generated when the threshold timer is timed out.
9	**FIFOTIMEOUT**	FIFOTIMEOUT	**FIFO time-out** 0: No interrupt is generated. 1: Interrupt is generated upon FIFO time-out.
8	**TXABORT**	TXABORT	**SIR mode only. Transmits aborting frame** 0: No interrupt is generated. 1: Interrupt is generated when transmitting an aborting frame.
7	**RXABORT**	RXABORT	**Receives aborting frame** 0: No interrupt is generated. 1: Interrupt is generated when receiving an aborting frame.
6	**MAXTIMEOUT**	MAXTIMEOUT	**Max. time time-out** 0: No interrupt is generated. 1: Interrupt is generated when the maximum timer is timed out.
5	**MINTIMEOUT**	MINTIMEOUT	**Min, time time-out.** 0: No interrupt is generated. 1: Interrupt is generated when the minimum timer is timed out.
4	**RXCOMPLETE**	RXCOMPLETE	**Receives one frame completely** 0: No interrupt is generated. 1: Interrupt is generated when one frame is completely received.
3	**TXCOMPLETE**	TXCOMPLETE	**Transmits one frame completely** 0: No interrupt is generated. 1: Interrupt is generated when one frame has been completely transmitted.
2	**ERROR**	ERROR	**Enables error status interrupt** 0: No interrupt is generated. 1: Interrupt is generated when an error status occurs.
1	**RXTHRES**	RXTHRES	**Received data reach the threshold level** For debugging only. Should be set to 0. 0: No interrupt is generated. 1: Interrupt is generated when receive FIFO size reaches its threshold.
0	**TXTHRES**	TXTHRES	**Transmitted data reach the threshold level** For debugging only. Should be set to 0. 0: No interrupt is generated. 1: Interrupt is generated when transmit FIFO size reaches it threshold.

11010034 **IRQ_STA** **Interrupt Status** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				2ND RX_COMP	RXREST ART	THRESHTIMEOUT	FIFOTIMEOUT	TXABORT	RXABORT	MAXTIMEOUT	MINTIMEOUT	RXCOMPLETE	TXCOMPLETE	ERROR	RXTHRES	TXTHRES
Type				RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12	**2NDRX_**	_2NDRX_COMP	**Receives second frame and completely obtains the P/F bit**

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Bit(s)	Mnemonic	Name	Description
	COMP		
11	**RXRESTART**	RXRESTART	**Receives a new frame before one frame is completely received**
10	**THRESHTIMEOUT**	THRESHTIMEOUT	**Threshold time time-out**
9	**FIFOTIMEOUT**	FIFOTIMEOUT	**FIFO time-out has occurred**
8	**TXABORT**	TXABORT	**Transmits an aborting frame**
7	**RXABORT**	RXABORT	**Receives an aborting frame**
6	**MAXTIMEOUT**	MAXTIMEOUT	**Max. turn-around time time-out**
5	**MINTIMEOUT**	MINTIMEOUT	**Min. turn-around time time-out**
4	**RXCOMPLETE**	RXCOMPLETE	**One frame completely received**
3	**TXCOMPLETE**	TXCOMPLETE	**One frame completely transmitted**
2	**ERROR**	ERROR	**Generated when any of status in error status register occurs** Once the source of an interrupt is determined to be caused by an error (bit 2), the error status register should be read. Once read, both the error status register and the interrupt source are read-cleared. If the error status register indicates either a frame 1 or frame 2 error, the corresponding frame status register should be read.
1	**RXTHRES**	RXTHRES	**Receives when FIFO reaches threshold** For debugging only. Not recommended for normal usage.
0	**TXTHRES**	TXTHRES	**Transmits when FIFO reaches threshold** For debugging only. Not recommended for normal usage.

11010038 **ERR_STATUS** **Error Status Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										TXFIFOUNDERRUN	FRAME2DATAERR	FRAME1DATAERR	RESERVED2	RESERVED	OVERRUN	RXSIZE
Type										RC	RC	RC	RC	RC	RC	RC
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6	**TXFIFOUNDERRUN**	TXFIFOUNDERRUN	**MIR and FIR mode only** Tx FIFO under run has occurred. Data transmission is aborted. Software must reset the tx_en signal.
5	**FRAME2DATAERR**	FRAME2DATAERR	**Indicates an error condition occurred in Rx frame 2** Must check the RX frame 2 status.
4	**FRAME1**	FRAME1DATAE	**Indicates an error condition occurred in RX frame 1**

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Bit(s)	Mnemonic	Name	Description
	DATAERR	RR	Must check the RX frame 1 status.
1	OVERRUN	OVERRUN	**Frame overrun**
0	RXSIZE	RXSIZE	**Received frame size error**

1101003C **TRANSCEIVER_PDN** **Transceiver Power On/Off Control Selects transceiver mode** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														TXCVRCONFIG	TXMANUAL	TRANS_PDN
Type														RW	WO	WO
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2	TXCVRCONFIG	TXCVRCONFIG	0: Irda_txd comes from core logic. 1: Irda_txd depends on tx_manual value.
1	TXMANUAL	TXMANUAL	When txcvr config is set to 1, this bit can be used to select the operation mode of the external IrDA transceiver (some transceivers require selection between high speed and low speed operating modes by software programming the desired sequence to transmit through the irda_txd pin)
0	TRANS_PDN	TRANS_PDN	Used for power on/off control for the external IrDA transceiver

11010040 **RX_FRAME_MAX** **Max. Number of Receiving Frame Size** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					MAX_RX_FRAME_SIZE											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0	MAX_RX_FRAME_SIZE	MAX_RX_FRAME_SIZE	**Received frame I field max size** When the actual receiving frame size is larger than the rx_frame_max, RXSIZE will be asserted. The maximum allowed I field size is 2,048.

11010044 **THRESH_T** **Threshold Time** **0BB8**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DISCONNECT_TIME															
Type	RW															
Reset	0	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
15:0	**DISCONNECT_TIME**	DISCONNECT_TIME	**Threshold time** Used to control the time a station waits without receiving a valid frame before disconnecting the link. Associated with this is the time a station waits without receiving a valid frame before sending a status indication to the service user layer.

11010048 **COUNT_ENABLE** **Counter Enabling Signal** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														THRESH_EN	MIN_EN	MAX_EN
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2	**THRESH_EN**	THRESH_EN	Enables threshhold_time_counter to increment
1	**MIN_EN**	MIN_EN	Enables min_turn_around_counter to increment
0	**MAX_EN**	MAX_EN	Enables max_turn_around_counter to increment

1101004C **CLOCK_RATE** **Indication of System Clock Rate** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CLOCK_RATE	
Type															RW	
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1:0	**CLOCK_RATE**	CLOCK_RATE	**SIR mode. Indicates system clock rate** 0: 26MHz 1: 52MHz 2: 13MHz

11010050 **RATE_FIX** **System Clock Rate Fix** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											FIR_RX_SYN_VALUE	MIR_TIMING_TUNE		CRC_REPORT	SIR_FRAMING_SET	RATE_FIX
Type											RW	RW		RW	RW	RW
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5	**FIR_RX_**	FIR_RX_SYN_V	0: Does not adjust the sync value

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Bit(s)	Mnemonic	Name	Description
	SYN_VALUE	ALUE	1: Adjust the sync value
4:3	**MIR_TIMING_TUNE**	MIR_TIMING_TUNE	**MIR mode only. For some transceivers, in MIR 0.576mbps mode, the RX output pulse does not conform to IRDA specification. Therefore, this option is used to detect the RX output from those transceivers correctly.** 0: For transceivers that conform to spec. 1: For transceivers that do not conform to spec, and the RX output pulse is half of that specified. 2: For transceivers that do not conform to spec, and the RX output pulse is quarter of that specified.
2	**CRC_REPORT**	CRC_REPORT	**When set to 1, CRC error is reported via error status register and error interrupt.**
1	**SIR_FRAMING_SET**	SIR_FRAMING_SET	**SIR mode only. Framing error check condition.** 0: Ignore the STOP bit of the last byte of a frame. 1: Check the STOP bit of the last byte of a frame.
0	**RATE_FIX**	RATE_FIX	**SIR mode only. Fix the IrDA framer sample base clock rate as 13MHz.** 0: Clock rate based on clock_rate selection. 1: Clock rate fixed at 13MHz.

11010054 **FRAME1_STATUS** **Rx Frame 1 Status** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										FIR_STO_ERR	FIR_4PPM_ERR	MIR_HDLC_ERR	UNKNOW_ERROR	PF_DETECT	CRC_FAIL	FRAME_ERROR
Type										RC	RC	RC	RC	RC	RC	RC
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6	**FIR_STO_ERR**	FIR_STO_ERR	**FIR mode only. FIR STO sequence error** 0: No error 1: Error
5	**FIR_4PPM_ERR**	FIR_4PPM_ERR	**FIR mode only. FIR 4ppm encoding error** 0: No error 1: Error
4	**MIR_HDLC_ERR**	MIR_HDLC_ERR	**MIR mode only. MIR HDLC encoding error** 0: No error 1: Error
3	**UNKNOW_ERROR**	UNKNOW_ERROR	**SIR mode only** Receiving error data, i.e. escape character is followed by a character that is not an ESC, BOF, or EOF character. 0: Data received correctly 1: Unknown error occurs.
2	**PF_DETECT**	PF_DETECT	**P/F bit detection** 0: Not a P/F bit frame 1: Detected P/F bit in this frame
1	**CRC_FAIL**	CRC_FAIL	**CRC check failure** 0: CRC check is successful. 1: CRC check fails.

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Bit(s)	Mnemonic	Name	Description
0	**FRAME_ERROR**	FRAME_ERROR	**SIR mode only** Framing error, i.e. STOP bit = 0. 0: No framing error 1: Framing error occurs.

11010058 **FRAME2_STATUS** **Rx Frame 2 Status** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										FIR_STO_ERR	FIR_4PPM_ERR	MIR_HDLC_ERR	UNKNOW_ERROR	PF_DETECT	CRC_FAIL	FRAME_ERROR
Type										RC	RC	RC	RC	RC	RC	RC
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6	**FIR_STO_ERR**	FIR_STO_ERR	**FIR mode only. FIR STO sequence error** 0: No error 1: Error
5	**FIR_4PPM_ERR**	FIR_4PPM_ERR	**FIR mode only. FIR 4ppm encoding error** 0: No error 1: Error
4	**MIR_HDLC_ERR**	MIR_HDLC_ERR	**MIR mode only. MIR HDLC encoding error** 0: No error 1: Error
3	**UNKNOW_ERROR**	UNKNOW_ERROR	**SIR mode only** Receiving error data, i.e. escape character is followed by a character that is not an ESC, BOF, or EOF character. 0: Data received correctly 1: Unknown error occurs.
2	**PF_DETECT**	PF_DETECT	**P/F bit detection** 0: Not a P/F bit frame 1: Detected P/F bit in this frame
1	**CRC_FAIL**	CRC_FAIL	**CRC check failure** 0: CRC check is successful. 1: CRC check fails.
0	**FRAME_ERROR**	FRAME_ERROR	**SIR mode only** Framing error, i.e. STOP bit = 0. 0: No framing error 1: Framing error occurs.

1101005C **RX_FRAME2_SIZE** **Receiving Frame 2 Size** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_FRAME2_SIZE											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
11:0	**RX_FRAME2_SIZE**	RX_FRAME2_SIZE	**Reports the number of bytes received** Includes only the A+C+I fields.

11010060 IRDA_MODE IrDA Mode Selection 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												IRDA_TX_DMA_EN	IRDA_RX_DMA_EN	MIR_SPEED	IRDA_MODE	
Type												RW	RW	RW	RW	
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4	**IRDA_TX_DMA_EN**	IRDA_TX_DMA_EN	**New DMA is designed for IrDA** If TX DMA is enabled, also set this register to 1.
3	**IRDA_RX_DMA_EN**	IRDA_RX_DMA_EN	**New DMA is designed for IrDA** If RX DMA is enabled, also set this register to 1.
2	**MIR_SPEED**	MIR_SPEED	**Selects MIR speed** 0: 0.576 Mbps 1: 1.152 Mbps
1:0	**IRDA_MODE**	IRDA_MODE	**Selects IrDA operating mode** *Note: This mode selection cannot be issued while transmitting or receiving.* 0: IR mode 1: MIR mode 2: FIR mode

11010064 FIFO_STAT FIFO Status 0005

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RX_FIFO_HOLD	TX_FIFO_WR_FULL	TX_FIFO_RD_EMPTY	RX_FIFO_WR_FULL	RX_FIFO_RD_EMPTY
Type												RO	RO	RO	RO	RO
Reset												0	0	1	0	1

Bit(s)	Mnemonic	Name	Description
4	**RX_FIFO_HOLD**	RX_FIFO_HOLD	
3	**TX_FIFO_WR_FULL**	TX_FIFO_WR_FULL	
2	**TX_FIFO_RD_EM**	TX_FIFO_RD_EMPTY	

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Bit(s)	Mnemonic	Name	Description
	PTY		
1	RX_FIFO_WR_FULL	RX_FIFO_WR_FULL	
0	RX_FIFO_RD_EMPTY	RX_FIFO_RD_EMPTY	

11010068 **IRDA_FIR_DIV** **Generate FIR Sampling clk** **000C**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIR_DIV							
Type									RW							
Reset									0	0	0	0	1	1	0	0

Bit(s)	Mnemonic	Name	Description
7:0	FIR_DIV	FIR_DIV	**Generates FIR sampling clock** A clock which is a multiple to 8 is needed for FIR. In an earlier design, the clock is 48MHz. In the MT6276, this clock is set to 104MHz. This register has been designed to divide the high speed clock to 8MHz. For example: if the clock is 104MHz, this register shall be set to 12. (104/(12+1) = 8). In the MT6276_E2, this clock is set to 48MHz. If the input clock is 48MHz, this register shall be set to 5. (48/(5+1) = 8)

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5.16 Audio System

5.16.1 Introduction

The audio system provides the audio data exchange ability between AP, internal modem and external components. The interfaces are list as follows:

Master/Slave I2S input interface with SRC x 1
Master I2S output x 2
Master I2S input x 1
Slave PCM interface for internal MODEM x 1
Master/Slave PCM interface with SRC for internal/external MODEM x 1
Proprietary audio interface for MTK PMIC x 1
PCM/I2S merged interface for MTK connectivity IC x 1

5.16.2 Features

- Audio playing
  - Supports 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, and 48kHz sampling rate output
  - Supports playing stereo data
- Audio recording
  - Supports 8, 16, 32, 48kHz sampling rate recording
  - Supports stereo recording
- Speech
  - Supports dual MIC
  - Supports 8/16kHz sampling rate recording
  - Supports side tone filter
  - Master/Slave PCM interface with SRC function
- I2S
  - Supports master/slave input mode
  - Supports master output mode
  - Supports 16/24-bit stereo data
  - Supports 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96, 176.4, and 192kHz sampling rate in master mode
  - Supports EIAJ/I2S format
- PCM/I2S merged interface
  - 4-pin interface for concurrently supporting I2S and PCM
  - PCM supports 8k/16k Hz sampling rate
  - I2S supports 32, 44.1, and 48 kHz sampling rate
- Hardware gain function with higher resolution to enhance the audio quality and flexibility of interconnection
- Flexible interconnection system to make data exchange between interfaces without intervention of CPU

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5.16.3 Block Diagram

The diagram and table below show the flexibility on the interconnection between audio interfaces.

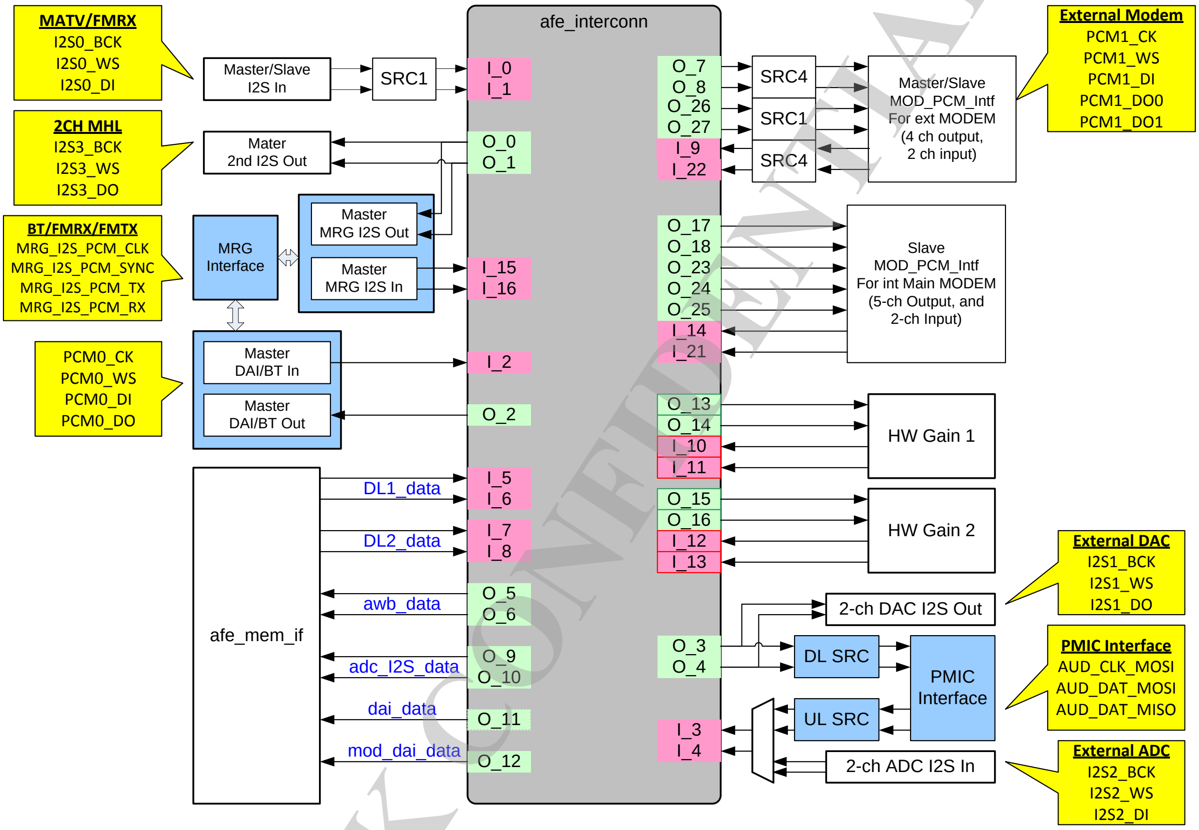

Figure 5-35. Block diagram of audio sys

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Table 5-7. Interface of audio sys

Input	Output	O_00	O_01	O_02	O_03	O_04	O_05	O_06	O_07	O_08	O_09	O_10	O_11	O_12
		I2S_2_LO	I2S_2_RO	DAI_O	DAC_I2S_LO	DAC_I2S_RO	MEM_AWB_LO	MEM_AWB_RO	MOD_DAI_LO	MOD_DAI_RO	MEM_ADC_LO	MEM_ADC_RO	MEM_DAI_O	MEM_MOD_DAI_O
I_00	I2S_I_L	RS	RS	RS	RS	RS	RS	x	S	S	S	S	x	x
I_01	I2S_I_R	RS	RS	RS	RS	RS	x	RS	S	S	S	S	x	x
I_02	DAI_I	S	S	S	S	S	S	x	S	S	x	x	S	x
I_03	ADC_I2S_I_L	S	S	RS	S	S	S	x	S	x	S	x	x	x
I_04	ADC_I2S_I_R	S	S	RS	S	S	x	S	x	S	x	S	x	x
I_05	MEM_DL1_LI	RS	RS	RS	RS	RS	S	x	S	x	S	x	S	x
I_06	MEM_DL1_RI	RS	RS	RS	RS	RS	x	S	x	S	x	S	x	S
I_07	MEM_DL2_LI	RS	RS	RS	RS	RS	S	x	S	x	S	x	S	x
I_08	MEM_DL2_RI	RS	RS	RS	RS	RS	x	S	x	S	x	S	x	S
I_09	MOD_DAI_I	S	S	S	S	S	S	x	x	x	S	x	x	S
I_10	GAIN1_LI	RS	x	RS	RS	x	S	x	S	x	S	S	S	S
I_11	GAIN1_RI	x	RS	RS	x	RS	x	S	x	S	S	S	S	S
I_12	GAIN2_LI	RS	x	RS	RS	x	S	x	S	x	S	S	S	S
I_13	GAIN2_RI	x	RS	RS	x	RS	x	S	x	S	S	S	S	S
I_14	SPCM_I	S	S	S	S	S	S	x	S	S	S	x	x	S
I_15	MRG_I2S_LI	RS	RS	RS	RS	RS	RS	x	x	x	S	x	x	x
I_16	MRG_I2S_RI	RS	RS	RS	RS	RS	x	RS	x	x	x	S	x	x
I_17	ADC2_I2S_I_L	S	x	RS	S	x	S	x	S	x	S	x	S	x
I_18	ADC2_I2S_I_R	x	S	RS	x	S	x	S	x	S	x	S	x	S
~~I_19~~	~~MEM_DL1_2_LI~~	~~RS~~	~~x~~	~~RS~~	~~RS~~	~~RS~~	~~S~~	~~x~~	~~S~~	~~x~~	~~S~~	~~x~~	~~S~~	~~x~~
~~I_20~~	~~MEM_DL1_2_RI~~	~~x~~	~~RS~~	~~RS~~	~~RS~~	~~RS~~	~~x~~	~~S~~	~~x~~	~~S~~	~~x~~	~~S~~	~~x~~	~~S~~
I_21	SPCM2_I	S	S	S	S	S	x	S	S	S	x	S	x	S

Input	Output	O_13	O_14	O_15	O_16	O_17	O_18	~~O_19~~	~~O_20~~	O_21	O_22	O_23	O_24	O_25
		GAIN1_LO	GAIN1_RO	GAIN2_LO	GAIN2_RO	SPCM_LO	SPCM_RO	~~I2S_3_LO~~	~~I2S_3_RO~~	MEM_ADC2_LO	MEM_ADC2_RO	SPCM2_LO	SPCM2_RO	SPCM3_LO
I_00	I2S_I_L	S	S	RS	RS	S	S	~~RS~~	~~RS~~	S	x	S	x	S
I_01	I2S_I_R	S	S	RS	RS	S	S	~~RS~~	~~RS~~	x	S	x	S	x
I_02	DAI_I	S	S	S	S	S	S	~~x~~	~~x~~	x	x	x	x	x
I_03	ADC_I2S_I_L	S	S	S	S	S	x	~~S~~	~~S~~	S	x	S	x	S
I_04	ADC_I2S_I_R	S	S	S	S	x	S	~~S~~	~~S~~	x	S	x	S	x
I_05	MEM_DL1_LI	S	S	S	S	S	x	~~RS~~	~~RS~~	S	x	x	x	x
I_06	MEM_DL1_RI	S	S	S	S	x	S	~~RS~~	~~RS~~	x	S	x	x	x
I_07	MEM_DL2_LI	S	S	S	S	S	x	~~RS~~	~~RS~~	S	x	x	x	x
I_08	MEM_DL2_RI	S	S	S	S	x	S	~~RS~~	~~RS~~	x	S	x	x	x
I_09	MOD_DAI_I	S	S	S	S	S	S	~~S~~	~~S~~	x	x	S	S	S
I_10	GAIN1_LI	x	x	x	x	S	x	~~S~~	~~x~~	S	S	S	x	S
I_11	GAIN1_RI	x	x	x	x	x	S	~~x~~	~~S~~	S	S	x	S	x
I_12	GAIN2_LI	x	x	x	x	S	x	~~S~~	~~x~~	S	S	x	x	x
I_13	GAIN2_RI	x	x	x	x	x	S	~~x~~	~~S~~	S	S	x	x	x
I_14	SPCM_I	S	S	S	S	x	x	~~S~~	~~S~~	x	x	x	x	x
I_15	MRG_I2S_LI	S	S	RS	S	x	x	~~x~~	~~x~~	S	x	x	x	x
I_16	MRG_I2S_RI	S	S	S	RS	x	x	~~x~~	~~x~~	x	S	x	x	x
I_17	ADC2_I2S_I_L	S	S	S	S	S	x	~~S~~	~~S~~	S	x	S	x	S
I_18	ADC2_I2S_I_R	S	S	S	S	x	S	~~S~~	~~S~~	x	S	x	S	x
~~I_19~~	~~MEM_DL1_2_LI~~	~~S~~	~~S~~	~~S~~	~~S~~	~~S~~	~~x~~	~~S~~	~~S~~	~~S~~	~~x~~	~~S~~	~~x~~	~~S~~
~~I_20~~	~~MEM_DL1_2_RI~~	~~S~~	~~S~~	~~S~~	~~S~~	~~x~~	~~S~~	~~S~~	~~S~~	~~x~~	~~S~~	~~x~~	~~S~~	~~x~~
I_21	SPCM2_I	S	S	S	S	x	x	~~S~~	~~S~~	x	x	x	x	x

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5.16.4 Register Definition

Module name: audio_sys_top Base address: (+11220000h)

Address	Name	Width	Register Function
11220000	AUDIO_TOP_CON0	32	**Audio Top Control Register 0** Top configuration for Audiosys. Set the PDN bit to 0 while initializing those blocks. Suggested value: 0x60004000
11220004	AUDIO_TOP_CON1	32	**Audio Top Control Register 1**
1122000C	AUDIO_TOP_CON3	32	**Audio Top Control Register 3**
11220010	AFE_DAC_CON0	32	**AFE Control Register 0** Switch for audio blocks
11220014	AFE_DAC_CON1	32	**AFE Control Register 1** Sets up the operation mode for each block.
11220018	AFE_I2S_CON	32	**AFE I2S Control Register 0** Control register for I2S. Suggested Value: 0x1d
1122001C	AFE_DAIBT_CON0	32	**AFE DAI/BT Control Register 0**
11220020	AFE_CONN0	32	**AFE Connection Register 0** Sets up the operation for interconnection blocks.
11220024	AFE_CONN1	32	**AFE Connection Register 1** Sets up the operation for interconnection blocks.
11220028	AFE_CONN2	32	**AFE Connection Register 2** Sets up the operation for interconnection blocks.
1122002C	AFE_CONN3	32	**AFE Connection Register 3** Sets up the operation for interconnection blocks.
11220030	AFE_CONN4	32	**AFE Connection Register 4**
11220034	AFE_I2S_CON1	32	**AFE I2S Control Register 1** Control register for the 2nd I2S, which is output only. Suggested value: 0x0009.
11220038	AFE_I2S_CON2	32	**AFE I2S Control Register 2** Control register for the 3rd I2S, which is input only. Suggested value: 0x08000009.
1122003C	AFE_MRGIF_CON	32	**AFE Merge Interface Control Register**
11220040	AFE_DL1_BASE	32	**AFE DL1 Base Address Register** Sets up the base address of the DL1 input in master mode.
11220044	AFE_DL1_CUR	32	**AFE DL1 Cursor Register** Indicates the current address of the DL1 input buffer.
11220048	AFE_DL1_END	32	**AFE_DL1_END** Sets up the end address of the DL1 input in master mode.
1122004C	AFE_I2S_CON3	32	**AFE I2S Control Register 3** Control register for the 4th I2S, which is output only. Suggested value: 0x0009.
11220050	AFE_DL2_BASE	32	**AFE DL2 Base Address Register** Sets up the base address of the DL2 input in master mode.
11220054	AFE_DL2_CUR	32	**AFE DL2 Cursor Register** Indicates the current address of the DL2 input buffer.
11220058	AFE_DL2_END	32	**AFE_DL2_END** Sets up the end address of the DL2 input in master mode.
1122005C	AFE_CONN5	32	**AFE Connection Register 5** Sets up the operation for interconnection blocks.

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Address	Name	Width	Register Function
1122006C	AFE_CONN_24BIT	32	**AFE Connection 24-bit Register** Sets up the operation for interconnection blocks.
11220070	AFE_AWB_BASE	32	**AFE AWB Base Address Register** Sets up the base address of the AWB input in master mode.
11220078	AFE_AWB_END	32	**AFE AWB End Address Register** Sets up the end address of the AWB input in master mode.
1122007C	AFE_AWB_CUR	32	**AFE AWB Cursor Register** Indicates the current address of the AWB input buffer.
11220080	AFE_VUL_BASE	32	**AFE VUL Base Address Register** Sets up the base address of the VUL input in master mode.
11220088	AFE_VUL_END	32	**AFE VUL End Address Register** Sets up the end address of the VUL input in master mode.
1122008C	AFE_VUL_CUR	32	**AFE VUL Cursor Register** Indicates the current address of the VUL input buffer.
11220090	AFE_DAI_BASE	32	**AFE DAI Base Address Register** Sets up the base address of the DAI input in master mode.
11220098	AFE_DAI_END	32	**AFE_DAI_END** Sets up the end address of the DAI input in master mode.
1122009C	AFE_DAI_CUR	32	**AFE DAI Cursor Register** Sets up the end address of the DAI input in master mode.
112200BC	AFE_CONN6	32	**AFE Connection Register 6** Sets up the operation for interconnection blocks.
112200CC	AFE_MEMIF_MSB	32	**AFE Memory Interface MSB Register**
112200D0	AFE_MEMIF_MON0	32	**AFE Memory Interface Monitor Register 0** Monitors DL1 memory interface output.
112200D4	AFE_MEMIF_MON1	32	**AFE Memory Interface Monitor Register 1** Monitors DL2 memory interface output.
112200D8	AFE_MEMIF_MON2	32	**AFE Memory Interface Monitor Register 2** Monitors VUL/DAI memory interface input.
112200E0	AFE_MEMIF_MON4	32	**AFE Memory Interface Monitor Register 4** Monitors AWB memory interface input.
11220108	AFE_ADDA_DL_SRC2_CON0	32	AFE_DL_SRC2 Control Register 0
1122010C	AFE_ADDA_DL_SRC2_CON1	32	AFE_DL_SRC2 Control Register 1 Part
11220114	AFE_ADDA_UL_SRC_CON0	32	AFE Uplink SRC Control Register 0 Part
11220118	AFE_ADDA_UL_SRC_CON1	32	AFE Uplink SRC Control Register 1 Part
11220120	AFE_ADDA_TOP_CON0	16	**AFE Top Control Register 0** Control register for loopback test
11220124	AFE_ADDA_UL_DL_CON0	16	Audio UL and DL Control Register 0
1122012C	AFE_ADDA_SRC_DEBUG	32	AFE UL Debug Control
11220130	AFE_ADDA_SRC_DEBUG_MON0	32	AFE Uplink SRC Monitor Register 0
11220134	AFE_ADDA_SRC_DEBUG_MON1	32	AFE Downlink SRC Monitor Register 1
112201D0	AFE_SIDETONE_DEBUG	32	Side-tone Debug
112201D4	AFE_SIDETONE	32	Side-tone Debug Monitor

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Address	Name	Width	Register Function
	_MON		
112201E0	AFE_SIDETONE_CON0	32	Side-tone Control Port 0
112201E4	AFE_SIDETONE_COEFF	32	Side-tone coefficient Port
112201E8	AFE_SIDETONE_CON1	32	Side-tone Control Port 1
112201EC	AFE_SIDETONE_GAIN	32	Side-tone Gain Port
112201F0	AFE_SGEN_CON0	32	AFE Sine-wave Gen Config 0
11220200	AFE_TOP_CON0	32	AFE Top Control Register 0
11220260	AFE_ADDA_PREDIS_CON0	32	AFE Pre-distortion Control Port 0 High Part
11220264	AFE_ADDA_PREDIS_CON1	32	AFE Pre-distortion Control Port 1 High Part
11220270	AFE_MRGIF_MON0	32	AFE Merge Interface Monitor Register 0
11220274	AFE_MRGIF_MON1	32	AFE Merge Interface Monitor Register 1
11220278	AFE_MRGIF_MON2	32	AFE Merge Interface Monitor Register 2
11220330	AFE_MOD_DAI_BASE	32	**AFE MOD_DAI Base Address Register** Sets up the base address of the MOD_DAI input in master mode.
11220338	AFE_MOD_DAI_END	32	**AFE_MOD_DAI_END** Sets up the end address of the MOD_DAI input in master mode.
1122033C	AFE_MOD_DAI_CUR	32	**AFE MOD_DAI Cursor Register** Sets up the end address of the MOD_DAI input in master mode.
112203A0	AFE_IRQ_MCU_CON	32	AFE IRQ MCU Control Register
112203A4	AFE_IRQ_MCU_STATUS	32	AFE IRQ MCU Status Register
112203A8	AFE_IRQ_MCU_CLR	32	AFE IRQ Clear Register
112203AC	AFE_IRQ_MCU_CNT1	32	AFE IRQ1 MCU Counter Register
112203B0	AFE_IRQ_MCU_CNT2	32	AFE IRQ2 MCU Counter Register
112203B4	AFE_IRQ_MCU_EN	32	AFE IRQ MCU Enable Register
112203B8	AFE_IRQ_MCU_MON2	32	**AFE IRQ MCU MON2 Register** Monitors the command for AFE_IRQ_MCU_CLR register.
112203C0	AFE_IRQ1_MCU_CNT_MON	32	AFE IRQ1 MCU Count Monitor Register
112203C4	AFE_IRQ2_MCU_CNT_MON	32	AFE IRQ2 MCU Count Monitor Register
112203C8	AFE_IRQ1_MCU_EN_CNT_MON	32	**AFE IRQ1 MCU Enable Count Monitor Register** Monitors the enable count number of IRQ1.
112203D4	AFE_MEMIF_MAXLEN	32	**AFE Memif Max BLength Register** Defines the maximum burst length.
112203D8	AFE_MEMIF_PBUF_SIZE	32	**AFE MEMIF Prefecth Buffer Size**

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Address	Name	Width	Register Function
112203DC	AFE_IRQ_MCU_CNT7	32	**AFE IRQ7 MCU Counter Register** Sets up the counter for IRQ1. Note: It is suggested not to set the value of AFE_IRQ1_CNT too short (i.e. 1), or the IRQ period may not be as expected due to MCU IRQ processing delay. Remember to set up the desired AFE_IRQ_MCU_CNT1 before IRQ1 is set. Never set AFE_IRQ1_CNT to 0, or there will be no interrupt for IRQ1 after it is set.
112203F0	AFE_APLL1_TUNER_CFG	32	**AFE Tuner Control Register** Setting for APLL frequency tuner
112203F4	AFE_APLL2_TUNER_CFG	32	**AFE Tuner 2 Control Register** Setting for APLL frequency tuner 2
11220410	AFE_GAIN1_CON0	32	**AFE Gain1 Control Register 0** Defines how many samples per step.
11220414	AFE_GAIN1_CON1	32	**AFE Gain1 Control Register 1** Defines the gain1 target.
11220418	AFE_GAIN1_CON2	32	**AFE Gain1 Control Register 2** Defines the gain1 down step.
1122041C	AFE_GAIN1_CON3	32	**AFE Gain1 Control Register 3** Defines the gain1 up step.
11220420	AFE_GAIN1_CONN	32	**AFE Gain1 Connection Register** Sets up the gain1 interconnection blocks.
11220424	AFE_GAIN1_CUR	32	**AFE Gain1 Cursor Register** Indicates the value current GAIN 1.
11220428	AFE_GAIN2_CON0	32	**AFE Gain2 Control Register 0** Defines how many samples per step.
1122042C	AFE_GAIN2_CON1	32	**AFE Gain2 Control Register 1** Defines the GAIN2 target.
11220430	AFE_GAIN2_CON2	32	**AFE Gain2 Control Register 2** Defines the GAIN2 down step.
11220434	AFE_GAIN2_CON3	32	**AFE Gain2 Control Register 3** Defines the GAIN2 up step.
11220438	AFE_GAIN2_CONN	32	**AFE Gain2 Connection Register** Sets up the GAIN2 interconnection blocks.
1122043C	AFE_GAIN2_CUR	32	**AFE Gain2 Cursor Register** Indicates the value current GAIN 2.
11220440	AFE_GAIN2_CONN2	32	**AFE Gain2 Connection Register 2** Sets up the GAIN2 interconnection blocks.
11220444	AFE_GAIN2_CONN3	32	**AFE Gain2 Connection Register 3** Sets up the GAIN2 interconnection blocks.
11220448	AFE_GAIN1_CONN2	32	**AFE Gain1 Connection Register 2** Sets up the gain1 interconnection blocks.
1122044C	AFE_GAIN1_CONN3	32	**AFE Gain1 Connection Register 3** Sets up the gain1 interconnection blocks.
11220468	AFE_CONN9	32	AFE Connection Register 9
1122046C	AFE_CONN10	32	AFE Connection Register 10
112204F0	AFE_SRAM_DELSEL_CON0	32	Memory DELSEL Control 0
112204F4	AFE_SRAM_DELSEL_CON1	32	Memory DELSEL Control 1
11220500	AFE_ASRC_CON0	32	ASRC Config 0
11220504	AFE_ASRC_CON1	32	ASRC Config 1

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Address	Name	Width	Register Function
11220508	AFE_ASRC_CON2	32	ASRC Config 2
1122050C	AFE_ASRC_CON3	32	ASRC Config 3
11220510	AFE_ASRC_CON4	32	ASRC Config 4
11220514	AFE_ASRC_CON5	32	ASRC Config 5
11220518	AFE_ASRC_CON6	32	ASRC Config 6
1122051C	AFE_ASRC_CON7	32	ASRC Config 7
11220520	AFE_ASRC_CON8	32	ASRC Config 8
11220524	AFE_ASRC_CON9	32	ASRC Config 9
11220528	AFE_ASRC_CON10	32	ASRC Config 10
1122052C	AFE_ASRC_CON11	32	ASRC Config 11
11220530	PCM_INTF_CON1	32	PCM Interface Config 1
11220538	PCM_INTF_CON2	32	PCM Interface Config 2
1122053C	PCM2_INTF_CON	32	PCM2 Interface Config
11220550	AFE_ASRC_CON13	32	ASRC Config 13
11220554	AFE_ASRC_CON14	32	ASRC Config 14
11220558	AFE_ASRC_CON15	32	ASRC Config 15
1122055C	AFE_ASRC_CON16	32	ASRC Config 16
11220560	AFE_ASRC_CON17	32	ASRC Config 17
11220564	AFE_ASRC_CON18	32	ASRC Config 18
11220568	AFE_ASRC_CON19	32	ASRC Config 19
1122056C	AFE_ASRC_CON20	32	ASRC Config 20
11220570	AFE_ASRC_CON21	32	ASRC Config 21
11220578	AFE_ASRC_CON23	32	ASRC Config 23
1122057C	AFE_ASRC4_CON24	32	ASRC Config 24
112206C0	AFE_ASRC4_CON0	32	ASRC4 Config 0
112206C4	AFE_ASRC4_CON1	32	ASRC4 Config 1
112206C8	AFE_ASRC4_CON2	32	ASRC4 Config 2
112206CC	AFE_ASRC4_CON3	32	ASRC4 Config 3

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Address	Name	Width	Register Function
112206D0	AFE_ASRC4_CON4	32	ASRC4 Config 4
112206D4	AFE_ASRC4_CON5	32	ASRC4 Config 5
112206D8	AFE_ASRC4_CON6	32	ASRC4 Config 6
112206DC	AFE_ASRC4_CON7	32	ASRC4 Config 7
112206E0	AFE_ASRC4_CON8	32	ASRC4 Config 8
112206E4	AFE_ASRC4_CON9	32	ASRC4 Config 9
112206E8	AFE_ASRC4_CON10	32	ASRC4 Config 10
112206EC	AFE_ASRC4_CON11	32	ASRC4 Config 11
112206F4	AFE_ASRC4_CON13	32	ASRC4 Config 13
112206F8	AFE_ASRC4_CON14	32	ASRC4 Config 14

11220000 AUDIO_TOP_CON0 Audio Top Control Register 0 80FD4038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		ahb_idle_en_int	ahb_idle_en_ext		pdn_tml	pdn_dac_predis	pdn_dac	pdn_adc	Reserved_23_20				PDN_APLL_TUNER	PDN_APLL2_TUNER		
Type		RW	RW		RW	RW	RW	RW	RW				RW	RW		
Reset		0	0		0	0	0	0	1	1	1	1	1	1		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		APB3_SEL	APB_R2T	APB_W2T			PDN_24M	PDN_22M		PDN_I2S				PDN_AFE	Reserved_1_0	
Type		RW	RW	RW			RW	RW		RW				RW	RW	
Reset		1	0	0			0	0		0				0	0	0

Bit(s)	Name	Description
30	ahb_idle_en_int	**Enables AHB idle for internal bus clock** 0: Disable 1: Enable
29	ahb_idle_en_ext	**Enables AHB idle for external bus clock** 0: Disable 1: Enable
27	pdn_tml	**Powers down ADDA ADC sine generator (test model) clock** 0: Does not power down 1: Power down
26	pdn_dac_predis	**Powers down ADDA DAC pre-distortion clock** 0: Does not power down 1: Power down
25	pdn_dac	**Powers down ADDA DAC clock** 0: Does not power down ADDA DAC 1: Power down ADDA DAC
24	pdn_adc	**Powers down ADDA ADC clock**

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Bit(s)	Name	Description
		0: Does not power down ADDA ADC 1: Power down ADDA ADC
19	PDN_APLL_TUNER	**Controls power-down for APLL tuner** 0: Power on apll_tuner clock. 1: Power down apll_tuner clock.
18	PDN_APLL2_TUNER	**Controls power-down for APLL2 tuner** 0: Power on apll_tuner clock. 1: Power down apll_tuner clock.
14	APB3_SEL	**Uses APB 3.0 protocol** 0: Does not use APB 30 1: Use APB 30
13	APB_R2T	**Read cycle for APB write** 0: 1T 1: 2T
12	APB_W2T	**Read cycle for APB read** 0: 1T 1: 2T
9	PDN_24M	**Power-down signal for low-jitter 24.576M clock** 0: Power on 24M clock 1: Power down 24M clock
8	PDN_22M	**Power-down signal for low-jitter 22.5792M clock** 0: Power on 22M clock 1: Power down 22M clock
6	PDN_I2S	**Power-down signal for I2S input clock** 0: Does not power down 1: Power down
2	PDN_AFE	**Power-down signal for AFE clock** 0: Power on AFE clock 1: Power down AFE clock

11220004 **AUDIO_TOP_CON1** **Audio Top Control Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									I2S4_BCLK_SW_CG	I2S3_BCLK_SW_CG	I2S2_BCLK_SW_CG	I2S1_BCLK_SW_CG		I2S_SOFT_RST2	I2S_SOFT_RST	
Type									RW	RW	RW	RW		RW	RW	
Reset									0	0	0	0		0	0	

Bit(s)	Name	Description
7	I2S4_BCLK_SW_CG	**Set to 1 to gate I2S4 engine clock** 0: Not clock-gated 1: Clock-gated
6	I2S3_BCLK_SW_CG	**Set to 1 to gate I2S3 engine clock** 0: Not clock-gated 1: Clock-gated
5	I2S2_BCLK_SW_CG	**Set to 1 to gate I2S2 engine clock**

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Bit(s)	Name	Description
		0: Not clock-gated 1: Clock-gated
4	I2S1_BCLK_SW_CG	**Set to 1 to gate I2S1 engine clock** 0: Not clock-gated 1: Clock-gated
2	I2S_SOFT_RST2	**Soft reset bit for 4-wire DAC/ADC I2S mode** Set to 1 before configuring AFE_I2S_CON1 and AFE_I2S_CON2. After finishing configuration, reset it to 0. 0: Normal 1: Soft reset
1	I2S_SOFT_RST	**Soft reset bit for 4-wire I2S mode** Set to 1 before configuring AFE_I2S_CON and AFE_I2S_CON3. After finishing configuration, reset it to 0. 0: Normal 1: Soft reset

1122000C **AUDIO_TOP_CON3** **Audio Top Control Register 3** **60000004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**BUSY**	**OS_DISABLE**	**CG_DISABLE**	**Reserved_28_16**												
Type	RW	RW	RW	RW												
Reset	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**Reserved_3_1**			**CLEAR_FLAG**
Type													RW			RW
Reset													0	1	0	0

Bit(s)	Name	Description
31	BUSY	Reserved
30	OS_DISABLE	
29	CG_DISABLE	
0	CLEAR_FLAG	Clears slave bus decoding error flag

11220010 **AFE_DAC_CON0** **AFE Control Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**AFE_AWB_RETM**	**AFE_DL1_data2_RETM**	**AFE_DL2_RETM**	**AFE_DL1_RETM**	**AFE_ON_RETM**	**MOD_PCM_DUP_WR**	**DAI_MODE**		**VUL_data2_MODE**				**DL1_data2_MODE**			
Type	RU	RU	RU	RU	RU	RW	RW		RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**VUL2_R_MONO**	**VUL2_DATA**	**VUL_data2_ON**	**DL1_data2_ON**	**MOD_PCM_ON**	**AWB_ON**		**DAI_ON**	**VUL_ON**	**DL2_ON**	**DL1_ON**	**AFE_ON**
Type					RW	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW

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Reset					0	0	0	0	0	0		0	0	0	0	0

Bit(s)	Name	Description
31	AFE_AWB_RETM	**Monitor signal for retiming of AWB_ON**
30	AFE_DL1_data2_RETM	**Monitor signal for retiming of DL1_data2_ON**
29	AFE_DL2_RETM	**Monitor signal for retiming of DL2_ON**
28	AFE_DL1_RETM	**Monitor signal for retiming of DL1_ON**
27	AFE_ON_RETM	**Monitor signal for retiming of AFE_ON**
26	MOD_PCM_DUP_WR	**Controls the data write mode for modem PCM memory interface path** 0: Normal write 1: Duplicated write
25:24	DAI_MODE	**Controls the sampling frequency for DAI path** 0: 8k 1: 16k 2: 32k
23:20	VUL_data2_MODE	**Controls the sampling frequency for voice uplink data2 path** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k
19:16	DL1_data2_MODE	**Controls the sampling frequency for downlink 1 data2 path** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k
11	VUL2_R_MONO	**Controls the data mono type for voice uplink memory data2 interface path** 0: Mono use L channel 1: Mono use R channel
10	VUL2_DATA	**Controls the data mode for voice uplink memory data2 interface path** 0: Stereo 1: Mono
9	VUL_data2_ON	**Controls the enabling of uplink data2 memory interface path** 0: Off 1: On
8	DL1_data2_ON	**Controls the enabling of downlink 1-data2 memory interface path**

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Bit(s)	Name	Description
		0: Off 1: On
7	MOD_PCM_ON	**Controls the enabling of modem PCM memory interface path** 0: Off 1: On
6	AWB_ON	**Controls the enabling of AWB memory interface path** 0: Off 1: On
4	DAI_ON	**Controls the enabling of DAI memory interface path** 0: Off 1: On
3	VUL_ON	**Controls the enabling of uplink memory interface path** 0: Off 1: On
2	DL2_ON	**Controls the enabling of downlink 2 memory interface path** 0: Off 1: On
1	DL1_ON	**Controls the enabling of downlink 1 memory interface path** 0: Off 1: On
0	AFE_ON	**Controls the enabling of the whole AFE module** 0: Off 1: On

11220014 **AFE_DAC_CON1** **AFE Control Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MOD_PCM_MODE		DAI_DUP_WR	VUL_R_MONO	VUL_DATA	AXI_2X1_CG_DISABLE	AWB_R_MONO	AWB_DATA	Reserved	DL2_DATA	DL1_DATA	DL1_data2_DATA	VUL_MODE			
Type	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	AWB_MODE				I2S_MODE				DL2_MODE				DL1_MODE			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	MOD_PCM_MODE	**Controls the sampling frequency for MOD_PCM path** 0: 8k 1: 16k 2: 32k
29	DAI_DUP_WR	**Controls the data write mode for DAI memory interface path** 0: Normal write 1: Duplicated write
28	VUL_R_MONO	**Controls the data mono type for voice uplink memory interface path** 0: Mono use L channel 1: Mono use R channel
27	VUL_DATA	**Controls the data mode for voice uplink memory interface path** 0: Stereo

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Bit(s)	Name	Description
		1: Mono
26	AXI_2X1_CG_DISABLE	0: Enable 1: Disable
25	AWB_R_MONO	**Controls the data mono type for audio write back memory interface path** 0: Mono use L channel 1: Mono use R channel
24	AWB_DATA	**Controls the data mode for audio write back memory interface path** 0: Stereo 1: Mono
22	DL2_DATA	**Controls the data mode for downlink 2 memory interface path** 0: Stereo 1: Mono
21	DL1_DATA	**Controls the data mode for downlink 1 memory interface path** 0: Stereo 1: Mono
20	DL1_data2_DATA	**Controls the data mode for downlink 1 data2 memory interface path** 0: Stereo 1: Mono
19:16	VUL_MODE	**Controls the sampling frequency for voice uplink path** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k
15:12	AWB_MODE	**Controls the sampling frequency for audio write back path** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 0111b: 130k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k 1111b: 260k
11:8	I2S_MODE	**Controls the sampling frequency for I2S path** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k

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Bit(s)	Name	Description
		1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k
7:4	DL2_MODE	**Controls the sampling frequency for downlink 2 path** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k
3:0	DL1_MODE	**Controls the sampling frequency for downlink 1 path** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k

11220018 AFE_I2S_CON AFE I2S Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PHASE_SHIFT_FIX	BCK_NEG_EG_LATCH	BCK_INV	I2SIN_PAD_SEL								I2S_LOOPBACK				
Type	RW	RW	RW	RW								RW				
Reset	0	0	0	0								0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				I2S1_HD_EN					INV_PAD_CTRL		INV_LRCK		I2S_FMT	I2S_SRC	I2S_WLEN	I2S_EN
Type				RW					RW		RW		RW	RW	RW	RW
Reset				0					0		0		0	0	0	0

Bit(s)	Name	Description
31	PHASE_SHIFT_FIX	0: Disable phase-shift fix 1: Enable phase-shift fix
30	BCK_NEG_EG_LATCH	**Controls I2S input data latching time** 0: Pos-edge latch 1: Neg-edge latch
29	BCK_INV	**Controls I2S output bck phase**

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Bit(s)	Name	Description
		0: Does not invert bck 1: Invert bck
28	I2SIN_PAD_SEL	**Controls I2S input source** If it's FM Rx i2s in, choose 0 from connsys. If mATV, choose 1 from io_mux. 0: I2S in from connsys 1: I2S in from io_mux
20	I2S_LOOPBACK	**Controls I2S internal loopback mode** The loopback source is from 2nd I2S output. 0: Normal I2S in 1.: I2S in from internal 2nd I2S output
12	I2S1_HD_EN	**Enables low-jitter bck HD audio** 0: Normal h26m clock 1: Low-jitter clock
7	INV_PAD_CTRL	**Decides if the output enabling of I2S pads should be inverted** 0: No inverse 1: Invert
5	INV_LRCK	**Controls the phase of I2S path** 0: Does not invert LRCK 1: Invert LRCK for LJ mode
3	I2S_FMT	**Controls the format for I2S path** 0: EIAJ 1: I2S
2	I2S_SRC	**Controls the master/slave for I2S path** 0: Master mode. Clock goes from AFE. 1: Slave mode. Clock receives from other devices.
1	I2S_WLEN	**Controls the word length of I2S** 0: 16 bits 1: 32 bits
0	I2S_EN	**Controls the enabling of I2S path** 0: Disable I2S 1: Enable I2S

1122001C **AFE_DAIBT_CON0** **AFE DAI/BT Control Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				USE_MRGIF_INPUT			DAIBT_MODE	DAI_SEL		BT_LEN			DATA_RDY	BTSYNC	BT_ON	DAIBT_ON
Type				RW			RW	RW		RW			RW	RW	RW	RW
Reset				0			0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
12	USE_MRGIF_INPUT	**Selects input data are from MRGIF or BT** 0: Off 1: On
9	DAIBT_MODE	**Selects data rate of DAI/BT** 0: 8k mode

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Bit(s)	Name	Description
		1: 16k mode
8	DAI_SEL	**Selects H/L word received to DSP** Suggested: 0 0: High word ([31:16]) 1: Low word ([15:0])
6:4	BT_LEN	**Bluetooth PCM long frame sync length = BT_LEN + 1**
3	DATA_RDY	**Indicates DSP is ready to transmit data** 0: Not ready 1: Data ready
2	BTSYNC	**Bluetooth PCM frame sync type** 0: Not ready 1: Ready
1	BT_ON	**Controls the enabling of Bluetooth function** 0: Turn off BT. Turn on DAI if DAIBT_ON = 1 1: Turn on BT
0	DAIBT_ON	**Controls the enabling of DAI/BT function** 0: Disable DAI/BT 1: Enable DAI/BT

11220020 AFE_CONN0 AFE Connection Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I08_O01_R	I07_O01_R	I06_O01_R	I05_O01_R	I01_O01_R	I00_O01_R	I09_O01_S	I08_O01_S	I07_O01_S	I06_O01_S	I05_O01_S	I04_O01_S	I03_O01_S	I02_O01_S	I01_O01_S	I00_O01_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I08_O00_R	I07_O00_R	I06_O00_R	I05_O00_R	I01_O00_R	I00_O00_R	I09_O00_S	I08_O00_S	I07_O00_S	I06_O00_S	I05_O00_S	I04_O00_S	I03_O00_S	I02_O00_S	I01_O00_S	I00_O00_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	I08_O01_R	**Controls the enabling of right shift 1 bit from I08 to O01** 0: No shift 1: Right shift 1 bit
30	I07_O01_R	**Controls the enabling of right shift 1 bit from I07 to O01** 0: No shift 1: Right shift 1 bit
29	I06_O01_R	**Controls the enabling of right shift 1 bit from I06 to O01** 0: No shift 1: Right shift 1 bit
28	I05_O01_R	**Controls the enabling of right shift 1 bit from I05 to O01** 0: No shift 1: Right shift 1 bit
27	I01_O01_R	**Controls the enabling of right shift 1 bit from I01 to O01** 0: No shift 1: Right shift 1 bit
26	I00_O01_R	**Controls the enabling of right shift 1 bit from I00 to O01** 0: No shift 1: Right shift 1 bit

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Bit(s)	Name	Description
25	I09_O01_S	**Controls the path from I09 to O01** 0: Off 1: On
24	I08_O01_S	**Controls the path from I08 to O01** 0: Off 1: On
23	I07_O01_S	**Controls the path from I07 to O01** 0: Off 1: On
22	I06_O01_S	**Controls the path from I06 to O01** 0: Off 1: On
21	I05_O01_S	**Controls the path from I05 to O01** 0: Off 1: On
20	I04_O01_S	**Controls the path from I04 to O01** 0: Off 1: On
19	I03_O01_S	**Controls the path from I03 to O01** 0: Off 1: On
18	I02_O01_S	**Controls the path from I02 to O01** 0: Off 1: On
17	I01_O01_S	**Controls the path from I01 to O01** 0: Off 1: On
16	I00_O01_S	**Controls the path from I00 to O01** 0: Off 1: On
15	I08_O00_R	**Controls the enabling of right shift 1 bit from I08 to O00** 0: No shift 1: Right shift 1 bit
14	I07_O00_R	**Controls the enabling of right shift 1 bit from I07 to O00** 0: No shift 1: Right shift 1 bit
13	I06_O00_R	**Controls the enabling of right shift 1 bit from I06 to O00** 0: No shift 1: Right shift 1 bit
12	I05_O00_R	**Controls the enabling of right shift 1 bit from I05 to O00** 0: No shift 1: Right shift 1 bit
11	I01_O00_R	**Controls the enabling of right shift 1 bit from I01 to O00** 0: No shift 1: Right shift 1 bit
10	I00_O00_R	**Controls the enabling of right shift 1 bit from I00 to O00** 0: No shift 1: Right shift 1 bit
9	I09_O00_S	**Controls the path from I09 to O00** 0: Off 1: On
8	I08_O00_S	**Controls the path from I08 to O00** 0: Off

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Bit(s)	Name	Description
		1: On
7	I07_O00_S	**Controls the path from I07 to O00** 0: Off 1: On
6	I06_O00_S	**Controls the path from I06 to O00** 0: Off 1: On
5	I05_O00_S	**Controls the path from I05 to O00** 0: Off 1: On
4	I04_O00_S	**Controls the path from I04 to O00** 0: Off 1: On
3	I03_O00_S	**Controls the path from I03 to O00** 0: Off 1: On
2	I02_O00_S	**Controls the path from I02 to O00** 0: Off 1: On
1	I01_O00_S	**Controls the path from I01 to O00** 0: Off 1: On
0	I00_O00_S	**Controls the path from I00 to O00** 0: Off 1: On

11220024 AFE_CONN1 AFE Connection Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I08_O03_R	I07_O03_R	I06_O03_R	I05_O03_R	I01_O03_R	I00_O03_R	I09_O03_S	I08_O03_S	I07_O03_S	I06_O03_S	I05_O03_S	I04_O03_S	I03_O03_S	I02_O03_S	I01_O03_S	I00_O03_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I08_O02_R	I07_O02_R	I06_O02_R	I05_O02_R	I01_O02_R	I00_O02_R	I09_O02_S	I08_O02_S	I07_O02_S	I06_O02_S	I05_O02_S	I04_O02_S	I03_O02_S	I02_O02_S	I01_O02_S	I00_O02_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	I08_O03_R	**Controls the enabling of right shift 1 bit from I08 to O03** 0: No shift 1: Right shift 1 bit
30	I07_O03_R	**Controls the enabling of right shift 1 bit from I07 to O03** 0: No shift 1: Right shift 1 bit
29	I06_O03_R	**Controls the enabling of right shift 1 bit from I06 to O03** 0: No shift 1: Right shift 1 bit
28	I05_O03_R	**Controls the enabling of right shift 1 bit from I05 to O03** 0: No shift

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Bit(s)	Name	Description
		1: Right shift 1 bit
27	I01_O03_R	**Controls the enabling of right shift 1 bit from I01 to O03** 0: No shift 1: Right shift 1 bit
26	I00_O03_R	**Controls the enabling of right shift 1 bit from I00 to O03** 0: No shift 1: Right shift 1 bit
25	I09_O03_S	**Controls the path from I09 to O03** 0: Off 1: On
24	I08_O03_S	**Controls the path from I08 to O03** 0: Off 1: On
23	I07_O03_S	**Controls the path from I07 to O03** 0: Off 1: On
22	I06_O03_S	**Controls the path from I06 to O03** 0: Off 1: On
21	I05_O03_S	**Controls the path from I05 to O03** 0: Off 1: On
20	I04_O03_S	**Controls the path from I04 to O03** 0: Off 1: On
19	I03_O03_S	**Controls the path from I03 to O03** 0: Off 1: On
18	I02_O03_S	**Controls the path from I02 to O03** 0: Off 1: On
17	I01_O03_S	**Controls the path from I01 to O03** 0: Off 1: On
16	I00_O03_S	**Controls the path from I00 to O03** 0: Off 1: On
15	I08_O02_R	**Controls the enabling of right shift 1 bit from I08 to O02** 0: No shift 1: Right shift 1 bit
14	I07_O02_R	**Controls the enabling of right shift 1 bit from I07 to O02** 0: No shift 1: Right shift 1 bit
13	I06_O02_R	**Controls the enabling of right shift 1 bit from I06 to O02** 0: No shift 1: Right shift 1 bit
12	I05_O02_R	**Controls the enabling of right shift 1 bit from I05 to O02** 0: No shift 1: Right shift 1 bit
11	I01_O02_R	**Controls the enabling of right shift 1 bit from I01 to O02** 0: No shift 1: Right shift 1 bit

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Bit(s)	Name	Description
10	I00_O02_R	**Controls the enabling of right shift 1 bit from I00 to O02** 0: No shift 1: Right shift 1 bit
9	I09_O02_S	**Controls the path from I09 to O02** 0: Off 1: On
8	I08_O02_S	**Controls the path from I08 to O02** 0: Off 1: On
7	I07_O02_S	**Controls the path from I07 to O02** 0: Off 1: On
6	I06_O02_S	**Controls the path from I06 to O02** 0: Off 1: On
5	I05_O02_S	**Controls the path from I05 to O02** 0: Off 1: On
4	I04_O02_S	**Controls the path from I04 to O02** 0: Off 1: On
3	I03_O02_S	**Controls the path from I03 to O02** 0: Off 1: On
2	I02_O02_S	**Controls the path from I02 to O02** 0: Off 1: On
1	I01_O02_S	**Controls the path from I01 to O02** 0: Off 1: On
0	I00_O02_S	**Controls the path from I00 to O02** 0: Off 1: On

11220028 AFE_CONN2 AFE Connection Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I08_O08_S	I06_O08_S	I04_O08_S	I07_O07_S	I05_O07_S	I03_O07_S	I08_O06_S	I06_O06_S	I04_O06_S	I01_O06_S	I09_O05_S	I07_O05_S	I05_O05_S	I03_O05_S	I02_O05_S	I00_O05_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I08_O04_R	I07_O04_R	I06_O04_R	I05_O04_R	I01_O04_R	I00_O04_R	I09_O04_S	I08_O04_S	I07_O04_S	I06_O04_S	I05_O04_S	I04_O04_S	I03_O04_S	I02_O04_S	I01_O04_S	I00_O04_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	I08_O08_S	**Controls the path from I08 to O08** 0: Off 1: On

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Bit(s)	Name	Description
30	I06_O08_S	**Controls the path from I06 to O08** 0: Off 1: On
29	I04_O08_S	**Controls the path from I04 to O08** 0: Off 1: On
28	I07_O07_S	**Controls the path from I07 to O07** 0: Off 1: On
27	I05_O07_S	**Controls the path from I05 to O07** 0: Off 1: On
26	I03_O07_S	**Controls the path from I03 to O07** 0: Off 1: On
25	I08_O06_S	**Controls the path from I08 to O06** 0: Off 1: On
24	I06_O06_S	**Controls the path from I06 to O06** 0: Off 1: On
23	I04_O06_S	**Controls the path from I04 to O06** 0: Off 1: On
22	I01_O06_S	**Controls the path from I01 to O06** 0: Off 1: On
21	I09_O05_S	**Controls the path from I09 to O05** 0: Off 1: On
20	I07_O05_S	**Controls the path from I07 to O05** 0: Off 1: On
19	I05_O05_S	**Controls the path from I05 to O05** 0: Off 1: On
18	I03_O05_S	**Controls the path from I03 to O05** 0: Off 1: On
17	I02_O05_S	**Controls the path from I02 to O05** 0: Off 1: On
16	I00_O05_S	**Controls the path from I00 to O05** 0: Off 1: On
15	I08_O04_R	**Controls the enabling of right shift 1 bit from I08 to O04** 0: No shift 1: Right shift 1 bit
14	I07_O04_R	**Controls the enabling of right shift 1 bit from I07 to O04** 0: No shift 1: Right shift 1 bit
13	I06_O04_R	**Controls the enabling of right shift 1 bit from I06 to O04** 0: No shift

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Bit(s)	Name	Description
		1: Right shift 1 bit
12	I05_O04_R	**Controls the enabling of right shift 1 bit from I05 to O04** 0: No shift 1: Right shift 1 bit
11	I01_O04_R	**Controls the enabling of right shift 1 bit from I01 to O04** 0: No shift 1: Right shift 1 bit
10	I00_O04_R	**Controls the enabling of right shift 1 bit from I00 to O04** 0: No shift 1: Right shift 1 bit
9	I09_O04_S	**Controls the path from I09 to O04** 0: Off 1: On
8	I08_O04_S	**Controls the path from I08 to O04** 0: Off 1: On
7	I07_O04_S	**Controls the path from I07 to O04** 0: Off 1: On
6	I06_O04_S	**Controls the path from I06 to O04** 0: Off 1: On
5	I05_O04_S	**Controls the path from I05 to O04** 0: Off 1: On
4	I04_O04_S	**Controls the path from I04 to O04** 0: Off 1: On
3	I03_O04_S	**Controls the path from I03 to O04** 0: Off 1: On
2	I02_O04_S	**Controls the path from I02 to O04** 0: Off 1: On
1	I01_O04_S	**Controls the path from I01 to O04** 0: Off 1: On
0	I00_O04_S	**Controls the path from I00 to O04** 0: Off 1: On

1122002C **AFE_CONN3** **AFE Connection Register 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I16_O03_R	I15_O03_R	I16_O03_S	I15_O03_S	I14_O03_S	I16_O02_R	I15_O02_R	I16_O02_S	I15_O02_S	I14_O02_S	I16_O01_R	I15_O01_R	I16_O01_S	I15_O01_S	I14_O01_S	I16_O00_R
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O00_R	I16_O00_S	I15_O00_S	I14_O00_S	I09_O12_S	I08_O12_S	I06_O12_S	I07_O11_S	I05_O11_S	I02_O11_S	I08_O10_S	I06_O10_S	I04_O10_S	I07_O09_S	I05_O09_S	I03_O09_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	I16_O03_R	**Controls the enabling of right shift 1 bit from I16 to O03** 0: Off 1: On
30	I15_O03_R	**Controls the enabling of right shift 1 bit from I15 to O03** 0: Off 1: On
29	I16_O03_S	**Controls the path from I16 to O03** 0: Off 1: On
28	I15_O03_S	**Controls the path from I15 to O03** 0: Off 1: On
27	I14_O03_S	**Controls the path from I14 to O03** 0: Off 1: On
26	I16_O02_R	**Controls the enabling of right shift 1 bit from I16 to O02** 0: Off 1: On
25	I15_O02_R	**Controls the enabling of right shift 1 bit from I15 to O02** 0: Off 1: On
24	I16_O02_S	**Controls the path from I16 to O02** 0: Off 1: On
23	I15_O02_S	**Controls the path from I15 to O02** 0: Off 1: On
22	I14_O02_S	**Controls the path from I14 to O02** 0: Off 1: On
21	I16_O01_R	**Controls the enabling of right shift 1 bit from I16 to O01** 0: Off 1: On
20	I15_O01_R	**Controls the enabling of right shift 1 bit from I15 to O01** 0: Off 1: On
19	I16_O01_S	**Controls the path from I16 to O01** 0: Off 1: On
18	I15_O01_S	**Controls the path from I15 to O01** 0: Off 1: On
17	I14_O01_S	**Controls the path from I14 to O01** 0: Off 1: On
16	I16_O00_R	**Controls the enabling of right shift 1 bit from I16 to O00** 0: Off 1: On
15	I15_O00_R	**Controls the enabling of right shift 1 bit from I15 to O00** 0: Off

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Bit(s)	Name	Description
		1: On
14	I16_O00_S	**Controls the path from I16 to O00** 0: Off 1: On
13	I15_O00_S	**Controls the path from I15 to O00** 0: Off 1: On
12	I14_O00_S	**Controls the path from I14 to O00** 0: Off 1: On
11	I09_O12_S	**Controls the path from I09 to O12** 0: Off 1: On
10	I08_O12_S	**Controls the path from I08 to O12** 0: Off 1: On
9	I06_O12_S	**Controls the path from I06 to O12** 0: Off 1: On
8	I07_O11_S	**Controls the path from I07 to O11** 0: Off 1: On
7	I05_O11_S	**Controls the path from I05 to O11** 0: Off 1: On
6	I02_O11_S	**Controls the path from I02 to O11** 0: Off 1: On
5	I08_O10_S	**Controls the path from I08 to O10** 0: Off 1: On
4	I06_O10_S	**Controls the path from I06 to O10** 0: Off 1: On
3	I04_O10_S	**Controls the path from I04 to O10** 0: Off 1: On
2	I07_O09_S	**Controls the path from I07 to O09** 0: Off 1: On
1	I05_O09_S	**Controls the path from I05 to O09** 0: Off 1: On
0	I03_O09_S	**Controls the path from I03 to O09** 0: Off 1: On

11220030 AFE_CONN4 AFE Connection Register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		BYPASS_A				I04_O02_	I03_O02_	I02_O18_	I02_O17_	I02_O08_	I02_O07_	I01_O06_R	I00_O05_	I08_O18_	I06_O18_	I04_O18_

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		SRC				R	R	S	S	S	S		R	S	S	S
Type		RW				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset		0				0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I07_O17_S	I05_O17_S	I03_O17_S	I14_O12_S	I16_O10_S	I15_O09_S	I16_O06_R	I16_O06_S	I15_O05_R	I15_O05_S	I14_O05_S	I16_O04_R	I15_O04_R	I16_O04_S	I15_O04_S	I14_O04_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30	BYPASS_ASRC	**I2S in I_0, I_1 bypass ASRC** 0: Off 1: On
26	I04_O02_R	**Controls the enabling of right shift 1 bit from I04 to O02** 0: Off 1: On
25	I03_O02_R	**Controls the enabling of right shift 1 bit from I03 to O02** 0: Off 1: On
24	I02_O18_S	**Controls the path from I02 to O18** 0: Off 1: On
23	I02_O17_S	**Controls the path from I02 to O17** 0: Off 1: On
22	I02_O08_S	**Controls the path from I02 to O08** 0: Off 1: On
21	I02_O07_S	**Controls the path from I02 to O07** 0: Off 1: On
20	I01_O06_R	**Controls the enabling of right shift 1 bit from I01 to O06** 0: Off 1: On
19	I00_O05_R	**Controls the enabling of right shift 1 bit from I00 to O05** 0: Off 1: On
18	I08_O18_S	**Controls the path from I08 to O18** 0: Off 1: On
17	I06_O18_S	**Controls the path from I06 to O18** 0: Off 1: On
16	I04_O18_S	**Controls the path from I04 to O18** 0: Off 1: On
15	I07_O17_S	**Controls the path from I07 to O17** 0: Off 1: On
14	I05_O17_S	**Controls the path from I05 to O17** 0: Off 1: On
13	I03_O17_S	**Controls the path from I03 to O17** 0: Off

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Bit(s)	Name	Description
		1: On
12	I14_O12_S	**Controls the path from I14 to O12** 0: Off 1: On
11	I16_O10_S	**Controls the path from I16 to O10** 0: Off 1: On
10	I15_O09_S	**Controls the path from I15 to O09** 0: Off 1: On
9	I16_O06_R	**Controls the enabling of right shift 1 bit from I16 to O06** 0: Off 1: On
8	I16_O06_S	**Controls the path from I16 to O06** 0: Off 1: On
7	I15_O05_R	**Controls the enabling of right shift 1 bit from I15 to O05** 0: Off 1: On
6	I15_O05_S	**Controls the path from I15 to O05** 0: Off 1: On
5	I14_O05_S	**Controls the path from I14 to O05** 0: Off 1: On
4	I16_O04_R	**Controls the enabling of right shift 1 bit from I16 to O04** 0: Off 1: On
3	I15_O04_R	**Controls the enabling of right shift 1 bit from I15 to O04** 0: Off 1: On
2	I16_O04_S	**Controls the path from I16 to O04** 0: Off 1: On
1	I15_O04_S	**Controls the path from I15 to O04** 0: Off 1: On
0	I14_O04_S	**Controls the path from I14 to O04** 0: Off 1: On

11220034 **AFE_I2S_CON1** **AFE I2S Control Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I2S2_LR_SWAP															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				I2S2_HD_E	I2S2_OUT_MODE						INV_LRCK		I2S2_FMT		I2S2_WLE	I2S2_EN

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				N										N		
Type				RW	RW						RW		RW		RW	RW
Reset				0	0	0	0	0			0		0		0	0

Bit(s)	Name	Description
31	I2S2_LR_SWAP	**Only for the flexibility usage** 0: No swapping L and R channel 1: Swap left and right channel
12	I2S2_HD_EN	**Enables low-jitter bck HD audio** 0: Normal h26m clock 1: Low-jitter clock
11:8	I2S2_OUT_MODE	**Controls the sampling frequency for I2S2 output path** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k
5	INV_LRCK	**Controls the phase of I2S path** 0: Does not invert LRCK 1: Invert LRCK for LJ mode
3	I2S2_FMT	**Controls the format for I2S path** 0: EIAJ 1: I2S
1	I2S2_WLEN	**Controls the word length of I2S** 0: 16 bits 1: 32 bits
0	I2S2_EN	**Controls the enbling of I2S path** 0: Disable I2S output 1: Enable I2S output

11220038 **AFE_I2S_CON2** **AFE I2S Control Register 2** **08000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I2S3_LR_SWAP			I2S3_UPDATE_WORD					I2S3_bck_inv	I2S3_fpga_bit_test	I2S3_fpga_bit	I2S3_LOOPBACK				
Type	RW			RW					RW	RW	RW	RW				
Reset	0			0	1	0	0	0	0	0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				I2S3_HD_EN	I2S3_OUT_MODE								I2S3_FMT		I2S3_WLEN	I2S3_EN
Type				RW	RW								RW		RW	RW
Reset				0	0	0	0	0					0		0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31	I2S3_LR_SWAP	**Just for the flexibility usage** 0: No swapping L and R channel 1: Swap left and right channel
28:24	I2S3_UPDATE_WORD	**I2S3 buffer update timing** Valid between 0 ~ 15 for 32fs BCK or 0 ~ 31 for 64fs BCK
23	I2S3_bck_inv	**Inverts bit_ck for EXTADC** 0: Does not invert bit_ck (to EXTADC) 1: Invert bit_ck (to EXTADC)
22	I2S3_fpga_bit_test	**For debugging** 0: sdata depends on bit[20]. 1: sdata depends on bit[21].
21	I2S3_fpga_bit	**Valid when bit[22] = 1** 0: sdata set to 0 1: sdata set to 1
20	I2S3_LOOPBACK	**Controls I2S internal loopback mode** The loopback source is from I2S4 output. 0: Normal I2S in 1.: I2S in from internal DAC I2S output
12	I2S3_HD_EN	**Enables low-jitter bck HD audio** 0: Normal h26m clock 1: Low-jitter clock
11:8	I2S3_OUT_MODE	**Controls the sampling frequency for I2S3 output path** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k
3	I2S3_FMT	0: EIAJ 1: I2S
1	I2S3_WLEN	**Controls the word length of I2S** 0: 16 bits 1: 32 bits
0	I2S3_EN	**Controls the enabling of I2S path** 0: Disable I2S input 1: Enable I2S input

1122003C **AFE_MRGIF_CON** **AFE Merge Interface Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									**MRGIF_I2S_MODE**				**MRGIF_LOOPBACK**			**MRGIF_I2S_EN**
Type									RW				RW			RW
Reset									0	0	0	0	0			0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name		MRG_CLK_NO_INV	MRG_I2S_TX_DIS	MRG_CNT_CLR	MRG_SYNC_DLY				MRG_CLK_EDGE_DLY		MRG_CLK_DLY					MRGIF_EN
Type		RW	RW	RW	RW				RW		RW					RW
Reset		0	0	0	0	0	0	0	0	0	0	0				0

Bit(s)	Name	Description
23:20	MRGIF_I2S_MODE	**Merge I2S mode** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k
19	MRGIF_LOOPBACK	**Merge interface I2S loopback** 0: Off 1: On
16	MRGIF_I2S_EN	**Merge interface I2S transmit** 0: Off 1: On
14	MRG_CLK_NO_INV	**Set to 1 to not to invert merge interface I2S clock.** 0: Invert 1: No inverse
13	MRG_I2S_TX_DIS	**Set to 1 to disable merge interface I2S Tx.** 0: Enable 1: Disable
12	MRG_CNT_CLR	**When this bit is 1, the I2S and PCM's monitor counter will be cleared. When monitor is used, this bit should be 0.** 0: Off 1: On
11:8	MRG_SYNC_DLY	**Merge interface sync delay number in 26M clock domain**
7:6	MRG_CLK_EDGE_DLY	**Sample and output data's delay number in 26M clock domain**
5:4	MRG_CLK_DLY	**Merge interface clk delay number in 26M clock domain**
0	MRGIF_EN	**Enables merge interface** 0: Off 1: On

11220040 **AFE_DL1_BASE** **AFE DL1 Base Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL1_BASE[27:12]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL1_BASE[11:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:4	AFE_DL1_BASE	**Base address of DL1 input in master mode** Always set AFE_DL1_BASE[3:0] = 4'h0 for the convenience of HW implementation.

11220044 AFE_DL1_CUR AFE DL1 Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL1_CUR[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL1_CUR[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AFE_DL1_CUR	Indicates the current address of the DL1 input buffer

11220048 AFE_DL1_END AFE_DL1_END 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL1_END[27:12]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL1_END[11:0]												AFE_DL1_END_LSB			
Type	RW												RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit(s)	Name	Description
31:4	AFE_DL1_END	**End address of DL1 input in master mode** Always set AFE_DL1_END[3:0] = 4'hf for the convenience of HW implementation.
3:0	AFE_DL1_END_LSB	

1122004C AFE_I2S_CON3 AFE I2S Control Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I2S4_LR_SWAP															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				I2S4_HD_EN	I2S4_OUT_MODE						INV_LRCK		I2S4_FMT		I2S4_WLEN	I2S4_EN
Type				RW	RW						RW		RW		RW	RW
Reset				0	0	0	0	0			0		0		0	0

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Bit(s)	Name	Description
31	I2S4_LR_SWAP	**For flexibility usage only** 0: No swapping L and R channel 1: Swaps left and right channel
12	I2S4_HD_EN	**Enables low-jitter bck HD audio** 0: Normal h26m clock 1: Low-jitter clock
11:8	I2S4_OUT_MODE	**Controls the sampling frequency for I2S4 output path** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k
5	INV_LRCK	**Controls the phase of I2S4 path** 0: Does not invert LRCK 1: Invert LRCK for LJ mode
3	I2S4_FMT	**Controls the format for I2S4 path** 0: EIAJ 1: I2S
1	I2S4_WLEN	**Controls the word length of I2S4 path** 0: 16 bits 1: 32 bits
0	I2S4_EN	**Controls the enabling of I2S path** 0: Disable I2S output 1: Enable I2S output

11220050 **AFE_DL2_BASE** **AFE DL2 Base Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL2_BASE[27:12]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL2_BASE[11:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	AFE_DL2_BASE	**Base address of DL2 input in master mode** Always set AFE_DL2_BASE[3:0] = 4'h0 for the convenience of HW implementation.

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11220054 AFE_DL2_CUR AFE DL2 Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL2_CUR[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL2_CUR[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AFE_DL2_CUR	Indicates the current address of the DL2 input buffer

11220058 AFE_DL2_END AFE_DL2_END 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL2_END[27:12]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL2_END[11:0]												AFE_DL2_END_LSB			
Type	RW												RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit(s)	Name	Description
31:4	AFE_DL2_END	**End address of DL2 input in master mode** Always set AFE_DL2_END[3:0] = 4'hf for the convenience of HW implementation.
3:0	AFE_DL2_END_LSB	

1122005C AFE_CONN5 AFE Connection Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												I09_O18_S	I01_O18_S	I00_O18_S		I09_O17_S
Type												RW	RW	RW		RW
Reset												0	0	0		0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I01_O17_S	I00_O17_S	I01_O10_S	I00_O10_S	I14_O09_S	I09_O09_S	I01_O09_S	I00_O09_S	I14_O08_S	I01_O08_S	I00_O08_S	I14_O07_S	I01_O07_S	I00_O07_S		
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
20	I09_O18_S	**Controls the path from I09 to O18** 0: Off 1: On
19	I01_O18_S	**Controls the path from I01 to O18** 0: Off 1: On

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Bit(s)	Name	Description
18	I00_O18_S	**Controls the path from I00 to O18** 0: Off 1: On
16	I09_O17_S	**Controls the path from I09 to O17** 0: Off 1: On
15	I01_O17_S	**Controls the path from I01 to O17** 0: Off 1: On
14	I00_O17_S	**Controls the path from I00 to O17** 0: Off 1: On
13	I01_O10_S	**Controls the path from I01 to O10** 0: Off 1: On
12	I00_O10_S	**Controls the path from I00 to O10** 0: Off 1: On
11	I14_O09_S	**Controls the path from I14 to O09** 0: Off 1: On
10	I09_O09_S	**Controls the path from I09 to O09** 0: Off 1: On
9	I01_O09_S	**Controls the path from I01 to O09** 0: Off 1: On
8	I00_O09_S	**Controls the path from I00 to O09** 0: Off 1: On
7	I14_O08_S	**Controls the path from I14 to O08** 0: Off 1: On
6	I01_O08_S	**Controls the path from I01 to O08** 0: Off 1: On
5	I00_O08_S	**Controls the path from I00 to O08** 0: Off 1: On
4	I14_O07_S	**Controls the path from I14 to O07** 0: Off 1: On
3	I01_O07_S	**Controls the path from I01 to O07** 0: Off 1: On
2	I00_O07_S	**Controls the path from I00 to O07** 0: Off 1: On

1122006C AFE_CONN_2 AFE Connection 24-bit Register 0019E018

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4BIT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							O25_24BIT	O24_24BIT	O23_24BIT	O22_24BIT	O21_24BIT	O20_24BIT	O19_24BIT	O18_24BIT	O17_24BIT	O16_24BIT
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	1	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	O15_24BIT	O14_24BIT	O13_24BIT	O12_24BIT	O11_24BIT	O10_24BIT	O09_24BIT	O08_24BIT	O07_24BIT	O06_24BIT	O05_24BIT	O04_24BIT	O03_24BIT	O02_24BIT	O01_24BIT	O00_24BIT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0

Bit(s)	Name	Description
25	O25_24BIT	**Controls output data format of O25** 0: 16-bit 1: 24-bit
24	O24_24BIT	**Controls output data format of O24** 0: 16-bit 1: 24-bit
23	O23_24BIT	**Controls output data format of O23** 0: 16-bit 1: 24-bit
22	O22_24BIT	**Controls output data format of O22** 0: 16-bit 1: 24-bit
21	O21_24BIT	**Controls output data format of O21** 0: 16-bit 1: 24-bit
20	O20_24BIT	**Controls output data format of O20** 0: 16-bit 1: 24-bit
19	O19_24BIT	**Controls output data format of O19** 0: 16-bit 1: 24-bit
18	O18_24BIT	**Controls output data format of O18** 0: 16-bit 1: 24-bit
17	O17_24BIT	**Controls output data format of O17** 0: 16-bit 1: 24-bit
16	O16_24BIT	**Controls output data format of O16** 0: 16-bit 1: 24-bit
15	O15_24BIT	**Controls output data format of O15** 0: 16-bit 1: 24-bit
14	O14_24BIT	**Controls output data format of O14** 0: 16-bit 1: 24-bit
13	O13_24BIT	**Controls output data format of O13** 0: 16-bit 1: 24-bit
12	O12_24BIT	**Controls output data format of O12**

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Bit(s)	Name	Description
		0: 16-bit 1: 24-bit
11	O11_24BIT	**Controls output data format of O11** 0: 16-bit 1: 24-bit
10	O10_24BIT	**Controls output data format of O10** 0: 16-bit 1: 24-bit
9	O09_24BIT	**Controls output data format of O09** 0: 16-bit 1: 24-bit
8	O08_24BIT	**Controls output data format of O08** 0: 16-bit 1: 24-bit
7	O07_24BIT	**Controls output data format of O07** 0: 16-bit 1: 24-bit
6	O06_24BIT	**Controls output data format of O06** 0: 16-bit 1: 24-bit
5	O05_24BIT	**Controls output data format of O05** 0: 16-bit 1: 24-bit
4	O04_24BIT	**Controls output data format of O04** 0: 16-bit 1: 24-bit
3	O03_24BIT	**Controls output data format of O03** 0: 16-bit 1: 24-bit
2	O02_24BIT	**Controls output data format of O02** 0: 16-bit 1: 24-bit
1	O01_24BIT	**Controls output data format of O01** 0: 16-bit 1: 24-bit
0	O00_24BIT	**Controls output data format of O00** 0: 16-bit 1: 24-bit

11220070 **AFE_AWB_BASE** **AFE AWB Base Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_AWB_BASE[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_AWB_BASE[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:3	AFE_AWB_BASE	**Base address of AWB input in master mode** Always set AFE_AWB_BASE[2:0] = 3'h0 for the convenience of HW implementation.

11220078 **AFE_AWB_END** **AFE AWB End Address Register** **00000007**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**AFE_AWB_END[28:13]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AFE_AWB_END[12:0]**													**AFE_AWB_END_LSB**		
Type	RW													RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Name	Description
31:3	AFE_AWB_END	**End address of AWB input in master mode** Always set AFE_AWB_END[2:0] = 3'h7 for the convenience of HW implementation.
2:0	AFE_AWB_END_LSB	

1122007C **AFE_AWB_CUR** **AFE AWB Cursor Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**AFE_AWB_CUR[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AFE_AWB_CUR[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AFE_AWB_CUR	Indicates the current address of the AWB input buffer

11220080 **AFE_VUL_BASE** **AFE VUL Base Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**AFE_VUL_BASE[28:13]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AFE_VUL_BASE[12:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:3	AFE_VUL_BASE	**Base address of VUL input in master mode** Always set AFE_VUL_BASE[2:0] = 3'h0 for the convenience of HW implementation.

11220088 AFE_VUL_END AFE VUL End Address Register 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_VUL_END[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_VUL_END[12:0]													AFE_VUL_END_LSB		
Type	RW													RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Name	Description
31:3	AFE_VUL_END	**End address of the VUL input in master mode** Always set AFE_VUL_END[2:0] = 3'h7 for the convenience of HW implementation.
2:0	AFE_VUL_END_LSB	

1122008C AFE_VUL_CUR AFE VUL Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_VUL_CUR[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_VUL_CUR[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AFE_VUL_CUR	Indicates the current address of the VUL input buffer

11220090 AFE_DAI_BASE AFE DAI Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DAI_BASE[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DAI_BASE[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:3	AFE_DAI_BASE	**Base address of DAI input in master mode** Always set AFE_DAI_BASE[2:0] = 3'h0 for the convenience of HW implementation.

11220098 AFE_DAI_END AFE_DAI_END 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DAI_END[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DAI_END[12:0]													AFE_DAI_END_LSB		
Type	RW													RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Name	Description
31:3	AFE_DAI_END	**End address of the DAI input in master mode** Always set AFE_DAI_END[2:0] = 3'h7 for the convenience of HW implementation.
2:0	AFE_DAI_END_LSB	

1122009C AFE_DAI_CUR AFE DAI Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DAI_CUR[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DAI_CUR[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AFE_DAI_CUR	Indicates the current address of the DAI input buffer

112200BC AFE_CONN6 AFE Connection Register 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			I09_O24_S	I09_O23_S			I09_O25_S	I03_O25_S			I21_O12_S	I21_O10_S	I21_O08_S	I21_O07_S	I21_O06_S	I21_O04_S
Type			RW	RW			RW	RW			RW	RW	RW	RW	RW	RW
Reset			0	0			0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I21_O03_S	I21_O02_S	I21_O01_S	I21_O00_S			I04_O24_S			I03_O23_S						
Type	RW	RW	RW	RW			RW			RW						
Reset	0	0	0	0			0			0						

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Bit(s)	Name	Description
29	I09_O24_S	**Controls the path from I09 to O24** 0: Off 1: On
28	I09_O23_S	**Controls the path from I09 to O23** 0: Off 1: On
25	I09_O25_S	**Controls the path from I09 to O25** 0: Off 1: On
24	I03_O25_S	**Controls the path from I03 to O25** 0: Off 1: On
21	I21_O12_S	**Controls the path from I21 to O12** 0: Off 1: On
20	I21_O10_S	**Controls the path from I21 to O10** 0: Off 1: On
19	I21_O08_S	**Controls the path from I21 to O08** 0: Off 1: On
18	I21_O07_S	**Controls the path from I21 to O07** 0: Off 1: On
17	I21_O06_S	**Controls the path from I21 to O06** 0: Off 1: On
16	I21_O04_S	**Controls the path from I21 to O04.** 0: Off 1: On
15	I21_O03_S	**Controls the path from I21 to O03** 0: Off 1: On
14	I21_O02_S	**Controls the path from I21 to O02** 0: Off 1: On
13	I21_O01_S	**Controls the path from I21 to O01** 0: Off 1: On
12	I21_O00_S	**Controls the path from I21 to O00** 0: Off 1: On
9	I04_O24_S	**Controls the path from I04 to O24** 0: Off 1: On
6	I03_O23_S	**Controls the path from I03 to O23** 0: Off 1: On

112200CC AFE_MEMIF AFE Memory Interface MSB Register 003F0000

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MSB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											VUL2_AXI_WR_SIGN	VUL_AXI_WR_SIGN	DAI_AXI_WR_SIGN	MOD_DAI_AXI_WR_SIGN	AWB_MSTR_SIGN	SYSRAM_SIGN
Type											RW	RW	RW	RW	RW	RW
Reset											1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									VUL2_data2_MSB	VUL_MSB	DAI_MSB	MOD_DAI_MSB	AWB_MSB	DL1_data2_MSB	DL2_MSB	DL1_MSB
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21	VUL2_AXI_WR_SIGN	**Signed extension 24-bit data to 32-bit for VUL2 memory agent** 0: Append 0 1: bit[23] signed extension
20	VUL_AXI_WR_SIGN	**Signed extension 24-bit data to 32-bit for VUL memory agent** 0: Append 0 1: bit[23] signed extension
19	DAI_AXI_WR_SIGN	**Signed extension 24-bit data to 32-bit for DAI memory agent** 0: Append 0 1: bit[23] signed extension
18	MOD_DAI_AXI_WR_SIGN	**Signed extension 24-bit data to 32-bit for MOD_DAI memory agent** 0: Append 0 1: bit[23] signed extension
17	AWB_MSTR_SIGN	**Signed extension 24-bit data to 32-bit for AWB memory agent** 0: Append 0 1: bit[23] signed extension
16	SYSRAM_SIGN	**Signed extension 24-bit data to 32-bit for bus read SYSRAM** 0: Append 0 1: bit[23] signed extension
7	VUL2_data2_MSB	**Indicates the MSB (bit33) of VUL2 memory address**
6	VUL_MSB	**Indicates the MSB (bit33) of VUL memory address**
5	DAI_MSB	**Indicates the MSB (bit33) of DAI memory address**
4	MOD_DAI_MSB	**Indicates the MSB (bit33) of MOD_DAI memory address**
3	AWB_MSB	**Indicates the MSB (bit33) of AWB memory address**
2	DL1_data2_MSB	**Indicates the MSB (bit33) of DL1_2 memory address**
1	DL2_MSB	**Indicates the MSB (bit33) of DL2 memory address**
0	DL1_MSB	**Indicates the MSB (bit33) of DL1 memory address**

112200D0 **AFE_MEMIF_MON0** **AFE Memory Interface Monitor Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DL1_RCH_DATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DL1_LCH_DATA															

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Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	DL1_RCH_DATA	Memory interface DL1 right channel data output.
15:0	DL1_LCH_DATA	Memory interface DL1 left channel data output.

112200D4 AFE_MEMIF_MON1 AFE Memory Interface Monitor Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DL2_RCH_DATA**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DL2_LCH_DATA**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	DL2_RCH_DATA	Memory interface DL2 right channel data output.
15:0	DL2_LCH_DATA	Memory interface DL2 left channel data output.

112200D8 AFE_MEMIF_MON2 AFE Memory Interface Monitor Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**VUL_RCH_DATA**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DAI_DATA**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	VUL_RCH_DATA	Memory interface VUL right channel data input.
15:0	DAI_DATA	Memory interface DAI data input.

112200E0 AFE_MEMIF_MON4 AFE Memory Interface Monitor Register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**AWB_RCH_DATA**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AWB_LCH_DATA**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:16	AWB_RCH_DATA	Memory interface AWB right channel data input.
15:0	AWB_LCH_DATA	Memory interface AWB left channel data input.

11220108 **AFE_ADDA_DL_SRC2_CON0** **AFE_DL_SRC2 Control Register 0** **0F000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dl_2_input_mode_ctl				dl_2_ch1_saturation_en_ctl	dl_2_ch2_saturation_en_ctl	dl_2_output_sel_ctl								dl_2_fadein_ostart_en	
Type	RW				RW	RW	RW								RW	
Reset	0	0	0	0	1	1	1	1							0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		c_data_en_sel_ctl_pre	dl_2_sidetone_on_ctl_pre	dl_2_mute_ch1_off_ctl_pre	dl_2_mute_ch2_off_ctl_pre	dl2_aramps_ctl_pre		dl_2_iirmode_ctl_pre			dl_2_voice_mode_ctl_pre	d2_2_mute_ch1_on_ctl_pre	d2_2_mute_ch2_on_ctl_pre	dl_2_iir_on_ctl_pre	dl_2_gain_on_ctl_pre	dl_2_src_on_tmp_ctl_pre
Type		RW	RW	RW	RW	RW		RW			RW	RW	RW	RW	RW	RW
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	dl_2_input_mode_ctl	**Selects input sampling rate of down-link** 0: 8k 1: 11.025k 2: 12k 3: 16k 4: 22.05k 5: 24k 6: 32k 7: 44.1k 8: 48k Others: 8k
27	dl_2_ch1_saturation_en_ctl	**Saturates input signal into -1~1-1LSB (origin: -8~8-1lsb)**
26	dl_2_ch2_saturation_en_ctl	**Saturates input signal into -1~1-1LSB (origin: -8~8-1lsb)**
25:24	dl_2_output_sel_ctl	**Selects output mode of down-link** 0: x1 of up-sample rate 1: x2 of up-sample rate 2: x4 of up-sample rate 3: x8 of up-sample rate
17:16	dl_2_fadein_ostart_en	**When [12:11]=0 (mute_off=0 means mute function enabled), the test method should be** 2-1 [12:11]=0 and [4:3]=0 (fade-in), then [17:16]=2'b11 to trigger fade-in start at 0 gain. To trigger, write [17:16]=2'b00 then [17:16]=2'b11. *Note: Each on/off of bit[17:16] should be seperated by time interval > 1/FS.* *2-2 test 2-1 but setup [4:3]=2'b11 (fade-out) and the fade-out procedure should not be affected.* 00: Disable ch1 and ch2 fadein from 0 11: Enable ch1 and ch2 fadein from 0
14	c_data_en_sel_ctl_pr	Default: 0

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Bit(s)	Name	Description
	e	DL output rate: 8x Otherwise, the output rate is decided by AFE_DL_SRC2_CON0_H[9: 8]
13	dl_2_side_tone_on_ctl_pre	**Turns on side-tone filter from up-link path** Reserved bit
12	dl_2_mute_ch1_off_ctl_pre	**Turns off mute function in channel1** 0: Turn on mute function 1: Turn off mute function
11	dl_2_mute_ch2_off_ctl_pre	**Turns off mute function in channel2** 0: Turn on mute function 1: Turn off mute function
10:9	dl2_arampsp_ctl_pre	**Speed of mute function to zero out** 0: Gain speed = 0.00025 per sample (total 4,096 samples) 1: Gain speed = 0.0005 per sample (total 2,048 samples) 2: Gain speed = 0.001 per sample (total 1,024 samples) 3: Gain speed = 0.002 per sample (total 512 samples)
8:6	dl_2_iirmode_ctl_pre	**Selects band of IIR DC-removal filter** 0: 4k: 90Hz, 8k: 180Hz 1: 4k: 160Hz, 8k: 320Hz 2: 4k: 200Hz, 8k: 400Hz 3: 4k: 250Hz, 8k: 500Hz 4: 16k: 100Hz
5	dl_2_voice_mode_ctl_pre	**Selects voice input** 0: Audio data 1: Voice data (small group delay and only enable 8k/16kHz)
4	d2_2_mute_ch1_on_ctl_pre	0: Mute up (back to gain = 1) 1: Mute down
3	d2_2_mute_ch2_on_ctl_pre	0: Mute up (back to gain = 1) 1: Mute down
2	dl_2_iir_on_ctl_pre	**Turns on DC_removal function**
1	dl_2_gain_on_ctl_pre	**Turns on degrade gain function**
0	dl_2_src_on_tmp_ctl_pre	**Turns on down-link**

1122010C **AFE_ADDA_DL_SRC2_CON1** **AFE_DL_SRC2 Control Register 1 Part** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dl_2_gain_ctl_pre															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																dl_2_gain_mode_ctl
Type																RW
Reset																0

Bit(s)	Name	Description
31:16	dl_2_gain_ctl_pre	**Gain of degrade gain stage [1, 0] = [FFFF, 0]**
0	dl_2_gain_mode_ctl	**Down link gain formatting** 0: gain_to_mac = [2:0:16] (suggested) 1: gain_to_mac = {[1:0:16],1'b0}

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11220114	AFE_ADDA_UL_SRC_CON0	AFE Uplink SRC Control Register 0 Part	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	c_comb_out_sin_gen_ctl	c_baseband_sin_gen_ctl	c_digmic_phase_sel_ch1_ctl			c_digmic_phase_sel_ch2_ctl			c_two_digital_mic_ctl	ul_mode_3p25m_ch2_ctl	ul_mode_3p25m_ch1_ctl	ul_voice_mode_ch2_ctl		ul_voice_mode_ch1_ctl		
Type	RW	RW	RW			RW			RW	RW	RW	RW		RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						ul_iir_on_tmp_ctl	ul_iirmode_ctl				digmic_3p25m_1p625m_sel_ctl	agc_260k_sel_ch2_ctl	agc_260k_sel_ch1_ctl	ul_loop_back_mode_ctl	ul_sdm_3_level_ctl	ul_src_on_tmp_ctl
Type						RW	RW				RW	RW	RW	RW	RW	RW
Reset						0	0	0	0		0	0	0	0	0	0

Bit(s)	Name	Description
31	c_comb_out_sin_gen_ctl	**Mux for uplink comb filter output to uDSP** 0: Uplink comb filter data path output 1: Sine table output
30	c_baseband_sin_gen_ctl	**Mux for the uplink SRC output to interconnections.** Reserved 0: Uplink SRC data path output 1: Sine table output
29:27	c_digmic_phase_sel_ch1_ctl	**Selects 8 input phase latch.** Reserved
26:24	c_digmic_phase_sel_ch2_ctl	**Selects 8 input phase latch.** Reserved
23	c_two_digital_mic_ctl	**Turns on dual digital microphones mode.** Reserved 0: Turn off 1: Turn on
22	ul_mode_3p25m_ch2_ctl	**Turns on digital microphone for channel 2. The input mode is 3.25MHz sampling rate.** Reserved 0: Turn off 1: Turn on
21	ul_mode_3p25m_ch1_ctl	**Turns on digital microphone for channel 1. The input mode is 3.25MHz sampling rate** Reserved 0: Turn off 1: Turn on
20:19	ul_voice_mode_ch2_ctl	**Selects voice mode of channel 2** 00b: 8kHz mode 01b: 16kHz mode 10b: 32kHz mode 11b: 48kHz mode
18:17	ul_voice_mode_ch1_ctl	**Selects voice mode of channel 1** 00b: 8kHz mode 01b: 16kHz mode 10b: 32kHz mode

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Bit(s)	Name	Description
		11b: 48kHz mode
10	ul_iir_on_tmp_ctl	**Turns on IIR DC removal filter** 0: Turn off 1: Turn on
9:7	ul_iirmode_ctl	**Selects stop band of IIR DC-removal filter** 000b: 90Hz if 8kHz mode; 180Hz if 16kHz mode 001b: 160Hz if 8kHz mode; 320Hz if 16kHz mode 010b: 200Hz if 8kHz mode; 400Hz if 16kHz mode 011b: 320Hz if 8kHz mode; 640Hz if 16kHz mode 100b: 100Hz if 16kHz mode
5	digmic_3p25m_1p625m_sel_ctl	**digmic input mode** 0: 325M mode 1: 1625M mode
4	agc_260k_sel_ch2_ctl	**Replaces the original raw data with AGC computed one at 260kHz in channel 2.** Reserved bit 0: Does not replace the original raw data 1: Replace the original raw data
3	agc_260k_sel_ch1_ctl	**Replaces the original raw data with AGC computed one at 260kHz in channel 1.** Reserved bit 0: Does not replace the original raw data 1: Replace the original raw data
2	ul_loop_back_mode_ctl	**Uplink input is from the downlink output.** The 2nd-priority choice 0: De-select loopback mode 1: Select loopback mode from downlink SDM
1	ul_sdm_3_level_ctl	**Selects SDM 3-level mode. (digital MIC data path), first priority choice** 0: De-select SDM 3-level mode 1: Select SDM 3-level mode
0	ul_src_on_tmp_ctl	**Turns on uplink SRC** 0: Turn off 1: Turn on

11220118 **AFE_ADDA_UL_SRC_CON1** **AFE Uplink SRC Control Register 1 Part** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	c_sdm_reset_ctl	adithon_ctl	adithval_ctl		c_dac_en_ctl	c_mute_sw_ctl	asdm_src_sel_ctl		c_amp_div_ch2_ctl			c_freq_div_ch2_ctl				
Type	RW	RW	RW		RW	RW	RW		RW			RW				
Reset	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c_sine_mode_ch2_ctl				c_amp_div_ch1_ctl			c_freq_div_ch1_ctl					c_sine_mode_ch1_ctl			
Type	RW				RW			RW					RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	c_sdm_reset_ctl	**Software reset of FPGA SDM.** Reserved bit 0: No reset

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Bit(s)	Name	Description
		1: Reset
30	adithon_ctl	**Turns on dither in FPGA SDM.** Reserved bit 0: Turn off 1: Turn on
29:28	adithval_ctl	**Sets up value of dither in FPGA SDM.** Reserved bit
27	c_dac_en_ctl	**Mux for uplink comb filter output to uDSP** 0: Uplink comb filter data path output 1: Sine table output
26	c_mute_sw_ctl	**Mute switch (SGEN)** 0: Turn on the sine wave output in this test mode 1: Mute the sine wave output
25	asdm_src_sel_ctl	**DAC SDM Tri-angular generator testing path (TSGEN)** 0: Normal path 1: Triangular tone
23:21	c_amp_div_ch2_ctl	**Amplitude setting of channel 2 (SGEN)** 000b: 1/128 full scale 001b: 1/64 full scale 010b: 1/32 full scale 011b: 1/16 full scale 100b: 1/8 full scale 101b: 1/4 full scale 110b: 1/2 full scale 111b: full scale
20:16	c_freq_div_ch2_ctl	**Frequency setting of channel 2.** 1X ~ 15X for voice, 1X ~ 31X for audio. Frequency = Sampling rate/64*FREQ_DIV (SGEN)
15:12	c_sine_mode_ch2_ctl	**Selects input mode of sine table of channel 2 (SGEN)** 0: 8k 1: 11.025k 2: 12k 3: 16k 4: 22.05k 5: 24k 6: 32k 7: 44.1k 8~15: 48k
11:9	c_amp_div_ch1_ctl	**Amplitude setting of channel 1 (SGEN)** 000b: 1/128 full scale 001b: 1/64 full scale 010b: 1/32 full scale 011b: 1/16 full scale 100b: 1/8 full scale 101b: 1/4 full scale 110b: 1/2 full scale 111b: Full scale
8:4	c_freq_div_ch1_ctl	**Frequency setting of channel 1** 1X ~ 15X for voice, 1X ~ 31X for audio. Frequency = Sampling rate/64*FREQ_DIV (SGEN)
3:0	c_sine_mode_ch1_ctl	**Select the input mode of sine table of channel 1 (SGEN)** 0: 8k 1: 11.025k 2: 12k 3: 16k 4: 22.05k

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Bit(s)	Name	Description
		5: 24k 6: 32k 7: 44.1k 8~15: 48k

11220120 **AFE_ADDA_TOP_CON0** **AFE Top Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c_loop_back_mode_ctl															c_ext_adc_ctl
Type	RW															RW
Reset	0	0	0	0												0

Bit(s)	Name	Description
15:12	c_loop_back_mode_ctl	**Built-in loop-back test mode** 0: Normal path from analog input path 2: Built-in sine table for UL-I2S-FIFO input (1st priority) 1: DL-I2S-FIFO output to UL-I2S input (2nd priority) 4: Down-link input from built-in sine table
0	c_ext_adc_ctl	**I_03/I_04 source from internal/external ADC** 0: Internal ADC output selection 1: External ADC output selection

11220124 **AFE_ADDA_UL_DL_CON0** **Audio UL and DL Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		afe_ul_dl_con0_reserved														adda_afe_on
Type		RW														RW
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:1	afe_ul_dl_con0_reserved	
0	adda_afe_on	**Enables ADDA total (synced with 26M)** 0: Disable ADDA interface 1: Enable ADDA interface

1122012C **AFE_ADDA_SRC_DEBUG** **AFE UL Debug Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				ul_slt_cnt_flag_reset_ctl		slt_cnt_thd_ctl										
Type				RW		RW										

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Reset				0		0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**dl_slt_cnt_flag_reset_ctl**	**dl_slt_cnt_thd_ctl**											
Type				RW	RW											
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	ul_slt_cnt_flag_reset_ctl	**Resets SLT_CNT_FLAG when SLT_CNT < SLT_CNT_THD** 0: Does not reset slt_cnt_flag of UL 1: Reset slt_cnt_flag of UL
26:16	slt_cnt_thd_ctl	**slt_cnt_thd threshold** ul state machine slt_cnt threshold
12	dl_slt_cnt_flag_reset_ctl	**Resets SLT_CNT_FLAG when SLT_CNT < SLT_CNT_THD** 0: Does not reset slt_cnt_flag of DL 1: Reset slt_cnt_flag of DL
11:0	dl_slt_cnt_thd_ctl	**slt_cnt_thd threshold** dl state machine slt_cnt threshold

11220130 **AFE_ADDA_SRC_DEBUG_MON0** **AFE Uplink SRC Monitor Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**slt_cnt_flag_ctl**		**slt_counter_ctl**										
Type				RU		RU										
Reset				0		0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**dl_slt_cnt_flag_ctl**			**dl_ini_sram_finish_ctl**	**dl_slt_counter_ctl**											
Type	RU			RU	RU											
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	slt_cnt_flag_ctl	
26:16	slt_counter_ctl	
15	dl_slt_cnt_flag_ctl	
12	dl_ini_sram_finish_ctl	
11:0	dl_slt_counter_ctl	

11220134 **AFE_ADDA_SRC_DEBUG_MON1** **AFE Downlink SRC Monitor Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													dlsatflag			
Type													RU			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	dlsatflag	[3] pos_sat_ch1 [2] neg_sat_ch1 [1] pos_sat_ch2 [0] neg_sat_ch2

112201D0 AFE_SIDETONE_DEBUG Side-tone Debug 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													STF_PRETEND_AS_I5I6_DL1	STF_SRC_SEL		
Type													RW	RW		
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				SLT_CNT_FLAG_RESET		SLT_CNT_THD										
Type				RW		RW										
Reset				0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	STF_PRETEND_AS_I5I6_DL1	**STF output to I_05/I_06 for debugging** 0: Normal I_05/I_06 function 1: STF output pretends as I_05/I_06 sources
18:16	STF_SRC_SEL	**Selects STF input source** 1: Sine generator 2: DL1 L and R from memory 3: I_03/I_04 (ADC I2S IN) 4: I_17/I_48 (ADC I2S IN 2) Others: From ADDA VUL channel out
12	SLT_CNT_FLAG_RESET	**Resets SLT_CNT_FLAG when SLT_CNT < SLT_CNT_THD** 0: Does not reset slt_cnt_flag 1: Reset slt_cnt_flag
10:0	SLT_CNT_THD	**slt_cnt_thd threshold** STF state machine slt_cnt threshold

112201D4 AFE_SIDETONE_MON Side-tone Debug Monitor 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

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Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**SLT_CNT_FLAG**		**SLT_CNT**										
Type				RU		RU										
Reset				0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12	SLT_CNT_FLAG	**Resets SLT_CNT_FLAG when SLT_CNT > SLT_CNT_THD** 0: slt_cnt >= SLT_CNT_THD 1: slt_cnt < SLT_CNT_THD
10:0	SLT_CNT	**STF state machine slt_cnt counted by fixed 26MHz between two consecutive input timings**

112201E0 **AFE_SIDETONE_CON0** **Side-tone Control Port 0** **02000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**R_RDY**	**W_RDY**				**R_W_EN**	**R_W_SEL**	**SEL_CH2**			**SIDE_TONE_COEFFICIENT_ADDR**				
Type		RU	RU				RW	RW	RW			RW				
Reset		0	0				1	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SIDE_TONE_COEFFICIENT**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30	R_RDY	**Read ready** If it is different from the value which is recorded before you assign a read address, read out the side tone coefficient with address specified ahead. 0: Ready/not ready 1: Ready/not ready
29	W_RDY	**Write ready** If it is different from the value which is recorded before the first written coefficient, write the "next" side tone coefficient. 0: Ready/not ready 1: Ready/not ready
25	R_W_EN	**Enables read/write** 0: Disable 1: Enable
24	R_W_SEL	**Reads or writes coefficients** 0: Read 1: Write
23	SEL_CH2	**Selects STF (side tone filter) input source** 0: Uplink I2S CH1 as STF input 1: Uplink i2s CH2 as STF input
20:16	SIDE_TONE_COEFFICIENT_ADDR	**Controls coefficient SRAM address access** For example, if address 0x00 has coefficient 0x1234, this field should be filled 0x00 and [15:0] filled 0x1234.
15:0	SIDE_TONE_COEFFICIENT	**Coefficient of the side tone filter** In 2's complement. The Q-format is 1.15.

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112201E4 **AFE_SIDETONE_COEFF** **Side-tone coefficient Port** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIDE_TONE_COEFF															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SIDE_TONE_COEFF	Reads out side tone coefficients

112201E8 **AFE_SIDETONE_CON1** **Side-tone Control Port 1** **0000001F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STF_BYPASS_MODE															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								SIDE_TONE_ON			SIDE_TONE_HALF_TAP_NUM					
Type								RW			RW					
Reset								0			0	1	1	1	1	1

Bit(s)	Name	Description
31	STF_BYPASS_MODE	**STF bypass mode** 0: Use STF result adding into I2S_OUT0 1: Bypass STF result
8	SIDE_TONE_ON	**STF enabling bit** 0: Disable STF 1: Enable STF
5:0	SIDE_TONE_HALF_TAP_NUM	**Number of half Nth taps for every symmetry** Example: SIDE_TONE_HALF_TAP_NUM[5:0] = 13 if taps number used = 26.

112201EC **AFE_SIDETONE_GAIN** **Side-tone Gain Port** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIDE_TONE_GAIN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	SIDE_TONE_GAIN	**Gain of side tone filter** In 2's complement. The Q-format is 1.15.

112201F0 **AFE_SGEN_CON0** **AFE Sine-wave Gen Config 0** **F0000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INNER_LOOP_BACK_MODE				IN_OUT_SEL	dac_en	mute_sw_ch2	mute_sw_ch1	sine_mode_ch2				amp_div_ch2			freq_div_ch2[4:4]
Type	RW				RW	RW	RW	RW	RW				RW			RW
Reset	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	freq_div_ch2[3:0]				sine_mode_ch1				amp_div_ch1				freq_div_ch1			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	INNER_LOOP_BACK_MODE	**Loopback mode testing for audio_conn** Valid when SINE_MODE_CH1 > 8 for sinewave gen ch1 and SINE_MODE_CH2 > 8 for sinewave gen ch2. 0: in_en[00], i_00, i_01 use sin_ch1 and sin_ch2 as input source (when bit[27] is set to 1'b0) 1: in_en[02], i_02 use sin_ch1 input source 2: in_en[03], i_03, i_04 use sin_ch1 and sin_ch2 as input source 3: in_en[05], i_05, i_06 use sin_ch1 and sin_ch2 as input source (if 0x1d0[19]=0) 4: in_en[07], i_07, i_08 use sin_ch1 and sin_ch2 as input source 5: in_en[09], i_09 use sin_ch1 6: in_en[10], i_10, i_11 use sin_ch1 and sin_ch2 as input source 7: in_en[12], i_12, i_13 use sin_ch1 and sin_ch2 as input source 8: in_en[14], i_14 use sin_ch1 9: in_en[15], i_15, i_16 use sin_ch1 and sin_ch2 as input source 10: in_en[17], i_17, i_18 use sin_ch1 and sin_ch2 as input source 11: in_en[19], i_19, i_20 use sin_ch1 and sin_ch2 as input source 12: in_en[21], i_21, i_22 use sin_ch1 and sin_ch2 as input source 0: out_en[00], o_00, o_01 use sin_ch1 and sin_ch2 as input source (when bit[27] is set to 1'b0) 1: out_en[02], o_02 use sin_ch1 as input source 2: out_en[03], o_03, o_04 use sin_ch1 and sin_ch2 as input source 3: out_en[05], o_05, o_06 use sin_ch1 and sin_ch2 as input source 4: out_en[07], o_07, o_08 use sin_ch1 and sin_ch2 5: out_en[09], o_09, o_10 use sin_ch1 and sin_ch2 as input source 6: out_en[11], o_11 use sin_ch1 as input source 7: out_en[12], o_12 use sin_ch1 as input source 8: out_en[13], o_13, o_14 use sin_ch1 and sin_ch2 as input source 9: out_en[15], o_15, o_16 use sin_ch1 and sin_ch2 as input source 10: out_en[17], o_17, o_18 use sin_ch1 and sin_ch2 as input source 11: out_en[19], o_19, o_20 use sin_ch1 and sin_ch2 as input source 12: out_en[21], o_21, o_22 use sin_ch1 and sin_ch2 as input source 13: out_en[23], o_23, o_24 use sin_ch1 and sin_ch2 as input source 14: out_en[25], o_25 use sin_ch1
27	IN_OUT_SEL	**Selects sinewave to input/output** 0: Input 1: Output
26	dac_en	**Enables sinewave generator**

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Bit(s)	Name	Description
		0: Disable sigen 1: Enable sigen
25	mute_sw_ch2	**Sinewave generator mute for ch2** 0: Unmute sigen 1: Mute sigen
24	mute_sw_ch1	**Sinewave generator mute for ch1** 0: Unmute sigen 1: Mute sigen
23:20	sine_mode_ch2	**Enables sinewave generator timing selection for ch2** 0: 8k 1: 11.025k 2: 12k 4: 16k 5: 22.05k 6: 24k 8: 32k 9: 44.1k 10: 48k 11: 88.2k 12: 96k 13: 176.4k 14: 192k
19:17	amp_div_ch2	**Selects sinewave generator amplitude for ch2** 0: sinewave_out/128 1: sinewave_out/64 2: sinewave_out/32 3: sinewave_out/16 4: sinewave_out/8 5: sinewave_out/4 6: sinewave_out/2 7: sinewave_out/1
16:12	freq_div_ch2	**Selects sinewave generator frequency for ch2 sampled by signal timing generator selection bit[23:20] (or bit[31:28]) for ch2** 0: DC output 1: 64/1 samples/period 2: 64/2 samples/period 3: 64/3 samples/period 4: 64/4 samples/period 5: 64/5 samples/period 6: 64/6 samples/period x: 64/x samples/period 31: 64/31 samples/period
11:8	sine_mode_ch1	**Enables sinewave generator timing selection for ch1** 0: 8k 1: 11.025k 2: 12k 4: 16k 5: 22.05k 6: 24k 8: 32k 9: 44.1k 10: 48k 11: 88.2k 12: 96k 13: 176.4k 14: 192k
7:5	amp_div_ch1	**Selects sinewave generator amplitude for ch1** 0: sinewave_out/128 1: sinewave_out/64

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Bit(s)	Name	Description
		2: sinewave_out/32 3: sinewave_out/16 4: sinewave_out/8 5: sinewave_out/4 6: sinewave_out/2 7: sinewave_out/1
4:0	freq_div_ch1	**Selects sinewave generator frequency for ch2 sampled by signal timing generator selection bit[23:20] (or bit[31:28]) for ch1** 0: DC output 1: 64/1 samples/period 2: 64/2 samples/period 3: 64/3 samples/period 4: 64/4 samples/period 5: 64/5 samples/period 6: 64/6 samples/period x: 64/x samples/period 31: 64/31 samples/period

11220200 **AFE_TOP_CON0** **AFE Top Control Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LOOP_BACK_MODE															
Type	RW															
Reset	0	0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31:28	LOOP_BACK_MODE	**Specifies loop back mode** 0: Normal mode 1: Sine tone output of ch1 to i_05, sine tone output of ch2 to i_06 2: Sine tone output of ch1 to i_07, sine tone output of ch2 to i_08 4: Sine tone output of ch1 to src_B ch1, sine tone output of ch2 to src_B ch2 6: Uplink left channel output to src_B ch1, uplink right channel output to src_B ch2

11220260 **AFE_ADDA_PREDIS_CON0** **AFE Pre-distortion Control Port 0 High Part** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	predis_on_ch1_ctl				predis_a2_ch1_ctl											
Type	RW				RW											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					predis_a3_ch1_ctl											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31	predis_on_ch1_ctl	Down-link pre-distortion on for ch1
27:16	predis_a2_ch1_ctl	Pre-distortion coefficient a2 for ch1
11:0	predis_a3_ch1_ctl	Pre-distortion coefficient a3 for ch1

11220264 **AFE_ADDA_PREDIS_CON1** **AFE Pre-distortion Control Port 1 High Part** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	predis_on_ch2_ctl				predis_a2_ch2_ctl											
Type	RW				RW											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					predis_a3_ch2_ctl											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	predis_on_ch2_ctl	Down-link pre-distortion on for ch2
27:16	predis_a2_ch2_ctl	Pre-distortion coefficient a2 for ch2
11:0	predis_a3_ch2_ctl	Pre-distortion coefficient a3 for ch2

11220270 **AFE_MRGIF_MON0** **AFE Merge Interface Monitor Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MRGIF_I2S_RCH_CNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	MRGIF_I2S_RCH_CNT	Indicates PCM Rx FIFO is overflow

11220274 **AFE_MRGIF_MON1** **AFE Merge Interface Monitor Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MRGIF_I2S_LCH_CNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	MRGIF_I2S_LCH_CNT	**Receive data's monitor counter of I2S's right channel** When data 0 is received, this counter will be not increased.

11220278 AFE_MRGIF_MON2 AFE Merge Interface Monitor Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															MRGIF_PCM_RX_OVF	MRGIF_PCM_RX_UNF
Type															RU	RU
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MRGIF_PCM_CNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	MRGIF_PCM_RX_OVF	**Indicates PCM Rx FIFO is underflow**
16	MRGIF_PCM_RX_UNF	**Receive data's monitor counter of PCM** When data 0 is received, this counter will be not increased.
15:0	MRGIF_PCM_CNT	**MRGIF_PCM_CNT**

11220330 AFE_MOD_DAI_BASE AFE MOD_DAI Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_MOD_DAI_BASE[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_MOD_DAI_BASE[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	AFE_MOD_DAI_BASE	**Base address of MOD_DAI input in master mode** Always set AFE_MOD_DAI_BASE[2:0] = 3'h0 for the convenience of HW implementation.

11220338 AFE_MOD_DAI_END AFE_MOD_DAI_END 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_MOD_DAI_END[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_MOD_DAI_END[12:0]													AFE_MOD_DAI_END_LSB		
Type	RW													RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Name	Description
31:3	AFE_MOD_DAI_END	**End address of MOD_DAI input in master mode** Always set AFE_MOD_DAI_END[2:0] = 3'h7 for the convenience of HW implementation.
2:0	AFE_MOD_DAI_END_LSB	

1122033C AFE_MOD_DAI_CUR AFE MOD_DAI Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_MOD_DAI_CUR[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_MOD_DAI_CUR[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AFE_MOD_DAI_CUR	Indicates the current address of the MOD_DAI input buffer

112203A0 AFE_IRQ_MCU_CON AFE IRQ MCU Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					IRQ7_MCU_MODE											
Type					RW											
Reset					0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		IRQ7_MCU_ON			IRQ2_MCU_MODE				IRQ1_MCU_MODE						IRQ2_MCU_ON	IRQ1_MCU_ON
Type		RW			RW				RW						RW	RW
Reset		0			0	0	0	0	0	0	0	0			0	0

Bit(s)	Name	Description
27:24	IRQ7_MCU_MODE	**Controls the IRQ7_MCU count unit** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 0111b: 130k 1000b: 32k 1001b: 44.1k 1010b: 48k

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Bit(s)	Name	Description
		1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k 1111b: 260k
14	IRQ7_MCU_ON	**Controls the enabling of IRQ7_MCU** 0: Off 1: On
11:8	IRQ2_MCU_MODE	**Controls the IRQ2_MCU count unit** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k
7:4	IRQ1_MCU_MODE	**Controls the IRQ1_MCU count unit** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k
1	IRQ2_MCU_ON	**Controls the enabling of IRQ2_MCU** 0: Off 1: On
0	IRQ1_MCU_ON	**Controls the enabling of IRQ1_MCU** 0: Off 1: On

112203A4 **AFE_IRQ_MCU_STATUS** **AFE IRQ MCU Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										IRQ7_MCU					IRQ2_MCU	IRQ1_MCU
Type										RU					RU	RU
Reset										0					0	0

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Bit(s)	Name	Description
6	IRQ7_MCU	**Reads the status for IRQ7_MCU (I2S)** 0: No interrupt 1: IRQ7 interrupt
1	IRQ2_MCU	**Reads the status for IRQ2_MCU (I2S)** 0: No interrupt 1: IRQ2 interrupt
0	IRQ1_MCU	**Reads the status for IRQ1_MCU (VUL/DL1/DL2/AWB)** 0: No interrupt 1: IRQ1 interrupt

112203A8 **AFE_IRQ_MCU_CLR** **AFE IRQ Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		IRQ7_MCU_MISS_CLR					IRQ2_MCU_MISS_CLR	IRQ1_MCU_MISS_CLR		IRQ7_MCU_CLR					IRQ2_MCU_CLR	IRQ1_MCU_CLR
Type		WO					WO	WO		WO					WO	WO
Reset		0					0	0		0					0	0

Bit(s)	Name	Description
14	IRQ7_MCU_MISS_CLR	**Clears the status of IRQ7 miss flag** 0: No operation 1: Clear IRQ7 miss flag
9	IRQ2_MCU_MISS_CLR	**Clears the status of IRQ2 miss flag** 0: No operation 1: Clear IRQ2 miss flag
8	IRQ1_MCU_MISS_CLR	**Clears the status of IRQ1 miss flag** 0: No operation 1: Clear IRQ1 miss flag
6	IRQ7_MCU_CLR	**Clears the status for IRQ7_MCU.** 0: No operation 1: Clear IRQ7 Interrupt
1	IRQ2_MCU_CLR	**Clears the status for IRQ2_MCU.** 0: No operation 1: Clear IRQ2 interrupt
0	IRQ1_MCU_CLR	**Clears the status for IRQ1_MCU.** 0: No operation 1: Clear IRQ1 interrupt

112203AC **AFE_IRQ_MCU_CNT1** **AFE IRQ1 MCU Counter Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AFE_IRQ_MCU_CNT1[17:16]	

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Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AFE_IRQ_MCU_CNT1[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:0	AFE_IRQ_MCU_CNT1	**Sets up the counter value for IRQ1 according to IRQ1_MODE** The IRQ1 counter in AFE will count down from AFE_IRQ_MCU_CNT1 and set up IRQ1 while IRQ1 counter reaches 1. Therefore, the maximum IRQ time for IRQ1 at 48kHz mode is 5s.

112203B0 AFE_IRQ_MCU_CNT2 AFE IRQ2 MCU Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															**AFE_IRQ_MCU_CNT2[17:16]**	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AFE_IRQ_MCU_CNT2[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:0	AFE_IRQ_MCU_CNT2	**Sets up the counter value for IRQ2 according to IRQ2_MODE** The IRQ2 counter in AFE will count down from AFE_IRQ_MCU_CNT2 and set up IRQ2 while IRQ2 counter reaches 1. Therefore, the maximum IRQ time for IRQ2 at 48kHz mode is 5s.

112203B4 AFE_IRQ_MCU_EN AFE IRQ MCU Enable Register 00080473

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											**AFE_IRQ_MD32H_EN**					
Type											RW					
Reset											0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**AFE_IRQ_MD32L_EN**							**AFE_IRQ_MCU_EN**						
Type			RW							RW						
Reset			0	0	0	1	0	0		1	1	1	0	0	1	1

Bit(s)	Name	Description
21:16	AFE_IRQ_MD32H_EN	Reserved
13:8	AFE_IRQ_MD32L_EN	Reserved
6:0	AFE_IRQ_MCU_EN	IRQ to MCU enable control

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112203B8 **AFE_IRQ_MCU_MON2** **AFE IRQ MCU MON2 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													IRQ6_MISS_CNT			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							IRQ2_MISS_FLAG	IRQ1_MISS_FLAG		AFE_IRQ_MCU_CLR_PHASE						
Type							RU	RU		RU						
Reset							0	0		0						

Bit(s)	Name	Description
19:16	IRQ6_MISS_CNT	**Shows how many IRQ6 missed since this register is last cleared** Write 1 to 0x3a8[16] to clear this register.
9	IRQ2_MISS_FLAG	**Shows if there is any miss of the IRQ2. Write 1 to 0x3a8[9] to clear this bit.** 0: No miss 1: Miss had happened
8	IRQ1_MISS_FLAG	**Shows if there is any miss of the IRQ1. Write 1 to 0x3a8[8] to clear this bit.** 0: No miss 1: Miss had happened
6	AFE_IRQ_MCU_CLR_PHASE	**For debugging AFE_IRQ_MCU_CLR**

112203C0 **AFE_IRQ1_MCU_CNT_MON** **AFE IRQ1 MCU Count Monitor Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AFE_IRQ1_CNT_MON[17:16]	
Type															RU	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ1_CNT_MON[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:0	AFE_IRQ1_CNT_MON	**Monitors the counter value for IRQ1 according toIRQ1_MODE** The IRQ1 counter in AFE will count down from AFE_IRQ_MCU_CNT1.

112203C4 **AFE_IRQ2_MCU_CNT_MON** **AFE IRQ2 MCU Count Monitor Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AFE_IRQ2_CNT_MON[17:16]	
Type															RU	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ2_CNT_MON[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:0	AFE_IRQ2_CNT_MON	**Monitors the counter value for IRQ2 according toI2S_MODE** The IRQ1 counter in AFE will count down from AFE_IRQ_MCU_CNT2.

112203C8 AFE_IRQ1_MCU_EN_CNT_MON AFE IRQ1 MCU Enable Count Monitor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_IRQ1_MCU_EN_CNT_MON[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ1_MCU_EN_CNT_MON[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AFE_IRQ1_MCU_EN_CNT_MON	Monitors the enable count number of IRQ1 enabling signal

112203D4 AFE_MEMIF_MAXLEN AFE Memif Max BLength Register 11111115

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved				HDMI_MAXLEN				Reserved1[15:8]							
Type	RW				RW				RW							
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved1[7:0]								DL2_MAXLEN				DL1_data2_MAXLEN		DL1_MAXLEN	
Type	RW								RW				RW		RW	
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	1	0	1

Bit(s)	Name	Description
27:24	HDMI_MAXLEN	0: Does not support 1: 16-byte burst 2: 32-byte burst 3: 64-byte burst
7:4	DL2_MAXLEN	0: Does not support 1: 16-byte burst 2: 32-byte burst 3: 64-byte burst
3:2	DL1_data2_MAXLEN	0: Does not support

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Bit(s)	Name	Description
1:0	DL1_MAXLEN	1: 16-byte burst 2: 32-byte burst 3: 64-byte burst 0: Does not support 1: 16-byte burst 2: 32-byte burst 3: 64-byte burst

112203D8 **AFE_MEMIF_PBUF_SIZE** **AFE MEMIF Prefecth Buffer Size** **000003FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			HDMI_HD_ALIGN	HDMI_HD	MOD_DAI_HD_ALIGN	MOD_DAI_HD	DAI_ALIGN	DAI_HD	VUL_HD_ALIGN	VUL_HD	AWB_HD_ALIGN	AWB_HD	DL2_HD_ALIGN	DL2_HD	DL1_HD_ALIGN	DL1_HD
Type			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VUL_data2_HD_ALIGN	VUL_data2_HD	DL1_data2_HD_ALIGN	DL1_data2_HD	DL1_data2_4ch	VUL_data2_4ch	DL1_data2_PBUF_SIZE		IEC_PBUF_SIZE		HDMI_PBUF_SIZE		DL2_PBUF_SIZE		DL1_PBUF_SIZE	
Type	RW	RW	RW	RW	RW	RW	RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
29	HDMI_HD_ALIGN	0: {8'b0, 24 bits data} 1: {24 bits data, 8'b0}
28	HDMI_HD	0: 16 bits format 1: 24 bits format
27	MOD_DAI_HD_ALIGN	0: {8'b0, 24 bits data} 1: {24 bits data, 8'b0}
26	MOD_DAI_HD	0: 16 bits format 1: 24 bits format
25	DAI_ALIGN	0: {8'b0, 24 bits data} 1: {24 bits data, 8'b0}
24	DAI_HD	0: 16 bits format 1: 24 bits format
23	VUL_HD_ALIGN	0: {8'b0, 24 bits data} 1: {24 bits data, 8'b0}
22	VUL_HD	0: 16 bits format 1: 24 bits format
21	AWB_HD_ALIGN	0: {8'b0, 24 bits data} 1: {24 bits data, 8'b0}
20	AWB_HD	0: 16 bits format 1: 24 bits format
19	DL2_HD_ALIGN	0: {8'b0, 24 bits data} 1: {24 bits data, 8'b0}
18	DL2_HD	0: 16 bits format 1: 24 bits format
17	DL1_HD_ALIGN	0: {8'b0, 24 bits data} 1: {24 bits data, 8'b0}

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Bit(s)	Name	Description
16	DL1_HD	0: 16 bits format 1: 24 bits format
15	VUL_data2_HD_ALIGN	0: {8'b0, 24 bits data} 1: {24 bits data, 8'b0}
14	VUL_data2_HD	0: 16 bits format 1: 24 bits format
13	DL1_data2_HD_ALIGN	0: {8'b0, 24 bits data} 1: {24 bits data, 8'b0}
12	DL1_data2_HD	0: 16 bits format 1: 24 bits format
11	DL1_data2_4ch	0: 2ch 1: 4ch
10	VUL_data2_4ch	0: 2ch 1: 4ch
9:8	DL1_data2_PBUF_SIZE	00: 16 bytes 01: 32 bytes 10: 64 bytes 11: 128 bytes
7:6	IEC_PBUF_SIZE	00: 16 bytes 01: 32 bytes 10: 64 bytes 11: 128 bytes
5:4	HDMI_PBUF_SIZE	00: 16 bytes 01: 32 bytes 10: 64 bytes 11: 128 bytes
3:2	DL2_PBUF_SIZE	00: 16 bytes 01: 32 bytes 10: 64 bytes 11: 128 bytes
1:0	DL1_PBUF_SIZE	00: 16 bytes 01: 32 bytes 10: 64 bytes 11: 128 bytes

112203DC **AFE_IRQ_MCU_CNT7** **AFE IRQ7 MCU Counter Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AFE_IRQ_MCU_CNT7[17:16]	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ_MCU_CNT7[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:0	AFE_IRQ_MCU_CNT7	**Sets up the counter value for IRQ7 according to IRQ7_MODE** The IRQ7 counter in AFE will count down from AFE_IRQ_MCU_CNT7 and set up IRQ7 while IRQ7 counter reaches 1.

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112203F0 **AFE_APLL1_TUNER_CFG** **AFE Tuner Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	upper_bound								apll_div					xtal_en_128fs_sel		freq_tuner_en
Type	RW								RW					RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0

Bit(s)	Name	Description
15:8	upper_bound	**Upper bound setting for changing PCW**
7:4	apll_div	**Divider setting of apll 128fs**
2:1	xtal_en_128fs_sel	2'b00: 32kHz*128 2'b01: 44.1kHz*128 2'b10: 48kHz*128 2'b11: 0
0	freq_tuner_en	1: Enable APLL tuner

112203F4 **AFE_APLL2_TUNER_CFG** **AFE Tuner 2 Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	upper_bound								apll_div					xtal_en_128fs_sel		freq_tuner_en
Type	RW								RW					RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0

Bit(s)	Name	Description
15:8	upper_bound	**Upper bound setting for changing PCW**
7:4	apll_div	**Divider setting of apll 128fs**
2:1	xtal_en_128fs_sel	2'b00: 32kHz*128 2'b01: 44.1kHz*128 2'b10: 48kHz*128 2'b11: 0
0	freq_tuner_en	1: Enable APLL tuner

11220410 **AFE_GAIN1_CON0** **AFE Gain1 Control Register 0** **0000C800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GAIN1_SAMPLE_PER_STEP								GAIN1_MODE							GAIN1_ON
Type	RW								RW							RW
Reset	1	1	0	0	1	0	0	0	0	0	0	0				0

Bit(s)	Name	Description
15:8	GAIN1_SAMPLE_PER_STEP	**GAIN1 sample per step**
7:4	GAIN1_MODE	**GAIN1 mode** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k
0	GAIN1_ON	**GAIN1 on** 0: Off 1: On

11220414 **AFE_GAIN1_CON1** **AFE Gain1 Control Register 1** **00080000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GAIN1_TARGET[19:16]			
Type													RW			
Reset													1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GAIN1_TARGET[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	GAIN1_TARGET	GAIN1 target

11220418 **AFE_GAIN1_CON2** **AFE Gain1 Control Register 2** **0007C5E5**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GAIN1_DOWN_STEP[19:16]			
Type													RW			
Reset													0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GAIN1_DOWN_STEP[15:0]															
Type	RW															
Reset	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1

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Bit(s)	Name	Description
19:0	GAIN1_DOWN_STEP	GAIN1 down step

1122041C **AFE_GAIN1_CON3** **AFE Gain1 Control Register 3** **00083BCD**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GAIN1_UP_STEP[19:16]			
Type													RW			
Reset													1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GAIN1_UP_STEP[15:0]															
Type	RW															
Reset	0	0	1	1	1	0	1	1	1	1	0	0	1	1	0	1

Bit(s)	Name	Description
19:0	GAIN1_UP_STEP	GAIN1 up step

11220420 **AFE_GAIN1_CONN** **AFE Gain1 Connection Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I11_O11_S	I10_O11_S	I11_O10_S	I10_O10_S	I11_O09_S	I10_O09_S	I11_O18_S	I10_O17_S	I08_O14_S	I07_O14_S	I06_O14_S	I05_O14_S	I08_O13_S	I07_O13_S	I06_O13_S	I05_O13_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I11_O08_S	I10_O07_S	I11_O06_S	I10_O05_S	I11_O04_R	I11_O04_S	I10_O03_R	I10_O03_S	I11_O02_R	I11_O02_S	I10_O02_R	I10_O02_S	I11_O01_R	I11_O01_S	I10_O00_R	I10_O00_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	I11_O11_S	**Controls the path from I11 to O11** 0: Off 1: On
30	I10_O11_S	**Controls the path from I10 to O11** 0: Off 1: On
29	I11_O10_S	**Controls the path from I11 to O10** 0: Off 1: On
28	I10_O10_S	**Controls the path from I10 to O10** 0: Off 1: On
27	I11_O09_S	**Controls the path from I11 to O09** 0: Off 1: On
26	I10_O09_S	**Controls the path from I10 to O09** 0: Off 1: On

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Bit(s)	Name	Description
25	I11_O18_S	**Controls the path from I11 to O18** 0: Off 1: On
24	I10_O17_S	**Controls the path from I10 to O17** 0: Off 1: On
23	I08_O14_S	**Controls the path from I08 to O14** 0: Off 1: On
22	I07_O14_S	**Controls the path from I07 to O14** 0: Off 1: On
21	I06_O14_S	**Controls the path from I06 to O14** 0: Off 1: On
20	I05_O14_S	**Controls the path from I05 to O14** 0: Off 1: On
19	I08_O13_S	**Controls the path from I08 to O13** 0: Off 1: On
18	I07_O13_S	**Controls the path from I07 to O13** 0: Off 1: On
17	I06_O13_S	**Controls the path from I06 to O13** 0: Off 1: On
16	I05_O13_S	**Controls the path from I05 to O13** 0: Off 1: On
15	I11_O08_S	**Controls the path from I11 to O08** 0: Off 1: On
14	I10_O07_S	**Controls the path from I10 to O07** 0: Off 1: On
13	I11_O06_S	**Controls the path from I11 to O06** 0: Off 1: On
12	I10_O05_S	**Controls the path from I10 to O05** 0: Off 1: On
11	I11_O04_R	**Controls the enabling of right shift 1 bit from I11 to O04** 0: No shift 1: Right shift 1 bit
10	I11_O04_S	**Controls the path from I11 to O04** 0: Off 1: On
9	I10_O03_R	**Controls the enabling of right shift 1 bit from I10 to O03** 0: No shift 1: Right shift 1 bit
8	I10_O03_S	**Controls the path from I10 to O03** 0: Off

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Bit(s)	Name	Description
		1: On
7	I11_O02_R	**Controls the enabling of right shift 1 bit from I11 to O02** 0: No shift 1: Right shift 1 bit
6	I11_O02_S	**Controls the path from I11 to O02** 0: Off 1: On
5	I10_O02_R	**Controls the enabling of right shift 1 bit from I10 to O02** 0: No shift 1: Right shift 1 bit
4	I10_O02_S	**Controls the path from I10 to O02** 0: Off 1: On
3	I11_O01_R	**Controls the enabling of right shift 1 bit from I11 to O01** 0: No shift 1: Right shift 1 bit
2	I11_O01_S	**Controls the path from I11 to O01** 0: Off 1: On
1	I10_O00_R	**Controls the enabling of right shift 1 bit from I10 to O00** 0: No shift 1: Right shift 1 bit
0	I10_O00_S	**Controls the path from I10 to O00** 0: Off 1: On

11220424 **AFE_GAIN1_CUR** **AFE Gain1 Cursor Register** **00080000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													AFE_GAIN1_CUR[19:16]			
Type													RW			
Reset													1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_GAIN1_CUR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	AFE_GAIN1_CUR	Indicates the current GAIN1

11220428 **AFE_GAIN2_CON0** **AFE Gain2 Control Register 0** **0000C800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GAIN2_SAMPLE_PER_STEP								GAIN2_MODE							GAIN2_ON
Type	RW								RW							RW

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Reset	1	1	0	0	1	0	0	0	0	0	0	0				0

Bit(s)	Name	Description
15:8	GAIN2_SAMPLE_PER_STEP	**GAIN2 sample per step**
7:4	GAIN2_MODE	**GAIN2 mode** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k
0	GAIN2_ON	**GAIN2 on** 0: Off 1: On

1122042C **AFE_GAIN2_CON1** **AFE Gain2 Control Register 1** **00080000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GAIN2_TARGET[19:16]			
Type													RW			
Reset													1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GAIN2_TARGET[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	GAIN2_TARGET	GAIN2 target

11220430 **AFE_GAIN2_CON2** **AFE Gain2 Control Register 2** **0007C5E5**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GAIN2_DOWN_STEP[19:16]			
Type													RW			
Reset													0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GAIN2_DOWN_STEP[15:0]															
Type	RW															
Reset	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1

Bit(s)	Name	Description
19:0	GAIN2_DOWN_STEP	GAIN2 down step

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11220434 **AFE_GAIN2_CON3** **AFE Gain2 Control Register 3** **00083BCD**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GAIN2_UP_STEP[19:16]			
Type													RW			
Reset													1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GAIN2_UP_STEP[15:0]															
Type	RW															
Reset	0	0	1	1	1	0	1	1	1	1	0	0	1	1	0	1

Bit(s)	Name	Description
19:0	GAIN2_UP_STEP	GAIN2 up step

11220438 **AFE_GAIN2_CONN** **AFE Gain2 Connection Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I00_O15_R	I16_O15_S	I15_O15_S	I14_O15_S	I09_O16_S	I04_O16_S	I03_O16_S	I02_O16_S	I01_O16_S	I00_O16_S	I09_O15_S	I04_O15_S	I03_O15_S	I02_O15_S	I01_O15_S	I00_O15_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I13_O08_S	I12_O07_S	I13_O06_S	I12_O05_S	I13_O04_R	I13_O04_S	I12_O03_R	I12_O03_S	I13_O02_R	I13_O02_S	I12_O02_R	I12_O02_S	I13_O01_R	I13_O01_S	I12_O00_R	I12_O00_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	I00_O15_R	**Controls the enabling of right shift 1 bit from I00 to O15** 0: No shift 1: Right shift 1 bit
30	I16_O15_S	**Controls the path from I16 to O15** 0: Off 1: On
29	I15_O15_S	**Controls the path from I15 to O15** 0: Off 1: On
28	I14_O15_S	**Controls the path from I14 to O15** 0: Off 1: On
27	I09_O16_S	**Controls the path from I09 to O16** 0: Off 1: On
26	I04_O16_S	**Controls the path from I04 to O16** 0: Off 1: On
25	I03_O16_S	**Controls the path from I03 to O16** 0: Off 1: On
24	I02_O16_S	**Controls the path from I02 to O16** 0: Off

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Bit(s)	Name	Description
		1: On
23	I01_O16_S	**Controls the path from I01 to O16** 0: Off 1: On
22	I00_O16_S	**Controls the path from I00 to O16** 0: Off 1: On
21	I09_O15_S	**Controls the path from I09 to O15** 0: Off 1: On
20	I04_O15_S	**Controls the path from I04 to O15** 0: Off 1: On
19	I03_O15_S	**Controls the path from I03 to O15** 0: Off 1: On
18	I02_O15_S	**Controls the path from I02 to O15** 0: Off 1: On
17	I01_O15_S	**Controls the path from I01 to O15** 0: Off 1: On
16	I00_O15_S	**Controls the path from I00 to O15** 0: Off 1: On
15	I13_O08_S	**Controls the path from I13 to O08** 0: Off 1: On
14	I12_O07_S	**Controls the path from I12 to O07** 0: Off 1: On
13	I13_O06_S	**Controls the path from I13 to O06** 0: Off 1: On
12	I12_O05_S	**Controls the path from I12 to O05** 0: Off 1: On
11	I13_O04_R	**Controls the enabling of right shift 1 bit from I13 to O04** 0: No shift 1: Right shift 1 bit
10	I13_O04_S	**Controls the path from I13 to O04** 0: Off 1: On
9	I12_O03_R	**Controls the enabling of right shift 1 bit from I12 to O03** 0: No shift 1: Right shift 1 bit
8	I12_O03_S	**Controls the path from I12 to O03** 0: Off 1: On
7	I13_O02_R	**Controls the enabling of right shift 1 bit from I13 to O02** 0: No shift 1: Right shift 1 bit

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Bit(s)	Name	Description
6	I13_O02_S	**Controls the path from I13 to O02** 0: Off 1: On
5	I12_O02_R	**Controls the enabling of right shift 1 bit from I12 to O02** 0: No shift 1: Right shift 1 bit
4	I12_O02_S	**Controls the path from I12 to O02** 0: Off 1: On
3	I13_O01_R	**Controls the enabling of right shift 1 bit from I13 to O01** 0: No shift 1: Right shift 1 bit
2	I13_O01_S	**Controls the path from I13 to O01** 0: Off 1: On
1	I12_O00_R	**Controls the enabling of right shift 1 bit from I12 to O00** 0: No shift 1: Right shift 1 bit
0	I12_O00_S	**Controls the path from I12 to O00** 0: Off 1: On

11220043C **AFE_GAIN2_CUR** **AFE Gain2 Cursor Register** **00080000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													AFE_GAIN2_CUR[19:16]			
Type													RW			
Reset													1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_GAIN2_CUR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	AFE_GAIN2_CUR	Indicates the current gain 2

11220440 **AFE_GAIN2_CONN2** **AFE Gain2 Connection Register 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			I08_O16_S	I07_O16_S	I06_O16_S	I05_O16_S	I00_O16_R					I08_O15_S	I07_O15_S	I06_O15_S	I05_O15_S	I01_O15_R
Type			RW	RW	RW	RW	RW					RW	RW	RW	RW	RW
Reset			0	0	0	0	0					0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I13_O12_S	I12_O12_S	I13_O11_S	I12_O11_S	I13_O10_S	I12_O10_S	I13_O09_S	I12_O09_S	I21_O16_S	I21_O15_S	I16_O16_R	I01_O16_R	I16_O16_S	I15_O16_S	I14_O16_S	I15_O15_R
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
29	I08_O16_S	**Controls the path from I08 to O16** 0: Off 1: On
28	I07_O16_S	**Controls the path from I07 to O16** 0: Off 1: On
27	I06_O16_S	**Controls the path from I06 to O16** 0: Off 1: On
26	I05_O16_S	**Controls the path from I05 to O16** 0: Off 1: On
25	I00_O16_R	**Controls the enabling of right shift 1 bit from I00 to O16** 0: No shift 1: Right shift 1 bit
20	I08_O15_S	**Controls the path from I08 to O15** 0: Off 1: On
19	I07_O15_S	**Controls the path from I07 to O15** 0: Off 1: On
18	I06_O15_S	**Controls the path from I06 to O15** 0: Off 1: On
17	I05_O15_S	**Controls the path from I05 to O15** 0: Off 1: On
16	I01_O15_R	**Controls the enabling of right shift 1 bit from I01 to O15** 0: No shift 1: Right shift 1 bit
15	I13_O12_S	**Controls the path from I13 to O12** 0: Off 1: On
14	I12_O12_S	**Controls the path from I12 to O12** 0: Off 1: On
13	I13_O11_S	**Controls the path from I13 to O11** 0: Off 1: On
12	I12_O11_S	**Controls the path from I12 to O11** 0: Off 1: On
11	I13_O10_S	**Controls the path from I13 to O10** 0: Off 1: On
10	I12_O10_S	**Controls the path from I12 to O10** 0: Off 1: On
9	I13_O09_S	**Controls the path from I13 to O09** 0: Off 1: On
8	I12_O09_S	**Controls the path from I12 to O09** 0: Off

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Bit(s)	Name	Description
		1: On
7	I21_O16_S	**Controls the path from I21 to O16** 0: Off 1: On
6	I21_O15_S	**Controls the path from I21 to O15** 0: Off 1: On
5	I16_O16_R	**Controls the enabling of right shift 1 bit from I16 to O16** 0: No shift 1: Right shift 1 bit
4	I01_O16_R	**Controls the enabling of right shift 1 bit from I01 to O16** 0: No shift 1: Right shift 1 bit
3	I16_O16_S	**Controls the path from I16 to O16** 0: Off 1: On
2	I15_O16_S	**Controls the path from I15 to O16** 0: Off 1: On
1	I14_O16_S	**Controls the path from I14 to O16** 0: Off 1: On
0	I15_O15_R	**Controls the enabling of right shift 1 bit from I15 to O15** 0: No shift 1: Right shift 1 bit

11220444 **AFE_GAIN2_CONN3** **AFE Gain2 Connection Register 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					I13_O18_S	I12_O17_S	I22_O16_S	I22_O15_S								
Type					RW	RW	RW	RW								
Reset					0	0	0	0								

Bit(s)	Name	Description
11	I13_O18_S	**Controls the path from I13 to O18** 0: Off 1: On
10	I12_O17_S	**Controls the path from I12 to O17** 0: Off 1: On
9	I22_O16_S	**Controls the path from I22 to O16** 0: Off 1: On
8	I22_O15_S	**Controls the path from I22 to O15** 0: Off 1: On

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11220448 **AFE_GAIN1_CONN2** **AFE Gain1 Connection Register 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									I16_O14_S	I15_O14_S	I14_O14_S	I09_O14_S	I04_O14_S	I03_O14_S	I02_O14_S	I01_O14_S
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	I00_O14_S					I16_O13_S	I15_O13_S	I14_O13_S	I09_O13_S	I04_O13_S	I03_O13_S	I02_O13_S	I01_O13_S	I00_O13_S	I11_O12_S	I10_O12_S
Type	RW					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0					0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23	I16_O14_S	**Controls the path from I16 to O14** 0: Off 1: On
22	I15_O14_S	**Controls the path from I15 to O14** 0: Off 1: On
21	I14_O14_S	**Controls the path from I14 to O14** 0: Off 1: On
20	I09_O14_S	**Controls the path from I09 to O14** 0: Off 1: On
19	I04_O14_S	**Controls the path from I04 to O14** 0: Off 1: On
18	I03_O14_S	**Controls the path from I03 to O14** 0: Off 1: On
17	I02_O14_S	**Controls the path from I02 to O14** 0: Off 1: On
16	I01_O14_S	**Controls the path from I01 to O14** 0: Off 1: On
15	I00_O14_S	**Controls the path from I00 to O14** 0: Off 1: On
10	I16_O13_S	**Controls the path from I16 to O13** 0: Off 1: On
9	I15_O13_S	**Controls the path from I15 to O13** 0: Off 1: On
8	I14_O13_S	**Controls the path from I14 to O13** 0: Off 1: On

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Bit(s)	Name	Description
7	I09_O13_S	**Controls the path from I09 to O13** 0: Off 1: On
6	I04_O13_S	**Controls the path from I04 to O13** 0: Off 1: On
5	I03_O13_S	**Controls the path from I03 to O13** 0: Off 1: On
4	I02_O13_S	**Controls the path from I02 to O13** 0: Off 1: On
3	I01_O13_S	**Controls the path from I01 to O13** 0: Off 1: On
2	I00_O13_S	**Controls the path from I00 to O13** 0: Off 1: On
1	I11_O12_S	**Controls the path from I11 to O12** 0: Off 1: On
0	I10_O12_S	**Controls the path from I10 to O12** 0: Off 1: On

1122044C **AFE_GAIN1_CONN3** **AFE Gain1 Connection Register 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						I11_O27_S	I10_O26_S	I22_O14_S	I22_O13_S	I10_O25_S	I21_O14_S	I21_O13_S	I11_O24_S	I10_O23_S		
Type						RW	RW	RW	RW	RW	RW	RW	RW	RW		
Reset						0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
10	I11_O27_S	**Controls the path from I11 to O27** 0: Off 1: On
9	I10_O26_S	**Controls the path from I10 to O26** 0: Off 1: On
8	I22_O14_S	**Controls the path from I22 to O14** 0: Off 1: On
7	I22_O13_S	**Controls the path from I22 to O13** 0: Off 1: On

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Bit(s)	Name	Description
6	I10_O25_S	**Controls the path from I10 to O25** 0: Off 1: On
5	I21_O14_S	**Controls the path from I21 to O14** 0: Off 1: On
4	I21_O13_S	**Controls the path from I21 to O13** 0: Off 1: On
3	I11_O24_S	**Controls the path from I11 to O24** 0: Off 1: On
2	I10_O23_S	**Controls the path from I10 to O23** 0: Off 1: On

11220468 AFE_CONN9 AFE Connection Register 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			I22_O25_S	I22_O24_S	I22_O23_S	I22_O18_S	I22_O17_S	I22_O12_S	I22_O10_S	I22_O06_S	I22_O04_S	I22_O03_S	I22_O02_S	I22_O01_S	I22_O00_S	I00_O25_S
Type			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I01_O24_S	I00_O23_S														
Type	RW	RW														
Reset	0	0														

Bit(s)	Name	Description
29	I22_O25_S	**Controls the path from I22 to O25** 0: Off 1: On
28	I22_O24_S	**Controls the path from I22 to O24** 0: Off 1: On
27	I22_O23_S	**Controls the path from I22 to O23** 0: Off 1: On
26	I22_O18_S	**Controls the path from I22 to O18** 0: Off 1: On
25	I22_O17_S	**Controls the path from I22 to O17** 0: Off 1: On
24	I22_O12_S	**Controls the path from I22 to O12** 0: Off 1: On
23	I22_O10_S	**Controls the path from I22 to O10** 0: Off 1: On

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Bit(s)	Name	Description
22	I22_O06_S	**Controls the path from I22 to O06** 0: Off 1: On
21	I22_O04_S	**Controls the path from I22 to O04** 0: Off 1: On
20	I22_O03_S	**Controls the path from I22 to O03** 0: Off 1: On
19	I22_O02_S	**Controls the path from I22 to O02** 0: Off 1: On
18	I22_O01_S	**Controls the path from I22 to O01** 0: Off 1: On
17	I22_O00_S	**Controls the path from I22 to O00** 0: Off 1: On
16	I00_O25_S	**Controls the path from I00 to O25** 0: Off 1: On
15	I01_O24_S	**Controls the path from I01 to O24** 0: Off 1: On
14	I00_O23_S	**Controls the path from I00 to O23** 0: Off 1: On

1122046C **AFE_CONN10** **AFE Connection Register 10** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							I21_O27_S		I14_O27_S	I04_O27_S	I01_O27_S	I21_O26_S		I14_O26_S	I03_O26_S	I00_O26_S
Type							RW		RW	RW	RW	RW		RW	RW	RW
Reset							0		0	0	0	0		0	0	0

Bit(s)	Name	Description
9	I21_O27_S	**Controls the path from I21 to O27** 0: Off 1: On
7	I14_O27_S	**Controls the path from I14 to O27** 0: Off 1: On
6	I04_O27_S	**Controls the path from I04 to O27** 0: Off 1: On
5	I01_O27_S	**Controls the path from I01 to O27** 0: Off

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Bit(s)	Name	Description
		1: On
4	I21_O26_S	**Controls the path from I21 to O26** 0: Off 1: On
2	I14_O26_S	**Controls the path from I14 to O26** 0: Off 1: On
1	I03_O26_S	**Controls the path from I03 to O26** 0: Off 1: On
0	I00_O26_S	**Controls the path from I00 to O26** 0: Off 1: On

112204F0 **AFE_SRAM_DELSEL_CON0** **Memory DELSEL Control 0** **5AAA55AA**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_src_4ch_mbist_delsel_1				afe_src_4ch_mbist_delsel_0				afe_src_mbist_delsel_1				afe_src_mbist_delsel_0			
Type	RW				RW				RW				RW			
Reset	0	1	0	1	1	0	1	0	1	0	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_side_tone_coeff_mbist_delsel				afe_side_tone_mbist_delsel				afe_dl_buf_mbist_delsel				afe_ul_buf_mbist_delsel			
Type	RW				RW				RW				RW			
Reset	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0

Bit(s)	Name	Description
31:28	afe_src_4ch_mbist_delsel_1	Controls DELSEL for SRC 4ch IIR coefficent memory
27:24	afe_src_4ch_mbist_delsel_0	Controls DELSEL for SRC 4ch history memory
23:20	afe_src_mbist_delsel_1	Controls DELSEL for SRC IIR coefficent memory
19:16	afe_src_mbist_delsel_0	Controls DELSEL for SRC history memory
15:12	afe_side_tone_coeff_mbist_delsel	Controls DELSEL for sidetone coefficent memory
11:8	afe_side_tone_mbist_delsel	Controls DELSEL for sidetone memory
7:4	afe_dl_buf_mbist_delsel	Controls DELSEL for DL memory
3:0	afe_ul_buf_mbist_delsel	Controls DELSEL for UL coefficent memory

112204F4 **AFE_SRAM_DELSEL_CON1** **Memory DELSEL Control 1** **000000AA**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

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Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									afe_memif_mbist_delsel_0				afe_memif_mbist_delsel_1			
Type									RW				RW			
Reset									1	0	1	0	1	0	1	0

Bit(s)	Name	Description
7:4	afe_memif_mbist_delsel_0	Controls DELSEL for MEMIF sysram memory
3:0	afe_memif_mbist_delsel_1	Controls DELSEL for MEMIF prefetch buffer memory

11220500 **AFE_ASRC_CON0** **ASRC Config 0** **80080000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHSET1_O16BIT		CHSET1_CLR_IIR_HISTORY	CHSET1_IS_MONO	CHSET1_OFS_SEL		CHSET1_IFS_SEL		CHSET1_IIR_EN	CHSET1_IIR_STAGE			CHSET0_O16BIT		CHSET0_CLR_IIR_HISTORY	CHSET0_IS_MONO
Type	RW		Other	RW	RW		RW		RW	RW			RW		Other	RW
Reset	1		0	0	0	0	0	0	0	0	0	0	1		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHSET0_OFS_SEL		CHSET0_IFS_SEL		CHSET0_IIR_EN	CHSET0_IIR_STAGE				CHSET_STR_CLR			CHSET_ON		COEF_SRAM_CTRL	ASM_ON
Type	RW		RW		RW	RW				Other			RU		RW	RW
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	CHSET1_O16BIT	**Selects 16-bit/24-bit output**
29	CHSET1_CLR_IIR_HISTORY	**Set to 1 to clear the current IIR output history buffer for RX** This register will be auto-cleared once the histories are cleared.
28	CHSET1_IS_MONO	**Mono/Stereo selection register**
27:26	CHSET1_OFS_SEL	**Selects output sample rate for RX** Set to 01 for OFS fix value.
25:24	CHSET1_IFS_SEL	**Selects input sample rate for RX** Set to 10 for frequency tracking mode.
23	CHSET1_IIR_EN	**Enables anti-alias IIR filter for RX** Set to 1 to turn on anti-alias IIR filter.
22:20	CHSET1_IIR_STAGE	**Anti-alias IIR filter stage for RX** Defines how many 2-order IIR stages are cascaded for the anti-alias filter. This value should be "real stage amount" minus 1, which means up to 8 stages and 16 orders are supported.
19	CHSET0_O16BIT	**Selects 16-bit/24-bit output**
17	CHSET0_CLR_IIR_HISTORY	**Set to 1 to clear current IIR output history buffer for TX** This register will be auto-cleared once the histories are cleared.
16	CHSET0_IS_MONO	**Mono/Stereo selection register**
15:14	CHSET0_OFS_SEL	**Selects output sample rate for TX** Set to 00 for OFS fix value.

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Bit(s)	Name	Description
13:12	CHSET0_IFS_SEL	**Selects input sample rate selection for TX** Set to 11 for period tracking mode.
11	CHSET0_IIR_EN	**Enables anti-alias IIR filter for TX** Set to 1 to turn on anti-alias IIR filter.
10:8	CHSET0_IIR_STAGE	**Anti-alias IIR filter stage for TX** Defines how many 2-order IIR stages are cascaded for the anti-alias filter. This value should be "real stage amount" minus 1, which means up to 8 stages and 16 orders are supported.
6:4	CHSET_STR_CLR	**Each channel set clear signal** Set bit 0 to 1 to clear the TX history. Set bit 1 to 1 to clear the RX history. Set bit 2 to 1 to clear the I2S history.
3:2	CHSET_ON	**Indicates which channel set is on currently** 01: TX 10: RX
1	COEFF_SRAM_CTRL	**Controls coefficient SRAM access** 0: Disable access 1: Enable access
0	ASM_ON	**ASRC enabling signal** Turn it on after all configurations are set. 0: Disable ASRC 1: Enable ASRC

11220504 <u>**AFE_ASRC_CON1**</u> **ASRC Config 1** **00000CB2**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_0[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_0[15:0]															
Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Name	Description
23:0	ASM_FREQ_0	**Frequency palette** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for TX OFS.

11220508 <u>**AFE_ASRC_CON2**</u> **ASRC Config 2** **00400000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_1[23:16]							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
23:0	ASM_FREQ_1	**Frequency palette** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for RX OFS.

1122050C AFE_ASRC_CON3 ASRC Config 3 00400000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_2[23:16]							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	ASM_FREQ_2	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for RX IFS.

11220510 AFE_ASRC_CON4 ASRC Config 4 00000CB2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_3[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_3[15:0]															
Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Name	Description
23:0	ASM_FREQ_3	**Frequency palette** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for TX IFS.

11220514 AFE_ASRC_CON5 ASRC Config 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RESULT_SEL		
Type														RW		
Reset														0	0	0

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Bit(s)	Name	Description
2:0	RESULT_SEL	**Selects output** 000: ASRC output 001: Data input 010: CMPF output 011: HBF1 output 100: HBF2 output 101: HBF3 output 110: HBF4 output 111: Each IIR stage output in order

11220518 **AFE_ASRC_CON6** **ASRC Config 6** **00010800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FREQ_CALI_CYCLE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FREQ_CALI_AUTORST_EN		FREQ_CALC_RUNNING	AUTO_TUNE_FREQ3	COMP_FREQ_RES_EN		FREQ_CALI_SEL		FREQ_CALI_BP_DGL	FREQ_CALI_MAX_GWIDTH			AUTO_TUNE_FREQ2	FREQ_CALI_AUTO_RESTART	CALI_USE_FREQ_OUT	CALI_EN
Type	RW		RU	RW	RW		RW		RW	RW			RW	RW	RW	RU
Reset	0		0	0	1		0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	FREQ_CALI_CYCLE	**Frequency calibrating cycle register** Defines how many input signal cycles the calibrator calibrates are in one round. This register is updated into calibrator once the calibrator enable [0] is turned on.
15	FREQ_CALI_AUTORST_EN	**Enables period calibration auto-reset** Period calibration bigger than 0x578 or smaller than 0x57c will trigger ASRC reset.
13	FREQ_CALC_RUNNING	**Shows if frequency calculation is running** For one round running case, wait for this bit and the CALI_EN bit to become low before frequency result is ready.
12	AUTO_TUNE_FREQ3	**Enables asm_freq_3 auto update with the calibrator result once the calibrator completes one round** 0: Disable auto update 1: Enable auto update
11	COMP_FREQ_RES_EN	**Frequency compensation enabling register** 0: Disable compensation 1: Enable compensation
9:8	FREQ_CALI_SEL	**Calibrator input source selection register** Before modifying this register, make sure the calibrator is turned off. 00: Use PCM SYNC word 01: Not connected 10: Not connected 11: Not connected
7	FREQ_CALI_BP_DGL	**Bypasses deglitch circuit for calibrator input** 0: Does not bypass 1: Bypass

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Bit(s)	Name	Description
6:4	FREQ_CALI_MAX_G WIDTH	**Defines the maximum glitch width of the calibrator input signal. Unit: Calibrator reference clock cycles.**
3	AUTO_TUNE_FREQ2	**Enables asm_freq_2 auto update with the calibrator result once the calibrator completes one round** 0: Disable auto update 1: Enable auto update
2	FREQ_CALI_AUTO_ RESTART	**Enables calibrator auto restart new calibration while one run is completed** This value will be updated into calibrator once the enabling signal is turned on from off state. 0: Disable auto restart 1: Enable auto restart
1	CALI_USE_FREQ_O UT	**Selects frequency or period calibration mode** 0: Use period calibration result to update asm_freq_2. Use frequency calibration result to update asm_freq_3 1: Use frequency calibration result to update asm_freq_2. Use period calibration result to update asm_freq_3
0	CALI_EN	**Enables frequency calibrator** If auto restart is 0, this bit will be cleared when one calibration run is completed. If this bit is set to 0, wait until this bit becomes 0 before making the next run start safely. 0: Disable calibrator 1: Enable calibrator

1122051C **AFE_ASRC_CON7** **ASRC Config 7** **00000659**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALC_DENOMINATOR[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALC_DENOMINATOR[15:0]															
Type	RW															
Reset	0	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1

Bit(s)	Name	Description
23:0	FREQ_CALC_DENO MINATOR	Determines the denominator for performing period-to-frequency calibration result translation

11220520 **AFE_ASRC_CON8** **ASRC Config 8** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									PRD_CALI_RESULT_RECORD[23:16]							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRD_CALI_RESULT_RECORD[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
23:0	PRD_CALI_RESULT_RECORD	**Period calibration result** Records the calibration result of the previous round. Writing any value to this register will clear the result.

11220524 **AFE_ASRC_CON9** **ASRC Config 9** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_RESULT[23:16]							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_RESULT[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	FREQ_CALI_RESULT	**Frequency calibrator result** Records the calibration result of previous round. This value is got from the quotient (FREQ_CALC_DENOMINATOR/PRD_CALI_RESULT) in 1.23 format.

11220528 **AFE_ASRC_CON10** **ASRC Config 10** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									COEFF_SRAM_DATA[23:16]							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COEFF_SRAM_DATA[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	COEFF_SRAM_DATA	**Read/Write data port of coefficient SRAM** Read data have one cycle delay. The coefficients are filled stage by stage: each stage has 6 coefficients. For the 2nd-order IIR filter with transfer function of one stage as: "(2^shift)*a0 + (2^shift)*a1*Z^-1 + (2^shift)*a2*Z^-2/1 + (2^shift)*b1*Z^ -1 + (2^shift)*b2*Z^-2" The coefficient should be filled as (from low address to high address) a2 a1 a0 -b1 -b2 shift

1122052C **AFE_ASRC_CON11** **ASRC Config 11** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name										COEFF_SRAM_ADR						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	COEFF_SRAM_ADR	**Determines the rd/wr address of IIR coefficient SRAM** Read/Write COEFF_SRAM_DATA will make this register increase by 1.

11220530 PCM_INTF_CON1 PCM Interface Config 1 00000006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIX_VALUE_SEL	BUFFER_LOOPBACK	PARALLEL_LOOPBACK	SERIAL_LOOPBACK	DAI_PCM_LOOPBACK	I2S_PCM_LOOPBACK	SYNC_DELSEL	TX_LR_SWAP	SYNC_OUT_INV	BCLK_OUT_INV	SYNC_IN_INV	BCLK_IN_INV	TX_LCH_RPT	VBT_16K_MODE	EXT_MODEM	PCM_24BIT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PCM_WLEN		SYNC_LENGTH					SYNC_TYPE	BT_MODE	BYP_ASRC	PCM_SLAVE	PCM_MODE		PCM_FMT		PCM_EN
Type	RW		RW					RW	RW	RW	RW	RW		RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bit(s)	Name	Description
31	FIX_VALUE_SEL	**Selects fix register value sent on PCM TX** Fix register value is from 0x0538. 0: Disable fix value on TX 1: Enable fix value on TX
30	BUFFER_LOOPBACK	**PCM RX parallel data in async FIFO are loopback to PCM TX async FIFO.** 2-channel TX data receive the same 1-channel RX data. 0: Disable loopback 1: Enable loopback
29	PARALLEL_LOOPBACK	**PCM RX parallel data are loopback to PCM TX directly** 2-channel TX data receive the same 1-channel RX data. 0: Disable loopback 1: Enable loopback
28	SERIAL_LOOPBACK	**PCM RX serial data are loopback to PCM TX directly** 0: Disable loopback 1: Enable loopback
27	DAI_PCM_LOOPBACK	**Internal loopback with AFE_DAIBT module** 0: Disable loopback 1: Enable loopback
26	I2S_PCM_LOOPBACK	**Internal loopback with AFE_I2S module** 0: Disable loopback 1: Enable loopback
25	SYNC_DELSEL	**Selects synchronizer** 0: Select 2 FFs synchronizer 1: Select 1 FF synchronizer
24	TX_LR_SWAP	**TX L/R channels swap** 0: Disable swap 1: Enable swap

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Bit(s)	Name	Description
23	SYNC_OUT_INV	**Inverts PCM SYNC out** 0: No inverse 1: Invert
22	BCLK_OUT_INV	**Inverts PCM BCLK out** 0: No inverse 1: Invert
21	SYNC_IN_INV	**Inverts PCM SYNC in** 0: No inverse 1: Invert
20	BCLK_IN_INV	**Inverts PCM BCLK in** 0: No inverse 1: Invert
19	TX_LCH_RPT	**TX L-channel repeats twice in one sample period.** 0: No repeat 1: Repeat
18	VBT_16K_MODE	**Mode support for 2 samples in once sync Used in 16K mode only.** 0: Disable 1: Enable
17	EXT_MODEM	**Selects internal/external modem PCM interface** 0: Select internal modem 1: Select external modem
16	PCM_24BIT	**Selects data sample bit width** 0: 16-bit sample 1: 24-bit sample
15:14	PCM_WLEN	**Selects BCK cycles in one LRCK period** 00: 32 BCK 01: 64 BCK
13:9	SYNC_LENGTH	**PCM mode B sync length** SYNC_TYPE must be set to 1 to enable extended sync length. 00000: Sync is 1 BCK cycle 00001: Sync is 2 BCK cycles. 00010: Sync is 3 BCK cycles. 11111: Sync is 32 BCK cycles.
8	SYNC_TYPE	**PCM mode B single BCK cycle sync length or multiple BCK cycles sync length** 0: 1 BCK cycle sync length 1: Extended BCK cycles sync length
7	BT_MODE	**In BT mode, only L channel data are sent on PCM TX.** 0: Dual mic on TX 1: Single mic on TX
6	BYP_ASRC	**Set to 0 when source and destination use different crystals.** Set to 1 when the source and destination use same crystal. 0: TX/RX parallel data go through ASRC 1: TX/RX parallel data go through async FIFO
5	PCM_SLAVE	**Selects master/slave mode** 0: Master mode 1: Slave mode
4:3	PCM_MODE	**Selects sampling rate** 00: 8K 01: 16K 10: 32K
2:1	PCM_FMT	**PCM interface formats** 00: I2S 01: EIAJ

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Bit(s)	Name	Description
		10: PCM mode A 11: PCM mode B
0	PCM_EN	**Enables PCM interface** 0: Disable PCM interface 1: Enable PCM interface

11220538 **PCM_INTF_CON2** **PCM Interface Config 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PCM1_TX_FIFO_OV	PCM1_RX_FIFO_OV	PCM2_TX_FIFO_OV	PCM2_RX_FIFO_OV	PCM1_SYNC_GLITCH	PCM2_SYNC_GLITCH										
Type	RU	RU	RU	RU	RU	RU										
Reset	0	0	0	0	0	0										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PCM1_PCM2_LOOPBACK		DAI_PCM_LOOPBACK_CH	I2S_PCM_LOOPBACK_CH				PCM_USE_MD3	TX_FIX_VALUE							
Type	RW		RW	RW				RW	RW							
Reset	0		0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PCM1_TX_FIFO_OV	**PCM1 (master/slave PCM) TX async FIFO overflow/underflow flag**
30	PCM1_RX_FIFO_OV	**PCM1 (master/slave PCM) RX async FIFO overflow/underflow flag**
29	PCM2_TX_FIFO_OV	**PCM2 (slave only PCM) TX Async FIFO overflow/underflow flag**
28	PCM2_RX_FIFO_OV	**PCM2 (slave only PCM) RX Async FIFO overflow/underflow flag**
27	PCM1_SYNC_GLITCH	**PCM1 (master/slave PCM) sync glitch flag**
26	PCM2_SYNC_GLITCH	**PCM2 (slave only PCM) sync glitch flag**
15	PCM1_PCM2_LOOPBACK	**Internal loopback with AFE_PCM_SLV_INTF module** 0: Disable loopback 1: Enable loopback
13	DAI_PCM_LOOPBACK_CH	**Selects internal loopback signal with AFE_DAIBT module** 0: TX 1: TX2
12	I2S_PCM_LOOPBACK_CH	**Selects internal loopback signal with AFE_I2S module** 0: TX 1: TX2
8	PCM_USE_MD3	**Selects internal MD2/MD3 PCM interface** 0: Select internal MD2 1: Select internal MD3
7:0	TX_FIX_VALUE	**Fix register value sent on PCM TX**

1122053C **PCM2_INTF_CON** **PCM2 Interface Config** **00000006**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	TX_FIX_VALUE								FIX_VALUE_SEL	BUFFER_LOOPBACK	PARALLEL_LOOPBACK	SERIAL_LOOPBACK	DAI_PCM_LOOPBACK	I2S_PCM_LOOPBACK	SYNC_DELSEL	TX_LR_SWAP
Type	RW								RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYNC_IN_INV	BCLK_IN_INV	TX_LCH_RPT	VBT_16K_MODE	LOOPBACK_CH_SEL			TX2BT_MODE	BT_MODE	PCM_AFIFO	PCM_WLEN	PCM_MODE		PCM_FMT		PCM_EN
Type	RW	RW	RW	RW	RW			RW	RW	RW	RW	RW		RW		RW
Reset	0	0	0	0	0	0		0	0	0	0	0	0	1	1	0

Bit(s)	Name	Description
31:24	TX_FIX_VALUE	**Fix register value sent on PCM TX**
23	FIX_VALUE_SEL	**Selects fix register value sent on PCM TX. Fix register value is from bit[31:24].** 0: Disable fix value on TX 1: Enable fix value on TX
22	BUFFER_LOOPBACK	**PCM RX parallel data in async FIFO are loopback to PCM TX async FIFO.** 2-channel TX data receive the same 1-channel RX data. 0: Disable loopback 1: Enable loopback
21	PARALLEL_LOOPBACK	**PCM RX parallel data are loopback to PCM TX directly.** 2-channels TX data receives same 1-channel RX data. 0: Disable loopback 1: Enable loopback
20	SERIAL_LOOPBACK	**PCM RX serial data are loopback to PCM TX directly** 0: Disable loopback 1: Enable loopback
19	DAI_PCM_LOOPBACK	**Internal loopback with DAIBT module** 0: Disable loopback 1: Enable loopback
18	I2S_PCM_LOOPBACK	**Internal loopback with AFE_I2S module** 0: Disable loopback 1: Enable loopback
17	SYNC_DELSEL	**Selects synchronizer** 0: Select 2 FFs synchronizer 1: Select 1 FF synchronizer
16	TX_LR_SWAP	**Swaps TX L/R channels** 0: Disable swap 1: Enable swap
15	SYNC_IN_INV	**Inverts PCM SYNC in** 0: No inverse 1: Invert
14	BCLK_IN_INV	**Inverts PCM BCLK in** 0: No inverse 1: Invert
13	TX_LCH_RPT	**TX L-channel repeat twice in one sample period** 0: No repeat 1: Repeat
12	VBT_16K_MODE	**Mode support for 2 samples in once sync** Used in 16K mode only. 0: Disable

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Bit(s)	Name	Description
		1: Enable
11:10	LOOPBACK_CH_SEL	**Select loopback channels for PCM2 to I2S or PCM2 to DAI loopback mode** 00: PCM2_TX for loopback 01: PCM2_TX2 for loopback 10: PCM2_TX3 for loopback
8	TX2_BT_MODE	**In BT mode, only L channel data are sent on PCM TX2.** 0: Dual mic on TX2 1: Single mic on TX2
7	BT_MODE	**In BT mode, only L channel data are sent on PCM TX.** 0: Dual mic on TX 1: Single mic on TX
6	PCM_AFIFO	**Selects ASRC if modem is using different clock source; selects AFIFO if modem is using the same clock source** 0: ASRC 1: AFIFO
5	PCM_WLEN	**Selects BCK cycles in one LRCK period** 0: 32 BCK cycles 1: 64 BCK cycles
4:3	PCM_MODE	**Selects sampling rate** 00: 8K 01: 16K 10: 32K
2:1	PCM_FMT	**PCM interface formats** 00: I2S 01: EIAJ 10: PCM mode A 11: PCM mode B
0	PCM_EN	**Enables PCM interface** 0: Disable PCM interface 1: Enable PCM interface

11220550 **AFE_ASRC_CON13** **ASRC Config 13** **00080000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													CHSET2_O16BIT			CHSET2_IS_MONO
Type													RW			RW
Reset													1			0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CHSET_STR_CLR			CHSET_ON			COEFF_SRAM_CTRL	ASM_ON
Type									RU			RU			RU	RU
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	CHSET2_O16BIT	**Selects 16-bit/24-bit output**
16	CHSET2_IS_MONO	**Mono/Stereo selection register**
7:5	CHSET_STR_CLR	**Sets up AFE_ASRC_CON0 to clear**

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Bit(s)	Name	Description
		Read-only.
4:2	CHSET_ON	**Indicates which channel set is on currently** 001: PCM TX 010: PCM RX 100: I2S RX
1	COEFF_SRAM_CTRL	**Controls coefficient SRAM access** 0: Disable access 1: Enable access
0	ASM_ON	**ASRC enabling signal** Turn it on after all configurations are set. 0: ASRC disable 1: ASRC enable

11220554 **AFE_ASRC_CON14** **ASRC Config 14** **00600000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_4[23:16]							
Type									RW							
Reset									0	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_4[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	ASM_FREQ_4	**Frequency palette** The frequency palette for each channel is set to define its input frequency and output frequency. Default: Set for I2S RX OFS. 48K: 3250/[(26M/48K)*8] = 0x600000 44.1K: 8125/[(26M/44.1K)*8] = 0xDC8000

11220558 **AFE_ASRC_CON15** **ASRC Config 15** **00400000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_5[23:16]							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_5[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	ASM_FREQ_5	**Frequency palette** The frequency palette for each channel is set to define its input frequency and output frequency. Default: Set for I2S RX IFS. 48K: 3250/[(26M/32K)*8] = 0x400000 44.1K: 8125/[(26M/32K)*8] = 0xA00000

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1122055C **AFE_ASRC_CON16** **ASRC Config 16** **00010800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FREQ_CALI2_CYCLE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		FREQ_CALI2_AUTORST_EN	FREQ_CALC2_RUNNING	AUTO_TUNE_FREQ4	COMP_FREQ_RES_EN2		FREQ_CALI2_SEL		FREQ_CALI2_BP_DGL	FREQ_CALI2_MAX_GWIDTH			AUTO_TUNE_FREQ5	FREQ_CALI2_AUTORESTART	CALI2_USE_FREQ_OUT	CALI2_EN
Type		RW	RU	RW	RW		RW		RW	RW			RW	RW	RW	RW
Reset		0	0	0	1		0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	FREQ_CALI2_CYCLE	**Frequency calibrating 2 cycle register** Defines how many input signal cycles the calibrator calibrates in one round. This register is updated into calibrator once the calibrator enable [0] is turned on. In OFS 48K or 44.1K, set it to 7.
14	FREQ_CALI2_AUTORST_EN	**Enables freq_cali2 auto reset with the calibrator result that is too large (slow I2S in when FM change)** For I2S in, set it to 1. 0: Disable auto reset 1: Enable auto reset
13	FREQ_CALC2_RUNNING	**Shows if frequency calculation 2 is running.** For one round running case, wait for this bit and the CALI_EN bit to become low before frequency result is ready.
12	AUTO_TUNE_FREQ4	**Enables asm_freq_4 auto update with the calibrator result once the calibrator completes one round** For I2S in, set it to 0. 0: Disable auto update 1: Enable auto update
11	COMP_FREQ_RES_EN2	**Frequency compensation 2 enabling register** 0: Disable compensation 1: Enable compensation
9:8	FREQ_CALI2_SEL	**Selects calibrator 2 input source** Before modifying this register, make sure the calibrator is turned off. For I2S in, set it to 2'b01. 00: Use PCM SYNC word 01: Not connected 10: Not connected 11: Not connected
7	FREQ_CALI2_BP_DGL	**Bypasses deglitch circuit for calibrator 2 input** 0: No bypass 1: Bypass
6:4	FREQ_CALI2_MAX_GWIDTH	**Defines maximum glitch width of calibrator 2 input signal** Unit: Calibrator reference clock cycles
3	AUTO_TUNE_FREQ5	**Enables asm_freq_5 auto update with the calibrator result once the calibrator completes one round** For I2S in, set it to 1. 0: Disable auto update 1: Enable auto update
2	FREQ_CALI2_AUTO	**Enables calibrator 2 auto restart new calibration when one run is**

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Bit(s)	Name	Description
	_RESTART	**completed** This value will be updated into calibrator once the enabling signal is turned on from off state. 0: Disable auto restart 1: Enable auto restart
1	CALI2_USE_FREQ_OUT	**Selects frequency or period calibration mode** For I2S in, set it to 1. 0: Use period calibration result to update asm_freq_2, use frequency calibration result to update asm_freq_3 1: Use frequency calibration result to update asm_freq_2, use period calibration result to update asm_freq_3
0	CALI2_EN	**Enables frequency calibrator 2** If auto restart is 0, this bit will be cleared when one calibration run is completed. If this bit is set to 0, wait until this bit becomes 0 before making the next run start safely. 0: Disable calibrator 1: Enable calibrator

11220560 **AFE_ASRC_CON17** **ASRC Config 17** **00000CB2**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									**FREQ_CALC2_DENOMINATOR[23:16]**							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**FREQ_CALC2_DENOMINATOR[15:0]**															
Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Name	Description
23:0	FREQ_CALC2_DENOMINATOR	**Determines denominator for performing period-to-frequency calibration result translation.** 48K: 3250 (0xCB2) 44.1K: 8125 (0x1FBD)

11220564 **AFE_ASRC_CON18** **ASRC Config 18** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									**PRD_CALI2_RESULT_RECORD[23:16]**							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**PRD_CALI2_RESULT_RECORD[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	PRD_CALI2_RESULT_RECORD	**Period calibration 2 result** Records the calibration result of the previous round. Write any value to this register to clear the result.

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11220568 **AFE_ASRC_CON19** **ASRC Config 19** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI2_RESULT[23:16]							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI2_RESULT[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	FREQ_CALI2_RESULT	**Frequency calibrator 2 result** Records the calibration result of the previous round. This value is got from the quotient (FREQ_CALC2_DENOMINATOR/PRD_CALI2_RESULT) in 1.23 format.

1122056C **AFE_ASRC_CON20** **ASRC Config 20** **00001B00**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI2_AUTORST_TH_HIGH[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI2_AUTORST_TH_HIGH[15:0]															
Type	RW															
Reset	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	FREQ_CALI2_AUTORST_TH_HIGH	**Frequency calibrator 2 auto reset threshold high bound** When the calibration result is bigger than this value, HW will auto reset freq_cali2/ring2/history status when the calibration result returns to normal value. Enabling 0x55c[14] is required.

11220570 **AFE_ASRC_CON21** **ASRC Config 21** **00001800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI2_AUTORST_TH_LOW[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI2_AUTORST_TH_LOW[15:0]															
Type	RW															
Reset	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	FREQ_CALI2_AUTORST_TH_LOW	**Frequency calibrator 2 auto reset threshold low bound** When the calibration result is smaller than this value, HW will auto reset freq_cali2/ring2/history status when the calibration result returns to normal value. Enabling 0x55c[14] is required.

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11220578 **AFE_ASRC_CON23** **ASRC Config 23** **00001B00**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_AUTORST_TH_HIGH[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FREQ_CALI_AUTORST_TH_HIGH[15:0]															
Type	RW															
Reset	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	FREQ_CALI_AUTORST_TH_HIGH	**High period calibration threshold to trigger autoreset** Enabling 0x718[15] is required.

1122057C **AFE_ASRC4_CON24** **ASRC Config 24** **00001800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_AUTORST_TH_LOW[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FREQ_CALI_AUTORST_TH_LOW[15:0]															
Type	RW															
Reset	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	FREQ_CALI_AUTORST_TH_LOW	**Low period calibration threshold to trigger autoreset** Enabling 0x718[15] is required.

112206C0 **AFE_ASRC4_CON0** **ASRC4 Config 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			CHSET1_CLR_IIR_HISTORY	CHSET1_IS_MONO	CHSET1_OFS_SEL		CHSET1_IFS_SEL		CHSET1_IIR_EN	CHSET1_IIR_STAGE					CHSET0_CLR_IIR_HISTORY	CHSET0_IS_MONO
Type			Other	RW	RW		RW		RW	RW					Other	RW
Reset			0	0	0	0	0	0	0	0	0	0			0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CHSET0_OFS_SEL		CHSET0_IFS_SEL		CHSET0_IIR_EN	CHSET0_IIR_STAGE					CHSET_STR_CLR		CHSET_ON		COEF_SRAM_CTRL	ASM_ON
Type	RW		RW		RW	RW					Other		RU		RW	RW
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
29	CHSET1_CLR_IIR_HISTORY	**Set to 1 to clear the current IIR output history buffer for RX.** This register will be auto-cleared once the histories are cleared.
28	CHSET1_IS_MONO	**Mono/Stereo selection register**
27:26	CHSET1_OFS_SEL	**Selects output sample rate for RX** Set to 01 for OFS fix value.
25:24	CHSET1_IFS_SEL	**Selects input sample rate for RX** Set to 10 for frequency tracking mode.
23	CHSET1_IIR_EN	**Enables anti-alias IIR filter for RX** Set 1 to Turns on anti-alias IIR filter.
22:20	CHSET1_IIR_STAGE	**Anti-alias IIR filter stage for RX** Defines how many 2-order IIR stages are cascaded for the anti-alias filter. This value should be "real stage amount" minus 1, which means up to 8 stages and 16 orders are supported.
17	CHSET0_CLR_IIR_HISTORY	**Set to 1 to clear current IIR output history buffer for TX.** This register will auto-cleared once the histories are cleared.
16	CHSET0_IS_MONO	**Mono/Stereo selection register**
15:14	CHSET0_OFS_SEL	**Selects output sample rate for TX** Set to 00 for OFS fix value.
13:12	CHSET0_IFS_SEL	**Selects input sample rate selection for TX** Set to 11 for period tracking mode.
11	CHSET0_IIR_EN	**Enables anti-alias IIR filter for TX** Set to 1 to turn on anti-alias IIR filter.
10:8	CHSET0_IIR_STAGE	**Anti-alias IIR filter stage for TX** Defines how many 2-order IIR stages are cascaded for the anti-alias filter. This value should be "real stage amount" minus 1, which means up to 8 stages and 16 orders are supported.
5:4	CHSET_STR_CLR	**Each channel set clear signal** Set bit 0 to 1 to clear the TX history. Set bit 1 to 1 to clear the RX history. Set bit 2 to 1 to clear the I2S history.
3:2	CHSET_ON	**Indicates which channel set is on currently** 01: TX 10: RX
1	COEFF_SRAM_CTRL	**Controls coefficient SRAM access** 0: Disable access 1: Enable access
0	ASM_ON	**ASRC enabling signal** Turn it on after all configurations are set. 0: Disable ASRC 1: Enable ASRC

112206C4 **AFE_ASRC4_CON1** **ASRC4 Config 1** **00000CB2**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_0[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_0[15:0]															
Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

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Bit(s)	Name	Description
23:0	ASM_FREQ_0	**Frequency palette** The frequency palette for each channel is set to define its input frequency and output frequency. Default: Set for TX OFS.

112206C8 **AFE_ASRC4_CON2** **ASRC4 Config 2** **00400000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_1[23:16]							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	ASM_FREQ_1	**Frequency palette** The frequency palette for each channel is set to define its input frequency and output frequency. Default: Set for RX OFS.

112206CC **AFE_ASRC4_CON3** **ASRC4 Config 3** **00400000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_2[23:16]							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	ASM_FREQ_2	**Frequency palette** The frequency palette for each channel is set to define its input frequency and output frequency. Default: Set for RX IFS.

112206D0 **AFE_ASRC4_CON4** **ASRC4 Config 4** **00000CB2**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_3[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_3[15:0]															
Type	RW															

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Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Name	Description
23:0	ASM_FREQ_3	**Frequency palette** The frequency palette for each channel is set to define its input frequency and output frequency. Default: Set for TX IFS.

112206D4 AFE_ASRC4_CON5 ASRC4 Config 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RESULT_SEL		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	RESULT_SEL	**Selects output** 000: ASRC output 001: Data input 010: CMPF output 011: HBF1 output 100: HBF2 output 101: HBF3 output 110: HBF4 output 111: Each IIR stage output in order

112206D8 AFE_ASRC4_CON6 ASRC4 Config 6 00010800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FREQ_CALI_CYCLE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_EN		FREQ_CALC_RUNNING	AUTO_TUNE_FREQ3	COMP_FREQ_RES_EN		FREQ_CALI_SEL		FREQ_CALI_BP_DGL	FREQ_CALI_MAX_GWIDTH			AUTO_TUNE_FREQ2	FREQ_CALI_AUTO_RESTART	CALI_USE_FREQ_OUT	CALI_EN
Type	RW		RU	RW	RW		RW		RW	RW			RW	RW	RW	RU
Reset	0		0	0	1		0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	FREQ_CALI_CYCLE	**Frequency calibrating cycle register** Defines how many input signal cycles the calibrator calibrates are in one round. This register is updated into calibrator once the calibrator enable [0] is turned on.
15	FREQ_CALI_AUTORST_EN	**Enables period calibration auto-reset** Period calibration bigger than 0x734 or smaller than 0x738 will trigger ASRC

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Bit(s)	Name	Description
		reset.
13	FREQ_CALC_RUNNING	**Shows if frequency calculation is running** For one round running case, wait for this bit and the CALI_EN bit to become low before frequency result is ready.
12	AUTO_TUNE_FREQ3	**Enables asm_freq_3 auto update with the calibrator result once the calibrator completes one round** 0: Disable auto update 1: Enable auto update
11	COMP_FREQ_RES_EN	**Frequency compensation enabling register** 0: Disable compensation 1: Enable compensation
9:8	FREQ_CALI_SEL	**Calibrator input source selection register** Before modifying this register, make sure the calibrator is turned off. 00: Use PCM SYNC word 01: Not connected 10: Not connected 11: Not connected
7	FREQ_CALI_BP_DGL	**Bypasses deglitch circuit for calibrator input** 0: No bypass 1: Bypass
6:4	FREQ_CALI_MAX_GWIDTH	**Defines maximum glitch width of calibrator input signal** Unit: Calibrator reference clock cycles.
3	AUTO_TUNE_FREQ2	**Enables asm_freq_2 auto update with the calibrator result once the calibrator completes one round** 0: Disable auto update 1: Enable auto update
2	FREQ_CALI_AUTO_RESTART	**Enables calibrator auto restart new calibration when one run is completed. This value will be updated into calibrator once the enabling signal is turned on from off state.** 0: Disable auto restart 1: Enable auto restart
1	CALI_USE_FREQ_OUT	**Selects frequency or period calibration mode** 0: Use period calibration result to update asm_freq_2. Use frequency calibration result to update asm_freq_3 1: Use frequency calibration result to update asm_freq_2. Use period calibration result to update asm_freq_3
0	CALI_EN	**Enables frequency calibrator** If auto restart is 0, this bit will be cleared when one calibration run is completed. If this bit is set to 0, wait until this bit to become 0 before making the next run start safely. 0: Disable calibrator 1: Enable calibrator

112206DC **AFE_ASRC4_CON7** **ASRC4 Config 7** **00000659**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALC_DENOMINATOR[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALC_DENOMINATOR[15:0]															
Type	RW															
Reset	0	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1

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Bit(s)	Name	Description
23:0	FREQ_CALC_DENOMINATOR	Determines the denominator for performing period-to-frequency calibration result translation

112206E0 **AFE_ASRC4_CON8** **ASRC4 Config 8** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									PRD_CALI_RESULT_RECORD[23:16]							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRD_CALI_RESULT_RECORD[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	PRD_CALI_RESULT_RECORD	**Period calibration result** Records the calibration result of the previous round. Writing any value to this register will clear the result.

112206E4 **AFE_ASRC4_CON9** **ASRC4 Config 9** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_RESULT[23:16]							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_RESULT[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	FREQ_CALI_RESULT	**Frequency calibrator result** Records the calibration result of the previous round. This value is got from the quotient (FREQ_CALC_DENOMINATOR/PRD_CALI_RESULT) in 1.23 format.

112206E8 **AFE_ASRC4_CON10** **ASRC4 Config 10** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									COEFF_SRAM_DATA[23:16]							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COEFF_SRAM_DATA[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
23:0	COEFF_SRAM_DATA	**Read/Write data port of coefficient SRAM** Read data have one cycle delay. The coefficients are filled stage by stage: each stage has 6 coefficients. For the 2nd-order IIR filter with transfer function of one stage as: "(2^shift)*a0 + (2^shift)*a1*Z^-1 + (2^shift)*a2*Z^-2/1 + (2^shift)*b1*Z^ -1 + (2^shift)*b2*Z^-2" The coefficient should be filled as (from low address to high address) a2 a1 a0 -b1 -b2 shift

112206EC **AFE_ASRC4_CON11** **ASRC4 Config 11** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										COEFF_SRAM_ADR						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	COEFF_SRAM_ADR	**Determines the rd/wr address of IIR coefficient SRAM** Read/Write COEFF_SRAM_DATA will make this register increase by 1.

112206F4 **AFE_ASRC4_CON13** **ASRC4 Config 13** **00001B00**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_AUTORST_TH_HIGH[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_TH_HIGH[15:0]															
Type	RW															
Reset	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	FREQ_CALI_AUTOR ST_TH_HIGH	**High period calibration threshold to trigger auto reset** Enabling 0x718[15] is required.

112206F8 **AFE_ASRC4_CON14** **ASRC4 Config 14** **00001800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_AUTORST_TH_LOW[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_TH_LOW[15:0]															
Type	RW															
Reset	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
23:0	FREQ_CALI_AUTORST_TH_LOW	**Low period calibration threshold to trigger auto reset** Enabling 0x718[15] is required.

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6 Multimedia Subsystem

6.1 Multimedia Subsystem

6.1.1 Multimedia Subsystem Configuration

6.1.1.1 Introduction

The multimedia subsystem contains multimedia controller, multimedia data path v2.0 (MDP 2.0) and display (DISP). The multimedia controller includes bus fabric control, Smart Memory Interface (SMI) control, memory access second level arbiter, and multimedia configuration. It plays the key role to handle different handshaking between infra subsystem, video subsystem, image subsystem and G3D subsystem. MDP 2.0 is the time sharing pipeline data flow controller to process resizing and rotation by memory access. The display pipeline outputs pixels to display interface with overlay, color enhancement, adaptive ambient light processing, color correction and gamma correction.

6.1.1.2 Features

The multimedia subsystem has the following features:

- APB bus fabric control center
- Smart Multimedia Interface (SMI) controller
- Second level arbiter for memory access request
- Multimedia Data Path v2.0. It has one read DMA, two resizers, one 2D-sharpness enhancement, one write DMA and one write rotator
- Two display pipe lines. One of the pipelines has its own read DMA, overlay, color engine, adaptive ambient light processing, color correction, gamma correction and display interface controller as basic components. The other one only includes read DMA and display interface controller.
- Supports 3D display
- Supports color enhancement engine
- Supports adaptive ambient light processing for backlight power saving and sunlight visibility improvement
- Supports color correction and gamma correction for accurate image reproduction
- Supports concurrent dual display output
- Display output interface: 1 DSI and 1 DPI. DPI interface can connect to external LVDS, HDMI, and MHL bridge chips to support these interfaces.

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6.1.1.3 Block Diagram

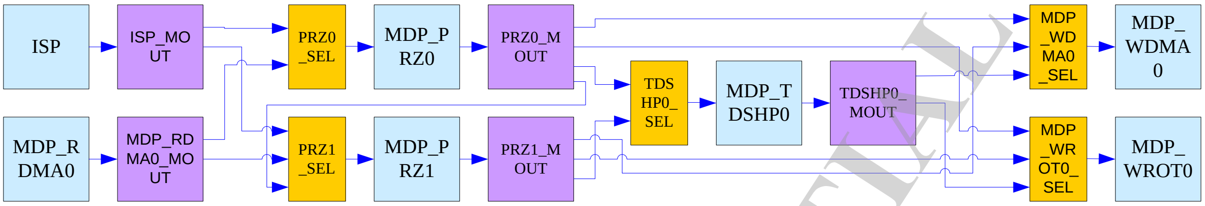

Figure 6-1. MDP function blocks of multimedia partition

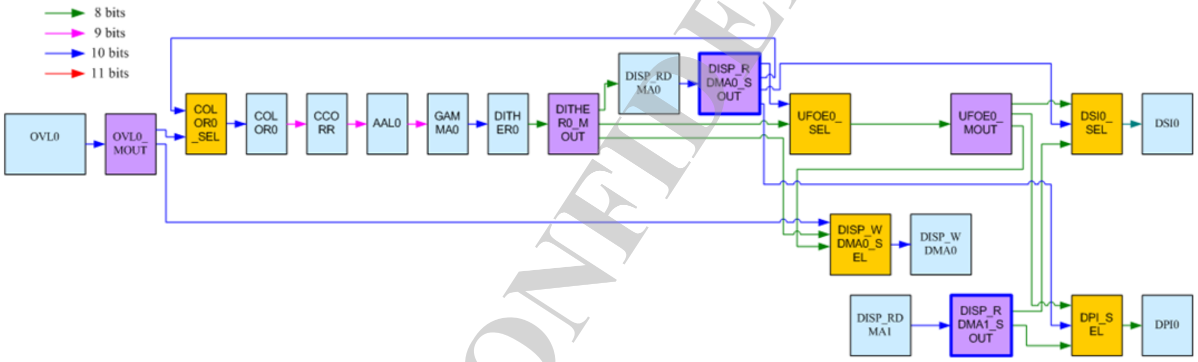

Figure 6-2. DISP function blocks of multimedia partition

6.1.1.4 Register Definition

Module name: MMSYS_CONFIG Base address: (+14000000h)

Address	Name	Width	Register Function
14000000	**MMSYS_INTEN**	32	MMSYS Interrupt Enable
14000004	**MMSYS_INTSTA**	32	MMSYS Interrupt Status
1400000C	**PWM_APB_ERR_ADDR**	32	PWM APB TX Error Address
1400001C	**ISP_MOUT_EN**	16	ISP_MDP Multiple Output Enable
14000020	**MDP_RDMA_MOUT_EN**	16	MDP_RDMA Multiple Output Enable
14000024	**MDP_PRZ0_MOUT_EN**	16	MDP Resize0 Multiple Output Enable
14000028	**MDP_PRZ1_MOUT_EN**	16	MDP Resize1 Multiple Output Enable
1400002C	**MDP_TDSHP_MOUT_EN**	16	MDP 2D Sharpness Multiple Output Enable
14000030	**DISP_OVL0_MOUT_EN**	16	Display Overlay0 Multiple Output Enable
14000038	**DISP_DITHER_MOUT_EN**	16	Display Dither Multiple Output Enable
1400003C	**DISP_UFOE_MOUT_EN**	16	Display UFOE Multiple Output Enable
14000040	**MMSYS_MOUT_RST**	16	MMSYS Multiple Output Reset

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Address	Name	Width	Register Function
14000044	MDP_PRZ0_SEL_IN	16	MDP PRZ0 Input Selection
14000048	MDP_PRZ1_SEL_IN	16	MDP PRZ1 Input Selection
1400004C	MDP_TDSHP_SEL_IN	16	MDP TDSHP Input Selection
14000050	MDP_WDMA_SEL_IN	16	MDP WDMA Input Selection
14000054	MDP_WROT_SEL_IN	16	MDP WROT Input Selection
14000058	DISP_COLOR_SEL_IN	16	DISP_COLOR Input Selection
1400005C	DISP_WDMA_SEL_IN	16	DISP_WDMA Input Selection
14000060	DISP_UFOE_SEL_IN	16	DISP_UFOE Input Selection
14000064	DSI0_SEL_IN	16	DSI0 Input Selection
14000068	DPI0_SEL_IN	16	DPI0 Input Selection
1400006C	DISP_RDMA0_SOUT_SEL_IN	16	DISP_RDMA0 Output Select
14000070	DISP_RDMA1_SOUT_SEL_IN	16	DISP_RDMA1 Output Select
140000F0	MMSYS_MISC	16	MMSYS_MISC
14000100	MMSYS_CG_CON0	32	MMSYS Clock Gating Config 0
14000104	MMSYS_CG_SET0	32	MMSYS Clock Gating Set 0
14000108	MMSYS_CG_CLR0	32	MMSYS Clock Gating Clear 0
14000110	MMSYS_CG_CON1	32	MMSYS Clock Gating Config 1
14000114	MMSYS_CG_SET1	32	MMSYS Clock Gating Set 1
14000118	MMSYS_CG_CLR1	32	MMSYS Clock Gating Clr 1
14000120	MMSYS_HW_DCM_DIS0	32	DISP Hardware DCM Disable 0
14000124	MMSYS_HW_DCM_DIS_SET0	32	MMSYS Hardware DCM Disable Set 0
14000128	MMSYS_HW_DCM_DIS_CLR0	32	MMSYS Hardware DCM Disable Clear 0
14000140	MMSYS_SW0_RST_B	32	MMSYS Software Reset
14000144	MMSYS_SW1_RST_B	32	MMSYS Software Reset
14000150	MMSYS_LCM_RST_B	32	LCM Reset
14000200	DISP_FAKE_ENG_EN	32	DISP Fake Engine Enable
14000204	DISP_FAKE_ENG_RST	32	DISP Fake Engine Reset
14000208	DISP_FAKE_ENG_CON0	32	DISP Fake Engine Control 0
1400020C	DISP_FAKE_ENG_CON1	32	DISP Fake Engine Control 1
14000210	DISP_FAKE_ENG_RD_ADDR	32	DISP Fake Engine Read Address
14000214	DISP_FAKE_ENG_WR_ADDR	32	DISP Fake Engine Write Address

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Address	Name	Width	Register Function
14000218	DISP_FAKE_ENG_STATE	32	DISP Fake Engine Status
14000800	MMSYS_MBIST_CON	32	MMSYS MBIST Control
14000804	MMSYS_MBIST_DONE	32	MMSYS MBIST Done
14000808	MMSYS_MBIST_HOLDB	32	MMSYS MBIST holdb
1400080C	MMSYS_MBIST_MODE	32	MMSYS MBIST Mode
14000810	MMSYS_MBIST_FAIL0	32	MMSYS MBIST Fail 0
14000814	MMSYS_MBIST_FAIL1	32	MMSYS MBIST Fail 1
14000820	MMSYS_MBIST_BSEL0	32	MMSYS MBIST BSEL 0
14000824	MMSYS_MBIST_BSEL1	32	MMSYS MBIST BSEL 1
14000830	MMSYS_MEM_DELSEL0	32	MMSYS Memory Delay Select 0
14000834	MMSYS_MEM_DELSEL1	32	MMSYS Memory Delay Select 1
14000838	MMSYS_MEM_DELSEL2	32	MMSYS Memory Delay Select 2
1400083C	MMSYS_MEM_DELSEL3	32	MMSYS Memory Delay Select 3
14000880	MMSYS_DEBUG_OUT_SEL	32	MMSYS Debug Output Select
14000890	MMSYS_DUMMY0	32	MMSYS Dummy Register 0
14000894	MMSYS_DUMMY1	32	MMSYS Dummy Register 1
14000898	MMSYS_DUMMY2	32	MMSYS Dummy Register 2
1400089C	MMSYS_DUMMY3	32	MMSYS Dummy Register 3
140008A0	DISP_DL_VALID_0	32	DISP Direct Link Valid Status 0
140008A4	DISP_DL_READY_0	32	DISP Direct Link READY Status 0
140008A8	MDP_DL_VALID_0	32	MDP Direct Link Valid Status 0
140008AC	MDP_DL_READY_0	32	MDP Direct Link READY Status 0
140008D0	SMI_LARB0_GREQ	32	SMI LARB0 Request

14000000 MMSYS_INTEN MMSYS Interrupt Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name									MMSYS_INTEN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
7:0	**MMSYS_INTEN**	MMSYS_INTEN	**Enables MMSYS interrupt** 0: Disable this interrupt source 1: Enable this interrupt source bit 0: mmsys to MFG APB TX error bit 1: PWM0 APB TX error

14000004 MMSYS_INTSTA MMSYS Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name															MMSYS_INTSTA	
Type															A1	
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1:0	**MMSYS_INTSTA**	MMSYS_INTSTA	**MMSYS interrupt status** 0: No interrupt occurs 1: Interrupt occurs bit 0: mmsys to MFG APB TX error bit 1: PWM0 APB TX error

1400000C PWM_APB_ERR_ADDR PWM APB TX Error Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					PWM0_APB_ERR_ADDR											
Type					RU											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0	**PWM0_APB_ERR_ADDR**	PWM0_APB_ERR_ADDR	Address to make PWM0 APB TX error

1400001C ISP_MOUT_EN ISP_MDP Multiple Output Enable 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															ISP_MOUT_EN	
Type															RW	
Reset															0	0

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Bit(s)	Mnemonic	Name	Description
1:0	**ISP_MOUT_EN**	ISP_MOUT_EN	**Enables ISP_MDP multiple output** 0: Disable this output port 1: Enable this output port bit 0: Output to PRZ0 bit 1: Output to PRZ1

14000020 MDP_RDMA_MOUT_EN MDP_RDMA Multiple Output Enable 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**MDP_RDMA_MOUT_EN**	
Type															RW	
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1:0	**MDP_RDMA_MOUT_EN**	MDP_RDMA_MOUT_EN	**Enables MDP_RDMA multiple output** 0: Disable this output port 1: Enable this output port bit 0: Output to PRZ0 bit 1: Output to PRZ1

14000024 MDP_PRZ0_MOUT_EN MDP Resize0 Multiple Output Enable 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**MDP_PRZ0_MOUT_EN**			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**MDP_PRZ0_MOUT_EN**	MDP_PRZ0_MOUT_EN	**Enables MDP Resize0 multiple output** 0: Disable this output port 1: Enable this output port bit 0: Output to MDP_WDMA bit 1: Output to MDP_WROT bit 2: Output to MDP_TDSHP bit 3: Output to MDP_RSZ1

14000028 MDP_PRZ1_MOUT_EN MDP Resize1 Multiple Output Enable 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**MDP_PRZ1_MOUT_EN**		
Type														RW		
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2:0	**MDP_PR**	MDP_PRZ1_MO	**Enables MDP Resize1 multiple output**

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Bit(s)	Mnemonic	Name	Description
	Z1_MOUT_EN	UT_EN	0: Disable this output port 1: Enable this output port bit 0: Output to MDP_WDMA bit 1: Output to MDP_WROT bit 2: Output to MDP_TDSHP

1400002C **MDP_TDSHP_MOUT_EN** **MDP 2D Sharpness Multiple Output Enable** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**MDP_TDSHP_MOUT_EN**	
Type															RW	
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1:0	**MDP_TDSHP_MOUT_EN**	MDP_TDSHP_MOUT_EN	**Enables MDP 2D sharpness multiple output** 0: Disable this output port 1: Enable this output port bit 0: Output to MDP_WDMA bit 1: Output to MDP_WROT

14000030 **DISP_OVL0_MOUT_EN** **Display Overlay0 Multiple Output Enable** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**DISP_OVL0_MOUT_EN**	
Type															RW	
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1:0	**DISP_OVL0_MOUT_EN**	DISP_OVL0_MOUT_EN	**Enables display overlay0 multiple output** 0: Disable this output port 1: Enable this output port bit 0: Output to DISP_COLOR bit 1: Output to DISP_WDMA

14000038 **DISP_DITHER_MOUT_EN** **Display Dither Multiple Output Enable** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**DISP_DITHER_MOUT_EN**		
Type														RW		
Reset														0	0	0

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Bit(s)	Mnemonic	Name	Description
2:0	**DISP_DITHER_MOUT_EN**	DISP_DITHER_MOUT_EN	**Enables display dither multiple output** 0: Disable this output port 1: Enable this output port bit 0: Output to DISP_RDMA0 bit 1: Output to DISP_UFOE bit 2: Output to DISP_WDMA

1400003C DISP_UFOE_MOUT_EN Display UFOE Multiple Output Enable 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														DISP_UFOE_MOUT_EN		
Type														RW		
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2:0	**DISP_UFOE_MOUT_EN**	DISP_UFOE_MOUT_EN	**Enables display UFOE multiple output** 0: Disable this output port 1: Enable this output port bit 0: Output to DSI bit 1: Output to DPI bit 2: Output to DISP_WDMA

14000040 MMSYS_MOUT_RST MMSYS Multiple Output Reset 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MMSYS_MOUT_RST								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0	**MMSYS_MOUT_RST**	MMSYS_MOUT_RST	**Resets MMSYS multiple output** 0: Does not reset 1: Reset bit 0: Reset ISP_MDP multiple output bit 1: Reset MDP_RDMA multiple output bit 2: Reset MDP_PRZ0 multiple output bit 3: Reset MDP_PRZ1 multiple output bit 4: Reset MDP_TDSHP multiple output bit 5: Reset DISP_OVL0 multiple output bit 6: Reserved bit 7: Reset DISP_DITHER multiple output bit 8: Reset DISP_UFOE multiple output

14000044 MDP_PRZ0_SEL_IN MDP PRZ0 Input Selection 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MDP_PR

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																Z0_SEL_IN
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	MDP_PRZ0_SEL_IN	MDP_PRZ0_SEL_IN	**Selects MDP PRZ0 input** 0: From ISP_MDP 1: From MDP_RDMA0 Others: Reserved

14000048 **MDP_PRZ1_SEL_IN** **MDP PRZ1 Input Selection** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															MDP_PRZ1_SEL_IN	
Type															RW	
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1:0	MDP_PRZ1_SEL_IN	MDP_PRZ1_SEL_IN	**Selects MDP PRZ1 input** 0: From ISP_MDP 1: From MDP_RDMA0 2: From MDP_PRZ0 Others: Reserved

1400004C **MDP_TDSHP_SEL_IN** **MDP TDSHP Input Selection** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MDP_TDSHP_SEL_IN
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	MDP_TDSHP_SEL_IN	MDP_TDSHP_SEL_IN	**Selects MDP TDSHP input** 0: From MDP_PRZ0 1: From MDP_PRZ1 Others: Reserved

14000050 **MDP_WDMA_SEL_IN** **MDP WDMA Input Selection** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															MDP_WDMA_SEL_I	

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															N	
Type															RW	
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1:0	MDP_WDMA_SEL_IN	MDP_WDMA_SEL_IN	**Selects MDP WDMA input** 0: From MDP_PRZ0 1: From MDP_PRZ1 2: From MDP_TDSHP Others: Reserved

14000054 MDP_WROT_SEL_IN MDP WROT Input Selection 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															MDP_WROT_SEL_IN	
Type															RW	
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1:0	MDP_WROT_SEL_IN	MDP_WROT_SEL_IN	**Selects MDP WROT input** 0: From MDP_PRZ0 1: From MDP_PRZ1 2: From MDP_TDSHP Others: Reserved

14000058 DISP_COLOR_SEL_IN DISP_COLOR Input Selection 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DISP_COLOR_SEL_IN
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	DISP_COLOR_SEL_IN	DISP_COLOR_SEL_IN	**Selects DISP_COLOR input** 0: From DISP_RDMA0 1: From DISP_OVL0 Others: Reserved

1400005C DISP_WDMA_SEL_IN DISP_WDMA Input Selection 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															DISP_WDMA_SEL_I	

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															N	
Type															RW	
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1:0	**DISP_WDMA_SEL_IN**	DISP_WDMA_SEL_IN	**Selects DISP_WDMA input** 0: From DISP_OVL0 1: From DISP_DITHER 2: From DISP_UFOE Others: Reserved

14000060 **DISP_UFOE_SEL_IN** **DISP_UFOE Input Selection** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DISP_UFOE_SEL_IN
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**DISP_UFOE_SEL_IN**	DISP_UFOE_SEL_IN	**Selects DISP_UFOE input** 0: From DISP_RDMA0 1: From DISP_DITHER Others: Reserved

14000064 **DSI0_SEL_IN** **DSI0 Input Selection** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															DSI0_SEL_IN	
Type															RW	
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1:0	**DSI0_SEL_IN**	DSI0_SEL_IN	**Selects DSI0 input** 0: From DISP_UFOE 1: From DISP_RDMA0 2: From DISP_RDMA1 Others: Reserved

14000068 **DPI0_SEL_IN** **DPI0 Input Selection** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															DPI0_SEL_IN	
Type															RW	
Reset															0	0

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Bit(s)	Mnemonic	Name	Description
1:0	DPI0_SEL_IN	DPI0_SEL_IN	**Selects DPI0 input** 0: From DISP_UFOE 1: From DISP_RDMA0 2: From DISP_RDMA1 Others: Reserved

14000006C **DISP_RDMA0_SOUT_SEL_IN** **DISP_RDMA0 Output Select** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															DISP_RDMA0_SOUT_SEL_IN	
Type															RW	
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1:0	DISP_RDMA0_SOUT_SEL_IN	DISP_RDMA0_SOUT_SEL_IN	**Selects DISP_RDMA0 output** 0: Output to DISP_UFOE 1: Output to DISP_COLOR0 2: Output to DSI0 3: Output to DPI0

14000070 **DISP_RDMA1_SOUT_SEL_IN** **DISP_RDMA1 Output Select** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DISP_RDMA1_SOUT_SEL_IN
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	DISP_RDMA1_SOUT_SEL_IN	DISP_RDMA1_SOUT_SEL_IN	**Selects DISP_RDMA1 output** 0: Output to DSI0 1: Output to DPI0

140000F0 **MMSYS_MISC** **MMSYS_MISC** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SMI_LA

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																RB0_TEST_MODE
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**SMI_LARB0_TEST_MODE**	SMI_LARB0_TEST_MODE	**SMI_LARB0 test mode** 0: Normal mode 1: SMI_LARB0 test mode. All RDMA's output ready is tied to 1; all WDMA's input valid is tied to 1.

14000100 **MMSYS_CG_CON0** **MMSYS Clock Gating Config 0** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CG_CON0[31:16]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CG_CON0[15:0]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0	**CG_CON0**	CG0	**Free run clock gating** bit 0: SMI COMMON bit 1: SMI LARB0 bit 2: CAM_MDP bit 3: MDP_RDMA bit 4: MDP_RSZ0 bit 5: MDP_RSZ1 bit 6: MDP_TDSHP bit 7: MDP_WDMA bit 8: MDP_WROT bit 9: FAKE_ENG bit 10: DISP_OVL0 bit 11: DISP_RDMA0 bit 12: DISP_RDMA1 bit 13: DISP_WDMA bit 14: DISP_COLOR bit 15: DISP_CCORR bit 16: DISP_AAL bit 17: DISP_GAMMA bit 18: DISP_DITHER bit 19: DISP_UFOE 0: Enable clock 1: Clock gating

14000104 **MMSYS_CG_SET0** **MMSYS Clock Gating Set 0** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CG_SET0[31:16]															
Type	WO															

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Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CG_SET0[15:0]															
Type	WO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0	CG_SET0	CG0	**Sets up free run clock gating** 0: No effect 1: Clock gating

14000108 MMSYS_CG_CLR0 MMSYS Clock Gating Clear 0 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CG_CLR0[31:16]															
Type	WO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CG_CLR0[15:0]															
Type	WO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0	CG_CLR0	CG0	**Clears free run clock gating** 0: No effect 1: Enable clock

14000110 MMSYS_CG_CON1 MMSYS Clock Gating Config 1 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CG_CON1[31:16]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CG_CON1[15:0]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0	CG_CON1	CG1	**Free run clock gating** bit 0: DISP_PWM MM clock bit 1: DISP_PWM 26M clock bit 2: DSI engine bit 3: DSI digital bit 4: DPI pixel clock bit 5: DPI engine clock Others: Reserved 0: Enable clock 1: Clock gating

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14000114 **MMSYS_CG_SET1** **MMSYS Clock Gating Set 1** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CG_SET1[31:16]															
Type	WO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CG_SET1[15:0]															
Type	WO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0	CG_SET1	CG1	**Sets up free run clock gating** 0: No effect 1: Clock gating

14000118 **MMSYS_CG_CLR1** **MMSYS Clock Gating Clr 1** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CG_CLR1[31:16]															
Type	WO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CG_CLR1[15:0]															
Type	WO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0	CG_CLR1	CG1	**Clears free run clock gating** 0: No effect 1: Enable clock

14000120 **MMSYS_HW_DCM_DIS0** **DISP Hardware DCM Disable 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HW_DCM_DIS0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_DCM_DIS0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	HW_DCM_DIS0	DCM_DIS0	**Disables hardware DCM 0** bit 0: MDP_RDMA bit 1: MDP_RSZ0 bit 2: MDP_RSZ1 bit 3: MDP_TDSHP bit 4: MDP_WDMA bit 5: MDP_WROT

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Bit(s)	Mnemonic	Name	Description
			bit 6: DISP_OVL0 bit 7: DISP_RDMA0 bit 8: DISP_RDMA1 bit 9: DISP_WDMA bit 10: DISP_COLOR bit 11: DISP_CCORR bit 12: DISP_AAL bit 13: DISP_GAMMA bit 14: DISP_DITHER bit 15: DISP_UFOE bit 16: DSI0 Others: Reserved 0: Enable HW DCM 1: Disable HW DCM

14000124 **MMSYS_HW_DCM_DIS_SET0** **MMSYS Hardware DCM Disable Set 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HW_DCM_DIS_SET0[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_DCM_DIS_SET0[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	HW_DCM_DIS_SET0	DCM_DIS0	**Sets up hardware DCM 0 disable** 0: No effect 1: Disable HW DCM

14000128 **MMSYS_HW_DCM_DIS_CLR0** **MMSYS Hardware DCM Disable Clear 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HW_DCM_DIS_CLR0[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_DCM_DIS_CLR0[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	HW_DCM_DIS_CLR0	DCM_DIS0	**Clears hardware DCM 0 disable** 0: No effect

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14000140 MMSYS_SW0_RST_B MMSYS Software Reset FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SW0_RST_B[31:16]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SW0_RST_B[15:0]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0	**SW0_RST_B**	SW0_RST_B	**Software reset 0** bit 0: SMI COMMON bit 1: SMI LARB0 bit 2: CAM_MDP bit 3: MDP_RDMA bit 4: MDP_RSZ0 bit 5: MDP_RSZ1 bit 6: MDP_TDSHP bit 7: MDP_WDMA bit 8: MDP_WROT bit 9: FAKE_ENG bit 10: MUTEX bit 11: DISP_OVL0 bit 12: DISP_RDMA0 bit 13: DISP_RDMA1 bit 14: DISP_WDMA0 bit 15: DISP_COLOR bit 16: DISP_CCORR bit 17: DISP_AAL bit 18: DISP_GAMMA bit 19: DISP_DITHER bit 20: DISP_UFOE bit 21: DISP_PWM bit 22: DSI bit 23: DPI 0: Reset 1: Does not reset

14000144 MMSYS_SW1_RST_B MMSYS Software Reset FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SW1_RST_B[31:16]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SW1_RST_B[15:0]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0	**SW1_RST_B**	SW1_RST_B	Software reset 1

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14000150	MMSYS_LCM_RST_B	LCM Reset	00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MMSYS_LCM_RST_B
Type																RW
Reset																1

Bit(s)	Mnemonic	Name	Description
0	MMSYS_LCM_RST_B	MMSYS_LCM_RST_B	**Resets LCM** 0: Reset 1: Does not reset

14000200	DISP_FAKE_ENG_EN	DISP Fake Engine Enable	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															DFE_START	DFE_MUX_SEL
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	DFE_START	DFE_START	**After this bit is enabled, DFE starts to issue read/write command immediately.** Programming sequence: Write DISP_FAKE_ENG_CON0; Write DISP_FAKE_ENG_CON1; Write DISP_FAKE_ENG_RD_ADDR; Write DISP_FAKE_ENG_WR_ADDR; Write DISP_FAKE_ENG_EN = 1; Write DISP_FAKE_ENG_EN = 3; While ((*DISP_FAKE_ENG_STATE & 1)!=0); *DISP_FAKE_ENG = 1; 0: Stop DFE 1: Start DFE
0	DFE_MUX_SEL	DFE_MUX_SEL	**DISP_FAKE_ENG (DFE) shares the SMI port with CMDQ.** Before starting DFE, mux selection should be enabled. 0: Disable DFE mux selection 1: Enable DFE mux selection

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14000204	DISP_FAKE_ENG_RST	DISP Fake Engine Reset	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DISP_FAKE_ENG_RST
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	DISP_FAKE_ENG_RST	DISP_FAKE_ENG_RST	**Resets DISP fake engine** 0: Does not reset 1: Reset

14000208	DISP_FAKE_ENG_CON0	DISP Fake Engine Control 0	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									DFE_DRE_EN	DFE_LOOP_MODE			DFE_TEST_LEN[19:16]			
Type									RW	RW			RW			
Reset									0	0			0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DFE_TEST_LEN[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23	DFE_DRE_EN	DFE_DRE_EN	**When DRE is enabled, DFE keeps busy but masks the commands to EMI.** 0: Disable 1: Enable
22	DFE_LOOP_MODE	DFE_LOOP_MODE	**When loop mode is enabled, DFE issues read/write command continuously until DISP_FAKE_ENG_EN[1]=0** 0: Normal mode 1: Enable loop mode
19:0	DFE_TEST_LEN	DFE_TEST_LEN	**DFE test length in normal mode**

1400020C	DISP_FAKE_ENG_CON1	DISP Fake Engine Control 1	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

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Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DFE_WR_DIS	DFE_RD_DIS	DFE_SLOW_DOWN									
Type					RW	RW	RW									
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11	**DFE_WR_DIS**	DFE_WR_DIS	**Disables DFE write commands** 0: Enable write requests 1: Disable write requests
10	**DFE_RD_DIS**	DFE_RD_DIS	**Disables DFE read commands** 0: Enable read requests 1: Disable read requests
9:0	**DFE_SLOW_DOWN**	DFE_SLOW_DOWN	**Slow down counter**

14000210 DISP_FAKE_ENG_RD_ADDR DISP Fake Engine Read Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DISP_FAKE_ENG_RD_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DISP_FAKE_ENG_RD_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DISP_FAKE_ENG_RD_ADDR**	DISP_FAKE_ENG_RD_ADDR	DISP fake engine read address

14000214 DISP_FAKE_ENG_WR_ADDR DISP Fake Engine Write Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DISP_FAKE_ENG_WR_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DISP_FAKE_ENG_WR_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DISP_FA**	DISP_FAKE_EN	DISP fake engine write Address

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Bit(s)	Mnemonic	Name	Description
	KE_ENG _WR_AD DR	G_WR_ADDR	

14000218 **DISP_FAKE_ENG_STATE** **DISP Fake Engine Status** **00001100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DFE_RD_ST			DFE_WR_ST											DFE_BUSY
Type		RU			RU											RU
Reset		0	0	1	0	0	0	1								0

Bit(s)	Mnemonic	Name	Description
14:12	**DFE_RD _ST**	DFE_RD_ST	**DFE read engine state** 001: Idle 010: Busy 100: Finish
11:8	**DFE_WR _ST**	DFE_WR_ST	**DFE write engine state** 0001: Idle 0010: Busy 0100: Last 1000: Finish
0	**DFE_BU SY**	DFE_BUSY	**DFE busy**

14000800 **MMSYS_MBIST_CON** **MMSYS MBIST Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														MMSYS_MBIST_BACKGROUND		
Type														RW		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MMSYS_MBIST_RSTB				MMSYS_MBIST_SCAN OUT_SEL				MMSYS_MBIST_DEBUG		MMSYS_MBIST_FAILOUT_SEL					
Type	RW				RW				RW		RW					
Reset	0				0	0	0	0	0		0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
18:16	**MMSYS_ MBIST_ BACKGR**	MMSYS_MBIST_ BACKGROUND	MMSYS_MBIST_BACKGROUND

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Bit(s)	Mnemonic	Name	Description
	OUND		
15	**MMSYS_MBIST_RSTB**	MMSYS_MBIST_RSTB	MMSYS_MBIST_RSTB
11:8	**MMSYS_MBIST_SCANOUT_SEL**	MMSYS_MBIST_SCANOUT_SEL	MMSYS_MBIST_SCANOUT_SEL
7	**MMSYS_MBIST_DEBUG**	MMSYS_MBIST_DEBUG	MMSYS_MBIST_DEBUG
5:0	**MMSYS_MBIST_FAILOUT_SEL**	MMSYS_MBIST_FAILOUT_SEL	MMSYS_MBIST_FAILOUT_SEL

14000804 **MMSYS_MBIST_DONE** **MMSYS MBIST Done** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					MMSYS_MBIST_DONE											
Type					RU											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0	**MMSYS_MBIST_DONE**	MMSYS_MBIST_DONE	MMSYS MBIST done

14000808 **MMSYS_MBIST_HOLDB** **MMSYS MBIST holdb** **00000FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					MMSYS_MBIST_HOLDB											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
11:0	**MMSYS_MBIST_HOLDB**	MMSYS_MBIST_HOLDB	MMSYS MBIST holdb

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1400080C **MMSYS_MBIST_MODE** MMSYS MBIST Mode 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					MMSYS_MBIST_MODE											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0	**MMSYS_MBIST_MODE**	MMSYS_MBIST_MODE	MMSYS MBIST mode

14000810 **MMSYS_MBIST_FAIL0** MMSYS MBIST Fail 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMSYS_MBIST_FAIL0[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MMSYS_MBIST_FAIL0[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**MMSYS_MBIST_FAIL0**	MMSYS_MBIST_FAIL0	MMSYS MBIST fail 0

14000814 **MMSYS_MBIST_FAIL1** MMSYS MBIST Fail 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MMSYS_MBIST_FAIL1
Type																RU
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**MMSYS_MBIST_FAIL1**	MMSYS_MBIST_FAIL1	MMSYS MBIST fail 1

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14000820	MMSYS_MBIST_BSEL0	MMSYS MBIST BSEL 0	FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MDP_WROT_MBIST_BSEL								MDP_RDMA_MBIST_BSEL							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MDP_TDSHP_MBIST_BSEL															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24	**MDP_WROT_MBIST_BSEL**	MDP_WROT_MBIST_BSEL	MDP_WROT_MBIST_BSEL
23:16	**MDP_RDMA_MBIST_BSEL**	MDP_RDMA_MBIST_BSEL	MDP_RDMA_MBIST_BSEL
15:0	**MDP_TDSHP_MBIST_BSEL**	MDP_TDSHP_MBIST_BSEL	MDP_TDSHP_MBIST_BSEL

14000824	MMSYS_MBIST_BSEL1	MMSYS MBIST BSEL 1	FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DISP_UFOE_MBIST_BSEL							MDP_RSZ1_MBIST_BSEL[11:3]								
Type	RW							RW								
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MDP_RSZ1_MBIST_BSEL[2:0]			MDP_RSZ0_MBIST_BSEL												
Type	RW			RW												
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:25	**DISP_UFOE_MBIST_BSEL**	DISP_UFOE_MBIST_BSEL	DISP_UFOE_MBIST_BSEL
24:13	**MDP_RSZ1_MBIST_BSEL**	MDP_RSZ1_MBIST_BSEL	MDP_RSZ1_MBIST_BSEL
12:0	**MDP_RSZ0_MBIST_BSEL**	MDP_RSZ0_MBIST_BSEL	MDP_RSZ0_MBIST_BSEL

14000830	MMSYS_MEM_DELSEL0	MMSYS Memory Delay Select 0	16AA5555

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			MDP_RDMA_MEM_DELSEL													
Type			RW													
Reset			0	1	0	1	1	0	1	0	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MDP_RSZ_MEM_DELSEL															
Type	RW															
Reset	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
29:16	**MDP_RDMA_MEM_DELSEL**	MDP_RDMA_MEM_DELSEL	MDP_RDMA_MEM_DELSEL
15:0	**MDP_RSZ_MEM_DELSEL**	MDP_RSZ_MEM_DELSEL	MDP_RSZ_MEM_DELSEL

14000834 MMSYS_MEM_DELSEL1 MMSYS Memory Delay Select 1 A5AAAAAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MDP_TDSHP_MEM_DELSEL				MDP_WDMA_MEM_DELSEL						MDP_WROT_MEM_DELSEL[21:16]					
Type	RW				RW						RW					
Reset	1	0	1	0	0	1	0	1	1	0	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MDP_WROT_MEM_DELSEL[15:0]															
Type	RW															
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
31:28	**MDP_TDSHP_MEM_DELSEL**	MDP_TDSHP_MEM_DELSEL	MDP_TDSHP_MEM_DELSEL
27:22	**MDP_WDMA_MEM_DELSEL**	MDP_WDMA_MEM_DELSEL	MDP_WDMA_MEM_DELSEL
21:0	**MDP_WROT_MEM_DELSEL**	MDP_WROT_MEM_DELSEL	MDP_WROT_MEM_DELSEL

14000838 MMSYS_MEM_DELSEL2 MMSYS Memory Delay Select 2 2AAAAA5A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DISP_UFOE_MEM_DELSEL												DISP_GAMMA_MEM_DELSEL[3:2]	
Type			RW												RW	
Reset			1	0	1	0	1	0	1	0	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	DISP_GAMMA_MEM_DELSEL[1:0]		DISP_WDMA_MEM_DELSEL						DISP_RDMA_MEM_DELSEL				DISP_OVL_MEM_DELSEL			
Type	RW		RW						RW				RW			
Reset	1	0	1	0	1	0	1	0	0	1	0	1	1	0	1	0

Bit(s)	Mnemonic	Name	Description
29:18	DISP_UFOE_MEM_DELSEL	DISP_UFOE_MEM_DELSEL	DISP_UFOE_MEM_DELSEL
17:14	DISP_GAMMA_MEM_DELSEL	DISP_GAMMA_MEM_DELSEL	DISP_GAMMA_MEM_DELSEL
13:8	DISP_WDMA_MEM_DELSEL	DISP_WDMA_MEM_DELSEL	DISP_WDMA_MEM_DELSEL
7:4	DISP_RDMA_MEM_DELSEL	DISP_RDMA_MEM_DELSEL	DISP_RDMA_MEM_DELSEL
3:0	DISP_OVL_MEM_DELSEL	DISP_OVL_MEM_DELSEL	DISP_OVL_MEM_DELSEL

1400083C **MMSYS_MEM_DELSEL3** **MMSYS Memory Delay Select 3** **00000005**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DSI_MEM_DELSEL			
Type													RW			
Reset													0	1	0	1

Bit(s)	Mnemonic	Name	Description
3:0	DSI_MEM_DELSEL	DSI_MEM_DELSEL	DSI_MEM_DELSEL

14000880 **MMSYS_DEBUG_OUT_SEL** **MMSYS Debug Output Select** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												MMSYS_DEBUG_OUT_SEL				

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Type												RW				
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0	**MMSYS_DEBUG_OUT_SEL**	MMSYS_DEBUG_OUT_SEL	MMSYS_DEBUG_OUT_SEL

14000890 MMSYS_DUMMY0 MMSYS Dummy Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMSYS_DUMMY0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MMSYS_DUMMY0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**MMSYS_DUMMY0**	MMSYS_DUMMY0	MMSYS_DUMMY0

14000894 MMSYS_DUMMY1 MMSYS Dummy Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMSYS_DUMMY1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MMSYS_DUMMY1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**MMSYS_DUMMY1**	MMSYS_DUMMY1	MMSYS_DUMMY1

14000898 MMSYS_DUMMY2 MMSYS Dummy Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMSYS_DUMMY2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MMSYS_DUMMY2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31:0	**MMSYS_DUMMY2**	MMSYS_DUMMY2	MMSYS_DUMMY2

1400089C **MMSYS_DUMMY3** **MMSYS Dummy Register 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMSYS_DUMMY3[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MMSYS_DUMMY3[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**MMSYS_DUMMY3**	MMSYS_DUMMY3	MMSYS_DUMMY3

140008A0 **DISP_DL_VALID_0** **DISP Direct Link Valid Status 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DISP_DL_VALID_0[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DISP_DL_VALID_0[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DISP_DL_VALID_0**	DISP_DL_VALID_0	DISP direct link valid status 0

140008A4 **DISP_DL_READY_0** **DISP Direct Link READY Status 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DISP_DL_READY_0[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DISP_DL_READY_0[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31:0	**DISP_DL_READY_0**	DISP_DL_READY_0	DISP direct link ready status 0

1400008A8 **MDP_DL_VALID_0** **MDP Direct Link Valid Status 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MDP_DL_VALID_0[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MDP_DL_VALID_0[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**MDP_DL_VALID_0**	MDP_DL_VALID_0	MDP direct link valid status 0

1400008AC **MDP_DL_READY_0** **MDP Direct Link READY Status 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MDP_DL_READY_0[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MDP_DL_READY_0[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**MDP_DL_READY_0**	MDP_DL_READY_0	MDP direct link ready status 0

1400008D0 **SMI_LARB0_GREQ** **SMI LARB0 Request** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			SMI_LARB0_GREQ													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
13:0	**SMI_LARB0_GREQ**	SMI_LARB0_GREQ	SMI LARB0 request

6.1.1.5 Programming Guide

Before we introduce the programming model, two basic operation modes and one terminology "STREAM" must be explained first to make the programming model reasonable. The basic operation modes are:

1. Single mode:
   In this mode, one SW trigger only makes modules to process one frame. Usually, it is a memory-in-memory-output operation (e.g. memory -> RDMA0 -> PRZ0 -> WDMA0 -> memory), or an operation output to the display device with frame buffer (e.g. memory -> RDMA0-> color0-> gamma -> DSI0. SW must wait for one frame processing to be done before triggering the next frame.

2. Refresh mode:
   In this mode, pixels must be outputted to the display device without frame buffer (e.g. DSI video mode and DPI). After a data path is configured as refresh mode and starts, it will process frame-by-frame automatically until the data path stops. The process follows the refresh timing (vsync, hsync and data enable) of the display output interface.

In the refresh mode, the display output interface refresh timing is asynchronous to software, and we must guarantee each module receives complete settings for one frame when it starts to process this frame. For this reason, a mutex between software and hardware is used to achieve this.

A mutex is used to specify a STREAM and to guarantee a complete setting of this STREAM is seen by modules in this STREAM.

- A STREAM means a data stream from Source to Sink.
- Source can be any module with read memory capability, which is RDMA or OVL.
- Sink can be any module with capability of outputting to external display devices or to memory, which is DSI0, DPI or WDMA/WROT.

In multimedia subsys, there are at most 8 STREAMs concurrently. Therefore, we provide 10 mutexes. Every mutex's function and register interface are the same.

Mutex has the following attributes, which can be set in dispsys_mutex.

- Source of SOF (Start Of Frame)
  It means the Sink of this STREAM is which module. Due to the display timing of a STREAM, when to start a frame/when to end a frame, is decided by the Sink, and the display subsys must know it to route the SOF signal to all modules in this mutex.
- Which modules are in the STREAM.

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Because one mutex describes one STREAM, there is a constraint that one module can be set in only one mutex. In other words, one module cannot be set in more than one mutex.

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6.2 SMI_COMMON

6.2.1 Introduction

SMI (Smart Multimedia Interface) is a simple bus protocol for multimedia engines to access system memories, including off-chip and on-chip memories. As in the block diagram, multimedia engines access EMI and MM memory through the SMI bus. The MM memory is part of SMI controller and designed to have short accessing latency and high bandwidth for multimedia engines. From the perspective of SMI, the multimedia engines are masters of the bus, and SMI itself is the slave of the bus. Furthermore, the MM memory is regarded as internal memory and EMI which is a type of external memory.

In this document, we will focus on SMI_COMMON.

6.2.2 Features

- Auto clock gating for power reduction
- Arbitration among request from local arbiters to EMI
- Bandwidth/outstanding limiter
- Performance monitor
- Command throttling for reducing latency

6.2.3 Block Diagram

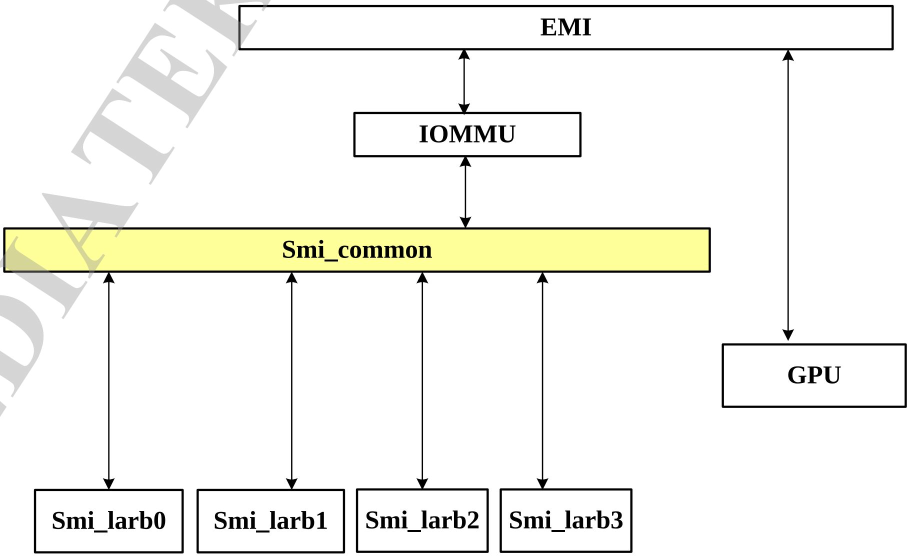

Figure 6-3. SMI_COMMON and neighbor blocks

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6.2.4 Register Definition

Module name: SMI_COMMON_EXT Base address: (+14016000h)

Address	Name	Width	Register Function
14016100	SMI_L1LEN	32	**SMI Level 1 ARB Setting** Sets up Level 1 bandwidth filter length.
14016104	SMI_L1ARB0	32	**SMI Level 1 BW Filter Control M0** Controls master 0 bandwidth filter.
14016108	SMI_L1ARB1	32	**SMI Level 1 BW Filter Control M1** Controls master 1 bandwidth filter.
1401610C	SMI_L1ARB2	32	**SMI Level 1 BW Filter Control M2** Controls master 2 bandwidth filter.
14016110	SMI_L1ARB3	32	**SMI Level 1 BW Filter Control M2** Controls master 2 bandwidth filter.
140161A0	SMI_MON_AXI_ENA	32	**SMI AXI Performance Monitor Enable** Enables AXI performance monitor.
140161A4	SMI_MON_AXI_CLR	32	**SMI AXI Performance Monitor Clear** Clears AXI performance monitor.
140161AC	SMI_MON_AXI_TYPE	32	**SMI AXI Monitor Type Selection Register** Selects performance monitor type.
140161B0	SMI_MON_AXI_CON	32	**SMI AXI Performance Monitor Control Register** Controls performance monitor.
140161C0	SMI_MON_AXI_ACT_CNT	32	**SMI AXI Monitor Active Counter Register** Counts active cycles for monitor.
140161C4	SMI_MON_AXI_REQ_CNT	32	**SMI AXI Monitor Request Counter Register** Counts request cycles for monitor.
140161C8	SMI_MON_AXI_OSTD_CNT	32	**SMI AXI Monitor OSTD Counter Register** Counts idle cycles for monitor.
140161CC	SMI_MON_AXI_BEA_CNT	32	**SMI AXI Monitor Beat Counter Register** Counts beats for monitor.
140161D0	SMI_MON_AXI_BYT_CNT	32	**SMI AXI Monitor Byte Counter Register** Counts bytes for monitor.
140161D4	SMI_MON_AXI_CP_CNT	32	**SMI AXI Monitor Command Phase Counter Register** Counts command phase cycles for monitor.
140161D8	SMI_MON_AXI_DP_CNT	32	**SMI AXI Monitor Data Phase Counter Register** Counts data phase cycles for monitor.
140161DC	SMI_MON_AXI_CP_MAX	32	**SMI AXI Monitor Command Phase Maximum Register** Counts command/data phase maximum cycles for monitor.
140161E0	SMI_MON_AXI_COS_MAX	32	**SMI AXI Monitor Outstanding Transaction Maximum Register** Counts outstanding transaction's maximum cycles for monitor.
14016228	SMI_WRR_REG0	32	**SMI WRR Credit CTRL0** WRR credit control 0
14016230	SMI_READ_FIFO_TH	32	**ARB Mode** Controls command throttling
14016234	SMI_M4U_TH	32	**CH OUTS Limiter EN**
1401623C	SMI_PREULTRA_MASK0	32	**SMI Preultra Mask Setting 0** Sets up preultra mask.
14016240	SMI_PREULTRA_MASK1	32	**SMI Preultra Mask Setting 1** Sets up preultra mask.
14016300	SMI_DCM	32	**SMI DCM Control** Controls SMI DCM.

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Address	Name	Width	Register Function
14016304	**SMI_ELA**	32	**SMI ELA Control**
14016400	**SMI_DEBUG_S0**	32	**SMI Debug Register 0** Debug register
14016404	**SMI_DEBUG_S1**	32	**SMI Debug Register 1** Debug register
14016408	**SMI_DEBUG_S2**	32	**SMI Debug Register 2** Debug register
1401640C	**SMI_DEBUG_S3**	32	**SMI Debug Register 3** Debug register
14016430	**SMI_DEBUG_M0**	32	**SMI Debug Register** Debug register
14016440	**SMI_DEBUG_MISC**	32	**SMI Debug Register** Debug register
14016444	**SMI_DUMMY**	32	Reserved
14016500	**SMI_HIST_REC0**	32	SMI History Recorder Config
14016504	**SMI_HIST_REC_DATA0**	32	SMI History Recorder Data 0
14016508	**SMI_HIST_REC_DATA1**	32	SMI History Recorder Data 1
1401650C	**SMI_HIST_REC_DATA2**	32	SMI History Recorder Data 2
14016510	**SMI_HIST_REC_DATA3**	32	SMI History Recorder Data 3
14016514	**SMI_HIST_REC_DATA4**	32	SMI History Recorder Data 4
14016518	**SMI_HIST_REC_DATA5**	32	SMI History Recorder Data 5
1401651C	**SMI_HIST_REC_DATA6**	32	SMI History Recorder Data 6
14016520	**SMI_HIST_REC_DATA7**	32	SMI History Recorder Data 7
14016524	**SMI_HIST_REC_DATA8**	32	SMI History Recorder Data 8
14016528	**SMI_HIST_REC_DATA9**	32	SMI History Recorder Data 9

14016100 SMI_L1LEN SMI Level 1 ARB Setting 00000003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name													AXUSER_G3D	FLOW_CTRL		BW_OVSHT_CTRL
Type													RW	RW		RW
Reset													0	0	1	1

Bit(s)	Mnemonic	Name	Description
3	**AXUSER_G3D**	FLOW_CTRL	**New outstanding control mechanism (command throttling between SMI/M4U)**

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Bit(s)	Mnemonic	Name	Description
			0: Disable 1: Enable
2:1	**FLOW_CTRL**	BW_OVSHT_CTRL	**Overshoot control of bandwidth limiter** 2'd0: Threshold /2 2'd1: Threshold /4 2'd2: Threshold /8 2'd3: No overshoot
0	**BW_OVSHT_CTRL**	M4U_ARB_WDATA	**Uses WARB channel or not** 0: Disable WARB channel and use arbiter in SMI for wdata (old mode) 1: Enable WARB channel (new mode)

14016104 SMI_L1ARB0 SMI Level 1 BW Filter Control M0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						**OUTS_LIMIT_EN**	**OUTS_LIMIT_WSOFT_EN**	**OUTS_LIMIT_EN**	**OUTS_WR_LIMIT_TH**					**OUTS_RD_LIMIT_TH[4:2]**		
Type						RW	RW	RW	RW					RW		
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**OUTS_RD_LIMIT_TH[1:0]**		**BW_HFILTER_EN**	**BW_FILTER_EN**	**MAX_GNT_CNT**											
Type	RW		RW	RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26	**OUTS_LIMIT_EN**	OUTS_LIMIT_RSOFT_EN	**Enables outstanding limiter read ultra soft mode** 0: Disable (ultra cannot pass outstanding limiter) 1: Enable (ultra can pass outstanding limiter)
25		OUTS_LIMIT_WSOFT_EN	**Enables outstanding limiter write ultra soft mode** 0: Disable (ultra cannot pass outstanding limiter) 1: Enable (ultra can pass outstanding limiter)
24		OUTS_LIMIT_EN	**Enables outstanding limiter** 0: Disable 1: Enable
23:19	**OUTS_WR_LIMIT_TH**	OUTS_WR_LIMIT_TH	**Outstanding write limiter threshold**
18:14	**OUTS_RD_LIMIT_TH**	OUTS_RD_LIMIT_TH	**Outstanding read limiter threshold**
13	**BW_HFILTER_EN**	BW_HFILTER_EN	**Enables Level 1 hard limiter (BW limiter & outstanding limiter)** 0: Soft limit 1: Hard limit
12	**BW_FILTER_EN**	BW_FILTER_EN	**Enables Level 1 bandwidth filter** 0: Disable bandwidth filter 1: Enable bandwidth filter
11:0	**MAX_GNT_CNT**	MAX_GNT_CNT	**Level 1 bandwidth filter maximum grant counts** The bandwidth threshold will be x/4096, x=SMI_L1ARBx[11:0].

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14016108 SMI_L1ARB1 SMI Level 1 BW Filter Control M1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						OUTS_LIMIT_EN	OUTS_LIMIT_WSOFT_EN	OUTS_LIMIT_EN	OUTS_WR_LIMIT_TH					OUTS_RD_LIMIT_TH[4:2]		
Type						RW	RW	RW	RW					RW		
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OUTS_RD_LIMIT_TH[1:0]		BW_HFILTER_EN	BW_FILTER_EN	MAX_GNT_CNT											
Type	RW		RW	RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26	OUTS_LIMIT_EN	OUTS_LIMIT_RSOFT_EN	**Enables outstanding limiter read ultra soft mode** 0: Disable (ultra cannot pass outstanding limiter) 1: Enable (ultra can pass outstanding limiter)
25		OUTS_LIMIT_WSOFT_EN	**Enables outstanding limiter write ultra soft mode** 0: Disable (ultra cannot pass outstanding limiter) 1: Enable (ultra can pass outstanding limiter)
24		OUTS_LIMIT_EN	**Enables outstanding limiter** 0: Disable 1: Enable
23:19	OUTS_WR_LIMIT_TH	OUTS_WR_LIMIT_TH	**Outstanding write limiter threshold**
18:14	OUTS_RD_LIMIT_TH	OUTS_RD_LIMIT_TH	**Outstanding read limiter threshold**
13	BW_HFILTER_EN	BW_HFILTER_EN	**Enables Level 1 hard limiter (BW limiter & outstanding limiter)** 0: Soft limit 1: Hard limit
12	BW_FILTER_EN	BW_FILTER_EN	**Enables Level 1 bandwidth filter** 0: Disable bandwidth filter 1: Enable bandwidth filter
11:0	MAX_GNT_CNT	MAX_GNT_CNT	**Level 1 bandwidth filter maximum grant counts** The bandwidth threshold will be x/4096, x=SMI_L1ARBx[11:0].

1401610C SMI_L1ARB2 SMI Level 1 BW Filter Control M2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						OUTS_LIMIT_EN	OUTS_LIMIT_WSOFT_EN	OUTS_LIMIT_EN	OUTS_WR_LIMIT_TH					OUTS_RD_LIMIT_TH[4:2]		
Type						RW	RW	RW	RW					RW		
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	OUTS_RD_LIMIT_TH[1:0]		BW_HFILTER_EN	BW_FILTER_EN	MAX_GNT_CNT											
Type	RW		RW	RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26	OUTS_LIMIT_EN	OUTS_LIMIT_RSOFT_EN	**Enables outstanding limiter read ultra soft mode** 0: Disable (ultra cannot pass outstanding limiter) 1: Enable (ultra can pass outstanding limiter)
25		OUTS_LIMIT_WSOFT_EN	**Enables outstanding limiter write ultra soft mode** 0: Disable(ultra cannot pass outstanding limiter) 1: Enable (ultra can pass outstanding limiter)
24		OUTS_LIMIT_EN	**Enables outstanding limiter** 0: Disable 1: Enable
23:19	OUTS_WR_LIMIT_TH	OUTS_WR_LIMIT_TH	**Outstanding write limiter threshold**
18:14	OUTS_RD_LIMIT_TH	OUTS_RD_LIMIT_TH	**Outstanding read limiter threshold**
13	BW_HFILTER_EN	BW_HFILTER_EN	**Enables Level 1 hard limiter (BW limiter & outstanding limiter)** 0: Soft limit 1: Hard limit
12	BW_FILTER_EN	BW_FILTER_EN	**Enables Level 1 bandwidth filter** 0: Disable bandwidth filter 1: Enable bandwidth filter
11:0	MAX_GNT_CNT	MAX_GNT_CNT	**Level 1 bandwidth filter maximum grant counts** The bandwidth threshold will be x/4096, x=SMI_L1ARBx[11:0].

14016110 SMI_L1ARB3 SMI Level 1 BW Filter Control M2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						OUTS_LIMIT_EN	OUTS_LIMIT_WSOFT_EN	OUTS_LIMIT_EN	OUTS_WR_LIMIT_TH					OUTS_RD_LIMIT_TH[4:2]		
Type						RW	RW	RW	RW					RW		
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OUTS_RD_LIMIT_TH[1:0]		BW_HFILTER_EN	BW_FILTER_EN	MAX_GNT_CNT											
Type	RW		RW	RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26	OUTS_LIMIT_EN	OUTS_LIMIT_RSOFT_EN	**Enables outstanding limiter read ultra soft mode** 0: Disable (ultra cannot pass outstanding limiter) 1: Enable (ultra can pass outstanding limiter)
25		OUTS_LIMIT_WS	**Enables outstanding limiter write ultra soft mode**

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Bit(s)	Mnemonic	Name	Description
		OFT_EN	0: Disable(ultra cannot pass outstanding limiter) 1: Enable (ultra can pass outstanding limiter)
24		OUTS_LIMIT_EN	**Enables outstanding limiter** 0: Disable 1: Enable
23:19	**OUTS_WR_LIMIT_TH**	OUTS_WR_LIMIT_TH	**Outstanding write limiter threshold**
18:14	**OUTS_RD_LIMIT_TH**	OUTS_RD_LIMIT_TH	**outstanding read limiter threshold**
13	**BW_HFILTER_EN**	BW_HFILTER_EN	**Enables Level 1 hard limiter (BW limiter & outstanding limiter)** 0: Soft limit 1: Hard limit
12	**BW_FILTER_EN**	BW_FILTER_EN	**Enables Level 1 bandwidth filter** 0: Disable bandwidth filter 1: Enable bandwidth filter
11:0	**MAX_GNT_CNT**	MAX_GNT_CNT	**Level 1 bandwidth filter maximum grant counts** The bandwidth threshold will be x/4096, x=SMI_L1ARBx[11:0].

140161A0 **SMI_MON_AXI_ENA** **SMI AXI Performance Monitor Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															MONAXIENA	MONAXIENA
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	**MONAXIENA**	MON_PARA	**Selects performance monitor mode** 0: Normal mode 1: Enable parallel mode for byte count
0		MONAXIENA	**Selects performance monitor bus** 0: Stop counting 1: Start to count *Note: When set to monitoring the AXI master bus (MON_BUS=1), the MON_TYPE must be set to monitoring only read or only write. Monitoring both read and write at same time is not supported for monitoring AXI bus.*

140161A4 **SMI_MON_AXI_CLR** **SMI AXI Performance Monitor Clear** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

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Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MON AXIC LR
Type																Other
Reset																0

Bit(s)	Mnemonic	Name	Description
0	MONAXICLR	MONAXICLR	**Clears performance monitor** 1: Clear

140161AC **SMI_MON_AXI_TYPE** **SMI AXI Monitor Type Selection Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MON TSEL [9:9]
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MONTSEL[8:0]									MON_COMPARE_ID_EN	MON_TYPE_REQ_SEL		MON_TYPE_RW_SEL_PARA_2	MON_TYPE_RW_SEL_PARA_1	MON_TYPE_RW_SEL_PARA_0	MON_TYPE_RW_SEL
Type	RW									RW	RW		RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16:7	MONTSEL	MON_COMPARE_ID	**AXI ID of performance monitor**
6		MON_COMPARE_ID_EN	**Enables performance monitor ID comparison** 0: Disable 1:enable
5:4		MON_TYPE_REQ_SEL	**Selects performance request type** 2'd0: All 2'd1: Ultra 2'd2: Preultra 2'd3: Normal
3		MON_TYPE_RW_SEL_PARA_2	**Selects performance monitor type #2** Only used in parallel byte count mode. 0: Read 1: Write
2		MON_TYPE_RW_SEL_PARA_1	**Selects performance monitor type #1** Only used in parallel byte count mode. 0: Read 1: Write
1		MON_TYPE_RW_SEL_PARA_0	**Selects performance monitor type #0** Only used in parallel byte count mode. 0: Read 1: Write
0		MON_TYPE_RW_SEL	**Selects performance monitor type** 0: Read

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Bit(s)	Mnemonic	Name	Description
			1: Write

140161B0 **SMI_MON_AXI_CON** **SMI AXI Performance Monitor Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													AXIBUSSEL			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AXI_BUS_SELECT_PARA_1				AXI_BUS_SELECT_PARA_0				AXI_BUS_SELECT							DPSEL
Type	RW				RW				RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0				0

Bit(s)	Mnemonic	Name	Description
19:16	**AXIBUSSEL**	AXI_BUS_SELECT_PARA_2	**Selects AXI port to be monitored, #2** Only used in parallel byte count mod. 4'd0: AXI master port 1 of SMI 4'd1: AXI master port 2 of SMI 4'd2: AXI bus from LARB0 4'd3: AXI bus from LARB1 4'd4: AXI bus from LARB2 4'd5: AXI bus from LARB3 4'd6: AXI bus from LARB4 4'd7: AXI bus from LARB5 Others: Reserved
15:12		AXI_BUS_SELECT_PARA_1	**Selects AXI port to be monitored, #1** Only used in parallel byte count mode. 4'd0: AXI master port 1 of SMI 4'd1: AXI master port 2 of SMI 4'd2: AXI bus from LARB0 4'd3: AXI bus from LARB1 4'd4: AXI bus from LARB2 4'd5: AXI bus from LARB3 4'd6: AXI bus from LARB4 4'd7: AXI bus from LARB5 Others: Reserved
11:8		AXI_BUS_SELECT_PARA_0	**Selects AXI port to be monitored, #0** Only used in parallel byte count mode. 4'd0: AXI master port 1 of SMI 4'd1: AXI master port 2 of SMI 4'd2: AXI bus from LARB0 4'd3: AXI bus from LARB1 4'd4: AXI bus from LARB2 4'd5: AXI bus from LARB3 4'd6: AXI bus from LARB4 4'd7: AXI bus from LARB5 Others: Reserved
7:4		AXI_BUS_SELECT	**Select AXI port to be monitored** 4'd0: AXI master port 1 of SMI 4'd1: AXI master port 2 of SMI 4'd2: AXI bus from LARB0 4'd3: AXI bus from LARB1 4'd4: AXI bus from LARB2 4'd5: AXI bus from LARB3 4'd6: AXI bus from LARB4

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Bit(s)	Mnemonic	Name	Description
			4'd7: AXI bus from LARB5 Others: Reserved
0	**DPSEL**	DP_SEL	**Selects data phase** 0: Type 0. The data phase increases one when any outstanding transaction waits for data transfer. 1: Type 1. The data phase increases N when N outstanding transactions are waiting for data transfer.

140161C0 **SMI_MON_AXI_ACT_CNT** **SMI AXI Monitor Active Counter Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ACTCNT[23:16]							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACTCNT[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0	**ACTCNT**	ACT_CNT	**Monitor active counter** ACT_CNT counts how many cycles when MONAXIENA = 1. It stops when the upper bound, 0xffffffff, is reached and is cleared when MONAXICLR = 1.

140161C4 **SMI_MON_AXI_REQ_CNT** **SMI AXI Monitor Request Counter Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									REQCNT[23:16]							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REQCNT[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0	**REQCNT**	REQ_CNT	**Monitor request counter** REQ_CNT counts how many transactions when MONAXIENA = 1. It stops when upper bound, 0xffffffff, is reached and is cleared when MONAXICLR = 1.

140161C8 **SMI_MON_AXI_OSTD_CNT** **SMI AXI Monitor OSTD Counter Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name											**IDLCNT**					
Type											RU					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0	**IDLCNT**	IDL_CNT	**Monitor outstanding number** Counts the number of the outstanding . *Note:* *1. This index is unavailable when MON_TYPE_REQ_SEL is not "all".* *2. This index is unavailable in MET tool. (monitor enable cannot be 0 during monitoring.)* *3. The definition of this outstanding number of write is from command grant to wlast instead of write response.*

140161CC **SMI_MON_AXI_BEA_CNT** SMI AXI Monitor Beat Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									**BEACNT[23:16]**							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BEACNT[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0	**BEACNT**	BEA_CNT	**Performance monitor beat counter** BEA_CNT counts the total number of data beats when MONAXIENA = 1. It stops when 0xffffffff is reached and is cleared when MONAXICLR = 1.

140161D0 **SMI_MON_AXI_BYT_CNT** SMI AXI Monitor Byte Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**BYTCNT[27:16]**											
Type					RU											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BYTCNT[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:0	**BYTCNT**	BYT_CNT	**Performance monitor byte counter** BYT_CNT counts the total number of data bytes transferred when MONAXIENA = 1. It stops when 0xffffffff is reached and is cleared when MONAXICLR = 1.

140161D4 **SMI_MON_AX** SMI AXI Monitor Command Phase Counter 00000000

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I_CP_CNT Register

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									**CPCNT[23:16]**							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CPCNT[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0	**CPCNT**	CP_CNT	**Monitor command phase cycle counter** CP_CNT accumulate the cycles from greq=1 to the assertion of glcomd when MONAXIENA = 1. It stops counting when 0xffffffff is reached and is cleared when MONAXICLR = 1.

140161D8 SMI_MON_AXI_DP_CNT SMI AXI Monitor Data Phase Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DPCNT[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DPCNT[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DPCNT**	DP_CNT	**Monitor data phase cycle counter** DP_CNT accumulates the cycles from the start of the data phase to its end when MONAXIENA = 1. It stops counting when 32'hffffffff is reached and is cleared when MONAXICLR = 1. *Note: DP_CNT does not support profiling both read and write at the same time, i.e. mon_type[3:2] cannot be 2'b00.*

140161DC SMI_MON_AXI_CP_MAX SMI AXI Monitor Command Phase Maximum Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													**CDPMAX[19:16]**			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CDPMAX[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:0	**CDPMAX**	CP_MAX	**Maximum monitor command phase** CP_MAX will record the maximum latency of command phase among all transactions when MONAXIENA = 1. Cleared when MONAXICLR = 1.

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140161E0 **SMI_MON_AXI_COS_MAX** **SMI AXI Monitor Outstanding Transaction Maximum Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											COSMAX					
Type											RU					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0	COSMAX	COS_MAX	**Monitors maximum command outstanding number** COS_MAX records the maximum number of outstanding transactions when MONAXIENA = 1. Cleared when MONAXICLR = 1.

14016228 **SMI_WRR_REG0** **SMI WRR Credit CTRL0** **00041041**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									SMI_WRR_REG0_4						SMI_WRR_REG0_2[5:4]	
Type									RW						RW	
Reset									0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SMI_WRR_REG0_2[3:0]				SMI_WRR_REG0_1						SMI_WRR_REG0_3					
Type	RW				RW						RW					
Reset	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
23:18	SMI_WRR_REG0_4	SMI_WRR_REG0_3	**Credit control for LARB3** The minimum value of this field should be 1.
17:12		SMI_WRR_REG0_2	**Credit control for LARB2** The minimum value of this field should be 1.
11:6		SMI_WRR_REG0_1	**Credit control for LARB1** The minimum value of this field should be 1.
5:0	SMI_WRR_REG0_3	SMI_WRR_REG0_0	**Credit control for LARB0 port** The minimum value of this field should be 1.

14016230 **SMI_READ_FIFO_TH** **ARB Mode** **00000C80**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOTA	SLIC	TOTAL_NONULTRA_CMD_N					TOTAL_CMD_NUM					SLICE_TH			

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	L_C MD_ NUM	E_TH	UM_WR													
Type	RW	RW	RW					RW					RW			
Reset	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**TOTAL_CMD_NUM**	ARB_ORI	**Arbitration behavior** 0: New arbitration behavior (2T WRR/state jump sequence) 1: Arbitration behavior as previous project
14	**SLICE_TH**	STD_AXI_MODE	**Controls the operation mode of read AXI slice** 0: Does not let ultra command be blocked by any normal command 1: There is ultra feature but might be blocked by one normal command ahead
13:9	**TOTAL_NONULTRA_CMD_NUM_WR**	TOTAL_NONULTRA_CMD_NUM	**Controls total number of non-ultra command between smi_common and M4U**
8:4		TOTAL_CMD_NUM	**Controls total number of command between smi_common and M4U**
3:0		SLICE_TH	**Controls how many commands can be in write AXI slice** [0]: LARB0 [1]: LARB1 [2]: LARB2 [3]:LARB3 0: 2 commands 1: 1 command

14016234 SMI_M4U_TH CH OUTS Limiter EN F7E29CA7

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CH_OUTS_LIMITER_EN	NON_ULTRA_OUTS_LIMITER_OF_EACH_AXI_CH					TOTAL_CMD_NUM_WR					TOTAL_NONULTRA_CMD_NUM_RD	TOTAL_CMD_NUM_RD [4:1]			
Type	RW	RW					RW					RW	RW			
Reset	1	1	1	1	0	1	1	1	1	1	1	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOTAL_CMD_NUM_RD[0:0]	TOTAL_CMD_NUM_WR					TOTAL_NONULTRA_CMD_NUM_RD					TOTAL_CMD_NUM_RD				
Type	RW	RW					RW					RW				
Reset	1	0	0	1	1	1	0	0	1	0	1	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
31		CH_OUTS_LIMITER_EN	Enables channel outstanding limiter
30:26		NON_ULTRA_OUTS_LIMITER_OF_EACH_AXI_CH	Non-ultra outstanding limiter threshold for each AXI channel
25:21	**TOTAL_CMD_NUM_**	OUTS_LIMITER_OF_EACH_AXI_C	Outstanding limiter threshold for each AXI channel

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Bit(s)	Mnemonic	Name	Description
	WR	H	
20	**TOTAL_NONULTRA_CMD_NUM_RD**	RD_FLUSH_ENTER_CMD_THROT_EN	Enables RD flush command bypass non-ultra threshold of command throttling
19:15	**TOTAL_CMD_NUM_RD**	TOTAL_NONULTRA_CMD_NUM_WR	Controls total write number of non-ultra command between smi_common and M4U
14:10		TOTAL_CMD_NUM_WR	Controls total write number of command between smi_common and M4U
9:5		TOTAL_NONULTRA_CMD_NUM_RD	Controls total read number of non-ultra command between smi_common and M4U
4:0		TOTAL_CMD_NUM_RD	Controls total read number of command between smi_common and M4U

1401623C **SMI_PREULTRA_MASK0** **SMI Preultra Mask Setting 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name		**EMI_2CH**	**MASK_FIX_WINDOW**	**SMI_DCM**												**MASK_EN**
Type		RW	RW	RW												RW
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
14		EMI_2CH	**Selects DRAM device type** 0: Single channel DRAM 1: Wwo channel DRAM
13		MASK_FIX_WINDOW	**Selects preultra mask mode** 0: The counter is added only when EMI is busy. 1: The counter is added in each cycle.
12:1	**SMI_DCM**	MASK_COUNT_TH	**Period setting of mask** Cycles for changing to the next group ID for mask. The minimum setting should be 1.
0		MASK_EN	**Enables preultra mask** 0: Disable 1: Enable

14016240 **SMI_PREULTRA_MASK1** **SMI Preultra Mask Setting 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ID_SEQ[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ID_SEQ[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		ID_SEQ	**Group ID of mask sequence** [1:0] Masked group ID in time0 [3:2] Masked group ID in time1 etc.

14016300 SMI_DCM SMI DCM Control 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SMI_DCM
Type																RW
Reset																1

Bit(s)	Mnemonic	Name	Description
0		SMI_DCM	**Controls SMI DCM** 0: Off 1: On

14016304 SMI_ELA SMI ELA Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						SMI_DEBUG0	SMI_DEBUG1	SMI_DEBUG1								
Type						RU	RU	RW								
Reset						0	0	0								

Bit(s)	Mnemonic	Name	Description
10	SMI_DEBUG0	SMI_COMMON_SLP_PROT_ACT	**Status of reset glitch protection of SMI_COMMON** 0: Not active (idle) 1: Active
9	SMI_DEBUG1	SMI_COMMON_SLP_PROT_RDY	**Status of reset glitch protection ready of SMI_COMMON** 0: Not ready 1: Ready
8	SMI_DEBUG1	SMI_COMMON_SLP_PROT_EN	**Enables reset glitch protection enable of SMI_COMMON** 0: Disable 1: Enable

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14016400 SMI_DEBUG_S0 SMI Debug Register 0 000002C5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										SMI_DEBUG1[22:16]						
Type										RU						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SMI_DEBUG1[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	1	0	1	1	0	0	0	1	0	1

Bit(s)	Mnemonic	Name	Description
22:0	SMI_DEBUG1	SMI_DEBUG_S0	SMI debug register 0 (AXI interface signals)

14016404 SMI_DEBUG_S1 SMI Debug Register 1 000002C5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										SMI_DEBUG1[22:16]						
Type										RU						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SMI_DEBUG1[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	1	0	1	1	0	0	0	1	0	1

Bit(s)	Mnemonic	Name	Description
22:0	SMI_DEBUG1	SMI_DEBUG_S1	SMI debug register 1 (AXI interface signals & DCM status)

14016408 SMI_DEBUG_S2 SMI Debug Register 2 000002C5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										SMI_DUMMY[22:16]						
Type										RU						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SMI_DUMMY[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	1	0	1	1	0	0	0	1	0	1

Bit(s)	Mnemonic	Name	Description
22:0	SMI_DUMMY	SMI_DEBUG_S2	SMI debug register 2 (AXI interface signals & DCM status)

1401640C SMI_DEBUG_S3 SMI Debug Register 3 000002C5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										SMI_DUMMY[22:16]						

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Type										RU						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SMI_DUMMY[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	1	0	1	1	0	0	0	1	0	1

Bit(s)	Mnemonic	Name	Description
22:0	**SMI_DUMMY**	SMI_DEBUG_S3	SMI debug register 3 (AXI interface signals & DCM status)

14016430 SMI_DEBUG_M0 SMI Debug Register 00000555

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											**SMI_DEBUG_M0[21:16]**					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SMI_DEBUG_M0[15:0]**															
Type	RU															
Reset	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
21:0		SMI_DEBUG_M0	SMI debug register (AXI interface signals & DCM status)

14016440 SMI_DEBUG_MISC SMI Debug Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**SMI_DEBUG4**
Type																RU
Reset																1

Bit(s)	Mnemonic	Name	Description
0		SMI_DEBUG4	SMI debug register (AXI interface signals & DCM status)

14016444 SMI_DUMMY 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SMI_DUMMY[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SMI_DUMMY[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31:0		SMI_DUMMY	Reserved

14016500 SMI_HIST_REC0 SMI History Recorder Config 000017FE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SMI_REC_BUSY	SMI_REC_WPTR				SMI_HIST_VLD[9:1]								
Type			RU	RU				RU								
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SMI_HIST_VLD[0:0]	SMI_HIST_STOP_DLY			SMI_SW_STOP_MODE	SMI_HIST_CYCLE_MAX										SMI_HIST_EN
Type	RU	RW			RW	RW										RW
Reset	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	0

Bit(s)	Mnemonic	Name	Description
29		SMI_REC_BUSY	**State of history recorder** 0: Idle 1: Busy
28:25		SMI_REC_WPTR	**Pointer state of history recorder**
24:15		SMI_HIST_VLD	**Valid state of history recorder**
14:12		SMI_HIST_STOP_DLY	**Number of delay samples after stop**
11		SMI_SW_STOP_MODE	**Selects stop mode of history recorder** 0: HW trigger stop 1: SW trigger stop
10:1		SMI_HIST_CYCLE_MAX	**Cycles between samples of history recorder**
0		SMI_HIST_EN	**Enables history recorder** 0: Disable 1: Enable

14016504 SMI_HIST_REC_DATA0 SMI History Recorder Data 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SMI_HIST_DATA0[19:16]			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SMI_HIST_DATA0[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:0		SMI_HIST_DATA0	**Recording data of history recorder** [19:13]: Number of finished commands

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Bit(s)	Mnemonic	Name	Description
			[12:6]: Number of granted commands [5:3]: Block cycles of command throttling [2:0]: Block cycles of outstanding limiter

14016508 **SMI_HIST_REC_DATA1** **SMI History Recorder Data 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SMI_HIST_DATA1[19:16]			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SMI_HIST_DATA1[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:0		SMI_HIST_DATA1	**Recording data of history recorder** [19:13]: Number of finished commands [12:6]: Number of granted commands [5:3]: Block cycles of command throttling [2:0]: Block cycles of outstanding limiter

1401650C **SMI_HIST_REC_DATA2** **SMI History Recorder Data 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SMI_HIST_DATA2[19:16]			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SMI_HIST_DATA2[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:0		SMI_HIST_DATA2	**Recording data of history recorder** [19:13]: Number of finished commands [12:6]: Number of granted commands [5:3]: Block cycles of command throttling [2:0]: Block cycles of outstanding limiter

14016510 **SMI_HIST_REC_DATA3** **SMI History Recorder Data 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SMI_HIST_DATA3[19:16]			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	**SMI_HIST_DATA3[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:0		SMI_HIST_DATA3	**Recording data of history recorder** [19:13]: Number of finished commands [12:6]: Number of granted commands [5:3]: Block cycles of command throttling [2:0]: Block cycles of outstanding limiter

14016514 SMI_HIST_REC_DATA4 SMI History Recorder Data 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													**SMI_HIST_DATA4[19:16]**			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SMI_HIST_DATA4[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:0		SMI_HIST_DATA4	**Recording data of history recorder** [19:13]: Number of finished commands [12:6]: Number of granted commands [5:3]: Block cycles of command throttling [2:0]: Block cycles of outstanding limiter

14016518 SMI_HIST_REC_DATA5 SMI History Recorder Data 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													**SMI_HIST_DATA5[19:16]**			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SMI_HIST_DATA5[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:0		SMI_HIST_DATA5	**Recording data of history recorder** [19:13]: Number of finished commands [12:6]: Number of granted commands [5:3]: Block cycles of command throttling [2:0]: Block cycles of outstanding limiter

1401651C SMI_HIST_RE SMI History Recorder Data 6 00000000

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C_DATA6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SMI_HIST_DATA6[19:16]			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SMI_HIST_DATA6[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:0		SMI_HIST_DATA6	**Recording data of history recorder** [19:13]: Number of finished commands [12:6]: Number of granted commands [5:3]: Block cycles of command throttling [2:0]: Block cycles of outstanding limiter

14016520 SMI_HIST_REC_DATA7 SMI History Recorder Data 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SMI_HIST_DATA7[19:16]			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SMI_HIST_DATA7[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:0		SMI_HIST_DATA7	**Recording data of history recorder** [19:13]: Number of finished commands [12:6]: Number of granted commands [5:3]: Block cycles of command throttling [2:0]: Block cycles of outstanding limiter

14016524 SMI_HIST_REC_DATA8 SMI History Recorder Data 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SMI_HIST_DATA8[19:16]			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SMI_HIST_DATA8[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:0		SMI_HIST_DATA8	**Recording data of history recorder** [19:13]: Number of finished commands [12:6]: Number of granted commands

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Bit(s)	Mnemonic	Name	Description
			[5:3]: Block cycles of command throttling [2:0]: Block cycles of outstanding limiter

14016528 **SMI_HIST_REC_DATA9** **SMI History Recorder Data 9** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													**SMI_HIST_DATA9[19:16]**			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SMI_HIST_DATA9[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:0		SMI_HIST_DATA9	**Recording data of history recorder** [19:13]: Number of finished commands [12:6]: Number of granted commands [5:3]: Block cycles of command throttling [2:0]: Block cycles of outstanding limiter

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6.3 SMI_LARB

6.3.1 Introduction

The SMI (Smart Multimedia Interface) is a MediaTek proprietary interface used in multimedia systems. The SMI bus fabric deals with the complex bus interconnection and memory access transaction in a high-performance multimedia-rich system. The SMI bus fabric is separated into 2 parts for hierarchical arbitration. The SMI local arbiter is used for the first level arbitration for part of multimedia engines. The granted masters from SMI local arbiters are arbitrated at the second level arbiter at SMI common arbiter with other masters in other multimedia sub-systems.

6.3.2 Features

- 1st level arbitration of multimedia engines
- GMC/SMI protocol to AXI protocol conversion
- Supports bandwidth regulation for each master
- Performance monitor enables performance index measurement

6.3.3 Block Diagram

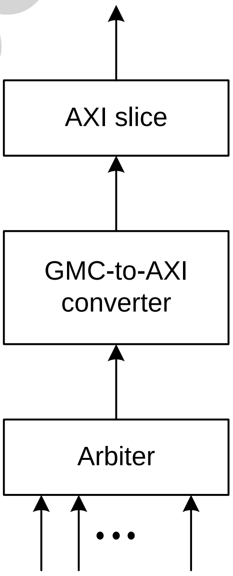

Figure 6-4. SMI local arbiter block diagram

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6.3.4 Register Definition

The base addresses of local arbiters are listed below.

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Table 6-1. Base addresses of SMI local arbiters

Module	Base address
SMI_LARB0	0x1401_5000
SMI_LARB1	0x1601_0000
SMI_LARB2	0x1500_1000
SMI_LARB3	0x1700_1000

The following register table is for SMI_LARB0. Replace the base address 0x14016000 with the base address of other SMI local arbiters when you are to program other SMI local arbiters.

Module name: SMI_LARB0 Base address: (+14015000h)

Address	Name	Width	Register Function
14015000	SMI_LARB_STAT	32	**SMI Local Arbiter Status Register** SMI local arbiter global status register
14015004	SMI_LARB_IRQ_EN	32	**SMI Local Arbiter IRQ Enable Register** Controls SMI local arbiter interrupt enabling settings.
14015008	SMI_LARB_IRQ_STATUS	32	**SMI Local Arbiter IRQ Status Register** Reports SMI local arbiter interrupt status.
1401500C	SMI_LARB_SLP_CON	32	**SMI Local Arbiter Sleep Control Register** Controls SMI local arbiter sleep procedure.
14015010	SMI_LARB_CON	32	**SMI Local Arbiter Control Status Register** SMI local arbiter control status register
14015014	SMI_LARB_CON_SET	32	**SMI Local Arbiter Control Set Register** SMI local arbiter control set register
14015018	SMI_LARB_CON_CLR	32	**SMI Local Arbiter Control Clear Register** SMI local arbiter control clear register
14015020	SMI_LARB_VC_PRI_MODE	32	**SMI Local Arbiter VC Priority Mode Register** Controls VC priority settings.
14015024	SMI_LARB_CMD_THRT_CON	32	**SMI Local Arbiter Command Throttling Control Register** Controls command throttling settings.
14015028	SMI_LARB_STARV_CON	32	**SMI Local Arbiter Starvation Control Register** Controls starvation control settings.
1401502C	SMI_LARB_EMI_CON	32	**SMI Local Arbiter EMI Control Register** Controls EMI feedback status.
14015030	SMI_LARB_SHARE_EN	32	**SMI Local Arbiter Sharable Bit Enable Register** Controls port 0~31 coherence settings.
14015050	SMI_LARB_BWL_EN	32	**SMI Local Arbiter Bandwidth Limiter Enable Register** Controls port 0~31 bandwidth limiter enabling.
14015054	SMI_LARB_BWL_SOFT_EN	32	**SMI Local Arbiter Bandwidth Limiter Soft Mode Enable Register** Controls port 0~31 bandwidth limiter soft mode enabling.
14015058	SMI_LARB_BWL_CON	32	**SMI Local Arbiter Bandwidth Limiter Control Register** Controls bandwidth limiters' overshoot bandwidth level.
14015060	SMI_LARB_OSTDL_EN	32	**SMI Local Arbiter Outstanding Limiter Enable Register** Controls port 0~31 outstanding limiter enabling.
14015064	SMI_LARB_OSTDL_SOFT_EN	32	**SMI Local Arbiter Outstanding Limiter Soft Mode Enable Register**

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Address	Name	Width	Register Function
			Controls port 0~31 outstanding limiter soft mode enabling.
14015070	SMI_LARB_ULTRA_DIS	32	**SMI Local Arbiter Ultra-high Sideband Disable Register** Forces disabling of port 0~31 ultra high sideband.
14015074	SMI_LARB_PREULTRA_DIS	32	**SMI Local Arbiter Pre-ultra-high Sideband Disable Register** Forces disabling of port 0~31 pre-ultra high sideband.
14015078	SMI_LARB_FORCE_ULTRA	32	**SMI Local Arbiter Force Enable Ultra-high Sideband Register** Forces enabling of port 0~31 ultra high sideband.
1401507C	SMI_LARB_FORCE_PREULTRA	32	**SMI Local Arbiter Force Enable Pre-ultra-high Sideband Register** Forces enabling of port 0~31 pre-ultra high sideband.
14015080	SMI_LARB_MST_GRP_SEL_L	32	**SMI Local Arbiter Master Group Selection Low Register** Sets up port 0~15 group ID.
14015084	SMI_LARB_MST_GRP_SEL_H	32	**SMI Local Arbiter Master Group Selection High Register** Sets up port 16~31 group ID.
14015090	SMI_LARB_INT_PATH_SEL	32	**SMI Local Arbiter Internal SRAM Access Path Selection Register** Controls the SMI local arbiter's internal SRAM path.
14015094	SMI_LARB_CMD_DET_CON	32	**SMI Local Arbiter Specific Command Detection Control Register** Controls the command detection function.
14015098	SMI_LARB_SPEC_CMD_DET	32	**SMI Local Arbiter Specific Command Detection Status Register** Records the occurrence of specific command.
1401509C	SMI_LARB_CRS4K_CMD_DET	32	**SMI Local Arbiter Cross-4KB Command Detection Status Register** Records the occurrence of cross 4K command.
140150A0	SMI_LARB_EXT_GREQ_VIO	32	**SMI Local Arbiter External Access Request Violation Status Register** Records the occurrence of external memory request address violation.
140150A4	SMI_LARB_INT_GREQ_VIO	32	**SMI Local Arbiter Internal Access Request Violation Status Register** Records the occurrence of internal memory request address violation.
140150A8	SMI_LARB_OSTD_UDF_VIO	32	**SMI Local Arbiter Outstanding Counter Underflow Violation Status Register** Records the occurrence of outstanding counter underflow.
140150AC	SMI_LARB_OSTD_CRS_VIO	32	**SMI Local Arbiter Cross-outstanding Access Violation Status Register** Records the occurrence of cross outstanding access of internal and external memory.
140150B0	SMI_LARB_FIFO_STAT	32	**SMI Local Arbiter FIFO Status Register** Shows SMI local arbiter's FIFO status.
140150B4	SMI_LARB_BUS_STAT	32	**SMI Local Arbiter AXI Bus Status Register** Shows SMI local arbiter's AXI bus status.
140150B8	SMI_LARB_CMD_THRT_STAT	32	**SMI Local Arbiter Command Throttling Status Register** Reports command throttling status.
140150BC	SMI_LARB_MON_REQ	32	**SMI Local Arbiter Primary Input Request Monitor Register** Monitors request of master 0~31.

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Address	Name	Width	Register Function
140150C0	SMI_LARB_REQ_MASK	32	**SMI Local Arbiter Primary Input Masked Request Monitor Register** Monitors request mask of master 0~31.
140150C4	SMI_LARB_REQ_DET	32	**SMI Local Arbiter Request Type Detection Monitor Register** Monitors occurrence of request type of master 0~31.
140150C8	SMI_LARB_EXT_ONGOING	32	**SMI Local Arbiter On-going External Memory Access Monitor Register** Monitors if the external memory access of a master is active.
140150CC	SMI_LARB_INT_ONGOING	32	**SMI Local Arbiter On-going Internal Memory Access Monitor Register** Monitors if the internal memory access of a master is active.
140150D0	SMI_LARB_MISC_MON0	32	**SMI Local Arbiter Miscellaneous Monitor Register** Monitors sleep protection related signals.
140150D8	SMI_LARB_ARB_MON0	32	**SMI Local Arbiter Arbitration Monitor Register 0** Monitors arbiter related signals.
140150DC	SMI_LARB_ARB_MON1	32	**SMI Local Arbiter Arbitration Monitor Register 1** Monitors arbiter related signals.
140150F0	SMI_LARB_DBG_CON	32	**SMI Local Arbiter Debug Control Register** Sets up SMI local arbiter's debugging features.
140150F4	SMI_LARB_TST_MODE	32	**SMI Local Arbiter Test Mode Control Register** Sets up SMI local arbiter's test modes.
14015100 ~ 1401517C	SMI_LARB_WRR_PORT[n] (n=0~31)	32	**SMI Local Arbiter Master Port Weighting Value Register** Controls external access port weighted round-robin credit.
14015180 ~ 140151FC	SMI_LARB_BWL_PORT[n] (n=0~31)	32	**SMI Local Arbiter Master Port Bandwidth Value Register** Controls each master's bandwidth limit value.
14015200 ~ 1401527C	SMI_LARB_OSTDL_PORT[n] (n=0~31)	32	**SMI Local Arbiter Master Port Outstanding Value Register** Controls outstanding limiter of memory access.
14015280 ~ 140152FC	SMI_LARB_OSTD_MON_PORT[n] (n=0~31)	32	**SMI Local Arbiter Master Port Outstanding Count Monitor Register** Monitors outstanding counter.
14015300 ~ 1401537C	SMI_LARB_PINFO[n] (n=0~31)	32	**SMI Local Arbiter Master Port Information Register** Reports port spec.
14015400	SMI_LARB_MON_EN	32	**SMI Local Arbiter Performance Monitor Enable Register** Enables performance monitor.
14015404	SMI_LARB_MON_CLR	32	**SMI Local Arbiter Performance Monitor Result Clear Register** Clears performance monitor.
14015408	SMI_LARB_MON_PORT	32	**SMI Local Arbiter Performance Monitor Port Selection Register** Selects one port to monitor its performance.
1401540C	SMI_LARB_MON_CON	32	**SMI Local Arbiter Performance Monitor Control Register** Controls performance monitor.
14015410	SMI_LARB_MON_ACT_CNT	32	**SMI Local Arbiter Active Count Performance Monitor Register** Counts active cycles for monitor.
14015414	SMI_LARB_MON_REQ_CNT	32	**SMI Local Arbiter Request Count Performance Monitor Register** Counts request cycles for monitor.

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Address	Name	Width	Register Function
14015418	SMI_LARB_MON_BEAT_CNT	32	**SMI Local Arbiter Beat Count Performance Monitor Register** Counts beats for monitor.
1401541C	SMI_LARB_MON_BYTE_CNT	32	**SMI Local Arbiter Byte Count Performance Monitor Register** Counts bytes for monitor.
14015420	SMI_LARB_MON_CP_CNT	32	**SMI Local Arbiter Command Phase Count Performance Monitor Register** Counts command phase cycles for monitor.
14015424	SMI_LARB_MON_DP_CNT	32	**SMI Local Arbiter Data Phase Count Performance Monitor Register** Counts data phase cycles for monitor.
14015428	SMI_LARB_MON_OSTD_CNT	32	**SMI Local Arbiter Outstanding Count Performance Monitor Register** Counts outstanding command count.
14015430	SMI_LARB_MON_CP_MAX	32	**SMI Local Arbiter Max. Command Phase Count Performance Monitor Register** Counts command phase maximum cycles for monitor.
14015434	SMI_LARB_MON_COS_MAX	32	**SMI Local Arbiter Max. Outstanding Count Performance Monitor Register** Counts outstanding transaction's maximum cycles for monitor.
14015480 ~ 140154A4	SMI_LARB_HIST_REC[n] (n=0~9)	32	**SMI Local Arbiter History Recorder Monitor Register**
14015FC0	SMI_LARB_MMU_EN	32	**SMI Local Arbiter Master Port MMU Enable Register** Controls port 0~31 MMU settings.
14015FC4	SMI_LARB_SECU_EN	32	**SMI Local Arbiter Master Port Security Enable Register** Controls port 0~31 security settings.
14015FD0	SMI_LARB_DOMN_0	32	**SMI Local Arbiter Master Port Domain Register 0** Controls port 0~7 domain settings.
14015FD4	SMI_LARB_DOMN_1	32	**SMI Local Arbiter Master Port Domain Register 1** Controls port 8~15 domain settings.
14015FD8	SMI_LARB_DOMN_2	32	**SMI Local Arbiter Master Port Domain Register 2** Controls port 16~23 domain settings.
14015FDC	SMI_LARB_DOMN_3	32	**SMI Local Arbiter Master Port Domain Register 3** Controls port 24~31 domain settings.

14015000 **SMI_LARB_STAT** **SMI Local Arbiter Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														INT1_BUSY	INT0_BUSY	EXT_BUSY
Type														RU	RU	RU
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
2	**INT1_BUSY**	INT1_BUSY	**Busy state indication of internal memory access path 1** 0: Idle 1: Busy
1	**INT0_BUSY**	INT0_BUSY	**Busy state indication of internal memory access path 0** 0: Idle 1: Busy
0	**EXT_BUSY**	EXT_BUSY	**Busy state indication of external memory access path** 0: Idle 1: Busy

14015004 **SMI_LARB_IRQ_EN** **SMI Local Arbiter IRQ Enable Register** **0000001F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TEST_IRQ_EN	CRS4K_DET_EN	CMD_DET_EN	STARV_IRQ_EN	VIO_IRQ_EN
Type												RW	RW	RW	RW	RW
Reset												1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
4	**TEST_IRQ_EN**	SW_IRQ_EN	**Enables software IRQ interrupt** 0: Disable 1: Enable
3	**CRS4K_DET_EN**	CRS4K_DET_EN	**Enables SMI cross-4K command detection interrupt** 0 : Disable 1 : Enable
2	**CMD_DET_EN**	CMD_DET_EN	**Enables SMI specific command detection interrupt** 0: Disable 1: Enable
1	**STARV_IRQ_EN**	STARV_IRQ_EN	**Enables SMI starvation interrupt** 0: Disable 1: Enable
0	**VIO_IRQ_EN**	VIO_IRQ_EN	**Enables SMI violation interrupt** 0: Disable 1: Enable

14015008 **SMI_LARB_IRQ_STATUS** **SMI Local Arbiter IRQ Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												STA	CRS	CM	STA	VIO

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												RV_ASSERT	4K_ASSERT	D_ASSERT	RV_ASSERT	_ASSERT
Type												RO	RO	RO	W1C	W1C
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4	**STARV_ASSERT**	SW_ASSERT	**Software IRQ status**
3	**CRS4K_ASSERT**	CRS4K_ASSERT	**Cross4K command is detected** Clear the status by disabling CRS4K_DET_EN in SMI_LARB_CRS4K_DET_CON register.
2	**CMD_ASSERT**	CMD_ASSERT	**Specific command is detected** Clear the status by disabling CMD_DET_EN in SMI_LARB_CMD_DET_CON register.
1	**STARV_ASSERT**	STARV_ASSERT	**Starvation occurrence when the command phase counter in performance monitor reaches the value set in SMI_LARB_MON_CON[25:16]**
0	**VIO_ASSERT**	VIO_ASSERT	**Violation status** Check detailed status at SMI_LARB_EXT_GREQ_VIO, SMI_LARB_INT_GREQ_VIO and SMI_LARB_OSTD_VIO registers.

1401500C   SMI_LARB_SLP_CON   SMI Local Arbiter Sleep Control Register   00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**SLP_PROT_RDY**
Type																RU
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**SLP_PROT_EN**
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
16	**SLP_PROT_RDY**	SLP_PROT_RDY	**Sleep protection ready** 0: Not ready 1: Ready (LARB is ready to be reset by software reset.)
0	**SLP_PROT_EN**	SLP_PROT_EN	**Enables sleep protection** 0: Disable 1 : Enable

14015010   SMI_LARB_CON   SMI Local Arbiter Control Status Register   00000073

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

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Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RESERVED			REG_DCM_EN	INT_DCM_EN	EXT_DCM_EN	AR_STD_AXI_EN	RESERVED	HP_PREULTRA_EN	HP_ULTRA_EN
Type							RU			RU	RU	RU	RU	RU	RU	RU
Reset							0	0	0	1	1	1	0	0	1	1

Bit(s)	Mnemonic	Name	Description
6	**REG_DCM_EN**	REG_DCM_EN	**Enables DCM for register access** 0: Disable 1: Enable
5	**INT_DCM_EN**	INT_DCM_EN	**Enables DCM for internal memory access** 0: Disable 1: Enable
4	**EXT_DCM_EN**	EXT_DCM_EN	**Enables DCM for external memory access** 0: Disable 1: Enable
3	**AR_STD_AXI_EN**	AR_STD_AXI_EN	**Enables standard AXI for AR AXI slice** 0: Disable. The AR command can change despite arvalid is issued. 1: Enable. The AR command cannot change when arvalid is issued before arready is asserted.
1	**HP_PREULTRA_EN**	HP_PREULTRA_EN	**Enables pre-ultra high sideband signal in AXI** Pre-ultra sideband signal is attached in AXI when HP_PREULTRA_EN is set 1 and {gpreultra,gultra} of the corresponding master is {1,0} at arbitration cycle. 0: Disable 1: Enable
0	**HP_ULTRA_EN**	HP_ULTRA_EN	**Enables ultra high sideband signal in AXI** Ultra sideband signal is attached in AXI when HP_ULTRA_EN is set 1 and gultra of the corresponding master is 1 at arbitration cycle. 0: Disable 1: Enable

14015014 **SMI_LARB_CON_SET** **SMI Local Arbiter Control Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RESERVED			REG_DCM_EN_SET	INT_DCM_EN_SET	EXT_DCM_EN_SET	AR_STD_AXI_EN_SET	RESERVED	HP_PREULTRA_EN_SET	HP_ULTRA_EN_SET
Type							WO			WO	WO	WO	WO	WO	WO	WO
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6	**REG_DCM_EN_S**	REG_DCM_EN_SET	**Enables DCM for register access** 0: Disable

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Bit(s)	Mnemonic	Name	Description
	ET		1: Enable
5	INT_DCM_EN_SET	INT_DCM_EN_SET	**Enables DCM for internal memory access** 0: Disable 1: Enable
4	EXT_DCM_EN_SET	EXT_DCM_EN_SET	**Enables DCM for external memory access** 0: Disable 1: Enable
3	AR_STD_AXI_EN_SET	AR_STD_AXI_EN_SET	**Enables standard AXI for AR AXI slice** 0: Disable. The AR command can change despite arvalid is issued. 1: Enable. The AR command cannot change when arvalid is issued before arready is asserted.
1	HP_PREULTRA_EN_SET	HP_PREULTRA_EN_SET	**Enables pre-ultra high sideband signal in AXI** 0: Disable 1: Enable
0	HP_ULTRA_EN_SET	HP_ULTRA_EN_SET	**Enables ultra high sideband signal in AXI** 0: Disable 1: Enable

14015018 **SMI_LARB_CON_CLR** **SMI Local Arbiter Control Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RESERVED			REG_DCM_CLR	INT_DCM_EN_CLR	EXT_DCM_EN_CLR	AR_STD_AXI_EN_CLR	RESERVED	HP_PREULTRA_EN_CLR	HP_ULTRA_EN_CLR
Type							WO			WO	WO	WO	WO	WO	WO	WO
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6	REG_DCM_CLR	REG_DCM_CLR	**Enables DCM for register access** 0: Enable 1: Disable
5	INT_DCM_EN_CLR	INT_DCM_EN_CLR	**Enables DCM for internal memory access** 0: Enable 1 : Disable
4	EXT_DCM_EN_CLR	EXT_DCM_EN_CLR	**Enables DCM for external memory access** 0: Enable 1: Disable
3	AR_STD_AXI_EN_CLR	AR_STD_AXI_EN_CLR	**Enables standard AXI for AR AXI slice** 0: Enable. The AR command cannot change when arvalid is issued before arready is asserted. 1: Disable. The AR command can change despite arvalid is issued.
1	HP_PREULTRA_EN_CLR	HP_PREULTRA_EN_CLR	**Enables pre-ultra high sideband signal in AXI** 0: Disable 1: Enable
0	HP_ULTRA_EN_	HP_ULTRA_EN	**Enables ultra high sideband signal in AXI**

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Bit(s)	Mnemonic	Name	Description
	CLR	_CLR	0: Disable 1: Enable

14015020 **SMI_LARB_VC_PRI_MODE** **SMI Local Arbiter VC Priority Mode Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							VC_PRI_MODE	RMODE_CHG							VC_PRI_MODE	
Type							RU	RU							RW	
Reset							0	0							0	0

Bit(s)	Mnemonic	Name	Description
9	VC_PRI_MODE	WMODE_CHG	**VC_PRI_MODE can be changed dynamically but may not be taken by arbiter at once** The status indicates the new value of VC priority mode has been taken or not in write arbiter. 0: New value of VC priority mode has been updated in write arbiter. 1: New value of VC priority mode is still not updated in write arbiter.
8		RMODE_CHG	**VC_PRI_MODE can be changed dynamically but may not be taken by arbiter at once** The status indicates the new value of VC priority mode has been taken or not in read arbiter. 0: New value of VC priority mode has been updated in read arbiter. 1: New value of VC priority mode is still not updated in read arbiter.
1:0	VC_PRI_MODE	VC_PRI_MODE	**VC priority mode** 2'b00: VC0>VC1>VC2 2'b01: VC0>VC1=VC2 2'b10: VC0=VC1=VC2 2'b11: Reserved

14015024 **SMI_LARB_CMD_THRT_CON** **SMI Local Arbiter Command Throttling Control Register** **08370246**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AW_COMMIT_SRC	AR_COMMIT_SRC	WR_COD_EN			WR_COD_LMT						WR_EN	RD_NU_EN	RD_EN
Type			RW	RW	RW			RW						RW	RW	RW
Reset			0	0	1			0	0	0	1	1		1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					WR_LMT				RD_NU_LMT				RD_LMT			
Type					RW				RW				RW			
Reset					0	0	1	0	0	1	0	0	0	1	1	0

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Bit(s)	Mnemonic	Name	Description
29	**AW_COMMIT_SRC**	AW_COMMIT_SRC	**Write command commit source** 0: From smi_common 1: From SMI_LARB internal
28	**AR_COMMIT_SRC**	AR_COMMIT_SRC	**Read command commit source** 0: From smi_common 1: From SMI_LARB internal
27	**WR_COD_EN**	WR_COD_EN	**Enables write command over data throttling** 0: Disable 1: Enable
24:20	**WR_COD_LMT**	WR_COD_LMT	**Write command over data throttling limit**
18	**WR_EN**	WR_EN	**Enables write command throttling** 0: Disable 1: Enable
17	**RD_NU_EN**	RD_NU_EN	**Enables read non-ultra command throttling** 0: Disable 1: Enable
16	**RD_EN**	RD_EN	**Enables read command throttling** 0: Disable 1: Enable
11:8	**WR_LMT**	WR_LMT	**Write command throttling limit**
7:4	**RD_NU_LMT**	RD_NU_LMT	**Read non-ultra command throttling limit**
3:0	**RD_LMT**	RD_LMT	**Read command throttling limit**

14015028 **SMI_LARB_STARV_CON** **SMI Local Arbiter Starvation Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**STARV_EN**
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**STARV_ID**								**STARV_CNT**							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	**STARV_EN**	STARV_EN	**Enables starvation counter** 0: Disable 1: Enable
15:8	**STARV_ID**	STARV_ID	**Master ID for starvation protection** STARV_ID = 'd0 chooses MASTER #0, STARV_ID = 'd1 chooses MASTER #1, and so on.
7:0	**STARV_CNT**	STARV_CNT	**Starvation trigger timer** Time unit: 8T. For example, the master which asserts "greq" for 8T and does not get "glcomd" can trigger the starvation counter if the STARV_CNT is set 1.

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1401502C	SMI_LARB_EMI_CON	SMI Local Arbiter EMI Control Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														OSTD_DBL_DIS	PRI_MASK_DIS	EMI_CHN_DIS
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2	**OSTD_DBL_DIS**	OSTD_DBL_DIS	**Disables doubling outstanding limit when EMI is empty** 0: Enable doubling outstanding limit by EMI status 1: Disable doubling outstanding limit by EMI status
1	**PRI_MASK_DIS**	PRI_MASK_DIS	**Disables priority mask** 0: Enable masking of pre-ultra sideband EMI status 1: Disable masking of pre-ultra sideband by EMI status
0	**EMI_CHN_DIS**	EMI_CHN_DIS	**Disables EMI channel selection in LARB to behaves like single channel** 0: Does no disable 1: Disable (behave like single channel)

14015030	SMI_LARB_SHARE_EN	SMI Local Arbiter Sharable Bit Enable Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SHARE_EN[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SHARE_EN[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SHARE_EN**	SHARE_EN	**Enabling bits for coherent transaction of port 0 - 31** This register is only set for external access masters. Each bit controls a master. MSB controls master 31, and LSB controls master 0. Note: There is no coherence path in this project. 0: Agent transaction is a non-coherent transaction. 1: Agent transaction is a coherent transaction.

14015050	SMI_LARB_BWL_EN	SMI Local Arbiter Bandwidth Limiter Enable Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	BWL_EN[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BWL_EN[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	BWL_EN	BWL_EN	**Enables bandwidth limiter** Each port is controlled by 1 bit. MSB controls port 31, and LSB controls port 0. 0: Disable 1: Enable

14015054 **SMI_LARB_BWL_SOFT_EN** **SMI Local Arbiter Bandwidth Limiter Soft Mode Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BWL_SOFT_EN[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BWL_SOFT_EN[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	BWL_SOFT_EN	BWL_SOFT_EN	**Enables bandwidth limiter soft mode** Each port is controlled by 1 bit. MSB controls port 31, and LSB controls port 0. The soft mode means ultra-high request can access DRAM without bandwidth limitation. 0: Disable 1: Enable

14015058 **SMI_LARB_BWL_CON** **SMI Local Arbiter Bandwidth Limiter Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BWL_CON	
Type															RW	
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1:0	BWL_CON	BWL_CON	**Gives master ports extra bandwidth quota when starting access if bandwidth limiter is enabled** 00: Maximum/2 01: Maximum/4 10: Maximum/8

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Bit(s)	Mnemonic	Name	Description
			11: 0

14015060 **SMI_LARB_OSTDL_EN** **SMI Local Arbiter Outstanding Limiter Enable Register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OSTD_EN[31:16]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OSTD_EN[15:0]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0	OSTD_EN	OSTDL_EN	**Enables outstanding limiter** Each port is controlled by 1 bit. MSB controls port 31, and LSB controls port 0. 0: Disable 1: Enable

14015064 **SMI_LARB_OSTDL_SOFT_EN** **SMI Local Arbiter Outstanding Limiter Soft Mode Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OSTD_SOFT_EN[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OSTD_SOFT_EN[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	OSTD_SOFT_EN	OSTDL_SOFT_EN	**Enables outstanding limiter soft mode** Each port is controlled by 1 bit. MSB controls port 31, and LSB controls port 0. The soft mode means ultra-high request can access DRAM without outstanding limitation. 0: Disable 1: Enable

14015070 **SMI_LARB_ULTRA_DIS** **SMI Local Arbiter Ultra-high Sideband Disable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ULTRA_DIS[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ULTRA_DIS[15:0]															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	ULTRA_DIS	ULTRA_DIS	**Disables ultra high sideband signal** Each port is controlled by 1 bit. MSB controls port 31, and LSB controls port 0. The priority of FORCE_ULTRA is higher than ULTRA_DIS, i.e. when FORCE_ULTRA and ULTRA_DIS are both set, the ultra signal will still be forced high. 0: Enable ultra high capability 1: Disable ultra high capability

14015074 SMI_LARB_PREULTRA_DIS — SMI Local Arbiter Pre-ultra-high Sideband Disable Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PREULTRA_DIS[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PREULTRA_DIS[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	PREULTRA_DIS	PREULTRA_DIS	**Disables pre-ultra high sideband signal** Each port is controlled by 1 bit. MSB controls port 31, and LSB controls port 0. The priority of FORCE_PREULTRA is higher than PREULTRA_DIS, i.e. when FORCE_PREULTRA and PREULTRA_DIS are both set, the preultra signal will still be forced high. 0: Enable pre-ultra high capability 1: Disable pre-ultra high capability

14015078 SMI_LARB_FORCE_ULTRA — SMI Local Arbiter Force Enable Ultra-high Sideband Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FORCE_ULTRA[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FORCE_ULTRA[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	FORCE_ULTRA	FORCE_ULTRA	**Forces ultra high sideband signal** Each port is controlled by 1 bit. MSB controls port 31, and LSB controls port 0. The priority of FORCE_ULTRA is higher than ULTRA_DIS, i.e. when FORCE_ULTRA and ULTRA_DIS are both set, the ultra signal will still be forced high. 0: No force

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Bit(s)	Mnemonic	Name	Description
			1: Force ultra high

1401507C **SMI_LARB_FORCE_PREULTRA** **SMI Local Arbiter Force Enable Pre-ultra-high Sideband Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FORCE_PREULTRA[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FORCE_PREULTRA[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	FORCE_PREULTRA	FORCE_PREULTRA	**Forces pre-ultra high sideband signal** Each port is controlled by 1 bit. MSB controls port 31, and LSB controls port 0. The priority of FORCE_PREULTRA is higher than PREULTRA_DIS, i.e. when FORCE_PREULTRA and PREULTRA_DIS are both set, the preultra signal will still be forced high. 0: No force 1: Force pre-ultra high

14015080 **SMI_LARB_MST_GRP_SEL_L** **SMI Local Arbiter Master Group Selection Low Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GRP_SEL_L[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GRP_SEL_L[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	GRP_SEL_L	GRP_SEL_L	**Group setting for port 0 - 15** Each 2-bit controls a master. For example, bit[1:0] controls master 0, and bit[3:2] controls master 1, etc. The preultra sideband signals of the masters with the same group are dynamically masked according to EMI's full status.

14015084 **SMI_LARB_MST_GRP_SEL_H** **SMI Local Arbiter Master Group Selection High Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GRP_SEL_H[31:16]															

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Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**GRP_SEL_H[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	GRP_SEL_H	GRP_SEL_H	**Group setting for port 16 - 31** Each 2-bit controls a master. For example, bit[1:0] controls master 16, and bit[3:2] controls master 17, etc. The preultra sideband siganls of the masters with the same group are dynamically masked according to EMI's full status.

14015090 SMI_LARB_INT_PATH_SEL — SMI Local Arbiter Internal SRAM Access Path Selection Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**INT_PATH_SEL[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**INT_PATH_SEL[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	INT_PATH_SEL	INT_PATH_SEL	**Selects path for internal port defect** 0: Path 0 1: Path 1 Each internal master is controlled by one bit. LSB controls the internal access master 0; MSB controls the internal access master 31. To find the port number of a master name, refer to the "Programming Guide" section.

14015094 SMI_LARB_CMD_DET_CON — SMI Local Arbiter Specific Command Detection Control Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**SPEC_CMD_DET_LEN**					**SPEC_CMD_DET_SIZE**			**SPEC_CMD_DET_RW**	**SPEC_CMD_DET_EN**	**CRS4K_CMD_DET_RW**	**CRS4K_CMD_DET_EN**
Type					RW					RW			RW	RW	RW	RW
Reset					0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
11:8		SPEC_CMD_DET_LEN	**Specific command detection with target transaction length**
6:4		SPEC_CMD_DET_SIZE	**Specific command detection with target transaction size**
3		SPEC_CMD_DET_RW	**Specific command detection with read or write transaction** 0: Read 1: Write
2		SPEC_CMD_DET_EN	**Enables specific command detection.** The detection is only valid for external memory access. 0: Disable 1: Enable
1		CRS4K_CMD_DET_RW	**Cross-4K command detection with read or write transaction** 0: Read 1: Write
0		CRS4K_CMD_DET_EN	**Enables Cross-4K command detection.** The detection is only valid for external memory access. 0: Disable 1: Enable

14015098 **SMI_LARB_SPEC_CMD_DET** **SMI Local Arbiter Specific Command Detection Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPEC_CMD_DET[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPEC_CMD_DET[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	SPEC_CMD_DET	SPEC_CMD_DET	**Status register indicating any specified command is detected for a master's external request** Each port is indicated by 1 bit. MSB controls port 31, and LSB controls port 0. 0: Not detected 1: Detected

1401509C **SMI_LARB_CRS4K_CMD_DET** **SMI Local Arbiter Cross-4KB Command Detection Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRS4K_CMD_DET[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRS4K_CMD_DET[15:0]															

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Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CRS4K_CMD_DET**	CRS4K_CMD_DET	**Status register indicating any cross-4KB command is detected for a master's external request** Each port is indicated by 1 bit. MSB controls port 31, and LSB controls port 0. 0: Not detected 1: Detected

140150A0 **SMI_LARB_EXT_GREQ_VIO** **SMI Local Arbiter External Access Request Violation Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EXT_GREQ_VIO[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXT_GREQ_VIO[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**EXT_GREQ_VIO**	EXT_GREQ_VIO	**Status register indicate any violation occurrence for a master's external request** Each port is indicated by 1 bit. MSB controls port 31, and LSB controls port 0. 0: No violation 1: Violation

140150A4 **SMI_LARB_INT_GREQ_VIO** **SMI Local Arbiter Internal Access Request Violation Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_GREQ_VIO[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT_GREQ_VIO[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**INT_GREQ_VIO**	INT_GREQ_VIO	**Status register indicating any violation occurrence for a master's internal request** Each port is indicated by 1 bit. MSB controls port 31, and LSB controls port 0. 0: No violation 1 : Violation

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140150A8	SMI_LARB_OSTD_UDF_VIO	SMI Local Arbiter Outstanding Counter Underflow Violation Status Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OSTD_UDF_VIO[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OSTD_UDF_VIO[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	OSTD_UDF_VIO	OSTD_UDF_VIO	**Status register indicating underflow occurrence for a master's outstanding counter** Each port is indicated by 1 bit. MSB controls port 31, and LSB controls port 0. 0: No violation 1: Violation

140150AC	SMI_LARB_OSTD_CRS_VIO	SMI Local Arbiter Cross-outstanding Access Violation Status Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OSTD_CRS_VIO[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OSTD_CRS_VIO[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	OSTD_CRS_VIO	OSTD_CRS_VIO	**Status register indicating the occurrence of cross outstanding access of internal and external memory for a master** Each port is indicated by 1 bit. MSB controls port 31, and LSB controls port 0. 0: No violation 1: Violation

140150B0	SMI_LARB_FIFO_STAT	SMI Local Arbiter FIFO Status Register	000AAAAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													B_EMP	B_FULL	R_EMP	R_FULL
Type													RU	RU	RU	RU
Reset													1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	W_EMP	W_FULL	AW_EM	AW_FU	AR_EMP	AR_FUL	I_EMP	I_FULL	D_EMP	D_FULL	C_EMP	C_FULL	W_FIFO	W_FIFO	R_FIFO	R_FIFO

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			P	LL		L							_EM P	_FU LL	_EM P	_FU LL
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
19	**B_EMP**	B_EMP	AXI slice FIFO empty indication
18	**B_FULL**	B_FULL	AXI slice FIFO full indication
17	**R_EMP**	R_EMP	AXI slice FIFO empty indication
16	**R_FULL**	R_FULL	AXI slice FIFO full indication
15	**W_EMP**	W_EMP	AXI slice FIFO empty indication
14	**W_FULL**	W_FULL	AXI slice FIFO full indication
13	**AW_EMP**	AW_EMP	AXI slice FIFO empty indication
12	**AW_FULL**	AW_FULL	AXI slice FIFO full indication
11	**AR_EMP**	AR_EMP	AXI slice FIFO empty indication
10	**AR_FULL**	AR_FULL	AXI slice FIFO full indication
9	**I_EMP**	I_EMP	GMC2AXI ififo. FIFO empty indication
8	**I_FULL**	I_FULL	GMC2AXI ififo. FIFO full indication
7	**D_EMP**	D_EMP	GMC2AXI data FIFO empty indication
6	**D_FULL**	D_FULL	GMC2AXI data FIFO full indication
5	**C_EMP**	C_EMP	GMC2AXI cfifo FIFO empty indication
4	**C_FULL**	C_FULL	GMC2AXI cfifo FIFO full indication
3	**W_FIFO_EMP**	W_FIFO_EMP	Write command FIFO empty indication
2	**W_FIFO_FULL**	W_FIFO_FULL	Write command FIFO full indication
1	**R_FIFO_EMP**	R_FIFO_EMP	Read command FIFO empty indication
0	**R_FIFO_FULL**	R_FIFO_FULL	Read command FIFO full indication

140150B4 **SMI_LARB_BUS_STAT** **SMI Local Arbiter AXI Bus Status Register** **000D83E0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													**BREADY_M**	**RREADY_M**	**WREADY_M**	**AWREADY_M**
Type													RU	RU	RU	RU
Reset													1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ARREADY_M**	**BVALID_M**	**RVALID_M**	**WVALID_M**	**AWVALID_M**	**ARVALID_M**	**BREADY**	**RREADY**	**WREADY**	**AWREADY**	**ARREADY**	**BVALID**	**RVALID**	**WVALID**	**AWVALID**	**ARVALID**
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	1	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
19	**BREADY_M**	BREADY_M	External AXI bus ready indication
18	**RREADY_M**	RREADY_M	External AXI bus ready indication
17	**WREADY_M**	WREADY_M	External AXI bus ready indication
16	**AWREADY_M**	AWREADY_M	External AXI bus ready indication
15	**ARREADY_M**	ARREADY_M	External AXI bus ready indication
14	**BVALID_M**	BVALID_M	External AXI bus valid indication
13	**RVALID_M**	RVALID_M	External AXI bus valid indication
12	**WVALID_M**	WVALID_M	External AXI bus valid indication
11	**AWVALID_M**	AWVALID_M	External AXI bus valid indication
10	**ARVALID_M**	ARVALID_M	External AXI bus valid indication
9	**BREADY**	BREADY	Internal AXI bus ready indication
8	**RREADY**	RREADY	Internal AXI bus ready indication
7	**WREADY**	WREADY	Internal AXI bus ready indication
6	**AWREADY**	AWREADY	Internal AXI bus ready indication
5	**ARREADY**	ARREADY	Internal AXI bus ready indication
4	**BVALID**	BVALID	Internal AXI bus valid indication
3	**RVALID**	RVALID	Internal AXI bus valid indication
2	**WVALID**	WVALID	Internal AXI bus valid indication
1	**AWVALID**	AWVALID	Internal AXI bus valid indication
0	**ARVALID**	ARVALID	Internal AXI bus valid indication

140150B8 **SMI_LARB_CMD_THRT_STAT** **SMI Local Arbiter Command Throttling Status Register** **00200020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**W_CMD_IN_Q**										**WR_ARB_EN**	**CMD_THRT_WR_COD**	**CMD_THRT_WR**		**W_OSTD_FULL**	**W_FIFO_FULL**
Type	RU										RU	RU	RU		RU	RU
Reset	0	0	0	0							1	0	0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**R_CMD_IN_Q**				**R_CMD_NU_IN_Q**						**RD_ARB_EN**		**CMD_THRT**	**CMD_THRT**	**R_OSTD_FU**	**R_FIFO_FU**

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													_RD	_RD _NU	LL	LL
Type	RU				RU						RU		RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0			1		0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28	**W_CMD _IN_Q**	W_CMD_IN_Q	Non-ultra write command in queue
21	**WR_ARB _EN**	WR_ARB_EN	Enables write arbitration
20	**CMD_TH RT_WR_ COD**	CMD_THRT_WR _COD	Write command over data throttling
19	**CMD_TH RT_WR**	CMD_THRT_WR	Write command throttling
17	**W_OSTD _FULL**	W_OSTD_FULL	Write command outstanding full
16	**W_FIFO _FULL**	W_FIFO_FULL	Write command FIFO full
15:12	**R_CMD_ IN_Q**	R_CMD_IN_Q	Non-ultra read command in queue
11:8	**R_CMD_ NU_IN_ Q**	R_CMD_NU_IN _Q	Read command in queue
5	**RD_ARB _EN**	RD_ARB_EN	Enables read arbitration
3	**CMD_TH RT_RD**	CMD_THRT_RD	Read command throttling
2	**CMD_TH RT_RD_ NU**	CMD_THRT_RD _NU	Non-ultra read command throttling
1	**R_OSTD _FULL**	R_OSTD_FULL	Read command outstanding full
0	**R_FIFO_ FULL**	R_FIFO_FULL	Read command FIFO full

140150BC **SMI_LARB_MON_REQ** **SMI Local Arbiter Primary Input Request Monitor Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MON_BUS_REQ[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MON_BUS_REQ[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**MON_B US_REQ**	MON_BUS_REQ	**Monitor GMC bus request for master 0 ~31.** LSB indicates the monitored request of master 0; MSB indicates the monitored request of master 31.

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140150C0	SMI_LARB_REQ_MASK	SMI Local Arbiter Primary Input Masked Request Monitor Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REQ_MASK[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REQ_MASK[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	REQ_MASK	REQ_MASK	**Masks monitor GMC bus request for master 0 ~31** LSB indicates the monitored request of master 0; MSB indicates the monitored request of master 31.

140150C4	SMI_LARB_REQ_DET	SMI Local Arbiter Request Type Detection Monitor Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REQ_DET[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REQ_DET[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	REQ_DET	REQ_DET	**Detects occurrence of each request type for external access master 0 ~31** LSB indicates the monitored request of master 0; MSB indicates the monitored request of master 31.

140150C8	SMI_LARB_EXT_ONGOING	SMI Local Arbiter On-going External Memory Access Monitor Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EXT_ONGOING[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXT_ONGOING[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	EXT_ONGOING	EXT_ONGOING	Active status of external memory access of master 0~31

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140150CC SMI_LARB_INT_ONGOING — SMI Local Arbiter On-going Internal Memory Access Monitor Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_ONGOING[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT_ONGOING[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	INT_ONGOING	INT_ONGOING	Active status of internal memory access of master 0~31

140150D0 SMI_LARB_MISC_MON0 — SMI Local Arbiter Miscellaneous Monitor Register — 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														SLP_PROT_STATE		
Type														RU		
Reset														0	0	1

Bit(s)	Mnemonic	Name	Description
2:0	SLP_PROT_STATE	SLP_PROT_STATE	State of sleep protection state machine

140150D8 SMI_LARB_ARB_MON0 — SMI Local Arbiter Arbitration Monitor Register 0 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											ARB_MON0[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ARB_MON0[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:0	ARB_MON0	ARB_MON0	Read arbitration signal monitor

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140150DC **SMI_LARB_ARB_MON1** **SMI Local Arbiter Arbitration Monitor Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											ARB_MON1[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ARB_MON1[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:0	**ARB_MON1**	ARB_MON1	Write arbitration signal monitor

140150F0 **SMI_LARB_DBG_CON** **SMI Local Arbiter Debug Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HIST_REC_BUSY				HIST_REC_WPTR						HIST_REC_MAX[9:4]					
Type	RU				RU						RW					
Reset	0				0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_REC_MAX[3:0]						HIST_REC_SEL	HIST_REC_EN		REQ_DET_SEL		REQ_DET_EN	DBG_SEL			LA_EN
Type	RW						RW	RW		RW		RW	RW			RW
Reset	0	0	0	0			0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**HIST_REC_BUSY**	HIST_REC_BUSY	**History recorder is busy** 1'b0: Idle 1'b1: Busy
27:24	**HIST_REC_WPTR**	HIST_REC_WPTR	**History recorder write pointer**
21:12	**HIST_REC_MAX**	HIST_REC_MAX	**Sampling distance between 2 history samples** This setting must be bigger than 5.
9	**HIST_REC_SEL**	HIST_REC_SEL	**General selection signal for history recorder** 1'b0: Select cmd_thrt_rd for read and cmd_thrt_wr_cod for write 1'b1: Select cmd_thrt_rd_nu for read and cmd_thrt_wr for write
8	**HIST_REC_EN**	HIST_REC_EN	**Enables history recorder** 0: Disable 1: Enable
6:5	**REQ_DET_SEL**	REQ_DET_SEL	**Selects request type for request detection** 2'b00: All 2'b01: Ultra 2'b10: Preultra 2'b11: Normal
4	**REQ_DET_EN**	REQ_DET_EN	**Enables request detection** 1'b0: Disable

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Bit(s)	Mnemonic	Name	Description
			1'b1: Enable
3:1	**DBG_SEL**	DBG_SEL	**Selects debugging monitor**
0	**LA_EN**	LA_EN	**Enables embedded LA**

140150F4 **SMI_LARB_TST_MODE** **SMI Local Arbiter Test Mode Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														TEST_AR_OOO_DIS	TEST_AR_PROMOTE_DIS	TEST_IRQ
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2	**TEST_AR_OOO_DIS**	TEST_AR_OOO_DIS	**Test mode register for disabling out-of-order mode in AR slice** 0: Does not disable 1: Disable out-of-order in AR slice. Force in-order
1	**TEST_AR_PROMOTE_DIS**	TEST_AR_PROMOTE_DIS	**Test mode register for disabling ultra promotion in AR slice** 0: Does not disable 1: Disable
0	**TEST_IRQ**	TEST_IRQ	**TEST mode register for triggering SMI IRQ** 0: Disable 1: Enable

14015100 ~ 1401517C **SMI_LARB_WRR_PORT[n] (n=0~31)** **SMI Local Arbiter Master Port Weighting Value Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															WRR_PORT	
Type															RW	
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1:0	**WRR_PORT**	WRR_PORT	**Weighted round-robin setting for external access masters** This register controls the number of successive grants for a master

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Bit(s)	Mnemonic	Name	Description
			if its request keeps asserting. Each master occupies 2 bits which support setting up 1~4 successive grants for a master. From the start address 0x100, offset 0x0 represents port 0, offset 0x4 represents port 1, and so on. 2'b00: Grant once 2'b01: Successive 2 grants 2'b10: Successive 3 grants 2'b11: Successive 4 grants

14015180 ~ 140151FC **SMI_LARB_BWL_PORT[n] (n=0~31)** **SMI Local Arbiter Master Port Bandwidth Value Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BWL_PORT							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	BWL_PORT	BWL_PORT	**Bandwidth limiter threshold of master port m** The sum of the threshold of all external ports should be less than 1,024, and the sum of the threshold of all internal ports should be less than 1,024. From the start address 0x180, offset 0x0 represents port 0, offset 0x4 represents port 1, and so on. The value shall be <=128 for each port. When a master port's BWL_PORT is set to 0, it cannot be granted anymore.

14015200 ~ 1401527C **SMI_LARB_OSTDL_PORT[n] (n=0~31)** **SMI Local Arbiter Master Port Outstanding Value Register** **0000001F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												OSTDL_PORT				
Type												RW				
Reset												1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
4:0	OSTDL_PORT	OSTDL_PORT	**Outstanding limiter threshold of port m** From the start address 0x200, offset 0x0 represents port 0, offset 0x4 represents port 1, and so on. When a master port's OSTDL_PORT is set to 0, it cannot be granted anymore.

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14015280 ~ 140152FC	**SMI_LARB_OSTD_MON_PORT[n] (n=0~31)**	**SMI Local Arbiter Master Port Outstanding Count Monitor Register**	**00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												OSTD_MON_PORT				
Type												RU				
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0	**OSTD_MON_PORT**	OSTD_MON_PORT	**Outstanding count of port m** From the start address 0x280, offset 0x0h represents port 0, offset 0x4 represents port 1, and so on. This register is only valid when the master's outstanding limiter is turned on.

14015300 ~ 1401537C	**SMI_LARB_PINFO[n] (n=0~31)**	**SMI Local Arbiter Master Port Information Register**	**00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									NUM_IN_VC_VALID	NUM_IN_VC					VC_NUM_VALID	VC_NUM[4:4]
Type									RO	RO					RO	RO
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VC_NUM[3:0]				INT_PORT_VALID	INT_PORT_NUM					EXT_PORT_VALID	EXT_PORT_NUM				
Type	RO				RO	RO					RO	RO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23	**NUM_IN_VC_VALID**	NUM_IN_VC_VALID	**Value of NUM_IN_VC is valid or not** From the start address 0x300, offset 0x0 represents master 0, offset 0x4 represents master 1, and so on. 0: Invalid 1: Valid
22:18	**NUM_IN_VC**	NUM_IN_VC	**Port number of a master in VC** From the start address 0x300, offset 0x0 represents master 0, offset 0x4 represents master 1, and so on.
17	**VC_NUM_VALID**	VC_NUM_VALID	**Value of VC_NUM is valid or not** From the start address 0x300, offset 0x0 represents master 0, offset 0x4 represents master 1, and so on. 0: Invalid 1: Valid
16:12	**VC_NUM**	VC_NUM	**Number of the VC to which a master port is connected**

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Bit(s)	Mnemonic	Name	Description
			From the start address 0x300, offset 0x0 represents master 0, offset 0x4 represents master 1, and so on.
11	**INT_PORT_VALID**	INT_PORT_VALID	**Value of INT_PORT_NUM is valid or not** From the start address 0x300, offset 0x0 represents master 0, offset 0x4 represents master 1, and so on. 0: Invalid 1: Valid
10:6	**INT_PORT_NUM**	INT_PORT_NUM	**Internal SRAM access port number of a master** From the start address 0x300, offset 0x0 represents master 0, offset 0x4 represents master 1, and so on.
5	**EXT_PORT_VALID**	EXT_PORT_VALID	**Value of EXT_PORT_NUM is valid or not** From the start address 0x300, offset 0x0 represents master 0, offset 0x4 represents master 1, and so on. 0: Invalid 1: Valid
4:0	**EXT_PORT_NUM**	EXT_PORT_NUM	**External memory access port number of a master** From the start address 0x300, offset 0x0 represents master 0, offset 0x4 represents master 1, and so on.

14015400 SMI_LARB_MON_EN SMI Local Arbiter Performance Monitor Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name																MON_EN
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**MON_EN**	MON_EN	**Selects performance monitor bus** 0: Stop counting 1: Start to count Note: When set to monitoring AXI master bus (MON_BUS=1), MON_TYPE must be set to monitoring only read or only write. Monitoring both read and write at same time is not supported for monitoring AXI bus.

14015404 SMI_LARB_MON_CLR SMI Local Arbiter Performance Monitor Result Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name																MON_CLR
Type																Oth

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																er
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**MON_CLR**	MON_CLR	**Clears performance monitor** 0: Disable clear 1: Enable clear When this bit is set to 1, it will only last for 1 cycle and will be automatically reset to 0 by hardware in the next cycle.

14015408 SMI_LARB_MON_PORT SMI Local Arbiter Performance Monitor Port Selection Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			MON_PORT_SEL3								MON_PORT_SEL2					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			MON_PORT_SEL1								MON_PORT_SEL0					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:24	**MON_PORT_SEL3**	MON_PORT_SEL3	**Performance monitor port selection3** This register is only valid when SMI_LARB_MON_CON[10] = 1. MON_PORT_SEL0 = 0 chooses MASTER0, MON_PORT_SEL0 = 1 chooses MASTER1, and so on. Only byte count can be monitored for the selected port in the SMI_LARB_MON_BYTE_CNT register.
21:16	**MON_PORT_SEL2**	MON_PORT_SEL2	**Performance monitor port selection2** This register is only valid when SMI_LARB_MON_CON[10] = 1. MON_PORT_SEL0 = 0 chooses MASTER0, MON_PORT_SEL0 = 1 chooses MASTER1, and so on. Only byte count can be monitored for the selected port in the SMI_LARB_MON_BEAT_CNT register.
13:8	**MON_PORT_SEL1**	MON_PORT_SEL1	**Performance monitor port selection1** This register is only valid when SMI_LARB_MON_CON[10] = 1. MON_PORT_SEL0 = 0 chooses MASTER0, MON_PORT_SEL0 = 1 chooses MASTER1, and so on. Only byte count can be monitored for the selected port in the SMI_LARB_MON_REQ_CNT register.
5:0	**MON_PORT_SEL0**	MON_PORT_SEL0	**Performance monitor port selection 0** MON_PORT_SEL0 = 0 chooses MASTER0, MON_PORT_SEL0 = 1 chooses MASTER1, and so on. When SMI_LARB_MON_CON[10] = 0, all performance indices can be monitored for the selected port. When SMI_LARB_MON_CON[10] = 1, only byte count can be monitored for the selected port in the SMI_LARB_MON_ACT_CNT register.

1401540C SMI_LARB_MON_CON SMI Local Arbiter Performance Monitor Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							STARV_TIME									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STARV_DEN					PARA_MODE	DP_MODE	CP_MODE	BEAT_MODE	STALL_SEL	REQ_SEL		DST_SEL		RW_SEL	
Type	RW					RW	RW	RW	RW	RW	RW		RW		RW	
Reset	0					0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
25:16	STARV_TIME	STARV_TIME	**Time of starvation** Unit: 1,024 cycles
15	STARV_DEN	STARV_DEN	**Detects bus starvation** 0: Disable 1: Enable
10	PARA_MODE	PARA_MODE	**Parallel bandwidth measurement mode** 0: Disable 1: Enable When the parallel bandwidth measurement mode is disabled, only 1 master can be selected at SMI_LARB_MON_PORT[5:0] to monitor its all performance indicees from SMI_LARB_ACT_CNT to SMI_LARB_MON_CP_MAX. When the parallel bandwidth measurement mode is enabled , 4 masters can be selected at SMI_LARB_MON_PORT[5:0], SMI_LARB_MON_PORT[13:8], SMI_LARB_MON_PORT[21:16] and SMI_LARB_MON_PORT[29:24] to monitor their byte count simultaneously at SMI_LARB_MON_ACT_CNT, SMI_LARB_MON_REQ_CNT, SMI_LARB_MON_BEAT_CNT, and SMI_LARB_MON_BYTE_CNT respectively.
9	DP_MODE	DP_MODE	**Data phase counter mode** 0: The data phase increases one when any outstanding transaction waits for data transfer. 1: The data phase increases N when N outstanding transactions are waiting for data transfer.
8	CP_MODE	CP_MODE	**Command phase counter mode** 0: Count the cycles when request is asserted before it is latched 1: Count the stall cycles
7	BEAT_MODE	BEAT_MODE	**Beat counter mode** 0: Beat counter counts when command is latched. 1: Beat counter counts when data is latched.
6	STALL_SEL	STALL_SEL	**Selects stall cycle** 0: Count stall cycle when a master's stall status is high. 1: Count stall cycle when a master's stall status is high and other masters' stall statuses are low.
5:4	REQ_SEL	REQ_SEL	**Selects request type which is to be monitored** 2'b00: All request types 2'b01: Only ultra high requests 2'b10: Only preultra high requests 2'b11: Only normal requests
3:2	DST_SEL	RW_SEL	**Selects read/write monitor** 2'b00: All (including read & write) 2'b01: Read only 2'b10: Write only 2'b11: All (including read & write)
1:0	RW_SEL	DST_SEL	**Selects destination** 2'b00: All (including internal & external) 2'b01: External only 2'b10: Internal only 2'b11: All (including internal & external)

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14015410 **SMI_LARB_MON_ACT_CNT** **SMI Local Arbiter Active Count Performance Monitor Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					ACT_CNT[27:16]											
Type					RU											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACT_CNT[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:0	ACT_CNT	ACT_CNT	**Monitor active counter** When SMI_LARB_MON_CON[10] = 0, ACT_CNT counts how many cycles when MON_EN = 1. When SMI_LARB_MON_CON[10] = 1, ACT_CNT counts byte counts of the master selected by MON_PORT_SEL0. It stops when reaching the upper bound, 28'hfffffff and is cleared when MON_CLR = 1.

14015414 **SMI_LARB_MON_REQ_CNT** **SMI Local Arbiter Request Count Performance Monitor Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					REQ_CNT[27:16]											
Type					RU											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REQ_CNT[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:0	REQ_CNT	REQ_CNT	**Monitor request counter** When SMI_LARB_MON_CON[10] = 0, REQ_CNT counts how many transactions when MON_EN = 1. The request type of the transaction can be controlled by REQ_SEL. When SMI_LARB_MON_CON[10] = 1 , REQ_CNT counts byte counts of the master selected by MON_PORT_SEL1. It stops when reaching the upper bound, 28'hfffffff and is cleared when MON_CLR = 1.

14015418 **SMI_LARB_MON_BEAT_CNT** **SMI Local Arbiter Beat Count Performance Monitor Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					BEAT_CNT[27:16]											
Type					RU											

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Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BEAT_CNT[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:0	**BEAT_CNT**	BEAT_CNT	**Performance monitor beat counter** When SMI_LARB_MON_CON[10] = 0, BEAT_CNT counts total number of data beats when MON_EN = 1. It is a multi-function counter controlled by BEAT_SEL. When SMI_LARB_MON_CON[10] = 1, BEAT_CNT counts byte counts of the master selected by MON_PORT_SEL2. It stops when reaching 28'hfffffff and is cleared when MON_CLR = 1.

1401541C SMI_LARB_MON_BYTE_CNT SMI Local Arbiter Byte Count Performance Monitor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**BYTE_CNT[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BYTE_CNT[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**BYTE_CNT**	BYTE_CNT	**Performance monitor byte counter** When SMI_LARB_MON_CON[10] = 0, BYTE_CNT counts the total number of data bytes transferred when MON_EN = 1. When SMI_LARB_MON_CON[10] = 1, BYTE_CNT counts byte counts of the master selected by MON_PORT_SEL3. It stops when reaching 32'hffffffff and is cleared when MON_CLR = 1.

14015420 SMI_LARB_MON_CP_CNT SMI Local Arbiter Command Phase Count Performance Monitor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**CP_CNT[27:16]**											
Type					RU											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CP_CNT[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:0	**CP_CNT**	CP_CNT	**Monitor command phase cycle counter** CP_CNT accumulates the cycles from greq=1 to the assertion of

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Bit(s)	Mnemonic	Name	Description
			glcomd when MON_EN = 1. It stops counting when reaching 28'hfffffff and is cleared when MON_CLR = 1.

14015424 SMI_LARB_MON_DP_CNT SMI Local Arbiter Data Phase Count Performance Monitor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DP_CNT[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DP_CNT[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	DP_CNT	DP_CNT	**Monitor data phase cycle counter** DP_CNT accumulates the cycles from the start of the data phase to its end when MON_EN = 1. It stops counting when reach 32'hffffffff and is cleared when MON_CLR = 1. Note: DP_CNT does not support profiling both read and write at the same time, i.e. mon_type[3:2] cannot be 2'b00.

14015428 SMI_LARB_MON_OSTD_CNT SMI Local Arbiter Outstanding Count Performance Monitor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												DP_CNT				
Type												RU				
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0	DP_CNT	OSTD_CNT	**Outstanding command counter** Shows the current outstanding count of the monitored master.

14015430 SMI_LARB_MON_CP_MAX SMI Local Arbiter Max. Command Phase Count Performance Monitor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													CP_MAX[19:16]			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CP_MAX[15:0]															

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Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:0	**CP_MAX**	CP_MAX	**Monitor command/data phase maximum** CDP_MAX records the max. latency of command or data phase (selected by MAX_SEL) among all transactions when MON_EN = 1 and is cleared when MON_CLR = 1.

14015434 **SMI_LARB_MON_COS_MAX** **SMI Local Arbiter Max. Outstanding Count Performance Monitor Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**COS_MAX**				
Type												RU				
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0	**COS_MAX**	OSTD_MAX	**Monitor maximum command outstanding number** COS_MAX records the max. number of outstanding transactions when MON_EN = 1 and is cleared when MON_CLR = 1.

14015480 ~ 140154A4 **SMI_LARB_HIST_REC[n] (n=0~9)** **SMI Local Arbiter History Recorder Monitor Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**HIST_REC_VLD**	**HIST_REC_DAT[30:16]**														
Type	RU	RU														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**HIST_REC_DAT[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		HIST_REC_VLD	**The history recorder entry is valid.**
30:0		HIST_REC_DAT	**History recorder content** [30:26]: Unfinished command count [25:19]: Finished command count [18:12]: Input command count [11:9]: Command throttled cycle count [8:6]: Outstanding full cycle count [5:3]: Ultra-high command phase count [2:0]: Command cphase count

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14015FC0	SMI_LARB_MMU_EN	SMI Local Arbiter Master Port MMU Enable Register	FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMU_EN[31:16]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MMU_EN[15:0]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0	MMU_EN	MMU_EN	**Enabling bits for VA transaction of port 0 - 31** Each bit controls a master. MSB controls master 31; LSB controls master 0. 0: Agent transaction is a PA transaction. 1: Agent transaction is a VA transaction.

14015FC4	SMI_LARB_SECU_EN	SMI Local Arbiter Master Port Security Enable Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SECU_EN[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SECU_EN[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	SECU_EN	SECU_EN	**Enabling bits for secure transaction of port 0 - 31** Each bit controls a master. MSB controls master 31; LSB controls master 0. 0: Agent transaction is a non-secure transaction. 1: Agent transaction is a secure transaction.

14015FD0	SMI_LARB_DOMN_0	SMI Local Arbiter Master Port Domain Register 0	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DOMN_0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOMN_0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	DOMN_0	DOMN_0	**Domain setting for port 0 - 7** Each 4-bit controls a master, e.g. bit[3:0] controls master 0; bit[7:4]

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Bit(s)	Mnemonic	Name	Description
			controls master 1, etc.

14015FD4 **SMI_LARB_DOMN_1** **SMI Local Arbiter Master Port Domain Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DOMN_1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOMN_1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	DOMN_1	DOMN_1	**Domain setting for port 8 - 15** Each 4-bit controls a master, e.g. bit[3:0] controls master 8; bit[7:4] controls master 9, etc.

14015FD8 **SMI_LARB_DOMN_2** **SMI Local Arbiter Master Port Domain Register 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DOMN_2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOMN_2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	DOMN_2	DOMN_2	**Domain setting for port 16 - 23** Each 4-bit controls a master, e.g. bit[3:0] controls master 16; bit[7:4] controls master 17, etc.

14015FDC **SMI_LARB_DOMN_3** **SMI Local Arbiter Master Port Domain Register 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DOMN_3[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOMN_3[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	DOMN_3	DOMN_3	**Domain setting for port 24 - 31**

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Bit(s)	Mnemonic	Name	Description
			Each 4-bit controls a master, e.g. bit[3:0] controls master 24; bit[7:4] controls master 25, etc.

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6.4 CAM

6.4.1 Introduction

Camera receives RAW and SOC sensor image data after processing of images and outputting YUV data to DRAM.

6.4.2 Features

The camera incorporates a feature-rich image signal processor to connect with a variety of image sensor components. This processor consists of timing generated unit (TG), lens/sensor compensation unit and image process unit.

- Interface
  - Main cam: MIPI 4 lane, 1.5Gbps/lane/parallel interface
  - Sub cam: MIPI 4 lane1.5Gbps/lane /parallel interface
- Raw dump frame rate is 13M@30fps
- Supports video snapshot, which enables user capture image while recording video
- Image processing
  - Bad pix compensation
  - Lens shading compensation
  - Demosaic
  - Color clipping
  - Gamma correction
  - Edge enhancement
  - Noise reduction with large kernel
  - Temporal noise reduction
  - Multi frame blending for lowlight condition
  - Preference color adaptation
- 3A statistics and correction
- Flicker detection
- Electronic image stabilization for video
- Video face beautifier
- Image face Beautifier
- Supports picture in picture/video in video
- High quality resizers

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6.4.3 Register Definition

Module name: CAM Base address: (+15006000h)

Address	Name	Width	Register Function
15004000	CAM_CTL_START	32	**CTL_START** ISP start control
15004004	CAM_CTL_EN_P1	32	**ISP P1 Enable1** ISP sub module pass1 enable1

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Address	Name	Width	Register Function
15004008	CAM_CTL_EN_P1_DMA	32	**ISP P1 DMA Enable1** ISP DMA pass1 enable1
15004010	CAM_CTL_EN_P1_D	32	**ISP Enable1 for 2nd Sensor** ISP sub module enable1
15004014	CAM_CTL_EN_P1_DMA_D	32	**ISP P1 DMA Enable1** ISP DMA pass1 enable1
15004018	CAM_CTL_EN_P2	32	**ISP Enable2** ISP sub module enable2
1500401C	CAM_CTL_EN_P2_DMA	32	**ISP DMA Enable** Enables ISP DMA
15004020	CAM_CTL_CQ_EN	32	**ISP Enable2** ISP sub module enable2
15004024	CAM_CTL_SCENARIO	32	Scenario
15004028	CAM_CTL_FMT_SEL_P1	32	**ISP Format Selection** ISP input/output format
1500402C	CAM_CTL_FMT_SEL_P1_D	32	**ISP Format Selection** ISP input/output format
15004030	CAM_CTL_FMT_SEL_P2	32	IN_FMT
15004034	CAM_CTL_SEL_P1	32	**ISP Selection for P1** ISP input/output format
15004038	CAM_CTL_SEL_P1_D	32	**ISP Selection for P1 D** ISP input/output format
1500403C	CAM_CTL_SEL_P2	32	**ISP Selection** ISP input/output format
15004040	CAM_CTL_SEL_GLOBAL	32	**ISP Selection GLOBAL** CTL_SEL_GLOBAL
15004048	CAM_CTL_INT_P1_EN	32	**ISP Interrupt Enable** Enables ISP interrupt
1500404C	CAM_CTL_INT_P1_STATUS	32	ISP Interrupt Status
15004050	CAM_CTL_INT_P1_EN2	32	**CTL_DMA_INT** CTL_DMA_INT (P1_DMA)
15004054	CAM_CTL_INT_P1_STATUS2	32	**CTL_INT_STATUS2** CTL_INT_STATUS2 (P1_DMA)
15004058	CAM_CTL_INT_P1_EN_D	32	**ISP Interrupt Enable** Enables ISP interrupt (P1_D)
1500405C	CAM_CTL_INT_P1_STATUS_D	32	**ISP Interrupt Status** ISP interrupt status (P1_D)
15004060	CAM_CTL_INT_P1_EN2_D	32	**CTL_DMA_INT** CTL_DMA_INT (P1_D_DMA)
15004064	CAM_CTL_INT_P1_STATUS2_D	32	**CTL_INT_STATUS2** CTL_INT_STATUS2 (P1_D_DMA)
15004068	CAM_CTL_INT_P2_EN	32	**CTL_INT_P2_EN** CTL_INT_P2_EN
1500406C	CAM_CTL_INT_P2_STATUS	32	CTL_INT_P2_STATUS
15004070	CAM_CTL_INT_STATUSX	32	**ISP Interrupt Status** ISP interrupt status (P1 and P2)
15004074	CAM_CTL_INT_STATUS2X	32	**ISP Interrupt Status** ISP interrupt status (P1_D)

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Address	Name	Width	Register Function
15004078	CAM_CTL_INT_STATUS3X	32	**ISP Interrupt Status** ISP interrupt status (all DMA done)
1500407C	CAM_CTL_TPIPE	32	**Control TPIPE Setting** Control TPIPE setting
15004080	CAM_CTL_TDR_EN_STATUS	32	CTL_TDR_EN_STATUS
15004084	CAM_CTL_TCM_EN	32	**TCM Enable** Enables TPIPE configuration map
15004088	CAM_CTL_TDR_DBG_STATUS	32	**CTL_TDR_DBG_STATUS** CTL_TDR_DBG_STATUS
1500408C	CAM_CTL_SW_CTL	32	**CTL_SW_CTL** Controls software reset
15004090	CAM_CTL_SPARE0	32	CTL_SPARE0
15004094	CAM_CTL_SPARE1	32	CTL_SPARE1
1500409C	CAM_CTL_SPARE2	32	CTL_SPARE2
150040A0	CAM_CTL_CQ1_BASEADDR	32	CTL_CQ1_BASEADDR
150040A4	CAM_CTL_CQ2_BASEADDR	32	CTL_CQ2_BASEADDR
150040A8	CAM_CTL_CQ3_BASEADDR	32	CTL_CQ3_BASEADDR
150040AC	CAM_CTL_CQ0_BASEADDR	32	CTL_CQ0_BASEADDR
150040B0	CAM_CTL_CQ0B_BASEADDR	32	CTL_CQ0B_BASEADDR
150040B4	CAM_CTL_CQ0C_BASEADDR	32	CTL_CQ0C_BASEADDR
150040B8	CAM_CTL_CUR_CQ0_BASEADDR	32	CTL_CUR_CQ0_BASEADDR
150040BC	CAM_CTL_CUR_CQ0B_BASEADDR	32	CTL_CUR_CQ0B_BASEADDR
150040C0	CAM_CTL_CUR_CQ0C_BASEADDR	32	CTL_CUR_CQ0C_BASEADDR
150040C4	CAM_CTL_CQ0_D_BASEADDR	32	CTL_CQ0_D_BASEADDR
150040C8	CAM_CTL_CQ0B_D_BASEADDR	32	CTL_CQ0B_D_BASEADDR
150040CC	CAM_CTL_CQ0C_D_BASEADDR	32	CTL_CQ0C_D_BASEADDR
150040D0	CAM_CTL_CUR_CQ0_D_BASEADDR	32	CTL_CUR_CQ0_D_BASEADDR
150040D4	CAM_CTL_CUR_CQ0B_D_BASEADDR	32	CTL_CUR_CQ0B_D_BASEADDR
150040D8	CAM_CTL_CUR_CQ0C_D_BASEADDR	32	CTL_CUR_CQ0C_D_BASEADDR
150040DC	CAM_CTL_DB_LOAD_D	32	DB_LOAD_HOLD_D
150040E0	CAM_CTL_DB_LOAD	32	DB_LOAD_HOLD
150040E4	CAM_CTL_P1_DONE_BYP	32	CTL_P1_DONE_BYP
150040E8	CAM_CTL_P1_DONE_BYP_D	32	CTL_P1_DONE_BYP_D
150040EC	CAM_CTL_P2_DONE_BYP	32	CTL_P1_DONE_BYP

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Address	Name	Width	Register Function
150040F0	CAM_CTL_IMGO_FBC	32	CTL_IMGO_FBC
150040F4	CAM_CTL_RRZO_FBC	32	CTL_RRZO_FBC
150040F8	CAM_CTL_IMGO_D_FBC	32	CTL_IMGO_D_FBC
150040FC	CAM_CTL_RRZO_D_FBC	32	CTL_RRZO_D_FBC
15004100	CAM_CTL_SPARE3	32	CTL_SPARE3
15004104	CAM_CTL_IHDR	32	CTL_IHDR
15004108	CAM_CTL_IHDR_D	32	CTL_IHDR_D
1500410C	CAM_CTL_CQ_EN_P2	32	CTL_CQ_EN_P2
15004110	CAM_CTL_SEL_GLOBAL_P2	32	CTL_SEL_GLOBAL_P2
15004160	CAM_CTL_DBG_SET	32	**CTL_DBG_SET** Selects debugging signal
15004164	CAM_CTL_DBG_PORT	32	CTL_DBG_PORT
15004168	CAM_CTL_IMGI_CHECK	32	CTL_IMGI_CHECK
1500416C	CAM_CTL_IMGO_CHECK	32	CTL_IMGO_CHECK
15004170	CAM_CTL_CLK_EN	32	**CLK_EN** Enables clock
15004180	CAM_CTL_DATE_CODE	32	CTL_DATE_CODE
15004184	CAM_CTL_PROJ_CODE	32	CTL_PROJ_CODE
15004188	CAM_CTL_RAW_DCM_DIS	32	CTL_RAW_DCM_DIS
1500418C	CAM_CTL_RAW_D_DCM_DIS	32	CTL_RAW_D_DCM_DIS
15004190	CAM_CTL_DMA_DCM_DIS	32	CTL_DMA_DCM_DIS
15004194	CAM_CTL_RGB_DCM_DIS	32	CTL_RGB_DCM_DIS
15004198	CAM_CTL_YUV_DCM_DIS	32	CTL_YUV_DCM_DIS
1500419C	CAM_CTL_TOP_DCM_DIS	32	CTL_TOP_DCM_DIS
150041A0	CAM_CTL_RAW_DCM_STATUS	32	CTL_RAW_DCM_STATUS
150041A4	CAM_CTL_RAW_D_DCM_STATUS	32	CTL_RAW_D_DCM_STATUS
150041A8	CAM_CTL_DMA_DCM_STATUS	32	CTL_DMA_DCM_STATUS
150041AC	CAM_CTL_RGB_DCM_STATUS	32	CTL_RGB_DCM_STATUS
150041B0	CAM_CTL_YUV_DCM_STATUS	32	CTL_YUV_DCM_STATUS
150041B4	CAM_CTL_TOP_DCM_STATUS	32	CTL_TOP_DCM_STATUS
150041B8	CAM_CTL_RAW_REQ_STATUS	32	CTL_RAW_REQ_STATUS
150041BC	CAM_CTL_RAW_D_REQ_STATUS	32	CTL_RAW_D_REQ_STATUS

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Address	Name	Width	Register Function
150041C0	CAM_CTL_DMA_REQ_STATUS	32	CTL_DMA_REQ_STATUS
150041C4	CAM_CTL_RGB_REQ_STATUS	32	CTL_RGB_REQ_STATUS
150041C8	CAM_CTL_YUV_REQ_STATUS	32	CTL_YUV_REQ_STATUS
150041CC	CAM_CTL_RAW_RDY_STATUS	32	CTL_RAW_RDY_STATUS
150041D0	CAM_CTL_RAW_D_RDY_STATUS	32	CTL_RAW_D_RDY_STATUS
150041D4	CAM_CTL_DMA_RDY_STATUS	32	CTL_DMA_RDY_STATUS
150041D8	CAM_CTL_RGB_RDY_STATUS	32	CTL_RGB_RDY_STATUS
150041DC	CAM_CTL_YUV_RDY_STATUS	32	CTL_YUV_RDY_STATUS
15004410	CAM_TG_SEN_MODE	32	**Sensor Mode** Configures sensor mode
15004414	CAM_TG_VF_CON	32	**VF Control** Controls view finder mode
15004418	CAM_TG_SEN_GRAB_PXL	32	**Sensor Grab Pixel Start/End** Sensor grab window start/end pixel
1500441C	CAM_TG_SEN_GRAB_LIN	32	**Sensor Grab Line Start/End** Sensor grab window start/end line
15004420	CAM_TG_PATH_CFG	32	**TG Path Config** Configures TG path
15004424	CAM_TG_MEMIN_CTL	32	**MEMIN Control** Memory in control register
15004428	CAM_TG_INT1	32	**TG Interrupt 1** TG Interrupt 1 setting
1500442C	CAM_TG_INT2	32	**TG Interrupt 2** TG Interrupt 2 setting
15004430	CAM_TG_SOF_CNT	32	**TG SOF CNT** TG SOF count
15004434	CAM_TG_SOT_CNT	32	**TG SOT CNT** TG SOT count
15004438	CAM_TG_EOT_CNT	32	**TG EOT CNT** TG EOT count
1500443C	CAM_TG_ERR_CTL	32	**TG Error CTL** TG error control
15004440	CAM_TG_DAT_NO	32	**TG Out Data Num** TG output data number
15004444	CAM_TG_FRM_CNT_ST	32	**TG_FRM_CNT_ST** TG frame count status
15004448	CAM_TG_FRMSIZE_ST	32	**TG FRM SIZE ST** TG frame size status
1500444C	CAM_TG_INTER_ST	32	**TG INTER ST** TG internal status
15004460	CAM_TG_FLASHA_CTL	32	**FLASHA Control** FLASHA control registers
15004464	CAM_TG_FLASHA_LINE_CNT	32	**FLASHA Line Count** FLASHA line count and unit

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Address	Name	Width	Register Function
15004468	CAM_TG_FLASHA_POS	32	**FLASHA POS** FLASHA trigger position
1500446C	CAM_TG_FLASHB_CTL	32	**FLASHB Control** FLASHB control registers
15004470	CAM_TG_FLASHB_LINE_CNT	32	**FLASHB Line Count** FLASHB line count and unit
15004474	CAM_TG_FLASHB_POS	32	**FLASHB POS** FLASHB trigger position
15004478	CAM_TG_FLASHB_POS1	32	**FLASHB POS1** FLASHB trigger position 1
150044F0	CAM_HBN_SIZE	32	**HBN_SIZE** HBN input H and V size
150044F4	CAM_HBN_MODE	32	**HBN_MODE** Binning mode
15004500	CAM_OBC_OFFST0	32	**OBC Offset 0** Optical black correction offset 0 register
15004504	CAM_OBC_OFFST1	32	**OBC Offset 1** Optical black correction offset 1 register
15004508	CAM_OBC_OFFST2	32	**OBC Offset 2** Optical black correction offset 2 register
1500450C	CAM_OBC_OFFST3	32	**OBC Offset 3** Optical black correction offset 3 register
15004510	CAM_OBC_GAIN0	32	**OBC Gain 0** Optical black correction gain 0 register
15004514	CAM_OBC_GAIN1	32	**OBC Gain 1** Optical black correction gain 1 register
15004518	CAM_OBC_GAIN2	32	**OBC Gain 2** Optical black correction gain 2 register
1500451C	CAM_OBC_GAIN3	32	**OBC Gain 3** Optical black correction gain 3 register
15004530	CAM_LSC_CTL1	32	Shading Control 2 Register
15004534	CAM_LSC_CTL2	32	Shading Control 2 Register
15004538	CAM_LSC_CTL3	32	**LSC Spare Register** LSC spare register
1500453C	CAM_LSC_LBLOCK	32	**Shading Last Block Config Register** Shading last block configuration register
15004540	CAM_LSC_RATIO	32	**Shading Ratio Config Register** Shading ratio configuration register
15004544	CAM_LSC_TPIPE_OFST	32	**Shading TPIPE Offset Register** Shading TPIPE offset register
15004548	CAM_LSC_TPIPE_SIZE	32	**Shading TPIPE Size Register** Shading TPIPE size register
1500454C	CAM_LSC_GAIN_TH	32	**Shading Gain Threshold Register** Shading gain threshold register
15004550	CAM_RPG_SATU_1	32	**RPG_SATU_1** Maximum saturation value
15004554	CAM_RPG_SATU_2	32	**RPG_SATU_2** Maximum saturation value
15004558	CAM_RPG_GAIN_1	32	**RPG_GAIN_1** Gain control
1500455C	CAM_RPG_GAIN_2	32	**RPG_GAIN_2**

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Address	Name	Width	Register Function
			Gain control
15004560	CAM_RPG_OFST_1	32	**RPG_OFST_1** Offset
15004564	CAM_RPG_OFST_2	32	**RPG_OFST_2** Offset
15004580	CAM_SGG2_PGN	32	**SGG PGN** SGG gain control
15004584	CAM_SGG2_GMRC_1	32	**SGG GMRC 1** SGG gamma control 1
15004588	CAM_SGG2_GMRC_2	32	**SGG GMRC 2** SGG gamma control 2
150045B0	CAM_AWB_WIN_ORG	32	AWB Window Origin
150045B4	CAM_AWB_WIN_SIZE	32	AWB Window Size
150045B8	CAM_AWB_WIN_PIT	32	AWB Window Pitch
150045BC	CAM_AWB_WIN_NUM	32	AWB Window Number
150045C0	CAM_AWB_GAIN1_0	32	AWB Raw PreGain1 R/G
150045C4	CAM_AWB_GAIN1_1	32	AWB Raw PreGain1 B
150045C8	CAM_AWB_LMT1_0	32	AWB Raw Limit1 R/G
150045CC	CAM_AWB_LMT1_1	32	AWB Raw Limit1 B
150045D0	CAM_AWB_LOW_THR	32	AWB Low Threshold
150045D4	CAM_AWB_HI_THR	32	AWB High Threshold
150045D8	CAM_AWB_PIXEL_CNT0	32	AWB Pixel CNT 0
150045DC	CAM_AWB_PIXEL_CNT1	32	AWB Pixel CNT 1
150045E0	CAM_AWB_PIXEL_CNT2	32	AWB Pixel CNT 2
150045E4	CAM_AWB_ERR_THR	32	AWB Error Threshold
150045E8	CAM_AWB_ROT	32	AWB Rotation Parameter
150045EC	CAM_AWB_L0_X	32	AWB Light0 x Region
150045F0	CAM_AWB_L0_Y	32	AWB Light0 y Region
150045F4	CAM_AWB_L1_X	32	AWB Light1 x Region
150045F8	CAM_AWB_L1_Y	32	AWB Light1 y Region
150045FC	CAM_AWB_L2_X	32	AWB Light2 x Region
15004600	CAM_AWB_L2_Y	32	AWB Light2 y Region
15004604	CAM_AWB_L3_X	32	AWB Light3 x Region
15004608	CAM_AWB_L3_Y	32	AWB Light3 y Region
1500460C	CAM_AWB_L4_X	32	AWB Light4 x Region
15004610	CAM_AWB_L4_Y	32	AWB Light4 y Region
15004614	CAM_AWB_L5_X	32	AWB Light5 x Region
15004618	CAM_AWB_L5_Y	32	AWB Light5 y Region
1500461C	CAM_AWB_L6_X	32	AWB Light6 x Region
15004620	CAM_AWB_L6_Y	32	AWB Light6 y Region
15004624	CAM_AWB_L7_X	32	AWB Light7 x Region
15004628	CAM_AWB_L7_Y	32	AWB Light7 y Region
1500462C	CAM_AWB_L8_X	32	AWB Light8 x Region
15004630	CAM_AWB_L8_Y	32	AWB Light8 y Region
15004634	CAM_AWB_L9_X	32	AWB Light9 x Region

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Address	Name	Width	Register Function
15004638	CAM_AWB_L9_Y	32	AWB Light9 y Region
1500463C	CAM_AWB_SPARE	32	AWB Spare Register
15004650	CAM_AE_HST_CTL	32	AE Histogram Control
15004654	CAM_AE_GAIN2_0	32	AE Raw PreGain2 R/G
15004658	CAM_AE_GAIN2_1	32	AE Raw PreGain2 B
1500465C	CAM_AE_LMT2_0	32	AE Raw Limit2 R/G
15004660	CAM_AE_LMT2_1	32	AE Raw Limit2 B
15004664	CAM_AE_RC_CNV_0	32	AE Matrix Coeff 0
15004668	CAM_AE_RC_CNV_1	32	AE Matrix Coeff 1
1500466C	CAM_AE_RC_CNV_2	32	AE Matrix Coeff 2
15004670	CAM_AE_RC_CNV_3	32	AE Matrix Coeff 3
15004674	CAM_AE_RC_CNV_4	32	AE Matrix Coeff 4
15004678	CAM_AE_YGAMMA_0	32	AE YGAMMA Set 0
1500467C	CAM_AE_YGAMMA_1	32	AE YGAMMA Set 1
15004680	CAM_AE_HST_SET	32	AE Histogram Setting
15004684	CAM_AE_HST0_RNG	32	AE Histogram 0 Range
15004688	CAM_AE_HST1_RNG	32	AE Histogram 1 Range
1500468C	CAM_AE_HST2_RNG	32	AE Histogram 2 Range
15004690	CAM_AE_HST3_RNG	32	AE Histogram 3 Range
15004694	CAM_AE_SPARE	32	AE Spare Register
150046A0	CAM_SGG1_PGN	32	**SGG PGN** SGG gain control
150046A4	CAM_SGG1_GMRC_1	32	**SGG GMRC 1** SGG gamma control 1
150046A8	CAM_SGG1_GMRC_2	32	**SGG GMRC 2** SGG gamma control 2
150046B0	CAM_AF_CON	32	AF Control
150046B4	CAM_AF_WINX_1	32	AF Window X 0&1
150046B8	CAM_AF_WINX_2	32	AF Window X 2&3
150046BC	CAM_AF_WINX_3	32	AF Window X 4&5
150046C0	CAM_AF_WINY_1	32	AF Window Y 0&1
150046C4	CAM_AF_WINY_2	32	AF Window Y 2&3
150046C8	CAM_AF_WINY_3	32	AF Window Y 4&5
150046CC	CAM_AF_SIZE	32	AF Window Size
150046D4	CAM_AF_FLT_1	32	AF Filter P1~P4
150046D8	CAM_AF_FLT_2	32	AF Filter P5~P8
150046DC	CAM_AF_FLT_3	32	AF Filter P9~P12
150046E0	CAM_AF_TH	32	AF Filter Threshold
150046E4	CAM_AF_FLO_WIN_1	32	AF Floating Window 1 X&Y
150046E8	CAM_AF_FLO_SIZE_1	32	AF Floating Window 1 Size
150046EC	CAM_AF_FLO_WIN_2	32	AF Floating Window 2 X&Y
150046F0	CAM_AF_FLO_SIZE_2	32	AF Floating Window 2 Size
150046F4	CAM_AF_FLO_WIN_3	32	AF Floating Window 3 X&Y
150046F8	CAM_AF_FLO_SIZE_3	32	AF Floating Window 3 Size
150046FC	CAM_AF_FLO_TH	32	AF Floating Window Filter Threshold
15004700	CAM_AF_IMAGE_SIZE	32	AF Input Image Size

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Address	Name	Width	Register Function
15004704	CAM_AF_FLT_4	32	AF Vertical Filter X0~X1
15004708	CAM_AF_FLT_5	32	AF Vertical Filter X2~X3
1500470C	CAM_AF_STAT_L	32	AF Target Window Statistics Output (LSB)
15004710	CAM_AF_STAT_M	32	AF Target Window Statistics Output (MSB)
15004714	CAM_AF_FLO_STAT_1L	32	AF Floating Window 1 Statistics Output (LSB)
15004718	CAM_AF_FLO_STAT_1M	32	AF Floating Window 1 Statistics Output (MSB)
1500471C	CAM_AF_FLO_STAT_1V	32	AF Floating Window 1 Statistics Output (VER)
15004720	CAM_AF_FLO_STAT_2L	32	AF Floating Window 2 Statistics Output (LSB)
15004724	CAM_AF_FLO_STAT_2M	32	AF Floating Window 2 Statistics Output (MSB)
15004728	CAM_AF_FLO_STAT_2V	32	AF Floating Window 2 Statistics Output (VER)
1500472C	CAM_AF_FLO_STAT_3L	32	AF Floating Window 3 Statistics Output (LSB)
15004730	CAM_AF_FLO_STAT_3M	32	AF Floating Window 3 Statistics Output (MSB)
15004734	CAM_AF_FLO_STAT_3V	32	AF Floating Window 3 Statistics Output (VER)
15004760	CAM_WBN_SIZE	32	**WBN_SIZE** BIN input H and V size
15004764	CAM_WBN_MODE	32	**WBN_MODE** Binning mode
15004770	CAM_FLK_CON	32	FLK Control
15004774	CAM_FLK_OFST	32	FLK Start Offset
15004778	CAM_FLK_SIZE	32	FLK Window Size
1500477C	CAM_FLK_NUM	32	FLK Window Number
15004780	CAM_LCS_CON	32	LCS Control Register
15004784	CAM_LCS_ST	32	LCS Start Point
15004788	CAM_LCS_AWS	32	LCS Active Window Size
1500478C	CAM_LCS_FLR	32	LCS Flare
15004790	CAM_LCS_LRZR_1	32	LCS Horizontal Down-sampling Ratio
15004794	CAM_LCS_LRZR_2	32	LCS Vertical Down-sampling Ratio
150047A0	CAM_RRZ_CTL	32	**RRZ CTL** RRZ control register
150047A4	CAM_RRZ_IN_IMG	32	**RRZ IN IMG** RRZ input image size register
150047A8	CAM_RRZ_OUT_IMG	32	**RRZ OUT IMG** RRZ output image size register
150047AC	CAM_RRZ_HORI_STEP	32	**RRZ_HORI_STEP** RRZ horizontal coefficient step
150047B0	CAM_RRZ_VERT_STEP	32	**RRZ_VERT_STEP** RRZ vertical coefficient sStep
150047B4	CAM_RRZ_HORI_INT_OFST	32	**RRZ_HORI_INT_OFST** RRZ horizontal integer offset
150047B8	CAM_RRZ_HORI_SUB_OFST	32	**RRZ_HORI_SUB_OFST** RRZ horizontal sub-pixel offset
150047BC	CAM_RRZ_VERT_INT	32	**RRZ_VERT_INT_OFST**

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Address	Name	Width	Register Function
	_OFST		RRZ vertical integer offset
150047C0	CAM_RRZ_VERT_SUB_OFST	32	**RRZ_VERT_SUB_OFST** RRZ vertical sub-pixel offset
150047C4	CAM_RRZ_MODE_TH	32	RRZ_TH_MD
150047C8	CAM_RRZ_MODE_CTL	32	RRZ_TBL_SEL_SP
15004800	CAM_BPC_CON	32	2D BPC Control Register
15004804	CAM_BPC_TH1	32	BPC Detection Condition 1 Register 1
15004808	CAM_BPC_TH2	32	BPC Detection Condition 1 Register 2
1500480C	CAM_BPC_TH3	32	BPC Detection Condition 1 Register 3
15004810	CAM_BPC_TH4	32	BPC Detection Condition 1 Register 3
15004814	CAM_BPC_DTC	32	BPC Detection Condition 1/2/3 Register
15004818	CAM_BPC_COR	32	BPC Correction Register
1500481C	CAM_BPC_TBLI1	32	BPC Table Input Information Register 1
15004820	CAM_BPC_TBLI2	32	BPC Table Input Information Register 2
15004824	CAM_BPC_TH1_C	32	BPC Detection Extension Condition 1 Register 1
15004828	CAM_BPC_TH2_C	32	BPC Detection Extension Condition 1 Register 2
1500482C	CAM_BPC_TH3_C	32	BPC Detection Extension Condition 1 Register 3
15004850	CAM_NR1_CON	32	NR1 Control Register
15004854	CAM_NR1_CT_CON	32	NR1 Crosstalk Compensation Configuration Register
15004858	CAM_BNR_RSV1	32	BNR RSV1
1500485C	CAM_BNR_RSV2	32	BNR RSV2
15004880	CAM_PGN_SATU_1	32	PGN_SATU_1
15004884	CAM_PGN_SATU_2	32	PGN_SATU_2
15004888	CAM_PGN_GAIN_1	32	PGN_GAIN_1
1500488C	CAM_PGN_GAIN_2	32	PGN_GAIN_2
15004890	CAM_PGN_OFST_1	32	PGN_OFST_1
15004894	CAM_PGN_OFST_2	32	PGN_OFST_2
150048A0	CAM_DM_O_BYP	32	DM_O_BYP
150048A4	CAM_DM_O_ED_FLAT	32	**DM_O_ED_FLAT** Edge detection register for flat decision
150048A8	CAM_DM_O_ED_NYQ	32	**DM_O_ED_NYQ** Edge detection register for Nyquist decision
150048AC	CAM_DM_O_ED_STEP	32	**DM_O_ED_STEP** Edge detection register for step decision
150048B0	CAM_DM_O_RGB_HF	32	**DM_O_RGB_HF** Register for RGB, HF and active
150048B4	CAM_DM_O_DOT	32	**DM_O_DOT** Black dot, white dot and baseband threshold
150048B8	CAM_DM_O_F1_ACT	32	**DM_O_F1_ACT** Register for F1 ACT modulation
150048BC	CAM_DM_O_F2_ACT	32	**DM_O_F2_ACT** Register for F2 ACT modulation
150048C0	CAM_DM_O_F3_ACT	32	**DM_O_F3_ACT** Register for F3 ACT modulation
150048C4	CAM_DM_O_F4_ACT	32	**DM_O_F4_ACT** Register for F4 ACT modulation
150048C8	CAM_DM_O_F1_L	32	**DM_O_F1_L** Register for F1 Luma modulation

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Address	Name	Width	Register Function
150048CC	CAM_DM_O_F2_L	32	**DM_O_F2_L** Register for F2 Luma modulation
150048D0	CAM_DM_O_F3_L	32	**DM_O_F3_L** Register for F3 Luma modulation
150048D4	CAM_DM_O_F4_L	32	**DM_O_F4_L** Registers for F4 Luma modulation
150048D8	CAM_DM_O_HF_RB	32	**DM_O_HF_RB** Register for HF_Clip and RB_Diff
150048DC	CAM_DM_O_HF_GAIN	32	**DM_O_HF_GAIN** HFC global gain register
150048E0	CAM_DM_O_HF_COMP	32	**DM_O_HF_COMP** HFC compensation register
150048E4	CAM_DM_O_HF_CORIN_TH	32	**DM_O_HF_CORIN_TH** HF coring threshold
150048E8	CAM_DM_O_ACT_LUT	32	**DM_O_ACT_LUT** Activity non-linear modulation table
150048F0	CAM_DM_O_SPARE	32	**DM_O_SPARE** CFA spare register
150048F4	CAM_DM_O_BB	32	**DM_O_BB** Black dot, white dot and baseband threshold
15004910	CAM_CCL_GTC	32	CCL Global Threshold Configuration
15004914	CAM_CCL_ADC	32	CCL Anti De-saturation Configuration
15004918	CAM_CCL_BAC	32	CCL Blue Adjustment Configuration
15004920	CAM_G2G_CNV_1	32	G2G Matrix Coefficient
15004924	CAM_G2G_CNV_2	32	G2G Matrix Coefficient
15004928	CAM_G2G_CNV_3	32	G2G Matrix Coefficient
1500492C	CAM_G2G_CNV_4	32	G2G Matrix Coefficient
15004930	CAM_G2G_CNV_5	32	G2G Matrix Coefficient
15004934	CAM_G2G_CNV_6	32	G2G Matrix Coefficient
15004938	CAM_G2G_CTRL	32	G2G Control
15004948	CAM_UNP_OFST	32	**UNP Bit Offset** Unpacks 10-bit mode offset
15004950	CAM_C02_CON	32	C02 Control Register
15004954	CAM_C02_CROP_CON_1	32	C02 Crop X Control
15004958	CAM_C02_CROP_CON_2	32	C02 Crop Y Control
15004960	CAM_MFB_CON	32	**MFB Control** MFB control registers
15004964	CAM_MFB_LL_CON1	32	**MFB LL Control 1** MFB LL control registers
15004968	CAM_MFB_LL_CON2	32	**MFB LL Control 2** MFB LL control registers
1500496C	CAM_MFB_LL_CON3	32	**MFB LL Control 3** MFB LL control registers
15004970	CAM_MFB_LL_CON4	32	**MFB LL Control 4** MFB LL control registers
15004974	CAM_MFB_LL_CON5	32	**MFB LL Control 5** MFB LL control registers
15004978	CAM_MFB_LL_CON6	32	**MFB LL Control 6**

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Address	Name	Width	Register Function
			MFB LL control registers
150049C0	CAM_LCE_CON	32	LCE Control Register
150049C4	CAM_LCE_ZR	32	LCE Zoom Ratio
150049C8	CAM_LCE_QUA	32	LCE Quality Register
150049CC	CAM_LCE_DGC_1	32	LCE Degamma Control 1
150049D0	CAM_LCE_DGC_2	32	LCE Degamma Control 2
150049D4	CAM_LCE_GM	32	LCE Gain Modification
150049E0	CAM_LCE_SLM_LB	32	LCE SLM Lower Bound
150049E4	CAM_LCE_SLM_SIZE	32	LCE SLM Size
150049E8	CAM_LCE_OFST	32	LCE Offset
150049EC	CAM_LCE_BIAS	32	LCE Bias
150049F0	CAM_LCE_IMAGE_SIZE	32	LCE Image Size
15004A00	CAM_CPG_SATU_1	32	CPG_SATU_1
15004A04	CAM_CPG_SATU_2	32	CPG_SATU_2
15004A08	CAM_CPG_GAIN_1	32	CPG_GAIN_1
15004A0C	CAM_CPG_GAIN_2	32	CPG_GAIN_2
15004A10	CAM_CPG_OFST_1	32	CPG_OFST_1
15004A14	CAM_CPG_OFST_2	32	CPG_OFST_2
15004A1C	CAM_C42_CON	32	YUV444 to YUV422 Control Register
15004A20	CAM_ANR_CON1	32	ANR Control Register 1
15004A24	CAM_ANR_CON2	32	ANR Control Register 2
15004A28	CAM_ANR_CON3	32	ANR Control Register 3
15004A2C	CAM_ANR_YAD1	32	ANR Luma NR Strength Adaption Register 1
15004A30	CAM_ANR_YAD2	32	ANR Luma NR Strength Adaption Register 2
15004A34	CAM_ANR_4LUT1	32	ANR Slope4 LUT Register 1
15004A38	CAM_ANR_4LUT2	32	ANR Slope4 LUT Register 2
15004A3C	CAM_ANR_4LUT3	32	ANR Slope4 LUT Register 3
15004A40	CAM_ANR_PTY	32	ANR Luma Range Filter LUT Register
15004A44	CAM_ANR_CAD	32	ANR Chroma NR Strength Adaption Register
15004A48	CAM_ANR_PTC	32	ANR Chroma Range Filter LUT Register
15004A4C	CAM_ANR_LCE1	32	ANR LEC Gain Register 1
15004A50	CAM_ANR_LCE2	32	ANR LEC Gain Register 2
15004A54	CAM_ANR_HP1	32	**ANR HP Register 1** ANR High Pass Filter Register 1
15004A58	CAM_ANR_HP2	32	**ANR HP Register 2** ANR High Pass Filter Register 2
15004A5C	CAM_ANR_HP3	32	**ANR HP Register 3** ANR High Pass Filter Register 3
15004A60	CAM_ANR_ACTY	32	ANR Activity Luma Register
15004A64	CAM_ANR_ACTC	32	ANR Activity Chroma Register
15004A68	CAM_ANR_RSV1	32	ANR_RSV1
15004A6C	CAM_ANR_RSV2	32	ANR_RSV2
15004A80	CAM_CCR_CON	32	Chroma Choring Control Register
15004A84	CAM_CCR_YLUT	32	Chroma Choring Luma LUT Register
15004A88	CAM_CCR_UVLUT	32	Chroma Choring Chroma LUT Register
15004A8C	CAM_CCR_YLUT2	32	Chroma Choring Luma LUT 2 Register

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Address	Name	Width	Register Function
15004A90	CAM_CCR_SAT_CTRL	32	Chroma Choring Saturation Control Register
15004A94	CAM_CCR_UVLUT_SP	32	Chroma Choring Chroma LUT Slope Register
15004AA0	CAM_SEEE_SRK_CTRL	32	**Shrinkage Control** Controls whether shrinkage function is enabled or not
15004AA4	CAM_SEEE_CLIP_CTRL	32	**Clip Control** Controls clipping function
15004AA8	CAM_SEEE_FLT_CTRL_1	32	**Filter Control 1** Controls the result of filter
15004AAC	CAM_SEEE_FLT_CTRL_2	32	**Filter Control 2** Controls the parameters of filter
15004AB0	CAM_SEEE_GLUT_CTRL_01	32	**Edge Detection Filter Control 01** Controls gain lookup table
15004AB4	CAM_SEEE_GLUT_CTRL_02	32	**Edge Detection Filter Control 02** Controls gain lookup table
15004AB8	CAM_SEEE_GLUT_CTRL_03	32	**Edge Detection Filter Control 03** Controls gain lookup table
15004ABC	CAM_SEEE_GLUT_CTRL_04	32	**Edge Detection Filter Control 04** Controls gain lookup table
15004AC0	CAM_SEEE_GLUT_CTRL_05	32	**Edge Detection Filter Control 05** Controls gain lookup table
15004AC4	CAM_SEEE_GLUT_CTRL_06	32	**Edge Detection Filter Control 06** Controls gain lookup table
15004AC8	CAM_SEEE_EDTR_CTRL	32	**Edge Detection Control** Controls edge detection filter
15004ACC	CAM_SEEE_OUT_EDGE_CTRL	32	**Target of Edge Enhancement** Controls output target of edge enhancement
15004AD0	CAM_SEEE_SE_Y_CTRL	32	**Special Effect Y Control** Controls Y value of special effect
15004AD4	CAM_SEEE_SE_EDGE_CTRL_1	32	**Special Effect Edge Control 1** Controls edge detection of special effect
15004AD8	CAM_SEEE_SE_EDGE_CTRL_2	32	**Special Effect Edge Control 2** Controls edge detection of special effect
15004ADC	CAM_SEEE_SE_EDGE_CTRL_3	32	**Special Effect Edge Control 3** Controls edge detection of special effect
15004AE0	CAM_SEEE_SE_SPECL_CTRL	32	**Special Effect Special Control** Controls final output of special effect
15004AE4	CAM_SEEE_SE_CORE_CTRL_1	32	**Special Effect Core Control 1** Controls CORE function of special effect
15004AE8	CAM_SEEE_SE_CORE_CTRL_2	32	**Special Effect Core Control 2** Controls CORE function of special effect
15004AEC	CAM_SEEE_GLUT_CTRL_07	32	**Edge Detection Filter Control 07** Controls gain lookup table
15004AF0	CAM_SEEE_GLUT_CTRL_08	32	**Edge Detection Filter Control 08** Controls gain lookup table
15004AF4	CAM_SEEE_GLUT_CTRL_09	32	**Edge Detection Filter Control 09** Controls gain lookup table
15004AF8	CAM_SEEE_GLUT_CTRL_10	32	**Edge Detection Filter Control 10** Controls gain lookup table
15004AFC	CAM_SEEE_GLUT_CTRL_11	32	**Edge Detection Filter Control 11** Controls gain lookup table
15004B00	CAM_CRZ_CONTROL	32	**CRZ Control**

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Address	Name	Width	Register Function
			CRZ control register
15004B04	CAM_CRZ_IN_IMG	32	**CRZ IN IMG** CRZ input image size register
15004B08	CAM_CRZ_OUT_IMG	32	**CRZ OUT IMG** CRZ output image size register
15004B0C	CAM_CRZ_HORI_STEP	32	**CRZ_HORI_STEP** CRZ horizontal coefficient step
15004B10	CAM_CRZ_VERT_STEP	32	**CRZ_VERT_STEP** CRZ vertical coefficient step
15004B14	CAM_CRZ_LUMA_HORI_INT_OFST	32	**CRZ_LUMA_HORI_INT_OFST** CRZ horizontal integer offset
15004B18	CAM_CRZ_LUMA_HORI_SUB_OFST	32	**CRZ_LUMA_HORI_SUB_OFST** CRZ horizontal sub-pixel offset
15004B1C	CAM_CRZ_LUMA_VERT_INT_OFST	32	**CRZ_LUMA_VERT_INT_OFST** CRZ vertical integer offset
15004B20	CAM_CRZ_LUMA_VERT_SUB_OFST	32	**CRZ_LUMA_VERT_SUB_OFST** CRZ vertical sub-pixel offset
15004B24	CAM_CRZ_CHRO_HORI_INT_OFST	32	**CRZ_CHRO_HORI_INT_OFST** CRZ horizontal integer offset
15004B28	CAM_CRZ_CHRO_HORI_SUB_OFST	32	**CRZ_CHRO_HORI_SUB_OFST** CRZ horizontal sub-pixel offset
15004B2C	CAM_CRZ_CHRO_VERT_INT_OFST	32	**CRZ_CHRO_VERT_INT_OFST** CRZ vertical integer offset
15004B30	CAM_CRZ_CHRO_VERT_SUB_OFST	32	**CRZ_CHRO_VERT_SUB_OFST** CRZ vertical sub-pixel offset
15004B34	CAM_CRZ_DER_1	32	**CRZ_DER_1** CRZ spare register 1
15004B38	CAM_CRZ_DER_2	32	**CRZ_DER_2** CRZ spare register 2
15004BA0	CAM_G2C_CONV_0A	32	RGB/YUV to YUV Matrix Coefficient Row 0 (Part A)
15004BA4	CAM_G2C_CONV_0B	32	RGB/YUV to YUV Matrix Coefficient Row 0 (Part B)
15004BA8	CAM_G2C_CONV_1A	32	RGB/YUV to YUV Matrix Coefficient Row 1 (Part A)
15004BAC	CAM_G2C_CONV_1B	32	RGB/YUV to YUV Matrix Coefficient Row 1 (Part B)
15004BB0	CAM_G2C_CONV_2A	32	RGB/YUV to YUV Matrix Coefficient Row 2 (Part A)
15004BB4	CAM_G2C_CONV_2B	32	RGB/YUV to YUV Matrix Coefficient Row 2 (Part B)
15004BB8	CAM_G2C_SHADE_CON_1	32	SHADE Con Part 1
15004BBC	CAM_G2C_SHADE_CON_2	32	SHADE Con Part 2
15004BC0	CAM_G2C_SHADE_CON_3	32	SHADE Con Part 3
15004BC4	CAM_G2C_SHADE_TAR	32	SHADE Position
15004BC8	CAM_G2C_SHADE_SP	32	OFF
15004C30	CAM_SRZ1_CONTROL	32	**SRZ1 Control** SRZ1 control register
15004C34	CAM_SRZ1_IN_IMG	32	**SRZ1 IN IMG** SRZ1 input image size register
15004C38	CAM_SRZ1_OUT_IMG	32	**SRZ1 OUT IMG** SRZ1 output image size register
15004C3C	CAM_SRZ1_HORI_STE	32	**SRZ1_HORI_STEP**

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Address	Name	Width	Register Function
	P		SRZ1 horizontal coefficient step
15004C40	CAM_SRZ1_VERT_STEP	32	**SRZ1_VERT_STEP** SRZ1 vertical coefficient step
15004C44	CAM_SRZ1_HORI_INT_OFST	32	**SRZ1_HORI_INT_OFST** SRZ1 horizontal integer offset
15004C48	CAM_SRZ1_HORI_SUB_OFST	32	**SRZ1_HORI_SUB_OFST** SRZ1 horizontal sub-pixel offset
15004C4C	CAM_SRZ1_VERT_INT_OFST	32	**SRZ1_VERT_INT_OFST** SRZ1 vertical integer offset
15004C50	CAM_SRZ1_VERT_SUB_OFST	32	**SRZ1_VERT_SUB_OFST** SRZ1 vertical sub-pixel offset
15004C60	CAM_SRZ2_CONTROL	32	**SRZ2 Control** SRZ2 control register
15004C64	CAM_SRZ2_IN_IMG	32	**SRZ2 IN IMG** SRZ2 input image size register
15004C68	CAM_SRZ2_OUT_IMG	32	**SRZ2 OUT IMG** SRZ2 output image size register
15004C6C	CAM_SRZ2_HORI_STEP	32	**SRZ2_HORI_STEP** SRZ2 horizontal coefficient step
15004C70	CAM_SRZ2_VERT_STEP	32	**SRZ2_VERT_STEP** SRZ2 vertical coefficient step
15004C74	CAM_SRZ2_HORI_INT_OFST	32	**SRZ2_HORI_INT_OFST** SRZ2 horizontal integer offset
15004C78	CAM_SRZ2_HORI_SUB_OFST	32	**SRZ2_HORI_SUB_OFST** SRZ2 horizontal sub-pixel offset
15004C7C	CAM_SRZ2_VERT_INT_OFST	32	**SRZ2_VERT_INT_OFST** SRZ2 vertical integer offset
15004C80	CAM_SRZ2_VERT_SUB_OFST	32	**SRZ2_VERT_SUB_OFST** SRZ2 vertical sub-pixel offset
15004C90	CAM_MIX1_CTRL_0	32	MIX1 Control Register 0
15004C94	CAM_MIX1_CTRL_1	32	MIX1 Control Register 1
15004C98	CAM_MIX1_SPARE	32	MIX1 Spare Register
15004CA0	CAM_MIX2_CTRL_0	32	MIX2 Control Register 0
15004CA4	CAM_MIX2_CTRL_1	32	MIX2 Control Register 1
15004CA8	CAM_MIX2_SPARE	32	MIX2 Spare Register
15004CB0	CAM_MIX3_CTRL_0	32	MIX3 Control Register 0
15004CB4	CAM_MIX3_CTRL_1	32	MIX3 Control Register 1
15004CB8	CAM_MIX3_SPARE	32	MIX3 Spare Register
15004CC0	CAM_NR3D_BLEND	32	3D NR Blending Register
15004CC4	CAM_NR3D_FBCNT_OFF	32	**3D NR FBCNT Offset Register** 3D NR FB_COUNT offset Register
15004CC8	CAM_NR3D_FBCNT_SIZ	32	**3D NR FBCNT Size Register** 3D NR FB_COUNT size Register
15004CCC	CAM_NR3D_FB_COUNT	32	3D NR FB COUNT Register
15004CD0	CAM_NR3D_LMT_CPX	32	3D NR LIMIT CPX Register
15004CD4	CAM_NR3D_LMT_Y_CON1	32	3D NR LIMIT Y Control Register 1
15004CD8	CAM_NR3D_LMT_Y_CON2	32	3D NR LIMIT Y Control Register 2

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Address	Name	Width	Register Function
15004CDC	CAM_NR3D_LMT_Y_CON3	32	3D NR LIMIT Y Control Register 3
15004CE0	CAM_NR3D_LMT_U_CON1	32	3D NR LIMIT U Control Register 1
15004CE4	CAM_NR3D_LMT_U_CON2	32	3D NR LIMIT U Control Register 2
15004CE8	CAM_NR3D_LMT_U_CON3	32	3D NR LIMIT U Control Register 3
15004CEC	CAM_NR3D_LMT_V_CON1	32	3D NR LIMIT V Control Register 1
15004CF0	CAM_NR3D_LMT_V_CON2	32	3D NR LIMIT V Control Register 2
15004CF4	CAM_NR3D_LMT_V_CON3	32	3D NR LIMIT V Control Register 3
15004CF8	CAM_NR3D_CTRL	32	3D NR Control Register
15004CFC	CAM_NR3D_ON_OFF	32	3D NR On Offset Register
15004D00	CAM_NR3D_ON_SIZ	32	3D NR On Size Register
15004D04	CAM_NR3D_SPARE0	32	3D NR Spare Register
15004D10	CAM_MDP_CROP_X	32	**MDP_CROP_X** MDP_CROP horizontal direction
15004D20	CAM_MDP_CROP_Y	32	**MDP_CROP_Y** MDP_CROP vertical direction
15004DC0	CAM_EIS_PREP_ME_CTRL1	32	EIS Preprocessor and ME Engine Control 1
15004DC4	CAM_EIS_PREP_ME_CTRL2	32	EIS Preprocessor and ME Engine Control 2
15004DC8	CAM_EIS_LMV_TH	32	EIS LMV Thresholds
15004DCC	CAM_EIS_FL_OFFSET	32	EIS Search Window Offset in Floating Mode
15004DE0	CAM_EIS_MB_OFFSET	32	EIS Macro Block Offset
15004DE4	CAM_EIS_MB_INTERVAL	32	EIS Macro Block Interval
15004DE8	CAM_EIS_GMV	32	EIS Global Motion Vector
15004DEC	CAM_EIS_ERR_CTRL	32	EIS Error Control Register
15004DF0	CAM_EIS_IMAGE_CTRL	32	EIS Image Control Register
15004E00	CAM_DMX_CTL	32	**DMX_CTL** Controls DMX
15004E04	CAM_DMX_CROP	32	**DMX_CROP** DMX crop for datapath
15004E08	CAM_DMX_VSIZE	32	**DMX_VSIZE** DMX vertical size
15004E10	CAM_BMX_CTL	32	**BMX_CTL** Controls BMX
15004E14	CAM_BMX_CROP	32	**BMX_CROP** BMX crop for datapath
15004E18	CAM_BMX_VSIZE	32	**BMX_VSIZE** BMX vertical size
15004E20	CAM_RMX_CTL	32	**RMX_CTL** Controls RMX
15004E24	CAM_RMX_CROP	32	**RMX_CROP** RMX crop for datapath
15004E28	CAM_RMX_VSIZE	32	**RMX_VSIZE**

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Address	Name	Width	Register Function
			RMX vertical size
15004F40	CAM_SL2_CEN	32	SL2 Circular Center Register
15004F44	CAM_SL2_MAX0_RR	32	SL2 MAX0 Radius Register
15004F48	CAM_SL2_MAX1_RR	32	SL2 MAX1 Radius Register
15004F4C	CAM_SL2_MAX2_RR	32	SL2 MAX2 Radius Register
15004F50	CAM_SL2_HRZ	32	SL2 HRZ Compensation Register
15004F54	CAM_SL2_XOFF	32	SL2 Horizontal Offset Register
15004F58	CAM_SL2_YOFF	32	SL2 Vertical Offset Register
15004F60	CAM_SL2B_CEN	32	SL2B Circular Center Register
15004F64	CAM_SL2B_MAX0_RR	32	SL2B MAX0 Radius Register
15004F68	CAM_SL2B_MAX1_RR	32	SL2B MAX1 Radius Register
15004F6C	CAM_SL2B_MAX2_RR	32	SL2B MAX2 Radius Register
15004F70	CAM_SL2B_HRZ	32	SL2B HRZ Compensation Register
15004F74	CAM_SL2B_XOFF	32	SL2B Horizontal Offset Register
15004F78	CAM_SL2B_YOFF	32	SL2B Vertical Offset Register
15004FA0	CAM_CRSP_CTRL	32	**CRSP Control** Controls CRSP
15004FA8	CAM_CRSP_OUT_IMG	32	**CRSP Output Image Size** CRSP output image size register
15004FAC	CAM_CRSP_STEP_OFST	32	CRSP Coefficient Step and OFST
15004FB0	CAM_CRSP_CROP_X	32	**CRSP_CROP_X** CRSP_CROP horizontal direction
15004FB4	CAM_CRSP_CROP_Y	32	**CRSP_CROP_Y** CRSP_CROP vertical direction
15004FC0	CAM_SL2C_CEN	32	SL2C Circular Center Register
15004FC4	CAM_SL2C_MAX0_RR	32	SL2C MAX0 Radius Register
15004FC8	CAM_SL2C_MAX1_RR	32	SL2C MAX1 Radius Register
15004FCC	CAM_SL2C_MAX2_RR	32	SL2C MAX2 Radius Register
15004FD0	CAM_SL2C_HRZ	32	SL2C HRZ Compensation Register
15004FD4	CAM_SL2C_XOFF	32	SL2C Horizontal Offset Register
15004FD8	CAM_SL2C_YOFF	32	SL2C Vertical Offset Register
15005000 ~ 1500523C	CAM_GGM_LUT_RB[n] (n=0~143)	32	GGM_RB_GAMMA_TABLE
15005240 ~ 1500547C	CAM_GGM_LUT_G[n] (n=0~143)	32	GGM_G_GAMMA_TABLE
15005480	CAM_GGM_CTRL	32	GGM_CONTROL
15005800 ~ 15005D9C	CAM_PCA_TBL[n] (n=0~359)	32	PCA Table Register
15005E00	CAM_PCA_CON1	32	PCA Control Register 1
15005E04	CAM_PCA_CON2	32	PCA Control Register 2
15006410	CAM_TG2_SEN_MODE	32	**Sensor Mode** Configures sensor mode
15006414	CAM_TG2_VF_CON	32	**VF Control** Controls view finder mode
15006418	CAM_TG2_SEN_GRAB_PXL	32	**Sensor Grab Pixel Start/End** Sensor grab window start/end pixel

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Address	Name	Width	Register Function
1500641C	CAM_TG2_SEN_GRAB_LIN	32	**SENSOR GRAB LINE Start/End** Sensor grab window start/end line
15006420	CAM_TG2_PATH_CFG	32	**TG Path Config** Configures TG path
15006424	CAM_TG2_MEMIN_CTL	32	**MEMIN Control** Memory in control register
15006428	CAM_TG2_INT1	32	**TG Interrupt 1** TG interrupt 1 setting
1500642C	CAM_TG2_INT2	32	**TG Interrupt 2** TG interrupt 2 setting
15006430	CAM_TG2_SOF_CNT	32	**TG SOF CNT** TG SOF count
15006434	CAM_TG2_SOT_CNT	32	**TG SOT CNT** TG SOT count
15006438	CAM_TG2_EOT_CNT	32	**TG EOT CNT** TG EOT count
1500643C	CAM_TG2_ERR_CTL	32	**TG Error CTL** TG error control
15006440	CAM_TG2_DAT_NO	32	**TG Out Data Num** TG output data number
15006444	CAM_TG2_FRM_CNT_ST	32	**TG_FRM_CNT_ST** TG frame count status
15006448	CAM_TG2_FRMSIZE_ST	32	**TG FRM SIZE ST** TG frame size status
1500644C	CAM_TG2_INTER_ST	32	**TG INTER ST** TG internal status
15006500	CAM_OBC_D_OFFST0	32	**OBC Offset 0** Optical black correction offset 0 register
15006504	CAM_OBC_D_OFFST1	32	**OBC Offset 1** Optical black correction offset 1 register
15006508	CAM_OBC_D_OFFST2	32	**OBC Offset 2** Optical black correction offset 2 register
1500650C	CAM_OBC_D_OFFST3	32	**OBC Offset 3** Optical black correction offset 3 register
15006510	CAM_OBC_D_GAIN0	32	**OBC Gain 0** Optical black correction gain 0 register
15006514	CAM_OBC_D_GAIN1	32	**OBC Gain 1** Optical black correction gain 1 register
15006518	CAM_OBC_D_GAIN2	32	**OBC Gain 2** Optical black correction gain 2 register
1500651C	CAM_OBC_D_GAIN3	32	**OBC Gain 3** Optical black correction gain 3 register
15006530	CAM_LSC_D_CTL1	32	Shading Control 2 Register
15006534	CAM_LSC_D_CTL2	32	Shading Control 2 Register
15006538	CAM_LSC_D_CTL3	32	**LSC Spare Register** LSC spare register
1500653C	CAM_LSC_D_LBLOCK	32	**Shading Last Block Config Register** Shading last block configuration register
15006540	CAM_LSC_D_RATIO	32	**Shading Ratio Config Register** Shading ratio configuration register
15006544	CAM_LSC_D_TPIPE_O	32	**Shading Tile Offset Register**

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Address	Name	Width	Register Function
	FST		Shading tile offset register
15006548	CAM_LSC_D_TPIPE_SIZE	32	**Shading Tile Size Register** Shading tile size register
1500654C	CAM_LSC_D_GAIN_TH	32	**Shading Gain Threshold Register** Shading gain threshold register
15006550	CAM_RPG_D_SATU_1	32	**RPG_D_SATU_1** Maximum saturation value
15006554	CAM_RPG_D_SATU_2	32	**RPG_D_SATU_2** Maximum saturation value
15006558	CAM_RPG_D_GAIN_1	32	**RPG_D_GAIN_1** Controls gain
1500655C	CAM_RPG_D_GAIN_2	32	**RPG_D_GAIN_2** Controls gain
15006560	CAM_RPG_D_OFST_1	32	**RPG_D_OFST_1** Offset
15006564	CAM_RPG_D_OFST_2	32	**RPG_D_OFST_2** Offset
150065B0	CAM_AWB_D_WIN_ORG	32	AWB Window Origin
150065B4	CAM_AWB_D_WIN_SIZE	32	AWB Window Size
150065B8	CAM_AWB_D_WIN_PIT	32	AWB Window Pitch
150065BC	CAM_AWB_D_WIN_NUM	32	AWB Window Number
150065C0	CAM_AWB_D_GAIN1_0	32	AWB Raw PreGain1 R/G
150065C4	CAM_AWB_D_GAIN1_1	32	AWB Raw PreGain1 B
150065C8	CAM_AWB_D_LMT1_0	32	AWB Raw Limit1 R/G
150065CC	CAM_AWB_D_LMT1_1	32	AWB Raw Limit1 B
150065D0	CAM_AWB_D_LOW_THR	32	AWB Low Threshold
150065D4	CAM_AWB_D_HI_THR	32	AWB High Threshold
150065D8	CAM_AWB_D_PIXEL_CNT0	32	AWB Pixel cnt 0
150065DC	CAM_AWB_D_PIXEL_CNT1	32	AWB Pixel cnt 1
150065E0	CAM_AWB_D_PIXEL_CNT2	32	AWB Pixel cnt 2
150065E4	CAM_AWB_D_ERR_THR	32	AWB Error Threshold
150065E8	CAM_AWB_D_ROT	32	AWB Rotation Parameter
150065EC	CAM_AWB_D_L0_X	32	AWB Light0 x Region
150065F0	CAM_AWB_D_L0_Y	32	AWB Light0 y Region
150065F4	CAM_AWB_D_L1_X	32	AWB Light1 x Region
150065F8	CAM_AWB_D_L1_Y	32	AWB Light1 y Region
150065FC	CAM_AWB_D_L2_X	32	AWB Light2 x Region
15006600	CAM_AWB_D_L2_Y	32	AWB Light2 y Region
15006604	CAM_AWB_D_L3_X	32	AWB Light3 x Region
15006608	CAM_AWB_D_L3_Y	32	AWB Light3 y Region

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Address	Name	Width	Register Function
1500660C	CAM_AWB_D_L4_X	32	AWB Light4 x Region
15006610	CAM_AWB_D_L4_Y	32	AWB Light4 y Region
15006614	CAM_AWB_D_L5_X	32	AWB Light5 x Region
15006618	CAM_AWB_D_L5_Y	32	AWB Light5 y Region
1500661C	CAM_AWB_D_L6_X	32	AWB Light6 x Region
15006620	CAM_AWB_D_L6_Y	32	AWB Light6 y Region
15006624	CAM_AWB_D_L7_X	32	AWB Light7 x Region
15006628	CAM_AWB_D_L7_Y	32	AWB Light7 y Region
1500662C	CAM_AWB_D_L8_X	32	AWB Light8 x Region
15006630	CAM_AWB_D_L8_Y	32	AWB Light8 y Region
15006634	CAM_AWB_D_L9_X	32	AWB Light9 x Region
15006638	CAM_AWB_D_L9_Y	32	AWB Light9 y Region
1500663C	CAM_AWB_D_SPARE	32	AWB Spare Register
15006650	CAM_AE_D_HST_CTL	32	AE Histogram Control
15006654	CAM_AE_D_GAIN2_0	32	AE Raw PreGain2 R/G
15006658	CAM_AE_D_GAIN2_1	32	AE Raw PreGain2 B
1500665C	CAM_AE_D_LMT2_0	32	AE Raw Limit2 R/G
15006660	CAM_AE_D_LMT2_1	32	AE Raw Limit2 B
15006664	CAM_AE_D_RC_CNV_0	32	AE Matrix Coeff 0
15006668	CAM_AE_D_RC_CNV_1	32	AE Matrix Coeff 1
1500666C	CAM_AE_D_RC_CNV_2	32	AE Matrix Coeff 2
15006670	CAM_AE_D_RC_CNV_3	32	AE Matrix Coeff 3
15006674	CAM_AE_D_RC_CNV_4	32	AE Matrix Coeff 4
15006678	CAM_AE_D_YGAMMA_0	32	AE YGAMMA Set 0
1500667C	CAM_AE_D_YGAMMA_1	32	AE YGAMMA Set 1
15006680	CAM_AE_D_HST_SET	32	AE Histogram Setting
15006684	CAM_AE_D_HST0_RNG	32	AE Histogram 0 Range
15006688	CAM_AE_D_HST1_RNG	32	AE Histogram 1 Range
1500668C	CAM_AE_D_HST2_RNG	32	AE Histogram 2 Range
15006690	CAM_AE_D_HST3_RNG	32	AE Histogram 3 Range
15006694	CAM_AE_D_SPARE	32	**AE Spare Register** AE spare register
150066A0	CAM_SGG1_D_PGN	32	**SGG PGN** SGG gain control
150066A4	CAM_SGG1_D_GMRC_1	32	**SGG GMRC 1** SGG gamma control 1
150066A8	CAM_SGG1_D_GMRC_2	32	**SGG GMRC 2** SGG gamma control 2
150066B0	CAM_AF_D_CON	32	AF Control

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Address	Name	Width	Register Function
150066B4	CAM_AF_D_WINX_1	32	AF Window X 0&1
150066B8	CAM_AF_D_WINX_2	32	AF Window X 2&3
150066BC	CAM_AF_D_WINX_3	32	AF Window X 4&5
150066C0	CAM_AF_D_WINY_1	32	AF Window Y 0&1
150066C4	CAM_AF_D_WINY_2	32	AF Window Y 2&3
150066C8	CAM_AF_D_WINY_3	32	AF Window Y 4&5
150066CC	CAM_AF_D_SIZE	32	AF Window Size
150066D4	CAM_AF_D_FLT_1	32	AF Filter P1~P4
150066D8	CAM_AF_D_FLT_2	32	AF Filter P5~P8
150066DC	CAM_AF_D_FLT_3	32	AF Filter P9~P12
150066E0	CAM_AF_D_TH	32	AF Filter Threshold
150066E4	CAM_AF_D_FLO_WIN_1	32	AF Floating Window 1 X&Y
150066E8	CAM_AF_D_FLO_SIZE_1	32	AF Floating Window 1 Size
150066EC	CAM_AF_D_FLO_WIN_2	32	AF Floating Window 2 X&Y
150066F0	CAM_AF_D_FLO_SIZE_2	32	AF Floating Window 2 Size
150066F4	CAM_AF_D_FLO_WIN_3	32	AF Floating Window 3 X&Y
150066F8	CAM_AF_D_FLO_SIZE_3	32	AF Floating Window 3 Size
150066FC	CAM_AF_D_FLO_TH	32	AF Floating Window Filter Threshold
15006700	CAM_AF_D_IMAGE_SIZE	32	AF Input Image Size
15006704	CAM_AF_D_FLT_4	32	AF Vertical Filter X0~X1
15006708	CAM_AF_D_FLT_5	32	AF Vertical Filter X2~X3
1500670C	CAM_AF_D_STAT_L	32	AF Target Window Statistics Output (LSB)
15006710	CAM_AF_D_STAT_M	32	AF Target Window Statistics Output (MSB)
15006714	CAM_AF_D_FLO_STAT_1L	32	AF Floating Window 1 Statistics Output (LSB)
15006718	CAM_AF_D_FLO_STAT_1M	32	AF Floating Window 1 Statistics Output (MSB)
1500671C	CAM_AF_D_FLO_STAT_1V	32	AF Floating Window 1 Statistics Output (VER)
15006720	CAM_AF_D_FLO_STAT_2L	32	AF Floating Window 2 Statistics Output (LSB)
15006724	CAM_AF_D_FLO_STAT_2M	32	AF Floating Window 2 Statistics Output (MSB)
15006728	CAM_AF_D_FLO_STAT_2V	32	AF Floating Window 2 Statistics Output (VER)
1500672C	CAM_AF_D_FLO_STAT_3L	32	AF Floating Window 3 Statistics Output (LSB)
15006730	CAM_AF_D_FLO_STAT_3M	32	AF Floating Window 3 Statistics Output (MSB)
15006734	CAM_AF_D_FLO_STAT_3V	32	AF Floating Window 3 Statistics Output (VER)
15006760	CAM_WBN_D_SIZE	32	**WBN_D_SIZE** BIN input H and V size
15006764	CAM_WBN_D_MODE	32	**WBN_D_MODE** Binning mode

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Address	Name	Width	Register Function
15006780	CAM_LCS_D_CON	32	LCS Control Register
15006784	CAM_LCS_D_ST	32	LCS Start Point
15006788	CAM_LCS_D_AWS	32	LCS Active Window Size
1500678C	CAM_LCS_D_FLR	32	LCS Flare
15006790	CAM_LCS_D_LRZR_1	32	LCS Horizontal Down-sampling Ratio
15006794	CAM_LCS_D_LRZR_2	32	LCS Vertical Down-sampling Ratio
150067A0	CAM_RRZ_D_CTL	32	**RRZ_D CTL** RRZ control register
150067A4	CAM_RRZ_D_IN_IMG	32	**RRZ_D IN IMG** RRZ input image size register
150067A8	CAM_RRZ_D_OUT_IMG	32	**RRZ_D OUT IMG** RRZ output image size register
150067AC	CAM_RRZ_D_HORI_STEP	32	**RRZ_D_HORI_STEP** RRZ horizontal coefficient step
150067B0	CAM_RRZ_D_VERT_STEP	32	**RRZ_D_VERT_STEP** RRZ vertical coefficient step
150067B4	CAM_RRZ_D_HORI_INT_OFST	32	**RRZ_D_HORI_INT_OFST** RRZ horizontal integer offset
150067B8	CAM_RRZ_D_HORI_SUB_OFST	32	**RRZ_D_HORI_SUB_OFST** RRZ horizontal sub-pixel offset
150067BC	CAM_RRZ_D_VERT_INT_OFST	32	**RRZ_D_VERT_INT_OFST** RRZ vertical integer offset
150067C0	CAM_RRZ_D_VERT_SUB_OFST	32	**RRZ_D_VERT_SUB_OFST** RRZ vertical sub-pixel offset
150067C4	CAM_RRZ_D_MODE_TH	32	RRZ_D_TH_MD
150067C8	CAM_RRZ_D_MODE_CTL	32	RRZ_D_TBL_SEL_SP
15006800	CAM_BPC_D_CON	32	2D BPC_D Control Register
15006804	CAM_BPC_D_TH1	32	BPC_D Detection Condition 1 Register 1
15006808	CAM_BPC_D_TH2	32	BPC_D Detection Condition 1 Register 1
1500680C	CAM_BPC_D_TH3	32	BPC_D Detection Condition 1 Register 2
15006810	CAM_BPC_D_TH4	32	BPC_D Detection Condition 1 Register 3
15006814	CAM_BPC_D_DTC	32	BPC_D Detection Condition 1/2/3 Register
15006818	CAM_BPC_D_COR	32	BPC_D Correction Register
1500681C	CAM_BPC_D_TBLI1	32	BPC_D Table input information Register 1
15006820	CAM_BPC_D_TBLI2	32	BPC_D Table input information Register 2
15006824	CAM_BPC_D_TH1_C	32	BPC_D Detection Extension Condition 1 Register 1
15006828	CAM_BPC_D_TH2_C	32	BPC_D Detection Extension Condition 1 Register 2
1500682C	CAM_BPC_D_TH3_C	32	BPC_D Detection Extension Condition 1 Register 3
15006850	CAM_NR1_D_CON	32	NR1_D Control Register
15006854	CAM_NR1_D_CT_CON	32	NR1_D Crosstalk Compensation Configuration Register
15006858	CAM_BNR_D_RSV1	32	BNR_D RSV1
1500685C	CAM_BNR_D_RSV2	32	BNR_D RSV2
15006A00	CAM_CPG_D_SATU_1	32	CPG_SATU_1
15006A04	CAM_CPG_D_SATU_2	32	CPG_SATU_2
15006A08	CAM_CPG_D_GAIN_1	32	CPG_GAIN_1
15006A0C	CAM_CPG_D_GAIN_2	32	CPG_GAIN_2

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Address	Name	Width	Register Function
15006A10	CAM_CPG_D_OFST_1	32	CPG_OFST_1
15006A14	CAM_CPG_D_OFST_2	32	CPG_OFST_2
15006E00	CAM_DMX_CTL	32	**DMX_CTL** DMX control
15006E04	CAM_DMX_CROP	32	**DMX_CROP** DMX crop for datapath
15006E08	CAM_DMX_VSIZE	32	**DMX_VSIZE** DMX vertical sSize
15006E10	CAM_BMX_CTL	32	**BMX_CTL** BMX control
15006E14	CAM_BMX_CROP	32	**BMX_CROP** BMX crop for datapath
15006E18	CAM_BMX_VSIZE	32	**BMX_VSIZE** BMX vertical size
15006E20	CAM_RMX_CTL	32	**RMX_CTL** RMX control
15006E24	CAM_RMX_CROP	32	**RMX_CROP** RMX crop for datapath
15006E28	CAM_RMX_VSIZE	32	**RMX_VSIZE** RMX vertical size
15007200	CAM_DMA_SOFT_RSTSTAT	32	DMA Software Reset Status
15007204	CAM_TDRI_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
15007208	CAM_TDRI_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
1500720C	CAM_TDRI_XSIZE	32	DMA XSIZE
15007210	CAM_CQ0I_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
15007214	CAM_CQ0I_XSIZE	32	**DMA XSIZE** DMA XSIZE
15007218	CAM_CQ0I_D_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
1500721C	CAM_CQ0I_D_XSIZE	32	DMA XSIZE
15007220	CAM_VERTICAL_FLIP_EN	32	**DMA Vertical Flip Register** DMA base address
15007224	CAM_DMA_SOFT_RESET	32	**DMA Software Reset** DMA base address
15007228	CAM_LAST_ULTRA_EN	32	**DMA Last Ultra Register** DMA base address
1500722C	CAM_IMGI_SLOW_DOWN	32	**DMA IMGI Slow Down Register** DMA base address
15007230	CAM_IMGI_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
15007234	CAM_IMGI_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
15007238	CAM_IMGI_XSIZE	32	DMA XSIZE
1500723C	CAM_IMGI_YSIZE	32	DMA YSIZE
15007240	CAM_IMGI_STRIDE	32	DMA Stride
15007248	CAM_IMGI_CON	32	DMA Control Register

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Address	Name	Width	Register Function
1500724C	CAM_IMGI_CON2	32	DMA Control Register 2
15007250	CAM_BPCI_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
15007254	CAM_BPCI_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
15007258	CAM_BPCI_XSIZE	32	DMA XSIZE
1500725C	CAM_BPCI_YSIZE	32	DMA YSIZE
15007260	CAM_BPCI_STRIDE	32	DMA Stride
15007264	CAM_BPCI_CON	32	DMA Control Register
15007268	CAM_BPCI_CON2	32	DMA Control Register 2
1500726C	CAM_LSCI_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
15007270	CAM_LSCI_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
15007274	CAM_LSCI_XSIZE	32	DMA XSIZE
15007278	CAM_LSCI_YSIZE	32	DMA YSIZE
1500727C	CAM_LSCI_STRIDE	32	DMA Stride
15007280	CAM_LSCI_CON	32	DMA Control Register
15007284	CAM_LSCI_CON2	32	DMA Control Register 2
15007288	CAM_UFDI_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
1500728C	CAM_UFDI_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
15007290	CAM_UFDI_XSIZE	32	DMA XSIZE
15007294	CAM_UFDI_YSIZE	32	DMA YSIZE
15007298	CAM_UFDI_STRIDE	32	DMA Stride
1500729C	CAM_UFDI_CON	32	DMA Control Register
150072A0	CAM_UFDI_CON2	32	DMA Control Register 2
150072A4	CAM_LCEI_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
150072A8	CAM_LCEI_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
150072AC	CAM_LCEI_XSIZE	32	DMA XSIZE
150072B0	CAM_LCEI_YSIZE	32	DMA YSIZE
150072B4	CAM_LCEI_STRIDE	32	DMA Stride
150072B8	CAM_LCEI_CON	32	DMA Control Register
150072BC	CAM_LCEI_CON2	32	DMA Control Register 2
150072C0	CAM_VIPI_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
150072C4	CAM_VIPI_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
150072C8	CAM_VIPI_XSIZE	32	DMA XSIZE
150072CC	CAM_VIPI_YSIZE	32	DMA YSIZE
150072D0	CAM_VIPI_STRIDE	32	DMA Stride
150072D8	CAM_VIPI_CON	32	DMA Control Register
150072DC	CAM_VIPI_CON2	32	DMA Control Register 2
150072E0	CAM_VIP2I_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address

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Address	Name	Width	Register Function
150072E4	CAM_VIP2I_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
150072E8	CAM_VIP2I_XSIZE	32	DMA XSIZE
150072EC	CAM_VIP2I_YSIZE	32	DMA YSIZE
150072F0	CAM_VIP2I_STRIDE	32	DMA Stride
150072F8	CAM_VIP2I_CON	32	DMA Control Register
150072FC	CAM_VIP2I_CON2	32	DMA Control Register 2
15007300	CAM_IMGO_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
15007304	CAM_IMGO_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
15007308	CAM_IMGO_XSIZE	32	DMA XSIZE
1500730C	CAM_IMGO_YSIZE	32	DMA YSIZE
15007310	CAM_IMGO_STRIDE	32	DMA Stride
15007314	CAM_IMGO_CON	32	DMA Control Register
15007318	CAM_IMGO_CON2	32	DMA Control Register 2
1500731C	CAM_IMGO_CROP	32	DMA Crop Function Register
15007320	CAM_RRZO_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
15007324	CAM_RRZO_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
15007328	CAM_RRZO_XSIZE	32	DMA XSIZE
1500732C	CAM_RRZO_YSIZE	32	DMA YSIZE
15007330	CAM_RRZO_STRIDE	32	DMA Stride
15007334	CAM_RRZO_CON	32	DMA Control Register
15007338	CAM_RRZO_CON2	32	DMA Control Register 2
1500733C	CAM_RRZO_CROP	32	DMA Crop Function Register
15007340	CAM_LCSO_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
15007344	CAM_LCSO_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
15007348	CAM_LCSO_XSIZE	32	DMA XSIZE
1500734C	CAM_LCSO_YSIZE	32	DMA YSIZE
15007350	CAM_LCSO_STRIDE	32	DMA Stride
15007354	CAM_LCSO_CON	32	DMA Control Register
15007358	CAM_LCSO_CON2	32	DMA Control Register 2
1500735C	CAM_EISO_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
15007360	CAM_EISO_XSIZE	32	DMA XSIZE
15007364	CAM_AFO_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
15007368	CAM_AFO_XSIZE	32	DMA XSIZE
1500736C	CAM_ESFKO_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
15007370	CAM_ESFKO_XSIZE	32	DMA XSIZE
15007374	CAM_ESFKO_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
15007378	CAM_ESFKO_YSIZE	32	DMA YSIZE

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Address	Name	Width	Register Function
1500737C	CAM_ESFKO_STRIDE	32	DMA Stride
15007380	CAM_ESFKO_CON	32	DMA Control Register
15007384	CAM_ESFKO_CON2	32	DMA Control Register 2
15007388	CAM_AAO_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
1500738C	CAM_AAO_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
15007390	CAM_AAO_XSIZE	32	DMA XSIZE
15007394	CAM_AAO_YSIZE	32	DMA YSIZE
15007398	CAM_AAO_STRIDE	32	DMA Stride
1500739C	CAM_AAO_CON	32	DMA Control Register
150073A0	CAM_AAO_CON2	32	DMA Control Register 2
150073A4	CAM_VIP3I_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
150073A8	CAM_VIP3I_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
150073AC	CAM_VIP3I_XSIZE	32	DMA XSIZE
150073B0	CAM_VIP3I_YSIZE	32	DMA YSIZE
150073B4	CAM_VIP3I_STRIDE	32	DMA Stride
150073BC	CAM_VIP3I_CON	32	DMA Control Register
150073C0	CAM_VIP3I_CON2	32	DMA Control Register 2
150073C4	CAM_UFEO_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
150073C8	CAM_UFEO_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
150073CC	CAM_UFEO_XSIZE	32	DMA XSIZE
150073D0	CAM_UFEO_YSIZE	32	DMA YSIZE
150073D4	CAM_UFEO_STRIDE	32	DMA Stride
150073D8	CAM_UFEO_CON	32	DMA Control Register
150073DC	CAM_UFEO_CON2	32	DMA Control Register 2
150073E0	CAM_MFBO_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
150073E4	CAM_MFBO_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
150073E8	CAM_MFBO_XSIZE	32	DMA XSIZE
150073EC	CAM_MFBO_YSIZE	32	DMA YSIZE
150073F0	CAM_MFBO_STRIDE	32	DMA Stride
150073F4	CAM_MFBO_CON	32	DMA Control Register
150073F8	CAM_MFBO_CON2	32	DMA Control Register 2
150073FC	CAM_MFBO_CROP	32	DMA Crop Function Register
15007400	CAM_IMG3BO_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
15007404	CAM_IMG3BO_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
15007408	CAM_IMG3BO_XSIZE	32	DMA XSIZE
1500740C	CAM_IMG3BO_YSIZE	32	DMA YSIZE
15007410	CAM_IMG3BO_STRIDE	32	DMA Stride
15007414	CAM_IMG3BO_CON	32	DMA Control Register

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Address	Name	Width	Register Function
15007418	CAM_IMG3BO_CON2	32	DMA Control Register 2
1500741C	CAM_IMG3BO_CROP	32	DMA Crop Function Register
15007420	CAM_IMG3CO_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
15007424	CAM_IMG3CO_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
15007428	CAM_IMG3CO_XSIZE	32	DMA XSIZE
1500742C	CAM_IMG3CO_YSIZE	32	DMA YSIZE
15007430	CAM_IMG3CO_STRIDE	32	DMA Stride
15007434	CAM_IMG3CO_CON	32	DMA Control Register
15007438	CAM_IMG3CO_CON2	32	DMA Control Register 2
1500743C	CAM_IMG3CO_CROP	32	DMA Crop Function Register
15007440	CAM_IMG2O_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
15007444	CAM_IMG2O_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
15007448	CAM_IMG2O_XSIZE	32	DMA XSIZE
1500744C	CAM_IMG2O_YSIZE	32	DMA YSIZE
15007450	CAM_IMG2O_STRIDE	32	DMA Stride
15007454	CAM_IMG2O_CON	32	DMA Control Register
15007458	CAM_IMG2O_CON2	32	DMA Control Register 2
1500745C	CAM_IMG2O_CROP	32	DMA Crop Function Register
15007460	CAM_IMG3O_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
15007464	CAM_IMG3O_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
15007468	CAM_IMG3O_XSIZE	32	DMA XSIZE
1500746C	CAM_IMG3O_YSIZE	32	DMA YSIZE
15007470	CAM_IMG3O_STRIDE	32	DMA Stride
15007474	CAM_IMG3O_CON	32	DMA Control Register
15007478	CAM_IMG3O_CON2	32	DMA Control Register 2
1500747C	CAM_IMG3O_CROP	32	DMA Crop Function Register
15007480	CAM_FEO_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
15007484	CAM_FEO_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
15007488	CAM_FEO_XSIZE	32	DMA XSIZE
1500748C	CAM_FEO_YSIZE	32	DMA YSIZE
15007490	CAM_FEO_STRIDE	32	DMA Stride
15007494	CAM_FEO_CON	32	DMA Control Register
15007498	CAM_FEO_CON2	32	DMA Control Register 2
1500749C	CAM_BPCI_D_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
150074A0	CAM_BPCI_D_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
150074A4	CAM_BPCI_D_XSIZE	32	DMA XSIZE
150074A8	CAM_BPCI_D_YSIZE	32	DMA YSIZE
150074AC	CAM_BPCI_D_STRIDE	32	DMA Stride

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Address	Name	Width	Register Function
150074B0	CAM_BPCI_D_CON	32	DMA Control Register
150074B4	CAM_BPCI_D_CON2	32	DMA Control Register 2
150074B8	CAM_LSCI_D_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
150074BC	CAM_LSCI_D_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
150074C0	CAM_LSCI_D_XSIZE	32	DMA XSIZE
150074C4	CAM_LSCI_D_YSIZE	32	DMA YSIZE
150074C8	CAM_LSCI_D_STRIDE	32	DMA Stride
150074CC	CAM_LSCI_D_CON	32	DMA Control Register
150074D0	CAM_LSCI_D_CON2	32	DMA Control Register 2
150074D4	CAM_IMGO_D_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
150074D8	CAM_IMGO_D_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
150074DC	CAM_IMGO_D_XSIZE	32	DMA XSIZE
150074E0	CAM_IMGO_D_YSIZE	32	DMA YSIZE
150074E4	CAM_IMGO_D_STRIDE	32	DMA Stride
150074E8	CAM_IMGO_D_CON	32	DMA Control Register
150074EC	CAM_IMGO_D_CON2	32	DMA Control Register 2
150074F0	CAM_IMGO_D_CROP	32	DMA Crop Function Register
150074F4	CAM_RRZO_D_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
150074F8	CAM_RRZO_D_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
150074FC	CAM_RRZO_D_XSIZE	32	DMA XSIZE
15007500	CAM_RRZO_D_YSIZE	32	DMA YSIZE
15007504	CAM_RRZO_D_STRIDE	32	DMA Stride
15007508	CAM_RRZO_D_CON	32	DMA Control Register
1500750C	CAM_RRZO_D_CON2	32	DMA Control Register 2
15007510	CAM_RRZO_D_CROP	32	DMA Crop Function Register
15007514	CAM_LCSO_D_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
15007518	CAM_LCSO_D_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
1500751C	CAM_LCSO_D_XSIZE	32	DMA XSIZE
15007520	CAM_LCSO_D_YSIZE	32	DMA YSIZE
15007524	CAM_LCSO_D_STRIDE	32	DMA Stride
15007528	CAM_LCSO_D_CON	32	DMA Control Register
1500752C	CAM_LCSO_D_CON2	32	DMA control register 2
15007530	CAM_AFO_D_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
15007534	CAM_AFO_D_XSIZE	32	DMA XSIZE
15007538	CAM_AFO_D_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
1500753C	CAM_AFO_D_YSIZE	32	DMA YSIZE

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Address	Name	Width	Register Function
15007540	CAM_AFO_D_STRIDE	32	DMA Stride
15007544	CAM_AFO_D_CON	32	DMA Control Register
15007548	CAM_AFO_D_CON2	32	DMA Control Register 2
1500754C	CAM_AAO_D_BASE_ADDR	32	**DMA Base ADDR Register** DMA base address
15007550	CAM_AAO_D_OFST_ADDR	32	**DMA Offset ADDR Register** DMA offset address
15007554	CAM_AAO_D_XSIZE	32	DMA XSIZE
15007558	CAM_AAO_D_YSIZE	32	DMA YSIZE
1500755C	CAM_AAO_D_STRIDE	32	DMA Stride
15007560	CAM_AAO_D_CON	32	DMA Control Register
15007564	CAM_AAO_D_CON2	32	DMA Control Register 2
15007568	CAM_DMA_ERR_CTRL	32	DMA Error Control Register
1500756C	CAM_IMGI_ERR_STAT	32	IMGI Error Status Register
15007570	CAM_BPCI_ERR_STAT	32	IMGI Error Status Register
15007574	CAM_LSCI_ERR_STAT	32	LSCI Error Status Register
15007578	CAM_UFDI_ERR_STAT	32	UFDI Error Status Register
1500757C	CAM_LCEI_ERR_STAT	32	LCEI Error Status Register
15007580	CAM_VIPI_ERR_STAT	32	VIPI Error Status Register
15007584	CAM_VIP2I_ERR_STAT	32	VIP2I Error Status Register
15007588	CAM_VIP3I_ERR_STAT	32	VIP3I Error Status Register
1500758C	CAM_IMGO_ERR_STAT	32	IMGO Error Status Register
15007590	CAM_RRZO_ERR_STAT	32	RRZO Error Status Register
15007594	CAM_LCSO_ERR_STAT	32	LCEO Error Status Register
15007598	CAM_ESFKO_ERR_STAT	32	ESFKO Error Status Register
1500759C	CAM_AAO_ERR_STAT	32	AAO Error Status Register
150075A0	CAM_UFEO_ERR_STAT	32	UFEO Error Status Register
150075A4	CAM_MFBO_ERR_STAT	32	MFBO Error Status Register
150075A8	CAM_IMG3BO_ERR_STAT	32	IMG3BO Error Status Register
150075AC	CAM_IMG3CO_ERR_STAT	32	IMG3CO Error Status Register
150075B0	CAM_IMG2O_ERR_STAT	32	IMG2O Error Status Register
150075B4	CAM_IMG3O_ERR_STAT	32	IMG3O Error Status Register
150075B8	CAM_FEO_ERR_STAT	32	FEO Error Status Register
150075BC	CAM_BPCI_D_ERR_STAT	32	BPCI_D Error Status Register
150075C0	CAM_LSCI_D_ERR_STAT	32	LSCI_D Error Status Register
150075C4	CAM_IMGO_D_ERR_STAT	32	IMGO_D Error Status Register

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Address	Name	Width	Register Function
150075C8	CAM_RRZO_D_ERR_STAT	32	RRZO_D Error Status Register
150075CC	CAM_LCSO_D_ERR_STAT	32	LCSO_D Error Status Register
150075D0	CAM_AFO_D_ERR_STAT	32	AFO_D Error Status Register
150075D4	CAM_AAO_D_ERR_STAT	32	AAO_D Error Status Register
150075D8	CAM_DMA_DEBUG_ADDR	32	**DMA Debug Address** DMA debugging address
150075DC	CAM_DMA_RSV1	32	Reserve1
150075E0	CAM_DMA_RSV2	32	Reserve2
150075E4	CAM_DMA_RSV3	32	Reserve3
150075E8	CAM_DMA_RSV4	32	Reserve4
150075EC	CAM_DMA_RSV5	32	Reserve5
150075F0	CAM_DMA_RSV6	32	Reserve6
150075F4	CAM_DMA_DEBUG_SEL	32	**DMA Debug Sel Register** Reserve6
150075F8	CAM_DMA_BW_SELF_TEST	32	**DMA BWs Self Test Register** Reserve6

15004000 CAM_CTL_START CTL_START 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			CQ0B_D_START	CQ0_D_START			LSC_PREFETCH_TRIG_D	LSC_PREFETCH_TRIG		CQ0B_START	CQ0_START	PASS2C_START			PASS2B_START	PASS2_START
Type			WO	WO			WO	WO		WO	WO	WO			WO	WO
Reset			0	0			0	0		0	0	0			0	0

Bit(s)	Name	Description
13	CQ0B_D_START	**CQ0b start** It has two modes. See CQ0_mode field in CTL_SEL module. CQ0B is for TG2 in Native 3D case; only works when CQ0B_CONT=0.
12	CQ0_D_START	**CQ0 start** It has two modes. See CQ0_mode field in CTL_SEL module. Only works when CQ0_CONT=0.
9	LSC_PREFETCH_TRIG_D	**Triggers lens shading table preftech** It triggers immediately. For LSCI and LSC.
8	LSC_PREFETCH_TRIG	**Triggers lens shading table preftech** It triggers immediately trigger. For LSCI and LSC.
6	CQ0B_START	**CQ0b start** It has two modes. See CQ0_mode field in CTL_SEL module. CQ0B is for TG2

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Bit(s)	Name	Description
		in Native 3D case; only works when CQ0B_CONT=0.
5	CQ0_START	**CQ0 start** It has two modes. See CQ0_mode field in CTL_SEL module. Only works when CQ0_CONT=0.
4	PASS2C_START	**Pass2C module start signal** Used for all sceanrio and concurrence modes. In this case, the command queue must be eanbled and load CQ3 data 2. In TPIPE processing scenario, if TPIPE interrupt setting on TPIPE cofiguration map is 1, it will need to trigger pass2_start again after TPIPE_int is issued.
1	PASS2B_START	**Pass2B module start signal** Used for all sceanrio and concurrence modes. In this case, the command queue must eanbled and load CQ2 data. In TPIPE processing scenario, if TPIPE interrupt setting on TPIPE cofiguration map is 1, it will need to trigger pass2_start again after TPIPE_int is issued.
0	PASS2_START	**Pass2 module start signal** Used for all sceanrios. If CQ_en =1, it will load CQ1 data first. In TPIPE processing scenario, if TPIPE interrupt setting on TPIPE cofiguration map is 1, it will need to trigger pass2_start again after TPIPE_int is issued.

15004004 **CAM_CTL_EN_P1** **ISP P1 Enable1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CPG_EN	RMG_EN	EIS_EN	SGG2_EN	AA_EN	HBIN_EN	FLK_EN	AF_EN
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SGG1_EN	LCS_EN	UFE_EN	PAK_EN	BMX_EN	PAKG_EN	RMX_EN	RRZ_EN	RPG_EN	LSC_EN	BNR_EN	OB_EN	W2G_EN	WBN_EN	DMX_EN	TG1_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23	CPG_EN	**Double buffer** Enables CPG
22	RMG_EN	**Double buffer** Enables IDHR RMG
21	EIS_EN	**Double buffer** Enables EIS
20	SGG2_EN	**Double buffer** Enables SGG2
19	AA_EN	**Double buffer** Enables AE/AWB
18	HBIN_EN	**Double buffer** Enables camera bin
17	FLK_EN	**Double buffer** Enables flicker
16	AF_EN	**Double buffer**

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Bit(s)	Name	Description
		Enables AF
15	SGG1_EN	**Double buffer** Enables simple Gain and Gamma for AF
14	LCS_EN	**Double buffer** Enables LCE statics. Please enable also LCEO DMA.
13	UFE_EN	**Double buffer** Enables UFE
12	PAK_EN	**Double buffer** Enables packing
11	BMX_EN	**Double buffer** Enables BMX
10	PAKG_EN	**Double buffer** Enables Packing2
9	RMX_EN	**Double buffer** Enables RRZ2
8	RRZ_EN	**Double buffer** Enables RRZ
7	RPG_EN	**Double buffer** Enables RRZ resizer pregain
6	LSC_EN	**Double buffer** Enables LSC. Please enable also LSCI DMA.
5	BNR_EN	**Double buffer** Enables BNR
4	OB_EN	**Double buffer** Enables OB1 (at main path)
3	W2G_EN	**Double buffer** Enables W2G
2	WBN_EN	**Double buffer** Enables WBN
1	DMX_EN	**Double buffer** Enables RRZ data de-mux
0	TG1_EN	**Enables TG1**

15004008 CAM_CTL_EN_P1_DMA ISP P1 DMA Enable1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name									LSCI_EN	BPCI_EN	AAO_EN	LCSO_EN	ESFKO_EN	RRZO_EN	UFEO_EN	IMGO_EN
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	LSCI_EN	**Double buffer**

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Bit(s)	Name	Description
		Enables shadding table input DMA
6	BPCI_EN	**Double buffer** Enables bad pix table read DMA
5	AAO_EN	**Double buffer** AE/AWB output DMA output
4	LCSO_EN	**Double buffer** Enables LCS output DMA
3	ESFKO_EN	**Double buffer** Enables EIS/Flk/AF DMA. Use this DMA for time share.
2	RRZO_EN	**Double buffer** For RRZ image data ouput
1	UFEO_EN	**Double buffer** Enables UFE length table output DMA
0	IMGO_EN	**Double buffer** LSC, WBN and TG1 image data output. Use bin_out_sel to select.

15004010 **CAM_CTL_EN_P1_D** **ISP Enable1 for 2nd Sensor** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CPG_D_EN	RMG_D_EN			AA_D_EN			AF_D_EN
Type									RW	RW			RW			RW
Reset									0	0			0			0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SGG1_D_EN	LCS_D_EN		PAK_D_EN	BMX_D_EN	PAKG_D_EN	RMX_D_EN	RRZ_D_EN	RPG_D_EN	LSC_D_EN	BNR_D_EN	OB_D_EN	W2G_D_EN	WBN_D_EN	DMX_D_EN	TG1_D_EN
Type	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23	CPG_D_EN	**Double buffer** Enables CPG
22	RMG_D_EN	**Double buffer** Enables IHDR RMG
19	AA_D_EN	**Double buffer** Enables AE/AWB
16	AF_D_EN	**Double buffer** Enables AF
15	SGG1_D_EN	**Double buffer** Enables simple Gain and Gamma for AF
14	LCS_D_EN	**Double buffer** Enables LCE statics. Please enable also LCEO DMA.
12	PAK_D_EN	**Double buffer** Enables packing
11	BMX_D_EN	**Double buffer** Enables BMX
10	PAKG_D_EN	**Double buffer**

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Bit(s)	Name	Description
		Enables Packing2
9	RMX_D_EN	**Double buffer** Enables RRZ2
8	RRZ_D_EN	**Double buffer** Enables RRZ
7	RPG_D_EN	**Double buffer** Enables RRZ resizer pregain
6	LSC_D_EN	**Double buffer** Enables LSC. Please enable also LSCI DMA.
5	BNR_D_EN	**Double buffer** Enables BNR
4	OB_D_EN	**Double buffer** Enables OB1 (at main path)
3	W2G_D_EN	**Double buffer** Enables W2G
2	WBN_D_EN	**Double buffer** Enables WBN
1	DMX_D_EN	**Double buffer** Enables RRZ data de-mux
0	TG1_D_EN	**Enables TG1**

15004014 **CAM_CTL_EN_P1_DMA_D** **ISP P1 DMA Enable1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									LSCI_D_EN	BPCI_D_EN	AAO_D_EN	LCSO_D_EN	AFO_D_EN	RRZO_D_EN		IMGO_D_EN
Type									RW	RW	RW	RW	RW	RW		RW
Reset									0	0	0	0	0	0		0

Bit(s)	Name	Description
7	LSCI_D_EN	**Double buffer** Enables 2nd shadding table input DMA
6	BPCI_D_EN	**Double buffer** Enables 2nd bad pix table read DMA
5	AAO_D_EN	**Double buffer** 2nd AE/AWB output DMA output
4	LCSO_D_EN	**Double buffer** Enables 2nd LCS output DMA
3	AFO_D_EN	**Double buffer** Enables 2nd AF. Use this DMA for time share.
2	RRZO_D_EN	**Double buffer** For 2nd RRZ image data ouput

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Bit(s)	Name	Description
0	IMGO_D_EN	**Double buffer** Second LSC, WBN and TG1 image data output. Use bin_out_sel to select.

15004018 **CAM_CTL_EN_P2** **ISP Enable2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Co2_EN	UNP_EN	FE_EN	MDPCROP_EN	C24B_EN	CRSP_EN			MIX3_EN	MIX2_EN	MIX1_EN	CRZ_EN	SRZ2_EN	SRZ1_EN	SL2C_EN	SL2B_EN
Type	RW	RW	RW	RW	RW	RW			RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0			0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NR3D_EN	LCE_EN	SEEE_EN	PCA_EN	NBC_EN	C42_EN	G2C_EN	C24_EN	MFB_EN	GGM_EN	G2G_EN	CCL_EN	CFA_EN	SL2_EN	PGN_EN	UFD_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	Co2_EN	**Double buffer** Enables Co2
30	UNP_EN	**Double buffer** Enables UN-pack
29	FE_EN	**Double buffer** Enables FE
28	MDPCROP_EN	**Double buffer** Enables MDP output crop
27	C24B_EN	**Double buffer** Enables MDP output 422 to 444 module
26	CRSP_EN	**Double buffer** Enables 3DNR output YUV420 path
23	MIX3_EN	**Double buffer** Enables MIX3
22	MIX2_EN	**Double buffer** Enables MIX2
21	MIX1_EN	**Double buffer** Enables MIX1
20	CRZ_EN	**Double buffer** Enables CRZ. If CDRZ is outputted to DRAM, also enable DPO DMA.
19	SRZ2_EN	**Double buffer** Enables SRZ2
18	SRZ1_EN	**Double buffer** Enables SRZ1
17	SL2C_EN	**Double buffer** Enables SL2 C
16	SL2B_EN	**Double buffer** Enables SL2B
15	NR3D_EN	**Double buffer**

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Bit(s)	Name	Description
		Enables NR3D
14	LCE_EN	**Dobule buffer** Enables LCEr
13	SEEE_EN	**Double buffer** Enables SEEE
12	PCA_EN	**Double buffer** Enables PCA
11	NBC_EN	**Double buffer** Enables NBC
10	C42_EN	**Double buffer** Enables YUV 444 to 422
9	G2C_EN	**Double buffer** Enables GB to YUV, including negative and sephia function.
8	C24_EN	**Double buffer** Enables YUV 422 to 444. The double buffer load time depends on scenario. If the module is at pass1, load time will be RG frame start. If the module is at pass2, load time will be pass2_start.
7	MFB_EN	**Enables MFB** DPI, VEI, BPI, PDI DMA and PDO DMA should also be enabled. Double buffer
6	GGM_EN	**Double buffer** Enables RGB Gamma
5	G2G_EN	**Double buffer** Enables 3x3 matrix
4	CCL_EN	**Double buffer** Enables CCL
3	CFA_EN	**Double buffer** Enables demosaic. HF compensation uses the same enable.
2	SL2_EN	**Double buffer** Enables SL2
1	PGN_EN	**Double buffer** Enables pregain
0	UFD_EN	**Double buffer** Enables UFD

1500401C **CAM_CTL_EN_P2_DMA** **ISP DMA Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					FEO_EN	IMG3CO_EN	IMG3BO_EN	IMG3O_EN	IMG2O_EN	MFBO_EN	LCEI_EN	VIP3I_EN	VIP2I_EN	VIPI_EN	UFDI_EN	IMGI_EN
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
11	FEO_EN	**Double buffer** Enables FE output DMA
10	IMG3CO_EN	**Double buffer** Enables 3DNR output IMG3CO, V plane
9	IMG3BO_EN	**Double buffer** Enables 3DNR output IMG3BO, U plane or UV plane
8	IMG3O_EN	**Double buffer** Enables 3DNR output IMG3Om Y plane or YUYV plane
7	IMG2O_EN	**Double buffer**
6	MFBO_EN	**Dobule buffer** Enables MFB weighting table output DMA
5	LCEI_EN	**Double buffer** Enables LCE input DMA
4	VIP3I_EN	**Double buffer** Enables VIP3I. For MFB 422 1p or N3D C02 v plane input.
3	VIP2I_EN	**Double buffer** Enables VIP2I DMA. For MFB weighting, 422 1p input or N3D c02 U plane or UV plane input.
2	VIPI_EN	**Double buffer** Enables MFB 2nd 422 1 plane DMA
1	UFDI_EN	**Double buffer** Enables UFO input DMA
0	IMGI_EN	**Double buffer** Enables IMGI. Can be UNO , UFD, C24, CCL, MFB and NR3D input. Depends on scenario. In CC scenario: UNP for bayer input UFD for UFO input CCL for RGB input C24 for YUV422 input MFB for MFB scenario NR3D for NCC scneario CQ1/2/3 also shares with IMGI DMA.

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15004020 **CAM_CTL_CQ_EN** **ISP Enable2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				CQ0_EN	CQ0B_EN	CQ0C_EN	CQ0B_MODE	CQ0C_RRZO_SEL	CQ0_MODE	CQ0B_SEL	CQ0C_IMGO_SEL	CQ0B_CONT	CQ0_CONT	CQ0A_MASK_CQ0C_EN	CQ0A_MASK_CQ0B_EN	CQ_APB_2T
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CQ0_D_EN				CQ0B_D_EN	CQ0C_D_EN	CQ0B_D_MODE	CQ0C_D_RRZO_SEL	CQ0_D_MODE	CQ0B_D_SEL	CQ0C_IMGO_D_SEL	CQ0B_CONT_D	CQ0_CONT_D	CQ0A_MASK_CQ0C_D_EN	CQ0A_MASK_CQ0B_D_EN	
Type	RW				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	

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Reset	0				0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
28	CQ0_EN	**Enables CQ0 (for pass1 module)**
27	CQ0B_EN	**Enables CQ0B (for pass1 module)**
26	CQ0C_EN	**Enables CQ0C (for pass1 module)** For IMGO or IMG2O for frame buffer control. It must be continuous mode. IMGO or IM2O is selected by CQ0C_IMGO_SEL and CQ0C_IMG2O_SEL.
25	CQ0B_MODE	**CQ0B_MODE** 0: Trigger wait pass1 frame done 1: Trigger immediately
24	CQ0C_RRZO_SEL	**Selects CQ0C trigger source** 0: Disable 1: From RRZO
23	CQ0_MODE	**CQ0_MODE** 0: Trigger wait pass1 frame done 1: Trigger immediately
22	CQ0B_SEL	**Selects CQ0B trigger source** 0: From IMG2O 1: From pass1_done
21	CQ0C_IMGO_SEL	**Selects CQ0C trigger source** 0: Disable 1: From IMGO
20	CQ0B_CONT	**0: CQ0B loads APB CMD by CQ0_TRIGGER.** 1: CQ0B automatically loads APB CMD at pass1 done.
19	CQ0_CONT	**0: CQ0 loads APB CMD by CQ0_TRIGGER.** 1: CQ0 automatically loads APB CMD at pass1 done.
18	CQ0A_MASK_CQ0C_EN	**CQ0A can mask CQ0C trigger.**
17	CQ0A_MASK_CQ0B_EN	**CQ0A can mask CQ0B trigger.**
16	CQ_APB_2T	**Selects CQ APB 2T** 0: CQ issues 1T write. 1: CQ issues 2T write.
15	CQ0_D_EN	**Enables CQ0**
11	CQ0B_D_EN	**Enables CQ0B (for pass1 module)**
10	CQ0C_D_EN	**Enables CQ0C (for pass1 module)** For IMGO or IMG2O for frame buffer control. It must be continuous mode. IMGO or IM2O is selected by CQ0C_IMGO_SEL and CQ0C_IMG2O_SEL.
9	CQ0B_D_MODE	**CQ0B_MODE** 0: Trigger wait pass1 frame done 1T: Trigger immediately
8	CQ0C_D_RRZO_SEL	**Selects CQ0C trigger source** 0: Disable 1: From RRZO
7	CQ0_D_MODE	**CQ0_MODE** 0: Trigger wait pass1 frame done 1: Trigger immediately
6	CQ0B_D_SEL	**Selects CQ0B trigger source** 0: From IMG2O 1: From pass1_done
5	CQ0C_IMGO_D_S	**Selects CQ0C trigger source**

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Bit(s)	Name	Description
	EL	0: Disable 1: From IMGO
4	CQ0B_CONT_D	0: CQ0B loads APB CMD by CQ0_TRIGGER. 1: CQ0B automatically loads APB CMD at pass1 done.
3	CQ0_CONT_D	0: CQ0 loads APB CMD by CQ0_TRIGGER. 1: CQ0 automatically loads APB CMD at pass1 done.
2	CQ0A_MASK_CQ0C_D_EN	**CQ0A can mask CQ0C trigger.**
1	CQ0A_MASK_CQ0B_D_EN	**CQ0A can mask CQ0B trigger.**

15004024 **CAM_CTL_SCENARIO** **Scenario** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name										SUB_MODE				SCENARIO		
Type										RW				RW		
Reset										0	0	0		0	0	0

Bit(s)	Name	Description
6:4	SUB_MODE	0: RAW sensor 1: YUV sensor 2: RGB sensor 3: JPG sensor
2:0	SCENARIO	3: IP 6: CC Others: Reserved

15004028 **CAM_CTL_FMT_SEL_P1** **ISP Format Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			TG1_SW			TWO_PIX_DMX	TWO_PIX_RMX	TWO_PIX	TWO_PIX_BMX					TG1_FMT		
Type			RW			RW	RW	RW	RW					RW		
Reset			0	0		0	0	0	0					0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	OUT_FMT										PAKG_FMT				PIX_ID	
Type	RW										RW				RW	
Reset	0	0	0	0							0	0			0	0

Bit(s)	Name	Description
29:28	TG1_SW	**Bit 0 is YC swap; bit 1 is UV or RB swap.** For YUV format, LSB to MSB: 0: UYVY

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Bit(s)	Name	Description
		1: YUYV 2: VYUY 3: YVYU For RGB format: 0, 1: RGB 2, 3: BGR
26	TWO_PIX_DMX	**Two pix sel** For DMX out. Must be set to 0 at dual raw in non-dual sensor mode; can be set to 0 or 1. If set to 1, WBN must operate in HBIN mode to reduce pipe pix rate. It is legacy design for HBIN usage.
25	TWO_PIX_RMX	**Two pix sel** For SGG2 and PAKG
24	TWO_PIX	**Two pix sel** For TG1
23	TWO_PIX_BMX	**Two pix sel** For BMX
18:16	TG1_FMT	**TG1 format** 3'h0: RAW 8 bits 3'h1: RAW 10 bits 3'h2: RAW 12 bits 3'h3: YUV422 3'h4: RAW 14 bits 3'h5: RGB565 3'h6: RGB888 3'h7: JPEG format
15:12	OUT_FMT	**Pass 1 path output format** If the output format is YUV, 0: Reserved 1: Reserved 2: 422 1 plane 3: Reserved If the output format is RGB, 0: RGB565 1: RGB888 2: Reserved If the output format is Bayer, 0: Bayer 8 1: Bayer 10 2: Bayer 12 3: Bayer 14 (SW) Others: Reserved It controls IMGO output format.
5:4	PAKG_FMT	**PAKG_FMT** 0: 8 1: 10 2: 12
1:0	PIX_ID	**Bayer sequence** For RAW and RGB module. If TG_PIX_ID_EN=1, it means pass2 pix_id; if TG_PIX_ID_EN=0, it means both pass1/pass2 pix_id. 0: B Gb Gr R 1: Gb B R Gr 2: Gr R B Gb 3: R Gr Gb B

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1500402C **CAM_CTL_FMT_SEL_P1_D** **ISP Format Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			TG1_SW_D			TWO_PIX_DMX_D	TWO_PIX_RMX_D	TWO_PIX_D	TWO_PIX_BMX_D					TG1_FMT_D		
Type			RW			RW	RW	RW	RW					RW		
Reset			0	0		0	0	0	0					0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	OUT_FMT_D										PAKG_FMT_D				PIX_ID_D	
Type	RW										RW				RW	
Reset	0	0	0	0							0	0			0	0

Bit(s)	Name	Description
29:28	TG1_SW_D	**Bit 0 is YC swap; bit 1 is UV or RB swap.** For YUV format, LSB to MSB: 0: UYVY 1: YUYV 2: VYUY 3: YVYU For RGB format: 0, 1: RGB 2, 3: BGR
26	TWO_PIX_DMX_D	**Two pix sel** For DMX out. Must be set to 0 at dual raw in non-dual sensor mode. Can be set to 0 or 1. If set to 1, WBN must operate in HBIN mode to reduce pipe pix rate. It is legacy design for HBIN usage.
25	TWO_PIX_RMX_D	**Two pix sel** For SGG2 and PAKG
24	TWO_PIX_D	**Two pix sel** For TG1
23	TWO_PIX_BMX_D	**Two pix sel** For BMX
18:16	TG1_FMT_D	**TG1 format** 3'h0: RAW 8 bits 3'h1: RAW 10 bits 3'h2: RAW 12 bits 3'h3: YUV422 3'h4: RAW 14 bits 3'h5:RGB565 3'h6: RGB888 3'h7: JPEG format
15:12	OUT_FMT_D	**Pass 1 path output format** If the output format is YUV, 0: Reserved 1: Reserved 2: 422 1 plane 3: Reserved If the output format is RGB, 0: RGB565 1: RGB888 2: Reserved If the output format is Bayer, 0: Bayer 8

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Bit(s)	Name	Description
		1: Bayer 10 2: Bayer 12 3: Bayer 14 (SW) Others: Reserved It controls IMGO output format.
5:4	PAKG_FMT_D	**PAKG_FMT** 0: 8 1: 10 2: 12
1:0	PIX_ID_D	**Bayer sequence** For RAW and RGB module. If TG_PIX_ID_EN=1, it means pass2 pix_id; if TG_PIX_ID_EN=0, it means both pass1/pass2 pix_id. 0: B Gb Gr R 1: Gb B R Gr 2: Gr R B Gb 3: R Gr Gb B

15004030 **CAM_CTL_FMT_SEL_P2** **IN_FMT** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																FG_MODE
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PIX_ID_P2			UFDI_FMT		VIPI_FMT				IMG3O_FMT			IN_FMT			
Type	RW			RW		RW				RW			RW			
Reset	0	0		0		0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
16	FG_MODE	**Full G format**
15:14	PIX_ID_P2	**Bayer sequence** For RAW and RGB module. If TG_PIX_ID_EN=1, it means pass2 pix_id; if TG_PIX_ID_EN=0, it means both pass1/pass2 pix_id. 0: B Gb Gr R 1: Gb B R Gr 2: Gr R B Gb 3: R Gr Gb B
12	UFDI_FMT	0: UFO length table 1: Weighting table
10:8	VIPI_FMT	**VIPI format** 0: 420 3 plane 1: 420 2 plane 2: 422 1 plane 3: MFB Lowlight/Postblend (vip3i: weighting table) 4: MFB Multimotion (vip3i: 422 1 plane)
6:4	IMG3O_FMT	**IMG3O format** 0: 420 3plane 1: 4202 plane 2: 422 1 plane
3:0	IN_FMT	**Pass2 path input format**

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Bit(s)	Name	Description
		If pass2 is YUV input, 422 1 plane (IMGI) If pass2 is RGB input, 0: RGB565 1: RGB888 2: XRGB8888 3: RGB101010 (RGB format (RGBC, iHDR), MSB align) 4: RGB121212 (RGB format (RGBC, iHDR), MSB align) If pass2 is Bayer, 0: Bayer 8, 1: Bayer10 2: Bayer12 3: Bayer14 Others: Reserved It controls input format.

15004034 **CAM_CTL_SEL_P1** **ISP Selection for P1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				W2G_SEL	EIS_SEL		UFE_SEL			IMG_SEL	LCS_SEL_EN	LCS_SEL	SGG_SEL_EN	SGG_SEL		
Type				RW	RW		RW			RW	RW	RW	RW	RW		
Reset				0	0	0	0	0		0	0	0	0	0	0	

Bit(s)	Name	Description
12	W2G_SEL	**W2GSEL** 0: PGN from RRZ, bayer sensor case 1: RGN from W2G, RGBC sensor case
11:10	EIS_SEL	0: From BMX 1: From BIN 2: From RMX
9:8	UFE_SEL	0: From pak 1: From UFE
6	IMG_SEL	0: From LSC (BMX) 1: From TG
5	LCS_SEL_EN	**Enables LCS sel**
4	LCS_SEL	**LCS_SEL** Only works when LCS_SEL_EN=1. 0: For SOC sensor 1: For RAW sensor
3	SGG_SEL_EN	**Enables sgg sel**
2:1	SGG_SEL	**SGG_SEL** Only works when SGG_SEL_EN=1. 0: For SOC sensor 1: For RAW sensor 2: From RMX

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15004038 **CAM_CTL_SEL_P1_D** **ISP Selection for P1 D** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				W2G_SEL_D	EIS_SEL_D		UFE_SEL_D			IMG_SEL_D	LCS_SEL_EN_D	LCS_SEL_D	SGG_SEL_EN_D	SGG_SEL_D		
Type				RW	RW		RW			RW	RW	RW	RW	RW		
Reset				0	0	0	0	0		0	0	0	0	0	0	

Bit(s)	Name	Description
12	W2G_SEL_D	**W2GSEL** 0: PGN from RRZ, bayer sensor case 1: RGN from W2G, RGBC sensor case
11:10	EIS_SEL_D	0: From BMX 1: From BIN 2: From RMX
9:8	UFE_SEL_D	0: From pak 1: From UFE
6	IMG_SEL_D	0: From LSC (BMX) 1: From TG
5	LCS_SEL_EN_D	**Enables LCS sel**
4	LCS_SEL_D	**LCS_SEL** Only works when LCS_SEL_EN=1. 0: For SOC sensor 1: For RAW sensor
3	SGG_SEL_EN_D	**Enables SGG sel**
2:1	SGG_SEL_D	**SGG_SEL** Only works when SGG_SEL_EN=1. 0: For SOC sensor 1: For RAW sensor 2: From RMX

1500403C **CAM_CTL_SEL_P2** **ISP Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name		MFB_MODE	PCA_SEL	FE_SEL	MDP_SEL	NR3D_SEL	CRZ_SEL		MIX1_SEL	SRZ1_SEL	C24_SEL	UFD_SEL	G2G_SEL_EN	G2G_SEL	CCL_SEL_EN	CCL_SEL
Type		RW	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14	MFB_MODE	**SRAM mux MFB mode**

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Bit(s)	Name	Description
13	PCA_SEL	0: PCA from mix1 1: PCA from co2
12	FE_SEL	0: From after CRZ 1: From before CRZ
11	MDP_SEL	0: From after CRZ 1: From before CRZ
10	NR3D_SEL	0: From CRZ 1: From LCE
9:8	CRZ_SEL	0: From LCE 1: From NBC 2: Form NR3D
7	MIX1_SEL	0: From NBC 1: From CRZ
6	SRZ1_SEL	0: From DMA 1: From FE
5	C24_SEL	0: From IMGI 1: From MFB
4	UFD_SEL	0: From UNP 1: From UFD
3	G2G_SEL_EN	**G2G_SEL_EN**
2	G2G_SEL	**G2G_SEL** Only works when G2G_SEL_EN=1. 0: From IMGI (YUV sensor) 1: From CFA (RAW sensor)
1	CCL_SEL_EN	**Enables CCL sel**
0	CCL_SEL	**CCL_SEL** Only works whenCCL_SEL_EN=1. 0: FromCFA (RAW sensor) 1: From IMGI (RGB sensor)

15004040 **CAM_CTL_SEL_GLOBAL** **ISP Selection GLOBAL** **00000003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												W2G_MODE_D	LSC_EARLY_SOF_EN_D	PREGAIN_SEL_EN_D	PREGAIN_SEL_D	BIN_SEL_EN_D
Type												RW	W1	RW	RW	RW
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIN_SEL_D	INT_MRG			W2G_MODE	LSC_EARLY_SOF_EN	PREGAIN_SEL_EN	PREGAIN_SEL	BIN_SEL_EN	BIN_SEL	DUAL_MODE		APB_CLK_GATE_BYPASS		PASS1_D_DB_EN	PASS1_DB_EN
Type	RW	RW			RW	W1	RW	RW	RW	RW	RW		RW		RW	RW
Reset	0	0			0	0	0	0	0	0	0		0		1	1

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Bit(s)	Name	Description
20	W2G_MODE_D	**SRAM mux W2G mode (dual raw)**
19	LSC_EARLY_SOF_EN_D	**Enables LSC early SOF (dual raw)** 0: Normal case 1: Enable early LSC early SOF. It affects LSCI and LSC SOF/db_load. The priority is higher than LSCI_SOF_SEL_EN.
18	PREGAIN_SEL_EN_D	**Enables PREGAIN_SEL (dual raw)**
17	PREGAIN_SEL_D	**PREGAIN_SEL (dual raw)** Only works when PREGGAIN_SEL_EN=1. 0: From RRZ (CC) 1: From IMGI (IP)
16	BIN_SEL_EN_D	**Enables BIN_SEL (dual raw)**
15	BIN_SEL_D	**BIN_SEL (dual raw)** Only works when BIN_SEL_EN=1. 0: From TG (CC) 1: From DMA (IP)
14	INT_MRG	**Merges interrupt**
11	W2G_MODE	**SRAM mux W2G mode**
10	LSC_EARLY_SOF_EN	**Enables LSC early SOF** 0: Normal case 1: Enable early LSC early SOF. It affects LSCI and LSC SOF/db_load. The priority is higher than LSCI_SOF_SEL_EN.
9	PREGAIN_SEL_EN	**Enables PREGAIN_SEL**
8	PREGAIN_SEL	**PREGAIN_SEL** Only works when PREGGAIN_SEL_EN=1. 0: From RRZ (CC) 1: From IMGI (IP)
7	BIN_SEL_EN	**Enables BIN_SEL**
6	BIN_SEL	**BIN_SEL** Only works when BIN_SEL_EN=1. 0: From TG (CC) 1: From DMA (IP)
5	DUAL_MODE	0: Disable dual raw 1: Enable dual raw
3	APB_CLK_GATE_BYPASS	**Bypasses APB clock gating** 1: Always turn on APB clock
1	PASS1_D_DB_EN	**Enables Pass1 _D module double buffer**
0	PASS1_DB_EN	**Enables Pass1 module double buffer**

15004048 **CAM_CTL_INT_P1_EN** **ISP Interrupt Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_WCLR_EN	DMA_ERR_EN		FBC_IMGO_DON_EN	FBC_RRZO_DON_EN	LSC_ERR_EN	FLK_ERR_EN	ESFKO_ERR_EN	RRZO_ERR_EN	LCSO_ERR_EN	AAO_ERR_EN	IMGO_ERR_EN			FLK_DON_EN	AF_DON_EN
Type	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW			RW	RW
Reset	0	0		0	0	0	0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				SOF1_IN		PASS1_	RRZO_D	IMGO_D	CQ0_VS	CQ0_ER	TG1_GB	TG1_ER	EXP DON	TG1_IN	TG1_IN	VS1_INT

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				T_EN		DON_EN	ROP_FRAME_EN	ROP_FRAME_EN	_ERR_EN	R_EN	ERR_EN	R_EN	1_EN	T2_EN	T1_EN	_EN
Type				RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	INT_WCLR_EN	0: Read clear 1: Interrupt writes 1 to clear.
30	DMA_ERR_EN	Enables DMA error
28	FBC_IMGO_DON_EN	Enables FBC IMGO done interrupt
27	FBC_RRZO_DON_EN	Enables FBC RRZO done interrupt
26	LSC_ERR_EN	Enables LSC error interrupt
25	FLK_ERR_EN	Enables Flicker error interrupt
24	ESFKO_ERR_EN	Enables ESFKO error interrupt
23	RRZO_ERR_EN	Enables IMG2O error interrupt
22	LCSO_ERR_EN	Enables LCSO error interrupt
21	AAO_ERR_EN	Enables AEerror interrupt
20	IMGO_ERR_EN	Enables IMGO overrun interrupt
17	FLK_DON_EN	Enables Flicker end interrupt
16	AF_DON_EN	Enables AF done interrupt interrupt
12	SOF1_INT_EN	Enables TG1 SOF interrupt
10	PASS1_DON_EN	Enables PASS1 DONE interrupt
9	RRZO_DROP_FRAME_EN	Enables RRZO drop frame status
8	IMGO_DROP_FRAME_EN	Enables IMGO drop frame status
7	CQ0_VS_ERR_EN	CQ0 cover next vsync error
6	CQ0_ERR_EN	**CQ0_ERR_ST** 1: Syntax error
5	TG1_GBERR_EN	TG grab error status
4	TG1_ERR_EN	Enables TG1 ERR
3	EXPDON1_EN	Enables Exposusre1 done interrupt
2	TG1_INT2_EN	Enables TG1 interrupt2
1	TG1_INT1_EN	Enables TG1 interrupt1
0	VS1_INT_EN	Enables Vsync1 interrupt

1500404C **CAM_CTL_INT_P1_STATUS** **ISP Interrupt Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DMA_ERR_ST		FBC_IMGO_DON_ST	FBC_RRZO_DON_ST	LSC_ERR_ST	FLK_ERR_ST	ESFKO_ERR_ST	RRZO_ERR_ST	LCSO_ERR_ST	AAO_ERR_ST	IMGO_ERR_ST			FLK_DON_ST	AF_DON_ST
Type		RU		RU	RU	RU	RU	RU	RU	RU	RU	RU			RU	RU

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Reset		0		0	0	0	0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**SOF1_INT_ST**		**PASS1_DON_ST**	**RRZO_DROP_FRAME_ST**	**IMGO_DROP_FRAME_ST**	**CQ0_VS_ERR_ST**	**CQ0_ERR**	**TG1_GBERR**	**TG1_ERR_ST**	**EXPDON1_ST**	**TG1_INT2_ST**	**TG1_INT1_ST**	**VS1_INT_ST**
Type				RU		RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset				0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30	DMA_ERR_ST	DMA error status
28	FBC_IMGO_DON_ST	FBC IMGO DONE status
27	FBC_RRZO_DON_ST	FBC RRZO done status
26	LSC_ERR_ST	LSC error status
25	FLK_ERR_ST	Flicker error status
24	ESFKO_ERR_ST	ESFKO error status
23	RRZO_ERR_ST	IMG2O error status
22	LCSO_ERR_ST	LCSO error status
21	AAO_ERR_ST	AEerror status
20	IMGO_ERR_ST	IMGO overrun status
17	FLK_DON_ST	Flicker end status
16	AF_DON_ST	AF done interrupt status
12	SOF1_INT_ST	TG1 SOF interrupt status
10	PASS1_DON_ST	**PASS1 done interrupt status** Only for stereo mode
9	RRZO_DROP_FRAME_ST	RRZO drop frame status
8	IMGO_DROP_FRAME_ST	IMGO drop frame status
7	CQ0_VS_ERR_ST	CQ0 cover next vsync error
6	CQ0_ERR	CQ0_ERR
5	TG1_GBERR	TG1_GBERR
4	TG1_ERR_ST	**TG1 ERR status** 1: TG overrun occurs. The normal hint bandwidth is not enough.
3	EXPDON1_ST	Exposusre1 done interrupt status
2	TG1_INT2_ST	TG1 interrupt2 status
1	TG1_INT1_ST	TG1 interrupt1 status
0	VS1_INT_ST	Vsync1 interrupt status

15004050 **CAM_CTL_INT_P1_EN2** **CTL_DMA_INT** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name		CQ0C_DONE_ST_EN	CQ0B_DONE_ST_EN	CQ0_DONE_ST_EN	AF_FLO3_DONE_ST_EN	AF_FLO2_DONE_ST_EN	AF_FLO1_DONE_ST_EN	AF_TAR_DONE_ST_EN	LSCI_DONE_ST_EN	BPCI_DONE_ST_EN	AAO_DONE_ST_EN	LCSO_DONE_ST_EN	ESFKO_DONE_ST_EN	RRZO_DONE_ST_EN	UFEO_DONE_ST_EN	IMGO_DONE_ST_EN
Type		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14	CQ0C_DONE_ST_EN	CQ0C_DONE_EN
13	CQ0B_DONE_ST_EN	CQ0B_DONE_EN
12	CQ0_DONE_ST_EN	CQ0_DONE_EN
11	AF_FLO3_DONE_ST_EN	AF_FLO3_DONE_ST_EN
10	AF_FLO2_DONE_ST_EN	AF_FLO2_DONE_ST_EN
9	AF_FLO1_DONE_ST_EN	AF_FLO1_DONE_ST_EN
8	AF_TAR_DONE_ST_EN	AF_TAR_DONE_ST_EN
7	LSCI_DONE_ST_EN	LSCI_DONE_ST_EN
6	BPCI_DONE_ST_EN	BPCI_DONE_ST_EN
5	AAO_DONE_ST_EN	AAO_DONE_ST_EN
4	LCSO_DONE_ST_EN	LCSO_DONE_ST_EN
3	ESFKO_DONE_ST_EN	ESFKO_DONE_ST_EN
2	RRZO_DONE_ST_EN	RRZO_DONE_ST_EN
1	UFEO_DONE_ST_EN	UFEO_DONE_ST_EN
0	IMGO_DONE_ST_EN	IMGO_DONE_ST_EN

15004054 CAM_CTL_INT_P1_STATUS2 CTL_INT_STATUS2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CQ0C_DONE_ST	CQ0B_DONE_ST	CQ0_DONE_ST	AF_FLO3_DONE_ST	AF_FLO2_DONE_ST	AF_FLO1_DONE_ST	AF_TAR_DONE_ST	LSCI_DONE_ST	BPCI_DONE_ST	AAO_DONE_ST	LCSO_DONE_ST	ESFKO_DONE_ST	RRZO_DONE_ST	UFEO_DONE_ST	IMGO_DONE_ST
Type		RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU

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Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14	CQ0C_DONE_ST	CQ0C_DONE_ST
13	CQ0B_DONE_ST	CQ0B_DONE_ST
12	CQ0_DONE_ST	CQ0_DONE_ST
11	AF_FLO3_DONE_ST	AF_FLO3_DONE_ST
10	AF_FLO2_DONE_ST	AF_FLO2_DONE_ST
9	AF_FLO1_DONE_ST	AF_FLO1_DONE_ST
8	AF_TAR_DONE_ST	AF_TAR_DONE_ST
7	LSCI_DONE_ST	LSCI_DONE_ST
6	BPCI_DONE_ST	BPCI_DONE_ST
5	AAO_DONE_ST	AAO_DONE_ST
4	LCSO_DONE_ST	LCSO_DONE_ST
3	ESFKO_DONE_ST	ESFKO_DONE_ST
2	RRZO_DONE_ST	RRZO_DONE_ST
1	UFEO_DONE_ST	UFEO_DONE_ST
0	IMGO_DONE_ST	IMGO_DONE_ST

15004058 **CAM_CTL_INT_P1_EN_D** **ISP Interrupt Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DMA_ERR_EN		FBC_IMGO_DON_EN	FBC_RRZO_DON_EN	LSC_ERR_EN		AFO_ERR_EN	RRZO_ERR_EN	LCSO_ERR_EN	AAO_ERR_EN	IMGO_ERR_EN				AF_DON_EN
Type		RW		RW	RW	RW		RW	RW	RW	RW	RW				RW
Reset		0		0	0	0		0	0	0	0	0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				SOF1_INT_EN		PASS1_DON_EN	RRZO_DROP_FRAME_EN	IMGO_DROP_FRAME_EN	CQ0_VS_ERR_EN	CQ0_ERR_EN	TG1_GBERR_EN	TG1_ERR_EN	EXPDON1_EN	TG1_INT2_EN	TG1_INT1_EN	VS1_INT_EN
Type				RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30	DMA_ERR_EN	Enables DMA error
28	FBC_IMGO_DON_EN	Enables FBC IMGO done interrupt
27	FBC_RRZO_DON_EN	Enables FBC RRZO done interrupt
26	LSC_ERR_EN	Enables LSC error interrupt
24	AFO_ERR_EN	Enables AFO error interrupt

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Bit(s)	Name	Description
23	RRZO_ERR_EN	Enables IMG2O error interrupt
22	LCSO_ERR_EN	Enables LCSO error interrupt
21	AAO_ERR_EN	Enables AEerror interrupt
20	IMGO_ERR_EN	Enables IMGO overrun interrupt
16	AF_DON_EN	Enables AF done interrupt interrupt
12	SOF1_INT_EN	Enables TG1 SOF interrupt
10	PASS1_DON_EN	Enables PASS1 DONE interrupt
9	RRZO_DROP_FRAME_EN	Enables RRZO drop frame status
8	IMGO_DROP_FRAME_EN	Enables IMGO drop frame status
7	CQ0_VS_ERR_EN	CQ0 cover next vsync error
6	CQ0_ERR_EN	**CQ0_ERR_ST** 1: Syntax error
5	TG1_GBERR_EN	TG grab error status
4	TG1_ERR_EN	Enables TG1 ERR
3	EXPDON1_EN	Enables Exposusre1 done interrupt
2	TG1_INT2_EN	Enables TG1 interrupt2
1	TG1_INT1_EN	Enables TG1 interrupt1
0	VS1_INT_EN	Enables Vsync1 interrupt

1500405C **CAM_CTL_INT_P1_STATUS_D** **ISP Interrupt Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DMA_ERR_ST		FBC_IMGO_DON_ST	FBC_RRZO_DON_ST	LSC_ERR_ST		AFO_ERR_ST	RRZO_ERR_ST	LCSO_ERR_ST	AAO_ERR_ST	IMGO_ERR_ST				AF_DON_ST
Type		RU		RU	RU	RU		RU	RU	RU	RU	RU				RU
Reset		0		0	0	0		0	0	0	0	0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				SOF1_INT_ST		PASS1_DON_ST	RRZO_DROP_FRAME_ST	IMGO_DROP_FRAME_ST	CQ0_VS_ERR_ST	CQ0_ERR	TG1_GBERR	TG1_ERR_ST	EXPDON1_ST	TG1_INT2_ST	TG1_INT1_ST	VS1_INT_ST
Type				RU		RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset				0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30	DMA_ERR_ST	DMA error status
28	FBC_IMGO_DON_ST	FBC_IMGO_DON_ST
27	FBC_RRZO_DON_ST	FBC RRZO DON status
26	LSC_ERR_ST	LSC error status
24	AFO_ERR_ST	AFO error status

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Bit(s)	Name	Description
23	RRZO_ERR_ST	IMG2O error status
22	LCSO_ERR_ST	LCSO error status
21	AAO_ERR_ST	AEerror status
20	IMGO_ERR_ST	IMGO overrun status
16	AF_DON_ST	AF done interrupt status
12	SOF1_INT_ST	TG1 SOF interrupt status
10	PASS1_DON_ST	**PASS1 done interrupt status** Only for stereo mode
9	RRZO_DROP_FRAME_ST	RRZO drop frame status
8	IMGO_DROP_FRAME_ST	IMGO drop frame status
7	CQ0_VS_ERR_ST	CQ0 cover next vsync error
6	CQ0_ERR	CQ0_ERR
5	TG1_GBERR	TG1_GBERR
4	TG1_ERR_ST	**TG1 ERR status** 1: TG overrun occurs. The normal hint bandwidth is not enough.
3	EXPDON1_ST	Exposusre1 done interrupt status
2	TG1_INT2_ST	TG1 interrupt2 status
1	TG1_INT1_ST	TG1 interrupt1 status
0	VS1_INT_ST	Vsync1 interrupt status

15004060 **CAM_CTL_INT_P1_EN2_D** **CTL_DMA_INT** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**CQ0C_DONE_ST_EN**	**CQ0B_DONE_ST_EN**	**CQ0_DONE_ST_EN**	**AF_FLO3_DONE_EN**	**AF_FLO2_DONE_EN**	**AF_FLO1_DONE_EN**	**AF_TAR_DONE_EN**	**LSCI_D_DONE_ST_EN**	**BPCI_D_DONE_ST_EN**	**AAO_D_DONE_ST_EN**	**LCSO_D_DONE_ST_EN**	**AFO_D_DONE_ST_EN**	**RRZO_D_DONE_ST_EN**		**IMGO_D_DONE_ST_EN**
Type		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0		0

Bit(s)	Name	Description
14	CQ0C_DONE_ST_EN	CQ0C_DONE_EN
13	CQ0B_DONE_ST_EN	CQ0B_DONE_EN
12	CQ0_DONE_ST_EN	CQ0_DONE_EN
11	AF_FLO3_DONE_EN	AF_FLO3_DONE_EN
10	AF_FLO2_DONE_EN	AF_FLO2_DONE_EN

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Bit(s)	Name	Description
9	AF_FLO1_DONE_EN	AF_FLO1_DONE_EN
8	AF_TAR_DONE_EN	AF_TAR_DONE_EN
7	LSCI_D_DONE_ST_EN	LSCI_D_DONE_ST_EN
6	BPCI_D_DONE_ST_EN	BPCI_D_DONE_ST_EN
5	AAO_D_DONE_ST_EN	AAO_D_DONE_ST_EN
4	LCSO_D_DONE_ST_EN	LCSO_D_DONE_ST_EN
3	AFO_D_DONE_ST_EN	AFO_D_DONE_ST_EN
2	RRZO_D_DONE_ST_EN	RRZO_D_DONE_ST_EN
0	IMGO_D_DONE_ST_EN	IMGO_D_DONE_ST_EN

15004064	CAM_CTL_INT_P1_STATUS2_D	CTL_INT_STATUS2	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CQ0C_DONE_ST	CQ0B_DONE_ST	CQ0_DONE_ST	AF_FLO3_DONE_ST	AF_FLO2_DONE_ST	AF_FLO1_DONE_ST	AF_TAR_DONE_ST	LSCI_D_DONE_ST	BPCI_D_DONE_ST	AAO_D_DONE_ST	LCSO_D_DONE_ST	AFO_D_DONE_ST	RRZO_D_DONE_ST		IMGO_D_DONE_ST
Type		RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU		RU
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0		0

Bit(s)	Name	Description
14	CQ0C_DONE_ST	CQ0C_DONE_ST
13	CQ0B_DONE_ST	CQ0B_DONE_ST
12	CQ0_DONE_ST	CQ0_DONE_ST
11	AF_FLO3_DONE_ST	AF_FLO3_DONE_ST
10	AF_FLO2_DONE_ST	AF_FLO2_DONE_ST
9	AF_FLO1_DONE_ST	AF_FLO1_DONE_ST
8	AF_TAR_DONE_ST	AF_TAR_DONE_ST
7	LSCI_D_DONE_ST	LSCI_D_DONE_ST
6	BPCI_D_DONE_ST	BPCI_D_DONE_ST
5	AAO_D_DONE_ST	AAO_D_DONE_ST
4	LCSO_D_DONE_ST	LCSO_D_DONE_ST

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Bit(s)	Name	Description
3	AFO_D_DONE_ST	AFO_D_DONE_ST
2	RRZO_D_DONE_ST	RRZO_D_DONE_ST
0	IMGO_D_DONE_ST	IMGO_D_DONE_ST

15004068 **CAM_CTL_INT_P2_EN** **CTL_INT_P2_EN** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			PCA_COLLISION_ST_EN	GGM_COLLISION_ST_EN	DMA_ERR_EN	FEO_DONE_ST_EN	IMG3CO_DONE_ST_EN	IMG3BO_DONE_ST_EN	IMG3O_DONE_ST_EN	IMG2O_DONE_ST_EN	MFBO_DONE_ST_EN	LCEI_DONE_ST_EN	VIP3I_DONE_ST_EN	VIP2I_DONE_ST_EN	VIPI_DONE_ST_EN	UFDI_DONE_ST_EN
Type			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IMGI_DONE_ST_EN		PASS2C_ERR_TRIG_ST_EN	PASS2B_ERR_TRIG_ST_EN	PASS2A_ERR_TRIG_ST_EN	CQ3_DONE_ST_EN	CQ2_DONE_ST_EN	CQ1_DONE_ST_EN	PASS2C_DONE_ST_EN	PASS2B_DONE_ST_EN	PASS2A_DONE_ST_EN	TDR_ERR_EN	CQ_DON_EN	TPIPE_DON_EN	PASS2_DON_EN	CQ_ERR_EN
Type	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29	PCA_COLLISION_ST_EN	PCA_COLLISION_ST_EN
28	GGM_COLLISION_ST_EN	GGM_COLLISION_ST_EN
27	DMA_ERR_EN	Enables DMA error
26	FEO_DONE_ST_EN	FEO_DONE_ST_EN
25	IMG3CO_DONE_ST_EN	IMG3CO_DONE_ST_EN
24	IMG3BO_DONE_ST_EN	IMG3BO_DONE_ST_EN
23	IMG3O_DONE_ST_EN	IMG3O_DONE_ST_EN
22	IMG2O_DONE_ST_EN	IMG2O_DONE_ST_EN
21	MFBO_DONE_ST_EN	MFBO_DONE_ST_EN
20	LCEI_DONE_ST_EN	LCEI_DONE_ST_EN
19	VIP3I_DONE_ST_EN	VIP3I_DONE_ST_EN
18	VIP2I_DONE_ST_EN	VIP2I_DONE_ST_EN

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Bit(s)	Name	Description
17	VIPI_DONE_ST_EN	VIPI_DONE_ST_EN
16	UFDI_DONE_ST_EN	UFDI_DONE_ST_EN
15	IMGI_DONE_ST_EN	IMGI_DONE_ST_EN
13	PASS2C_ERR_TRIG_ST_EN	Enables PASS2C error trigger interrupt
12	PASS2B_ERR_TRIG_ST_EN	Enables PASS2B error trigger interrupt
11	PASS2A_ERR_TRIG_ST_EN	Enables PASS2A error trigger interrupt
10	CQ3_DONE_ST_EN	Enables CQ3 load done interrupt
9	CQ2_DONE_ST_EN	Enables CQ2 load done interrupt
8	CQ1_DONE_ST_EN	Enables CQ1 load done interrupt
7	PASS2C_DONE_ST_EN	Enables CQ Pass2 C done interrurp
6	PASS2B_DONE_ST_EN	Enables CQ Pass2 B done interrurp
5	PASS2A_DONE_ST_EN	Enables CQ Pass2 A done interrurp
4	TDR_ERR_EN	TDR error interrupt
3	CQ_DON_EN	Enables CQ error finished interrupt
2	TPIPE_DON_EN	Enables TPIPE done interrupt
1	PASS2_DON_EN	Enables Pass2 done interrupt
0	CQ_ERR_EN	Enables command queue error interrrupt

1500406C	CAM_CTL_INT_P2_STATUS	CTL_INT_P2_STATUS	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			PCA_COLLISION_ST	GGM_COLLISION_ST	DMA_ERR_ST	FEO_DONE_ST	IMG3CO_DONE_ST	IMG3BO_DONE_ST	IMG3O_DONE_ST	IMG2O_DONE_ST	MFBO_DONE_ST	LCEI_DONE_ST	VIP3I_DONE_ST	VIP2I_DONE_ST	VIPI_DONE_ST	UFDI_DONE_ST
Type			RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IMGI_DONE_ST		PASS2C_ERR_TRIG_ST	PASS2B_ERR_TRIG_ST	PASS2A_ERR_TRIG_ST	CQ3_DONE_ST	CQ2_DONE_ST	CQ1_DONE_ST	PASS2C_DONE_ST	PASS2B_DONE_ST	PASS2A_DONE_ST	TDR_ERR_ST	CQ_DON_ST	TPIPE_DONE_ST	PASS2_DON_ST	CQ_ERR_ST
Type	RU		RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
29	PCA_COLLISION_ST	PCA_COLLISION_ST
28	GGM_COLLISION_ST	GGM_COLLISION_ST
27	DMA_ERR_ST	DMA error status
26	FEO_DONE_ST	FEO_DONE_ST
25	IMG3CO_DONE_ST	IMG3CO_DONE_ST
24	IMG3BO_DONE_ST	IMG3BO_DONE_ST
23	IMG3O_DONE_ST	IMG3O_DONE_ST
22	IMG2O_DONE_ST	IMG2O_DONE_ST
21	MFBO_DONE_ST	MFBO_DONE_ST
20	LCEI_DONE_ST	LCEI_DONE_ST
19	VIP3I_DONE_ST	VIP3I_DONE_ST
18	VIP2I_DONE_ST	VIP2I_DONE_ST
17	VIPI_DONE_ST	VIPI_DONE_ST
16	UFDI_DONE_ST	UFDI_DONE_ST
15	IMGI_DONE_ST	IMGI_DONE_ST
13	PASS2C_ERR_TRIG_ST	PASS2C error trigger interrupt status
12	PASS2B_ERR_TRIG_ST	PASS2B error trigger interrupt status
11	PASS2A_ERR_TRIG_ST	PASS2A error trigger interrupt status
10	CQ3_DONE_ST	CQ3 load done interrupt status
9	CQ2_DONE_ST	CQ2 load done interrupt status
8	CQ1_DONE_ST	CQ1 load done interrupt status
7	PASS2C_DONE_ST	CQ Pass2 C done status
6	PASS2B_DONE_ST	CQ Pass2 B done status
5	PASS2A_DONE_ST	CQ Pass2 A done status
4	TDR_ERR_ST	TDR error status
3	CQ_DON_ST	CQ load finished time is after ISP start status
2	TPIPE_DON_ST	TPIPE done status
1	PASS2_DON_ST	PASS2 done status
0	CQ_ERR_ST	CQ Err status done status

15004070 **CAM_CTL_INT_STATUSX** **ISP Interrupt Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DMA_ERR_ST		FBC_IMGO_DONE_ST	FBC_RRZO_DONE_ST	LSC_ERR_ST	FLK_ERR_ST	ESFKO_ERR_ST	RRZO_ERR_ST	LCSO_ERR_ST	AAO_ERR_ST	IMGO_ERR_ST	CQ_DON_ST		FLK_DON_ST	AF_DON_ST
Type		RU		RU	RU	RU	RU	RU	RU	RU	RU	RU	RU		RU	RU
Reset		0		0	0	0	0	0	0	0	0	0	0		0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TPIPE_DON_ST	PASS2_DON_ST	CQ_ERR_ST	SOF1_INT_ST		PASS1_DON_ST	RRZO_DROP_FRAME_ST	IMGO_DROP_FRAME_ST	CQ0_VS_ERR_ST	CQ0_ERR	TG1_GBERR	TG1_ERR_ST	EXPDON1_ST	TG1_INT2_ST	TG1_INT1_ST	VS1_INT_ST
Type	RU	RU	RU	RU		RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30	DMA_ERR_ST	DMA error status
28	FBC_IMGO_DON_ST	FBC IMGO done status
27	FBC_RRZO_DON_ST	FBC RRZO done status
26	LSC_ERR_ST	LSC error status
25	FLK_ERR_ST	Flicker error status
24	ESFKO_ERR_ST	ESFKO error status
23	RRZO_ERR_ST	IMG2O error status
22	LCSO_ERR_ST	LCSO error status
21	AAO_ERR_ST	AEerror status
20	IMGO_ERR_ST	IMGO overrun status
19	CQ_DON_ST	CQ load finished time is after ISP start status
17	FLK_DON_ST	Flicker end status
16	AF_DON_ST	AF done interrupt status
15	TPIPE_DON_ST	TPIPE done status
14	PASS2_DON_ST	PASS2 done status
13	CQ_ERR_ST	CQ error status done status
12	SOF1_INT_ST	TG1 SOF interrupt status
10	PASS1_DON_ST	**PASS1 done interrupt status** Only for stereo mode
9	RRZO_DROP_FRAME_ST	RRZO drop frame status
8	IMGO_DROP_FRAME_ST	IMGO drop frame status
7	CQ0_VS_ERR_ST	CQ0 cover next vsync error
6	CQ0_ERR	CQ0_ERR
5	TG1_GBERR	TG1_GBERR
4	TG1_ERR_ST	**TG1 ERR status** 1: TG overrun occurs. The normal hint bandwidth is not enough.
3	EXPDON1_ST	Exposusre1 done interrupt status
2	TG1_INT2_ST	TG1 interrupt2 status
1	TG1_INT1_ST	TG1 interrupt1 status
0	VS1_INT_ST	Vsync1 interrupt status

15004074	**CAM_CTL_INT_STATUS2X**	**ISP Interrupt Status**	**00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DMA_ERR_ST		FBC_IMGO_DON_ST	FBC_RRZO_DON_ST	LSC_ERR_ST		AFO_ERR_ST	RRZO_ERR_ST	LCSO_ERR_ST	AAO_ERR_ST	IMGO_ERR_ST				AF_DON_ST
Type		RU		RU	RU	RU		RU	RU	RU	RU	RU				RU
Reset		0		0	0	0		0	0	0	0	0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				SOF1_INT_ST		PASS1_DON_ST	RRZO_DROP_FRAME_ST	IMGO_DROP_FRAME_ST	CQ0_VS_ERR_ST	CQ0_ERR	TG1_GBERR	TG1_ERR_ST	EXPDON1_ST	TG1_INT2_ST	TG1_INT1_ST	VS1_INT_ST
Type				RU		RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset				0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30	DMA_ERR_ST	DMA error status
28	FBC_IMGO_DON_ST	FBC IMGO done status
27	FBC_RRZO_DON_ST	FBC RRZO done status
26	LSC_ERR_ST	LSC error status
24	AFO_ERR_ST	AFO error status
23	RRZO_ERR_ST	IMG2O error status
22	LCSO_ERR_ST	LCSO error status
21	AAO_ERR_ST	AEerror status
20	IMGO_ERR_ST	IMGO overrun status
16	AF_DON_ST	AF done interrupt status
12	SOF1_INT_ST	TG1 SOF interrupt status
10	PASS1_DON_ST	**PASS1 done interrupt status** Only for stereo mode
9	RRZO_DROP_FRAME_ST	RRZO drop frame status
8	IMGO_DROP_FRAME_ST	IMGO drop frame status
7	CQ0_VS_ERR_ST	CQ0 cover next vsync error
6	CQ0_ERR	CQ0_ERR
5	TG1_GBERR	TG1_GBERR
4	TG1_ERR_ST	**TG1 ERR status** 1: TG overrun occurs. The normal hint bandwidth is not enough.
3	EXPDON1_ST	Exposusre1 done interrupt status
2	TG1_INT2_ST	TG1 interrupt2 status
1	TG1_INT1_ST	TG1 interrupt1 status
0	VS1_INT_ST	Vsync1 interrupt status

15004078	CAM_CTL_INT_STATUS3X	ISP Interrupt Status	00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			PCA_COLLISION_ST	GGM_COLLISION_ST	DMA_ERR_ST	FEO_DONE_ST	IMG3CO_DONE_ST	IMG3BO_DONE_ST	IMG3O_DONE_ST	IMG2O_DONE_ST	MFBO_DONE_ST	LCEI_DONE_ST	VIP3I_DONE_ST	VIP2I_DONE_ST	VIPI_DONE_ST	UFDI_DONE_ST
Type			RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IMGI_DONE_ST	LSCI_D_DONE_ST	BPCI_D_DONE_ST	AAO_D_DONE_ST	LCSO_D_DONE_ST	AFO_D_DONE_ST	RRZO_D_DONE_ST	IMGO_D_DONE_ST	LSCI_DONE_ST	BPCI_DONE_ST	AAO_DONE_ST	LCSO_DONE_ST	ESFKO_DONE_ST	RRZO_DONE_ST	UFEO_DONE_ST	IMGO_DONE_ST
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29	PCA_COLLISION_ST	PCA_COLLISION_ST
28	GGM_COLLISION_ST	GGM_COLLISION_ST
27	DMA_ERR_ST	DMA error status
26	FEO_DONE_ST	FEO_DONE_ST
25	IMG3CO_DONE_ST	IMG3CO_DONE_ST
24	IMG3BO_DONE_ST	IMG3BO_DONE_ST
23	IMG3O_DONE_ST	IMG3O_DONE_ST
22	IMG2O_DONE_ST	IMG2O_DONE_ST
21	MFBO_DONE_ST	MFBO_DONE_ST
20	LCEI_DONE_ST	LCEI_DONE_ST
19	VIP3I_DONE_ST	VIP3I_DONE_ST
18	VIP2I_DONE_ST	VIP2I_DONE_ST
17	VIPI_DONE_ST	VIPI_DONE_ST
16	UFDI_DONE_ST	UFDI_DONE_ST
15	IMGI_DONE_ST	IMGI_DONE_ST
14	LSCI_D_DONE_ST	LSCI_D_DONE_ST
13	BPCI_D_DONE_ST	BPCI_D_DONE_ST
12	AAO_D_DONE_ST	AAO_D_DONE_ST
11	LCSO_D_DONE_ST	LCSO_D_DONE_ST
10	AFO_D_DONE_ST	AFO_D_DONE_ST
9	RRZO_D_DONE_ST	RRZO_D_DONE_ST
8	IMGO_D_DONE_ST	IMGO_D_DONE_ST
7	LSCI_DONE_ST	LSCI_D_DONE_ST
6	BPCI_DONE_ST	BPCI_DONE_ST
5	AAO_DONE_ST	AAO_DONE_ST
4	LCSO_DONE_ST	LCSO_DONE_ST
3	ESFKO_DONE_ST	ESFKO_DONE_ST

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Bit(s)	Name	Description
2	RRZO_DONE_ST	RRZO_DONE_ST
1	UFEO_DONE_ST	UFEO_DONE_ST
0	IMGO_DONE_ST	IMGO_DONE_ST

1500407C **CAM_CTL_TPIPE** **Control TPIPE Setting** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MIX3_TCM_EN**	**CTL_EXTENSION_EN**	**NR3D_TCM_EN**	**CRSP_TCM_EN**	**SRZ2_TCM_EN**	**SRZ1_TCM_EN**	**LCE_TCM_EN**	**MDPCROP_TCM_EN**	**CRZ_TCM_EN**	**FE_TCM_EN**	**IMG3CO_TCM_EN**	**IMG3BO_TCM_EN**	**IMG3O_TCM_EN**	**IMG2O_TCM_EN**	**FEO_TCM_EN**	**VIP3I_TCM_EN**
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**VIP2I_TCM_EN**	**VIPI_TCM_EN**	**UFDI_TCM_EN**	**LCEI_TCM_EN**	**CRZ_EDGE**				**C24B_TCM_EN**	**C02_TCM_EN**	**LAST_TPIPE**	**TPIPE_IRQ**	**TPIPE_EDGE**			
Type	RW	RW	RW	RW	RW				RW	RW	RW	RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIX3_TCM_EN	**MIX3_TCM_EN**
30	CTL_EXTENSION_EN	**Enables CTL_EXTENSION** 0: Normal 1: imgo_en, img2o_en, cdrz_en and rsp_en are TPIPE parameters. In this case, CTL_LOAD_MODULE_EN must be 1. The TPIPE configuration map is not changed TPIPE by TPIPE.
29	NR3D_TCM_EN	**NR3D_TCM_EN**
28	CRSP_TCM_EN	**CRSP_TCM_EN**
27	SRZ2_TCM_EN	**SRZ2_TCM_EN**
26	SRZ1_TCM_EN	**SRZ1_TCM_EN**
25	LCE_TCM_EN	**LCE_TCM_EN**
24	MDPCROP_TCM_EN	**MDPCROP_TCM_EN**
23	CRZ_TCM_EN	**CRZ_TCM_EN**
22	FE_TCM_EN	**FE_TCM_EN**
21	IMG3CO_TCM_EN	**IMG3CO_TCM_EN**
20	IMG3BO_TCM_EN	**IMG3BO_TCM_EN**
19	IMG3O_TCM_EN	**IMG3O_TCM_EN**
18	IMG2O_TCM_EN	**IMG2O_TCM_EN**
17	FEO_TCM_EN	**FEO_TCM_EN**
16	VIP3I_TCM_EN	**VIP3I_TCM_EN**
15	VIP2I_TCM_EN	**VIP2I_TCM_EN**
14	VIPI_TCM_EN	**VIPI_TCM_EN**
13	UFDI_TCM_EN	**UFDI_TCM_EN**
12	LCEI_TCM_EN	**LCEI_TCM_EN**

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Bit(s)	Name	Description
11:8	CRZ_EDGE	**Edge after CRZ**
7	C24B_TCM_EN	**C24B_TCM_EN**
6	C02_TCM_EN	**C02_TCM_EN**
5	LAST_TPIPE	**LAST TPIPE index** 0: Not last 1: Last TPIPE
4	TPIPE_IRQ	**Enables TPIPE IRQ** 0: Does not issue interrupt at one TPIPE finished 1: Issue interrupt at one TPIPE finsihed
3:0	TPIPE_EDGE	**This TPIPE has the following edges if the value is 1'b1:** [0]: Left [1]: Right [2]: Top [3]: Bottom

15004080 **CAM_CTL_TDR_EN_STATUS** **CTL_TDR_EN_STATUS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			**CTL_TDR_EN_STATUS[29:16]**													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CTL_TDR_EN_STATUS[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:0	CTL_TDR_EN_STATUS	**CTL_TDR_EN_STATUS** imgi, ufdi (bit 29 ~ 28) lsci, lcei, vipi, vip2i (bit 27 ~ 24) vip3i, img3o, img3bo, img3co (bit23 ~ 20) img2o, feo, ufd, unp (bit 19~ 16) bnr, lsc, sl2, sl2b (bit 15 ~ 12) sl2c, srz1, srz2, lce (bit 11 ~ 8) crz, fe, nr3d, mdpcrop (bit 7 ~ 4) crsp, c02, mfb, g2c (bit 3~0)

15004084 **CAM_CTL_TCM_EN** **TCM Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**TDR_EN**	**TDR_SZ_DET**	**TDR_SOF_RST_EN**	**MFBO_TCM_EN**	**MIX1_TCM_EN**	**PCA_TCM_EN**	**MIX2_TCM_EN**	**SL2C_TCM_EN**	**SEEE_TCM_EN**	**TPIPE_HEIGHT[12:6]**						
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TPIPE_HEIGHT[5:0]**						**TPIPE_WIDTH**									
Type	RW						RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31	TDR_EN	**Enables TPIPE**
30	TDR_SZ_DET	**Enables TDR size detection** If set to 1, TDR will compare SW TPIPE size; if not equal, TDR will be reset and issue a TDR error interrupt.
29	TDR_SOF_RST_EN	**Enables TDR SOF reset** If set to 1, TDR will be reset by frame_sof.
28	MFBO_TCM_EN	**MFBO_TCM_EN**
27	MIX1_TCM_EN	**MIX1_TCM_EN**
26	PCA_TCM_EN	**PCA_TCM_EN**
25	MIX2_TCM_EN	**MIX2_TCM_EN**
24	SL2C_TCM_EN	**SL2C_TCM_EN**
23	SEEE_TCM_EN	**SEEE_TCM_EN**
22:10	TPIPE_HEIGHT	**TPIPE height**
9:0	TPIPE_WIDTH	**TPIPE width**

15004088 **CAM_CTL_TDR_DBG_STATUS** **CTL_TDR_DBG_STATUS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name		LOAD_SIZE							TPIPE_CNT							
Type		RU							RU							
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:8	LOAD_SIZE	**LOAD_SIZE** Compares with tdr_ctl[39:32] at TPIPEmain output hex file
7:0	TPIPE_CNT	**TPIPE counter, it show current TPIPE processing number**

1500408C **CAM_CTL_SW_CTL** **CTL_SW_CTL** **00000022**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name										HW_RST_P2	SW_RST_P2_ST	SW_RST_P2_Trig		HW_RST	SW_RST_ST	SW_RST_Trig
Type										RW	RU	WO		RW	RU	WO
Reset										0	1	0		0	1	0

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Bit(s)	Name	Description
6	HW_RST_P2	**Pass2** 0: No HW reset 1: Async HW reset. Reset all CAM modules, except for register setting module.
5	SW_RST_P2_ST	**Pass2** Software reset status 0: DMA is busy. 1: DMA is idle; can do HW reset.
4	SW_RST_P2_Trig	**Pass2** Triggers software reset. Write 1 to trigger.
2	HW_RST	**Pass1** 0: No HW reset 1: Async HW reset. Reset all CAM modules, except for register setting module.
1	SW_RST_ST	**Pass1** Software reset status 0: DMA is busy. 1: DMA is idle; can do HW reset.
0	SW_RST_Trig	**Pass1** Triggers software reset. Write 1 to trigger.

15004090 **CAM_CTL_SPARE0** **CTL_SPARE0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE0	Spare register

15004094 **CAM_CTL_SPARE1** **CTL_SPARE1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE1	Spare register

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1500409C **CAM_CTL_SPARE2** **CTL_SPARE2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE2	Spare register

150040A0 **CAM_CTL_CQ1_BASEADDR** **CTL_CQ1_BASEADDR** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CQ1_BASEADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CQ1_BASEADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CQ1_BASEADDR	CQ1 base address

150040A4 **CAM_CTL_CQ2_BASEADDR** **CTL_CQ2_BASEADDR** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CQ2_BASEADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CQ2_BASEADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CQ2_BASEADDR	CQ2 base address

150040A8 **CAM_CTL_CQ3_BASEADDR** **CTL_CQ3_BASEADDR** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	**CQ3_BASEADDR[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CQ3_BASEADDR[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CQ3_BASEADDR	CQ3 base address

150040AC **CAM_CTL_CQ0_BASEADDR** **CTL_CQ0_BASEADDR** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CQ0_BASEADDR[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CQ0_BASEADDR[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CQ0_BASEADDR	CQ0 base address

150040B0 **CAM_CTL_CQ0B_BASEADDR** **CTL_CQ0B_BASEADDR** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CQ0B_BASEADDR[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CQ0B_BASEADDR[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CQ0B_BASEADDR	CQ0B base address

150040B4 **CAM_CTL_CQ0C_BASEADDR** **CTL_CQ0C_BASEADDR** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CQ0C_BASEADDR[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	CQoC_BASEADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CQoC_BASEADDR	CQoC base address

150040B8 **CAM_CTL_CUR_CQ0_BASEADDR** **CTL_CUR_CQ0_BASEADDR** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CUR_CQ0_BASEADDR[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CUR_CQ0_BASEADDR[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CUR_CQ0_BASEADDR	CQ0 base address

150040BC **CAM_CTL_CUR_CQ0B_BASEADDR** **CTL_CUR_CQ0B_BASEADDR** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CUR_CQ0B_BASEADDR[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CUR_CQ0B_BASEADDR[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CUR_CQ0B_BASEADDR	CQ0B base address

150040C0 **CAM_CTL_CUR_CQ0C_BASEADDR** **CTL_CUR_CQ0C_BASEADDR** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CTL_CUR_CQ0C_BASEADDR[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CTL_CUR_CQ0C_BASEADDR[15:0]															
Type	RU															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CTL_CUR_CQ0C_BASEADDR	CQ0C base address

150040C4 **CAM_CTL_CQ0_D_BASEADDR** **CTL_CQ0_D_BASEADDR** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CTL_CQ0_D_BASEADDR[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CTL_CQ0_D_BASEADDR[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CTL_CQ0_D_BASEADDR	CTL_CQ0_D_BASEADDR

150040C8 **CAM_CTL_CQ0B_D_BASEADDR** **CTL_CQ0B_D_BASEADDR** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CTL_CQ0B_D_BASEADDR[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CTL_CQ0B_D_BASEADDR[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CTL_CQ0B_D_BASEADDR	CTL_CQ0B_D_BASEADDR

150040CC **CAM_CTL_CQ0C_D_BASEADDR** **CTL_CQ0C_D_BASEADDR** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CTL_CQ0C_D_BASEADDR[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CTL_CQ0C_D_BASEADDR[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	CTL_CQoC_D_BASEADDR	CTL_CQoC_D_BASEADDR

150040D0 **CAM_CTL_CUR_CQ0_D_BASEADDR** **CTL_CUR_CQ0_D_BASEADDR** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CTL_CUR_CQ0_D_BASEADDR[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CTL_CUR_CQ0_D_BASEADDR[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CTL_CUR_CQ0_D_BASEADDR	CTL_CUR_CQ0_D_BASEADDR

150040D4 **CAM_CTL_CUR_CQ0B_D_BASEADDR** **CTL_CUR_CQ0B_D_BASEADDR** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CTL_CUR_CQ0B_D_BASEADDR[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CTL_CUR_CQ0B_D_BASEADDR[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CTL_CUR_CQ0B_D_BASEADDR	CTL_CUR_CQ0B_D_BASEADDR

150040D8 **CAM_CTL_CUR_CQ0C_D_BASEADDR** **CTL_CUR_CQ0C_D_BASEADDR** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CTL_CUR_CQ0C_D_BASEADDR[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CTL_CUR_CQ0C_D_BASEADDR[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	CTL_CUR_CQ0C_D_BASEADDR	CTL_CUR_CQ0C_D_BASEADDR

150040DC **CAM_CTL_DB_LOAD_D** **DB_LOAD_HOLD_D** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															DB_LOAD_HOLD_D	
Type															RW	
Reset															0	

Bit(s)	Name	Description
1	DB_LOAD_HOLD_D	Pass1_D db load hold

150040E0 **CAM_CTL_DB_LOAD** **DB_LOAD_HOLD** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															DB_LOAD_HOLD	
Type															RW	
Reset															0	

Bit(s)	Name	Description
1	DB_LOAD_HOLD	Pass1 db load hold

150040E4 **CAM_CTL_P1_DONE_BYP** **CTL_P1_DONE_BYP** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TG1_DO	LSCI_DO	BPCI_D	AAO_DO	LCSO_D	ESFKO_	RRZO_D	UFEO_D	IMGO_D

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								NE_ BYP	NE_ BYP	ONE _BY P	NE_ BYP	ONE _BY P	DON E_B YP	ONE _BY P	ONE _BY P	ONE _BY P
Type								RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8	TG1_DONE_BYP	**TG1_DONE_BYP** 1: Pass1 does not refer to this condition.
7	LSCI_DONE_BYP	LSCI_DONE_BYP
6	BPCI_DONE_BYP	BPCI_DONE_BYP
5	AAO_DONE_BYP	AAO_DONE_BYP
4	LCSO_DONE_BYP	LCSO_DONE_BYP
3	ESFKO_DONE_BYP	ESFKO_DONE_BYP
2	RRZO_DONE_BYP	RRZO_DONE_BYP
1	UFEO_DONE_BYP	UFEO_DONE_BYP
0	IMGO_DONE_BYP	IMGO_DONE_BYP

150040E8 **CAM_CTL_P1_DONE_BYP_D** **CTL_P1_DONE_BYP_D** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TG1 _DO NE_ BYP _D	LSCI _DO NE_ BYP _D	BPC I_D ONE _BY P_D	AAO _DO NE_ BYP _D	LCS O_D ONE _BY P_D	AFO _DO NE_ BYP _D	RRZ O_D ONE _BY P_D		IMG O_D ONE _BY P_D
Type								RW	RW	RW	RW	RW	RW	RW		RW
Reset								0	0	0	0	0	0	0		0

Bit(s)	Name	Description
8	TG1_DONE_BYP_D	**TG1_DONE_BYP_D** 1: pass1_D does not refer to this condition.
7	LSCI_DONE_BYP_D	LSCI_DONE_BYP_D
6	BPCI_DONE_BYP_D	BPCI_DONE_BYP_D
5	AAO_DONE_BYP_D	AAO_DONE_BYP_D
4	LCSO_DONE_BYP_D	LCSO_DONE_BYP_D
3	AFO_DONE_BYP_D	AFO_DONE_BYP_D
2	RRZO_DONE_BYP_D	RRZO_DONE_BYP_D
0	IMGO_DONE_BYP_D	IMGO_DONE_BYP_D

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150040EC **CAM_CTL_P2_DONE_BYP** **CTL_P1_DONE_BYP** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					FEO_DONE_BYP	IMG3CO_DONE_BYP	IMG3BO_DONE_BYP	IMG3O_DONE_BYP	IMG2O_DONE_BYP	MFBO_DONE_BYP	LCEI_DONE_BYP	VIP3I_DONE_BYP	VIP2I_DONE_BYP	VIPI_DONE_BYP	UFDI_DONE_BYP	IMGI_DONE_BYP
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	FEO_DONE_BYP	**FEO_DONE_BYP** Pass2 dooes not refer to this condition.
10	IMG3CO_DONE_BYP	IMG3CO_DONE_BYP
9	IMG3BO_DONE_BYP	IMG3BO_DONE_BYP
8	IMG3O_DONE_BYP	IMG3O_DONE_BYP
7	IMG2O_DONE_BYP	IMG2O_DONE_BYP
6	MFBO_DONE_BYP	MFBO_DONE_BYP
5	LCEI_DONE_BYP	LCEI_DONE_BYP
4	VIP3I_DONE_BYP	VIP3I_DONE_BYP
3	VIP2I_DONE_BYP	VIP2I_DONE_BYP
2	VIPI_DONE_BYP	VIPI_DONE_BYP
1	UFDI_DONE_BYP	UFDI_DONE_BYP
0	IMGI_DONE_BYP	IMGI_DONE_BYP

150040F0 **CAM_CTL_IMGO_FBC** **CTL_IMGO_FBC** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DROP_CNT				WCNT				RCNT				FB_NUM			
Type	RU				RU				RU				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LOCK_EN	FBC_EN			RCNT_INC								FBC_CNT			
Type	RW	RW			WO								RU			
Reset	0	0			0								0	0	0	0

Bit(s)	Name	Description
31:28	DROP_CNT	**Drop frame counter**

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Bit(s)	Name	Description
		1: Drop 1 frame at TG
27:24	WCNT	**WCNT** HW increases 1 when pass1 done occurs.
23:20	RCNT	**Frame buffer read counter** At pass2 done, increase 1 by rcnt_inc.
19:16	FB_NUM	**Frame buffer number**
15	LOCK_EN	**Enables frame buffer lock**
14	FBC_EN	**Enables frame buffer**
11	RCNT_INC	**Frame buffer control rcnt increasement by writing 1**
3:0	FBC_CNT	**Available frame buffer counter**

150040F4 CAM_CTL_RRZO_FBC CTL_RRZO_FBC 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DROP_CNT				WCNT				RCNT				FB_NUM			
Type	RU				RU				RU				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LOCK_EN	FBC_EN			RCNT_INC								FBC_CNT			
Type	RW	RW			WO								RU			
Reset	0	0			0								0	0	0	0

Bit(s)	Name	Description
31:28	DROP_CNT	**Drop frame counter** 1: Drop 1 frame at TG
27:24	WCNT	**WCNT** HW increases 1 when pass1 done occurs.
23:20	RCNT	**Frame buffer read counter** At pass2 done, increase 1 by rcnt_inc.
19:16	FB_NUM	**Frame buffer number**
15	LOCK_EN	**Enables frame buffer lock**
14	FBC_EN	**Enables frame buffer**
11	RCNT_INC	**Frame buffer control rcnt increasement by writing 1**
3:0	FBC_CNT	**Available frame buffer counter**

150040F8 CAM_CTL_IMGO_D_FBC CTL_IMGO_D_FBC 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DROP_CNT				WCNT				RCNT				FB_NUM			
Type	RU				RU				RU				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LOCK_EN	FBC_EN			RCNT_INC								FBC_CNT			

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Type	RW	RW			WO								RU			
Reset	0	0			0								0	0	0	0

Bit(s)	Name	Description
31:28	DROP_CNT	**Drop frame counter** 1: Drop 1 frame at TG
27:24	WCNT	**WCNT** HW increases 1 when pass1 done occurs.
23:20	RCNT	**Frame buffer read counter** At pass2 done, increase 1 by rcnt_inc.
19:16	FB_NUM	**Frame buffer number**
15	LOCK_EN	**Enables frame buffer lock**
14	FBC_EN	**Enables frame buffer**
11	RCNT_INC	**Frame buffer control rcnt increasement by writing 1**
3:0	FBC_CNT	**Available frame buffer counter**

150040FC **CAM_CTL_RRZO_D_FBC** **CTL_RRZO_D_FBC** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DROP_CNT**				**WCNT**				**RCNT**				**FB_NUM**			
Type	RU				RU				RU				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**LOCK_EN**	**FBC_EN**			**RCNT_INC**								**FBC_CNT**			
Type	RW	RW			WO								RU			
Reset	0	0			0								0	0	0	0

Bit(s)	Name	Description
31:28	DROP_CNT	**Drop frame counter** 1: Drop 1 frame at TG
27:24	WCNT	**WCNT** HW increases 1 when pass1 done occurs.
23:20	RCNT	**Frame buffer read counter** At pass2 done, increase 1 by rcnt_inc.
19:16	FB_NUM	**Frame buffer number**
15	LOCK_EN	**Enables frame buffer lock**
14	FBC_EN	**Enables frame buffer**
11	RCNT_INC	**Frame buffer control rcnt increasement by writing 1**
3:0	FBC_CNT	**Available frame buffer counter**

15004100 **CAM_CTL_SPARE3** **CTL_SPARE3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SPARE3[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE3[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE3	Spare register

15004104 **CAM_CTL_IHDR** **CTL_IHDR** **00000040**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name			IHDR_LE_FIRST	IHDR_MODE				IHDR_GAIN								
Type			RW	RW				RW								
Reset			0	0				0	0	1	0	0	0	0	0	0

Bit(s)	Name	Description
13	IHDR_LE_FIRST	ihdr long exposure first
12	IHDR_MODE	ihdr mode
8:0	IHDR_GAIN	idhr gain

15004108 **CAM_CTL_IHDR_D** **CTL_IHDR_D** **00000040**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name			IHDR_D_LE_FIRST	IHDR_D_MODE				IHDR_D_GAIN								
Type			RW	RW				RW								
Reset			0	0				0	0	1	0	0	0	0	0	0

Bit(s)	Name	Description
13	IHDR_D_LE_FIRST	ihdr long exposure first
12	IHDR_D_MODE	ihdr mode
8:0	IHDR_D_GAIN	idhr gain

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1500410C **CAM_CTL_CQ_EN_P2** **CTL_CQ_EN_P2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name														CQ3_EN	CQ2_EN	CQ1_EN
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	CQ3_EN	Enables Command3 queue
1	CQ2_EN	Enables Command2 queue
0	CQ1_EN	Enables Command queue

15004110 **CAM_CTL_SEL_GLOBAL_P2** **CTL_SEL_GLOBAL_P2** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name																PASS2_DB_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	PASS2_DB_EN	Enables Pass2 module double buffer

15004160 **CAM_CTL_DBG_SET** **CTL_DBG_SET** **0000F000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DEBUG_TOP_SEL				DEBUG_SEL				DEBUG_MOD_SEL							
Type	RW				RW				RW							
Reset	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:12	DEBUG_TOP_SEL	**0: DMA** 1: RAW 2: RGB 3: YUV

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Bit(s)	Name	Description
		4: RAW_D 5: TDR 6: CQ 7: CQo 8: Reserved 9: Top
11:8	DEBUG_SEL	**Selects debugging** Used for sub-module
7:0	DEBUG_MOD_SEL	**Selects debugging module** Used for RAW/RGB/YUV to choose which module is for debugging port output. For top (Debug_TOP_SEL==9): 0~2: IMGO 3~5: IMGI 6~8: raw_cfa 9~11: rgb_yuv 12~14: yuv_out

15004164 **CAM_CTL_DBG_PORT** **CTL_DBG_PORT** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CTL_DBG_PORT[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CTL_DBG_PORT[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CTL_DBG_PORT	Debugging port

15004168 **CAM_CTL_IMGI_CHECK** **CTL_IMGI_CHECK** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CTL_IMGI_CHECK[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CTL_IMGI_CHECK[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CTL_IMGI_CHECK	IMGI checksum

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1500416C **CAM_CTL_IMGO_CHECK** **CTL_IMGO_CHECK** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CTL_IMGO_CHECK[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CTL_IMGO_CHECK[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CTL_IMGO_CHECK	IMGO checksum

15004170 **CAM_CTL_CLK_EN** **CLK_EN** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DMA_DP_CK_EN	DIP_DP_CK_EN	RAW_D_DP_CK_EN	RAW_DP_CK_EN
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	DMA_DP_CK_EN	Enables DMA DP CK
2	DIP_DP_CK_EN	Enables DIP_DP_CK
1	RAW_D_DP_CK_EN	Enables RAW_DP_CK
0	RAW_DP_CK_EN	Enables RAW_DP_CK

15004180 **CAM_CTL_DATE_CODE** **CTL_DATE_CODE** **20130510**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CTL_DATE_CODE[31:16]															
Type	RO															
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CTL_DATE_CODE[15:0]															
Type	RO															
Reset	0	0	0	0	0	1	0	1	0	0	0	1	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:0	CTL_DATE_CODE	Date code

15004184 **CAM_CTL_PROJ_CODE** **CTL_PROJ_CODE** **65930000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CTL_PROJ_CODE[31:16]															
Type	RO															
Reset	0	1	1	0	0	1	0	1	1	0	0	1	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CTL_PROJ_CODE[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CTL_PROJ_CODE	Project code

15004188 **CAM_CTL_RAW_DCM_DIS** **CTL_RAW_DCM_DIS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						CPG_DCM_DIS	RMG_DCM_DIS	EIS_DCM_DIS	SGG2_DCM_DIS	AA_DCM_DIS	HBIN_DCM_DIS	FLK_DCM_DIS	AF_DCM_DIS	SGG1_DCM_DIS	LCS_DCM_DIS	UFE_DCM_DIS
Type						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAK_DCM_DIS	BMX_DCM_DIS	PAKG_DCM_DIS	RMX_DCM_DIS	RRZ_DCM_DIS	RPG_DCM_DIS	LSC_DCM_DIS	BNR_DCM_DIS	OB_DCM_DIS	W2G_DCM_DIS	WBN_DCM_DIS	DMX_DCM_DIS	TG1_DCM_DIS	UNP_DCM_DIS	PGN_DCM_DIS	UFD_DCM_DIS
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26	CPG_DCM_DIS	0: DCM is on. 1: DCM is off.
25	RMG_DCM_DIS	0: DCM is on. 1: DCM is off.
24	EIS_DCM_DIS	0: DCM is on. 1: DCM is off.
23	SGG2_DCM_DIS	0: DCM is on. 1: DCM is off.
22	AA_DCM_DIS	0: DCM is on. 1: DCM is off.
21	HBIN_DCM_DIS	0: DCM is on. 1: DCM is off.
20	FLK_DCM_DIS	0: DCM is on. 1: DCM is off.

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Bit(s)	Name	Description
19	AF_DCM_DIS	0: DCM is on. 1: DCM is off.
18	SGG1_DCM_DIS	0: DCM is on. 1: DCM is off.
17	LCS_DCM_DIS	0: DCM is on. 1: DCM is off.
16	UFE_DCM_DIS	0: DCM is on. 1: DCM is off.
15	PAK_DCM_DIS	0: DCM is on. 1: DCM is off.
14	BMX_DCM_DIS	0: DCM is on. 1: DCM is off.
13	PAKG_DCM_DIS	0: DCM is on. 1: DCM is off.
12	RMX_DCM_DIS	0: DCM is on. 1: DCM is off.
11	RRZ_DCM_DIS	0: DCM is on. 1: DCM is off.
10	RPG_DCM_DIS	0: DCM is on. 1: DCM is off.
9	LSC_DCM_DIS	0: DCM is on. 1: DCM is off.
8	BNR_DCM_DIS	0: DCM is on. 1: DCM is off.
7	OB_DCM_DIS	0: DCM is on. 1: DCM is off.
6	W2G_DCM_DIS	0: DCM is on. 1: DCM is off.
5	WBN_DCM_DIS	0: DCM is on. 1: DCM is off.
4	DMX_DCM_DIS	0: DCM is on. 1: DCM is off.
3	TG1_DCM_DIS	0: DCM is on. 1: DCM is off.
2	UNP_DCM_DIS	0: DCM is on. 1: DCM is off.
1	PGN_DCM_DIS	0: DCM is on. 1: DCM is off.
0	UFD_DCM_DIS	0: DCM is on. 1: DCM is off.

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1500418C	CAM_CTL_RAW_D_DCM_DIS	CTL_RAW_D_DCM_DIS	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						CPG_D_DCM	RMG_D_DC			AA_D_DCM_			AF_D_DCM_	SGG1_D_DC	LCS_D_DCM	

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						_DI S	M_D IS			DIS			DIS	M_D IS	_DI S	
Type						RW	RW			RW			RW	RW	RW	
Reset						0	0			0			0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**PAK _D_ DCM _DI S**		**PAK G_D _DC M_D IS**		**RRZ _D_ DCM _DI S**	**RPG _D_ DCM _DI S**	**LSC _D_ DCM _DI S**	**BNR _D_ DCM _DI S**	**OB_ D_D CM_ DIS**	**W2G _D_ DCM _DI S**	**WB N_D _DC M_D IS**		**TG1 _D_ DCM _DIS**			
Type	RW		RW		RW	RW	RW	RW	RW	RW	RW		RW			
Reset	0		0		0	0	0	0	0	0	0		0			

Bit(s)	Name	Description
26	CPG_D_DCM_DIS	0: DCM is on. 1: DCM is off.
25	RMG_D_DCM_DIS	0: DCM is on. 1: DCM is off.
22	AA_D_DCM_DIS	0: DCM is on. 1: DCM is off.
19	AF_D_DCM_DIS	0: DCM is on. 1: DCM is off.
18	SGG1_D_DCM_DIS	0: DCM is on. 1: DCM is off.
17	LCS_D_DCM_DIS	0: DCM is on. 1: DCM is off.
15	PAK_D_DCM_DIS	0: DCM is on. 1: DCM is off.
13	PAKG_D_DCM_DIS	0: DCM is on. 1: DCM is off.
11	RRZ_D_DCM_DIS	0: DCM is on. 1: DCM is off.
10	RPG_D_DCM_DIS	0: DCM is on. 1: DCM is off.
9	LSC_D_DCM_DIS	0: DCM is on. 1: DCM is off.
8	BNR_D_DCM_DIS	0: DCM is on. 1: DCM is off.
7	OB_D_DCM_DIS	0: DCM is on. 1: DCM is off.
6	W2G_D_DCM_DIS	0: DCM is on. 1: DCM is off.
5	WBN_D_DCM_DIS	0: DCM is on. 1: DCM is off.
3	TG1_D_DCM_DIS	0: DCM is on. 1: DCM is off.

15004190 **CAM_CTL_DMA_DCM_DIS** **CTL_DMA_DCM_DIS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name						LSCI_DCM_DIS	BPCI_DCM_DIS	AAO_DCM_DIS	LCSO_DCM_DIS	ESFKO_DCM_DIS	RRZO_DCM_DIS	UFEO_DCM_DIS	IMGO_DCM_DIS	LSCI_D_DCM_DIS	BPCI_D_DCM_DIS	AAO_D_DCM_DIS
Type						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LCSO_D_DCM_DIS	AFO_D_DCM_DIS	RRZO_D_DCM_DIS	IMGO_D_DCM_DIS	FEO_DCM_DIS	IMG3CO_DCM_DIS	IMG3BO_DCM_DIS	IMG3O_DCM_DIS	IMG2O_DCM_DIS	MFBO_DCM_DIS	LCEI_DCM_DIS	VIP3I_DCM_DIS	VIP2I_DCM_DIS	VIPI_DCM_DIS	UFDI_DCM_DIS	IMGI_DCM_DIS
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26	LSCI_DCM_DIS	0: DCM is on. 1: DCM is off.
25	BPCI_DCM_DIS	0: DCM is on. 1: DCM is off.
24	AAO_DCM_DIS	0: DCM is on. 1: DCM is off.
23	LCSO_DCM_DIS	0: DCM is on. 1: DCM is off.
22	ESFKO_DCM_DIS	0: DCM is on. 1: DCM is off.
21	RRZO_DCM_DIS	0: DCM is on. 1: DCM is off.
20	UFEO_DCM_DIS	0: DCM is on. 1: DCM is off.
19	IMGO_DCM_DIS	0: DCM is on. 1: DCM is off.
18	LSCI_D_DCM_DIS	0: DCM is on. 1: DCM is off.
17	BPCI_D_DCM_DIS	0: DCM is on. 1: DCM is off.
16	AAO_D_DCM_DIS	0: DCM is on. 1: DCM is off.
15	LCSO_D_DCM_DIS	0: DCM is on. 1: DCM is off.
14	AFO_D_DCM_DIS	0: DCM is on. 1: DCM is off.
13	RRZO_D_DCM_DIS	0: DCM is on. 1: DCM is off.
12	IMGO_D_DCM_DIS	0: DCM is on. 1: DCM is off.
11	FEO_DCM_DIS	0: DCM is on. 1: DCM is off.
10	IMG3CO_DCM_DIS	0: DCM is on. 1: DCM is off.
9	IMG3BO_DCM_DIS	0: DCM is on. 1: DCM is off.

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Bit(s)	Name	Description
8	IMG3O_DCM_DIS	0: DCM is on. 1: DCM is off.
7	IMG2O_DCM_DIS	0: DCM is on. 1: DCM is off.
6	MFBO_DCM_DIS	0: DCM is on. 1: DCM is off.
5	LCEI_DCM_DIS	0: DCM is on. 1: DCM is off.
4	VIP3I_DCM_DIS	0: DCM is on. 1: DCM is off.
3	VIP2I_DCM_DIS	0: DCM is on. 1: DCM is off.
2	VIPI_DCM_DIS	0: DCM is on. 1: DCM is off.
1	UFDI_DCM_DIS	0: DCM is on. 1: DCM is off.
0	IMGI_DCM_DIS	0: DCM is on. 1: DCM is off.

15004194 **CAM_CTL_RGB_DCM_DIS** **CTL_RGB_DCM_DIS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										GGM_DCM_DIS	MFB_DCM_DIS	C24_DCM_DIS	G2G_DCM_DIS	CCL_DCM_DIS	CFA_DCM_DIS	SL2_DCM_DIS
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	GGM_DCM_DIS	0: DCM is on. 1: DCM is off.
5	MFB_DCM_DIS	0: DCM is on. 1: DCM is off.
4	C24_DCM_DIS	0: DCM is on. 1: DCM is off.
3	G2G_DCM_DIS	0: DCM is on. 1: DCM is off.
2	CCL_DCM_DIS	0: DCM is on. 1: DCM is off.
1	CFA_DCM_DIS	0: DCM is on. 1: DCM is off.
0	SL2_DCM_DIS	0: DCM is on. 1: DCM is off.

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15004198	CAM_CTL_YUV_DCM_DIS	CTL_YUV_DCM_DIS	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													FE_DCM_DIS	MDPCROP_DCM_DIS	C24B_DCM_DIS	CRSP_DCM_DIS
Type													RW	RW	RW	RW
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIX3_DCM_DIS	MIX2_DCM_DIS	MIX1_DCM_DIS	CRZ_DCM_DIS	SRZ2_DCM_DIS	SRZ1_DCM_DIS	SL2C_DCM_DIS	SL2B_DCM_DIS	NR3D_DCM_DIS	LCE_DCM_DIS	SEEE_DCM_DIS	PCA_DCM_DIS	NBC_DCM_DIS	C42_DCM_DIS	G2C_DCM_DIS	C02_DCM_DIS
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	FE_DCM_DIS	0: DCM is on. 1: DCM is off.
18	MDPCROP_DCM_DIS	0: DCM is on. 1: DCM is off.
17	C24B_DCM_DIS	0: DCM is on. 1: DCM is off.
16	CRSP_DCM_DIS	0: DCM is on. 1: DCM is off.
15	MIX3_DCM_DIS	0: DCM is on. 1: DCM is off.
14	MIX2_DCM_DIS	0: DCM is on. 1: DCM is off.
13	MIX1_DCM_DIS	0: DCM is on. 1: DCM is off.
12	CRZ_DCM_DIS	0: DCM is on. 1: DCM is off.
11	SRZ2_DCM_DIS	0: DCM is on. 1: DCM is off.
10	SRZ1_DCM_DIS	0: DCM is on. 1: DCM is off.
9	SL2C_DCM_DIS	0: DCM is on. 1: DCM is off.
8	SL2B_DCM_DIS	0: DCM is on. 1: DCM is off.
7	NR3D_DCM_DIS	0: DCM is on. 1: DCM is off.
6	LCE_DCM_DIS	0: DCM is on. 1: DCM is off.
5	SEEE_DCM_DIS	0: DCM is on. 1: DCM is off.

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Bit(s)	Name	Description
4	PCA_DCM_DIS	0: DCM is on. 1: DCM is off.
3	NBC_DCM_DIS	0: DCM is on. 1: DCM is off.
2	C42_DCM_DIS	0: DCM is on. 1: DCM is off.
1	G2C_DCM_DIS	0: DCM is on. 1: DCM is off.
0	C02_DCM_DIS	0: DCM is on. 1: DCM is off.

1500419C	CAM_CTL_TOP_DCM_DIS	CTL_TOP_DCM_DIS	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TDR_DCM_DIS	FBC_DCM_DIS	CQ_DCM_DIS	TOP_DCM_DIS
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	TDR_DCM_DIS	0: DCM is on. 1: DCM is off.
2	FBC_DCM_DIS	0: DCM is on. 1: DCM is off.
1	CQ_DCM_DIS	0: DCM is on. 1: DCM is off.
0	TOP_DCM_DIS	0: DCM is on. 1: DCM is off.

150041A0	CAM_CTL_RAW_DCM_STATUS	CTL_RAW_DCM_STATUS	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						CPG_DCM_STATUS	RMG_DCM_STATUS	EIS_DCM_STATUS	SGG2_DCM_STATUS	AA_DCM_STATUS	HBIN_DCM_STATUS	FLK_DCM_STATUS	AF_DCM_STATUS	SGG1_DCM_STATUS	LCS_DCM_STATUS	UFE_DCM_STATUS
Type						RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAK_DC	BMX_DC	PAKG_D	RMX_D	RRZ_DC	RPG_DC	LSC_DC	BNR_DC	OB_DCM	W2G_DC	WBN_D	DMX_D	TG1_DC	UNP_DC	PGN_DC	UFD_DC

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	M_STATUS	M_STATUS	CM_STATUS	CM_STATUS	M_STATUS	M_STATUS	M_STATUS	M_STATUS	_STATUS	M_STATUS	CM_STATUS	CM_STATUS	M_STATUS	M_STATUS	M_STATUS	M_STATUS
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26	CPG_DCM_STATUS	0: DCM is on. 1: DCM is off.
25	RMG_DCM_STATUS	0: DCM is on. 1: DCM is off.
24	EIS_DCM_STATUS	0: DCM is on. 1: DCM is off.
23	SGG2_DCM_STATUS	0: DCM is on. 1: DCM is off.
22	AA_DCM_STATUS	0: DCM is on. 1: DCM is off.
21	HBIN_DCM_STATUS	0: DCM is on. 1: DCM is off.
20	FLK_DCM_STATUS	0: DCM is on. 1: DCM is off.
19	AF_DCM_STATUS	0: DCM is on. 1: DCM is off.
18	SGG1_DCM_STATUS	0: DCM is on. 1: DCM is off.
17	LCS_DCM_STATUS	0: DCM is on. 1: DCM is off.
16	UFE_DCM_STATUS	0: DCM is on. 1: DCM is off.
15	PAK_DCM_STATUS	0: DCM is on. 1: DCM is off.
14	BMX_DCM_STATUS	0: DCM is on. 1: DCM is off.
13	PAKG_DCM_STATUS	0: DCM is on. 1: DCM is off.
12	RMX_DCM_STATUS	0: DCM is on. 1: DCM is off.
11	RRZ_DCM_STATUS	0: DCM is on. 1: DCM is off.
10	RPG_DCM_STATUS	0: DCM is on. 1: DCM is off.
9	LSC_DCM_STATUS	0: DCM is on. 1: DCM is off.
8	BNR_DCM_STATUS	0: DCM is on. 1: DCM is off.
7	OB_DCM_STATUS	0: DCM is on. 1: DCM is off.
6	W2G_DCM_STATUS	0: DCM is on. 1: DCM is off.
5	WBN_DCM_STATUS	0: DCM is on.

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Bit(s)	Name	Description
		1: DCM is off.
4	DMX_DCM_STATUS	0: DCM is on. 1: DCM is off.
3	TG1_DCM_STATUS	0: DCM is on. 1: DCM is off.
2	UNP_DCM_STATUS	0: DCM is on. 1: DCM is off.
1	PGN_DCM_STATUS	0: DCM is on. 1: DCM is off.
0	UFD_DCM_STATUS	0: DCM is on. 1: DCM is off.

150041A4 **CAM_CTL_RAW_D_DCM_STATUS** **CTL_RAW_D_DCM_STATUS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						CPG_D_DCM_STATUS	RMG_D_DCM_STATUS			AA_D_DCM_STATUS			AF_D_DCM_STATUS	SGG1_D_DCM_STATUS	LCS_D_DCM_STATUS	
Type						RU	RU			RU			RU	RU	RU	
Reset						0	0			0			0	0	0	
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PAK_D_DCM_STATUS		PAKG_D_DCM_STATUS		RRZ_D_DCM_STATUS	RPG_D_DCM_STATUS	LSC_D_DCM_STATUS	BNR_D_DCM_STATUS	OB_D_DCM_STATUS	W2G_D_DCM_STATUS	WBN_D_DCM_STATUS		TG1_D_DCM_STATUS			
Type	RU		RU		RU	RU	RU	RU	RU	RU	RU		RU			
Reset	0		0		0	0	0	0	0	0	0		0			

Bit(s)	Name	Description
26	CPG_D_DCM_STATUS	0: DCM is on. 1: DCM is off.
25	RMG_D_DCM_STATUS	0: DCM is on. 1: DCM is off.
22	AA_D_DCM_STATUS	0: DCM is on. 1: DCM is off.
19	AF_D_DCM_STATUS	0: DCM is on. 1: DCM is off.
18	SGG1_D_DCM_STATUS	0: DCM is on. 1: DCM is off.
17	LCS_D_DCM_STATUS	0: DCM is on. 1: DCM is off.
15	PAK_D_DCM_STATUS	0: DCM is on. 1: DCM is off.
13	PAKG_D_DCM_STATUS	0: DCM is on. 1: DCM is off.

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Bit(s)	Name	Description
11	RRZ_D_DCM_STATUS	0: DCM is on. 1: DCM is off.
10	RPG_D_DCM_STATUS	0: DCM is on. 1: DCM is off.
9	LSC_D_DCM_STATUS	0: DCM is on. 1: DCM is off.
8	BNR_D_DCM_STATUS	0: DCM is on. 1: DCM is off.
7	OB_D_DCM_STATUS	0: DCM is on. 1: DCM is off.
6	W2G_D_DCM_STATUS	0: DCM is on. 1: DCM is off.
5	WBN_D_DCM_STATUS	0: DCM is on. 1: DCM is off.
3	TG1_D_DCM_STATUS	0: DCM is on. 1: DCM is off.

150041A8 **CAM_CTL_DMA_DCM_STATUS** **CTL_DMA_DCM_STATUS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LSCI_DCM_STATUS	BPCI_DCM_STATUS	AAO_DCM_STATUS	LCSO_DCM_STATUS	ESFKO_DCM_STATUS	RRZO_DCM_STATUS	UFEO_DCM_STATUS	IMGO_DCM_STATUS	LSCI_D_DCM_STATUS	BPCI_D_DCM_STATUS	AAO_D_DCM_STATUS
Type						RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LCSO_D_DCM_STATUS	AFO_D_DCM_STATUS	RRZO_D_DCM_STATUS	IMGO_D_DCM_STATUS	FEO_DCM_STATUS	IMG3CO_DCM_STATUS	IMG3BO_DCM_STATUS	IMG3O_DCM_STATUS	IMG2O_DCM_STATUS	MFBO_DCM_STATUS	LCEI_DCM_STATUS	VIP3I_DCM_STATUS	VIP2I_DCM_STATUS	VIPI_DCM_STATUS	UFDI_DCM_STATUS	IMGI_DCM_STATUS
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26	LSCI_DCM_STATUS	0: DCM is on. 1: DCM is off.
25	BPCI_DCM_STATUS	0: DCM is on. 1: DCM is off.
24	AAO_DCM_STATUS	0: DCM is on. 1: DCM is off.
23	LCSO_DCM_STATUS	0: DCM is on. 1: DCM is off.
22	ESFKO_DCM_STATUS	0: DCM is on. 1: DCM is off.
21	RRZO_DCM_STAT	0: DCM is on.

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Bit(s)	Name	Description
	US	1: DCM is off.
20	UFEO_DCM_STATUS	0: DCM is on. 1: DCM is off.
19	IMGO_DCM_STATUS	0: DCM is on. 1: DCM is off.
18	LSCI_D_DCM_STATUS	0: DCM is on. 1: DCM is off.
17	BPCI_D_DCM_STATUS	0: DCM is on. 1: DCM is off.
16	AAO_D_DCM_STATUS	0: DCM is on. 1: DCM is off.
15	LCSO_D_DCM_STATUS	0: DCM is on. 1: DCM is off.
14	AFO_D_DCM_STATUS	0: DCM is on. 1: DCM is off.
13	RRZO_D_DCM_STATUS	0: DCM is on. 1: DCM is off.
12	IMGO_D_DCM_STATUS	0: DCM is on. 1: DCM is off.
11	FEO_DCM_STATUS	0: DCM is on. 1: DCM is off.
10	IMG3CO_DCM_STATUS	0: DCM is on. 1: DCM is off.
9	IMG3BO_DCM_STATUS	0: DCM is on. 1: DCM is off.
8	IMG3O_DCM_STATUS	0: DCM is on. 1: DCM is off.
7	IMG2O_DCM_STATUS	0: DCM is on. 1: DCM is off.
6	MFBO_DCM_STATUS	0: DCM is on. 1: DCM is off.
5	LCEI_DCM_STATUS	0: DCM is on. 1: DCM is off.
4	VIP3I_DCM_STATUS	0: DCM is on. 1: DCM is off.
3	VIP2I_DCM_STATUS	0: DCM is on. 1: DCM is off.
2	VIPI_DCM_STATUS	0: DCM is on. 1: DCM is off.
1	UFDI_DCM_STATUS	0: DCM is on. 1: DCM is off.
0	IMGI_DCM_STATUS	0: DCM is on. 1: DCM is off.

150041AC	**<u>CAM_CTL_RGB_DCM_STATUS</u>**	**CTL_RGB_DCM_STATUS**	**00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										GGM_DCM_STATUS	MFB_DCM_STATUS	C24_DCM_STATUS	G2G_DCM_STATUS	CCL_DCM_STATUS	CFA_DCM_STATUS	SL2_DCM_STATUS
Type										RU	RU	RU	RU	RU	RU	RU
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	GGM_DCM_STATUS	0: DCM is on. 1: DCM is off.
5	MFB_DCM_STATUS	0: DCM is on. 1: DCM is off.
4	C24_DCM_STATUS	0: DCM is on. 1: DCM is off.
3	G2G_DCM_STATUS	0: DCM is on. 1: DCM is off.
2	CCL_DCM_STATUS	0: DCM is on. 1: DCM is off.
1	CFA_DCM_STATUS	0: DCM is on. 1: DCM is off.
0	SL2_DCM_STATUS	0: DCM is on. 1: DCM is off.

150041B0 **CAM_CTL_YUV_DCM_STATUS** **CTL_YUV_DCM_STATUS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													FE_DCM_STATUS	MDPCROP_DCM_STATUS	C24B_DCM_STATUS	CRSP_DCM_STATUS
Type													RU	RU	RU	RU
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIX3_DCM_STATUS	MIX2_DCM_STATUS	MIX1_DCM_STATUS	CRZ_DCM_STATUS	SRZ2_DCM_STATUS	SRZ1_DCM_STATUS	SL2C_DCM_STATUS	SL2B_DCM_STATUS	NR3D_DCM_STATUS	LCE_DCM_STATUS	SEEE_DCM_STATUS	PCA_DCM_STATUS	NBC_DCM_STATUS	C42_DCM_STATUS	G2C_DCM_STATUS	C02_DCM_STATUS
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	FE_DCM_STATUS	0: DCM is on. 1: DCM is off.
18	MDPCROP_DCM_STATUS	0: DCM is on.

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Bit(s)	Name	Description
		1: DCM is off.
17	C24B_DCM_STATUS	0: DCM is on. 1: DCM is off.
16	CRSP_DCM_STATUS	0: DCM is on. 1: DCM is off.
15	MIX3_DCM_STATUS	0: DCM is on. 1: DCM is off.
14	MIX2_DCM_STATUS	0: DCM is on. 1: DCM is off.
13	MIX1_DCM_STATUS	0: DCM is on. 1: DCM is off.
12	CRZ_DCM_STATUS	0: DCM is on. 1: DCM is off.
11	SRZ2_DCM_STATUS	0: DCM is on. 1: DCM is off.
10	SRZ1_DCM_STATUS	0: DCM is on. 1: DCM is off.
9	SL2C_DCM_STATUS	0: DCM is on. 1: DCM is off.
8	SL2B_DCM_STATUS	0: DCM is on. 1: DCM is off.
7	NR3D_DCM_STATUS	0: DCM is on. 1: DCM is off.
6	LCE_DCM_STATUS	0: DCM is on. 1: DCM is off.
5	SEEE_DCM_STATUS	0: DCM is on. 1: DCM is off.
4	PCA_DCM_STATUS	0: DCM is on. 1: DCM is off.
3	NBC_DCM_STATUS	0: DCM is on. 1: DCM is off.
2	C42_DCM_STATUS	0: DCM is on. 1: DCM is off.
1	G2C_DCM_STATUS	0: DCM is on. 1: DCM is off.
0	C02_DCM_STATUS	0: DCM is on. 1: DCM is off.

150041B4 **CAM_CTL_TOP_DCM_STATUS** **CTL_TOP_DCM_STATUS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TDR_DCM_S	FBC_DCM_S	CQ_DCM_ST	TOP_DCM_S

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													TATUS	TATUS	ATUS	TATUS
Type													RU	RU	RU	RU
Reset													0	0	0	0

Bit(s)	Name	Description
3	TDR_DCM_STATUS	0: DCM is on. 1: DCM is off.
2	FBC_DCM_STATUS	0: DCM is on. 1: DCM is off.
1	CQ_DCM_STATUS	0: DCM is on. 1: DCM is off.
0	TOP_DCM_STATUS	0: DCM is on. 1: DCM is off.

150041B8 **CAM_CTL_RAW_REQ_STATUS** **CTL_RAW_REQ_STATUS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						CPG_REQ_STATUS	RMG_REQ_STATUS	EIS_REQ_STATUS	SGG2_REQ_STATUS	AA_REQ_STATUS	HBIN_REQ_STATUS	FLK_REQ_STATUS	AF_REQ_STATUS	SGG1_REQ_STATUS	LCS_REQ_STATUS	UFE_REQ_STATUS
Type						RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAK_REQ_STATUS	BMX_REQ_STATUS	PAKG_REQ_STATUS	RMX_REQ_STATUS	RRZ_REQ_STATUS	RPG_REQ_STATUS	LSC_REQ_STATUS	BNR_REQ_STATUS	OB_REQ_STATUS	W2G_REQ_STATUS	WBN_REQ_STATUS	DMX_REQ_STATUS	TG1_REQ_STATUS	UNP_REQ_STATUS	PGN_REQ_STATUS	UFD_REQ_STATUS
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26	CPG_REQ_STATUS	Request status
25	RMG_REQ_STATUS	Request status
24	EIS_REQ_STATUS	Request status
23	SGG2_REQ_STATUS	Request status
22	AA_REQ_STATUS	Request status
21	HBIN_REQ_STATUS	Request status
20	FLK_REQ_STATUS	Request status
19	AF_REQ_STATUS	Request status
18	SGG1_REQ_STATUS	Request status
17	LCS_REQ_STATUS	Request status
16	UFE_REQ_STATUS	Request status
15	PAK_REQ_STATUS	Request status

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Bit(s)	Name	Description
14	BMX_REQ_STATUS	Request status
13	PAKG_REQ_STATUS	Request status
12	RMX_REQ_STATUS	Request status
11	RRZ_REQ_STATUS	Request status
10	RPG_REQ_STATUS	Request status
9	LSC_REQ_STATUS	Request status
8	BNR_REQ_STATUS	Request status
7	OB_REQ_STATUS	Request status
6	W2G_REQ_STATUS	Request status
5	WBN_REQ_STATUS	Request status
4	DMX_REQ_STATUS	Request status
3	TG1_REQ_STATUS	Request status
2	UNP_REQ_STATUS	Request status
1	PGN_REQ_STATUS	Request status
0	UFD_REQ_STATUS	Request status

150041BC **CAM_CTL_RAW_D_REQ_STATUS** **CTL_RAW_D_REQ_STATUS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						CPG_D_REQ_STATUS	RMG_D_REQ_STATUS			AA_D_REQ_STATUS			AF_D_REQ_STATUS	SGG1_D_REQ_STATUS	LCS_D_REQ_STATUS	
Type						RU	RU			RU			RU	RU	RU	
Reset						0	0			0			0	0	0	
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PAK_D_REQ_STATUS		PAKG_D_REQ_STATUS		RRZ_D_REQ_STATUS	RPG_D_REQ_STATUS	LSC_D_REQ_STATUS	BNR_D_REQ_STATUS	OB_D_REQ_STATUS	W2G_D_REQ_STATUS	WBN_D_REQ_STATUS		TG1_D_REQ_STATUS			
Type	RU		RU		RU	RU	RU	RU	RU	RU	RU		RU			
Reset	0		0		0	0	0	0	0	0	0		0			

Bit(s)	Name	Description
26	CPG_D_REQ_STATUS	Request status
25	RMG_D_REQ_STATUS	Request status
22	AA_D_REQ_STATUS	Request status

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Bit(s)	Name	Description
19	AF_D_REQ_STATUS	Request status
18	SGG1_D_REQ_STATUS	Request status
17	LCS_D_REQ_STATUS	Request status
15	PAK_D_REQ_STATUS	Request status
13	PAKG_D_REQ_STATUS	Request status
11	RRZ_D_REQ_STATUS	Request status
10	RPG_D_REQ_STATUS	Request status
9	LSC_D_REQ_STATUS	Request status
8	BNR_D_REQ_STATUS	Request status
7	OB_D_REQ_STATUS	Request status
6	W2G_D_REQ_STATUS	Request status
5	WBN_D_REQ_STATUS	Request status
3	TG1_D_REQ_STATUS	Request status

150041C0 **CAM_CTL_DMA_REQ_STATUS** **CTL_DMA_REQ_STATUS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LSCI_REQ_STATUS	BPCI_REQ_STATUS	AAO_REQ_STATUS	LCSO_REQ_STATUS	ESFKO_REQ_STATUS	RRZO_REQ_STATUS	UFEO_REQ_STATUS	IMGO_REQ_STATUS	LSCI_D_REQ_STATUS	BPCI_D_REQ_STATUS	AAO_D_REQ_STATUS
Type						RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LCSO_D_REQ_STATUS	AFO_D_REQ_STATUS	RRZO_D_REQ_STATUS	IMGO_D_REQ_STATUS	FEO_REQ_STATUS	IMG3CO_REQ_STATUS	IMG3BO_REQ_STATUS	IMG3O_REQ_STATUS	IMG2O_REQ_STATUS	MFBO_REQ_STATUS	LCEI_REQ_STATUS	VIP3I_REQ_STATUS	VIP2I_REQ_STATUS	VIPI_REQ_STATUS	UFDI_REQ_STATUS	IMGI_REQ_STATUS
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26	LSCI_REQ_STATUS	Request status
25	BPCI_REQ_STATU	Request status

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Bit(s)	Name	Description
	S	
24	AAO_REQ_STATUS	Request status
23	LCSO_REQ_STATUS	Request status
22	ESFKO_REQ_STATUS	Request status
21	RRZO_REQ_STATUS	Request status
20	UFEO_REQ_STATUS	Request status
19	IMGO_REQ_STATUS	Request status
18	LSCI_D_REQ_STATUS	Request status
17	BPCI_D_REQ_STATUS	Request status
16	AAO_D_REQ_STATUS	Request status
15	LCSO_D_REQ_STATUS	Request status
14	AFO_D_REQ_STATUS	Request status
13	RRZO_D_REQ_STATUS	Request status
12	IMGO_D_REQ_STATUS	Request status
11	FEO_REQ_STATUS	Request status
10	IMG3CO_REQ_STATUS	Request status
9	IMG3BO_REQ_STATUS	Request status
8	IMG3O_REQ_STATUS	Request status
7	IMG2O_REQ_STATUS	Request status
6	MFBO_REQ_STATUS	Request status
5	LCEI_REQ_STATUS	Request status
4	VIP3I_REQ_STATUS	Request status
3	VIP2I_REQ_STATUS	Request status
2	VIPI_REQ_STATUS	Request status
1	UFDI_REQ_STATUS	Request status
0	IMGI_REQ_STATUS	Request status

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150041C4 **CAM_CTL_RGB_REQ_STATUS** **CTL_RGB_REQ_STATUS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										GGM_REQ_STATUS	MFB_REQ_STATUS	C24_REQ_STATUS	G2G_REQ_STATUS	CCL_REQ_STATUS	CFA_REQ_STATUS	SL2_REQ_STATUS
Type										RU	RU	RU	RU	RU	RU	RU
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	GGM_REQ_STATUS	Request status
5	MFB_REQ_STATUS	Request status
4	C24_REQ_STATUS	Request status
3	G2G_REQ_STATUS	Request status
2	CCL_REQ_STATUS	Request status
1	CFA_REQ_STATUS	Request status
0	SL2_REQ_STATUS	Request status

150041C8 **CAM_CTL_YUV_REQ_STATUS** **CTL_YUV_REQ_STATUS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													FE_REQ_STATUS	MDPCROP_REQ_STATUS	C24B_REQ_STATUS	CRSP_REQ_STATUS
Type													RU	RU	RU	RU
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIX3_REQ_STATUS	MIX2_REQ_STATUS	MIX1_REQ_STATUS	CRZ_REQ_STATUS	SRZ2_REQ_STATUS	SRZ1_REQ_STATUS	SL2C_REQ_STATUS	SL2B_REQ_STATUS	NR3D_REQ_STATUS	LCE_REQ_STATUS	SEEE_REQ_STATUS	PCA_REQ_STATUS	NBC_REQ_STATUS	C42_REQ_STATUS	G2C_REQ_STATUS	C02_REQ_STATUS
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	FE_REQ_STATUS	Request status
18	MDPCROP_REQ_STATUS	Request status
17	C24B_REQ_STATUS	Request status

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Bit(s)	Name	Description
16	CRSP_REQ_STATUS	Request status
15	MIX3_REQ_STATUS	Request status
14	MIX2_REQ_STATUS	Request status
13	MIX1_REQ_STATUS	Request status
12	CRZ_REQ_STATUS	Request status
11	SRZ2_REQ_STATUS	Request status
10	SRZ1_REQ_STATUS	Request status
9	SL2C_REQ_STATUS	Request status
8	SL2B_REQ_STATUS	Request status
7	NR3D_REQ_STATUS	Request status
6	LCE_REQ_STATUS	Request status
5	SEEE_REQ_STATUS	Request status
4	PCA_REQ_STATUS	Request status
3	NBC_REQ_STATUS	Request status
2	C42_REQ_STATUS	Request status
1	G2C_REQ_STATUS	Request status
0	C02_REQ_STATUS	Request status

150041CC **CAM_CTL_RAW_RDY_STATUS** **CTL_RAW_RDY_STATUS** **07FFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						CPG_RDY_STATUS	RMG_RDY_STATUS	EIS_RDY_STATUS	SGG2_RDY_STATUS	AA_RDY_STATUS	HBIN_RDY_STATUS	FLK_RDY_STATUS	AF_RDY_STATUS	SGG1_RDY_STATUS	LCS_RDY_STATUS	UFE_RDY_STATUS
Type						RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset						1	1	1	1	1	1	1	1	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PAK_RDY_STATUS	BMX_RDY_STATUS	PAKG_RDY_STATUS	RMX_RDY_STATUS	RRZ_RDY_STATUS	RPG_RDY_STATUS	LSC_RDY_STATUS	BNR_RDY_STATUS	OB_RDY_STATUS	W2G_RDY_STATUS	WBN_RDY_STATUS	DMX_RDY_STATUS	TG1_RDY_STATUS	UNP_RDY_STATUS	PGN_RDY_STATUS	UFD_RDY_STATUS
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
26	CPG_RDY_STATUS	Ready status
25	RMG_RDY_STATU	Ready status

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Bit(s)	Name	Description
	S	
24	EIS_RDY_STATUS	Ready status
23	SGG2_RDY_STATUS	Ready status
22	AA_RDY_STATUS	Ready status
21	HBIN_RDY_STATUS	Ready status
20	FLK_RDY_STATUS	Ready status
19	AF_RDY_STATUS	Ready status
18	SGG1_RDY_STATUS	Ready status
17	LCS_RDY_STATUS	Ready status
16	UFE_RDY_STATUS	Ready status
15	PAK_RDY_STATUS	Ready status
14	BMX_RDY_STATUS	Ready status
13	PAKG_RDY_STATUS	Ready status
12	RMX_RDY_STATUS	Ready status
11	RRZ_RDY_STATUS	Ready status
10	RPG_RDY_STATUS	Ready status
9	LSC_RDY_STATUS	Ready status
8	BNR_RDY_STATUS	Ready status
7	OB_RDY_STATUS	Ready status
6	W2G_RDY_STATUS	Ready status
5	WBN_RDY_STATUS	Ready status
4	DMX_RDY_STATUS	Ready status
3	TG1_RDY_STATUS	Ready status
2	UNP_RDY_STATUS	Ready status
1	PGN_RDY_STATUS	Ready status
0	UFD_RDY_STATUS	Ready status

150041D0 **CAM_CTL_RAW_D_RDY_STATUS** **CTL_RAW_D_RDY_STATUS** **064EAFE8**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						CPG_D_RDY_STATUS	RMG_D_RDY_STATUS			AA_D_RDY_STATUS			AF_D_RDY_STATUS	SGG1_D_RDY_STATUS	LCS_D_RDY_STATUS	
Type						RU	RU			RU			RU	RU	RU	
Reset						1	1			1			1	1	1	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAK		PAK		RRZ	RPG	LSC	BNR	OB_	W2G	WB		TG1			

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	_D_ RDY _ST ATU S		G_D _RD Y_S TAT US		_D_ RDY _ST ATU S	_D_ RDY _ST ATU S	_D_ RDY _ST ATU S	_D_ RDY _ST ATU S	D_R DY_ STA TUS	_D_ RDY _ST ATU S	N_D _RD Y_S TAT US		_D_ RDY _ST ATU S			
Type	RU		RU		RU	RU	RU	RU	RU	RU	RU		RU			
Reset	1		1		1	1	1	1	1	1	1		1			

Bit(s)	Name	Description
26	CPG_D_RDY_STATUS	Ready status
25	RMG_D_RDY_STATUS	Ready status
22	AA_D_RDY_STATUS	Ready status
19	AF_D_RDY_STATUS	Ready status
18	SGG1_D_RDY_STATUS	Ready status
17	LCS_D_RDY_STATUS	Ready status
15	PAK_D_RDY_STATUS	Ready status
13	PAKG_D_RDY_STATUS	Ready status
11	RRZ_D_RDY_STATUS	Ready status
10	RPG_D_RDY_STATUS	Ready status
9	LSC_D_RDY_STATUS	Ready status
8	BNR_D_RDY_STATUS	Ready status
7	OB_D_RDY_STATUS	Ready status
6	W2G_D_RDY_STATUS	Ready status
5	WBN_D_RDY_STATUS	Ready status
3	TG1_D_RDY_STATUS	Ready status

150041D4 **CAM_CTL_DMA_RDY_STATUS** **CTL_DMA_RDY_STATUS** **07FFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LSCI_RDY_STATUS	BPCI_RDY_STATUS	AAO_RDY_STATUS	LCSO_RDY_STATUS	ESFKO_RDY_STATUS	RRZO_RDY_STATUS	UFEO_RDY_STATUS	IMGO_RDY_STATUS	LSCI_D_RDY_STATUS	BPCI_D_RDY_STATUS	AAO_D_RDY_STATUS
Type						RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset						1	1	1	1	1	1	1	1	1	1	1

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LCSO_D_RDY_STATUS	AFO_D_RDY_STATUS	RRZO_D_RDY_STATUS	IMGO_D_RDY_STATUS	FEO_RDY_STATUS	IMG3CO_RDY_STATUS	IMG3BO_RDY_STATUS	IMG3O_RDY_STATUS	IMG2O_RDY_STATUS	MFBO_RDY_STATUS	LCEI_RDY_STATUS	VIP3I_RDY_STATUS	VIP2I_RDY_STATUS	VIPI_RDY_STATUS	UFDI_RDY_STATUS	IMGI_RDY_STATUS
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
26	LSCI_RDY_STATUS	Ready status
25	BPCI_RDY_STATUS	Ready status
24	AAO_RDY_STATUS	Ready status
23	LCSO_RDY_STATUS	Ready status
22	ESFKO_RDY_STATUS	Ready status
21	RRZO_RDY_STATUS	Ready status
20	UFEO_RDY_STATUS	Ready status
19	IMGO_RDY_STATUS	Ready status
18	LSCI_D_RDY_STATUS	Ready status
17	BPCI_D_RDY_STATUS	Ready status
16	AAO_D_RDY_STATUS	Ready status
15	LCSO_D_RDY_STATUS	Ready status
14	AFO_D_RDY_STATUS	Ready status
13	RRZO_D_RDY_STATUS	Ready status
12	IMGO_D_RDY_STATUS	Ready status
11	FEO_RDY_STATUS	Ready status
10	IMG3CO_RDY_STATUS	Ready status
9	IMG3BO_RDY_STATUS	Ready status
8	IMG3O_RDY_STATUS	Ready status
7	IMG2O_RDY_STATUS	Ready status
6	MFBO_RDY_STATUS	Ready status
5	LCEI_RDY_STATUS	Ready status
4	VIP3I_RDY_STATUS	Ready status

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Bit(s)	Name	Description
3	VIP2I_RDY_STATUS	Ready status
2	VIPI_RDY_STATUS	Ready status
1	UFDI_RDY_STATUS	Ready status
0	IMGI_RDY_STATUS	Ready status

150041D8 **CAM_CTL_RGB_RDY_STATUS** **CTL_RGB_RDY_STATUS** **0000007F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										GGM_RDY_STATUS	MFB_RDY_STATUS	C24_RDY_STATUS	G2G_RDY_STATUS	CCL_RDY_STATUS	CFA_RDY_STATUS	SL2_RDY_STATUS
Type										RU	RU	RU	RU	RU	RU	RU
Reset										1	1	1	1	1	1	1

Bit(s)	Name	Description
6	GGM_RDY_STATUS	Ready status
5	MFB_RDY_STATUS	Ready status
4	C24_RDY_STATUS	Ready status
3	G2G_RDY_STATUS	Ready status
2	CCL_RDY_STATUS	Ready status
1	CFA_RDY_STATUS	Ready status
0	SL2_RDY_STATUS	Ready status

150041DC **CAM_CTL_YUV_RDY_STATUS** **CTL_YUV_RDY_STATUS** **000FFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													FE_RDY_STATUS	MDP CROP_RDY_STATUS	C24B_RDY_STATUS	CRSP_RDY_STATUS
Type													RU	RU	RU	RU
Reset													1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIX3_RDY_	MIX2_RDY_	MIX1_RDY_	CRZ_RDY_S	SRZ2_RDY_	SRZ1_RDY_	SL2C_RDY_	SL2B_RDY_	NR3D_RDY_	LCE_RDY_S	SEEE_RDY_	PCA_RDY_S	NBC_RDY_S	C42_RDY_S	G2C_RDY_S	C02_RDY_S

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	STA TUS	STA TUS	STA TUS	TAT US	STA TUS	STA TUS	STA TUS	STA TUS	STA TUS	TAT US	STA TUS	TAT US	TAT US	TAT US	TAT US	TAT US
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
19	FE_RDY_STATUS	Ready status
18	MDPCROP_RDY_STATUS	Ready status
17	C24B_RDY_STATUS	Ready status
16	CRSP_RDY_STATUS	Ready status
15	MIX3_RDY_STATUS	Ready status
14	MIX2_RDY_STATUS	Ready status
13	MIX1_RDY_STATUS	Ready status
12	CRZ_RDY_STATUS	Ready status
11	SRZ2_RDY_STATUS	Ready status
10	SRZ1_RDY_STATUS	Ready status
9	SL2C_RDY_STATUS	Ready status
8	SL2B_RDY_STATUS	Ready status
7	NR3D_RDY_STATUS	Ready status
6	LCE_RDY_STATUS	Ready status
5	SEEE_RDY_STATUS	Ready status
4	PCA_RDY_STATUS	Ready status
3	NBC_RDY_STATUS	Ready status
2	C42_RDY_STATUS	Ready status
1	G2C_RDY_STATUS	Ready status
0	C02_RDY_STATUS	Ready status

15004410 **CAM_TG_SEN_MODE** **Sensor Mode** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**PXL_CNT_RST_SRC**	**EOF_SRC**		**SOF_SRC**						**SOT_CLR_MODE**	**SOT_MODE**	**DBL_DATA_BUS**	**CMOS_EN**
Type				RW	RW		RW						RW	RW	RW	RW
Reset				0	0	0	0	0					0	0	0	0

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Bit(s)	Name	Description
12	PXL_CNT_RST_SRC	**Pixel counter reset source** 0: Vsync rising edge (default) 1: Vsync falling edge
11:10	EOF_SRC	**End of frame source** 0: Line count reaches LIN_END. Pixel count reaches PXL_END (only this case). 1: Vsync rising edge 2: Vsync falling edge 3: pixel_cnt reaches EOT_CNT.
9:8	SOF_SRC	**Start of frame source** 0: Vsync rising edge 1: Vsync falling edge 2: pixel_cnt reaches SOF_CNT.
3	SOT_CLR_MODE	**SOT RGB/YUV mode** 0: Choose SOT_MODE selection 1: SOT position before data 1T. Only for RGB, YUV and JPG (default case)
2	SOT_MODE	**SOT mode** 0: SOT position is at SOT_CNT. 1: SOT position is sof_1d (fixed to this).
1	DBL_DATA_BUS	**Doubles asynchronous FIFO data bus** For YUV422, RGB565 or JPEG mode, this bit can be set to 1'b1. For RAW/RGB888 mode, this bit must be 1'b0.
0	CMOS_EN	**Enables CMOS**

15004414 **CAM_TG_VF_CON** **VF Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				SPDELAY_MODE		SP_DELAY				FR_CON					SINGLE_MODE	VFDATA_EN
Type				RW		RW				RW					RW	RW
Reset				0		0	0	0		0	0	0			0	0

Bit(s)	Name	Description
12	SPDELAY_MODE	**SP delay mode** 0: Count by vsync 1: Count by grab window
10:8	SP_DELAY	**Still picture mode frame delay** When SP_DELAY is non-zero, TAKE_PIC will start to trigger after SP_DELAY frames.
6:4	FR_CON	**Controls frame sampling rate** 000: Every frame is sampled. 001: One frame is sampled every 2 frames. 010: One frame is sampled every 3 frames. 011: One frame is sampled every 4 frames. 100: One frame is sampled every 5 frames. 101: One frame is sampled every 6 frames.

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Bit(s)	Name	Description
		110: One frame is sampled every 7 frames. 111: One frame is sampled every 8 frames.
1	SINGLE_MODE	**Single mode** 0: Continuous mode 1: Single mode
0	VFDATA_EN	**Take picture request**

15004418 **CAM_TG_SEN_GRAB_PXL** **Sensor Grab Pixel Start/End** **7FFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		PXL_E														
Type		RW														
Reset		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PXL_S														
Type		RW														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:16	PXL_E	**Grab end pixel clock number** Image size = PIXL_E-PIXL_S
14:0	PXL_S	**Grab start pixel clock number** The first pixel starts from 0.

1500441C **CAM_TG_SEN_GRAB_LIN** **Sensor Grab Line Start/End** **1FFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LIN_E												
Type				RW												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				LIN_S												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	LIN_E	**Grab end line number** Image height = LINE_E - LINE_S
12:0	LIN_S	**Grab start line number** The first line starts from 0.

15004420 **CAM_TG_PATH_CFG** **TG Path Config** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	**DROP_CNT**				**WCNT**				**RCNT**				**FB_NUM**			
Type	RO				RO				RO				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**LOCK_EN**	**FBC_EN**	**YUV_BIN_EN**	**YUV_U2S_DIS**	**RCNT_INC**	**DB_LOAD_VSPOL**	**DB_LOAD_SRC**	**DB_LOAD_DIS**	**JPG_LINEND_EN**		**MEMIN_EN**	**JPGINF_EN**			**SEN_IN_LSB**	
Type	RW	RW	RW	RW	WO	RW	RW	RW	RW		RW	RW			RW	
Reset	0	0	0	0	0	0	0	0	0		0	0			0	0

Bit(s)	Name	Description
31:28	DROP_CNT	**Drop frame counter**
27:24	WCNT	**HW increases 1 when Pass1 done occurs.**
23:20	RCNT	
19:16	FB_NUM	
15	LOCK_EN	**Enables drame buffer lock**
14	FBC_EN	**Enables frame buffer**
13	YUV_BIN_EN	**Enables YUV binning**
12	YUV_U2S_DIS	**Disables YUV sensor unsigned to signed**
11	RCNT_INC	**Increases frame buffer control RCNT by writing 1**
10	DB_LOAD_VSPOL	**Double buffer load, vsync polarity** 1'b0: Vsync rises. (Fixed to this value) 1'b1: Vsync falls.
9	DB_LOAD_SRC	**Double buffer load source** 1'b0: TG vs rising edge after polarity 1'b1: External source (DBG mode)
8	DB_LOAD_DIS	**Disables double buffer load** 1'b0: Enable. Only load when db_load is high. 1'b1: Disable. Always load.
7	JPG_LINEND_EN	**Enables JPEG interface line mode** 1'b0: JPG frame end is vsync signal. 1'b1: JPG frame end is hsync signal.
5	MEMIN_EN	**Enables memory input**
4	JPGINF_EN	**Enables JPEG interface**
1:0	SEN_IN_LSB	**Selects sensor input data bit order** Used in ISP YUV422/RGB888/RGB565/Bayer format. Data input in ISP is 12-bit, datain[11:0] (moved to seninf top). 0: datain[11:0] as TG data input 1: datain[9:0] as TG data input 2: datain[7:0] as TG data input

15004424 **CAM_TG_MEMIN_CTL** **MEMIN Control** **00001430**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													**FBC_CNT**			
Type													RO			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**MEMIN_DUMMYLIN**					**MEMIN_DUMMYPXL**							
Type				RW					RW							
Reset				1	0	1	0	0	0	0	1	1	0	0	0	0

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Bit(s)	Name	Description
19:16	FBC_CNT	Available frame buffer counter
12:8	MEMIN_DUMMYLIN	
7:0	MEMIN_DUMMYPXL	

15004428 **CAM_TG_INT1** **TG Interrupt 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**VSYNC_INT_POL**	**TG_INT1_PXLNO**														
Type	RW	RW														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**TG_INT1_LINENO**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	VSYNC_INT_POL	**Vsync interrupt polarity** 0: Rising eage 1: Falling edge
30:16	TG_INT1_PXLNO	**TG Interrupt1 pixel number**
12:0	TG_INT1_LINENO	**TG Interrupt1 line number**

1500442C **CAM_TG_INT2** **TG Interrupt 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**TG_INT2_PXLNO**														
Type		RW														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**TG_INT2_LINENO**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:16	TG_INT2_PXLNO	TG Interrupt2 pixel number
12:0	TG_INT2_LINENO	TG Interrupt2 line number

15004430 **CAM_TG_SOF_CNT** **TG SOF CNT** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name					**SOF_CNT[27:16]**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SOF_CNT[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:0	SOF_CNT	User specified SOF count

15004434 CAM_TG_SOT_CNT TG SOT CNT 00000010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**SOT_CNT[27:16]**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SOT_CNT[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
27:0	SOT_CNT	User specified SOT count

15004438 CAM_TG_EOT_CNT TG EOT CNT 0FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**EOT_CNT[27:16]**											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EOT_CNT[15:0]**															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27:0	EOT_CNT	User specified EOT count

1500443C CAM_TG_ERR_CTL TG Error CTL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									**DBG_SRC_SEL**							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**REZ_OV**	**REZ_OVRUN_FLIMIT_NO**						**GRAB_E**	**GRAB_E**	**GRAB_ERR_FLIMIT_NO**			

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				RUN_FLIMIT_EN							RR_EN	RR_FLIMIT_EN				
Type				RW	RW						RW	RW	RW			
Reset				0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
23:16	DBG_SRC_SEL	
12	REZ_OVRUN_FLIMIT_EN	**Enables camera to CRZ interface overrun frame count limit**
11:8	REZ_OVRUN_FLIMIT_NO	
5	GRAB_ERR_EN	**Enables TG grab error frame limit**
4	GRAB_ERR_FLIMIT_EN	**Enables TG grab error frame limit** Only for single mode
3:0	GRAB_ERR_FLIMIT_NO	**TG grab error frame limit number** Only for single mode

15004440 **CAM_TG_DAT_NO** **TG Out Data Num** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DAT_NO[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DAT_NO[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DAT_NO	**TG output data number** 1. For JPEG, RGB and YUV format, it is equal to byte count. 2. For RAW format, it is data count.

15004444 **CAM_TG_FRM_CNT_ST** **TG_FRM_CNT_ST** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**GRAB_ERR_FCNT**								**REZ_OVRUN_FCNT**			
Type					RO								RO			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
11:8	GRAB_ERR_FCNT	**Grab error frame count** This frame count is for still mode. It will be reset every time TAK_PIC is set to 0 and add 1 when GRAB_ERR occurs in a frame.

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Bit(s)	Name	Description
3:0	REZ_OVRUN_FCNT	**Camera to resizer (or out) interface overrun frame count** This frame count is for still mode. It will be reset every time TAK_PIC is set to 0 and add 1 when REZOVRUN occurs in a frame.

15004448 **CAM_TG_FRMSIZE_ST** **TG FRM SIZE ST** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		PXL_CNT														
Type		RO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				LINE_CNT												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:16	PXL_CNT	Input frame line counter
12:0	LINE_CNT	Input frame pixel counter

1500444C **CAM_TG_INTER_ST** **TG INTER ST** **00000102**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CAM_FRM_CNT							
Type									RO							
Reset									0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name			TG_CAM_CS											OUT_REQ	OUT_RDY	SYN_VF_DATA_EN
Type			RO											RO	RO	RO
Reset			0	0	0	0	0	1						0	1	0

Bit(s)	Name	Description
23:16	CAM_FRM_CNT	**Input frame counter**
13:8	TG_CAM_CS	**TG state** 6'h1: IDLE 6'h2: VFON_EXP 6'h4: VFON_IDLE 6'h8: VFON_WAIT 6'h10: CAP_EXP 6'h20: CAP_IDLE
2	OUT_REQ	**out req**
1	OUT_RDY	**out rdy**
0	SYN_VF_DATA_EN	**View finder double buffer register status**

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15004460 **CAM_TG_FLASHA_CTL** **FLASHA Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				FLASH_POL		FLASHA_END_FRM					FLASHA_STARTPNT				FLASH_EN	FLASHA_EN
Type				RW		RW					RW				RW	RW
Reset				0		0	0	0			0	0			0	0

Bit(s)	Name	Description
12	FLASH_POL	**Flash line polarity**
10:8	FLASHA_END_FRM	**FlashA end frame**
5:4	FLASHA_STARTPNT	**FlashA frame count start point** 0: Start from vsync rising 1: Start from vsync falling 2: Start from readoutdone
1	FLASH_EN	**Enables Flash**
0	FLASHA_EN	**Enables FlashA** If flahs_en=0, this bit should also be 0. 0: Enable FlashA 1: Disable FlashA

15004464 **CAM_TG_FLASHA_LINE_CNT** **FLASHA Line Count** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FLASHA_LUNIT				FLASHA_LUNIT_NO[19:16]			
Type									RW				RW			
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FLASHA_LUNIT_NO[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:20	FLASHA_LUNIT	**FlashA line unit** 0~15 lines in rolling shutter mode.
19:0	FLASHA_LUNIT_NO	**FlashA line unit count**

15004468 **CAM_TG_FLASHA_POS** **FLASHA POS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				FLASHA_LINE												
Type				RW												

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Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		FLASHA_PXL														
Type		RW														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	FLASHA_LINE	**FlashA start line**
14:0	FLASHA_PXL	**FlashA start pixel** *Note:* *1. Start pixel cannot be set to 0.* *2. In 1-pixel mode, it can be even or odd.* *3. In 2-pixel mode, it can only be even.*

1500446C CAM_TG_FLASHB_CTL FLASHB Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		FLASHB_CONT_FRM			FLASHB_START_FRM						FLASHB_STARTPNT				FLASHB_TRIG_SRC	FLASHB_EN
Type		RW			RW						RW				RW	RW
Reset		0	0	0	0	0	0	0			0	0			0	0

Bit(s)	Name	Description
14:12	FLASHB_CONT_FRM	**FlashB continuous frame count**
11:8	FLASHB_START_FRM	**FlashB start frame count**
5:4	FLASHB_STARTPNT	**FlashB start point** 0: Start from vsync rising 1: Start from vsync falling 2: Start from readoutdone
1	FLASHB_TRIG_SRC	**FlashB trigger source** 1'b0: hsync and pixel clock 1'b1: Cam cycle count
0	FLASHB_EN	**Enables FlashB** If flahs_en=0, this bit should also be 0. 0: Enable FlashB 1: Disable FlashB

15004470 CAM_TG_FLASHB_LINE_CNT FLASHB Line Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FLASHB_LUNIT				FLASHB_LUNIT_NO[19:16]			

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Type									RW				RW			
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**FLASHB_LUNIT_NO[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:20	FLASHB_LUNIT	**FlashB line unit** 0~15 lines in rolling shutter mode
19:0	FLASHB_LUNIT_NO	**FlashB line unit count**

15004474 **CAM_TG_FLASHB_POS** **FLASHB POS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**FLASHB_LINE**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**FLASHB_PXL**														
Type		RW														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	FLASHB_LINE	**FlashB start line**
14:0	FLASHB_PXL	**FlashB start pixel** *Note:* *1. Start pixel cannot be set to 0.* *2. In 1-pixel mode, it can be even or odd.* *3. For 2-pixel mode, it can only be even.*

15004478 **CAM_TG_FLASHB_POS1** **FLASHB POS1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													**FLASHB_CYC_CNT[19:16]**			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**FLASHB_CYC_CNT[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	FLASHB_CYC_CNT	**FlashB start cycle count** FLASHB start cycle count = FLASHB_CYC_CNT*256

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150044F0 **CAM_HBN_SIZE** **HBN_SIZE** **0F3C14B4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**HBN_IN_V**												
Type				RW												
Reset				0	1	1	1	1	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**HBN_IN_H**												
Type				RW												
Reset				1	0	1	0	0	1	0	1	1	0	1	0	0

Bit(s)	Name	Description
28:16	HBN_IN_V	**Binning module input vertical resolution** Max. value: 3,900
12:0	HBN_IN_H	**Binning module input horizontal resolution** Max. value: 5,300

150044F4 **CAM_HBN_MODE** **HBN_MODE** **00000010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**HBIN_EN**			**HBIN_ACC**	
Type												RW			RW	
Reset												1			0	0

Bit(s)	Name	Description
4	HBIN_EN	**Enables binning function** Binning can be enabled only if the input image width % 4 = 0. 0: Disable
1:0	HBIN_ACC	**Binning mode** 0: (1 1) filter, gain = 2 1: (1 1) filter, gain = 1 2: (3 1) + (1 3) filter, gain = 4 3: (1 2 1) + (1 3 3 1) filter, gain = 4 and 8

15004500 **CAM_OBC_OFFST0** **OBC Offset 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**OBC_OFST_B**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
12:0	OBC_OFST_B	Optical black offset for B channel [-4096~4095]

15004504 **CAM_OBC_OFFST1** **OBC Offset 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OBC_OFST_GR												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	OBC_OFST_GR	Optical black offset for GR channel [-4096~4095]

15004508 **CAM_OBC_OFFST2** **OBC Offset 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OBC_OFST_GB												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	OBC_OFST_GB	Optical black offset for GB channel [-4096~4095]

1500450C **CAM_OBC_OFFST3** **OBC Offset 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OBC_OFST_R												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	OBC_OFST_R	Optical black offset for R channel [-4096~4095]

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15004510 **CAM_OBC_GAIN0** **OBC Gain 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OBC_GAIN_B												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	OBC_GAIN_B	Optical black register gain for B channel [0~8191]

15004514 **CAM_OBC_GAIN1** **OBC Gain 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OBC_GAIN_GR												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	OBC_GAIN_GR	Optical black register offset for GR channel [0~8191]

15004518 **CAM_OBC_GAIN2** **OBC Gain 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OBC_GAIN_GB												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	OBC_GAIN_GB	Optical black register offset for GB channel [0~8191]

1500451C **CAM_OBC_GAIN3** **OBC Gain 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OBC_GAIN_R												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	OBC_GAIN_R	Optical black register offset for R channel [0~8191]

15004530 CAM_LSC_CTL1 Shading Control 2 Register 20000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			LSC_PRC_MODE	SD_ULTRA_MODE				SD_COEFRD_MODE			SDBLK_XOFST					
Type			RW	RW				RW			RW					
Reset			1	0				0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											SDBLK_YOFST					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
29	LSC_PRC_MODE	**LSC coeff00 signed unsigned switch (i.e. x4 x8 switch)** 0: Original, coeff00 considered as signed, max. x4 (but coeff00 with negative value will be protected, which will result in x1.) 1: coef00 considered as unsigned, max. x8
28	SD_ULTRA_MODE	**Shading ultra read mode**
24	SD_COEFRD_MODE	**Shading coefficient read mode**
21:16	SDBLK_XOFST	**x directional address offset**
5:0	SDBLK_YOFST	**y directional address offset**

15004534 CAM_LSC_CTL2 Shading Control 2 Register 00006000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															LSC_OFLN	LSC_SDBLK_XNUM[4:4]
Type															RW	W1
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LSC_SDBLK_XNUM[3:0]				LSC_SDBLK_WIDTH											
Type	W1				RW											
Reset	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
17	LSC_OFLN	0: Online 1: Offline
16:12	LSC_SDBLK_XNUM	x directional number of block
11:0	LSC_SDBLK_WIDTH	Block width in x direction

15004538 CAM_LSC_CTL3 LSC Spare Register 00006000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LSC_SPARE															LSC_SDBLK_YNUM[4:4]
Type	RW															W1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LSC_SDBLK_YNUM[3:0]				LSC_SDBLK_HEIGHT											
Type	W1				RW											
Reset	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:17	LSC_SPARE	LSC spare register
16:12	LSC_SDBLK_YNUM	y directional number of block
11:0	LSC_SDBLK_HEIGHT	Block height in y direction

1500453C CAM_LSC_LBLOCK Shading Last Block Config Register 00FF00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					LSC_SDBLK_lWIDTH											
Type					RW											
Reset					0	0	0	0	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					LSC_SDBLK_lHEIGHT											
Type					RW											
Reset					0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27:16	LSC_SDBLK_lWIDTH	Last block width
11:0	LSC_SDBLK_lHEIGHT	Last block height

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15004540 CAM_LSC_RATIO Shading Ratio Config Register 20202020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			LSC_RA0								LSC_RA1					
Type			W1								W1					
Reset			1	0	0	0	0	0			1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			LSC_RA2								LSC_RA3					
Type			W1								W1					
Reset			1	0	0	0	0	0			1	0	0	0	0	0

Bit(s)	Name	Description
29:24	LSC_RA0	Shading ratio of channel 0
21:16	LSC_RA1	Shading ratio of channel 1
13:8	LSC_RA2	Shading ratio of channel 2
5:0	LSC_RA3	Shading ratio of channel 3

15004544 CAM_LSC_TPIPE_OFST Shading TPIPE Offset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					LSC_TPIPE_OFST_X											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					LSC_TPIPE_OFST_Y											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	LSC_TPIPE_OFST_X	Shading TPIPE x offset to block boundary
11:0	LSC_TPIPE_OFST_Y	Shading TPIPE y offset to block boundary

15004548 CAM_LSC_TPIPE_SIZE Shading TPIPE Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LSC_TPIPE_SIZE_X												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				LSC_TPIPE_SIZE_Y												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	LSC_TPIPE_SIZE_X	Shading TPIPE x size
12:0	LSC_TPIPE_SIZE_Y	Shading TPIPE y size

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1500454C CAM_LSC_GAIN_TH Shading Gain Threshold Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LSC_GAIN_TH0										LSC_GAIN_TH1[8:6]		
Type				W1										W1		
Reset				0	0	0	0	0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LSC_GAIN_TH1[5:0]							LSC_GAIN_TH2								
Type	W1							W1								
Reset	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:20	LSC_GAIN_TH0	Shading gain link threshold 0
18:10	LSC_GAIN_TH1	Shading gain link threshold 1
8:0	LSC_GAIN_TH2	Shading gain link threshold 2

15004550 CAM_RPG_SATU_1 RPG_SATU_1 0FFF0FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RPG_SATU_GB											
Type					USER0											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RPG_SATU_B											
Type					USER0											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27:16	RPG_SATU_GB	**Double buffer** Q0.12.0: Saturation clip for Gb
11:0	RPG_SATU_B	**Double buffer** Q0.12.0: Saturation clip for B

15004554 CAM_RPG_SATU_2 RPG_SATU_2 0FFF0FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RPG_SATU_R											
Type					USER0											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RPG_SATU_GR											
Type					USER0											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description

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Bit(s)	Name	Description
27:16	RPG_SATU_R	**Double buffer** Q0.12.0: Saturation clip for R
11:0	RPG_SATU_GR	**Double buffer** Q0.12.0: Saturation clip for Gr

15004558 **CAM_RPG_GAIN_1** **RPG_GAIN_1** **02000200**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RPG_GAIN_GB												
Type				USER0												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RPG_GAIN_B												
Type				USER0												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	RPG_GAIN_GB	**Double buffer** Q0.4.9: Gain for Gb
12:0	RPG_GAIN_B	**Double buffer** Q0.4.9: Gain for B

1500455C **CAM_RPG_GAIN_2** **RPG_GAIN_2** **02000200**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RPG_GAIN_R												
Type				USER0												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RPG_GAIN_GR												
Type				USER0												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	RPG_GAIN_R	**Double buffer** Q0.4.9: Gain for R
12:0	RPG_GAIN_GR	**Double buffer** Q0.4.9: Gain for Gr

15004560 **CAM_RPG_OFST_1** **RPG_OFST_1** **00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RPG_OFST_GB											
Type					USERO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RPG_OFST_B											
Type					USERO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	RPG_OFST_GB	**Double buffer** Q1.11.0: Offset for Gb
11:0	RPG_OFST_B	**Double buffer** Q1.11.0: Offset for B

15004564 **CAM_RPG_OFST_2** **RPG_OFST_2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RPG_OFST_R											
Type					USERO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RPG_OFST_GR											
Type					USERO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	RPG_OFST_R	**Double buffer** Q1.11.0: Offset for R
11:0	RPG_OFST_GR	**Double buffer** Q1.11.0: Offset for Gr

15004580 **CAM_SGG2_PGN** **SGG PGN** **00000010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						SGG2_GAIN										
Type						RW										
Reset						0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
10:0	SGG2_GAIN	**Double buffer** SGG pre-gain for low contrast scene (Q0.7.4)

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15004584 CAM_SGG2_GMRC_1 SGG GMRC 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SGG2_GMR_4								SGG2_GMR_3							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SGG2_GMR_2								SGG2_GMR_1							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	SGG2_GMR_4	**Double buffer** SGG gamma control point 4 (256)
23:16	SGG2_GMR_3	**Double buffer** SGG gamma control point 3 (128)
15:8	SGG2_GMR_2	**Double buffer** SGG gamma control point 2 (64)
7:0	SGG2_GMR_1	**Double buffer** SGG gamma control point 1 (32)

15004588 CAM_SGG2_GMRC_2 SGG GMRC 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									SGG2_GMR_7							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SGG2_GMR_6								SGG2_GMR_5							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	SGG2_GMR_7	**Double buffer** SGG gamma control point 7 (2048)
15:8	SGG2_GMR_6	**Double buffer** SGG gamma control point 6 (1024)
7:0	SGG2_GMR_5	**Double buffer** SGG gamma control point 5 (512)

150045B0 CAM_AWB_WIN_ORG AWB Window Origin 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AWB_W_VORG												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AWB_W_HORG												

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Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	AWB_W_VORG	AWB window origin y
12:0	AWB_W_HORG	AWB window origin x

150045B4 CAM_AWB_WIN_SIZE AWB Window Size 00020004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AWB_W_VSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AWB_W_HSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
28:16	AWB_W_VSIZE	AWB window size y
12:0	AWB_W_HSIZE	AWB window size x

150045B8 CAM_AWB_WIN_PIT AWB Window Pitch 00020004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AWB_W_VPIT												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AWB_W_HPIT												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
28:16	AWB_W_VPIT	AWB window pitch y
12:0	AWB_W_HPIT	AWB window pitch x

150045BC CAM_AWB_WIN_NUM AWB Window Number 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AWB_W_VNUM							
Type									RW							
Reset									0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AWB_W_HNUM							
Type									RW							
Reset									0	0	0	0	0	0	0	1

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Bit(s)	Name	Description
23:16	AWB_W_VNUM	AWB window number y
7:0	AWB_W_HNUM	AWB window number x

150045C0 CAM_AWB_GAIN1_0 AWB Raw PreGain1 R/G 02000200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AWB_GAIN1_G												
Type				RW												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				AWB_GAIN1_R												
Type				RW												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	AWB_GAIN1_G	Statistic RawPreGain1 G
12:0	AWB_GAIN1_R	Statistic RawPreGain1 R

150045C4 CAM_AWB_GAIN1_1 AWB Raw PreGain1 B 00000200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				AWB_GAIN1_B												
Type				RW												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	AWB_GAIN1_B	Statistic RawPreGain1 B

150045C8 CAM_AWB_LMT1_0 AWB Raw Limit1 R/G 0FFF0FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					AWB_LMT1_G											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					AWB_LMT1_R											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27:16	AWB_LMT1_G	Statistic RawLimit1 G
11:0	AWB_LMT1_R	Statistic RawLimit1 R

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150045CC CAM_AWB_LMT1_1 AWB Raw Limit1 B 00000FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AWB_LMT1_B											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
11:0	AWB_LMT1_B	Statistic RawLimit1 B

150045D0 CAM_AWB_LOW_THR AWB Low Threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AWB_LOW_THR2							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AWB_LOW_THR1								AWB_LOW_THR0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	AWB_LOW_THR2	AWB low threshold 2
15:8	AWB_LOW_THR1	AWB low threshold 1
7:0	AWB_LOW_THR0	AWB low threshold 0

150045D4 CAM_AWB_HI_THR AWB High Threshod 00FFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AWB_HI_THR2							
Type									RW							
Reset									1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AWB_HI_THR1								AWB_HI_THR0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
23:16	AWB_HI_THR2	AWB high threshold 2
15:8	AWB_HI_THR1	AWB high threshold 1
7:0	AWB_HI_THR0	AWB high threshold 0

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150045D8	CAM_AWB_PIXEL_CNT0	AWB Pixel CNT 0	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AWB_PIXEL_CNT0[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AWB_PIXEL_CNT0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	AWB_PIXEL_CNT0	AWB window pixel count, R

150045DC	CAM_AWB_PIXEL_CNT1	AWB Pixel CNT 1	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AWB_PIXEL_CNT1[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AWB_PIXEL_CNT1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	AWB_PIXEL_CNT1	AWB window pixel count, G

150045E0	CAM_AWB_PIXEL_CNT2	AWB Pixel CNT 2	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AWB_PIXEL_CNT2[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AWB_PIXEL_CNT2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	AWB_PIXEL_CNT2	AWB window pixel count, B

150045E4	CAM_AWB_ERR_THR	AWB Error Threshold	00000100

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														AWB_ERR_SFT		
Type														RW		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AWB_ERR_THR											
Type					RW											
Reset					0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
18:16	AWB_ERR_SFT	AWB truncate bit
11:0	AWB_ERR_THR	AWB error threshold

150045E8 CAM_AWB_ROT AWB Rotation Parameter 00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							AWB_S									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							AWB_C									
Type							RW									
Reset							0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	AWB_S	AWB rotation: Sine (Q1.1.8)
9:0	AWB_C	AWB rotation: Cosine (Q1.1.8)

150045EC CAM_AWB_Lo_X AWB Lighto x Region 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_Lo_X_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_Lo_X_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_Lo_X_UP	AWB Lighto Rx up
13:0	AWB_Lo_X_LOW	AWB Lighto Rx low

150045F0 CAM_AWB_Lo_Y AWB Lighto y Region 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_Lo_Y_UP													
Type			RW													

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Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**AWB_L0_Y_LOW**													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L0_Y_UP	AWB Light0 Ry up
13:0	AWB_L0_Y_LOW	AWB Light0 Ry low

150045F4 CAM_AWB_L1_X AWB Light1 x Region 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			**AWB_L1_X_UP**													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**AWB_L1_X_LOW**													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L1_X_UP	AWB Light1 Rx up
13:0	AWB_L1_X_LOW	AWB Light1 Rx low

150045F8 CAM_AWB_L1_Y AWB Light1 y Region 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			**AWB_L1_Y_UP**													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**AWB_L1_Y_LOW**													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L1_Y_UP	AWB Light1 Ry up
13:0	AWB_L1_Y_LOW	AWB Light1 Ry low

150045FC CAM_AWB_L2_X AWB Light2 x Region 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			**AWB_L2_X_UP**													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**AWB_L2_X_LOW**													

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Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L2_X_UP	AWB Light2 Rx up
13:0	AWB_L2_X_LOW	AWB Light2 Rx low

15004600 CAM_AWB_L2_Y AWB Light2 y Region 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L2_Y_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L2_Y_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L2_Y_UP	AWB Light2 Ry up
13:0	AWB_L2_Y_LOW	AWB Light2 Ry low

15004604 CAM_AWB_L3_X AWB Light3 x Region 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L3_X_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L3_X_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L3_X_UP	AWB Light3 Rx up
13:0	AWB_L3_X_LOW	AWB Light3 Rx low

15004608 CAM_AWB_L3_Y AWB Light3 y Region 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L3_Y_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L3_Y_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
29:16	AWB_L3_Y_UP	AWB Light3 Ry up
13:0	AWB_L3_Y_LOW	AWB Light3 Ry low

1500460C CAM_AWB_L4_X AWB Light4 x Region 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L4_X_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L4_X_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L4_X_UP	AWB Light4 Rx up
13:0	AWB_L4_X_LOW	AWB Light4 Rx low

15004610 CAM_AWB_L4_Y AWB Light4 y Region 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L4_Y_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L4_Y_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L4_Y_UP	AWB Light4 Ry up
13:0	AWB_L4_Y_LOW	AWB Light4 Ry low

15004614 CAM_AWB_L5_X AWB Light5 x Region 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L5_X_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L5_X_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L5_X_UP	AWB Light5 Rx up

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Bit(s)	Name	Description
13:0	AWB_L5_X_LOW	AWB Light5 Rx low

15004618 **CAM_AWB_L5_Y** **AWB Light5 y Region** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L5_Y_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L5_Y_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L5_Y_UP	AWB Light5 Ry up
13:0	AWB_L5_Y_LOW	AWB Light5 Ry low

1500461C **CAM_AWB_L6_X** **AWB Light6 x Region** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L6_X_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L6_X_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L6_X_UP	AWB Light6 Rx up
13:0	AWB_L6_X_LOW	AWB Light6 Rx low

15004620 **CAM_AWB_L6_Y** **AWB Light6 y Region** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L6_Y_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L6_Y_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L6_Y_UP	AWB Light6 Ry up
13:0	AWB_L6_Y_LOW	AWB Light6 Ry low

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15004624 **CAM_AWB_L7_X** **AWB Light7 x Region** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L7_X_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L7_X_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L7_X_UP	AWB Light7 Rx up
13:0	AWB_L7_X_LOW	AWB Light7 Rx low

15004628 **CAM_AWB_L7_Y** **AWB Light7 y Region** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L7_Y_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L7_Y_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L7_Y_UP	AWB Light7 Ry up
13:0	AWB_L7_Y_LOW	AWB Light7 Ry low

1500462C **CAM_AWB_L8_X** **AWB Light8 x Region** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L8_X_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L8_X_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L8_X_UP	AWB Light8 Rx up
13:0	AWB_L8_X_LOW	AWB Light8 Rx low

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15004630 **CAM_AWB_L8_Y** **AWB Light8 y Region** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L8_Y_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L8_Y_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L8_Y_UP	AWB Light8 Ry up
13:0	AWB_L8_Y_LOW	AWB Light8 Ry low

15004634 **CAM_AWB_L9_X** **AWB Light9 x Region** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L9_X_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L9_X_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L9_X_UP	AWB Light9 Rx up
13:0	AWB_L9_X_LOW	AWB Light9 Rx low

15004638 **CAM_AWB_L9_Y** **AWB Light9 y Region** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L9_Y_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L9_Y_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L9_Y_UP	AWB Light9 Ry up
13:0	AWB_L9_Y_LOW	AWB Light9 Ry low

1500463C **CAM_AWB_SPARE** **AWB Spare Register** **00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AWB_SPARE[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AWB_SPARE[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AWB_SPARE	AWB spare register

15004650 CAM_AE_HST_CTL AE Histogram Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													AE_HST3_EN	AE_HST2_EN	AE_HST1_EN	AE_HST0_EN
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	AE_HST3_EN	Enables AE hsitogram 3
2	AE_HST2_EN	Enables AE hsitogram 2
1	AE_HST1_EN	Enables AE hsitogram 1
0	AE_HST0_EN	Enables AE hsitogram 0

15004654 CAM_AE_GAIN2_0 AE Raw PreGain2 R/G 02000200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					AE_GAIN2_G											
Type					RW											
Reset					0	0	1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AE_GAIN2_R											
Type					RW											
Reset					0	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	AE_GAIN2_G	Statistic RawPreGain2 G
11:0	AE_GAIN2_R	Statistic RawPreGain2 R

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15004658 **CAM_AE_GAIN2_1** **AE Raw PreGain2 B** 00000200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					AE_GAIN2_B											
Type					RW											
Reset					0	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	AE_GAIN2_B	Statistic RawPreGain2 B

1500465C **CAM_AE_LMT2_0** **AE Raw Limit2 R/G** 0FFF0FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					AE_LMT2_G											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					AE_LMT2_R											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27:16	AE_LMT2_G	Statistic RawLimit2 G
11:0	AE_LMT2_R	Statistic RawLimit2 R

15004660 **CAM_AE_LMT2_1** **AE Raw Limit2 B** 00000FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					AE_LMT2_B											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
11:0	AE_LMT2_B	Statistic RawLimit2 B

15004664 **CAM_AE_RC_CNV_0** **AE Matrix Coeff 0** 00000200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name						AE_RC_CNV01										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						AE_RC_CNV00										
Type						RW										
Reset						0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:16	AE_RC_CNV01	Color conv matrix coef 01
10:0	AE_RC_CNV00	Color conv matrix coef 00

15004668 CAM_AE_RC_CNV_1 AE Matrix Coeff 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						AE_RC_CNV10										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						AE_RC_CNV02										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:16	AE_RC_CNV10	Color conv matrix coef 10
10:0	AE_RC_CNV02	Color conv matrix coef 02

1500466C CAM_AE_RC_CNV_2 AE Matrix Coeff 2 00000200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						AE_RC_CNV12										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						AE_RC_CNV11										
Type						RW										
Reset						0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:16	AE_RC_CNV12	Color conv matrix coef 12
10:0	AE_RC_CNV11	Color conv matrix coef 10

15004670 CAM_AE_RC_CNV_3 AE Matrix Coeff 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						AE_RC_CNV21										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						AE_RC_CNV20										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:16	AE_RC_CNV21	Color conv matrix coef 21
10:0	AE_RC_CNV20	Color conv matrix coef 20

15004674 CAM_AE_RC_CNV_4 AE Matrix Coeff 4 00090200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													AE_RC_ACC			
Type													RW			
Reset													1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						AE_RC_CNV22										
Type						RW										
Reset						0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:16	AE_RC_ACC	**Color conv matrix shift bits** Range: 6~9
10:0	AE_RC_CNV22	**Color conv matrix coef 22**

15004678 CAM_AE_YGAMMA_0 AE YGAMMA Set 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Y_GMR4								Y_GMR3							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Y_GMR2								Y_GMR1							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Y_GMR4	Spare
23:16	Y_GMR3	Spare
15:8	Y_GMR2	Spare
7:0	Y_GMR1	Spare

1500467C CAM_AE_YGAMMA_1 AE YGAMMA Set 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

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Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**Y_GMR5**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	Y_GMR5	Spare

15004680 **CAM_AE_HST_SET** **AE Histogram Setting** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**AE_COLOR_MODE_3**				**AE_COLOR_MODE_2**				**AE_COLOR_MODE_1**				**AE_COLOR_MODE_0**		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**AE_BIN_MODE_3**				**AE_BIN_MODE_2**				**AE_BIN_MODE_1**				**AE_BIN_MODE_0**	
Type			RW				RW				RW				RW	
Reset			0	0			0	0			0	0			0	0

Bit(s)	Name	Description
30:28	AE_COLOR_MODE_3	**AE histogram 3 source** 0: R 1: G 2: B 3: Reserved 4: AE_SUM
26:24	AE_COLOR_MODE_2	**AE histogram 2 source** 0: R 1: G 2: B 3: Reserved 4: AE_SUM
22:20	AE_COLOR_MODE_1	**AE histogram 1 source** 0: R 1: G 2: B 3: RGB mixed 4: AE_SUM
18:16	AE_COLOR_MODE_0	**AE histogram 0 source** 0/1/2/4: Reserved 3: Flare
13:12	AE_BIN_MODE_3	**AE hsitogram 3 bin mode** 0~1: 128 bin, 2: 256 bin low, 3: 256 bin high
9:8	AE_BIN_MODE_2	**AE hsitogram 2 bin mode** 0~1: 128 bin, 2: 256 bin low, 3: 256 bin high
5:4	AE_BIN_MODE_1	**AE hsitogram 1 bin mode** 0~1: 128 bin, 2: 256 bin low,

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Bit(s)	Name	Description
		3: 256 bin high
1:0	AE_BIN_MODE_0	**AE hsitogram 0 bin mode** 0~1: 128 bin, 2: 256 bin low, 3: 256 bin high

15004684 **CAM_AE_HST0_RNG** **AE Histogram 0 Range** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		AE_Y_HI_0								AE_Y_LOW_0						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		AE_X_HI_0								AE_X_LOW_0						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	AE_Y_HI_0	**Range of interest** Defined by window location 0 ~ 127 Histogram0, y high
22:16	AE_Y_LOW_0	**Range of interest** Defined by window location 0 ~ 127 Histogram0, ylow
14:8	AE_X_HI_0	**Range of interest** Defined by window location 0 ~ 127 Histogram0, xhigh
6:0	AE_X_LOW_0	**Range of interest** Defined by window location 0 ~ 127 Histogram 0, xlow

15004688 **CAM_AE_HST1_RNG** **AE Histogram 1 Range** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		AE_Y_HI_1								AE_Y_LOW_1						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		AE_X_HI_1								AE_X_LOW_1						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	AE_Y_HI_1	**Range of interest** Defined by window location 0 ~ 127 Histogram 1, y high
22:16	AE_Y_LOW_1	**Range of interest** Defined by window location 0 ~ 127 Histogram 1, ylow

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Bit(s)	Name	Description
14:8	AE_X_HI_1	**Range of interest** Defined by window location 0 ~ 127 Histogram 1, xhigh
6:0	AE_X_LOW_1	**Range of interest** Defined by window location 0 ~ 127 Histogram 1, xlow

1500468C CAM_AE_HST2_RNG AE Histogram 2 Range 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		AE_Y_HI_2								AE_Y_LOW_2						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		AE_X_HI_2								AE_X_LOW_2						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	AE_Y_HI_2	**Range of interest** Defined by window location 0 ~ 127 Histogram 2, y high
22:16	AE_Y_LOW_2	**Range of interest** Defined by window location 0 ~ 127 Histogram 2, ylow
14:8	AE_X_HI_2	**Range of interest** Defined by window location 0 ~ 127 Histogram 2, xhigh
6:0	AE_X_LOW_2	**Range of interest** Defined by window location 0 ~ 127 Histogram 2, xlow

15004690 CAM_AE_HST3_RNG AE Histogram 3 Range 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		AE_Y_HI_3								AE_Y_LOW_3						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		AE_X_HI_3								AE_X_LOW_3						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	AE_Y_HI_3	**Range of interest** Defined by window location 0 ~ 127 Histogram 3, y high
22:16	AE_Y_LOW_3	**Range of interest** Defined by window location 0 ~ 127

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Bit(s)	Name	Description
		Histogram 3, ylow
14:8	AE_X_HI_3	**Range of interest** Defined by window location 0 ~ 127 Histogram 3, xhigh
6:0	AE_X_LOW_3	**Range of interest** Defined by window location 0 ~ 127 Histogram 3, xlow

15004694 **CAM_AE_SPARE** **AE Spare Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AE_SPARE[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AE_SPARE[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AE_SPARE	AE spare register

150046A0 **CAM_SGG1_PGN** **SGG PGN** **00000010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						SGG1_GAIN										
Type						RW										
Reset						0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
10:0	SGG1_GAIN	**Double buffer** SGG pre-gain for low contrast scene (Q0.7.4)

150046A4 **CAM_SGG1_GMRC_1** **SGG GMRC 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SGG1_GMR_4								SGG1_GMR_3							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SGG1_GMR_2								SGG1_GMR_1							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:24	SGG1_GMR_4	**Double buffer** SGG gamma control point 4 (256)
23:16	SGG1_GMR_3	**Double buffer** SGG gamma control point 3 (128)
15:8	SGG1_GMR_2	**Double buffer** SGG gamma control point 2 (64)
7:0	SGG1_GMR_1	**Double buffer** SGG gamma control point 1 (32)

150046A8 **CAM_SGG1_GMRC_2** **SGG GMRC 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									SGG1_GMR_7							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SGG1_GMR_6								SGG1_GMR_5							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	SGG1_GMR_7	**Double buffer** SGG gamma control point 7 (2048)
15:8	SGG1_GMR_6	**Double buffer** SGG gamma control point 6 (1024)
7:0	SGG1_GMR_5	**Double buffer** SGG gamma control point 5 (512)

150046B0 **CAM_AF_CON** **AF Control** **0000000C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESERVED															
Type	RW															
Reset	0	0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						AF_TARY				AF_TARX			AF_ODD	AF_ZZ	AF_DECI	
Type						USER0				USER0			USER0	USER0	USER0	
Reset						0	0	0		0	0	0	1	1	0	0

Bit(s)	Name	Description
10:8	AF_TARY	**Double buffer** Y coordinate of target AF window (0 ~ 5)
6:4	AF_TARX	**Double buffer** X coordinate of target AF window (0 ~ 5)
3	AF_ODD	**Double buffer** Controls even or odd line to do 1 pixel shift when decimation is enabled

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Bit(s)	Name	Description
		0: Even line 1: Odd line
2	AF_ZZ	**Double buffer** Always set it to 1. Controls 1 pixel shift when decimation is enabled 0: No shift 1: 1 pixel shift
1:0	AF_DECI	**Double buffer** Enables decimation function to decimate input data for horizontal filters 0: No decimation 1: 1/2 decimation 2: 1/4 decimation

150046B4 **CAM_AF_WINX_1** **AF Window X 0&1** **1FFF1FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AF_WINX_1												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AF_WINX_0												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
28:16	AF_WINX_1	**Double buffer** AF window start point x1 Set to maximum value 8191 whenever this column of AF window is not enabled.
12:0	AF_WINX_0	**Double buffer** AF window start point x0 Set to maximum value 8191 whenever this column of AF window is not enabled.

150046B8 **CAM_AF_WINX_2** **AF Window X 2&3** **1FFF1FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AF_WINX_3												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AF_WINX_2												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
28:16	AF_WINX_3	**Double buffer** AF window start point x3 Set to maximum value 8191 whenever this column of AF window is not enabled.

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Bit(s)	Name	Description
12:0	AF_WINX_2	**Double buffer** AF window start point x2 Set to maximum value 8191 whenever this column of AF window is not enabled.

150046BC **CAM_AF_WINX_3** **AF Window X 4&5** **1FFF1FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AF_WINX_5												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AF_WINX_4												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
28:16	AF_WINX_5	**Double buffer** AF window start point x5 Set to maximum value 8191 whenever this column of AF window is not enabled.
12:0	AF_WINX_4	**Double buffer** AF window start point x4 Set to maximum value 8191 whenever this column of AF window is not enabled.

150046C0 **CAM_AF_WINY_1** **AF Window Y 0&1** **1FFF1FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AF_WINY_1												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AF_WINY_0												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
28:16	AF_WINY_1	**Double buffer** AF window start point y1 Set to maximum value 8191 whenever this row of AF window is not enabled.
12:0	AF_WINY_0	**Double buffer** AF window start point y0 Set to maximum value 8191 whenever this row of AF window is not enabled.

150046C4 **CAM_AF_WINY_2** **AF Window Y 2&3** **1FFF1FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name				AF_WINY_3												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AF_WINY_2												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
28:16	AF_WINY_3	**Double buffer** AF window start point y3 Set to maximum value 8191 whenever this row of AF window is not enabled.
12:0	AF_WINY_2	**Double buffer** AF window start point y2 Set to maximum value 8191 whenever this row of AF window is not enabled.

150046C8 CAM_AF_WINY_3 AF Window Y 4&5 1FFF1FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AF_WINY_5												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AF_WINY_4												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
28:16	AF_WINY_5	**Double buffer** AF window start point y5 Set to maximum value 8191 whenever this row of AF window is not enabled.
12:0	AF_WINY_4	**Double buffer** AF window start point y4 Set to maximum value 8191 whenever this row of AF window is not enabled.

150046CC CAM_AF_SIZE AF Window SIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							AF_WIN_HT									
Type							USER0									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							AF_WIN_WD									
Type							USER0									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	AF_WIN_HT	**Double buffer** AF window height y
9:0	AF_WIN_WD	**Double buffer** AF window width x

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150046D4 CAM_AF_FLT_1 AF Filter P1~P4 12111023

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AF_FLT_P_4								AF_FLT_P_3							
Type	RW								RW							
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AF_FLT_P_2								AF_FLT_P_1							
Type	RW								RW							
Reset	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	1

Bit(s)	Name	Description
31:24	AF_FLT_P_4	AF horizontal filter parameter P4
23:16	AF_FLT_P_3	AF horizontal filter parameter P3
15:8	AF_FLT_P_2	AF horizontal filter parameter P2
7:0	AF_FLT_P_1	AF horizontal filter parameter P1

150046D8 CAM_AF_FLT_2 AF Filter P5~P8 11121313

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AF_FLT_P_8								AF_FLT_P_7							
Type	RW								RW							
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AF_FLT_P_6								AF_FLT_P_5							
Type	RW								RW							
Reset	0	0	0	1	0	0	1	1	0	0	0	1	0	0	1	1

Bit(s)	Name	Description
31:24	AF_FLT_P_8	AF horizontal filter parameter P8
23:16	AF_FLT_P_7	AF horizontal filter parameter P7
15:8	AF_FLT_P_6	AF horizontal filter parameter P6
7:0	AF_FLT_P_5	AF horizontal filter parameter P5

150046DC CAM_AF_FLT_3 AF Filter P9~P12 02040709

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AF_FLT_P_12								AF_FLT_P_11							
Type	RW								RW							
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AF_FLT_P_10								AF_FLT_P_9							
Type	RW								RW							
Reset	0	0	0	0	0	1	1	1	0	0	0	0	1	0	0	1

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:24	AF_FLT_P_12	AF horizontal filter parameter P12
23:16	AF_FLT_P_11	AF horizontal filter parameter P11
15:8	AF_FLT_P_10	AF horizontal filter parameter P10
7:0	AF_FLT_P_9	AF horizontal filter parameter P9

150046E0 CAM_AF_TH AF Filter Threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								**AF_TH_MODE**	**AF_TH_1**							
Type								RW	RW							
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**AF_TH_0**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24	AF_TH_MODE	**Double buffer** AF threshold method 0: Hard threshold 1: Soft threshold
23:16	AF_TH_1	**Double buffer** AF vertical filter threshold
7:0	AF_TH_0	**Double buffer** AF horizontal filter threshold

150046E4 CAM_AF_FLO_WIN_1 AF Floating Window 1 X&Y 1FFF1FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**AF_FLO_WINY_1**												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**AF_FLO_WINX_1**												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
28:16	AF_FLO_WINY_1	**Double buffer** AF floating window start point y Set to maximum value 8191 whenever this floating AF window is not enabled.
12:0	AF_FLO_WINX_1	**Double buffer** AF floating window start point x Set to maximum value 8191 whenever this floating AF window is not enabled.

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150046E8 CAM_AF_FLO_SIZE_1 AF Floating Window 1 Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					AF_FLO_HT_1											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AF_FLO_WD_1											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	AF_FLO_HT_1	**Double buffer** AF floating window height y
11:0	AF_FLO_WD_1	**Double buffer** AF floating window width x

150046EC CAM_AF_FLO_WIN_2 AF Floating Window 2 X&Y 1FFF1FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AF_FLO_WINY_2												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AF_FLO_WINX_2												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
28:16	AF_FLO_WINY_2	**Double buffer** AF floating window 2 start point y Set to maximum value 8191 whenever this floating AF window is not enabled.
12:0	AF_FLO_WINX_2	**Double buffer** AF floating window 2 start point x Set to maximum value 8191 whenever this floating AF window is not enabled.

150046F0 CAM_AF_FLO_SIZE_2 AF Floating Window 2 Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					AF_FLO_HT_2											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AF_FLO_WD_2											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	AF_FLO_HT_2	**Double buffer** AF floating window 2 height y

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Bit(s)	Name	Description
11:0	AF_FLO_WD_2	**Double buffer** AF floating window 2 width x

150046F4 CAM_AF_FLO_WIN_3 AF Floating Window 3 X&Y 1FFF1FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AF_FLO_WINY_3												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AF_FLO_WINX_3												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
28:16	AF_FLO_WINY_3	**Double buffer** AF floating window 3 start point y Set to maximum value 8191 whenever this floating AF window is not enabled
12:0	AF_FLO_WINX_3	**Double buffer** AF floating window 3 start point x Set to maximum value 8191 whenever this floating AF window is not enabled

150046F8 CAM_AF_FLO_SIZE_3 AF Floating Window 3 Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					AF_FLO_HT_3											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AF_FLO_WD_3											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	AF_FLO_HT_3	**Double buffer** AF floating window 3 height y
11:0	AF_FLO_WD_3	**Double buffer** AF floating window 3 width x

150046FC CAM_AF_FLO_TH AF Floating Window Filter Threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AF_FLO_TH_1							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AF_FLO_TH_0							

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Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	AF_FLO_TH_1	**Double buffer** AF floating window vertical filter threshold
7:0	AF_FLO_TH_0	**Double buffer** AF floating window horizontal filter threshold

15004700 CAM_AF_IMAGE_SIZE AF Input Image Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AF_IMAGE_WD												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	AF_IMAGE_WD	AF input image width

15004704 CAM_AF_FLT_4 AF Vertical Filter X0~X1 01000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						AF_FLT_X_1										
Type						RW										
Reset						0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						AF_FLT_X_0										
Type						RW										
Reset						0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:16	AF_FLT_X_1	AF vertical filter parameter X1, Q1.2.8
10:0	AF_FLT_X_0	AF vertical filter parameter X0, Q1.2.8

15004708 CAM_AF_FLT_5 AF Vertical Filter X2~X3 07000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						AF_FLT_X_3										
Type						RW										
Reset						1	1	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						AF_FLT_X_2										
Type						RW										
Reset						1	1	1	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
26:16	AF_FLT_X_3	AF vertical filter parameter X3, Q1.2.8
10:0	AF_FLT_X_2	AF vertical filter parameter X2, Q1.2.8

1500470C **CAM_AF_STAT_L** **AF Target Window Statistics Output (LSB)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AF_STAT_LSB[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AF_STAT_LSB[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AF_STAT_LSB	AF target window statistics output (LSB)

15004710 **CAM_AF_STAT_M** **AF Target Window Statistics Output (MSB)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AF_STAT_MSB[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AF_STAT_MSB[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AF_STAT_MSB	AF target window statistics output (MSB)

15004714 **CAM_AF_FLO_STAT_1L** **AF Floating Window 1 Statistics Output (LSB)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AF_STAT_LSB[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AF_STAT_LSB[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AF_STAT_LSB	AF floating window 1 statistics output (LSB)

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15004718	CAM_AF_FLO_STAT_1M	AF Floating Window 1 Statistics Output (MSB)	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AF_STAT_MSB[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AF_STAT_MSB[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AF_STAT_MSB	AF floating window 1 statistics output (MSB)

1500471C	CAM_AF_FLO_STAT_1V	AF Floating Window 1 Statistics Output (VER)	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AF_STAT_VER[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AF_STAT_VER[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AF_STAT_VER	AF floating window 1 statistics output (VER)

15004720	CAM_AF_FLO_STAT_2L	AF Floating Window 2 Statistics Output (LSB)	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AF_STAT_LSB[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AF_STAT_LSB[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AF_STAT_LSB	AF floating window 2 statistics output (LSB)

15004724	CAM_AF_FLO_STAT_2M	AF Floating Window 2 Statistics Output (MSB)	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AF_STAT_MSB[31:16]															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AF_STAT_MSB[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AF_STAT_MSB	AF floating window 2 statistics output (MSB)

15004728 CAM_AF_FLO_STAT_2V AF Floating Window 2 Statistics Output (VER) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AF_STAT_VER[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AF_STAT_VER[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AF_STAT_VER	AF floating window 2 statistics output (VER)

1500472C CAM_AF_FLO_STAT_3L AF Floating Window 3 Statistics Output (LSB) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AF_STAT_LSB[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AF_STAT_LSB[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AF_STAT_LSB	AF floating window 3 statistics output (LSB)

15004730 CAM_AF_FLO_STAT_3M AF Floating Window 3 Statistics Output (MSB) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AF_STAT_MSB[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AF_STAT_MSB[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	AF_STAT_MSB	AF floating window 3 statistics output (MSB)

15004734 **CAM_AF_FLO_STAT_3V** **AF Floating Window 3 Statistics Output (VER)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AF_STAT_VER[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AF_STAT_VER[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AF_STAT_VER	AF floating window 3 statistics output (VER)

15004760 **CAM_WBN_SIZE** **WBN_SIZE** **0F3C14B4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				WBN_IN_V												
Type				RW												
Reset				0	1	1	1	1	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WBN_IN_H												
Type				RW												
Reset				1	0	1	0	0	1	0	1	1	0	1	0	0

Bit(s)	Name	Description
28:16	WBN_IN_V	**Binning module input vertical resolution** Max. value: 3,900
12:0	WBN_IN_H	**Binning module input vertical resolution** Max. value: 5,300

15004764 **CAM_WBN_MODE** **WBN_MODE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								WBN_RGBC_DIR			WBN_RGBC_ID			WBN_ACC		
Type								RW			RW			RW		
Reset								0			0	0		0	0	0

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Bit(s)	Name	Description
8	WBN_RGBC_DIR	0: Slash 1: Backslash
5:4	WBN_RGBC_ID	**RGBC offset**
2:0	WBN_ACC	**Binning mode** 0: (1 1) filter, gain=2 1: (1 1) filter, gain=1 2: (3 1)+(1 3) filter, gain = 4 3: (1 2 1)+(1 3 3 1) filter, gain = 4 and 8 4: W average 5: W accumulation

15004770 **CAM_FLK_CON** **FLK Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																Reserved
Type																RW
Reset																0

Bit(s)	Name	Description

15004774 **CAM_FLK_OFST** **FLK Start Offset** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					FLK_OFST_Y											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					FLK_OFST_X											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	FLK_OFST_Y	FLK start offset y
11:0	FLK_OFST_X	FLK start offset x

15004778 **CAM_FLK_SIZE** **FLK Window Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					FLK_SIZE_Y											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					FLK_SIZE_X											

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Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	FLK_SIZE_Y	FLK window size y
11:0	FLK_SIZE_X	FLK window size x

1500477C CAM_FLK_NUM FLK Window Number 00000066

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**FLK_NUM_Y**				**FLK_NUM_X**		
Type										RW				RW		
Reset										1	1	0		1	1	0

Bit(s)	Name	Description
6:4	FLK_NUM_Y	FLK window number y
2:0	FLK_NUM_X	FLK window number x

15004780 CAM_LCS_CON LCS Control Register 30400001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**LCS_OUT_HT**								**LCS_OUT_WD**						
Type		RW								RW						
Reset		0	1	1	0	0	0	0		1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**LCS_LG2**
Type																RW
Reset																1

Bit(s)	Name	Description
30:24	LCS_OUT_HT	**Output height of small light map** Max. value = 72
22:16	LCS_OUT_WD	**Output width of small light map** Max. value = 96
0	LCS_LG2	**Controls whether the input of LRZ is log2(G) or G**

15004784 CAM_LCS_ST LCS Start Point 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**LCS_START_I**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				LCS_START_J												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	LCS_START_I	**Vertical start point of active window** Must be even.
12:0	LCS_START_J	**Horizontal start point of active window** Must be even.

15004788 CAM_LCS_A WS LCS Active Window Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LCS_IN_HT												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				LCS_IN_WD												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	LCS_IN_HT	**Must be even** LCS_IN_HT ? LCS_OUT_HT
12:0	LCS_IN_WD	**Must be even** LCS_IN_WD ? 2*LCS_OUT_WD

1500478C CAM_LCS_F LR LCS Flare 00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LCS_FLR_GAIN									LCS_FLR_OFST						
Type	RW									RW						
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:7	LCS_FLR_GAIN	**Q0.1.8** The flare gain
6:0	LCS_FLR_OFST	**Q0.7.0** The flare offset: LCS_FLR_OFST = flare_offset / 4

15004790 CAM_LCS_L RZR_1 LCS Horizontal Down-sampling Ratio 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													LCS_LRZR_X[19:16]			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LCS_LRZR_X[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	LCS_LRZR_X	Down scale horizontal ratio

15004794 CAM_LCS_LRZR_2 LCS Vertical Down-sampling Ratio 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													LCS_LRZR_Y[19:16]			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LCS_LRZR_Y[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	LCS_LRZR_Y	Down scale vertical ratio

150047A0 CAM_RRZ_CTL RRZ CTL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							RRZ_VERT_TBL_SEL					RRZ_HORI_TBL_SEL				
Type							USER0					USER0				
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RRZ_VERT_EN	RRZ_HORI_EN
Type															USER0	USER0
Reset															0	0

Bit(s)	Name	Description
25:21	RRZ_VERT_TBL_SEL	**Double buffer** Selects vertical scaling coefficient table 4 tap: [20:25] (1x up ~ 1/2x down) Cubic accumulation: [0:19] (blur ~ sharp)
20:16	RRZ_HORI_TBL_SEL	**Double buffer** Selects horizontal scaling coefficient table 4 tap: [20:25] (1x up ~ 1/2x down) Cubic accumulation: [0:19] (blur ~ sharp)
1	RRZ_VERT_EN	**Double buffer** Enables vertical scaling function

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Bit(s)	Name	Description
0	RRZ_HORI_EN	**Double buffer** Enables horizontal scaling function

150047A4 **CAM_RRZ_IN_IMG** **RRZ IN IMG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RRZ_IN_HT												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RRZ_IN_WD												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	RRZ_IN_HT	**Double buffer** Imput Image height
12:0	RRZ_IN_WD	**Double buffer** Input Image width

150047A8 **CAM_RRZ_OUT_IMG** **RRZ OUT IMG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RRZ_OUT_HT												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RRZ_OUT_WD												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	RRZ_OUT_HT	**Double buffer** Output Image height
12:0	RRZ_OUT_WD	**Double buffer** Output Image width

150047AC **CAM_RRZ_HORI_STEP** **RRZ_HORI_STEP** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RRZ_HORI_STEP[16:16]
Type																USER0

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Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RRZ_HORI_STEP[15:0]**															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	RRZ_HORI_STEP	**Double buffer** Horiznotal scaling ratio

150047B0 CAM_RRZ_VERT_STEP RRZ_VERT_STEP 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**RRZ_VERT_STEP[16:16]**
Type																USER0
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RRZ_VERT_STEP[15:0]**															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	RRZ_VERT_STEP	**Double buffer** Vertical scaling ratio

150047B4 CAM_RRZ_HORI_INT_OFST RRZ_HORI_INT_OFST 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**RRZ_HORI_INT_OFST**												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	RRZ_HORI_INT_OFST	**Double buffer** Horizontal integer offset

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150047B8 **CAM_RRZ_HORI_SUB_OFST** **RRZ_HORI_SUB_OFST** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RRZ_HORI_SUB_OFST														
Type		USERO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:0	RRZ_HORI_SUB_OFST	**Double buffer** Horizontal sub-pixel offset

150047BC **CAM_RRZ_VERT_INT_OFST** **RRZ_VERT_INT_OFST** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RRZ_VERT_INT_OFST												
Type				USERO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	RRZ_VERT_INT_OFST	**Double buffer** Vertical Integer offset

150047C0 **CAM_RRZ_VERT_SUB_OFST** **RRZ_VERT_SUB_OFST** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RRZ_VERT_SUB_OFST														
Type		USERO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:0	RRZ_VERT_SUB_OFST	**Double buffer** Vertical Sub-pixel offset

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150047C4	CAM_RRZ_MODE_TH	RRZ_TH_MD	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RRZ_TH_MD2								RRZ_TH_LO							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RRZ_TH_HI								RRZ_TH_MD							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	RRZ_TH_MD2	**0~255** Threshold for detecting Nyquist region
23:16	RRZ_TH_LO	**0~255** Threshold for detecting flat region
15:8	RRZ_TH_HI	**0~255** Threshold for detecting Nyquist region
7:0	RRZ_TH_MD	**0~255** Threshold for detecting edge region

150047C8	CAM_RRZ_MODE_CTL	RRZ_TBL_SEL_SP	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RRZ_CR_MODE
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RRZ_BLD_SL					RRZ_PRF		RRZ_PRF_BLD								
Type	RW					RW		RW								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RRZ_CR_MODE	0/1 for 1-line/3-line chroma calculation kernel
15:11	RRZ_BLD_SL	Slope for directional blending
10:9	RRZ_PRF	Switch b/w high/low-pass G
8:0	RRZ_PRF_BLD	Blending ratio of low/high-pass output

15004800	CAM_BPC_CON	2D BPC Control Register	00008020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															BPC_CRC_MODE	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPC_CS_		BPC_DTC								BPC	BPC				BPC

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	MODE		_MODE								_TABLE_END_MODE	_LUT_EN				_EN
Type	RW		RW								RW	RW				RW
Reset	1	0	0	0							1	0				0

Bit(s)	Name	Description
17:16	BPC_CRC_MODE	**Double buffer** Anisotropic interpolation, ranking filter or both Valid value: 0 ~ 2 0: Automatic detect 1: Anisotropic filter only 2: Ranking filter only
15:14	BPC_CS_MODE	**Double buffer** Enables cluster handling solution mode for BPC cluster correction 0: Support up to size 2 1: Support up to size 4 (aggressive) 2: Support up to size 4 (conservative)
13:12	BPC_DTC_MODE	**Double buffer** OTF, table lookup or both. Should be '0' if BPC table is off. 0: Use OTF only to locate bad pixels; any one of 3 cases is held. Case A: Table lookup only (if table exists) Case B: OTF detected and strong bad pixel (BP_level>STRONG_BP_THR_LA) Case C: Very strong bad pixel (BP_level>STRONG_BP_THR_LB) 1: Bad pixels detected by OTF also locate in the table. 2: Use table only to locate bad pixels (This mode can handle >=3 clusters.)
5	BPC_TABLE_END_MODE	**Double buffer** Wait table input path finished (FKBPI eot) or not. 0: Does not wait for table finished. FKBPI is forced to be restarted by SOF. This mode can only be used when FKBPI configurations are not changed. 1: Wait table finished
4	BPC_LUT_EN	**Double buffer** Enables table lookup If 1, BPC_DTC_MODE = 0.
0	BPC_EN	**Double buffer** Enables 2D BPC correction

15004804 CAM_BPC_TH1 BPC Detection Condition 1 Register 1 000C606E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BPC_TH_Y[11:4]							
Type									RW							
Reset									0	0	0	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPC_TH_Y[3:0]				BPC_TH_LWB											
Type	RW				RW											
Reset	0	1	1	0	0	0	0	0	0	1	1	0	1	1	1	0

Bit(s)	Name	Description
23:12	BPC_TH_Y	Offset of the threshold curve section 3
11:0	BPC_TH_LWB	Threshold offset for dark region

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15004808 CAM_BPC_TH2 BPC Detection Condition 1 Register 2 00000258

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					**BPC_TH_UPB**											
Type					RW											
Reset					0	0	1	0	0	1	0	1	1	0	0	0

Bit(s)	Name	Description
11:0	BPC_TH_UPB	Upper bound of threshold curve

1500480C CAM_BPC_TH3 BPC Detection Condition 1 Register 3 B1200100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**BPC_TH_SLB**				**BPC_TH_SLA**				**BPC_TH_XB[11:4]**							
Type	RW				RW				RW							
Reset	1	0	1	1	0	0	0	1	0	0	1	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	**BPC_TH_XB[3:0]**				**BPC_TH_XA**											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	BPC_TH_SLB	Slope of threshold curve section 3
27:24	BPC_TH_SLA	Slope of the threshold curve section 2
23:12	BPC_TH_XB	Starting point of threshold curve section 3
11:0	BPC_TH_XA	Starting point of threshold curve section 2

15004810 CAM_BPC_TH4 BPC Detection Condition 1 Register 3 BB2C616E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**BPC_DK_TH_SLB**				**BPC_DK_TH_SLA**				**BPC_DK_TH_XB[11:4]**							
Type	RW				RW				RW							
Reset	1	0	1	1	1	0	1	1	0	0	1	0	1	1	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	**BPC_DK_TH_XB[3:0]**				**BPC_DK_TH_XA**											
Type	RW				RW											
Reset	0	1	1	0	0	0	0	1	0	1	1	0	1	1	1	0

Bit(s)	Name	Description
31:28	BPC_DK_TH_SLB	Slope of threshold_DK curve section 3
27:24	BPC_DK_TH_SLA	Slope of threshold_DK curve section 2
23:12	BPC_DK_TH_XB	Starting point of threshold_DK curve section 3
11:0	BPC_DK_TH_XA	Starting point of threshold_DK curve section 2

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15004814 CAM_BPC_DTC BPC Detection Condition 1/2/3 Register 00030031

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						BPC_NO_LV							BPC_TH_MUL			
Type						RW							RW			
Reset						0	0	0					0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					BPC_CT_LV					BPC_CS_RNG			BPC_RNG			
Type					RW					RW			RW			
Reset					0	0	0	0		0	1	1	0	0	0	1

Bit(s)	Name	Description
26:24	BPC_NO_LV	**Noise level of image** For tuning the false-positive ratio and false-negative ratio
19:16	BPC_TH_MUL	
11:8	BPC_CT_LV	**Crosstalk level of image**
6:4	BPC_CS_RNG	**Allowable number of neighboring pixels for cluster solution** Valid range: 0 ~ 7
3:0	BPC_RNG	**Allowable number of neighboring pixels falling in condition 1 threshold range** Valid range: 0 ~ 7

15004818 CAM_BPC_COR BPC Correction Register 05010519

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BPC_DIR_TH2													BPC_RANK_IDX		
Type	RW													RW		
Reset	0	0	0	0	0	1	0	1						0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPC_DIR_TH								BPC_DIR_MAX							
Type	RW								RW							
Reset	0	0	0	0	0	1	0	1	0	0	0	1	1	0	0	1

Bit(s)	Name	Description
31:24	BPC_DIR_TH2	
18:16	BPC_RANK_IDX	
15:8	BPC_DIR_TH	When the difference of anisotropic interpolation pixels is large than this threshold, ranking filter will be used to correct bad pixel.
7:0	BPC_DIR_MAX	Clamps the difference of anisotropic interpolation pixels to this value

1500481C CAM_BPC_TBLI1 BPC Table Input Information Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				BPC_YOFFSET												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name				BPC_XOFFSET												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	BPC_YOFFSET	**Double buffer** Number of first line to input the TPIPE from the beginning of a frame
12:0	BPC_XOFFSET	**Double buffer** Number of first pixel to input the TPIPE from the beginning of a line

15004820 CAM_BPC_TBLI2 BPC Table Input Information Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				BPC_YSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				BPC_XSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	BPC_YSIZE	**Double buffer** Number (minus 1) of lines to input in TPIPE
12:0	BPC_XSIZE	**Double buffer** Number (minus 1) of pixels per line to input in TPIPE

15004824 CAM_BPC_TH1_C BPC Detection Extension Condition 1 Register 1 000C606E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BPC_C_TH_Y[11:4]							
Type									RW							
Reset									0	0	0	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPC_C_TH_Y[3:0]				BPC_C_TH_LWB											
Type	RW				RW											
Reset	0	1	1	0	0	0	0	0	0	1	1	0	1	1	1	0

Bit(s)	Name	Description
23:12	BPC_C_TH_Y	Offset of threshold curve section 3
11:0	BPC_C_TH_LWB	Threshold offset for dark region

15004828 CAM_BPC_TH2_C BPC Detection Extension Condition 1 Register 2 00000258

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**BPC_C_TH_UPB**											
Type					RW											
Reset					0	0	1	0	0	1	0	1	1	0	0	0

Bit(s)	Name	Description
11:0	BPC_C_TH_UPB	Upper bound of threshold curve

1500482C CAM_BPC_TH3_C BPC Detection Extension Condition 1 Register 3 B1200100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**BPC_C_TH_SLB**				**BPC_C_TH_SLA**				**BPC_C_TH_XB[11:4]**							
Type	RW				RW				RW							
Reset	1	0	1	1	0	0	0	1	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BPC_C_TH_XB[3:0]**				**BPC_C_TH_XA**											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	BPC_C_TH_SLB	Slope of threshold curve section 3
27:24	BPC_C_TH_SLA	Slope of threshold curve section 2
23:12	BPC_C_TH_XB	Starting point of threshold curve section 3
11:0	BPC_C_TH_XA	Starting point of threshold curve section 2

15004850 CAM_NR1_CON NR1 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**NR1_CT_EN**				
Type												RW				
Reset												0				

Bit(s)	Name	Description
4	NR1_CT_EN	**Double buffer** Enables NR1 Cross-Talk compensation

15004854 CAM_NR1_CT_CON NR1 Crosstalk Compensation Configuration Register 50802003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**NR1_CT_DIV**		**NR1_CT_SLOPE**				**NR1_MBND**									
Type	RW		RW				RW									
Reset	0	1	0	1			0	0	1	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			NR1_CT_THRD										NR1_CT_MD2		NR1_CT_MD	
Type			RW										RW		RW	
Reset			1	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit(s)	Name	Description
31:30	NR1_CT_DIV	**Selects CT compensation value when CT detector output is false (minimum value of m_diff)** 0: Compensation value is clipped to 0. 1: Compensation value is 1/8 of the value. 2: Compensation value is 1/4 of the value. 3: Compensation value is half of the value.
29:28	NR1_CT_SLOPE	**Slope for CT suppression condition** Valid: 0 ~ 3 0: Steepest 1: Steep 2: Moderate 3: Gentle slope
25:16	NR1_MBND	**CT_MBND valid for 0~1023** Threshold of the difference between central pixel and neighbor pixels to calculate the mean value 128
13:4	NR1_CT_THRD	**Threshold for suppression condition**
3:2	NR1_CT_MD2	**Prevents over-compensation** 0: MT6238 algorithm (no limit for over-compensation) 1: Avoid 50% over-compensation (recommended) 2: Avoid 75% over-compensation 3: Avoid 100% over-compensation
1:0	NR1_CT_MD	**Selects pixels to use for CT detection** 0: 4 pixels (Xa, Xb, Xc, Xd) 1: 12 pixels (Xa ~ Xd, X1 ~ X8) 2: 8 pixels (X1 ~ X8) 3: 8 pixels (Xa ~ Xd, X5 ~ X8)

15004858 **CAM_BNR_RSV1** **BNR RSV1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RSV1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RSV1	Reserved 1

1500485C **CAM_BNR_RSV2** **BNR RSV2** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RSV2[31:16]															

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Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RSV2[15:0]**															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	RSV2	Reserved 2

15004880 **CAM_PGN_SATU_1** **PGN_SATU_1** **0FFF0FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**PGN_SATU_GB**											
Type					USER0											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**PGN_SATU_B**											
Type					USER0											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27:16	PGN_SATU_GB	**Double buffer** Q0.12.0: Saturation clip for Gb
11:0	PGN_SATU_B	**Double buffer** Q0.12.0: Saturation clip for B

15004884 **CAM_PGN_SATU_2** **PGN_SATU_2** **0FFF0FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**PGN_SATU_R**											
Type					USER0											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**PGN_SATU_GR**											
Type					USER0											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27:16	PGN_SATU_R	**Double buffer** Q0.12.0: Saturation clip for R
11:0	PGN_SATU_GR	**Double buffer** Q0.12.0: Saturation clip for Gr

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15004888 **CAM_PGN_GAIN_1** **PGN_GAIN_1** **02000200**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				PGN_GAIN_GB												
Type				USER0												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PGN_GAIN_B												
Type				USER0												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	PGN_GAIN_GB	**Double buffer** Q0.4.9: Gain for Gb
12:0	PGN_GAIN_B	**Double buffer** Q0.4.9: Gain for B

1500488C **CAM_PGN_GAIN_2** **PGN_GAIN_2** **02000200**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				PGN_GAIN_R												
Type				USER0												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PGN_GAIN_GR												
Type				USER0												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	PGN_GAIN_R	**Double buffer** Q0.4.9: Gain for R
12:0	PGN_GAIN_GR	**Double buffer** Q0.4.9: Gain for Gr

15004890 **CAM_PGN_OFST_1** **PGN_OFST_1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					PGN_OFST_GB											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					PGN_OFST_B											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
27:16	PGN_OFST_GB	**Double buffer** Q1.11.0: Offset for Gb
11:0	PGN_OFST_B	**Double buffer** Q1.11.0: Offset for B

15004894 **CAM_PGN_OFST_2** **PGN_OFST_2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**PGN_OFST_R**											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**PGN_OFST_GR**											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	PGN_OFST_R	**Double buffer** Q1.11.0: Offset for R
11:0	PGN_OFST_GR	**Double buffer** Q1.11.0: Offset for Gr

150048A0 **CAM_DM_O_BYP** **DM_O_BYP** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**DM_FG_MODE**	**DM_HF_LSC_MAX_BYP**	**DM_DEBUG_MODE**		**DM_BYP**
Type												RW	RW	RW		RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	DM_FG_MODE	**#DM_FG_MODE**
3	DM_HF_LSC_MAX_BYP	**LSC gain bypass process** The LSC gain output value will all be equal to input gain value. 0: Normal output (with 2x2 max) 1: LSC gain output bypass without 2x2 max
2:1	DM_DEBUG_MODE	**Debug mode for output signals** 0: Normal output

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Bit(s)	Name	Description
		1: Output direction image 2: Output activity 3: Output HF image
0	DM_BYP	**Bypasess bayer to RGB process** The RGB value will be equal to input bayer value. 0: Normal mode 1: Bypass DM for debugging purpose

150048A4 **CAM_DM_O_ED_FLAT** **DM_O_ED_FLAT** **0000FF03**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DM_FLAT_TH														DM_STEP_DET_MODE	DM_FLAT_DET_MODE
Type	RW														RW	RW
Reset	1	1	1	1	1	1	1	1							1	1

Bit(s)	Name	Description
15:8	DM_FLAT_TH	**Flat region threshold**
1	DM_STEP_DET_MODE	**STEP detection diameter** 0: HV priority 1: Diagonal priority
0	DM_FLAT_DET_MODE	**Flat detection diameter** 0: Small with Green only 1: Large with Green and RB

150048A8 **CAM_DM_O_ED_NYQ** **DM_O_ED_NYQ** **0100FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							DM_HF_NYQ_GAIN		DM_NYQ_TH_3							
Type							RW		RW							
Reset							0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DM_NYQ_TH_2								DM_NYQ_TH_1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
25:24	DM_HF_NYQ_GAIN	**Nyquist HF gain with F1 HF** 0 1 2 3 0: 1/1 HF Gain for Nyqquist 1: 1/2 HF Gain for Nyqquist 2: 1/4 HF Gain for Nyqquist

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Bit(s)	Name	Description
		3: 1/8 HF Gain for Nyqquist
23:16	DM_NYQ_TH_3	**Line condition for BAYER_NYQ_TH**
15:8	DM_NYQ_TH_2	**Nyquist edge detection Threshold2** Unconditional
7:0	DM_NYQ_TH_1	**Nyquist edge detection threshold** Conditional by BAYER_NYQ_TH3

150048AC **CAM_DM_O_ED_STEP** **DM_O_ED_STEP** **80FF00FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DM_RB_MODE								DM_STEP_TH_3							
Type	RW								RW							
Reset	1								1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DM_STEP_TH_2								DM_STEP_TH_1							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31	DM_RB_MODE	0: Standard filter size 1: Large filter size
23:16	DM_STEP_TH_3	**3 line edge condition for BAYER_STEP_TH**
15:8	DM_STEP_TH_2	**1 line and 2 line frequency condition for BAYER_STEP_TH**
7:0	DM_STEP_TH_1	**Step Edge TH** Unconditional

150048B0 **CAM_DM_O_RGB_HF** **DM_O_RGB_HF** **01084208**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DM_SSG_MODE	DM_RB_MODE_HV		DM_RB_MODE_D		DM_RB_MODE_F		DM_ROUGH_G_D					DM_ROUGH_G_F[4:1]			
Type	RW	RW		RW		RW		RW					RW			
Reset	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DM_ROUGH_G_F[0:0]	DM_ROUGH_RB_D					DM_ROUGH_RB_F					DM_HF_CORE_GAIN				
Type	RW	RW					RW					RW				
Reset	0	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
31	DM_SSG_MODE	**Small scale Green**

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Bit(s)	Name	Description
		0: For high ISP 1: For standard
30:29	DM_RB_MODE_HV	**Chroma interpolation at Hor/Ver** 0: Small diameter 1: Mid diameter 2: Large diameter 3: Largest
28:27	DM_RB_MODE_D	**Chroma interpolation at diagonal** 0: Small diameter 1: Mid diameter 2: Large diameter 3: Largest
26:25	DM_RB_MODE_F	**Chroma interpolation at flat** 0: Small diameter 1: Mid diameter 2: Large diameter 3: Largest
24:20	DM_ROUGH_G_D	**F1 roughness for G at diagonal** 0 ~ 31
19:15	DM_ROUGH_G_F	**F1 roughness for G at flat** 0 ~ 31
14:10	DM_ROUGH_RB_D	**F1 and F2 roughness for RB at diagonal** 0 ~ 31
9:5	DM_ROUGH_RB_F	**F1 roughness for RB at flat** 0 ~ 31
4:0	DM_HF_CORE_GAIN	**0 ~ 16** 0: Adaptive horizontal/vertical 100% 8: Hor./Ver. 50% core 50% 16: Core HF 100%

150048B4 **CAM_DM_O_DOT** **DM_O_DOT** **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DM_DOT_W_TH								DM_DOT_B_TH							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:8	DM_DOT_W_TH	**Cancels white dot induced by rb_hf** 0 ~ 255
7:0	DM_DOT_B_TH	**Cancels black dot induced by rb_hf** 0 ~ 255

150048B8 **CAM_DM_O_F1_ACT** **DM_O_F1_ACT** **0003FE00**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											DM_F1_SLOPE_2		DM_F1_SLOPE_1		DM_F1_TH_2[8:7]	
Type											RW		RW		RW	
Reset											0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DM_F1_TH_2[6:0]							DM_F1_TH_1								
Type	RW							RW								
Reset	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:20	DM_F1_SLOPE_2	**F1 higher slope** 0: 32 1: 64 2: 128 3: 256
19:18	DM_F1_SLOPE_1	**F1 lower slope** 0: 32 1: 64 2: 128 3: 256
17:9	DM_F1_TH_2	**F1 higher threshold (BAYER_F1_TH1 <= BAYER_F1_TH2)** 0 ~ 511
8:0	DM_F1_TH_1	**F1 lower threshold (BAYER_F1_TH1 <= BAYER_F1_TH2)** 0 ~ 511

150048BC **CAM_DM_O_F2_ACT** **DM_O_F2_ACT** **0003FE00**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											DM_F2_SLOPE_2		DM_F2_SLOPE_1		DM_F2_TH_2[8:7]	
Type											RW		RW		RW	
Reset											0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DM_F2_TH_2[6:0]							DM_F2_TH_1								
Type	RW							RW								
Reset	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:20	DM_F2_SLOPE_2	**F2 higher slope** 0: 32 1: 64 2: 128 3: 256
19:18	DM_F2_SLOPE_1	**F2 lower slope** 0: 32 1: 64 2: 128 3: 256
17:9	DM_F2_TH_2	**F2 higher threshold (BAYER_F2_TH1 <= BAYER_F2_TH2)** 0 ~ 511
8:0	DM_F2_TH_1	**F2 lower threshold (BAYER_F2_TH1 <= BAYER_F2_TH2)** 0 ~ 511

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150048C0 **CAM_DM_O_F3_ACT** **DM_O_F3_ACT** **0003FE00**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											DM_F3_SLOPE_2		DM_F3_SLOPE_1		DM_F3_TH_2[8:7]	
Type											RW		RW		RW	
Reset											0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DM_F3_TH_2[6:0]							DM_F3_TH_1								
Type	RW							RW								
Reset	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:20	DM_F3_SLOPE_2	**F3 higher slope** 0: 32 1: 64 2: 128 3: 256
19:18	DM_F3_SLOPE_1	**F3 lower slope** 0: 32 1: 64 2: 128 3: 256
17:9	DM_F3_TH_2	**F3 higher threshold (BAYER_F3_TH1 <= BAYER_F3_TH2)** 0 ~511
8:0	DM_F3_TH_1	**F3 lower threshold (BAYER_F3_TH1 <= BAYER_F3_TH2)** 0 ~ 511

150048C4 **CAM_DM_O_F4_ACT** **DM_O_F4_ACT** **0003FE00**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											DM_F4_SLOPE_2		DM_F4_SLOPE_1		DM_F4_TH_2[8:7]	
Type											RW		RW		RW	
Reset											0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DM_F4_TH_2[6:0]							DM_F4_TH_1								
Type	RW							RW								
Reset	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:20	DM_F4_SLOPE_2	**F4 higher slope** 0: 32 1: 64 2: 128 3: 256
19:18	DM_F4_SLOPE_1	**F4 lower slope** 0: 32 1: 64 2: 128 3: 256
17:9	DM_F4_TH_2	**F4 higher threshold (BAYER_F4_TH1 <= BAYER_F4_TH2)**

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Bit(s)	Name	Description
		0 ~ 511
8:0	DM_F4_TH_1	**F4 lower threshold (BAYER_F4_TH1 <= BAYER_F4_TH2)** 0 ~ 511

150048C8 **CAM_DM_O_F1_L** **DM_O_F1_L** **01084210**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								**DM_F1_LLUT_Y4**					**DM_F1_LLUT_Y3[4:1]**			
Type								RW					RW			
Reset								1	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DM_F1_LLUT_Y3[0:0]**	**DM_F1_LLUT_Y2**					**DM_F1_LLUT_Y1**					**DM_F1_LLUT_Y0**				
Type	RW	RW					RW					RW				
Reset	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
24:20	DM_F1_LLUT_Y4	**F1 Luma level dependent LUT** 0 ~ 31 16: x1.0
19:15	DM_F1_LLUT_Y3	**F1 Luma level dependent LUT** 0 ~ 31 16: x1.0
14:10	DM_F1_LLUT_Y2	**F1 Luma level dependent LUT** 0 ~ 31 16: x1.0
9:5	DM_F1_LLUT_Y1	**F1 Luma level dependent LUT** 0 ~ 31 16: x1.0
4:0	DM_F1_LLUT_Y0	**F1 Luma level dependent LUT** 0 ~ 31 16: x1.0

150048CC **CAM_DM_O_F2_L** **DM_O_F2_L** **01084210**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								**DM_F2_LLUT_Y4**					**DM_F2_LLUT_Y3[4:1]**			
Type								RW					RW			
Reset								1	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DM_F2_LLUT_Y3[0:0]**	**DM_F2_LLUT_Y2**					**DM_F2_LLUT_Y1**					**DM_F2_LLUT_Y0**				
Type	RW	RW					RW					RW				
Reset	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0

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Bit(s)	Name	Description
24:20	DM_F2_LLUT_Y4	**F2 Luma level dependent LUT** 0 ~ 31 16: x1.0
19:15	DM_F2_LLUT_Y3	**F2 Luma level dependent LUT** 0 ~ 31 16: x1.0
14:10	DM_F2_LLUT_Y2	**F2 Luma level dependent LUT** 0 ~ 31 16: x1.0
9:5	DM_F2_LLUT_Y1	**F2 Luma level dependent LUT** 0 ~ 31 16: x1.0
4:0	DM_F2_LLUT_Y0	**F2 Luma level dependent LUT** 0 ~ 31 16: x1.0

150048D0 **CAM_DM_O_F3_L** **DM_O_F3_L** **01084210**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								DM_F3_LLUT_Y4					DM_F3_LLUT_Y3[4:1]			
Type								RW					RW			
Reset								1	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DM_F3_LLUT_Y3[0:0]	DM_F3_LLUT_Y2					DM_F3_LLUT_Y1					DM_F3_LLUT_Y0				
Type	RW	RW					RW					RW				
Reset	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
24:20	DM_F3_LLUT_Y4	**F3 Luma level dependent LUT** 0 ~ 31 16: x1.0
19:15	DM_F3_LLUT_Y3	**F3 Luma level dependent LUT** 0 ~ 31 16: x1.0
14:10	DM_F3_LLUT_Y2	**F3 Luma level dependent LUT** 0 ~ 31 16: x1.0
9:5	DM_F3_LLUT_Y1	**F3 Luma level dependent LUT** 0 ~ 31 16: x1.0
4:0	DM_F3_LLUT_Y0	**F3 Luma level dependent LUT** 0 ~ 31 16: x1.0

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150048D4 **CAM_DM_O_F4_L** **DM_O_F4_L** **01084210**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								DM_F4_LLUT_Y4					DM_F4_LLUT_Y3[4:1]			
Type								RW					RW			
Reset								1	0	0	0	0	1	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DM_F4_LLUT_Y3[0:0]	DM_F4_LLUT_Y2					DM_F4_LLUT_Y1					DM_F4_LLUT_Y0				
Type	RW	RW					RW					RW				
Reset	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
24:20	DM_F4_LLUT_Y4	**F4 Luma level dependent LUT** 0 ~ 31 16: x1.0
19:15	DM_F4_LLUT_Y3	**F4 Luma level dependent LUT** 0 ~ 31 16: x1.0
14:10	DM_F4_LLUT_Y2	**F4 Luma level dependent LUT** 0 ~ 31 16: x1.0
9:5	DM_F4_LLUT_Y1	**F4 Luma level dependent LUT** 0 ~ 31 16: x1.0
4:0	DM_F4_LLUT_Y0	**F4 Luma level dependent LUT** 0 ~ 31 16: x1.0

150048D8 **CAM_DM_O_HF_RB** **DM_O_HF_RB** **000403FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														DM_HF_CLIP[8:6]		
Type														RW		
Reset														1	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DM_HF_CLIP[5:0]						DM_RB_DIFF_TH									
Type	RW						RW									
Reset	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
18:10	DM_HF_CLIP	HF clip level
9:0	DM_RB_DIFF_TH	RB difference threshold for RB HF

150048DC **CAM_DM_O_HF_GAIN** **DM_O_HF_GAIN** **00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DM_HF_GLOBL_GAIN			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	DM_HF_GLOBL_GAIN	**HF global gain** 0 ~ 15

150048E0 **CAM_DM_O_HF_COMP** **DM_O_HF_COMP** **FF048888**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DM_HF_UND_ACT_TH								DM_HF_UND_TH							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DM_HF_LSC_GAIN3				DM_HF_LSC_GAIN2				DM_HF_LSC_GAIN1				DM_HF_LSC_GAIN0			
Type	RW				RW				RW				RW			
Reset	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0

Bit(s)	Name	Description
31:24	DM_HF_UND_ACT_TH	**Activity threshold for canceling undershoot** 0 ~ 255
23:16	DM_HF_UND_TH	**Luma threshold for canceling undershoot** 0 ~ 255
15:12	DM_HF_LSC_GAIN3	**LSC gain compensation for Region 3** 0 ~ 8
11:8	DM_HF_LSC_GAIN2	**LSC gain compensation for Region 2** 0 ~ 8
7:4	DM_HF_LSC_GAIN1	**LSC gain compensation for Region 1** 0 ~ 8
3:0	DM_HF_LSC_GAIN0	**LSC gain compensation for Region 0** 0 ~ 8

150048E4 **CAM_DM_O_HF_CORIN_TH** **DM_O_HF_CORIN_TH** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DM_HF_CORIN_TH							
Type									RW							
Reset									0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
7:0	DM_HF_CORIN_TH	**HF coring threshold** 0 ~ 255

150048E8 **CAM_DM_O_ACT_LUT** **DM_O_ACT_LUT** **00842108**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								**DM_ACT_LUT_Y4**					**DM_ACT_LUT_Y3[4:1]**			
Type								RW					RW			
Reset								0	1	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DM_ACT_LUT_Y3[0:0]**	**DM_ACT_LUT_Y2**					**DM_ACT_LUT_Y1**					**DM_ACT_LUT_Y0**				
Type	RW	RW					RW					RW				
Reset	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
24:20	DM_ACT_LUT_Y4	**Activity modulation by Luma** 0 ~ 31
19:15	DM_ACT_LUT_Y3	**Activity modulation by Luma** 0 ~ 31
14:10	DM_ACT_LUT_Y2	**Activity modulation by Luma** 0 ~ 31
9:5	DM_ACT_LUT_Y1	**Activity modulation by Luma** 0 ~ 31
4:0	DM_ACT_LUT_Y0	**Activity modulation by Luma** 0 ~ 31

150048F0 **CAM_DM_O_SPARE** **DM_O_SPARE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DM_O_SPARE[30:15]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DM_O_SPARE[14:0]**															**DM_MG_BYP**
Type	RW															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:1	DM_O_SPARE	Reserved for spare registers
0	DM_MG_BYP	0: mg blending according to act (original) 1: mg depends on sg (modified)

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150048F4 **CAM_DM_O_BB** **DM_O_BB** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												**DM_BB_TH_2[8:4]**				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DM_BB_TH_2[3:0]**							**DM_BB_TH_1**								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:12	DM_BB_TH_2	**Threshold between MS_G and SS_G** 0 ~ 511
8:0	DM_BB_TH_1	**Threshold between LS_G and MS_G** 0 ~ 511

15004910 **CAM_CCL_GTC** **CCL Global Threshold Configuration** **00000CCC**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**CCL_GLOBL_TH**											
Type					RW											
Reset					1	1	0	0	1	1	0	0	1	1	0	0

Bit(s)	Name	Description
11:0	CCL_GLOBL_TH	Global threshold

15004914 **CAM_CCL_ADC** **CCL Anti De-saturation Configuration** **00130800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											**CCL_ADSAT_SLOPE**					
Type											RW					
Reset											0	1	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**CCL_ADSAT_TH**											
Type					RW											
Reset					1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:16	CCL_ADSAT_SLOPE	Anti de-saturation slope
11:0	CCL_ADSAT_TH	Anti de-saturation threshold

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15004918 CAM_CCL_BAC CCL Blue Adjustment Configuration 04002050

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CCL_B_DIFF											
Type					RW											
Reset					0	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CCL_B_SLOPE				CCL_B_OFST											
Type	RW				RW											
Reset	0	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0

Bit(s)	Name	Description
27:16	CCL_B_DIFF	Blue adjustment diff
15:12	CCL_B_SLOPE	Blue adjustment slope
11:0	CCL_B_OFST	Blue adjustment offset

15004920 CAM_G2G_CNV_1 G2G Matrix Coefficient 00000200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				G2G_CNV_01												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				G2G_CNV_00												
Type				USER0												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	G2G_CNV_01	**Double buffer** G2G matrix 0,1 coefficient
12:0	G2G_CNV_00	**Double buffer** G2G matrix 0,0 coefficient

15004924 CAM_G2G_CNV_2 G2G Matrix Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				G2G_CNV_02												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	G2G_CNV_02	**Double buffer** G2G matrix 0,2 coefficient

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15004928 **CAM_G2G_CNV_3** **G2G Matrix Coefficient** **02000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				G2G_CNV_11												
Type				USER0												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				G2G_CNV_10												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	G2G_CNV_11	**Double buffer** G2G matrix 1,1 coefficient
12:0	G2G_CNV_10	**Double buffer** G2G matrix 1,0 coefficient

1500492C **CAM_G2G_CNV_4** **G2G Matrix Coefficient** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				G2G_CNV_12												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	G2G_CNV_12	**Double buffer** G2G matrix 1,2 coefficient

15004930 **CAM_G2G_CNV_5** **G2G Matrix Coefficient** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				G2G_CNV_21												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				G2G_CNV_20												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	G2G_CNV_21	**Double buffer** G2G matrix 2,1 coefficient
12:0	G2G_CNV_20	**Double buffer** G2G matrix 2,0 coefficient

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15004934 **CAM_G2G_CNV_6** **G2G Matrix Coefficient** **00000200**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				G2G_CNV_22												
Type				USER0												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	G2G_CNV_22	**Double buffer** G2G matrix 2,2 coefficient

15004938 **CAM_G2G_CTRL** **G2G Control** **00000009**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											G2G_POFST_R	G2G_MOFST_R	G2G_ACC			
Type											RW	RW	RW			
Reset											0	0	1	0	0	1

Bit(s)	Name	Description
5	G2G_POFST_R	**G2G output R offset** 1'b0: out_R = out_R 1'b1: out_R = out_R + 256
4	G2G_MOFST_R	**G2G input R offset** 1'b0: in_R = in_R 1'b1: in_R = in_R - 256
3:0	G2G_ACC	**4'd11: Q1.1.11 precision** 4'd10: Q1.2.10 precision 4'd9: Q1.3.9 precision 4'd8: Q1.4.8 precision 4'd7: Q1.5.7 precision 4'd6: Q1.6.6 precision

15004948 **CAM_UNP_OFST** **UNP Bit Offset** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				UNP_OFST_EDB								UNP_OFST_STB				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
12:8	UNP_OFST_EDB	10-bit mode: End bit offset
4:0	UNP_OFST_STB	10-bit mode: Start bit offset

15004950 CAM_C02_CON C02 Control Register 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													C02_TPIPE_EDGE			
Type													RW			
Reset													1	1	1	1

Bit(s)	Name	Description
3:0	C02_TPIPE_EDGE	T-pipe edge control

15004954 CAM_C02_CROP_CON1 C02 Crop X Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C02_CROP_XEND												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C02_CROP_XSTART												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	C02_CROP_XEND	C02 crop end point x
12:0	C02_CROP_XSTART	C02 crop start point x

15004958 CAM_C02_CROP_CON2 C02 Crop Y Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C02_CROP_YEND												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C02_CROP_YSTART												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
28:16	C02_CROP_YEND	C02 crop end point y
12:0	C02_CROP_YSTART	C02 crop start point y

15004960 **CAM_MFB_CON** **MFB Control** **0F000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BLD_MM_TH															
Type	RW															
Reset	0	0	0	0	1	1	1	1								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RESERVED					BLD_MODE		
Type									RW					RW		
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
31:24	BLD_MM_TH	**Threshold of maximum difference for multi-motion mode**
2:0	BLD_MODE	**MFB blending mode** 0: Lowlight mode, first pass (no blended weight read-in) 1: Lowlight mode, following pass (requires blended weight read-in) 2: Multi-motion mode, first pass (no background image) 3: Multi-motion mode, following pass (first dma-in image is background image) 4: Reserved 5: Post blend mode (requires blended weight read-in)

15004964 **CAM_MFB_LL_CON1** **MFB LL Control 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				BLD_LL_OUT_YSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BLD_LL_OUT_XOFST			BLD_LL_OUT_XSIZE												
Type	RW			RW												
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	BLD_LL_OUT_YSIZE	Output image y size
15	BLD_LL_OUT_XOFST	Output image x offset
12:0	BLD_LL_OUT_XSIZE	Output image x size

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15004968 **CAM_MFB_LL_CON2** **MFB LL Control 2** **140A0606**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BLD_LL_TH2								BLD_LL_TH1							
Type	RW								RW							
Reset	0	0	0	1	0	1	0	0	0	0	0	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BLD_LL_DT1													BLD_LL_MAX_WT		
Type	RW													RW		
Reset	0	0	0	0	0	1	1	0						1	1	0

Bit(s)	Name	Description
31:24	BLD_LL_TH2	**Weighting threshold 1**
23:16	BLD_LL_TH1	**Weighting threshold 2**
15:8	BLD_LL_DT1	**Weighting slope**
2:0	BLD_LL_MAX_WT	**Max. blending weight (0<= BLD_LL_MAX_WT <= 7)** Total frames: 2 => BLD_LL_MAX_WT: 7 Total frames: 3 => BLD_LL_MAX_WT: 6 Total frames: 4 => BLD_LL_MAX_WT: 6 Total frames: 5 => BLD_LL_MAX_WT: 5 Total frames: 6 => BLD_LL_MAX_WT: 5 Total frames: 7 => BLD_LL_MAX_WT: 5 Total frames: 8 => BLD_LL_MAX_WT: 5

1500496C **CAM_MFB_LL_CON3** **MFB LL Control 3** **000F0011**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BLD_LL_TH_E							
Type									RW							
Reset									0	0	0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BLD_LL_DB_YDIST				BLD_LL_DB_XDIST							BLD_LL_DB_EN				BLD_LL_BRZ_EN
Type	RW				RW							RW				RW
Reset	0	0	0	0	0	0	0	0				1				1

Bit(s)	Name	Description
23:16	BLD_LL_TH_E	
15:12	BLD_LL_DB_YDIST	**Vertical distance to the upper non-overlapped 16x16 block boundary** The y coordinate corresponds to full resolution image % 16.
11:8	BLD_LL_DB_XDIST	**Horizontal distance to the left non-overlapped 16x16 block boundary** The x coordinate corresponds to full resolution image % 16.
4	BLD_LL_DB_EN	**Deblocks filter** 0: Disable 1: Enable
0	BLD_LL_BRZ_EN	**Controls bilinear filter**

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Bit(s)	Name	Description
		0: Disable 1: Enable

15004970 **CAM_MFB_LL_CON4** **MFB LL Control 4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BLD_LL_CLIP_TH2								BLD_LL_CLIP_TH1							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name							BLD_LL_FLT_WT_MODE2			BLD_LL_FLT_WT_MODE1					BLD_LL_FLT_MODE	
Type							RW			RW					RW	
Reset							0	0		0	0	0			0	0

Bit(s)	Name	Description
31:24	BLD_LL_CLIP_TH2	**Clip threshold 2**
23:16	BLD_LL_CLIP_TH1	**Clip threshold 1**
9:8	BLD_LL_FLT_WT_MODE2	**Weighting filter mode 2** Valid values: 0 ~ 2
6:4	BLD_LL_FLT_WT_MODE1	**Weighting filter mode 1** Valid value: 0 ~ 5
1:0	BLD_LL_FLT_MODE	**Filter mode** Valid value: 0 ~ 2

15004974 **CAM_MFB_LL_CON5** **MFB LL Control 5** **00068C64**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BLD_LL_MX_DT							
Type									RW							
Reset									0	0	0	0	0	1	1	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	BLD_LL_MX_M1								BLD_LL_MX_M0							
Type	RW								RW							
Reset	1	0	0	0	1	1	0	0	0	1	1	0	0	1	0	0

Bit(s)	Name	Description
23:16	BLD_LL_MX_DT	Mixer slope
15:8	BLD_LL_MX_M1	Mixer threshold M1
7:0	BLD_LL_MX_M0	Mixer threshold M0

15004978 **CAM_MFB_LL_CON6** **MFB LL Control 6** **0000DC0A**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

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Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BLD_LL_MX_B1								BLD_LL_MX_B0							
Type	RW								RW							
Reset	1	1	0	1	1	1	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:8	BLD_LL_MX_B1	Mixer weighting upper bound
7:0	BLD_LL_MX_B0	Mixer weighting lower bound

150049C0 CAM_LCE_CON LCE Control Register 000000FE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESERVED															
Type	RW															
Reset	0	0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									LCE_GLOB_VHALF							LCE_GLOB
Type									RW							RW
Reset									1	1	1	1	1	1	1	0

Bit(s)	Name	Description
7:1	LCE_GLOB_VHALF	**When LCE_GLOB =1,** Vhalf value= LCE_GLOB_VHALF<<5
0	LCE_GLOB	**Vhalf value** 0: vhalf value comes from lightmap. 1: vhalf value= LCE_GLOBAL_VHALF<<5

150049C4 CAM_LCE_ZR LCE Zoom Ratio 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		LCE_BCMK_Y														
Type		RW														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		LCE_BCMK_X														
Type		RW														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:16	LCE_BCMK_Y	**Vertical zoom ratio** The unit distance for vertical direction is 32768; LCE_BCMK_Y is set to {floor[32768*(small lightmap vertical size-1)/(image vertical size-1)]}
14:0	LCE_BCMK_X	**Horizontal zoom ratio** The unit distance for horizontal direction is 32768; LCE_BCMK_X is set to {floor[32768*(small lightmap horizontal size-1)/(image horizontal size-1)]}

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150049C8 CAM_LCE_QUA LCE Quality Register 00000040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									LCE_BA							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LCE_PB									LCE_PA						
Type	RW									RW						
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	LCE_BA	**Double buffer** Strength parameter Q0.8.0
15:7	LCE_PB	**Double buffer** Strength parameter Q1.8.0
6:0	LCE_PA	**Double buffer** Strength parameter Q0.1.6

150049CC CAM_LCE_DGC_1 LCE Degamma Control 1 2A1B1209

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LCE_DG_4								LCE_DG_3							
Type	RW								RW							
Reset	0	0	1	0	1	0	1	0	0	0	0	1	1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LCE_DG_2								LCE_DG_1							
Type	RW								RW							
Reset	0	0	0	1	0	0	1	0	0	0	0	0	1	0	0	1

Bit(s)	Name	Description
31:24	LCE_DG_4	Degamma control point X4 (128)
23:16	LCE_DG_3	Degamma control point X3 (96)
15:8	LCE_DG_2	Degamma control point X2 (64)
7:0	LCE_DG_1	Degamma control point X1 (32)

150049D0 CAM_LCE_DGC_2 LCE Degamma Control 2 0098603F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									LCE_DG_7							
Type									RW							
Reset									1	0	0	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LCE_DG_6								LCE_DG_5							
Type	RW								RW							
Reset	0	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1

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Bit(s)	Name	Description
23:16	LCE_DG_7	Degamma control point X7 (224)
15:8	LCE_DG_6	Degamma control point X6 (196)
7:0	LCE_DG_5	Degamma control point X5 (160)

150049D4 **CAM_LCE_GM** **LCE Gain Modification** **00001080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name			LCE_GM_TH						LCE_GM_LB							
Type			RW						RW							
Reset			0	1	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:8	LCE_GM_TH	Gain modification threshold
7:0	LCE_GM_LB	Gain modification lower bound

150049E0 **CAM_LCE_SLM_LB** **LCE SLM Lower Bound** **00000020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name										LCE_SLM_LB						
Type										RW						
Reset										0	1	0	0	0	0	0

Bit(s)	Name	Description
6:0	LCE_SLM_LB	**Lower bound of small light map** Value = 0~63

150049E4 **CAM_LCE_SLM_SIZE** **LCE SLM Size** **00003040**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name		LCE_SLM_HT								LCE_SLM_WD						
Type		RW								RW						
Reset		0	1	1	0	0	0	0		1	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
14:8	LCE_SLM_HT	**Small light map height** Max. value: 72
6:0	LCE_SLM_WD	**Small light map width** Max. value: 96 (must be multiple of 2)

150049E8 **CAM_LCE_OFST** **LCE Offset** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		LCE_OFST_Y														
Type		RW														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		LCE_OFST_X														
Type		RW														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:16	LCE_OFST_Y	Decimal part of vertical start point of small light map
14:0	LCE_OFST_X	Decimal part of horizontal start point of small light map

150049EC **CAM_LCE_BIAS** **LCE Bias** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							LCE_BIAS_Y							LCE_BIAS_X		
Type							RW							RW		
Reset							0	0						0	0	0

Bit(s)	Name	Description
9:8	LCE_BIAS_Y	**Integer part of vertical start point of small light map** Range: 0~3
2:0	LCE_BIAS_X	**Integer part of horizontal start point of small light map** Range: 0~4

150049F0 **CAM_LCE_IMAGE_SIZE** **LCE Image Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LCE_IMAGE_HT												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				LCE_IMAGE_WD												
Type				RW												

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Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	LCE_IMAGE_HT	Image height (line number)
12:0	LCE_IMAGE_WD	Image width (pixel number)

15004A00 **CAM_CPG_SATU_1** **CPG_SATU_1** **0FFF0FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CPG_SATU_GB											
Type					USER0											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CPG_SATU_B											
Type					USER0											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27:16	CPG_SATU_GB	**Double buffer** Q0.12.0: Saturation clip for Gb
11:0	CPG_SATU_B	**Double buffer** Q0.12.0: Saturation clip for B

15004A04 **CAM_CPG_SATU_2** **CPG_SATU_2** **0FFF0FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CPG_SATU_R											
Type					USER0											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CPG_SATU_GR											
Type					USER0											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27:16	CPG_SATU_R	**Double buffer** Q0.12.0: Saturation clip for R
11:0	CPG_SATU_GR	**Double buffer** Q0.12.0: Saturation clip for Gr

15004A08 **CAM_CPG_GAIN_1** **CPG_GAIN_1** **02000200**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				CPG_GAIN_GB												

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Type				USER0												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**CPG_GAIN_B**												
Type				USER0												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	CPG_GAIN_GB	**Double buffer** Q0.4.9: Gain for Gb
12:0	CPG_GAIN_B	**Double buffer** Q0.4.9: Gain for B

15004A0C **CAM_CPG_GAIN_2** **CPG_GAIN_2** **02000200**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**CPG_GAIN_R**												
Type				USER0												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**CPG_GAIN_GR**												
Type				USER0												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	CPG_GAIN_R	**Double buffer** Q0.4.9: Gain for R
12:0	CPG_GAIN_GR	**Double buffer** Q0.4.9: Gain for Gr

15004A10 **CAM_CPG_OFST_1** **CPG_OFST_1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**CPG_OFST_GB**											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**CPG_OFST_B**											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	CPG_OFST_GB	**Double buffer** Q1.11.0: Offset for Gb
11:0	CPG_OFST_B	**Double buffer** Q1.11.0:

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Bit(s)	Name	Description
		Offset for B

15004A14 **CAM_CPG_OFST_2** **CPG_OFST_2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CPG_OFST_R											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CPG_OFST_GR											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	CPG_OFST_R	**Double buffer** Q1.11.0: Offset for R
11:0	CPG_OFST_GR	**Double buffer** Q1.11.0: Offset for Gr

15004A1C **CAM_C42_CON** **YUV444 to YUV422 Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																C42_FILT_DIS
Type																USER0
Reset																0

Bit(s)	Name	Description
0	C42_FILT_DIS	**Double buffer** Enables YUV 444-to-422 horizontal 4-tap filter. 0: Horizontal 4-tap down-sampling filter 1: UV drop

15004A20 **CAM_ANR_CON1** **ANR Control Register 1** **01080200**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								ANR_LCE_LINK					ANR_Y_LUMA_SCALE			

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Type								RW					RW			
Reset								1					1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				ANR_MODE		ANR_FLT_MODE					ANR_SCALE_MODE				ANR_ENY	ANR_ENC
Type				RW		RW					RW				RW	RW
Reset				0		0	1	0			0	0			0	0

Bit(s)	Name	Description
24	ANR_LCE_LINK	**Double buffer** Enables link with LCE
19:16	ANR_Y_LUMA_SCALE	**Double buffer** Different in TPIPE mode and frame mode. TPIPE mode = (IC || N3D_IC || TDR_EN) TPIPE mode: The blending ratio between input and 7x7 lowpass filtered output. The blending result is for luma LUT. Valid range: 0 ~ 8. 0 is the un-filter image, and 8 is the 7x7 lowpas filter output. Frame mode: 0: Use input to calculate the difference 1: Use the 3x3 or 3x2 low pass filter on center pixel to calculate the difference in range filter. It reduces jaggy edges with a little reduced sharpness.
12	ANR_MODE	**Double buffer** Reserved. For using verification cmodel, it should be programmed correctly as "!(IC||N3D_IC||TDR_EN)".
10:8	ANR_FLT_MODE	**Double buffer** Different in TPIPE mode and frame mode. TPIPE mode = (IC || N3D_IC || TDR_EN) In frame mode: 0: No IIR 1: 2 lines of IIR 2: 3 lines of IIR 3: 3 lines of IIR 4: 4 lines of IIR 5: 4 lines of IIR In TPIPE mode: 0: No IIR
5:4	ANR_SCALE_MODE	**Double buffer** Different in TPIPE mode and frame mode. TPIPE mode = (IC || N3D_IC || TDR_EN) For TPIPE mode: 0: Use 19x19 kernel in luma channel and chroma 1: Use 19x19 and 39x39 kernel in luma and chroma channel respectively 2: Use 39x39 kernel in both luma and chroma channel (subsampled by 2) For frame mode: 0: Use single pixel as the luma LUT input Not 0: Use the 3x3 lowpass filter output as luma LUT input
1	ANR_ENY	**Double buffer** Enables Y ANR
0	ANR_ENC	**Double buffer** Enables C ANR

15004A24	CAM_ANR_CON2	ANR Control Register 2	00001012

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

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Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				ANR_GNC							ANR_GNY					
Type				RW							RW					
Reset				1	0	0	0	0			0	1	0	0	1	0

Bit(s)	Name	Description
12:8	ANR_GNC	**Blending weight of chroma bilateral filter output and 3x3 median filter** Valid range: 0~16. 16 means using only bilateral output.
5:0	ANR_GNY	**Luma channel blending weighting of input and bilateral output** Valid range: 0~32. 32 means using only bilateral output.

15004A28 CAM_ANR_CON3 ANR Control Register 3 00020001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ANR_QEC_VAL							
Type									RW							
Reset									0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				ANR_QEC				ANR_C_SM_EDGE			ANR_C_MED_EN				ANR_IMPL_MODE	
Type				RW				RW			RW				RW	
Reset				0				0			0	0			0	1

Bit(s)	Name	Description
23:16	ANR_QEC_VAL	**QEC function higher bound threshold to correct IIR propagation error**
12	ANR_QEC	**Enables QEC function to correct IIR propagation error**
8	ANR_C_SM_EDGE	**Enables chroma smooth edge function**
5:4	ANR_C_MED_EN	**Enables 3x3 median filter on chroma** 0: Disable 1: Low strength 2: Median strength 3: High strength
1:0	ANR_IMPL_MODE	**Valid: 0 ~ 2** 0: Does not apply min-max clipping 1: Apply min-max clipping on range filter difference calculation only 2: Apply min-max clipping on range filter difference calculation and weighted average in bilateral filter

15004A2C CAM_ANR_YAD1 ANR Luma NR Strength Adaption Register 1 09020101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					ANR_K_HI_TH								ANR_K_LO_TH			
Type					RW								RW			
Reset					1	0	0	1					0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name				**ANR_CEN_GAIN_HI_TH**								**ANR_CEN_GAIN_LO_TH**				
Type				RW								RW				
Reset				0	0	0	0	1				0	0	0	0	1

Bit(s)	Name	Description
27:24	ANR_K_HI_TH	**Kernel size upper bound** Valid range: 0~11. Rule: ANR_KSIZE_LO_TH <= ANR_KSIZE_HI_TH
19:16	ANR_K_LO_TH	**Kernel size lower bound** Valid range: 0~9. Rule: ANR_KSIZE_LO_TH <= ANR_KSIZE_HI_TH
12:8	ANR_CEN_GAIN_HI_TH	**Center pixel blending gain upper bound** Range: 0~16 Rule: ANR_CEN_GAIN_HI_TH >=ANR_CEN_GAIN_LO_TH
4:0	ANR_CEN_GAIN_LO_TH	**Center pixel blending gain lower bound** Range 0~16

15004A30 CAM_ANR_YAD2 ANR Luma NR Strength Adaption Register 2 00000206

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**ANR_PTY_GAIN_TH**									**ANR_PTY_VGAIN**			
Type				RW									RW			
Reset				0	0	0	1	0					0	1	1	0

Bit(s)	Name	Description
12:8	ANR_PTY_GAIN_TH	**Range filter PTY gain lower bound** Range 0~16
3:0	ANR_PTY_VGAIN	**Range filter gain in vertical bilateral filter** Range 0~15

15004A34 CAM_ANR_4LUT1 ANR Slope4 LUT Register 1 00A06428

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									**ANR_Y_CPX3**							
Type									RW							
Reset									1	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ANR_Y_CPX2**								**ANR_Y_CPX1**							
Type	RW								RW							
Reset	0	1	1	0	0	1	0	0	0	0	1	0	1	0	0	0

Bit(s)	Name	Description
23:16	ANR_Y_CPX3	**Luma LUT control point 3 luma axis [Q0.8.0]**
15:8	ANR_Y_CPX2	**Luma LUT control point 2 luma axis [Q0.8.0]**
7:0	ANR_Y_CPX1	**Luma LUT control point 1 luma axis [Q0.8.0]** Rule: ANR_Y_CPX1< ANR_Y_CPX2< ANR_Y_CPX3

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15004A38 CAM_ANR_4LUT2 ANR Slope4 LUT Register 2 080C1010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				ANR_Y_SCALE_CPY3								ANR_Y_SCALE_CPY2				
Type				RW								RW				
Reset				0	1	0	0	0				0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				ANR_Y_SCALE_CPY1								ANR_Y_SCALE_CPY0				
Type				RW								RW				
Reset				1	0	0	0	0				1	0	0	0	0

Bit(s)	Name	Description
28:24	ANR_Y_SCALE_CPY3	**Scale determination luma LUT. [Q0.1.4]** Valid range: 0~16
20:16	ANR_Y_SCALE_CPY2	**Scale determination luma LUT. [Q0.1.4]** Valid range: 0~16
12:8	ANR_Y_SCALE_CPY1	**Scale determination luma LUT. [Q0.1.4]** Valid range: 0~16
4:0	ANR_Y_SCALE_CPY0	**Scale determination luma LUT. [Q0.1.4]** Valid range: 0~16

15004A3C CAM_ANR_4LUT3 ANR Slope4 LUT Register 3 1F1E1E00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				ANR_Y_SCALE_SP3								ANR_Y_SCALE_SP2				
Type				RW								RW				
Reset				1	1	1	1	1				1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				ANR_Y_SCALE_SP1								ANR_Y_SCALE_SP0				
Type				RW								RW				
Reset				1	1	1	1	0				0	0	0	0	0

Bit(s)	Name	Description
28:24	ANR_Y_SCALE_SP3	**Scale determination luma LUT, slope 3. [Q1.0.5]** Valid range: -15~15
20:16	ANR_Y_SCALE_SP2	**Scale determination luma LUT, slope 2. [Q1.0.5]** Valid range: -15~15
12:8	ANR_Y_SCALE_SP1	**Scale determination luma LUT, slope 1. [Q1.0.5]** Valid range: -15~15
4:0	ANR_Y_SCALE_SP0	**Scale determination luma LUT, slope 0. [Q1.0.5]** Valid range: -15~15

15004A40 CAM_ANR_PTY ANR Luma Range Filter LUT Register 0C080402

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ANR_PTY4								ANR_PTY3							
Type	RW								RW							
Reset	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ANR_PTY2								ANR_PTY1							
Type	RW								RW							
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0

Bit(s)	Name	Description
31:24	ANR_PTY4	**Range filter difference step 4 parameter in bilateral filter**
23:16	ANR_PTY3	**Range filter difference step 3 parameter in bilateral filter**
15:8	ANR_PTY2	**Range filter difference step 2 parameter in bilateral filter**
7:0	ANR_PTY1	**Range filter difference step 1 parameter in bilateral filter** Rule: ANR_PTY1<= ANR_PTY2<= ANR_PTY3<= ANR_PTY3

15004A44 **CAM_ANR_CAD** **ANR Chroma NR Strength Adaption Register** **00460406**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ANR_C_L_DIFF_TH							
Type									RW							
Reset									0	1	0	0	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				ANR_PTC_GAIN_TH									ANR_PTC_VGAIN			
Type				RW									RW			
Reset				0	0	1	0	0					0	1	1	0

Bit(s)	Name	Description
23:16	ANR_C_L_DIFF_TH	**Luma difference threshold for chroma bilateral filter [Q0.8.0]**
12:8	ANR_PTC_GAIN_TH	**Range filter PTC gain lower bound** Range 0~16
3:0	ANR_PTC_VGAIN	**Gain for vertical chroma bilateral filter's range filter. [Q0.2.2]** Range 0~15

15004A48 **CAM_ANR_PTC** **ANR Chroma Range Filter LUT Register** **06040302**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ANR_PTC4								ANR_PTC3							
Type	RW								RW							
Reset	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ANR_PTC2								ANR_PTC1							
Type	RW								RW							
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0

Bit(s)	Name	Description
31:24	ANR_PTC4	**Chroma bilateral filter's range filter step 4. [Q0.8.0]**
23:16	ANR_PTC3	**Chroma bilateral filter's range filter step 3. [Q0.8.0]**
15:8	ANR_PTC2	**Chroma bilateral filter's range filter step 2. [Q0.8.0]**
7:0	ANR_PTC1	**Chroma bilateral filter's range filter step 1. [Q0.8.0].** Rule: ANR_PTY1<= ANR_PTY2<= ANR_PTY3<= ANR_PTY3

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15004A4C **CAM_ANR_LCE1** **ANR LEC Gain Register 1** **00000026**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										ANR_LCE_SCALE_GAIN			ANR_LCE_C_GAIN			
Type										RW			RW			
Reset										0	1	0	0	1	1	0

Bit(s)	Name	Description
6:4	ANR_LCE_SCALE_GAIN	**The scale could be changed by LCE slope information, and ANR_LCE_SCALE_GAIN can adjust the degree of change**
3:0	ANR_LCE_C_GAIN	**Additional chroma gain when LCE link is enabled. [Q0.2.2]** Valid range: 4~15

15004A50 **CAM_ANR_LCE2** **ANR LEC Gain Register 2** **100C0A08**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			ANR_LCE_GAIN3								ANR_LCE_GAIN2					
Type			RW								RW					
Reset			0	1	0	0	0	0			0	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ANR_LCE_GAIN1								ANR_LCE_GAIN0					
Type			RW								RW					
Reset			0	0	1	0	1	0			0	0	1	0	0	0

Bit(s)	Name	Description
29:24	ANR_LCE_GAIN3	**Range filter gain mapped from LCE slope information that is equal to 3 [Q0.3.3]** Valid range: 8~63
21:16	ANR_LCE_GAIN2	**Range filter gain mapped from LCE slope information that is equal to 2 [Q0.3.3]** Valid range: 8~63
13:8	ANR_LCE_GAIN1	**Range filter gain mapped from LCE slope information that is equal to 1 [Q0.3.3]** Valid range: 8~63
5:0	ANR_LCE_GAIN0	**Range filter gain mapped from LCE slope information that is equal to 0 [Q0.3.3]** Valid range: 8~63

15004A54 **CAM_ANR_HP1** **ANR HP Register 1** **B9192C78**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ANR_HP_E				ANR_HP_D							ANR_HP_C				
Type	RW				RW							RW				

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Reset	1	0	1	1	1	0	0	1				1	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**ANR_HP_B**						**ANR_HP_A**							
Type			RW						RW							
Reset			1	0	1	1	0	0	0	1	1	1	1	0	0	0

Bit(s)	Name	Description
31:28	ANR_HP_E	**Coefficient for 5x5 USM** Valid range: -8~7
27:24	ANR_HP_D	**Coefficient for 5x5 USM** Valid range: -8~7
20:16	ANR_HP_C	**Coefficient for 5x5 USM** Valid range: -16~15
13:8	ANR_HP_B	**Coefficient for 5x5 USM** Valid range: -32~31
7:0	ANR_HP_A	**Coefficient for 5x5 USM** Valid range: 0~255

15004A58 **CAM_ANR_HP2** **ANR HP Register 2** **00060A32**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														**ANR_HP_F**		
Type														RW		
Reset														1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**ANR_HP_X1**							**ANR_HP_S2**				**ANR_HP_S1**			
Type		RW							RW				RW			
Reset		0	0	0	1	0	1	0	0	0	1	1	0	0	1	0

Bit(s)	Name	Description
18:16	ANR_HP_F	**Coefficient for 5x5 USM** Valid range: -4~3
14:8	ANR_HP_X1	**USM LUT X1** Valid range: 0~127
7:4	ANR_HP_S2	**USM LUT S2** Valid range: 0~15
3:0	ANR_HP_S1	**USM LUT S1** Valid range: 0~15

15004A5C **CAM_ANR_HP3** **ANR HP Register 3** **80780678**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**ANR_HP_CLIP**								**ANR_HP_Y_LO**							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**ANR_HP_Y_SP**						**ANR_HP_Y_GAIN_CLIP**						
Type				RW						RW						
Reset				0	0	1	1	0		1	1	1	1	0	0	0

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Bit(s)	Name	Description
31:24	ANR_HP_CLIP	**Total clipping for USM** Valid range: 0~255
23:16	ANR_HP_Y_LO	**Luma LUT for USM** Valid range: 0~255
12:8	ANR_HP_Y_SP	**Luma LUT slope for USM** Valid range: 0~31
6:0	ANR_HP_Y_GAIN_CLIP	**Luma LUT clip for USM** Valid range: 0~127

15004A60 CAM_ANR_ACTY ANR Activity Luma Register 30081000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		ANR_ACT_BLD_TH_Y										ANR_ACT_SLANT_Y				
Type		RW										RW				
Reset		0	1	1	0	0	0	0				0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		ANR_ACT_BLD_BASE_Y							ANR_ACT_TH_Y							
Type		RW							RW							
Reset		0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	ANR_ACT_BLD_TH_Y	**Luma LUT for activity blending** Valid range: 0~64
20:16	ANR_ACT_SLANT_Y	**Luma LUT for activity blending** Valid range: 0~63
14:8	ANR_ACT_BLD_BASE_Y	**Luma LUT for activity blending** Valid range: 0~64
7:0	ANR_ACT_TH_Y	**Luma LUT for activity blending** Valid range: 0~255

15004A64 CAM_ANR_ACTC ANR Activity Chroma Register 30081000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		ANR_ACT_BLD_TH_C										ANR_ACT_SLANT_C				
Type		RW										RW				
Reset		0	1	1	0	0	0	0				0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		ANR_ACT_BLD_BASE_C							ANR_ACT_TH_C							
Type		RW							RW							
Reset		0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	ANR_ACT_BLD_TH_C	**Chroma LUT for activity blending** Valid range: 0~64
20:16	ANR_ACT_SLANT_C	**Chroma LUT for activity blending** Valid range: 0~63
14:8	ANR_ACT_BLD_B	**Chroma LUT for activity blending**

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Bit(s)	Name	Description
	ASE_C	Valid range: 0~64
7:0	ANR_ACT_TH_C	**Chroma LUT for activity blending** Valid range: 0~255

15004A68 **CAM_ANR_RSV1** **ANR_RSV1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RSV1[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RSV1[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RSV1	Reserved 1

15004A6C **CAM_ANR_RSV2** **ANR_RSV2** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RSV2[31:16]**															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RSV2[15:0]**															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	RSV2	Reserved 2

15004A80 **CAM_CCR_CON** **Chroma Choring Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CCR_Y_CPX3**									**CCR_UV_GAIN2**						
Type	RW									RW						
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**CCR_UV_GAIN_MODE**			**CCR_OR_MODE**					**CCR_EN**
Type								RW			RW					RW
Reset								0			0					0

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Bit(s)	Name	Description
31:24	CCR_Y_CPX3	**Gain LUT by luma, x control point 3 [Q0.8.0]** CCR_Y_CPX1 <= CCR_Y_CPX2 <= CCR_Y_CPX3
22:16	CCR_UV_GAIN2	**Gain LUT by UV, y control point 2 [Q0.1.6]** Valid range: 0~64
8	CCR_UV_GAIN_MODE	**Controls keeping UV gain when saturation is up**
5	CCR_OR_MODE	**Y/UV gain fusion mode** 0: Simple gain fusion 1: Complex gain fusion
0	CCR_EN	**Double buffer** Enables CCR

15004A84 **CAM_CCR_Y_LUT** **Chroma Choring Luma LUT Register** **10137828**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CCR_Y_CPY1								CCR_Y_SP1						
Type		RW								RW						
Reset		0	0	1	0	0	0	0		0	0	1	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CCR_Y_CPX2								CCR_Y_CPX1							
Type	RW								RW							
Reset	0	1	1	1	1	0	0	0	0	0	1	0	1	0	0	0

Bit(s)	Name	Description
30:24	CCR_Y_CPY1	**Gain LUT by luma, y control point 1 [Q0.1.6]** Valid range: 0 ~ 64
22:16	CCR_Y_SP1	**Gain LUT by luma, slope 1 [Q0.2.5]** CCR_Y_CPY1 + [CCR_Y_SP1*(CCR_Y_CPX2-CCR_Y_CPX1)]/32 < 1,024
15:8	CCR_Y_CPX2	**Gain LUT by luma, x control point 2 [Q0.8.0]**
7:0	CCR_Y_CPX1	**Gain LUT by luma, x control point 1 [Q0.8.0]** CCR_Y_CPX1 <= CCR_Y_CPX2 <= CCR_Y_CPX3

15004A88 **CAM_CCR_UVLUT** **Chroma Choring Chroma LUT Register** **40303004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CCR_UV_GAIN1							CCR_UV_X3							
Type		RW							RW							
Reset		1	0	0	0	0	0	0	0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CCR_UV_X2								CCR_UV_X1							
Type	RW								RW							
Reset	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
30:24	CCR_UV_GAIN1	**Gain LUT by UV, y control point 1 [Q0.1.6]** Valid range: 0 ~ 64
23:16	CCR_UV_X3	**Gain LUT by UV, x control point 3 [Q0.8.0]**

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Bit(s)	Name	Description
15:8	CCR_UV_X2	**Gain LUT by UV, x control point 2 [Q0.8.0]** CCR_UV_X2 <= CCR_UV_X3
7:0	CCR_UV_X1	**Gain LUT by UV, x control point 1 [Q0.8.0]** CCR_UV_X1 <= CCR_UV_X2

15004A8C CAM_CCR_Y_LUT2 Chroma Choring Luma LUT 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CCR_Y_CPY2								CCR_Y_CPY0						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CCR_Y_SP2								CCR_Y_SP0						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	CCR_Y_CPY2	**Gain LUT by luma, y control point 0 [Q01.6]** Valid range: 0 ~ 64
22:16	CCR_Y_CPY0	**Gain LUT by luma, y control point 2 [Q0.1.6]** Valid range: 0 ~ 64
14:8	CCR_Y_SP2	**Gain LUT by luma, slope 2 [Q0.2.5]**
6:0	CCR_Y_SP0	**Gain LUT by luma, slope 0 [Q0.2.5]** CCR_Y_CPY0 + (CCR_Y_SP0*CCR_Y_CPX1)/32 < 1,024

15004A90 CAM_CCR_SAT_CTRL Chroma Choring Saturation Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															CCR_CEN_V[5:4]	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CCR_CEN_V[3:0]						CCR_CEN_U									CCR_MODE
Type	RW						RW									RW
Reset	0	0	0	0			0	0	0	0	0	0				0

Bit(s)	Name	Description
17:12	CCR_CEN_V	**V center of saturation magnitude computation [Q1.6.0].**
9:4	CCR_CEN_U	**U center of saturation magnitude computation [Q1.6.0].**
0	CCR_MODE	**Saturation magnitude computation mode.** 0: |cr-CCR_CEN_U|+|cb-CCR_CEN_V| 1: MAX(|cr-CCR_CEN_U|,|cb-CCR_CEN_V|)*2

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15004A94 CAM_CCR_UVLUT_SP Chroma Choring Chroma LUT Slope Register 00000027

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							CCR_UV_GAIN_SP2									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							CCR_UV_GAIN_SP1									
Type							RW									
Reset							0	0	0	0	1	0	0	1	1	1

Bit(s)	Name	Description
25:16	CCR_UV_GAIN_SP2	Gain LUT by uv, slope 2 [Q0.5.5]
9:0	CCR_UV_GAIN_SP1	Gain LUT by uv, slope 1 [Q0.5.5]

15004AA0 CAM_SEEE_SRK_CTRL Shrinkage Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESERVED															
Type	RW															
Reset	0	0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

15004AA4 CAM_SEEE_CLIP_CTRL Clip Control 00400635

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									SEEE_RESP_CLIP							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEEE_DOT_TH								SEEE_DOT_WF			SEEE_DOT_REDUC_EN	SEEE_OVRSH_CLIP_STR			SEEE_OVRSH_CLIP_EN
Type	RW								RW			RW	RW			RW
Reset	0	0	0	0	0	1	1	0	0	0	1	1	0	1	0	1

Bit(s)	Name	Description
23:16	SEEE_RESP_CLIP	**Clips the response**
15:8	SEEE_DOT_TH	**A dot is decided if its value is bigger or smaller than all values of neighboring pixels by SEEE_DOT_TH.**
7:5	SEEE_DOT_WF	**If a single dot is detected, its corresponding response will be**

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Bit(s)	Name	Description
		reduced to Response*2^(-SEEE_DOT_WF-1)
4	SEEE_DOT_REDUC_EN	**Enables dot response reduction**
3:1	SEEE_OVRSH_CLIP_STR	**Overshoot/undershoot clip strength**
0	SEEE_OVRSH_CLIP_EN	**Overshoot/undershoot clipping enabling/disabling bit** 0: Disable 1: Enable

15004AA8 **CAM_SEEE_FLT_CTRL_1** **Filter Control 1** **00000426**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						SEEE_FLT_AMP			SEEE_FLT_TH							
Type						RW			RW							
Reset						1	0	0	0	0	1	0	0	1	1	0

Bit(s)	Name	Description
10:8	SEEE_FLT_AMP	Right-shift bit number for filter output: (9-SEEE_FLT_AMP)
7:0	SEEE_FLT_TH	Filter output coring level

15004AAC **CAM_SEEE_FLT_CTRL_2** **Filter Control 2** **35CE7C78**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SEEE_FLT_G6			SEEE_FLT_G5				SEEE_FLT_G4				SEEE_FLT_G3[4:2]		
Type			RW			RW				RW				RW		
Reset			1	1	0	1	0	1	1	1	0	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEEE_FLT_G3[1:0]		SEEE_FLT_G2						SEEE_FLT_G1							
Type	RW		RW						RW							
Reset	0	1	1	1	1	1	0	0	0	1	1	1	1	0	0	0

Bit(s)	Name	Description
29:27	SEEE_FLT_G6	Filter coefficient: [-4, 3]
26:23	SEEE_FLT_G5	Filter coefficient: [-8, 7]
22:19	SEEE_FLT_G4	Filter coefficient: [-8, 7]
18:14	SEEE_FLT_G3	Filter coefficient: [-16, 15]
13:8	SEEE_FLT_G2	Filter coefficient: [-32, 31]
7:0	SEEE_FLT_G1	Filter coefficient: [0, 255]

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15004AB0 CAM_SEEE_GLUT_CTRL_01 Edge Detection Filter Control 01 00140123

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SEEE_GLUT_Y1									
Type							RW									
Reset							0	0	0	0	0	1	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEEE_GLUT_S1								SEEE_GLUT_X1							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1

Bit(s)	Name	Description
25:16	SEEE_GLUT_Y1	**Gain LUT y value of control point 1 (Q0.10.0)**
15:8	SEEE_GLUT_S1	**Slope of segment 1 in gain LUT** (-128 <= SEEE_GLUT_Si <=127, Q1.7.0)
7:0	SEEE_GLUT_X1	**Gain LUT x value of control point 1** (SEEE_GLUT_X(i+1) - SEEE_GLUT_Xi >= 8, SEEE_GLUT_X1 >= 0, Q0.8.0)

15004AB4 CAM_SEEE_GLUT_CTRL_02 Edge Detection Filter Control 02 0266183C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SEEE_GLUT_Y2									
Type							RW									
Reset							1	0	0	1	1	0	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEEE_GLUT_S2								SEEE_GLUT_X2							
Type	RW								RW							
Reset	0	0	0	1	1	0	0	0	0	0	1	1	1	1	0	0

Bit(s)	Name	Description
25:16	SEEE_GLUT_Y2	Gain LUT y value of control point 2 (Q0.10.0)
15:8	SEEE_GLUT_S2	Slope of segment 2 in gain LUT (Q1.7.0)
7:0	SEEE_GLUT_X2	Gain LUT x value of control point 2 (Q0.8.0)

15004AB8 CAM_SEEE_GLUT_CTRL_03 Edge Detection Filter Control 03 0133F864

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SEEE_GLUT_Y3									
Type							RW									
Reset							0	1	0	0	1	1	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEEE_GLUT_S3								SEEE_GLUT_X3							
Type	RW								RW							
Reset	1	1	1	1	1	0	0	0	0	1	1	0	0	1	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
25:16	SEEE_GLUT_Y3	Gain LUT y value of control point 3 (Q0.10.0)
15:8	SEEE_GLUT_S3	Slope of segment 3 in gain LUT (Q1.7.0)
7:0	SEEE_GLUT_X3	Gain LUT x value of control point 3 (Q0.8.0)

15004ABC CAM_SEEE_GLUT_CTRL_04 Edge Detection Filter Control 04 0029FEDC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SEEE_GLUT_Y4									
Type							RW									
Reset							0	0	0	0	1	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEEE_GLUT_S4								SEEE_GLUT_X4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0

Bit(s)	Name	Description
25:16	SEEE_GLUT_Y4	**Gain LUT y value of control point 4 (Q0.10.0)**
15:8	SEEE_GLUT_S4	**Slope of segment 4 in gain LUT (Q1.7.0)**
7:0	SEEE_GLUT_X4	**Gain LUT x value of control point 4** (SEEE_GLUT_X4 <= (255 - 8) = 247, Q0.8.0)

15004AC0 CAM_SEEE_GLUT_CTRL_05 Edge Detection Filter Control 05 0000FF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEEE_GLUT_S5															
Type	RW															
Reset	1	1	1	1	1	1	1	1								

Bit(s)	Name	Description
15:8	SEEE_GLUT_S5	Slope of segment 5 in gain LUT (Q1.7.0)

15004AC4 CAM_SEEE_GLUT_CTRL_06 Edge Detection Filter Control 06 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									SEEE_GLUT_TH_MIN							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEEE_GLUT_TH_UND								SEEE_GLUT_TH_OVR							
Type	RW								RW							

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Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
23:16	SEEE_GLUT_TH_MIN	Minimum gain
15:8	SEEE_GLUT_TH_UND	Lower bound of gain if gain is negative
7:0	SEEE_GLUT_TH_OVR	Upper bound of gain if gain is positive

15004AC8 CAM_SEEE_EDTR_CTRL Edge Detection Control 00000643

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name		SEEE_EDTR_FLT_2_EN	SEEE_EDTR_FLT_MODE		SEEE_EDTR_LV			SEEE_EDTR_AMP						SEEE_EDTR_DIAG_AMP		
Type		RW	RW		RW			RW						RW		
Reset		0	0	0	0	1	1	0	0	1	0	0	0	0	1	1

Bit(s)	Name	Description
14	SEEE_EDTR_FLT_2_EN	**Enables edge detection filter with stable funcion**
13:12	SEEE_EDTR_FLT_MODE	0: Use 1st filter and 2nd filter result in edge detector 1: Use 1st filter result in edge detector 2: Use 2nd filter result in edge detector
11:9	SEEE_EDTR_LV	**Edge detection blending level: [0,4]**
8:3	SEEE_EDTR_AMP	**Edge detection maximum gain: [0, 32]**
2:0	SEEE_EDTR_DIAG_AMP	**Edge detecion diagonal gain** Its real value is (SEEE_EDTR_DIAG_AMP/4).

15004ACC CAM_SEEE_OUT_EDGE_CTRL Target of Edge Enhancement 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name															SEEE_OUT_EDGE_SEL	
Type															RW	
Reset															0	0

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Bit(s)	Name	Description
1:0	SEEE_OUT_EDGE_SEL	**Selects output** 0: No EE/SE 1: From EE 2. From SE

15004AD0 **CAM_SEEE_SE_Y_CTRL** **Special Effect Y Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										**SEEE_SE_COUT_QBIT**				**SEEE_SE_YOUT_QBIT**		
Type										RW				RW		
Reset										0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**SEEE_SE_CONST_Y_VAL**								**SEEE_SE_CONST_Y_EN**
Type								RW								RW
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
22:20	SEEE_SE_COUT_QBIT	**Number of lower bits are discarded in 8-bit Cb/Cr channel**
18:16	SEEE_SE_YOUT_QBIT	**Number of lower bits are discarded in 8-bit Y channel**
8:1	SEEE_SE_CONST_Y_VAL	**Constant value to replace original Y**
0	SEEE_SE_CONST_Y_EN	**Replaces Y with one constant value** 0: No replacement 1: Replace with a pre-defined constant

15004AD4 **CAM_SEEE_SE_EDGE_CTRL_1** **Special Effect Edge Control 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**SEEE_SE_VERT_EDGE_GAIN_C**					**SEEE_SE_VERT_EDGE_GAIN_B**					**SEEE_SE_VERT_EDGE_GAIN_A**				**SEEE_SE_VERT_EDGE_SEL**
Type		RW					RW					RW				RW
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**SEEE_SE_HORI_EDGE_GAIN_C**					**SEEE_SE_HORI_EDGE_GAIN_B**					**SEEE_SE_HORI_EDGE_GAIN_A**				**SEEE_SE_HORI_EDGE_SEL**

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Type		RW					RW					RW				RW
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	SEEE_SE_VERT_EDGE_GAIN_C	**Vertical gain for non-horizontal-step and non-central pixels in a vertical step-edge**
25:21	SEEE_SE_VERT_EDGE_GAIN_B	**General vertical gain**
20:17	SEEE_SE_VERT_EDGE_GAIN_A	**Vertical gain for central pixel in a step-edge transition**
16	SEEE_SE_VERT_EDGE_SEL	**Selects vertical edge** 0: Line edge 1: Point edge
14:10	SEEE_SE_HORI_EDGE_GAIN_C	**Horizontal gain for non-vertical-step and non-central pixels in a horizontal step-edge**
9:5	SEEE_SE_HORI_EDGE_GAIN_B	**General horizontal gain**
4:1	SEEE_SE_HORI_EDGE_GAIN_A	**Horizontal gain for central pixel in a step-edge transition**
0	SEEE_SE_HORI_EDGE_SEL	**Selects horizontal edge** 0: Line edge 1: Point edge

15004AD8	CAM_SEEE_SE_EDGE_CTRL_2	Special Effect Edge Control 2	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name										SEEE_SE_BOSS_GAIN_OFF	SEEE_SE_BOSS_IN_SEL	SEEE_SE_EDGE_DET_GAIN				
Type										RW	RW	RW				
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	SEEE_SE_BOSS_GAIN_OFF	**Edge boosting by multiplying one edge with a gain based on the step edge** 0: No boosting 1: Boosting
5	SEEE_SE_BOSS_IN_SEL	**Selects step edges or line/point edges** 0: Line/point edges 1: Step edges
4:0	SEEE_SE_EDGE_DET_GAIN	**Gain control before detecting the central pixel in a step edge**

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15004ADC **CAM_SEEE_SE_EDGE_CTRL_3** **Special Effect Edge Control 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															SEEE_SE_OIL_EN	SEEE_SE_CONVT_SLOPE_SEL
Type															RW	RW
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEEE_SE_CONVT_E_TH								SEEE_SE_CONVT_CORE_TH							SEEE_SE_CONVT_FORCE_EN
Type	RW								RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	SEEE_SE_OIL_EN	**Enables oil data generation** 0: Disable 1: Enable
16	SEEE_SE_CONVT_SLOPE_SEL	**Selects kneel slope in EdgeHVc_gen** 0: 1/2 1: 1/4
15:8	SEEE_SE_CONVT_E_TH	**Knee point in EdgeHVc_gen**
7:1	SEEE_SE_CONVT_CORE_TH	**Coring level in EdgeHVc_gen**
0	SEEE_SE_CONVT_FORCE_EN	**Forces EdgeHVc_gen block to work in all circumstances** 0: No effect 1: EdgeHVc_gen always works

15004AE0 **CAM_SEEE_SE_SPECL_CTRL** **Special Effect Special Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SEEE_SE_KNEE_SEL		SEEE_SE_SPECL_GAIN		SEEE_SE_SPECL_INV	SEEE_SE_SPECL_ABS	SEEE_SE_SPECL_HALF_MODE	
Type									RW		RW		RW	RW	RW	
Reset									0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
7:6	SEEE_SE_KNEE_SEL	**Selects final clip level** 0: 31 1: 48 2: 63 3: 127
5:4	SEEE_SE_SPECL_GAIN	**Controls final gain for SE** 0: 1x 1: 2x 2: 4x 3: 8x
3	SEEE_SE_SPECL_INV	**Sign inversion for all edges** 0: No effects 1: Sign inversion
2	SEEE_SE_SPECL_ABS	**Generates absolute values for all edges** 0: No effect 1: Absolute values of edges are generated.
1:0	SEEE_SE_SPECL_HALF_MODE	**Polarity control** 0: Nothing 1: Only positive edges are allowed. 2: Only negative edges are allowed.

15004AE4 **CAM_SEEE_SE_CORE_CTRL_1** **Special Effect Core Control 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								SEEE_SE_CORE_HORI_Y5						SEEE_SE_CORE_HORI_SDN		SEEE_SE_CORE_HORI_X2[7:7]
Type								RW						RW		RW
Reset								0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SEEE_SE_CORE_HORI_X2[6:0]							SEEE_SE_CORE_HORI_SUP		SEEE_SE_CORE_HORI_X0						
Type	RW							RW		RW						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:19	SEEE_SE_CORE_HORI_Y5	**Horizontal output level for the 5th section in Core LUT**
18:17	SEEE_SE_CORE_HORI_SDN	**Horizontal slope control for the 4th section in Core LUT**
16:9	SEEE_SE_CORE_HORI_X2	**Horizontal input clip threshold in Core LUT**
8:7	SEEE_SE_CORE_HORI_SUP	**Controls horizontal slope for the 2nd section in Core LUT** 0: 8 1: 16 2: 32

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Bit(s)	Name	Description
		3: 64
6:0	SEEE_SE_CORE_HORI_X0	**Horizontal coring level in Core LUT**

15004AE8 **CAM_SEEE_SE_CORE_CTRL_2** **Special Effect Core Control 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								SEEE_SE_CORE_VERT_Y5						SEEE_SE_CORE_VERT_SDN		SEEE_SE_CORE_VERT_X2[7:7]
Type								RW						RW		RW
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEEE_SE_CORE_VERT_X2[6:0]							SEEE_SE_CORE_VERT_SUP		SEEE_SE_CORE_VERT_X0						
Type	RW							RW		RW						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:19	SEEE_SE_CORE_VERT_Y5	**Vertical output level for the 5th section in Core LUT**
18:17	SEEE_SE_CORE_VERT_SDN	**Vertical slope control for the 4th section in Core LUT**
16:9	SEEE_SE_CORE_VERT_X2	**Vertical input clip threshold in Core LUT**
8:7	SEEE_SE_CORE_VERT_SUP	**Controls vertical slope for the 2nd section in Core LUT** 0: 8 1: 16 2: 32 3: 64
6:0	SEEE_SE_CORE_VERT_X0	**Vertical coring level in Core LUT**

15004AEC **CAM_SEEE_GLUT_CTRL_07** **Edge Detection Filter Control 07** **00180123**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								SEEE_GLUT_LLINK_EN	SEEE_GLUT_S2_1							
Type								RW	RW							
Reset								0	0	0	0	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	SEEE_GLUT_S1_1								SEEE_GLUT_X1_1							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1

Bit(s)	Name	Description
24	SEEE_GLUT_LLINK_EN	**Gain LUT enabling/disabling bit** 0: Disable 1: Enable
23:16	SEEE_GLUT_S2_1	**Slope of segment 2 in gain LUT when pixel's link value is 1**
15:8	SEEE_GLUT_S1_1	**Slope of segment 1 in gain LUT when pixel's link value is 1**
7:0	SEEE_GLUT_X1_1	**Gain LUT x value of control point 1 when pixel's link value is 1**

15004AF0 **CAM_SEEE_GLUT_CTRL_08** **Edge Detection Filter Control 08** **00180123**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									SEEE_GLUT_S2_2							
Type									RW							
Reset									0	0	0	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEEE_GLUT_S1_2								SEEE_GLUT_X1_2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1

Bit(s)	Name	Description
23:16	SEEE_GLUT_S2_2	Slope of segment 2 in gain LUT when pixel's link value is 2
15:8	SEEE_GLUT_S1_2	Slope of segment 1 in gain LUT when pixel's link value is 2
7:0	SEEE_GLUT_X1_2	Gain LUT x value of control point 1 when pixel's link value is 2

15004AF4 **CAM_SEEE_GLUT_CTRL_09** **Edge Detection Filter Control 09** **00180123**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									SEEE_GLUT_S2_3							
Type									RW							
Reset									0	0	0	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEEE_GLUT_S1_3								SEEE_GLUT_X1_3							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1

Bit(s)	Name	Description
23:16	SEEE_GLUT_S2_3	Slope of segment 2 in gain LUT when pixel's link value is 3
15:8	SEEE_GLUT_S1_3	Slope of segment 1 in gain LUT when pixel's link value is 3
7:0	SEEE_GLUT_X1_3	Gain LUT x value of control point 1 when pixel's link value is 3

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15004AF8 **CAM_SEEE_GLUT_CTRL_10** **Edge Detection Filter Control 10** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEEE_GLUT_TH_UND_2								SEEE_GLUT_TH_OVR_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEEE_GLUT_TH_UND_1								SEEE_GLUT_TH_OVR_1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	SEEE_GLUT_TH_UND_2	Lower bound of gain if gain is negative and pixel's link value is 2
23:16	SEEE_GLUT_TH_OVR_2	Upper bound of gain if gain is positive and pixel's link value is 2
15:8	SEEE_GLUT_TH_UND_1	Lower bound of gain if gain is negative and pixel's link value is 1
7:0	SEEE_GLUT_TH_OVR_1	Upper bound of gain if gain is positive and pixel's link value is 1

15004AFC **CAM_SEEE_GLUT_CTRL_11** **Edge Detection Filter Control 11** **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEEE_GLUT_TH_UND_3								SEEE_GLUT_TH_OVR_3							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:8	SEEE_GLUT_TH_UND_3	Lower bound of gain if gain is negative and pixel's link value is 3
7:0	SEEE_GLUT_TH_OVR_3	Upper bound of gain if gain is positive and pixel's link value is 3

15004B00 **CAM_CRZ_CONTROL** **CRZ Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							CRZ_VERT_TBL_SEL					CRZ_HORI_TBL_SEL				
Type							USER0					USER0				
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRZ_TRNC_VERT			CRZ_TRNC_HORI			CRZ_DER_EN	CRZ_VERT_ALGO		CRZ_HORI_ALGO		CRZ_VERT_FIRST			CRZ_VERT_EN	CRZ_HORI_EN

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Type	USERo			USERo			US ERo	USERo		USERo		US ERo			US ERo	USE Ro
Reset	0	0	0	0	0	0	0	0	0	0	0	0			0	0

Bit(s)	Name	Description
25:21	CRZ_VERT_TBL_SEL	**Double buffer** Selects vertical scaling coefficient table 4 tap: [20:25] (1x up ~ 1/2x down) Cubic accumulation: [0:19] (blur ~ sharp)
20:16	CRZ_HORI_TBL_SEL	**Double buffer** Selects horizontal scaling coefficient table 4 tap: [20:25] (1x up ~ 1/2x down) Cubic accumulation: [0:19] (blur ~ sharp)
15:13	CRZ_TRNC_VERT	**Double buffer** Cubic accumulation parameter. Truncate weighting bit for high ratio downsample
12:10	CRZ_TRNC_HORI	**Double buffer** Cubic accumulation parameter. Truncate weighting bit for high ratio downsample
9	CRZ_DER_EN	**Double buffer** Ring suppression enable (only for 4 tap)
8:7	CRZ_VERT_ALGO	**Double buffer** Vertical scaling algorithm 0: 4 tap 1: n tap source accumulation 2: 4n tap cubic accumulation 3: Reserved
6:5	CRZ_HORI_ALGO	**Double buffer** Horizontal scaling algorithm 0: 4 tap 1: n tap source accumulation 2: 4n tap cubic accumulation 3: Reserved
4	CRZ_VERT_FIRST	**Double buffer** 0: Horiznotal first then vertical scaling 1: Vertical first then horizontal scaling
1	CRZ_VERT_EN	**Double buffer** Enables vertical scaling function
0	CRZ_HORI_EN	**Double buffer** Enables horizontal scaling function

15004B04 **CAM_CRZ_IN_IMG** **CRZ IN IMG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				CRZ_IN_HT												
Type				USERo												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CRZ_IN_WD												
Type				USERo												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
28:16	CRZ_IN_HT	**Double buffer** Imput Image height
12:0	CRZ_IN_WD	**Double buffer** Input Image width

15004B08 **CAM_CRZ_OUT_IMG** **CRZ OUT IMG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				CRZ_OUT_HT												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CRZ_OUT_WD												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	CRZ_OUT_HT	**Double buffer** Output Image height
12:0	CRZ_OUT_WD	**Double buffer** Output Image width

15004B0C **CAM_CRZ_HORI_STEP** **CRZ_HORI_STEP** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										CRZ_HORI_STEP[22:16]						
Type										USER0						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRZ_HORI_STEP[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
22:0	CRZ_HORI_STEP	**Double buffer** Horiznotal scaling ratio

15004B10 **CAM_CRZ_VERT_STEP** **CRZ_VERT_STEP** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										CRZ_VERT_STEP[22:16]						
Type										USER0						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRZ_VERT_STEP[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
22:0	CRZ_VERT_STEP	**Double buffer** Vertical scaling ratio

15004B14 **CAM_CRZ_LUMA_HORI_INT_OFST** **CRZ_LUMA_HORI_INT_OFST** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**CRZ_LUMA_HORI_INT_OFST**												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	CRZ_LUMA_HORI_INT_OFST	**Double buffer** Horizontal Luma integer offset

15004B18 **CAM_CRZ_LUMA_HORI_SUB_OFST** **CRZ_LUMA_HORI_SUB_OFST** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												**CRZ_LUMA_HORI_SUB_OFST[20:16]**				
Type												USER0				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CRZ_LUMA_HORI_SUB_OFST[15:0]**															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	CRZ_LUMA_HORI_SUB_OFST	**Double buffer** Horizontal Luma sub-pixel offset

15004B1C **CAM_CRZ_LUMA_VERT_INT_OFST** **CRZ_LUMA_VERT_INT_OFST** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**CRZ_LUMA_VERT_INT_OFST**												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
12:0	CRZ_LUMA_VERT_INT_OFST	**Double buffer** Vertical Luma integer offset

15004B20 **CAM_CRZ_LUMA_VERT_SUB_OFST** **CRZ_LUMA_VERT_SUB_OFST** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												CRZ_LUMA_VERT_SUB_OFST[20:16]				
Type												USER0				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRZ_LUMA_VERT_SUB_OFST[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	CRZ_LUMA_VERT_SUB_OFST	**Double buffer** Vertical Luma sub-pixel offset

15004B24 **CAM_CRZ_CHRO_HORI_INT_OFST** **CRZ_CHRO_HORI_INT_OFST** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CRZ_CHRO_HORI_INT_OFST												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	CRZ_CHRO_HORI_INT_OFST	**Double buffer** Horizontal Chroma integer offset

15004B28 **CAM_CRZ_CHRO_HORI_SUB_OFST** **CRZ_CHRO_HORI_SUB_OFST** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												CRZ_CHRO_HORI_SUB_OFST[20:16]				
Type												USER0				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRZ_CHRO_HORI_SUB_OFST[15:0]															
Type	USER0															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	CRZ_CHRO_HORI_SUB_OFST	**Double buffer** Horizontal Chroma sub-pixel offset

15004B2C **CAM_CRZ_CHRO_VERT_INT_OFST** **CRZ_CHRO_VERT_INT_OFST** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CRZ_CHRO_VERT_INT_OFST												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	CRZ_CHRO_VERT_INT_OFST	**Double buffer** Vertical Chroma integer offset

15004B30 **CAM_CRZ_CHRO_VERT_SUB_OFST** **CRZ_CHRO_VERT_SUB_OFST** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												CRZ_CHRO_VERT_SUB_OFST[20:16]				
Type												USER0				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRZ_CHRO_VERT_SUB_OFST[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	CRZ_CHRO_VERT_SUB_OFST	**Double buffer** Vertical Chroma sub-pixel offset

15004B34 **CAM_CRZ_DER_1** **CRZ_DER_1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													CRZ_SPARE_1H			
Type													USER0			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CRZ_SPARE_1V			
Type													USER0			
Reset													0	0	0	0

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Bit(s)	Name	Description
19:16	CRZ_SPARE_1H	Spare register
3:0	CRZ_SPARE_1V	Spare register

15004B38 **CAM_CRZ_DER_2** **CRZ_DER_2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								CRZ_SPARE_2H								
Type								USER0								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								CRZ_SPARE_2V								
Type								USER0								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	CRZ_SPARE_2H	Spare register
8:0	CRZ_SPARE_2V	Spare register

15004BA0 **CAM_G2C_CONV_0A** **RGB/YUV to YUV Matrix Coefficient Row 0 (Part A)** **012D0099**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						G2C_CNV_01										
Type						RW										
Reset						0	0	1	0	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						G2C_CNV_00										
Type						RW										
Reset						0	0	0	1	0	0	1	1	0	0	1

Bit(s)	Name	Description
26:16	G2C_CNV_01	DIP RGB 2 YUV Matrix 0,1 coefficient in Q1.1.9
10:0	G2C_CNV_00	DIP RGB 2 YUV Matrix 0,0 coefficient in Q1.1.9

15004BA4 **CAM_G2C_CONV_0B** **RGB/YUV to YUV Matrix Coefficient Row 0 (Part B)** **0000003A**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						G2C_Y_OFST										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						G2C_CNV_02										
Type						RW										
Reset						0	0	0	0	0	1	1	1	0	1	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
26:16	G2C_Y_OFST	Y offset. Q1.10.0
10:0	G2C_CNV_02	DIP RGB 2 YUV Matrix 0,2 coefficient in Q1.1.9

15004BA8 CAM_G2C_CONV_1A RGB/YUV to YUV Matrix Coefficient Row 1 (Part A) 075607AA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						G2C_CNV_11										
Type						RW										
Reset						1	1	1	0	1	0	1	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						G2C_CNV_10										
Type						RW										
Reset						1	1	1	1	0	1	0	1	0	1	0

Bit(s)	Name	Description
26:16	G2C_CNV_11	DIP RGB 2 YUV Matrix 1,1 coefficient in Q1.1.9
10:0	G2C_CNV_10	DIP RGB 2 YUV Matrix 1,0 coefficient in Q1.1.9

15004BAC CAM_G2C_CONV_1B RGB/YUV to YUV Matrix Coefficient Row 1 (Part B) 00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							G2C_U_OFST									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						G2C_CNV_12										
Type						RW										
Reset						0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	G2C_U_OFST	U offset. Q1.9.0
10:0	G2C_CNV_12	DIP RGB 2 YUV Matrix 1,2 coefficient in Q1.1.9

15004BB0 CAM_G2C_CONV_2A RGB/YUV to YUV Matrix Coefficient Row 2 (Part A) 072A0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						G2C_CNV_21										
Type						RW										
Reset						1	1	1	0	0	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						G2C_CNV_20										
Type						RW										
Reset						0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:16	G2C_CNV_21	DIP RGB 2 YUV Matrix 2,1 coefficient in Q1.1.9

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Bit(s)	Name	Description
10:0	G2C_CNV_20	DIP RGB 2 YUV Matrix 2,0 coefficient in Q1.1.9

15004BB4 **CAM_G2C_CONV_2B** **RGB/YUV to YUV Matrix Coefficient Row 2 (Part B)** **000007D6**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							G2C_V_OFST									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						G2C_CNV_22										
Type						RW										
Reset						1	1	1	1	1	0	1	0	1	1	0

Bit(s)	Name	Description
25:16	G2C_V_OFST	V offset. Q1.9.0
10:0	G2C_CNV_22	DIP RGB 2 YUV Matrix 2,2 coefficient in Q1.1.9

15004BB8 **CAM_G2C_SHADE_CON_1** **SHADE Con Part 1** **0118000E**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				G2C_SHADE_EN		G2C_SHADE_P0										
Type				RW		RW										
Reset				0		0	0	1	0	0	0	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G2C_SHADE_VAR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

Bit(s)	Name	Description
28	G2C_SHADE_EN	Enables shade
26:16	G2C_SHADE_P0	G2C_SHADE_P0
15:0	G2C_SHADE_VAR	G2C_SHADE_VAR

15004BBC **CAM_G2C_SHADE_CON_2** **SHADE Con Part 2** **0074B740**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										G2C_SHADE_P2[10:4]						
Type										RW						
Reset										1	1	1	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G2C_SHADE_P2[3:0]					G2C_SHADE_P1										
Type	RW					RW										
Reset	1	0	1	1		1	1	1	0	1	0	0	0	0	0	0

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Bit(s)	Name	Description
22:12	G2C_SHADE_P2	G2C_SHADE_P2
10:0	G2C_SHADE_P1	G2C_SHADE_P1

15004BC0 **CAM_G2C_SHADE_CON_3** **SHADE Con Part 3** **00000133**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name								G2C_SHADE_UB								
Type								RW								
Reset								1	0	0	1	1	0	0	1	1

Bit(s)	Name	Description
8:0	G2C_SHADE_UB	Shade gain upper bound

15004BC4 **CAM_G2C_SHADE_TAR** **SHADE Position** **079F0A5A**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				G2C_SHADE_YMID												
Type				RW												
Reset				0	0	1	1	1	1	0	0	1	1	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				G2C_SHADE_XMID												
Type				RW												
Reset				0	1	0	1	0	0	1	0	1	1	0	1	0

Bit(s)	Name	Description
28:16	G2C_SHADE_YMID	Shade center y point
12:0	G2C_SHADE_XMID	Shade center x point

15004BC8 **CAM_G2C_SHADE_SP** **OFF** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				G2C_SHADE_YSP												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				G2C_SHADE_XSP												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
28:16	G2C_SHADE_YSP	Y starting offset
12:0	G2C_SHADE_XSP	X starting offset

15004C30 CAM_SRZ1_CONTROL SRZ1 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name												SRZ1_VERT_FIRST			SRZ1_VERT_EN	SRZ1_HORI_EN
Type												USER0			USER0	USER0
Reset												0			0	0

Bit(s)	Name	Description
4	SRZ1_VERT_FIRST	**Double buffer** 0: Horiznotal first then vertical scaling 1: Vertical first then horizontal scaling
1	SRZ1_VERT_EN	**Double buffer** Enables vertical scaling function
0	SRZ1_HORI_EN	**Double buffer** Enables horizontal scaling function

15004C34 CAM_SRZ1_IN_IMG SRZ1 IN IMG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				SRZ1_IN_HT												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				SRZ1_IN_WD												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	SRZ1_IN_HT	**Double buffer** Imput image height
12:0	SRZ1_IN_WD	**Double buffer** Input image width

15004C38 CAM_SRZ1_OUT_IMG SRZ1 OUT IMG 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				SRZ1_OUT_HT												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				SRZ1_OUT_WD												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	SRZ1_OUT_HT	**Double buffer** Output image height
12:0	SRZ1_OUT_WD	**Double buffer** Output image width

15004C3C CAM_SRZ1_HORI_STEP SRZ1_HORI_STEP 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														SRZ1_HORI_STEP[18:16]		
Type														USER0		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRZ1_HORI_STEP[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
18:0	SRZ1_HORI_STEP	**Double buffer** Horiznotal scaling ratio

15004C40 CAM_SRZ1_VERT_STEP SRZ1_VERT_STEP 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														SRZ1_VERT_STEP[18:16]		
Type														USER0		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRZ1_VERT_STEP[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
18:0	SRZ1_VERT_STEP	**Double buffer** Vertical scaling ratio

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15004C44 **CAM_SRZ1_HORI_INT_OFST** **SRZ1_HORI_INT_OFST** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**SRZ1_HORI_INT_OFST**												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	SRZ1_HORI_INT_OFST	**Double buffer** Horizontal integer offset

15004C48 **CAM_SRZ1_HORI_SUB_OFST** **SRZ1_HORI_SUB_OFST** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**SRZ1_HORI_SUB_OFST**														
Type		USER0														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:0	SRZ1_HORI_SUB_OFST	**Double buffer** Horizontal sub-pixel offset

15004C4C **CAM_SRZ1_VERT_INT_OFST** **SRZ1_VERT_INT_OFST** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**SRZ1_VERT_INT_OFST**												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	SRZ1_VERT_INT_OFST	**Double buffer** Vertical integer offset

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15004C50 CAM_SRZ1_VERT_SUB_OFST SRZ1_VERT_SUB_OFST 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		SRZ1_VERT_SUB_OFST														
Type		USER0														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:0	SRZ1_VERT_SUB_OFST	**Double buffer** Vertical sub-pixel offset

15004C60 CAM_SRZ2_CONTROL SRZ2 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												SRZ2_VERT_FIRST			SRZ2_VERT_EN	SRZ2_HORI_EN
Type												USER0			USER0	USER0
Reset												0			0	0

Bit(s)	Name	Description
4	SRZ2_VERT_FIRST	**Double buffer** 0: Horiznotal first then vertical scaling 1: Vertical first then horizontal scaling
1	SRZ2_VERT_EN	**Double buffer** Enables vertical scaling function
0	SRZ2_HORI_EN	**Double buffer** Enables horizontal scaling function

15004C64 CAM_SRZ2_IN_IMG SRZ2 IN IMG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				SRZ2_IN_HT												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				SRZ2_IN_WD												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
28:16	SRZ2_IN_HT	**Double buffer** Imput image height
12:0	SRZ2_IN_WD	**Double buffer** Input image width

15004C68 CAM_SRZ2_OUT_IMG SRZ2 OUT IMG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				SRZ2_OUT_HT												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				SRZ2_OUT_WD												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	SRZ2_OUT_HT	**Double buffer** Output image height
12:0	SRZ2_OUT_WD	**Double buffer** Output image width

15004C6C CAM_SRZ2_HORI_STEP SRZ2_HORI_STEP 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														SRZ2_HORI_STEP[18:16]		
Type														USER0		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRZ2_HORI_STEP[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
18:0	SRZ2_HORI_STEP	**Double buffer** Horiznotal scaling ratio

15004C70 CAM_SRZ2_VERT_STEP SRZ2_VERT_STEP 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														SRZ2_VERT_STEP[18:16]		
Type														USER0		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRZ2_VERT_STEP[15:0]															
Type	USER0															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
18:0	SRZ2_VERT_STEP	**Double buffer** Vertical scaling ratio

15004C74 **CAM_SRZ2_HORI_INT_OFST** **SRZ2_HORI_INT_OFST** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**SRZ2_HORI_INT_OFST**												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	SRZ2_HORI_INT_OFST	**Double buffer** Horizontal integer offset

15004C78 **CAM_SRZ2_HORI_SUB_OFST** **SRZ2_HORI_SUB_OFST** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**SRZ2_HORI_SUB_OFST**														
Type		USER0														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:0	SRZ2_HORI_SUB_OFST	**Double buffer** Horizontal sub-pixel offset

15004C7C **CAM_SRZ2_VERT_INT_OFST** **SRZ2_VERT_INT_OFST** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**SRZ2_VERT_INT_OFST**												
Type				USER0												

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Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	SRZ2_VERT_INT_OFST	**Double buffer** Vertical integer offset

15004C80 **CAM_SRZ2_VERT_SUB_OFST** **SRZ2_VERT_SUB_OFST** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**SRZ2_VERT_SUB_OFST**														
Type		USER0														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:0	SRZ2_VERT_SUB_OFST	**Double buffer** Vertical sub-pixel offset

15004C90 **CAM_MIX1_CTRL_0** **MIX1 Control Register 0** **01FF0001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MIX1_DT**								**MIX1_B1**							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MIX1_B0**															**MIX1_WT_SEL**
Type	RW															RW
Reset	0	0	0	0	0	0	0	0								1

Bit(s)	Name	Description
31:24	MIX1_DT	**Slope of weight lookup table** Format: Q0.8.0
23:16	MIX1_B1	**Upper bound of weight** MIX1_B0 ? MIX1_B1
15:8	MIX1_B0	**Lower bound of weight** MIX1_B0 ? MIX1_B1
0	MIX1_WT_SEL	**Weight switch control** 0: Out = wt*in0 + (1-wt)*in1 1: Out = (1-wt)*in0 + wt*in1

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15004C94 **CAM_MIX1_CTRL_1** **MIX1 Control Register 1** **00FF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									MIX1_M1							
Type									RW							
Reset									1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MIX1_M0							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	MIX1_M1	**Control point of lookup table** MIX1_M0 ? MIX1_M1
7:0	MIX1_M0	**Control point of lookup table** MIX1_M0 ? MIX1_M1

15004C98 **CAM_MIX1_SPARE** **MIX1 Spare Register** **FFFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIX1_SPARE[31:16]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIX1_SPARE[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MIX1_SPARE	Reserved

15004CA0 **CAM_MIX2_CTRL_0** **MIX2 Control Register 0** **01FF0001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIX2_DT								MIX2_B1							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIX2_B0															MIX2_WT_SEL
Type	RW															RW
Reset	0	0	0	0	0	0	0	0								1

Bit(s)	Name	Description
31:24	MIX2_DT	**Slope of weight lookup table** Format: Q0.8.0
23:16	MIX2_B1	**Upper bound of weight** MIX2_B0 ? MIX2_B1

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Bit(s)	Name	Description
15:8	MIX2_B0	**Lower bound of weight** MIX2_B0 ? MIX2_B1
0	MIX2_WT_SEL	**Weight switch control** 0: Out = wt*in0 + (1-wt)*in1 1: Out = (1-wt)*in0 + wt*in1

15004CA4 CAM_MIX2_CTRL_1 MIX2 Control Register 1 00FF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									MIX2_M1							
Type									RW							
Reset									1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MIX2_M0							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	MIX2_M1	**Control point of lookup table** MIX2_M0 ? MIX2_M1
7:0	MIX2_M0	**Control point of lookup table** MIX2_M0 ? MIX2_M1

15004CA8 CAM_MIX2_SPARE MIX2 Spare Register FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIX2_SPARE[31:16]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIX2_SPARE[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MIX2_SPARE	Reserved

15004CB0 CAM_MIX3_CTRL_0 MIX3 Control Register 0 01FF0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIX3_DT								MIX3_B1							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIX3_B0															MIX3_WT_SEL

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Type	RW															RW
Reset	0	0	0	0	0	0	0	0								1

Bit(s)	Name	Description
31:24	MIX3_DT	**Slope of weight lookup table** Format: Q0.8.0
23:16	MIX3_B1	**Upper bound of weight** MIX3_B0 ? MIX3_B1
15:8	MIX3_B0	**Lower bound of weight** MIX3_B0 ? MIX3_B1
0	MIX3_WT_SEL	**Weight switch control** 0: Out = wt*in0 + (1-wt)*in1 1: Out = (1-wt)*in0 + wt*in1

15004CB4 CAM_MIX3_CTRL_1 MIX3 Control Register 1 00FF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									MIX3_M1							
Type									RW							
Reset									1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MIX3_M0							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	MIX3_M1	**Control point of lookup table** MIX3_M0 ? MIX3_M1
7:0	MIX3_M0	**Control point of lookup table** MIX3_M0 ? MIX3_M1

15004CB8 CAM_MIX3_SPARE MIX3 Spare Register FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIX3_SPARE[31:16]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIX3_SPARE[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MIX3_SPARE	Reserved

15004CC0 CAM_NR3D_BLEND 3D NR Blending Register 10101019

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				NR3D_RND_V								NR3D_RND_U				
Type				RW								RW				
Reset				1	0	0	0	0				1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				NR3D_RND_Y								NR3D_GAIN				
Type				RW								RW				
Reset				1	0	0	0	0				1	1	0	0	1

Bit(s)	Name	Description
28:24	NR3D_RND_V	**0~31** Will be added for rounding [Feedback = (limiter_output*diff + NR3D_FEEDBACK_ROUND)/32]
20:16	NR3D_RND_U	**0~31** Will be added for rounding [Feedback = (limiter_output*diff + NR3D_FEEDBACK_ROUND)/32]
12:8	NR3D_RND_Y	**0~31** Will be added for rounding [Feedback = (limiter_output*diff + NR3D_FEEDBACK_ROUND)/32]
4:0	NR3D_GAIN	**0~31** 31: Close tot *1.0 feedback 25: *0.78 feedback

15004CC4 **CAM_NR3D_FBCNT_OFF** **3D NR FBCNT Offset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			NR3D_FB_CNT_YOFF													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			NR3D_FB_CNT_XOFF													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
29:16	NR3D_FB_CNT_YOFF	
13:1	NR3D_FB_CNT_XOFF	Actual x offset = XOFF*2

15004CC8 **CAM_NR3D_FBCNT_SIZ** **3D NR FBCNT Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			NR3D_FB_CNT_YSIZ													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			NR3D_FB_CNT_XSIZ													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	

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Bit(s)	Name	Description
29:16	NR3D_FB_CNT_YSIZ	
13:1	NR3D_FB_CNT_XSIZ	Actual x size = XSIZ*2

15004CCC **CAM_NR3D_FB_COUNT** **3D NR FB Count Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					NR3D_FB_CNT[27:16]											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NR3D_FB_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:0	NR3D_FB_CNT	**0~XSIZE*YSIZE** Firmware reads this value for feedback control.

15004CD0 **CAM_NR3D_LMT_CPX** **3D NR Limit CPX Register** **A0604020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NR3D_LMT_CPX4								NR3D_LMT_CPX3							
Type	RW								RW							
Reset	1	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NR3D_LMT_CPX2								NR3D_LMT_CPX1							
Type	RW								RW							
Reset	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31:24	NR3D_LMT_CPX4	**0~255** CPX1<CPX2<CPX3<CPX4
23:16	NR3D_LMT_CPX3	**0~255** CPX1<CPX2<CPX3<CPX4
15:8	NR3D_LMT_CPX2	**0~255** CPX1<CPX2<CPX3<CPX4
7:0	NR3D_LMT_CPX1	**0~255** CPX1<CPX2<CPX3<CPX4

15004CD4 **CAM_NR3D_LMT_Y_CON1** **3D NR Limit Y Control Register 1** **140A180C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				NR3D_LMT_Y1_TH								NR3D_LMT_Y1				

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Type				RW								RW				
Reset				1	0	1	0	0				0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				NR3D_LMT_Y0_TH								NR3D_LMT_Y0				
Type				RW								RW				
Reset				1	1	0	0	0				0	1	1	0	0

Bit(s)	Name	Description
28:24	NR3D_LMT_Y1_TH	**0~31** 0< Y1 < Y1_TH <= (2*Y1)
20:16	NR3D_LMT_Y1	**0~31** 0< Y1 < Y1_TH <= (2*Y1)
12:8	NR3D_LMT_Y0_TH	**0~31** 0< Y0 < Y0_TH <= (2*Y0)
4:0	NR3D_LMT_Y0	**0~31** 0< Y0 < Y0_TH <= (2*Y0)

15004CD8 CAM_NR3D_LMT_Y_CON2 3D NR Limit Y Control Register 2 0A051008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				NR3D_LMT_Y3_TH								NR3D_LMT_Y3				
Type				RW								RW				
Reset				0	1	0	1	0				0	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				NR3D_LMT_Y2_TH								NR3D_LMT_Y2				
Type				RW								RW				
Reset				1	0	0	0	0				0	1	0	0	0

Bit(s)	Name	Description
28:24	NR3D_LMT_Y3_TH	**0~31** 0< Y3 < Y3_TH <= (2*Y3)
20:16	NR3D_LMT_Y3	**0~31** 0< Y3 < Y3_TH <= (2*Y3)
12:8	NR3D_LMT_Y2_TH	**0~31** 0< Y2 < Y2_TH <= (2*Y2)
4:0	NR3D_LMT_Y2	**0~31** 0< Y2 < Y2_TH <= (2*Y2)

15004CDC CAM_NR3D_LMT_Y_CON3 3D NR Limit Y Control Register 3 00000603

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				NR3D_LMT_Y4_TH								NR3D_LMT_Y4				
Type				RW								RW				
Reset				0	0	1	1	0				0	0	0	1	1

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Bit(s)	Name	Description
12:8	NR3D_LMT_Y4_TH	**0~31** 0< Y4 < Y4_TH <= (2*Y4)
4:0	NR3D_LMT_Y4	**0~31** 0< Y4 < Y4_TH <= (2*Y4)

15004CE0 **CAM_NR3D_LMT_U_CON1** **3D NR Limit U Control Register 1** **05050505**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				NR3D_LMT_U1_TH								NR3D_LMT_U1				
Type				RW								RW				
Reset				0	0	1	0	1				0	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				NR3D_LMT_U0_TH								NR3D_LMT_U0				
Type				RW								RW				
Reset				0	0	1	0	1				0	0	1	0	1

Bit(s)	Name	Description
28:24	NR3D_LMT_U1_TH	**0~31** 0< U1 < U1_TH <= (2*U1)
20:16	NR3D_LMT_U1	**0~31** 0< U1 < U1_TH <= (2*U1)
12:8	NR3D_LMT_U0_TH	**0~31** 0< U0 < U0_TH <= (2*U0)
4:0	NR3D_LMT_U0	**0~31** 0< U0 < U0_TH <= (2*U0)

15004CE4 **CAM_NR3D_LMT_U_CON2** **3D NR Limit U Control Register 2** **05050505**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				NR3D_LMT_U3_TH								NR3D_LMT_U3				
Type				RW								RW				
Reset				0	0	1	0	1				0	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				NR3D_LMT_U2_TH								NR3D_LMT_U2				
Type				RW								RW				
Reset				0	0	1	0	1				0	0	1	0	1

Bit(s)	Name	Description
28:24	NR3D_LMT_U3_TH	**0~31** 0< U3 < U3_TH <= (2*U3)
20:16	NR3D_LMT_U3	**0~31** 0< U3 < U3_TH <= (2*U3)
12:8	NR3D_LMT_U2_TH	**0~31** 0< U2 < U2_TH <= (2*U2)

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Bit(s)	Name	Description
4:0	NR3D_LMT_U2	**0~31** 0< U2 < U2_TH <= (2*U2)

15004CE8 **CAM_NR3D_LMT_U_CON3** **3D NR Limit U Control Register 3** **00000202**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				NR3D_LMT_U4_TH								NR3D_LMT_U4				
Type				RW								RW				
Reset				0	0	0	1	0				0	0	0	1	0

Bit(s)	Name	Description
12:8	NR3D_LMT_U4_TH	**0~31** 0< U4 < U4_TH <= (2*U4)
4:0	NR3D_LMT_U4	**0~31** 0< U4 < U4_TH <= (2*U4)

15004CEC **CAM_NR3D_LMT_V_CON1** **3D NR Limit V Control Register 1** **05050505**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				NR3D_LMT_V1_TH								NR3D_LMT_V1				
Type				RW								RW				
Reset				0	0	1	0	1				0	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				NR3D_LMT_V0_TH								NR3D_LMT_V0				
Type				RW								RW				
Reset				0	0	1	0	1				0	0	1	0	1

Bit(s)	Name	Description
28:24	NR3D_LMT_V1_TH	**0~31** 0< V1 < V1_TH <= (2*V1)
20:16	NR3D_LMT_V1	**0~31** 0< V1 < V1_TH <= (2*V1)
12:8	NR3D_LMT_V0_TH	**0~31** 0< V0 < V0_TH <= (2*V0)
4:0	NR3D_LMT_V0	**0~31** 0< V0 < V0_TH <= (2*V0)

15004CF0 **CAM_NR3D_LMT_V_CON2** **3D NR Limit V Control Register 2** **05050505**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				NR3D_LMT_V3_TH								NR3D_LMT_V3				
Type				RW								RW				
Reset				0	0	1	0	1				0	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				NR3D_LMT_V2_TH								NR3D_LMT_V2				
Type				RW								RW				
Reset				0	0	1	0	1				0	0	1	0	1

Bit(s)	Name	Description
28:24	NR3D_LMT_V3_TH	**0~31** 0< V3 < V3_TH <= (2*V3)
20:16	NR3D_LMT_V3	**0~31** 0< V3 < V3_TH <= (2*V3)
12:8	NR3D_LMT_V2_TH	**0~31** 0< V2 < V2_TH <= (2*V2)
4:0	NR3D_LMT_V2	**0~31** 0< V2 < V2_TH <= (2*V2)

15004CF4 **CAM_NR3D_LMT_V_CON3** **3D NR Limit V Control Register 3** **00000202**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				NR3D_LMT_V4_TH								NR3D_LMT_V4				
Type				RW								RW				
Reset				0	0	0	1	0				0	0	0	1	0

Bit(s)	Name	Description
12:8	NR3D_LMT_V4_TH	**0~31** 0< V4 < V4_TH <= (2*V4)
4:0	NR3D_LMT_V4	**0~31** 0< V4 < V4_TH <= (2*V4)

15004CF8 **CAM_NR3D_CTRL** **3D NR Control Register** **00000002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												NR3D_ON_EN			NR3D_LMT_OUT_CNT_TH	
Type												RW			RW	
Reset												0			1	0

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Bit(s)	Name	Description
4	NR3D_ON_EN	Enables valid-area setting of previous frame
1:0	NR3D_LMT_OUT_CNT_TH	0~2

15004CFC **CAM_NR3D_ON_OFF** **3D NR On Offset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			NR3D_ON_OFST_Y													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			NR3D_ON_OFST_X													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	NR3D_ON_OFST_Y	**Y offset of valid area of the previous frame**
13:0	NR3D_ON_OFST_X	**X offset of valid area of the previous frame** Due to RDMA limitation, x offset must be even.

15004D00 **CAM_NR3D_ON_SIZ** **3D NR On Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			NR3D_ON_HT													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			NR3D_ON_WD													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	NR3D_ON_HT	**Height of valid area of the previous frame** If RDMA is disabled, the height must be 0. The entire previous buffer is in the invalid area.
13:0	NR3D_ON_WD	**Width of valid area of the previous frame** If RDMA is disabled, the width must be 0. The entire previous buffer is in the invalid area. The width must be even.

15004D04 **CAM_NR3D_SPARE0** **3D NR Spare Register** **FFFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NR3D_SPARE_0[31:16]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	NR3D_SPARE_0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	NR3D_SPARE_0	Spare register

15004D10 **CAM_MDP_CROP_X** **MDP_CROP_X** **0FFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MDP_CROP_END_X												
Type				USER0												
Reset				0	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				MDP_CROP_STR_X												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	MDP_CROP_END_X	**Double buffer** MDP_CROP horizontal crop end point
12:0	MDP_CROP_STR_X	**Double buffer** MDP_CROP horizontal crop start point

15004D20 **CAM_MDP_CROP_Y** **MDP_CROP_Y** **0FFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MDP_CROP_END_Y												
Type				USER0												
Reset				0	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				MDP_CROP_STR_Y												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	MDP_CROP_END_Y	**Double buffer** MDP_CROP vertical crop end point
12:0	MDP_CROP_STR_Y	**Double buffer** MDP_CROP vertical crop start point

15004DC0 **CAM_EIS_PREP_ME_CTRL1** **EIS Preprocessor and ME Engine Control 1** **00000009**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EIS_NUM_VWIN				EIS_NUM_HWIN			EIS_NUM_VRP				EIS_KNEE_1				EIS_KNEE_2[

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																3:3]
Type	W1				W1			W1				W1				W1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EIS_KNEE_2[2:0]			EIS_NUM_HRP						EIS_SUBG_EN	EIS_OP_VERT			EIS_OP_HORI		
Type	W1			W1						W1	W1			W1		
Reset	0	0	0	0	0	0	0	0		0	0	0	1	0	0	1

Bit(s)	Name	Description
31:28	EIS_NUM_VWIN	**Maximum vertical window idx (1~8)**
27:25	EIS_NUM_HWIN	**Maximum horizontal window idx (1~4)**
24:21	EIS_NUM_VRP	**Number of vertical RPs (1~8)**
20:17	EIS_KNEE_1	**Knee point of AD knee function**
16:13	EIS_KNEE_2	**Clipping point of AD knee function**
12:8	EIS_NUM_HRP	**Number of horizontal RPs (1~16)**
6	EIS_SUBG_EN	**Selects processing channel in raw domain** 0: Mix channel 1: Select G channel only
5:3	EIS_OP_VERT	**Vertical sub-sampling and IIR selection should be the same as DS_IIR_H.** 1: 1:1 (no sub-sampling) 2: 2:1 4: 4:1
2:0	EIS_OP_HORI	**Selects horizontal sub-sampling and IIR** 1: 1:1 2: 2:1 4: 4:1

15004DC4 CAM_EIS_PREP_ME_CTRL2 EIS Preprocessor and ME Engine Control 2 0000506C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EIS_SPARE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EIS_FIRST_FRM	EIS_RP_MODI	EIS_DC_DL						EIS_VERT_SHR			EIS_HORI_SHR			EIS_PROC_GAIN	
Type	RW	RW	W1						W1			W1			W1	
Reset	0	1	0	1	0	0	0	0	0	1	1	0	1	1	0	0

Bit(s)	Name	Description
31:16	EIS_SPARE	**Reserved spare register**
15	EIS_FIRST_FRM	**First frame signal, used for 2nd pass** circumstance to indicate the first frame 0: Other than first frame 1: The first frame
14	EIS_RP_MODI	**Enables write RP**

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Bit(s)	Name	Description
		Used for update rp, n3d vr scenario disable at odd frame; others always enabled. 0: Disable 1: Enable
13:8	EIS_DC_DL	**Controls horizontal FIR gain** 16: d16 32: d32
7:5	EIS_VERT_SHR	**Controls vertical IIR gain** 3: 1/8x 4: 1/16x
4:2	EIS_HORI_SHR	**Controls horizontal IIR gain** 3: 1/8x 4: 1/16x
1:0	EIS_PROC_GAIN	**Controls horizontal gain** 0: 1x 1: 2x 2: Reserved 3: 1/2x (valid when IIR_V = 1)

15004DC8 **CAM_EIS_LMV_TH** **EIS LMV Thresholds** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LMV_TH_X_CENTER								LMV_TH_X_SOURROUND							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LMV_TH_Y_CENTER								LMV_TH_Y_SURROUND							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	LMV_TH_X_CENTER	LMV X threshold for the central 4 macro blocks
23:16	LMV_TH_X_SOURROUND	LMV X threshold for the surrounding 12 macro blocks
15:8	LMV_TH_Y_CENTER	LMV Y threshold for the central 4 macro blocks
7:0	LMV_TH_Y_SURROUND	LMV Y threshold for the surrounding 12 macro blocks

15004DCC **CAM_EIS_FL_OFFSET** **EIS Search Widnow Offset in Floating Mode** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					EIS_WIN_HOFST											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					EIS_WIN_VOFST											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
27:16	EIS_WIN_HOFST	Horizontal search window offset in floating mode
11:0	EIS_WIN_VOFST	Vertical search window offset in floating mode

15004DE0 **CAM_EIS_MB_OFFSET** **EIS Macro Block Offset** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					EIS_RP_HOFST											
Type					W1											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					EIS_RP_VOFST											
Type					W1											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	EIS_RP_HOFST	Horizontal offset between the start of frame and the start of the 1st macro block
11:0	EIS_RP_VOFST	Vertical offset between the start of frame and the start of the 1st macro block

15004DE4 **CAM_EIS_MB_INTERVAL** **EIS Macro Block Interval** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					EIS_WIN_HSIZE											
Type					W1											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					EIS_WIN_VSIZE											
Type					W1											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	EIS_WIN_HSIZE	Horizontal interval between the 1st RPs of two neighbor macro blocks
11:0	EIS_WIN_VSIZE	Vertical offset interval between the 1st RPs of two neighbor macro blocks

15004DE8 **CAM_EIS_GMV** **EIS Global Motion Vector** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GMV_X															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GMV_Y															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:16	GMV_X	Horizontal global motion vector
15:0	GMV_Y	Vertical global motion vector

15004DEC **CAM_EIS_ERR_CTRL** **EIS Error Control Register** **000F0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CLEAR_ERR**												**ERR_MASK**			
Type	RW												RW			
Reset	0												1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CHK_SUM_OUT**											**CHK_SUM_EN**	**ERR_STATUS**			
Type	RO											RW	RO			
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
31	CLEAR_ERR	Horizontal search window offset in floating mode
19:16	ERR_MASK	Error mask
15:8	CHK_SUM_OUT	Outputs checksum
4	CHK_SUM_EN	Enables checksum
3:0	ERR_STATUS	ERR status

15004DF0 **CAM_EIS_IMAGE_CTRL** **EIS Image Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**PIPE_MODE**			**WIDTH**												
Type	RW			W1												
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**HEIGHT**												
Type				W1												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PIPE_MODE	EIS pipe mode
28:16	WIDTH	EIS image width
12:0	HEIGHT	EIS image height

15004E00 **CAM_DMX_CTL** **DMX_CTL** **000F0000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DMX_EDGE_SET**												**DMX_EDGE**			
Type	RW												RW			
Reset	0												1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**DMX_IHDR_ORD**				**DMX_IHDR_SEP_MODE**
Type												RW				RW
Reset												0				0

Bit(s)	Name	Description
31	DMX_EDGE_SET	**Double buffer** Sets up DMX edge.
19:16	DMX_EDGE	**Double buffer** DMX edge
4	DMX_IHDR_ORD	**Double buffer** DMX iHDR mode order
0	DMX_IHDR_SEP_MODE	**Double buffer** DMX iHDR separate mode

15004E04 CAM_DMX_CROP DMX_CROP 0FFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**DMX_END_X**												
Type				USER0												
Reset				0	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**DMX_STR_X**												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	DMX_END_X	**Double buffer** DMX end point for datapath
12:0	DMX_STR_X	**Double buffer** DMX start point for datapath

15004E08 CAM_DMX_VSIZE DMX_VSIZE 00000FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name				DMX_HT												
Type				USER0												
Reset				0	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
12:0	DMX_HT	**Double buffer** DMX height

15004E10 CAM_BMX_CTL BMX_CTL 000F0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BMX_EDGE_SET												BMX_EDGE			
Type	RW												RW			
Reset	0												1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				BMX_SINGLE_MODE_2				BMX_SINGLE_MODE_1								
Type				RW				RW								
Reset				0				0								

Bit(s)	Name	Description
31	BMX_EDGE_SET	**Double buffer** Sets up BMX edge.
19:16	BMX_EDGE	**Double buffer** BMX edge
12	BMX_SINGLE_MODE_2	**Double buffer** BMX single mode 2 (right)
8	BMX_SINGLE_MODE_1	**Double buffer** BMX single mode 1 (left)

15004E14 CAM_BMX_CROP BMX_CROP 0FFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				BMX_END_X												
Type				USER0												
Reset				0	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				BMX_STR_X												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	BMX_END_X	**Double buffer**

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Bit(s)	Name	Description
12:0	BMX_STR_X	BMX end point for datapath **Double buffer** BMX start Point for datapath

15004E18 **CAM_BMX_VSIZE** **BMX_VSIZE** **00000FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**BMX_HT**												
Type				USER0												
Reset				0	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
12:0	BMX_HT	**Double buffer** BMX height

15004E20 **CAM_RMX_CTL** **RMX_CTL** **000F0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RMX_EDGE_SET**												**RMX_EDGE**			
Type	RW												RW			
Reset	0												1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**RMX_SINGLE_MODE_2**				**RMX_SINGLE_MODE_1**								
Type				RW				RW								
Reset				0				0								

Bit(s)	Name	Description
31	RMX_EDGE_SET	**Double buffer** Sets up RMX edge.
19:16	RMX_EDGE	**Double buffer** RMX edge
12	RMX_SINGLE_MODE_2	**Double buffer** RMX single mode 2 (right)
8	RMX_SINGLE_MODE_1	**Double buffer** RMX single mode 1 (left)

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15004E24 **CAM_RMX_CROP** **RMX_CROP** **0FFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RMX_END_X												
Type				USER0												
Reset				0	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RMX_STR_X												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	RMX_END_X	**Double buffer** RMX end point for datapath
12:0	RMX_STR_X	**Double buffer** RMX start Point for datapath

15004E28 **CAM_RMX_VSIZE** **RMX_VSIZE** **00000FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RMX_HT												
Type				USER0												
Reset				0	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
12:0	RMX_HT	**Double buffer** RMX height

15004F40 **CAM_SL2_CEN** **SL2 Circular Center Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				SL2_CENTR_Y												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				SL2_CENTR_X												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	SL2_CENTR_Y	Center of concentric circles
12:0	SL2_CENTR_X	Center of concentric circles

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15004F44 CAM_SL2_MAX0_RR SL2 MAX0 Radius Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SL2_RR_0[25:16]									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SL2_RR_0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:0	SL2_RR_0	Threshold for gain link = level 0

15004F48 CAM_SL2_MAX1_RR SL2 MAX1 Radius Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SL2_RR_1[25:16]									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SL2_RR_1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:0	SL2_RR_1	Threshold for gain link = level 1

15004F4C CAM_SL2_MAX2_RR SL2 MAX2 Radius Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SL2_RR_2[25:16]									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SL2_RR_2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:0	SL2_RR_2	Threshold for gain link = level 2

15004F50 CAM_SL2_HRZ SL2 HRZ Compensation Register 00000800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

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Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			SL2_HRZ_COMP													
Type			RW													
Reset			0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	SL2_HRZ_COMP	SL2_HRZ_COMP = f = 1/HRZ_Scaling, Q0.3.11

15004F54 CAM_SL2_X_OFF SL2 Horizontal Offset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						SL2_X_OFST[26:16]										
Type						USER0										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SL2_X_OFST[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	SL2_X_OFST	**Double buffer** TPIPE parameter, horizontal offset of the current image, Q0.16.11

15004F58 CAM_SL2_Y_OFF SL2 Vertical Offset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				SL2_Y_OFST												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	SL2_Y_OFST	**Double buffer** TPIPE parameter, vertical offset of the current image, Q0.12.0

15004F60 CAM_SL2B_CEN SL2B Circular Center Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				SL2B_CENTR_Y												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				SL2B_CENTR_X												
Type				RW												

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Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	SL2B_CENTR_Y	Center of concentric circles
12:0	SL2B_CENTR_X	Center of concentric circles

15004F64 CAM_SL2B_MAX0_RR SL2B MAX0 Radius Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SL2B_RR_0[25:16]									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SL2B_RR_0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:0	SL2B_RR_0	Threshold for gain link = level 0

15004F68 CAM_SL2B_MAX1_RR SL2B MAX1 Radius Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SL2B_RR_1[25:16]									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SL2B_RR_1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:0	SL2B_RR_1	Threshold for gain link = level 1

15004F6C CAM_SL2B_MAX2_RR SL2B MAX2 Radius Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SL2B_RR_2[25:16]									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SL2B_RR_2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:0	SL2B_RR_2	Threshold for gain link = level 2

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15004F70 **CAM_SL2B_HRZ** **SL2B HRZ Compensation Register** **00000800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			SL2B_HRZ_COMP													
Type			RW													
Reset			0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	SL2B_HRZ_COMP	SL2B_HRZ_COMP = f = 1/HRZ_Scaling, Q0.3.11

15004F74 **CAM_SL2B_XOFF** **SL2B Horizontal Offset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						SL2B_X_OFST[26:16]										
Type						USER0										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SL2B_X_OFST[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	SL2B_X_OFST	**Double buffer** TPIPE parameter, horizontal offset of the current image, Q0.16.11

15004F78 **CAM_SL2B_YOFF** **SL2B Vertical Offset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				SL2B_Y_OFST												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	SL2B_Y_OFST	**Double buffer** TPIPE parameter, vertical offset of the current image, Q0.12.0

15004FA0 **CAM_CRSP_CTRL** **CRSP Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRSP_RSV_1														CRSP_VERT_EN	CRSP_HORI_EN
Type	RW														RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0			0	0

Bit(s)	Name	Description
15:4	CRSP_RSV_1	**CRSP spare registers** Register value: Don't care
1	CRSP_VERT_EN	**Double buffer** Enables vertical scaling function
0	CRSP_HORI_EN	**Double buffer** Enables horizontal scaling function

15004FA8 CAM_CRSP_OUT_IMG CRSP Output Image Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				CRSP_HT												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CRSP_WD												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	CRSP_HT	**Double buffer** Output image height
12:0	CRSP_WD	**Double buffer** Output image width

15004FAC CAM_CRSP_STEP_OFST CRSP Coefficient Step and OFST 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							CRSP_OFST_Y							CRSP_STEP_Y		
Type							RW							RW		
Reset							0	0						0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							CRSP_OFST_X							CRSP_STEP_X		
Type							RW							RW		
Reset							0	0						0	0	0

Bit(s)	Name	Description
25:24	CRSP_OFST_Y	**Horizontal OFST in vertical direction**

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Bit(s)	Name	Description
		For general output, set it to 0. For YUV420 without rotation, set it to 1. For YUV420 with rotation, set it to 0.
18:16	CRSP_STEP_Y	**Coefficient step in vertical direction** For general output, set it to 2. For YUV420 without rotation, set it to 4. For YUV420 with rotation, set it to 2.
9:8	CRSP_OFST_X	**Horizontal OFST in horizontal direction** For general output, set it to 0. For YUV420 without rotation, set it to 0. For YUV420 with rotation, set it to 1.
2:0	CRSP_STEP_X	**Coefficient step in horizontal direction** For general output, set it to 2. For YUV420 without rotation, set it to 2. For YUV420 with rotation, set it to 2.

15004FB0 **CAM_CRSP_CROP_X** **CRSP_CROP_X** **0FFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CRSP_CROP_EN**			**CRSP_CROP_END_X**												
Type	RW			RW												
Reset	0			0	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**CRSP_CROP_STR_X**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	CRSP_CROP_EN	CRSP_CROP_EN
28:16	CRSP_CROP_END_X	CRSP_CROP horizontal crop end point
12:0	CRSP_CROP_STR_X	CRSP_CROP horizontal crop start point

15004FB4 **CAM_CRSP_CROP_Y** **CRSP_CROP_Y** **0FFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**CRSP_CROP_END_Y**												
Type				RW												
Reset				0	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**CRSP_CROP_STR_Y**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	CRSP_CROP_END_Y	CRSP_CROP vertical crop end point

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Bit(s)	Name	Description
12:0	CRSP_CROP_STR_Y	CRSP_CROP vertical crop start point

15004FC0 **CAM_SL2C_CEN** **SL2C Circular Center Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**SL2C_CENTR_Y**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**SL2C_CENTR_X**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	SL2C_CENTR_Y	Center of concentric circles
12:0	SL2C_CENTR_X	Center of concentric circles

15004FC4 **CAM_SL2C_MAX0_RR** **SL2C MAX0 Radius Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							**SL2C_RR_0[25:16]**									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SL2C_RR_0[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:0	SL2C_RR_0	Threshold for gain link = level 0

15004FC8 **CAM_SL2C_MAX1_RR** **SL2C MAX1 Radius Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							**SL2C_RR_1[25:16]**									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SL2C_RR_1[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:0	SL2C_RR_1	Threshold for gain link = level 1

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15004FCC CAM_SL2C_MAX2_RR SL2C MAX2 Radius Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SL2C_RR_2[25:16]									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SL2C_RR_2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:0	SL2C_RR_2	Threshold for gain link = level 2

15004FD0 CAM_SL2C_HRZ SL2C HRZ Compensation Register 00000800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			SL2C_HRZ_COMP													
Type			RW													
Reset			0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	SL2C_HRZ_COMP	SL2C_HRZ_COMP = f = 1/HRZ_Scaling, Q0.3.11

15004FD4 CAM_SL2C_XOFF SL2C Horizontal Offset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						SL2C_X_OFST[26:16]										
Type						USER0										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SL2C_X_OFST[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	SL2C_X_OFST	**Double buffer** TPIPE parameter, horizontal offset of the current image, Q0.16.11

15004FD8 CAM_SL2C_YOFF SL2C Vertical Offset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

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Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**SL2C_Y_OFST**												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	SL2C_Y_OFST	**Double buffer** TPIPE parameter, vertical offset of the current image, Q0.12.0

15005000 ~ 1500523C **CAM_GGM_LUT_RB[n] (n=0~143)** **GGM_RB_GAMMA_TABLE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**GGM_B**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**GGM_R**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	GGM_B	**B gamma table entry** Do not read/write this control register when GGM is enabled, (ISP pipeline processing is on-going) or output data of GGM will be gated.
15:0	GGM_R	**R gamma table entry** Do not read/write this control register when GGM is enabled (ISP pipeline processing is on-going), or output data of GGM will be gated.

15005240 ~ 1500547C **CAM_GGM_LUT_G[n] (n=0~143)** **GGM_G_GAMMA_TABLE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**GGM_G**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GGM_G	**G Gamma table entry** Do NOT read/write this control register when GGM is enabled (ISP pipeline processing is on-going) or output data of GGM will be gated

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15005480 **CAM_GGM_CTRL** **GGM_CONTROL** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																GGM_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	GGM_EN	Enables gamma function

15005800 ~ 15005D9C **CAM_PCA_TBL[n] (n=0~359)** **PCA Table Register** **00FFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									PCA_HUE_SHIFT							
Type									RW							
Reset									1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PCA_SAT_GAIN								PCA_LUMA_GAIN							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
23:16	PCA_HUE_SHIFT	Yout = (1 + Y_GAIN/128)*Yin
15:8	PCA_SAT_GAIN	Satout = (1 + SAT_GAIN/128)*Satin
7:0	PCA_LUMA_GAIN	Hueout = Huein + (HUE_SHIFT)/2

15005E00 **CAM_PCA_CON1** **PCA Control Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RSV				PCA_LUT_360
Type												RW				RW
Reset												0				0

Bit(s)	Name	Description
4	RSV	**Double buffer** Reserved

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Bit(s)	Name	Description
0	PCA_LUT_360	**Double buffer** Total bins of PCA table 0: 180 bins 1: 360 bins

15005E04 CAM_PCA_CON2 PCA Control Register 2 00FF0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								PCA_Y2YLUT_EN	PCA_S_TH							
Type								RW	RW							
Reset								0	1	1	1	1	1	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				PCA_S_TH_EN			RSV					PCA_C_TH				
Type				RW			RW					RW				
Reset				0			1	0				0	0	0	0	0

Bit(s)	Name	Description
24	PCA_Y2YLUT_EN	0: vFB off 1: vFB on
23:16	PCA_S_TH	**Parameter for saturation gain** The SAT gain of pixels with chroma value bigger than chroma_th is not applied.
12	PCA_S_TH_EN	**Enables chroma threshold to saturation gain**
9:8	RSV	**Reserved**
4:0	PCA_C_TH	**Parameter for luminance gain** The Y gain of pixels with chroma value smaller than chroma_th is not applied.

15006410 CAM_TG2_SEN_MODE Sensor Mode 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				PXL_CNT_RST_SRC	EOF_SRC		SOF_SRC						SOT_CLR_MODE	SOT_MODE	DBL_DATA_BUS	CMOS_EN
Type				RW	RW		RW						RW	RW	RW	RW
Reset				0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
12	PXL_CNT_RST_SRC	**Pixel counter reset source** 0: Vsync rising edge 1: Vsync falling edge
11:10	EOF_SRC	**End of frame source** 0: Line count reaches LIN_END; pixel count reaches PXL_END. 1: Vsync rising edge 2: Vsync falling edge 3: pixel_cnt reaches EOT_CNT
9:8	SOF_SRC	**Start of frame source** 0: Vsync rising edge 1: Vsync falling edge 2: pixel_cnt reaches SOF_CNT
3	SOT_CLR_MODE	**SOT RGB/YUV mode** 0: Choose SOT_MODE selection 1: SOT position before data 1T; only for RGG, YUV
2	SOT_MODE	**SOT modeE** 0: SOT position is at SOT_CNT. 1: SOT position is at sof_1d.
1	DBL_DATA_BUS	**Doubles asynchronous FIFO data bus** For YUV422, RGB565 or JPEG mode, this bit can be set to 1'b1. For RAW/RGB888 mode, this bit must be 1'b0
0	CMOS_EN	**Enables CMOS**

15006414 **CAM_TG2_VF_CON** **VF Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				SPDELAY_MODE		SP_DELAY				FR_CON					SINGLE_MODE	VFDATA_EN
Type				RW		RW				RW					RW	RW
Reset				0		0	0	0		0	0	0			0	0

Bit(s)	Name	Description
12	SPDELAY_MODE	**SP delay mode** 0: Count by vsync 1: Count by grab window
10:8	SP_DELAY	**Still picture mode frame delay** When SP_DELAY is not 0, TAKE_PIC will start to trigger after SP_DELAY frames.
6:4	FR_CON	**Controls frame sampling rate** 000: Every frame is sampled. 001: One frame is sampled every 2 frames. 010: One frame is sampled every 3 frames. 011: One frame is sampled every 4 frames. 100: One frame is sampled every 5 frames. 101: One frame is sampled every 6 frames. 110: One frame is sampled every 7 frames. 111: One frame is sampled every 8 frames.

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Bit(s)	Name	Description
1	SINGLE_MODE	**Single mode** 0: Continuous mode 1: Single mode
0	VFDATA_EN	**Take picture request**

15006418 **CAM_TG2_SEN_GRAB_PXL** **Sensor Grab Pixel Start/End** **7FFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		PXL_E														
Type		RW														
Reset		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PXL_S														
Type		RW														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:16	PXL_E	**Grab end pixel clock number** The first pixel starts from 0.
14:0	PXL_S	**Grab start pixel clock number** The first pixel starts from 0.

1500641C **CAM_TG2_SEN_GRAB_LIN** **Sensor Grab Line Start/End** **1FFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LIN_E												
Type				RW												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				LIN_S												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	LIN_E	**Grab end line number** The first line starts from 0.
12:0	LIN_S	**Grab start line number** The first line starts from 0.

15006420 **CAM_TG2_PATH_CFG** **TG Path Config** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DROP_CNT				WCNT				RCNT				FB_NUM			
Type	RO				RO				RO				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LOCK_EN	FBC_EN	YUV_BIN_EN	YUV_U2S_DIS	RCNT_INC	DB_LOAD_VSPOL	DB_LOAD_SRC	DB_LOAD_DIS	JPG_LINEND_EN		MEMIN_EN	JPGINF_EN			SEN_IN_LSB	
Type	RW	RW	RW	RW	WO	RW	RW	RW	RW		RW	RW			RW	
Reset	0	0	0	0	0	0	0	0	0		0	0			0	0

Bit(s)	Name	Description
31:28	DROP_CNT	**Drop frame counter** 1: Drop 1 frame at TG
27:24	WCNT	**WCNT** HW increases 1 at pass1 done.
23:20	RCNT	**Frame buffer read counter** When pass2 done, increase 1 by rcnt_inc.
19:16	FB_NUM	**Frame buffer number**
15	LOCK_EN	**Enables frame buffer lock**
14	FBC_EN	**Enables frame buffer**
13	YUV_BIN_EN	**Enables YUV binning**
12	YUV_U2S_DIS	**Disables YUV sensor unsigned to signed**
11	RCNT_INC	**Frame buffer control rcnt Increasement by write 1**
10	DB_LOAD_VSPOL	**Double buffer load, vsync polarity** 1'b0: Vsync rises. 1'b1: Vsync falls.
9	DB_LOAD_SRC	**Double buffer load source** 1'b0: TG vs rising edge after polarity 1'b1: External source
8	DB_LOAD_DIS	**Disables double buffer load** 1'b0: Enable, Only load when db_load is high. 1'b1: Disable. Always load.
7	JPG_LINEND_EN	**Enables JPEG interface line mode** 1'b0: JPG frame end is vsync signal. 1'b1: JPG frame end is hsync signal.
5	MEMIN_EN	**Enables memory input**
4	JPGINF_EN	**Enables JPEG interface**
1:0	SEN_IN_LSB	**Selects sensor input data bit order** Used in ISP. YUV422/RGB888/RGB565/Bayer format. Data input in ISP is 12-bit, datain[13:0] 0: datain[13:0] as TG data input 1: datain[11:0] as TG data input 2: datain[9:0] as TG data input 3: datain[7:0] as TG data input

15006424 **CAM_TG2_MEMIN_CTL** **MEMIN Control** **00001430**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													FBC_CNT			
Type													RO			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				MEMIN_DUMMYLIN					MEMIN_DUMMYPXL							

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Type				RW					RW							
Reset				1	0	1	0	0	0	0	1	1	0	0	0	0

Bit(s)	Name	Description
19:16	FBC_CNT	Available frame buffer counter
12:8	MEMIN_DUMMYLIN	Memory input dummy line count
7:0	MEMIN_DUMMYPXL	Memory input dummy pixel count

15006428 **CAM_TG2_INT1** **TG Interrupt 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**VSYNC_INT_POL**	**TG_INT1_PXLNO**														
Type	RW	RW														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**TG_INT1_LINENO**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	VSYNC_INT_POL	**Vsync interrupt polarity** 0: Rising eage 1: Falling edge
30:16	TG_INT1_PXLNO	**TG interrupt1 pixel number**
12:0	TG_INT1_LINENO	**TG interrupt1 line number**

1500642C **CAM_TG2_INT2** **TG Interrupt 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**TG_INT2_PXLNO**														
Type		RW														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**TG_INT2_LINENO**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:16	TG_INT2_PXLNO	TG interrupt2 pixel number
12:0	TG_INT2_LINENO	TG interrupt2 line number

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15006430 **CAM_TG2_SOF_CNT** TG SOF CNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					SOF_CNT[27:16]											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SOF_CNT[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:0	SOF_CNT	User specified SOF count

15006434 **CAM_TG2_SOT_CNT** TG SOT CNT 00000010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					SOT_CNT[27:16]											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SOT_CNT[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
27:0	SOT_CNT	User specified SOT count

15006438 **CAM_TG2_EOT_CNT** TG EOT CNT 0FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					EOT_CNT[27:16]											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EOT_CNT[15:0]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27:0	EOT_CNT	User specified EOT count

1500643C **CAM_TG2_ERR_CTL** TG Error CTL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									DBG_SRC_SEL							
Type									RW							
Reset									0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				REZ_OVRUN_FLIMIT_EN	REZ_OVRUN_FLIMIT_NO						GRAB_ERR_EN	GRAB_ERR_FLIMIT_EN	GRAB_ERR_FLIMIT_NO			
Type				RW	RW						RW	RW	RW			
Reset				0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
23:16	DBG_SRC_SEL	**DBG_SRC**
12	REZ_OVRUN_FLIMIT_EN	**Enables camera to CRZ interface overrun frame count limit**
11:8	REZ_OVRUN_FLIMIT_NO	**Camera to CRZ interface overrun frame count limit number**
5	GRAB_ERR_EN	**Enables TG grab error frame limit**
4	GRAB_ERR_FLIMIT_EN	**Enables TG grab error frame limit** Only for single mode
3:0	GRAB_ERR_FLIMIT_NO	**TG grab error frame limit number** Only for single mode

15006440 **CAM_TG2_DAT_NO** **TG Out Data Num** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DAT_NO[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DAT_NO[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DAT_NO	**TG output data number** 1. For JPEG, RGB and YUV format, it is equal to byte count. 2. For RAW format, it is data count.

15006444 **CAM_TG2_FRM_CNT_ST** **TG_FRM_CNT_ST** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					GRAB_ERR_FCNT								REZ_OVRUN_FCNT			
Type					RO								RO			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
11:8	GRAB_ERR_FCNT	**Grab error frame count**

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Bit(s)	Name	Description
3:0	REZ_OVRUN_FCNT	This frame count is for still mode. Will be reset every time TAK_PIC is set to 0 and add 1 when GRAB_ERR occurs in a frame. **Camera to resizer (or out) interface over run frame count** This frame count is for still mode. Will be reset every time TAK_PIC is set to 0 and add 1 when REZOVRUN occurs in a frame.

15006448 **CAM_TG2_FRMSIZE_ST** **TG FRM SIZE ST** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		PXL_CNT														
Type		RO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				LINE_CNT												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:16	PXL_CNT	Input frame line counter
12:0	LINE_CNT	Input frame pixel counter

1500644C **CAM_TG2_INTER_ST** **TG INTER ST** **00000102**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CAM_FRM_CNT							
Type									RO							
Reset									0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name			TG_CAM_CS											OUT_REQ	OUT_RDY	SYN_VF_DATA_EN
Type			RO											RO	RO	RO
Reset			0	0	0	0	0	1						0	1	0

Bit(s)	Name	Description
23:16	CAM_FRM_CNT	**Input frame counter**
13:8	TG_CAM_CS	**TG state** 6'h1: IDLE 6'h2: VFON_EXP 6'h4: VFON_IDLE 6'h8: VFON_WAIT 6'h10: CAP_EXP 6'h20: CAP_IDLE
2	OUT_REQ	**out req**
1	OUT_RDY	**out rdy**
0	SYN_VF_DATA_EN	**View finder double buffer register status**

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15006500 **CAM_OBC_D_OFFST0** **OBC Offset 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OBC_D_OFST_B												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	OBC_D_OFST_B	Optical black offset for B channel [-4096~4095]

15006504 **CAM_OBC_D_OFFST1** **OBC Offset 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OBC_D_OFST_GR												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	OBC_D_OFST_GR	Optical black offset for GR channel [-4096~4095]

15006508 **CAM_OBC_D_OFFST2** **OBC Offset 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OBC_D_OFST_GB												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	OBC_D_OFST_GB	Optical black offset for GB channel [-4096~4095]

1500650C **CAM_OBC_D_OFFST3** **OBC Offset 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OBC_D_OFST_R												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	OBC_D_OFST_R	Optical black offset for R channel [-4096~4095]

15006510 **CAM_OBC_D_GAIN0** **OBC Gain 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OBC_D_GAIN_B												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	OBC_D_GAIN_B	Optical black register gain for B channel [0~8191]

15006514 **CAM_OBC_D_GAIN1** **OBC Gain 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OBC_D_GAIN_GR												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	OBC_D_GAIN_GR	Optical black register offset for GR channel [0~8191]

15006518 **CAM_OBC_D_GAIN2** **OBC Gain 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OBC_D_GAIN_GB												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
12:0	OBC_D_GAIN_GB	Optical black register offset for GB channel [0~8191]

15006514C **CAM_OBC_D_GAIN3** **OBC Gain 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**OBC_D_GAIN_R**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	OBC_D_GAIN_R	Optical black register offset for R channel [0~8191]

15006530 **CAM_LSC_D_CTL1** **Shading Control 2 Register** **20000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			**LSC_D_PRC_MODE**	**SD_ULTRA_MODE**				**SD_COEFRD_MODE**			**SDBLK_XOFST**					
Type			RW	RW				RW			RW					
Reset			1	0				0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											**SDBLK_YOFST**					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
29	LSC_D_PRC_MODE	**LSC coeff00 signed unsigned switch (i.e. x4 x8 switch)** 0: Original; coeff00 considered as signed, max. x4 (but coeff00 with negative value will be protected, which will result in x1) 1: coef00 considered as unsigned, max. x8 Only valid on MT6571 and later platforms (not supported on MT6582 but shares the same CODA).
28	SD_ULTRA_MODE	**Shading ultra read mode**
24	SD_COEFRD_MODE	**Shading coefficient read mode**
21:16	SDBLK_XOFST	**x directional address offset**
5:0	SDBLK_YOFST	**y directional address offset**

15006534 **CAM_LSC_D_CTL2** **Shading Control 2 Register** **00006000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															**LSC**	**LSC**

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															_D_OFLN	_D_SDBLK_XNUM[4:4]
Type															RW	W1
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**LSC_D_SDBLK_XNUM[3:0]**				**LSC_D_SDBLK_WIDTH**											
Type	W1				RW											
Reset	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	LSC_D_OFLN	0: Online 1: Offline
16:12	LSC_D_SDBLK_XNUM	x directional number of block
11:0	LSC_D_SDBLK_WIDTH	block width in x direction

15006538 CAM_LSC_D_CTL3 LSC Spare Register 00006000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**LSC_SPARE**															**LSC_D_SDBLK_YNUM[4:4]**
Type	RW															W1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**LSC_D_SDBLK_YNUM[3:0]**				**LSC_D_SDBLK_HEIGHT**											
Type	W1				RW											
Reset	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:17	LSC_SPARE	LSC spare register
16:12	LSC_D_SDBLK_YNUM	y directional number of block
11:0	LSC_D_SDBLK_HEIGHT	Block height in y direction

1500653C CAM_LSC_D_LBLOCK Shading Last Block Config Register 00FF00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**LSC_D_SDBLK_lWIDTH**											
Type					RW											
Reset					0	0	0	0	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name					LSC_D_SDBLK_lHEIGHT											
Type					RW											
Reset					0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27:16	LSC_D_SDBLK_lWIDTH	Last block width
11:0	LSC_D_SDBLK_lHEIGHT	Last block height

15006540 CAM_LSC_D_RATIO Shading Ratio Config Register 20202020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			LSC_D_RA0								LSC_D_RA1					
Type			W1								W1					
Reset			1	0	0	0	0	0			1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			LSC_D_RA2								LSC_D_RA3					
Type			W1								W1					
Reset			1	0	0	0	0	0			1	0	0	0	0	0

Bit(s)	Name	Description
29:24	LSC_D_RA0	Shading ratio of channel 0
21:16	LSC_D_RA1	Shading ratio of channel 1
13:8	LSC_D_RA2	Shading ratio of channel 2
5:0	LSC_D_RA3	Shading ratio of channel 3

15006544 CAM_LSC_D_TPIPE_OFST Shading Tile Offset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					LSC_D_TPIPE_OFST_X											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					LSC_D_TPIPE_OFST_Y											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	LSC_D_TPIPE_OFST_X	Shading tile x offset to block boundary
11:0	LSC_D_TPIPE_OFST_Y	Shading tile y offset to block boundary

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15006548 CAM_LSC_D_TPIPE_SIZE Shading Tile Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LSC_D_TPIPE_SIZE_X												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				LSC_D_TPIPE_SIZE_Y												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	LSC_D_TPIPE_SIZE_X	Shading tile x size
12:0	LSC_D_TPIPE_SIZE_Y	Shading tile y size

1500654C CAM_LSC_D_GAIN_TH Shading Gain Threshold Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LSC_D_GAIN_TH0										LSC_D_GAIN_TH1[8:6]		
Type				W1										W1		
Reset				0	0	0	0	0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LSC_D_GAIN_TH1[5:0]							LSC_D_GAIN_TH2								
Type	W1							W1								
Reset	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:20	LSC_D_GAIN_TH0	Shading gain link threshold 0
18:10	LSC_D_GAIN_TH1	Shading gain link threshold 1
8:0	LSC_D_GAIN_TH2	Shading gain link threshold 2

15006550 CAM_RPG_D_SATU_1 RPG_D_SATU_1 0FFF0FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RPG_SATU_GB											
Type					USER0											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RPG_SATU_B											
Type					USER0											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27:16	RPG_SATU_GB	**Double buffer** Q0.12.0: Saturation clip for Gb

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Bit(s)	Name	Description
11:0	RPG_SATU_B	**Double buffer** Q0.12.0: Saturation clip for B

15006554 **CAM_RPG_D_SATU_2** **RPG_D_SATU_2** **0FFF0FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**RPG_SATU_R**											
Type					USER0											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RPG_SATU_GR**											
Type					USER0											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27:16	RPG_SATU_R	**Double buffer** Q0.12.0: Saturation clip for R
11:0	RPG_SATU_GR	**Double buffer** Q0.12.0: Saturation clip for Gr

15006558 **CAM_RPG_D_GAIN_1** **RPG_D_GAIN_1** **02000200**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**RPG_GAIN_GB**												
Type				USER0												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**RPG_GAIN_B**												
Type				USER0												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	RPG_GAIN_GB	**Double buffer** Q0.4.9: Gain for Gb
12:0	RPG_GAIN_B	**Double buffer** Q0.4.9: Gain for B

1500655C **CAM_RPG_D_GAIN_2** **RPG_D_GAIN_2** **02000200**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**RPG_GAIN_R**												
Type				USER0												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RPG_GAIN_GR												
Type				USER0												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	RPG_GAIN_R	**Double buffer** Q0.4.9: Gain for R
12:0	RPG_GAIN_GR	**Double buffer** Q0.4.9: Gain for Gr

15006560 **CAM_RPG_D_OFST_1** **RPG_D_OFST_1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RPG_OFST_GB											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RPG_OFST_B											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	RPG_OFST_GB	**Double buffer** Q1.11.0: Offset for Gb
11:0	RPG_OFST_B	**Double buffer** Q1.11.0: Offset for B

15006564 **CAM_RPG_D_OFST_2** **RPG_D_OFST_2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RPG_OFST_R											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RPG_OFST_GR											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	RPG_OFST_R	**Double buffer** Q1.11.0: Offset for R
11:0	RPG_OFST_GR	**Double buffer** Q1.11.0: Offset for Gr

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150065B0 CAM_AWB_D_WIN_ORG AWB Window Origin 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AWB_W_VORG												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AWB_W_HORG												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	AWB_W_VORG	AWB window origin y
12:0	AWB_W_HORG	AWB window origin x

150065B4 CAM_AWB_D_WIN_SIZE AWB Window Size 00020004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AWB_W_VSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AWB_W_HSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
28:16	AWB_W_VSIZE	AWB window size y
12:0	AWB_W_HSIZE	AWB window size x

150065B8 CAM_AWB_D_WIN_PIT AWB Window Pitch 00020004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AWB_W_VPIT												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AWB_W_HPIT												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
28:16	AWB_W_VPIT	AWB window pitch y
12:0	AWB_W_HPIT	AWB window pitch x

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150065BC CAM_AWB_D_WIN_NUM AWB Window Number 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AWB_W_VNUM							
Type									RW							
Reset									0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AWB_W_HNUM							
Type									RW							
Reset									0	0	0	0	0	0	0	1

Bit(s)	Name	Description
23:16	AWB_W_VNUM	AWB window number y
7:0	AWB_W_HNUM	AWB window number x

150065C0 CAM_AWB_D_GAIN1_0 AWB Raw PreGain1 R/G 02000200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AWB_GAIN1_G												
Type				RW												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AWB_GAIN1_R												
Type				RW												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	AWB_GAIN1_G	Statistic RawPreGain1 G
12:0	AWB_GAIN1_R	Statistic RawPreGain1 R

150065C4 CAM_AWB_D_GAIN1_1 AWB Raw PreGain1 B 00000200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AWB_GAIN1_B												
Type				RW												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	AWB_GAIN1_B	Statistic RawPreGain1 B

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150065C8 CAM_AWB D_LMT1_0 AWB Raw Limit1 R/G 0FFF0FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					AWB_LMT1_G											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AWB_LMT1_R											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27:16	AWB_LMT1_G	Statistic RawLimit1 G
11:0	AWB_LMT1_R	Statistic RawLimit1 R

150065CC CAM_AWB D_LMT1_1 AWB Raw Limit1 B 00000FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AWB_LMT1_B											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
11:0	AWB_LMT1_B	Statistic RawLimit1 B

150065D0 CAM_AWB D_LOW_TH R AWB Low Threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AWB_LOW_THR2							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AWB_LOW_THR1								AWB_LOW_THR0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	AWB_LOW_THR2	AWB low threshold 2
15:8	AWB_LOW_THR1	AWB low threshold 1
7:0	AWB_LOW_THR0	AWB low threshold 0

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150065D4 CAM_AWB_D_HI_THR AWB High Threshod 00FFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AWB_HI_THR2							
Type									RW							
Reset									1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AWB_HI_THR1								AWB_HI_THR0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
23:16	AWB_HI_THR2	AWB high threshold 2
15:8	AWB_HI_THR1	AWB high threshold 1
7:0	AWB_HI_THR0	AWB high threshold 0

150065D8 CAM_AWB_D_PIXEL_CNT0 AWB Pixel cnt 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AWB_PIXEL_CNT0[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AWB_PIXEL_CNT0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	AWB_PIXEL_CNT0	AWB window pixel count, R

150065DC CAM_AWB_D_PIXEL_CNT1 AWB Pixel cnt 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AWB_PIXEL_CNT1[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AWB_PIXEL_CNT1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	AWB_PIXEL_CNT1	AWB window pixel count, G

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150065E0 **CAM_AWB_D_PIXEL_CNT2** **AWB Pixel cnt 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AWB_PIXEL_CNT2[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AWB_PIXEL_CNT2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	AWB_PIXEL_CNT2	AWB window pixel count, B

150065E4 **CAM_AWB_D_ERR_THR** **AWB Error Threshold** **00000100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														AWB_ERR_SFT		
Type														RW		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AWB_ERR_THR											
Type					RW											
Reset					0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
18:16	AWB_ERR_SFT	AWB truncate bit
11:0	AWB_ERR_THR	AWB error threshold

150065E8 **CAM_AWB_D_ROT** **AWB Rotation Parameter** **00000100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							AWB_S									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							AWB_C									
Type							RW									
Reset							0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	AWB_S	AWB Rotation: Sine (Q1.1.8)
9:0	AWB_C	AWB Rotation: Cosine (Q1.1.8)

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150065EC **CAM_AWB_D_Lo_X** **AWB Lighto x Region** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_Lo_X_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_Lo_X_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_Lo_X_UP	AWB lighto Rx up
13:0	AWB_Lo_X_LOW	AWB lighto Rx low

150065F0 **CAM_AWB_D_Lo_Y** **AWB Lighto y Region** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_Lo_Y_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_Lo_Y_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_Lo_Y_UP	AWB lighto ry up
13:0	AWB_Lo_Y_LOW	AWB lighto ry low

150065F4 **CAM_AWB_D_L1_X** **AWB Light1 x Region** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L1_X_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L1_X_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L1_X_UP	AWB light1 rx up
13:0	AWB_L1_X_LOW	AWB light1 rx low

150065F8 **CAM_AWB_D_L1_Y** **AWB Light1 y Region** **00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L1_Y_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L1_Y_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L1_Y_UP	AWB light1 ry up
13:0	AWB_L1_Y_LOW	AWB light1 ry low

150065FC CAM_AWB_D_L2_X AWB Light2 x Region 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L2_X_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L2_X_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L2_X_UP	AWB light2 rx up
13:0	AWB_L2_X_LOW	AWB light2 rx low

15006600 CAM_AWB_D_L2_Y AWB Light2 y Region 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L2_Y_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L2_Y_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L2_Y_UP	AWB light2 ry up
13:0	AWB_L2_Y_LOW	AWB light2 ry low

15006604 CAM_AWB_D_L3_X AWB Light3 x Region 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L3_X_UP													
Type			RW													

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Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**AWB_L3_X_LOW**													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L3_X_UP	AWB light3 rx up
13:0	AWB_L3_X_LOW	AWB light3rx low

15006608 CAM_AWB_D_L3_Y AWB Light3 y Region 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			**AWB_L3_Y_UP**													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**AWB_L3_Y_LOW**													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L3_Y_UP	AWB light3 ry up
13:0	AWB_L3_Y_LOW	AWB light3 ry low

1500660C CAM_AWB_D_L4_X AWB Light4 x Region 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			**AWB_L4_X_UP**													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**AWB_L4_X_LOW**													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L4_X_UP	AWB light4 rx up
13:0	AWB_L4_X_LOW	AWB light4 rx low

15006610 CAM_AWB_D_L4_Y AWB Light4 y Region 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			**AWB_L4_Y_UP**													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**AWB_L4_Y_LOW**													

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Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L4_Y_UP	AWB light4 ry up
13:0	AWB_L4_Y_LOW	AWB light4 ry low

15006614 CAM_AWB_D_L5_X AWB Light5 x Region 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L5_X_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L5_X_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L5_X_UP	AWB light5 rx up
13:0	AWB_L5_X_LOW	AWB light5 rx low

15006618 CAM_AWB_D_L5_Y AWB Light5 y Region 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L5_Y_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L5_Y_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L5_Y_UP	AWB light5 ry up
13:0	AWB_L5_Y_LOW	AWB light5 ry low

1500661C CAM_AWB_D_L6_X AWB Light6 x Region 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L6_X_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L6_X_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
29:16	AWB_L6_X_UP	AWB light6 rx up
13:0	AWB_L6_X_LOW	AWB light6 rx low

15006620 CAM_AWB_D_L6_Y AWB Light6 y Region 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L6_Y_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L6_Y_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L6_Y_UP	AWB light6 ry up
13:0	AWB_L6_Y_LOW	AWB light6 ry low

15006624 CAM_AWB_D_L7_X AWB Light7 x Region 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L7_X_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L7_X_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L7_X_UP	AWB light7 rx up
13:0	AWB_L7_X_LOW	AWB light7 rx low

15006628 CAM_AWB_D_L7_Y AWB Light7 y Region 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L7_Y_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L7_Y_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L7_Y_UP	AWB light7 ry up

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Bit(s)	Name	Description
13:0	AWB_L7_Y_LOW	AWB light7 ry low

1500662C **CAM_AWB_D_L8_X** **AWB Light8 x Region** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L8_X_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L8_X_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L8_X_UP	AWB light8 rx up
13:0	AWB_L8_X_LOW	AWB light8 rx low

15006630 **CAM_AWB_D_L8_Y** **AWB Light8 y Region** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L8_Y_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L8_Y_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L8_Y_UP	AWB light8 ry up
13:0	AWB_L8_Y_LOW	AWB light8 ry low

15006634 **CAM_AWB_D_L9_X** **AWB Light9 x Region** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L9_X_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L9_X_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L9_X_UP	AWB light9 rx up
13:0	AWB_L9_X_LOW	AWB light9 rx low

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15006638 **CAM_AWB_D_L9_Y** **AWB Light9 y Region** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AWB_L9_Y_UP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWB_L9_Y_LOW													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	AWB_L9_Y_UP	AWB light9 ry up
13:0	AWB_L9_Y_LOW	AWB light9 ry low

1500663C **CAM_AWB_D_SPARE** **AWB Spare Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AWB_SPARE[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AWB_SPARE[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AWB_SPARE	AWB spare register

15006650 **CAM_AE_D_HST_CTL** **AE Histogram Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													AE_HST3_EN	AE_HST2_EN	AE_HST1_EN	AE_HST0_EN
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	AE_HST3_EN	Enables AE hsitogram 3
2	AE_HST2_EN	Enables AE hsitogram 2
1	AE_HST1_EN	Enables AE hsitogram 1
0	AE_HST0_EN	Enables AE hsitogram 0

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15006654 CAM_AE_D_GAIN2_0 AE Raw PreGain2 R/G 02000200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					AE_GAIN2_G											
Type					RW											
Reset					0	0	1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AE_GAIN2_R											
Type					RW											
Reset					0	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	AE_GAIN2_G	Statistic RawPreGain2 G
11:0	AE_GAIN2_R	Statistic RawPreGain2 R

15006658 CAM_AE_D_GAIN2_1 AE Raw PreGain2 B 00000200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AE_GAIN2_B											
Type					RW											
Reset					0	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	AE_GAIN2_B	Statistic RawPreGain2 B

1500665C CAM_AE_D_LMT2_0 AE Raw Limit2 R/G 0FFF0FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					AE_LMT2_G											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AE_LMT2_R											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27:16	AE_LMT2_G	Statistic RawLimit2 G
11:0	AE_LMT2_R	Statistic RawLimit2 R

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15006660 CAM_AE_D_LMT2_1 AE Raw Limit2 B 00000FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					AE_LMT2_B											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
11:0	AE_LMT2_B	Statistic RawLimit2 B

15006664 CAM_AE_D_RC_CNV_0 AE Matrix Coeff 0 00000200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						AE_RC_CNV01										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name						AE_RC_CNV00										
Type						RW										
Reset						0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:16	AE_RC_CNV01	Color conv matrix coef 01
10:0	AE_RC_CNV00	Color conv matrix coef 00

15006668 CAM_AE_D_RC_CNV_1 AE Matrix Coeff 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						AE_RC_CNV10										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name						AE_RC_CNV02										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:16	AE_RC_CNV10	Color conv matrix coef 10
10:0	AE_RC_CNV02	Color conv matrix coef 02

1500666C CAM_AE_D_RC_CNV_2 AE Matrix Coeff 2 00000200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name						AE_RC_CNV12										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						AE_RC_CNV11										
Type						RW										
Reset						0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:16	AE_RC_CNV12	Color conv matrix coef 12
10:0	AE_RC_CNV11	Color conv matrix coef 10

15006670 **CAM_AE_D_RC_CNV_3** **AE Matrix Coeff 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						AE_RC_CNV21										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						AE_RC_CNV20										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:16	AE_RC_CNV21	Color conv matrix coef 21
10:0	AE_RC_CNV20	Color conv matrix coef 20

15006674 **CAM_AE_D_RC_CNV_4** **AE Matrix Coeff 4** **00090200**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													AE_RC_ACC			
Type													RW			
Reset													1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						AE_RC_CNV22										
Type						RW										
Reset						0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:16	AE_RC_ACC	**Color conv matrix shift bits** Range: 6~9
10:0	AE_RC_CNV22	**Color conv matrix coef 22**

15006678 **CAM_AE_D_YGAMMA_0** **AE YGAMMA Set 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Y_GMR4								Y_GMR3							

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Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Y_GMR2								Y_GMR1							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Y_GMR4	AE Y Gamma 4
23:16	Y_GMR3	AE Y Gamma 3
15:8	Y_GMR2	AE Y Gamma 2
7:0	Y_GMR1	AE Y Gamma 1

1500667C CAM_AE_D_YGAMMA_1 AE YGAMMA Set 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									Y_GMR5							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	Y_GMR5	AE Y Gamma 5

15006680 CAM_AE_D_HST_SET AE Histogram Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		AE_COLOR_MODE_3				AE_COLOR_MODE_2				AE_COLOR_MODE_1				AE_COLOR_MODE_0		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AE_BIN_MODE_3				AE_BIN_MODE_2				AE_BIN_MODE_1				AE_BIN_MODE_0	
Type			RW				RW				RW				RW	
Reset			0	0			0	0			0	0			0	0

Bit(s)	Name	Description
30:28	AE_COLOR_MODE_3	**AE histogram 3 source** 0: R 1: G 2: B 3: Reserved 4: AE_SUM
26:24	AE_COLOR_MODE_2	**AE histogram 2 source** 0: R 1: G

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Bit(s)	Name	Description
		2: B 3: Reserved 4: AE_SUM
22:20	AE_COLOR_MODE_1	**AE histogram 1 source** 0: R 1: G 2: B 3: RGB mixed 4: AE_SUM
18:16	AE_COLOR_MODE_0	**AE histogram 0 source** 0/1/2/4: Reserved 3: Flare
13:12	AE_BIN_MODE_3	**AE hsitogram 3 bin mode** 0~1: 128 bin 2: 256 bin low 3: 256 bin high
9:8	AE_BIN_MODE_2	**AE hsitogram 2 bin mode** 0~1: 128 bin 2: 256 bin low 3: 256 bin high
5:4	AE_BIN_MODE_1	**AE hsitogram 1 bin mode** 0~1: 128 bin 2: 256 bin low 3: 256 bin high
1:0	AE_BIN_MODE_0	**AE hsitogram 0 bin mode** 0~1: 128 bin 2: 256 bin low 3: 256 bin high

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15006684 CAM_AE_D_HST0_RNG AE Histogram 0 Range 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		AE_Y_HI_0								AE_Y_LOW_0						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		AE_X_HI_0								AE_X_LOW_0						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	AE_Y_HI_0	**Range of interest, defined by window location 0~127** histogram 0, y high
22:16	AE_Y_LOW_0	**Range of interest, defined by window location 0~127** histogram 0, y low
14:8	AE_X_HI_0	**Range of interest, defined by window location 0~127** histogram 0, x high
6:0	AE_X_LOW_0	**Range of interest, defined by window location 0~127** histogram 0, x low

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15006688 **CAM_AE_D_HST1_RNG** **AE Histogram 1 Range** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		AE_Y_HI_1								AE_Y_LOW_1						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		AE_X_HI_1								AE_X_LOW_1						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	AE_Y_HI_1	**Range of interest, defined by window location 0~127** histogram 1, y high
22:16	AE_Y_LOW_1	**Range of interest, defined by window location 0~127** histogram 1, y low
14:8	AE_X_HI_1	**Range of interest, defined by window location 0~127** histogram 1, x high
6:0	AE_X_LOW_1	**Range of interest, defined by window location 0~127** histogram 1, x low

1500668C **CAM_AE_D_HST2_RNG** **AE Histogram 2 Range** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		AE_Y_HI_2								AE_Y_LOW_2						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		AE_X_HI_2								AE_X_LOW_2						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	AE_Y_HI_2	**Range of interest, defined by window location 0~127** histogram 2, y high
22:16	AE_Y_LOW_2	**Range of interest, defined by window location 0~127** histogram 2, y low
14:8	AE_X_HI_2	**Range of interest, defined by window location 0~127** histogram 2, x high
6:0	AE_X_LOW_2	**Range of interest, defined by window location 0~127** histogram 2, x low

15006690 **CAM_AE_D_HST3_RNG** **AE Histogram 3 Range** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		AE_Y_HI_3								AE_Y_LOW_3						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name		AE_X_HI_3							AE_X_LOW_3						
Type		RW							RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	AE_Y_HI_3	**Range of interest, defined by window location 0~127** histogram 3, y high
22:16	AE_Y_LOW_3	**Range of interest, defined by window location 0~127** histogram 3, y low
14:8	AE_X_HI_3	**Range of interest, defined by window location 0~127** histogram 3, x high
6:0	AE_X_LOW_3	**Range of interest, defined by window location 0~127** histogram 3, x low

15006694 CAM_AE_D_SPARE AE Spare Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AE_SPARE[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AE_SPARE[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AE_SPARE	AE spare register

150066A0 CAM_SGG1_D_PGN SGG PGN 00000010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						SGG1_D_GAIN										
Type						RW										
Reset						0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
10:0	SGG1_D_GAIN	**Double buffer** SGG pre-gain for low contrast scene (Q0.7.4)

150066A4 CAM_SGG1_D_GMRC_1 SGG GMRC 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SGG1_D_GMR_4								SGG1_D_GMR_3							
Type	RW								RW							

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SGG1_D_GMR_2**								**SGG1_D_GMR_1**							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	SGG1_D_GMR_4	**Double buffer** SGG gamma control point 4 (256)
23:16	SGG1_D_GMR_3	**Double buffer** SGG gamma control point 3 (128)
15:8	SGG1_D_GMR_2	**Double buffer** SGG gamma control point 2 (64)
7:0	SGG1_D_GMR_1	**Double buffer** SGG gamma control point 1 (32)

150066A8 **CAM_SGG1_D_GMRC_2** **SGG GMRC 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									**SGG1_D_GMR_7**							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SGG1_D_GMR_6**								**SGG1_D_GMR_5**							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	SGG1_D_GMR_7	**Double buffer** SGG gamma control point 7 (2048)
15:8	SGG1_D_GMR_6	**Double buffer** SGG gamma control point 6 (1024)
7:0	SGG1_D_GMR_5	**Double buffer** SGG gamma control point 5 (512)

150066B0 **CAM_AF_D_CON** **AF Control** **0000000C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RESERVED**															
Type	RW															
Reset	0	0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**AF_D_TARY**				**AF_D_TARX**			**AF_D_ODD**	**AF_D_ZZ**	**AF_D_DECI**	
Type						USER0				USER0			USER0	USER0	USER0	
Reset						0	0	0		0	0	0	1	1	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
10:8	AF_D_TARY	**Double buffer** Y coordinate of target AF window (0~5)
6:4	AF_D_TARX	**Double buffer** X coordinate of target AF window (0~5)
3	AF_D_ODD	**Double buffer** Controls even or odd line to do 1 pixel shift when decimation is enabled 0: Even line 1: Odd line
2	AF_D_ZZ	**Double buffer** Always set to 1 Controls 1 pixel shift when decimation is enabled. 0: No shift 1: 1 pixel shift
1:0	AF_D_DECI	**Double buffer** Enables decimation function to decimate input data for horizontal filters 0: No decimation 1: 1/2 decimation 2: 1/4 decimation

150066B4 CAM_AF_D_WINX_1 AF Window X 0&1 1FFF1FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AF_D_WINX_1												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AF_D_WINX_0												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
28:16	AF_D_WINX_1	**Double buffer** AF window start point x1 Set to maximum value 8191 whenever this column of AF window is not enabled.
12:0	AF_D_WINX_0	**Double buffer** AF window start point x0 Set to maximum value 8191 whenever this column of AF window is not enabled.

150066B8 CAM_AF_D_WINX_2 AF Window X 2&3 1FFF1FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AF_D_WINX_3												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AF_D_WINX_2												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1

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Bit(s)	Name	Description
28:16	AF_D_WINX_3	**Double buffer** AF window start point x3 Set to maximum value 8191 whenever this column of AF window is not enabled.
12:0	AF_D_WINX_2	**Double buffer** AF window start point x2 Set to maximum value 8191 whenever this column of AF window is not enabled.

150066BC **CAM_AF_D_WINX_3** **AF Window X 4&5** **1FFF1FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AF_D_WINX_5												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AF_D_WINX_4												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
28:16	AF_D_WINX_5	**Double buffer** AF window start point x5 Set to maximum value 8191 whenever this column of AF window is not enabled.
12:0	AF_D_WINX_4	**Double buffer** AF window start point x4 Set to maximum value 8191 whenever this column of AF window is not enabled.

150066C0 **CAM_AF_D_WINY_1** **AF Window Y 0&1** **1FFF1FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AF_D_WINY_1												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AF_D_WINY_0												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
28:16	AF_D_WINY_1	**Double buffer** AF window start point y1 Set to maximum value 8191 whenever this row of AF window is not enabled.
12:0	AF_D_WINY_0	**Double buffer** AF window start point y0 Set to maximum value 8191 whenever this row of AF window is not enabled.

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150066C4 **CAM_AF_D_WINY_2** **AF Window Y 2&3** **1FFF1FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AF_D_WINY_3												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AF_D_WINY_2												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
28:16	AF_D_WINY_3	**Double buffer** AF window start point y3 Set to maximum value 8191 whenever this row of AF window is not enabled.
12:0	AF_D_WINY_2	**Double buffer** AF window start point y2 Set to maximum value 8191 whenever this row of AF window is not enabled.

150066C8 **CAM_AF_D_WINY_3** **AF Window Y 4&5** **1FFF1FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AF_D_WINY_5												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AF_D_WINY_4												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
28:16	AF_D_WINY_5	**Double buffer** AF window start point y5 Set to maximum value 8191 whenever this row of AF window is not enabled.
12:0	AF_D_WINY_4	**Double buffer** AF window start point y4 Set to maximum value 8191 whenever this row of AF window is not enabled.

150066CC **CAM_AF_D_SIZE** **AF Window Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							AF_D_WIN_HT									
Type							USER0									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							AF_D_WIN_WD									
Type							USER0									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
25:16	AF_D_WIN_HT	**Double buffer** AF window height y
9:0	AF_D_WIN_WD	**Double buffer** AF window width x

150066D4 **CAM_AF_D_FLT_1** **AF Filter P1~P4** **12111023**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AF_D_FLT_P_4								AF_D_FLT_P_3							
Type	RW								RW							
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AF_D_FLT_P_2								AF_D_FLT_P_1							
Type	RW								RW							
Reset	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	1

Bit(s)	Name	Description
31:24	AF_D_FLT_P_4	AF horizontal filter parameter P4
23:16	AF_D_FLT_P_3	AF horizontal filter parameter P3
15:8	AF_D_FLT_P_2	AF horizontal filter parameter P2
7:0	AF_D_FLT_P_1	AF horizontal filter parameter P1

150066D8 **CAM_AF_D_FLT_2** **AF Filter P5~P8** **11121313**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AF_D_FLT_P_8								AF_D_FLT_P_7							
Type	RW								RW							
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AF_D_FLT_P_6								AF_D_FLT_P_5							
Type	RW								RW							
Reset	0	0	0	1	0	0	1	1	0	0	0	1	0	0	1	1

Bit(s)	Name	Description
31:24	AF_D_FLT_P_8	AF horizontal filter parameter P8
23:16	AF_D_FLT_P_7	AF horizontal filter parameter P7
15:8	AF_D_FLT_P_6	AF horizontal filter parameter P6
7:0	AF_D_FLT_P_5	AF horizontal filter parameter P5

150066DC **CAM_AF_D_FLT_3** **AF Filter P9~P12** **02040709**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AF_D_FLT_P_12								AF_D_FLT_P_11							
Type	RW								RW							
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	AF_D_FLT_P_10								AF_D_FLT_P_9							
Type	RW								RW							
Reset	0	0	0	0	0	1	1	1	0	0	0	0	1	0	0	1

Bit(s)	Name	Description
31:24	AF_D_FLT_P_12	AF horizontal filter parameter P12
23:16	AF_D_FLT_P_11	AF horizontal filter parameter P11
15:8	AF_D_FLT_P_10	AF horizontal filter parameter P10
7:0	AF_D_FLT_P_9	AF horizontal filter parameter P9

150066E0 CAM_AF_D_TH AF Filter Threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								AF_D_TH_MODE	AF_D_TH_1							
Type								RW	RW							
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AF_D_TH_0							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24	AF_D_TH_MODE	**Double buffer** AF threshold method 0: Hard threshold 1: Soft threshold
23:16	AF_D_TH_1	**Double buffer** AF vertical filter threshold
7:0	AF_D_TH_0	**Double buffer** AF horizontal filter threshold

150066E4 CAM_AF_D_FLO_WIN_1 AF Floating Window 1 X&Y 1FFF1FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AF_D_FLO_WINY_1												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AF_D_FLO_WINX_1												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
28:16	AF_D_FLO_WINY_1	**Double buffer** AF floating window 1 start point y Set to maximum value 8191 whenever this floating AF window is not enabled.

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Bit(s)	Name	Description
12:0	AF_D_FLO_WINX_1	**Double buffer** AF floating window 1 start point x Set to maximum value 8191 whenever this floating AF window is not enabled.

150066E8 **CAM_AF_D_FLO_SIZE_1** **AF Floating Window 1 Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					AF_D_FLO_HT_1											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AF_D_FLO_WD_1											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	AF_D_FLO_HT_1	**Double buffer** AF floating window 1 height y
11:0	AF_D_FLO_WD_1	**Double buffer** AF floating window 1 width x

150066EC **CAM_AF_D_FLO_WIN_2** **AF Floating Window 2 X&Y** **1FFF1FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AF_D_FLO_WINY_2												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AF_D_FLO_WINX_2												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
28:16	AF_D_FLO_WINY_2	**Double buffer** AF floating window 2 start point y Set to maximum value 8191 whenever this floating AF window is not enabled.
12:0	AF_D_FLO_WINX_2	**Double buffer** AF floating window 2 start point x Set to maximum value 8191 whenever this floating AF window is not enabled.

150066F0 **CAM_AF_D_FLO_SIZE_2** **AF Floating Window 2 Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					AF_D_FLO_HT_2											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name					AF_D_FLO_WD_2											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	AF_D_FLO_HT_2	**Double buffer** AF floating window 2 height y
11:0	AF_D_FLO_WD_2	**Double buffer** AF floating window 2 width x

150066F4 CAM_AF_D_FLO_WIN_3 AF Floating Window 3 X&Y 1FFF1FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AF_D_FLO_WINY_3												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AF_D_FLO_WINX_3												
Type				USER0												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
28:16	AF_D_FLO_WINY_3	**Double buffer** AF floating window 3 start point y Set to maximum value 8191 whenever this floating AF window is not enabled.
12:0	AF_D_FLO_WINX_3	**Double buffer** AF floating window 3 start point x Set to maximum value 8191 whenever this floating AF window is not enabled.

150066F8 CAM_AF_D_FLO_SIZE_3 AF Floating Window 3 Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					AF_D_FLO_HT_3											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AF_D_FLO_WD_3											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	AF_D_FLO_HT_3	**Double buffer** AF floating window 3 height y
11:0	AF_D_FLO_WD_3	**Double buffer** AF floating window 3 width x

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150066FC **CAM_AF_D_FLO_TH** **AF Floating Window Filter Threshold** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AF_D_FLO_TH_1							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AF_D_FLO_TH_0							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	AF_D_FLO_TH_1	**Double buffer** AF floating window vertical filter threshold
7:0	AF_D_FLO_TH_0	**Double buffer** AF floating window horizontal filter threshold

15006700 **CAM_AF_D_IMAGE_SIZE** **AF Input Image Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AF_D_IMAGE_WD												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	AF_D_IMAGE_WD	AF input image width

15006704 **CAM_AF_D_FLT_4** **AF Vertical Filter X0~X1** **01000100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						AF_D_FLT_X_1										
Type						RW										
Reset						0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						AF_D_FLT_X_0										
Type						RW										
Reset						0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:16	AF_D_FLT_X_1	AF vertical filter parameter X1, Q1.2.8
10:0	AF_D_FLT_X_0	AF vertical filter parameter X0, Q1.2.8

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15006708 CAM_AF_D_FLT_5 AF Vertical Filter X2~X3 07000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						AF_D_FLT_X_3										
Type						RW										
Reset						1	1	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						AF_D_FLT_X_2										
Type						RW										
Reset						1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:16	AF_D_FLT_X_3	AF vertical filter parameter X3, Q1.2.8
10:0	AF_D_FLT_X_2	AF vertical filter parameter X2, Q1.2.8

1500670C CAM_AF_D_STAT_L AF Target Window Statistics Output (LSB) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AF_D_STAT_LSB[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AF_D_STAT_LSB[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AF_D_STAT_LSB	AF target window statistics output (LSB)

15006710 CAM_AF_D_STAT_M AF Target Window Statistics Output (MSB) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AF_D_STAT_MSB[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AF_D_STAT_MSB[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AF_D_STAT_MSB	AF target window statistics output (MSB)

15006714 CAM_AF_D_FLO_STAT_1L AF Floating Window 1 Statistics Output (LSB) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AF_D_STAT_LSB[31:16]															

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Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AF_D_STAT_LSB[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AF_D_STAT_LSB	AF floating window 1 statistics output (LSB)

15006718	**CAM_AF_D_FLO_STAT_1M**	**AF Floating Window 1 Statistics Output (MSB)**	**00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**AF_D_STAT_MSB[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AF_D_STAT_MSB[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AF_D_STAT_MSB	AF floating window 1 statistics output (MSB)

1500671C	**CAM_AF_D_FLO_STAT_1V**	**AF Floating Window 1 Statistics Output (VER)**	**00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**AF_D_STAT_VER[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AF_D_STAT_VER[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AF_D_STAT_VER	AF floating window 1 statistics output (VER)

15006720	**CAM_AF_D_FLO_STAT_2L**	**AF Floating Window 2 Statistics Output (LSB)**	**00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**AF_D_STAT_LSB[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AF_D_STAT_LSB[15:0]**															

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Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AF_D_STAT_LSB	AF floating window 2 statistics output (LSB)

15006724 **CAM_AF_D_FLO_STAT_2M** **AF Floating Window 2 Statistics Output (MSB)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AF_D_STAT_MSB[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AF_D_STAT_MSB[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AF_D_STAT_MSB	AF floating window 2 statistics output (MSB)

15006728 **CAM_AF_D_FLO_STAT_2V** **AF Floating Window 2 Statistics Output (VER)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AF_D_STAT_VER[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AF_D_STAT_VER[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AF_D_STAT_VER	AF floating window 2 statistics output (VER)

1500672C **CAM_AF_D_FLO_STAT_3L** **AF Floating Window 3 Statistics Output (LSB)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AF_D_STAT_LSB[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AF_D_STAT_LSB[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	AF_D_STAT_LSB	AF floating window 3 statistics output (LSB)

15006730 **CAM_AF_D_FLO_STAT_3M** **AF Floating Window 3 Statistics Output (MSB)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AF_D_STAT_MSB[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AF_D_STAT_MSB[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AF_D_STAT_MSB	AF floating window 3 statistics output (MSB)

15006734 **CAM_AF_D_FLO_STAT_3V** **AF Floating Window 3 Statistics Output (VER)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AF_D_STAT_VER[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AF_D_STAT_VER[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AF_D_STAT_VER	AF floating window 3 statistics output (VER)

15006760 **CAM_WBN_D_SIZE** **WBN_D_SIZE** **0F3C14B4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				WBN_D_IN_V												
Type				RW												
Reset				0	1	1	1	1	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WBN_D_IN_H												
Type				RW												
Reset				1	0	1	0	0	1	0	1	1	0	1	0	0

Bit(s)	Name	Description
28:16	WBN_D_IN_V	**Binning module input vertical resolution** Max. value: 3,900
12:0	WBN_D_IN_H	**Binning module input vertical resolution**

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Bit(s)	Name	Description
		Max. value: 5,300

15006764 **CAM_WBN_D_MODE** **WBN_D_MODE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								WBN_D_RGBC_DIR			WBN_D_RGBC_ID			WBN_D_ACC		
Type								RW			RW			RW		
Reset								0			0	0		0	0	0

Bit(s)	Name	Description
8	WBN_D_RGBC_DIR	0: slash 1: backslash
5:4	WBN_D_RGBC_ID	**RGBC offset**
2:0	WBN_D_ACC	**Binning mode** 0: (1 1) filter, gain=2 1: (1 1) filter, gain=1 2: (3 1)+(1 3) filter, gain = 4 3: (1 2 1)+(1 3 3 1) filter, gain = 4 and 8 4: W average 5: W accumulation

15006780 **CAM_LCS_D_CON** **LCS Control Register** **30400001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		LCS_D_OUT_HT								LCS_D_OUT_WD						
Type		RW								RW						
Reset		0	1	1	0	0	0	0		1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																LCS_D_LG2
Type																RW
Reset																1

Bit(s)	Name	Description
30:24	LCS_D_OUT_HT	**Output height of small light map** Max. value: 72
22:16	LCS_D_OUT_WD	**Output width of small light map** Max. value: 96
0	LCS_D_LG2	**Controls input of LRZ is log2(G) or G**

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15006784 CAM_LCS_D_ST LCS Start Point 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LCS_D_START_I												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				LCS_D_START_J												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	LCS_D_START_I	**Vertical start point of active window** Must be even.
12:0	LCS_D_START_J	**Horizontal start point of active window** Must be even.

15006788 CAM_LCS_D_AWS LCS Active Window Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LCS_D_IN_HT												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				LCS_D_IN_WD												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	LCS_D_IN_HT	**Must be even** LCS_IN_HT ? LCS_OUT_HT
12:0	LCS_D_IN_WD	**Must be even,** LCS_IN_WD ? 2 * LCS_OUT_WD

1500678C CAM_LCS_D_FLR LCS Flare 00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LCS_D_FLR_GAIN									LCS_D_FLR_OFST						
Type	RW									RW						
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:7	LCS_D_FLR_GAIN	**Q0.1.8** The flare gain
6:0	LCS_D_FLR_OFST	**Q0.7.0**

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Bit(s)	Name	Description
		The flare offset: LCS_FLR_OFST = flare_offset / 4

15006790 **CAM_LCS_D_LRZR_1** **LCS Horizontal Down-sampling Ratio** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													LCS_D_LRZR_X[19:16]			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LCS_D_LRZR_X[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	LCS_D_LRZR_X	Down scale horizontal ratio

15006794 **CAM_LCS_D_LRZR_2** **LCS Vertical Down-sampling Ratio** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													LCS_D_LRZR_Y[19:16]			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LCS_D_LRZR_Y[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	LCS_D_LRZR_Y	Down scale vertical ratio

150067A0 **CAM_RRZ_D_CTL** **RRZ_D CTL** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							RRZ_VERT_TBL_SEL					RRZ_HORI_TBL_SEL				
Type							USER0					USER0				
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RRZ_VERT_EN	RRZ_HORI_EN
Type															USER0	USER0
Reset															0	0

Bit(s)	Name	Description
25:21	RRZ_VERT_TBL_S	**Double buffer**

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Bit(s)	Name	Description
	EL	Selects vertical scaling coefficient table 4 tap: [20:25] (1x up ~ 1/2x down) Cubic accumulation: [0:19] (blur ~ sharp)
20:16	RRZ_HORI_TBL_SEL	**Double buffer** Selects horizontal scaling coefficient table 4 tap: [20:25] (1x up ~ 1/2x down) Cubic accumulation: [0:19] (blur ~ sharp)
1	RRZ_VERT_EN	**Double buffer** Enables vertical scaling function
0	RRZ_HORI_EN	**Double buffer** Enables horizontal scaling function

150067A4 **CAM_RRZ_D_IN_IMG** **RRZ_D IN IMG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RRZ_IN_HT												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RRZ_IN_WD												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	RRZ_IN_HT	**Double buffer** Imput Image height
12:0	RRZ_IN_WD	**Double buffer** Input Image width

150067A8 **CAM_RRZ_D_OUT_IMG** **RRZ_D OUT IMG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RRZ_OUT_HT												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RRZ_OUT_WD												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	RRZ_OUT_HT	**Double buffer** Output Image height
12:0	RRZ_OUT_WD	**Double buffer** Output Image width

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150067AC **CAM_RRZ_D_HORI_STEP** **RRZ_D_HORI_STEP** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**RRZ_HORI_STEP[16:16]**
Type																USER0
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RRZ_HORI_STEP[15:0]**															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	RRZ_HORI_STEP	**Double buffer** Horiznotal scaling ratio

150067B0 **CAM_RRZ_D_VERT_STEP** **RRZ_D_VERT_STEP** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**RRZ_VERT_STEP[16:16]**
Type																USER0
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RRZ_VERT_STEP[15:0]**															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	RRZ_VERT_STEP	**Double buffer** Vertical scaling ratio

150067B4 **CAM_RRZ_D_HORI_INT_OFST** **RRZ_D_HORI_INT_OFST** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**RRZ_HORI_INT_OFST**												

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Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	RRZ_HORI_INT_OFST	**Double buffer** Horizontal integer offset

150067B8 **CAM_RRZ_D_HORI_SUB_OFST** **RRZ_D_HORI_SUB_OFST** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RRZ_HORI_SUB_OFST														
Type		USER0														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:0	RRZ_HORI_SUB_OFST	**Double buffer** Horizontal sub-pixel offset

150067BC **CAM_RRZ_D_VERT_INT_OFST** **RRZ_D_VERT_INT_OFST** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RRZ_VERT_INT_OFST												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	RRZ_VERT_INT_OFST	**Double buffer** Vertical Integer offset

150067C0 **CAM_RRZ_D_VERT_SUB_OFST** **RRZ_D_VERT_SUB_OFST** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RRZ_VERT_SUB_OFST														

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Type		USER0														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:0	RRZ_VERT_SUB_OFST	**Double buffer** Vertical Sub-pixel offset

150067C4 **CAM_RRZ_D_MODE_TH** **RRZ_D_TH_MD** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RRZ_TH_MD2								RRZ_TH_LO							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RRZ_TH_HI								RRZ_TH_MD							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	RRZ_TH_MD2	**0~255** Threshold for detecting Nyquist region
23:16	RRZ_TH_LO	**0~255** Threshold for detecting flat region
15:8	RRZ_TH_HI	**0~255** Threshold for detecting Nyquist region
7:0	RRZ_TH_MD	**0~255** Threshold for detecting edge region

150067C8 **CAM_RRZ_D_MODE_CTL** **RRZ_D_TBL_SEL_SP** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RRZ_CR_MODE
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RRZ_BLD_SL					RRZ_PRF		RRZ_PRF_BLD								
Type	RW					RW		RW								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RRZ_CR_MODE	0/1 for 1-line/3-line chroma calculation kernel
15:11	RRZ_BLD_SL	Slope for directional blending
10:9	RRZ_PRF	Switch b/w high/low-pass G
8:0	RRZ_PRF_BLD	Blending ratio of low/high-pass output

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15006800	CAM_BPC_D_CON	2D BPC_D Control Register	00008020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															BPC_CRC_MODE	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPC_CS_MODE		BPC_DTC_MODE								BPC_TABLE_END_MODE	BPC_LUT_EN				BPC_EN
Type	RW		RW								RW	RW				RW
Reset	1	0	0	0							1	0				0

Bit(s)	Name	Description
17:16	BPC_CRC_MODE	**Double buffer** Anisotropic interpolation or ranking filter or both Valid value: 0~2 0: Automatic detect. 1: Anisotropic filter only 2. Ranking filter only
15:14	BPC_CS_MODE	**Double buffer** Enables cluster handling solution mode for BPC cluster correction 0: Support up to size 2 1: Support up to size 4 (aggressive) 2: Support up to size 4 (conservative)
13:12	BPC_DTC_MODE	**Double buffer** OTF or table lookup or both. Should be 0 if BPC table is off. 0: Use OTF only to locate bad pixels, any of the 3 cases hold Case 1) Table lookup only (if table exists) Case 2) OTF detected and strong bad pixel (BP_level>STRONG_BP_THR_LA) Case 3) Very strong bad pixel (BP_level>STRONG_BP_THR_LB) 1: Bad pixels detected by OTF also locate in the table 2: Use table only to locate bad pixels (This mode can handle >=3 clusters.)
5	BPC_TABLE_END_MODE	**Double buffer** Waits for table input path finished (FKBPI eot) or not 0: Does not wait for table finished. FKBPI is forced to restart by SOF. This mode can only be used when FKBPI configurations are not changed. 1: Wait for table finished
4	BPC_LUT_EN	**Double buffer.** Enables table lookup 1: BPC_DTC_MODE = 0
0	BPC_EN	**Double buffer** Enables 2D BPC correction

15006804	CAM_BPC_D_TH1	BPC_D Detection Condition 1 Register 1	000C606E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name									**BPC_TH_Y[11:4]**							
Type									RW							
Reset									0	0	0	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BPC_TH_Y[3:0]**				**BPC_TH_LWB**											
Type	RW				RW											
Reset	0	1	1	0	0	0	0	0	0	1	1	0	1	1	1	0

Bit(s)	Name	Description
23:12	BPC_TH_Y	Offset of threshold curve section 3
11:0	BPC_TH_LWB	Threshold offset for dark region

15006808 **CAM_BPC_D_TH2** **BPC_D Detection Condition 1 Register 1** **00000258**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**BPC_TH_UPB**											
Type					RW											
Reset					0	0	1	0	0	1	0	1	1	0	0	0

Bit(s)	Name	Description
11:0	BPC_TH_UPB	Upper bound of threshold curve

1500680C **CAM_BPC_D_TH3** **BPC_D Detection Condition 1 Register 2** **B1200100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**BPC_TH_SLB**				**BPC_TH_SLA**				**BPC_TH_XB[11:4]**							
Type	RW				RW				RW							
Reset	1	0	1	1	0	0	0	1	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BPC_TH_XB[3:0]**				**BPC_TH_XA**											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	BPC_TH_SLB	Slope of threshold curve section 3
27:24	BPC_TH_SLA	Slope of threshold curve section 2
23:12	BPC_TH_XB	Starting point of threshold curve section 3
11:0	BPC_TH_XA	Starting point of threshold curve section 2

15006810 **CAM_BPC_D_TH4** **BPC_D Detection Condition 1 Register 3** **BB2C616E**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**BPC_DK_TH_SLB**				**BPC_DK_TH_SLA**				**BPC_DK_TH_XB[11:4]**							
Type	RW				RW				RW							

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Reset	1	0	1	1	1	0	1	1	0	0	1	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPC_DK_TH_XB[3:0]				BPC_DK_TH_XA											
Type	RW				RW											
Reset	0	1	1	0	0	0	0	1	0	1	1	0	1	1	1	0

Bit(s)	Name	Description
31:28	BPC_DK_TH_SLB	Slope of threshold_DK curve section 3
27:24	BPC_DK_TH_SLA	Slope of threshold_DK curve section 2
23:12	BPC_DK_TH_XB	Starting point of threshold_DK curve section 3
11:0	BPC_DK_TH_XA	Starting point of threshold_DK curve section 2

15006814 CAM_BPC_D_DTC BPC_D Detection Condition 1/2/3 Register 00030031

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						BPC_NO_LV							BPC_TH_MUL			
Type						RW							RW			
Reset						0	0	0					0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					BPC_CT_LV					BPC_CS_RNG			BPC_RNG			
Type					RW					RW			RW			
Reset					0	0	0	0		0	1	1	0	0	0	1

Bit(s)	Name	Description
26:24	BPC_NO_LV	**Noise level of image** For tuning false-positive ratio and false-negative ratio
19:16	BPC_TH_MUL	**Threshold for identifying strong pixel**
11:8	BPC_CT_LV	**Crosstalk level of image**
6:4	BPC_CS_RNG	**Allowable number of neighboring pixels for cluster solution** Valid range: 0~7
3:0	BPC_RNG	**Allowable number of neighboring pixels falling in condition 1 threshold range** Valid range: 0~7

15006818 CAM_BPC_D_COR BPC_D Correction Register 05010519

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BPC_DIR_TH2													BPC_RANK_IDX		
Type	RW													RW		
Reset	0	0	0	0	0	1	0	1						0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPC_DIR_TH								BPC_DIR_MAX							
Type	RW								RW							
Reset	0	0	0	0	0	1	0	1	0	0	0	1	1	0	0	1

Bit(s)	Name	Description
31:24	BPC_DIR_TH2	Edge threshold 2 for aniotopic interpolation
18:16	BPC_RANK_IDX	Ranking filter output index

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Bit(s)	Name	Description
15:8	BPC_DIR_TH	When the difference of anisotropic interpolation pixels is bigger than this threshold, ranking filter will be used to correct bad pixels.
7:0	BPC_DIR_MAX	Clamps difference of anisotropic interpolation pixels to this value

1500681C **CAM_BPC_D_TBLI1** **BPC_D Table input information Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				BPC_YOFFSET												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				BPC_XOFFSET												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	BPC_YOFFSET	**Double buffer** The number of first line to input in tile from the beginning of a frame
12:0	BPC_XOFFSET	**Double buffer** The number of first pixel to input in tile from the beginning of a line

15006820 **CAM_BPC_D_TBLI2** **BPC_D Table input information Register 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				BPC_YSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				BPC_XSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	BPC_YSIZE	**Double buffer** The number (minus 1) of lines to input in tile
12:0	BPC_XSIZE	**Double buffer** The number (minus 1) of pixels per line to input in tile

15006824 **CAM_BPC_D_TH1_C** **BPC_D Detection Extension Condition 1 Register 1** **000C606E**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BPC_C_TH_Y[11:4]							
Type									RW							
Reset									0	0	0	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPC_C_TH_Y[3:0]				BPC_C_TH_LWB											
Type	RW				RW											

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Reset	0	1	1	0	0	0	0	0	0	1	1	0	1	1	1	0

Bit(s)	Name	Description
23:12	BPC_C_TH_Y	Offset of threshold curve section 3
11:0	BPC_C_TH_LWB	Threshold offset for dark region

15006828 CAM_BPC_D_TH2_C BPC_D Detection Extension Condition 1 Register 2 00000258

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					BPC_C_TH_UPB											
Type					RW											
Reset					0	0	1	0	0	1	0	1	1	0	0	0

Bit(s)	Name	Description
11:0	BPC_C_TH_UPB	Upper bound of threshold curve

1500682C CAM_BPC_D_TH3_C BPC_D Detection Extension Condition 1 Register 3 B1200100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BPC_C_TH_SLB				BPC_C_TH_SLA				BPC_C_TH_XB[11:4]							
Type	RW				RW				RW							
Reset	1	0	1	1	0	0	0	1	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPC_C_TH_XB[3:0]				BPC_C_TH_XA											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	BPC_C_TH_SLB	Slope of threshold curve section 3
27:24	BPC_C_TH_SLA	Slope of threshold curve section 2
23:12	BPC_C_TH_XB	Starting point of threshold curve section 3
11:0	BPC_C_TH_XA	Starting point of threshold curve section 2

15006850 CAM_NR1_D_CON NR1_D Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												NR1_CT_EN				
Type												RW				

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Reset												0				

Bit(s)	Name	Description
4	NR1_CT_EN	**Double buffer** Enables NR1 Cross-Talk compensation

15006854 CAM_NR1_D_CT_CON NR1_D Crosstalk Compensation Configuration Register 50802003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NR1_CT_DIV		NR1_CT_SLOPE				NR1_MBND									
Type	RW		RW				RW									
Reset	0	1	0	1			0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			NR1_CT_THRD										NR1_CT_MD2		NR1_CT_MD	
Type			RW										RW		RW	
Reset			1	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit(s)	Name	Description
31:30	NR1_CT_DIV	**Selects CT compensation value when CT detector output is false (min. value of m_diff)** 0: Compensation value is clipped to 0. 1: Compensation value is 1/8 of the value. 2: Compensation value is 1/4 of the value. 3: Compensation value is half of the value.
29:28	NR1_CT_SLOPE	**Slope for CT suppression condition** Valid from 0~3 0: Steepest 1: Steep 2: Moderate 3: Gentle slope
25:16	NR1_MBND	**CT_MBND valid for 0~1023** Threshold of the difference between central pixel and neighbor pixels to calculate the mean value 128
13:4	NR1_CT_THRD	**Threshold for suppression condition.**
3:2	NR1_CT_MD2	**Prevents overcompensation** 0: MT6238 algorithm (no limit for overcompensation) 1: 50% avoid the over compensation (recommended) 2: 75% avoid the over compensation 3: 100% avoid the over compensation
1:0	NR1_CT_MD	**Selects pixels to use for CT detection** 0: 4 pixels (Xa, Xb, Xc, Xd) 1: 12 pixels (Xa~Xd, X1~X8) 2: 8 pixels (X1~X8) 3: 8 pixels (Xa~Xd, X5~X8)

15006858 CAM_BNR_D_RSV1 BNR_D RSV1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RSV1[31:16]															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RSV1[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RSV1	RSV1

1500685C **CAM_BNR_D_RSV2** **BNR_D RSV2** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RSV2[31:16]**															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RSV2[15:0]**															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	RSV2	RSV2

15006A00 **CAM_CPG_D_SATU_1** **CPG_SATU_1** **0FFF0FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**CPG_D_SATU_GB**											
Type					USER0											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**CPG_D_SATU_B**											
Type					USER0											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27:16	CPG_D_SATU_GB	**Double buffer** Q0.12.0: Saturation clip for Gb
11:0	CPG_D_SATU_B	**Double buffer** Q0.12.0: Saturation clip for B

15006A04 **CAM_CPG_D_SATU_2** **CPG_SATU_2** **0FFF0FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**CPG_D_SATU_R**											
Type					USER0											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name					CPG_D_SATU_GR											
Type					USER0											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27:16	CPG_D_SATU_R	**Double bBuffer** Q0.12.0: Saturation clip for R
11:0	CPG_D_SATU_GR	**Double buffer** Q0.12.0: Saturation clip for Gr

15006A08 **CAM_CPG_D_GAIN_1** **CPG_GAIN_1** **02000200**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				CPG_D_GAIN_GB												
Type				USER0												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CPG_D_GAIN_B												
Type				USER0												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	CPG_D_GAIN_GB	**Double buffer** Q0.4.9: Gain for Gb
12:0	CPG_D_GAIN_B	**Double buffer** Q0.4.9: Gain for B

15006A0C **CAM_CPG_D_GAIN_2** **CPG_GAIN_2** **02000200**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				CPG_D_GAIN_R												
Type				USER0												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CPG_D_GAIN_GR												
Type				USER0												
Reset				0	0	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	CPG_D_GAIN_R	**Double buffer** Q0.4.9: Gain for R
12:0	CPG_D_GAIN_GR	**Double buffer** Q0.4.9: Gain for Gr

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15006A10 CAM_CPG_D_OFST_1 CPG_OFST_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CPG_D_OFST_GB											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CPG_D_OFST_B											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	CPG_D_OFST_GB	**Double buffer** Q1.11.0: Offset for Gb
11:0	CPG_D_OFST_B	**Double buffer** Q1.11.0: Offset for B

15006A14 CAM_CPG_D_OFST_2 CPG_OFST_2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CPG_D_OFST_R											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CPG_D_OFST_GR											
Type					USER0											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	CPG_D_OFST_R	**Double buffer** Q1.11.0: Offset for R
11:0	CPG_D_OFST_GR	**Double buffer** Q1.11.0: Offset for Gr

15006E00 CAM_DMX_CTL DMX_CTL 000F0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMX_EDGE_SET												DMX_EDGE			
Type	RW												RW			
Reset	0												1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												DMX_I				DMX_I

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												HDR_ORD				HDR_SEP_MODE
Type												RW				RW
Reset												0				0

Bit(s)	Name	Description
31	DMX_EDGE_SET	**Double buffer** Sets up DMX edge
19:16	DMX_EDGE	**Double buffer** DMX sdge
4	DMX_IHDR_ORD	**Double buffer** DMX iHDR mode order
0	DMX_IHDR_SEP_MODE	**Double buffer** DMX iHDR separate mode

15006E04 **CAM_DMX_CROP** **DMX_CROP** **0FFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DMX_END_X												
Type				USER0												
Reset				0	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DMX_STR_X												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	DMX_END_X	**Double buffer** DMX end point for datapath
12:0	DMX_STR_X	**Double buffer** DMX start point for datapath

15006E08 **CAM_DMX_VSIZE** **DMX_VSIZE** **00000FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DMX_HT												
Type				USER0												
Reset				0	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
12:0	DMX_HT	**Double buffer** DMX height

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15006E10 **CAM_BMX_CTL** **BMX_CTL** **000F0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**BMX_EDGE_SET**												**BMX_EDGE**			
Type	RW												RW			
Reset	0												1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**BMX_SINGLE_MODE_2**				**BMX_SINGLE_MODE_1**								
Type				RW				RW								
Reset				0				0								

Bit(s)	Name	Description
31	BMX_EDGE_SET	**Double buffer** Sets up BMX edge
19:16	BMX_EDGE	**Double buffer** BMX edge
12	BMX_SINGLE_MODE_2	**Double buffer** BMX single mode 2 (right)
8	BMX_SINGLE_MODE_1	**Double buffer** BMX single mode 1 (left)

15006E14 **CAM_BMX_CROP** **BMX_CROP** **0FFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**BMX_END_X**												
Type				USER0												
Reset				0	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**BMX_STR_X**												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	BMX_END_X	**Double buffer** BMX end point for datapath
12:0	BMX_STR_X	**Double buffer** BMX start point for datapath

15006E18 **CAM_BMX_VSIZE** **BMX_VSIZE** **00000FFF**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**BMX_HT**												
Type				USER0												
Reset				0	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
12:0	BMX_HT	**Double buffer** BMX height

15006E20 CAM_RMX_CTL RMX_CTL 000F0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RMX_EDGE_SET**												**RMX_EDGE**			
Type	RW												RW			
Reset	0												1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**RMX_SINGLE_MODE_2**				**RMX_SINGLE_MODE_1**								
Type				RW				RW								
Reset				0				0								

Bit(s)	Name	Description
31	RMX_EDGE_SET	**Double buffer** Sets up RMX edge
19:16	RMX_EDGE	**Double buffer** RMX edge
12	RMX_SINGLE_MODE_2	**Double buffer** RMX single mode 2 (right)
8	RMX_SINGLE_MODE_1	**Double buffer** RMX single mode 1 (left)

15006E24 CAM_RMX_CROP RMX_CROP 0FFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**RMX_END_X**												
Type				USER0												
Reset				0	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**RMX_STR_X**												
Type				USER0												

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Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	RMX_END_X	**Double buffer** RMX end point for datapath
12:0	RMX_STR_X	**Double buffer** RMX start Point for datapath

15006E28 **CAM_RMX_VSIZE** **RMX_VSIZE** **00000FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RMX_HT												
Type				USER0												
Reset				0	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
12:0	RMX_HT	**Double buffer** RMX height

15007200 **CAM_DMA_SOFT_RSTSTAT** **DMA Software Reset Status** **7FFFF3F6**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		AAO_D_SOFT_RST_STAT	AFO_D_SOFT_RST_STAT	LCSO_D_SOFT_RST_STAT	RRZO_D_SOFT_RST_STAT	IMGO_D_SOFT_RST_STAT	LSCI_D_SOFT_RST_STAT	BPCI_D_SOFT_RST_STAT	FEO_SOFT_RST_STAT	IMG3O_SOFT_RST_STAT	IMG2O_SOFT_RST_STAT	IMG3CO_SOFT_RST_STAT	IMG3BO_SOFT_RST_STAT	MFBO_SOFT_RST_STAT	UFEO_SOFT_RST_STAT	AAO_SOFT_RST_STAT
Type		RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ESFKO_SOFT_RST_STAT	LCSO_SOFT_RST_STAT	RRZO_SOFT_RST_STAT	IMGO_SOFT_RST_STAT			VIP3I_SOFT_RST_STAT	VIP2I_SOFT_RST_STAT	VIPI_SOFT_RST_STAT	LCEI_SOFT_RST_STAT	UFDI_SOFT_RST_STAT	LSCI_SOFT_RST_STAT		BPCI_SOFT_RST_STAT	IMGI_SOFT_RST_STAT	
Type	RO	RO	RO	RO			RO	RO	RO	RO	RO	RO		RO	RO	
Reset	1	1	1	1			1	1	1	1	1	1		1	1	

Bit(s)	Name	Description
30	AAO_D_SOFT_RST_STAT	AAO_D software reset status
29	AFO_D_SOFT_RST_STAT	AFO_D software reset status

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Bit(s)	Name	Description
28	LCSO_D_SOFT_RST_STAT	LCSO_D software reset status
27	RRZO_D_SOFT_RST_STAT	RRZO_D software reset status
26	IMGO_D_SOFT_RST_STAT	IMGO_D software reset status
25	LSCI_D_SOFT_RST_STAT	LSCI_D software reset status
24	BPCI_D_SOFT_RST_STAT	BPCI_D software reset status
23	FEO_SOFT_RST_STAT	FEO software reset status
22	IMG3O_SOFT_RST_STAT	IMG3O software reset status
21	IMG2O_SOFT_RST_STAT	IMG2O software reset status
20	IMG3CO_SOFT_RST_STAT	IMG3CO software reset status
19	IMG3BO_SOFT_RST_STAT	IMG3BO software reset status
18	MFBO_SOFT_RST_STAT	MFBO software reset status
17	UFEO_SOFT_RST_STAT	UFEO software reset status
16	AAO_SOFT_RST_STAT	AAO software reset status
15	ESFKO_SOFT_RST_STAT	ESFKO software reset status
14	LCSO_SOFT_RST_STAT	LCSO software reset status
13	RRZO_SOFT_RST_STAT	RRZO software reset status
12	IMGO_SOFT_RST_STAT	IMGO software reset status
9	VIP3I_SOFT_RST_STAT	VIP3I software reset status
8	VIP2I_SOFT_RST_STAT	VIP2I software reset status
7	VIPI_SOFT_RST_STAT	VIPI software reset status
6	LCEI_SOFT_RST_STAT	LCEI software reset status
5	UFDI_SOFT_RST_STAT	UFDI software reset status
4	LSCI_SOFT_RST_STAT	LSCI software reset status
2	BPCI_SOFT_RST_STAT	BPCI software reset status
1	IMGI_SOFT_RST_STAT	IMGI software reset status

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15007204 CAM_TDRI_BASE_ADDR DMA Base ADDR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASE_ADDR[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

15007208 CAM_TDRI_OFST_ADDR DMA Offset ADDR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OFFSET_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFFSET_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

1500720C CAM_TDRI_XSIZE DMA XSIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to read

15007210 CAM_CQoI_BASE_ADDR DMA Base ADDR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	BASE_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASE_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

15007214 **CAM_CQ0I_XSIZE** **DMA XSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to read

15007218 **CAM_CQ0I_D_BASE_ADDR** **DMA Base ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASE_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

1500721C **CAM_CQ0I_D_XSIZE** **DMA XSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to read

15007220 **CAM_VERTICAL_FLIP_EN** **DMA Vertical Flip Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		AAO_D_V_FLIP_EN	AFO_D_V_FLIP_EN	LCSO_D_V_FLIP_EN	RRZO_D_V_FLIP_EN	IMGO_D_V_FLIP_EN	LSCI_D_V_FLIP_EN	BPCI_D_V_FLIP_EN	FEO_V_FLIP_EN	IMG3O_V_FLIP_EN	IMG2O_V_FLIP_EN	IMG3CO_V_FLIP_EN	IMG3BO_V_FLIP_EN	MFBO_V_FLIP_EN	UFEO_V_FLIP_EN	AAO_V_FLIP_EN
Type		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ESFKO_V_FLIP_EN	LCSO_V_FLIP_EN	RRZO_V_FLIP_EN	IMGO_V_FLIP_EN			VIP3I_V_FLIP_EN	VIP2I_V_FLIP_EN	VIPI_V_FLIP_EN	LCEI_V_FLIP_EN	UFDI_V_FLIP_EN	LSCI_V_FLIP_EN		BPCI_V_FLIP_EN	IMGI_V_FLIP_EN	
Type	RW	RW	RW	RW			RW	RW	RW	RW	RW	RW		RW	RW	
Reset	0	0	0	0			0	0	0	0	0	0		0	0	

Bit(s)	Name	Description
30	AAO_D_V_FLIP_EN	0: Disable flip function 1: Enable flip function
29	AFO_D_V_FLIP_EN	0: Disable flip function 1: Enable flip function
28	LCSO_D_V_FLIP_EN	0: Disable flip function 1: Enable flip function
27	RRZO_D_V_FLIP_EN	0: Disable flip function 1: Enable flip function
26	IMGO_D_V_FLIP_EN	0: Disable flip function 1: Enable flip function
25	LSCI_D_V_FLIP_EN	0: Disable flip function 1: Enable flip function
24	BPCI_D_V_FLIP_EN	0: Disable flip function 1: Enable flip function
23	FEO_V_FLIP_EN	0: Disable flip function 1: Enable flip function
22	IMG3O_V_FLIP_EN	0: Disable flip function 1: Enable flip function
21	IMG2O_V_FLIP_EN	0: Disable flip function 1: Enable flip function
20	IMG3CO_V_FLIP_EN	0: Disable flip function 1: Enable flip function

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Bit(s)	Name	Description
19	IMG3BO_V_FLIP_EN	0: Disable flip function 1: Enable flip function
18	MFBO_V_FLIP_EN	0: Disable flip function 1: Enable flip function
17	UFEO_V_FLIP_EN	0: Disable flip function 1: Enable flip function
16	AAO_V_FLIP_EN	0: Disable flip function 1: Enable flip function
15	ESFKO_V_FLIP_EN	0: Disable flip function 1: Enable flip function
14	LCSO_V_FLIP_EN	0: Disable flip function 1: Enable flip function
13	RRZO_V_FLIP_EN	0: Disable flip function 1: Enable flip function
12	IMGO_V_FLIP_EN	0: Disable flip function 1: Enable flip function
9	VIP3I_V_FLIP_EN	0: Disable flip function 1: Enable flip function
8	VIP2I_V_FLIP_EN	0: Disable flip function 1: Enable flip function
7	VIPI_V_FLIP_EN	0: Disable flip function 1: Enable flip function
6	LCEI_V_FLIP_EN	0: Disable flip function 1: Enable flip function
5	UFDI_V_FLIP_EN	0: Disable flip function 1: Enable flip function
4	LSCI_V_FLIP_EN	0: Disable flip function 1: Enable flip function
2	BPCI_V_FLIP_EN	0: Disable flip function 1: Enable flip function
1	IMGI_V_FLIP_EN	0: Disable flip function 1: Enable flip function

15007224 **CAM_DMA_SOFT_RESET** **DMA Software Reset** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEPARATE_SOFT_RST_EN	AAO_D_SOFT_RST	AFO_D_SOFT_RST	LCSO_D_SOFT_RST	RRZO_D_SOFT_RST	IMGO_D_SOFT_RST	LSCI_D_SOFT_RST	BPCI_D_SOFT_RST	FEO_SOFT_RST	IMG3O_SOFT_RST	IMG2O_SOFT_RST	IMG3CO_SOFT_RST	IMG3BO_SOFT_RST	MFBO_SOFT_RST	UFEO_SOFT_RST	AAO_SOFT_RST
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ESFKO_SOFT_R	LCSO_SOFT_RS	RRZO_SOFT_RS	IMGO_SOFT_RS			VIP3I_SOFT_RS	VIP2I_SOFT_RS	VIPI_SOFT_RST	LCEI_SOFT_RS	UFDI_SOFT_RS	LSCI_SOFT_RST		BPCI_SOFT_RS	IMGI_SOFT_RS	

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	ST	T	T	T			T	T		T	T			T	T	
Type	RW	RW	RW	RW			RW	RW	RW	RW	RW	RW		RW	RW	
Reset	0	0	0	0			0	0	0	0	0	0		0	0	

Bit(s)	Name	Description
31	SEPARATE_SOFT_RST_EN	0: Top trig software reset 1: Enable separate software reset en
30	AAO_D_SOFT_RST	0: Dose not trigger software reset 1: Trigger software reset
29	AFO_D_SOFT_RST	0: Dose not trigger software reset 1: Trigger software reset
28	LCSO_D_SOFT_RST	0: Dose not trigger software reset 1: Trigger software reset
27	RRZO_D_SOFT_RST	0: Dose not trigger software reset 1: Trigger software reset
26	IMGO_D_SOFT_RST	0: Dose not trigger software reset 1: Trigger software reset
25	LSCI_D_SOFT_RST	0: Dose not trigger software reset 1: Trigger software reset
24	BPCI_D_SOFT_RST	0: Dose not trigger software reset 1: Trigger software reset
23	FEO_SOFT_RST	0: Dose not trigger software reset 1: Trigger software reset
22	IMG3O_SOFT_RST	0: Dose not trigger software reset 1: Trigger software reset
21	IMG2O_SOFT_RST	0: Dose not trigger software reset 1: Trigger software reset
20	IMG3CO_SOFT_RST	0: Dose not trigger software reset 1: Trigger software reset
19	IMG3BO_SOFT_RST	0: Dose not trigger software reset 1: Trigger software reset
18	MFBO_SOFT_RST	0: Dose not trigger software reset 1: Trigger software reset
17	UFEO_SOFT_RST	0: Dose not trigger software reset 1: Trigger software reset
16	AAO_SOFT_RST	0: Dose not trigger software reset 1: Trigger software reset
15	ESFKO_SOFT_RST	0: Dose not trigger software reset 1: Trigger software reset
14	LCSO_SOFT_RST	0: Dose not trigger software reset 1: Trigger software reset
13	RRZO_SOFT_RST	0: Dose not trigger software reset 1: Trigger software reset
12	IMGO_SOFT_RST	0: Dose not trigger software reset 1: Trigger software reset
9	VIP3I_SOFT_RST	0: Dose not trigger software reset 1: Trigger software reset
8	VIP2I_SOFT_RST	0: Dose not trigger software reset 1: Trigger software reset
7	VIPI_SOFT_RST	0: Dose not trigger software reset

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Bit(s)	Name	Description
		1: Trigger software reset
6	LCEI_SOFT_RST	0: Dose not trigger software reset 1: Trigger software reset
5	UFDI_SOFT_RST	0: Dose not trigger software reset 1: Trigger software reset
4	LSCI_SOFT_RST	0: Dose not trigger software reset 1: Trigger software reset
2	BPCI_SOFT_RST	0: Dose not trigger software reset 1: Trigger software reset
1	IMGI_SOFT_RST	0: Dose not trigger software reset 1: Trigger software reset

15007228 **CAM_LAST_ULTRA_EN** **DMA Last Ultra Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		AAO_D_LAST_ULTRA_EN	AFO_D_LAST_ULTRA_EN	LCSO_D_LAST_ULTRA_EN	RRZO_D_LAST_ULTRA_EN	IMGO_D_LAST_ULTRA_EN			FEO_LAST_ULTRA_EN	IMG3O_LAST_ULTRA_EN	IMG2O_LAST_ULTRA_EN	IMG3CO_LAST_ULTRA_EN	IMG3BO_LAST_ULTRA_EN	MFBO_LAST_ULTRA_EN	UFEO_LAST_ULTRA_EN	AAO_LAST_ULTRA_EN
Type		RW	RW	RW	RW	RW			RW	RW	RW	RW	RW	RW	RW	RW
Reset		0	0	0	0	0			0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ESFKO_LAST_ULTRA_EN	LCSO_LAST_ULTRA_EN	RRZO_LAST_ULTRA_EN	IMGO_LAST_ULTRA_EN									LSCI_D_LAST_ULTRA_EN	BPCI_D_LAST_ULTRA_EN	LSCI_LAST_ULTRA_EN	BPCI_LAST_ULTRA_EN
Type	RW	RW	RW	RW									RW	RW	RW	RW
Reset	0	0	0	0									0	0	0	0

Bit(s)	Name	Description
30	AAO_D_LAST_ULTRA_EN	0: Disable last ultra 1: Enable last ultra
29	AFO_D_LAST_ULTRA_EN	0: Disable last ultra 1: Enable last ultra
28	LCSO_D_LAST_ULTRA_EN	0: Disable last ultra 1: Enable last ultra
27	RRZO_D_LAST_ULTRA_EN	0: Disable last ultra 1: Enable last ultra
26	IMGO_D_LAST_ULTRA_EN	0: Disable last ultra 1: Enable last ultra
23	FEO_LAST_ULTRA_EN	0: Disable last ultra 1: Enable last ultra
22	IMG3O_LAST_ULTRA_EN	0: Disable last ultra 1: Enable last ultra
21	IMG2O_LAST_ULTRA_EN	0: Disable last ultra 1: Enable last ultra

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Bit(s)	Name	Description
20	IMG3CO_LAST_ULTRA_EN	0: Disable last ultra 1: Enable last ultra
19	IMG3BO_LAST_ULTRA_EN	0: Disable last ultra 1: Enable last ultra
18	MFBO_LAST_ULTRA_EN	0: Disable last ultra 1: Enable last ultra
17	UFEO_LAST_ULTRA_EN	0: Disable last ultra 1: Enable last ultra
16	AAO_LAST_ULTRA_EN	0: Disable last ultra 1: Enable last ultra
15	ESFKO_LAST_ULTRA_EN	0: Disable last ultra 1: Enable last ultra
14	LCSO_LAST_ULTRA_EN	0: Disable last ultra 1: Enable last ultra
13	RRZO_LAST_ULTRA_EN	0: Disable last ultra 1: Enable last ultra
12	IMGO_LAST_ULTRA_EN	0: Disable last ultra 1: Enable last ultra
3	LSCI_D_LAST_ULTRA_EN	0: Disable last ultra 1: Enable last ultra
2	BPCI_D_LAST_ULTRA_EN	0: Disable last ultra 1: Enable last ultra
1	LSCI_LAST_ULTRA_EN	0: Disable last ultra 1: Enable last ultra
0	BPCI_LAST_ULTRA_EN	0: Disable last ultra 1: Enable last ultra

1500722C **CAM_IMGI_SLOW_DOWN** **DMA IMGI Slow Down Register** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SLOW_EN	INTERLACE_MODE	UFO_IMGI_EN	UFO_IMGO_EN	CQ_ULTRA_IMGI_EN	CQ_ULTRA_LSCI_EN	CONTINUOUS_COM_EN	CONTINUOUS_COM_CON								IMGO_RRZO_SRAM_CHANGE_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW								RW
Reset	0	0	0	0	0	0	0	0	0							0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SLOW_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31	SLOW_EN	0: Original RDMA setting 1: Enable RDMA slow-down
30	INTERLACE_MOD	0: Original RDMA setting

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Bit(s)	Name	Description
	E	1: Enable RDMA interlace mode
29	UFO_IMGI_EN	0: Original RDMA setting 1: Enable UFO function
28	UFO_IMGO_EN	0: Original RDMA setting 1: Enable UFO function
27	CQ_ULTRA_IMGI_EN	0: Original setting 1: Enable CQ ultra IMGI function
26	CQ_ULTRA_LSCI_EN	0: Original setting 1: Enable CQ ultra LSCI function
25	CONTINUOUS_COM_EN	0: Original setting 1: Enable continuous command
24:23	CONTINUOUS_COM_CON	**Selects continuous command counter**
16	IMGO_RRZO_SRAM_CHANGE_EN	0: Original setting 1: Enable IMGO/RRZO SRAM change
15:0	SLOW_CNT	**The request will not be continuous and the interval is controlled by this register.** Unit: Engine clock cycle time

15007230 **CAM_IMGI_BASE_ADDR** **DMA Base ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASE_ADDR[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame After GDMA MCU mode, the register must be re-programmed.

15007234 **CAM_IMGI_OFST_ADDR** **DMA Offset ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OFFSET_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFFSET_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame**

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Bit(s)	Name	Description
		(dipi_base_addr+dipi_offset_addr=tile_start_addr)

15007238 **CAM_IMGI_XSIZE** **DMA XSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XSIZE															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to read

1500723C **CAM_IMGI_YSIZE** **DMA YSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				YSIZE												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	YSIZE	**Double buffer** (Number - 1) of lines to read

15007240 **CAM_IMGI_STRIDE** **DMA Stride** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SWAP							BUS_SIZE_EN	FORMAT_EN		FORMAT		BUS_SIZE			
Type	RW							RW	RW		RW		RW			
Reset	0	0						0	0		0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		STRIDE														
Type		USER0														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	SWAP	**For YUV422 one plane:**

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Bit(s)	Name	Description
		0: UYVY (LSB -> MSB) 1: YUYV 2: VYUY 3: YVYU For RGB/UV one plane: 0, 1: RGB/UV (LSB -> MSB) 2, 3: BGR/VU For ARGB one plane: 0: ARGB (LSB -> MSB) 1: RGBA 2: ABGR 3: BGRA For others: No effect
24	BUS_SIZE_EN	0: Use HW auto setting 1: Enable SW BUS_SIZE setting
23	FORMAT_EN	0: Use HW auto setting 1: Enable SW FORMAT setting
21:20	FORMAT	01: YUV format 10: RGB format 00: Others
19:16	BUS_SIZE	0: 8-bit 1: 16-bit 2: 24-bit 3: 32-bit 5: 48-bit 7: 64-bit 15: 128-bit
14:0	STRIDE	**Double buffer** Memory address distance from n-th line start address to (n+1)-th line start address. Unit: Byte

15007248 <u>**CAM_IMGI_CON**</u> **DMA Control Register** **80A0A0A0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MAX_BURST_LEN**					**FIFO_PRI_THRH_MSB**	**FIFO_PRI_THRL_MSB**	**FIFO_SIZE_MSB**	**FIFO_PRI_THRH**							
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	1	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**FIFO_PRI_THRL**								**FIFO_SIZE**							
Type	W1								W1							
Reset	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.

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Bit(s)	Name	Description
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

1500724C **CAM_IMGI_CON2** **DMA Control Register 2** **00A0A000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							**FIFO_PRE_PRI_THRH_MSB**	**FIFO_PRE_PRI_THRL_MSB**	**FIFO_PRE_PRI_THRH**							
Type							W1	W1	W1							
Reset							0	0	1	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**FIFO_PRE_PRI_THRL**															
Type	W1															
Reset	1	0	1	0	0	0	0	0								

Bit(s)	Name	Description
25	FIFO_PRE_PRI_THRH_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_THRH	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

15007250 **CAM_BPCI_BASE_ADDR** **DMA Base ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**BASE_ADDR[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BASE_ADDR[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

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15007254 **CAM_BPCI_OFST_ADDR** **DMA Offset ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OFFSET_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFFSET_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

15007258 **CAM_BPCI_XSIZE** **DMA XSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													XSIZE[19:16]			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XSIZE[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to read

1500725C **CAM_BPCI_YSIZE** **DMA YSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				YSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	YSIZE	**Double buffer** (Number - 1) of lines to read

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15007260 **CAM_BPCI_STRIDE** **DMA Stride** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SWAP**							**BUS_SIZE_EN**	**FORMAT_EN**			**FORMAT**				**BUS_SIZE**
Type	RW							RW	RW			RW				RW
Reset	0	0						0	0			0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**STRIDE**													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	SWAP	**For YUV422 one plane:** 0: UYVY (LSB -> MSB) 1: YUYV 2: VYUY 3: YVYU For RGB/UV one plane: 0, 1: RGB (LSB -> MSB) 2, 3: BGR For others: No effect
24	BUS_SIZE_EN	0: Use HW auto setting 1: Enable SW BUS_SIZE setting
23	FORMAT_EN	0: Use HW auto setting 1: Enable SW FORMAT setting
20	FORMAT	0: Others 1: YUV format
16	BUS_SIZE	0: 8-bit 1: 16-bit
13:0	STRIDE	**Double buffer** Memory address distance from n-th line start address to (n+1)-th line start address. Unit: Byte

15007264 **CAM_BPCI_CON** **DMA Control Register** **80202020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MAX_BURST_LEN**					**FIFO_PRI_THRH_MSB**	**FIFO_PRI_THRL_MSB**	**FIFO_SIZE_MSB**	**FIFO_PRI_THRH**							
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**FIFO_PRI_THRL**								**FIFO_SIZE**							
Type	W1								W1							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

15007268 **CAM_BPCI_CON2** **DMA Control Register 2** **00202000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FIFO_PRE_PRI_THRH_MSB	FIFO_PRE_PRI_THRL_MSB	FIFO_PRE_PRI_THRH							
Type							W1	W1	W1							
Reset							0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRE_PRI_THRL															
Type	W1															
Reset	0	0	1	0	0	0	0	0								

Bit(s)	Name	Description
25	FIFO_PRE_PRI_THRH_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_THRH	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

1500726C **CAM_LSCI_BASE_ADDR** **DMA Base ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASE_ADDR[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

15007270 **CAM_LSCI_OFST_ADDR** **DMA Offset ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OFFSET_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFFSET_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

15007274 **CAM_LSCI_XSIZE** **DMA XSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XSIZE															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to read

15007278 **CAM_LSCI_YSIZE** **DMA YSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				YSIZE												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	YSIZE	**Double buffer** (Number - 1) of lines to read

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1500727C **CAM_LSCI_STRIDE** **DMA Stride** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SWAP**							**BUS_SIZE_EN**	**FORMAT_EN**			**FORMAT**		**BUS_SIZE**		
Type	RW							RW	RW			RW		RW		
Reset	0	0						0	0			0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**STRIDE**													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	SWAP	**For YUV422 one plane:** 0: UYVY (LSB -> MSB) 1: YUYV 2: VYUY 3: YVYU For RGB/UV one plane: 0, 1: RGB (LSB -> MSB) 2, 3: BGR For others: No effect
24	BUS_SIZE_EN	0: Use HW auto setting 1: Enable SW BUS_SIZE setting
23	FORMAT_EN	0: Use HW auto setting 1: Enable SW FORMAT setting
20	FORMAT	0: Others 1: YUV format
18:16	BUS_SIZE	0: 8-bit 1: 16-bit 3: 32-bit 7: 64-bit
13:0	STRIDE	**Double buffer** Memory address distance from n-th line start address to (n+1)-th line start address. Unit: Byte

15007280 **CAM_LSCI_CON** **DMA Control Register** **80202020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MAX_BURST_LEN**					**FIFO_PRI_THRH_MSB**	**FIFO_PRI_THRL_MSB**	**FIFO_SIZE_MSB**	**FIFO_PRI_THRH**							
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**FIFO_PRI_THRL**								**FIFO_SIZE**							
Type	W1								W1							

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Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

15007284 **CAM_LSCI_CON2** **DMA Control Register 2** **00202000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FIFO_PRE_PRI_THRH_MSB	FIFO_PRE_PRI_THRL_MSB	FIFO_PRE_PRI_THRH							
Type							W1	W1	W1							
Reset							0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRE_PRI_THRL															
Type	W1															
Reset	0	0	1	0	0	0	0	0								

Bit(s)	Name	Description
25	FIFO_PRE_PRI_THRH_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_THRH	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

15007288 **CAM_UFDI_BASE_ADDR** **DMA Base ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASE_ADDR[15:0]															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

1500728C **CAM_UFDI_OFST_ADDR** **DMA Offset ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**OFFSET_ADDR[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**OFFSET_ADDR[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

15007290 **CAM_UFDI_XSIZE** **DMA XSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**XSIZE**													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to read

15007294 **CAM_UFDI_YSIZE** **DMA YSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**YSIZE**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
12:0	YSIZE	**Double buffer** (Number - 1) of lines to read

15007298 CAM_UFDI_STRIDE DMA Stride 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SWAP**							**BUS_SIZE_EN**	**FORMAT_EN**			**FORMAT**	**BUS_SIZE**			
Type	RW							RW	RW			RW	RW			
Reset	0	0						0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**STRIDE**													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	SWAP	**Reserved**
24	BUS_SIZE_EN	0: Use HW auto setting 1: Enable SW BUS_SIZE setting
23	FORMAT_EN	0: Use HW auto setting 1: Enable SW FORMAT setting
20	FORMAT	0: Others 1: YUV format
19:16	BUS_SIZE	0: 8-bit 1: 16-bit 15: 128-bit
13:0	STRIDE	**Double buffer** Memory address distance from n-th line start address to (n+1)-th line start address. Unit: Byte

1500729C CAM_UFDI_CON DMA Control Register 80202020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MAX_BURST_LEN**					**FIFO_PRI_THRH_MSB**	**FIFO_PRI_THRL_MSB**	**FIFO_SIZE_MSB**	**FIFO_PRI_THRH**							
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**FIFO_PRI_THRL**								**FIFO_SIZE**							
Type	W1								W1							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

150072A0 **CAM_UFDI_CON2** **DMA Control Register 2** **00202000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FIFO_PRE_PRI_THRH_MSB	FIFO_PRE_PRI_THRL_MSB	FIFO_PRE_PRI_THRH							
Type							W1	W1	W1							
Reset							0	0	0	0	1	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FIFO_PRE_PRI_THRL															
Type	W1															
Reset	0	0	1	0	0	0	0	0								

Bit(s)	Name	Description
25	FIFO_PRE_PRI_THRH_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_THRH	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

150072A4 **CAM_LCEI_BASE_ADDR** **DMA Base ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	BASE_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

150072A8 **CAM_LCEI_OFST_ADDR** **DMA Offset ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OFFSET_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFFSET_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

150072AC **CAM_LCEI_XSIZE** **DMA XSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			XSIZE													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to read

150072B0 **CAM_LCEI_YSIZE** **DMA YSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				YSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	YSIZE	**Double buffer** (Number - 1) of lines to read

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150072B4 **CAM_LCEI_STRIDE** **DMA Stride** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SWAP**							**BUS_SIZE_EN**	**FORMAT_EN**			**FORMAT**				**BUS_SIZE**
Type	RW							RW	RW			RW				RW
Reset	0	0						0	0			0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**STRIDE**													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	SWAP	**For YUV422 one plane:** 0: UYVY (LSB -> MSB) 1: YUYV 2: VYUY 3: YVYU For RGB/UV one plane: 0, 1: RGB (LSB -> MSB) 2, 3: BGR For others: No effect
24	BUS_SIZE_EN	0: Use HW auto setting 1: Enable SW BUS_SIZE setting
23	FORMAT_EN	0: Use HW auto setting 1: Enable SW FORMAT setting
20	FORMAT	0: Others 1: YUV format
16	BUS_SIZE	0: 8-bit 1: 16-bit
13:0	STRIDE	**Double buffer** Memory address distance from n-th line start address to (n+1)-th line start address. Unit: Byte

150072B8 **CAM_LCEI_CON** **DMA Control Register** **80202020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MAX_BURST_LEN**					**FIFO_PRI_THRH_MSB**	**FIFO_PRI_THRL_MSB**	**FIFO_SIZE_MSB**	**FIFO_PRI_THRH**							
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**FIFO_PRI_THRL**								**FIFO_SIZE**							
Type	W1								W1							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

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Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

150072BC **CAM_LCEI_CON2** **DMA Control Register 2** **00202000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FIFO_PRE_PRI_THRH_MSB	FIFO_PRE_PRI_THRL_MSB	FIFO_PRE_PRI_THRH							
Type							W1	W1	W1							
Reset							0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRE_PRI_THRL															
Type	W1															
Reset	0	0	1	0	0	0	0	0								

Bit(s)	Name	Description
25	FIFO_PRE_PRI_THRH_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_THRH	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

150072C0 **CAM_VIPI_BASE_ADDR** **DMA Base ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASE_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame After GDMA mcu mode, the register must be re-programmed.

150072C4 <u>CAM_VIPI_OFST_ADDR</u> **DMA Offset ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OFFSET_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFFSET_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

150072C8 <u>CAM_VIPI_XSIZE</u> **DMA XSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			XSIZE													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to read

150072CC <u>CAM_VIPI_YSIZE</u> **DMA YSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				YSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
12:0	YSIZE	**Double buffer** (Number - 1) of lines to read

150072D0 CAM_VIPI_STRIDE DMA Stride 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SWAP							BUS_SIZE_EN	FORMAT_EN		FORMAT					BUS_SIZE
Type	RW							RW	RW		RW					RW
Reset	0	0						0	0		0	0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			STRIDE													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	SWAP	**For YUV422 one plane:** 0: UYVY (LSB -> MSB) 1: YUYV 2: VYUY 3: YVYU For RGB/UV one plane: 0, 1: RGB (LSB -> MSB) 2, 3: BGR For others: No effect
24	BUS_SIZE_EN	0: Use HW auto setting 1: Enable SW BUS_SIZE setting
23	FORMAT_EN	0: Use HW auto setting 1: Enable SW FORMAT setting
21:20	FORMAT	01: YUV format 10: UV repeat (420->422) 00: Others
16	BUS_SIZE	0: 8-bit 1: 16-bit
13:0	STRIDE	**Double buffer** Memory address distance from n-th line start address to (n+1)-th line start address. Unit: Byte

150072D8 CAM_VIPI_CON DMA Control Register 80505050

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BURST_LEN					FIFO_PRI_THRH_MSB	FIFO_PRI_THRL_MSB	FIFO_SIZE_MSB	FIFO_PRI_THRH							
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	0	1	0	1	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRI_THRL								FIFO_SIZE							
Type	W1								W1							
Reset	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

150072DC **CAM_VIPI_CON2** **DMA Control Register 2** **00505000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FIFO_PRE_PRI_THRH_MSB	FIFO_PRE_PRI_THRL_MSB	FIFO_PRE_PRI_THRH							
Type							W1	W1	W1							
Reset							0	0	0	1	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRE_PRI_THRL															
Type	W1															
Reset	0	1	0	1	0	0	0	0								

Bit(s)	Name	Description
25	FIFO_PRE_PRI_THRH_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_THRH	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

150072E0 **CAM_VIP2I_BASE_ADDR** **DMA Base ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASE_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame After GDMA mcu mode, the register must be re-programmed.

150072E4 **CAM_VIP2I_OFST_ADDR** **DMA Offset ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OFFSET_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFFSET_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

150072E8 **CAM_VIP2I_XSIZE** **DMA XSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			XSIZE													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to read

150072EC **CAM_VIP2I_YSIZE** **DMA YSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				YSIZE												
Type				RW												

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Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	YSIZE	**Double buffer** (Number - 1) of lines to read

150072F0 CAM_VIP2I_STRIDE DMA Stride 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SWAP							BUS_SIZE_EN	FORMAT_EN		FORMAT					BUS_SIZE
Type	RW							RW	RW		RW					RW
Reset	0	0						0	0		0	0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			STRIDE													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	SWAP	**for UV one plane:** 0,1 : UV (LSB -> MSB) 2,3 : VU For others: No effect
24	BUS_SIZE_EN	0: Use HW auto setting 1: Enable SW BUS_SIZE setting
23	FORMAT_EN	0: Use HW auto setting 1: Enable SW FORMAT setting
21:20	FORMAT	01: YUV format 10: UV repeat (420->422) 00: Others
16	BUS_SIZE	0: 8-bit 1: 16-bit
13:0	STRIDE	**Double buffer** Memory address distance from n-th line start address to (n+1)-th line start address. Unit: Byte

150072F8 CAM_VIP2I_CON DMA Control Register 80404040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BURST_LEN					FIFO_PRI_THRH_MSB	FIFO_PRI_THRL_MSB	FIFO_SIZE_MSB	FIFO_PRI_THRH							
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRI_THRL								FIFO_SIZE							

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Type	W1								W1							
Reset	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

150072FC **CAM_VIP2I_CON2** **DMA Control Register 2** **00404000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FIFO_PRE_PRI_THRH_MSB	FIFO_PRE_PRI_THRL_MSB	FIFO_PRE_PRI_THRH							
Type							W1	W1	W1							
Reset							0	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRE_PRI_THRL															
Type	W1															
Reset	0	1	0	0	0	0	0	0								

Bit(s)	Name	Description
25	FIFO_PRE_PRI_THRH_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_THRH	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

15007300 **CAM_IMGO_BASE_ADDR** **DMA Base ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BASE_ADDR[15:0]**															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

15007304 **CAM_IMGO_OFST_ADDR** **DMA Offset ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**OFFSET_ADDR[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**OFFSET_ADDR[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

15007308 **CAM_IMGO_XSIZE** **DMA XSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**XSIZE**													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to write

1500730C **CAM_IMGO_YSIZE** **DMA YSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**YSIZE**												
Type				USER0												

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Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	YSIZE	**Double buffer** (Number - 1) of lines to write

15007310 **CAM_IMGO_STRIDE** **DMA Stride** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								**BUS_SIZE_EN**	**FORMAT_EN**		**FORMAT**				**BUS_SIZE**	
Type								RW	RW		RW				RW	
Reset								0	0		0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**STRIDE**													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24	BUS_SIZE_EN	0: Use HW auto setting 1: Enable SW FORMAT setting
23	FORMAT_EN	0: Use HW auto setting 1: Enable SW FORMAT setting
21:20	FORMAT	01: YUV format 10: JPG format 00: Others
17:16	BUS_SIZE	0: 8-bit 1: 16-bit 2: 24-bit 3: 32-bit
13:0	STRIDE	**Double buffer** Memory address distance from n-th line start address to (n+1)-th line start address. Unit: Byte

15007314 **CAM_IMGO_CON** **DMA Control Register** **80B0B0B0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MAX_BURST_LEN**					**FIFO_PRI_THRH_MSB**	**FIFO_PRI_THRL_MSB**	**FIFO_SIZE_MSB**	**FIFO_PRI_THRH**							
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	1	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**FIFO_PRI_THRL**								**FIFO_SIZE**							
Type	W1								W1							
Reset	1	0	1	1	0	0	0	0	1	0	1	1	0	0	0	0

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Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

15007318 **CAM_IMGO_CON2** **DMA Control Register 2** **00B0B000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FIFO_PRE_PRI_THRH_MSB	FIFO_PRE_PRI_THRL_MSB	FIFO_PRE_PRI_THRH							
Type							W1	W1	W1							
Reset							0	0	1	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRE_PRI_THRL															
Type	W1															
Reset	1	0	1	1	0	0	0	0								

Bit(s)	Name	Description
25	FIFO_PRE_PRI_THRH_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_THRH	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

1500731C **CAM_IMGO_CROP** **DMA Crop Function Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				YOFFSET												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			XOFFSET													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
28:16	YOFFSET	**Double buffer** Number of pixels to be discarded from top of the line
13:0	XOFFSET	**Double buffer** Number of pixels to be discarded from the left of the line

15007320 **CAM_RRZO_BASE_ADDR** **DMA Base ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASE_ADDR[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

15007324 **CAM_RRZO_OFST_ADDR** **DMA Offset ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OFFSET_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFFSET_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

15007328 **CAM_RRZO_XSIZE** **DMA XSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			XSIZE													
Type			USER0													

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Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to write

1500732C **CAM_RRZO_YSIZE** **DMA YSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**YSIZE**												
Type				USERO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	YSIZE	**Double buffer** (Number - 1) of lines to write

15007330 **CAM_RRZO_STRIDE** **DMA Stride** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								**BUS_SIZE_EN**	**FORMAT_EN**		**FORMAT**			**BUS_SIZE**		
Type								RW	RW		RW			RW		
Reset								0	0		0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**STRIDE**													
Type			USERO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24	BUS_SIZE_EN	0: Use HW auto setting 1: Enable SW FORMAT setting
23	FORMAT_EN	0: Use HW auto setting 1: Enable SW FORMAT setting
21:20	FORMAT	01: YUV format 10: JPG format 00: Others
18:16	BUS_SIZE	0: 8-bit 1: 16-bit 2: 24-bit 3: 32-bit 7: 64-bit
13:0	STRIDE	**Double buffer** Memory address distance from n-th line start address to (n+1)-th line start address.

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Bit(s)	Name	Description
		Unit: Byte

15007334 **CAM_RRZO_CON** **DMA Control Register** **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BURST_LEN					FIFO_PRI_THRH_MSB	FIFO_PRI_THRL_MSB	FIFO_SIZE_MSB	FIFO_PRI_THRH							
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRI_THRL								FIFO_SIZE							
Type	W1								W1							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

15007338 **CAM_RRZO_CON2** **DMA Control Register 2** **00808000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FIFO_PRE_PRI_THRH_MSB	FIFO_PRE_PRI_THRL_MSB	FIFO_PRE_PRI_THRH							
Type							W1	W1	W1							
Reset							0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRE_PRI_THRL															
Type	W1															
Reset	1	0	0	0	0	0	0	0								

Bit(s)	Name	Description
25	FIFO_PRE_PRI_THRH_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.

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Bit(s)	Name	Description
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_THRH	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

1500733C CAM_RRZO_CROP DMA Crop Function Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				YOFFSET												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			XOFFSET													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	YOFFSET	**Double buffer** Number of pixels to be discarded from top of the line
13:0	XOFFSET	**Double buffer** Number of pixels to be discarded from the left of the line

15007340 CAM_LCSO_BASE_ADDR DMA Base ADDR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASE_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

15007344 CAM_LCSO_OFST_ADDR DMA Offset ADDR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OFFSET_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFFSET_ADDR[15:0]															

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Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

15007348 CAM_LCSO_XSIZE DMA XSIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**XSIZE**													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to write

1500734C CAM_LCSO_YSIZE DMA YSIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**YSIZE**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	YSIZE	**Double buffer** (Number - 1) of lines to write

15007350 CAM_LCSO_STRIDE DMA Stride 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**STRIDE**													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
13:0	STRIDE	**Double buffer** Memory address distance from n-th line start address to (n+1)-th line start address. Unit: Byte

15007354 **CAM_LCSO_CON** **DMA Control Register** **80202020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MAX_BURST_LEN**					**FIFO_PRI_THRH_MSB**	**FIFO_PRI_THRL_MSB**	**FIFO_SIZE_MSB**	**FIFO_PRI_THRH**							
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**FIFO_PRI_THRL**								**FIFO_SIZE**							
Type	W1								W1							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

15007358 **CAM_LCSO_CON2** **DMA Control Register 2** **00202000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							**FIFO_PRE_PRI_THRH_MSB**	**FIFO_PRE_PRI_THRL_MSB**	**FIFO_PRE_PRI_THRH**							
Type							W1	W1	W1							
Reset							0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**FIFO_PRE_PRI_THRL**															
Type	W1															
Reset	0	0	1	0	0	0	0	0								

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Bit(s)	Name	Description
25	FIFO_PRE_PRI_THRH_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_THRH	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

1500735C CAM_EISO_BASE_ADDR DMA Base ADDR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASE_ADDR[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

15007360 CAM_EISO_XSIZE DMA XSIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							XSIZE									
Type							USER0									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to write

15007364 CAM_AFO_BASE_ADDR DMA Base ADDR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	BASE_ADDR[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

15007368 **CAM_AFO_XSIZE** **DMA XSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							XSIZE									
Type							USER0									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to write

1500736C **CAM_ESFKO_BASE_ADDR** **DMA Base ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASE_ADDR[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

15007370 **CAM_ESFKO_XSIZE** **DMA XSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XSIZE															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to write

15007374 **CAM_ESFKO_OFST_ADDR** **DMA Offset ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OFFSET_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFFSET_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

15007378 **CAM_ESFKO_YSIZE** **DMA YSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RSV												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	RSV	**Double buffer** (Number - 1) of lines to write

1500737C **CAM_ESFKO_STRIDE** **DMA Stride** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RSV													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
13:0	RSV	**Double buffer** Memory address distance from n-th line start address to (n+1)-th line start address. Unit: Byte

15007380 CAM_ESFKO_CON DMA Control Register 80202020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BURST_LEN					FIFO_PRI_THRH_MSB	FIFO_PRI_THRL_MSB	FIFO_SIZE_MSB	FIFO_PRI_THRH							
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRI_THRL								FIFO_SIZE							
Type	W1								W1							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

15007384 CAM_ESFKO_CON2 DMA Control Register 2 00202000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FIFO_PRE_PRI_THRH_MSB	FIFO_PRE_PRI_THRL_MSB	FIFO_PRE_PRI_THRH							
Type							W1	W1	W1							
Reset							0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRE_PRI_THRL															
Type	W1															
Reset	0	0	1	0	0	0	0	0								

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Bit(s)	Name	Description
25	FIFO_PRE_PRI_THRH_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_THRH	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

15007388 **CAM_AAO_BASE_ADDR** **DMA Base ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASE_ADDR[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

1500738C **CAM_AAO_OFST_ADDR** **DMA Offset ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OFFSET_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFFSET_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

15007390 **CAM_AAO_XSIZE** **DMA XSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																XSIZE[16:16]
Type																USER0

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Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**XSIZE[15:0]**															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to write

15007394 CAM_AAO_YSIZE DMA YSIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**RSV**												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	RSV	**Double buffer** (Number - 1) of lines to write

15007398 CAM_AAO_STRIDE DMA Stride 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								**BUS_SIZE_EN**							**BUS_SIZE**	
Type								RW							RW	
Reset								0							0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**RSV**													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24	BUS_SIZE_EN	0: Use HW auto setting 1: Enable SW BUS_SIZE setting
17:16	BUS_SIZE	1: 16-bit 3: 32-bit
13:0	RSV	**Double buffer** Memory address distance from n-th line start address to (n+1)-th line start address. Unit: Byte

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1500739C CAM_AAO_CON DMA Control Register 80202020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BURST_LEN					FIFO_PRI_THRH_MSB	FIFO_PRI_THRL_MSB	FIFO_SIZE_MSB	FIFO_PRI_THRH							
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRI_THRL								FIFO_SIZE							
Type	W1								W1							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

150073A0 CAM_AAO_CON2 DMA Control Register 2 00202000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FIFO_PRE_PRI_THRH_MSB	FIFO_PRE_PRI_THRL_MSB	FIFO_PRE_PRI_THRH							
Type							W1	W1	W1							
Reset							0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRE_PRI_THRL															
Type	W1															
Reset	0	0	1	0	0	0	0	0								

Bit(s)	Name	Description
25	FIFO_PRE_PRI_THRH_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_THRH	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.

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Bit(s)	Name	Description
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

150073A4 CAM_VIP3I_BASE_ADDR DMA Base ADDR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASE_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame After GDMA mcu mode, the register must be re-programmed.

150073A8 CAM_VIP3I_OFST_ADDR DMA Offset ADDR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OFFSET_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFFSET_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

150073AC CAM_VIP3I_XSIZE DMA XSIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			XSIZE													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	XSIZE	**Double buffer**

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Bit(s)	Name	Description
		(Number - 1) of bytes per line to read

150073B0 **CAM_VIP3I_YSIZE** **DMA YSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				YSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	YSIZE	**Double buffer** (Number - 1) of lines to read

150073B4 **CAM_VIP3I_STRIDE** **DMA Stride** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SWAP							BUS_SIZE_EN	FORMAT_EN		FORMAT					BUS_SIZE
Type	RW							RW	RW		RW					RW
Reset	0	0						0	0		0	0				0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name			STRIDE													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	SWAP	**For UV one plane:** 0,1 : UV (LSB -> MSB) 2,3 : VU For others: No effect
24	BUS_SIZE_EN	0: Use HW auto setting 1: Enable SW BUS_SIZE setting
23	FORMAT_EN	0: Use HW auto setting 1: Enable SW FORMAT setting
21:20	FORMAT	01: YUV format 10: UV repeat (420->422) 00: Others
16	BUS_SIZE	0: 8-bit 1: 16-bit
13:0	STRIDE	**Double buffer** Memory address distance from n-th line start address to (n+1)-th line start address. Unit: Byte

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150073BC **CAM_VIP3I_CON** **DMA Control Register** **80404040**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BURST_LEN					FIFO_PRI_THRH_MSB	FIFO_PRI_THRL_MSB	FIFO_SIZE_MSB	FIFO_PRI_THRH							
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRI_THRL								FIFO_SIZE							
Type	W1								W1							
Reset	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

150073C0 **CAM_VIP3I_CON2** **DMA Control Register 2** **00404000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FIFO_PRE_PRI_THRH_MSB	FIFO_PRE_PRI_THRL_MSB	FIFO_PRE_PRI_THRH							
Type							W1	W1	W1							
Reset							0	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRE_PRI_THRL															
Type	W1															
Reset	0	1	0	0	0	0	0	0								

Bit(s)	Name	Description
25	FIFO_PRE_PRI_THRH_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_T	For pre-priority control signal: If FIFO amount is larger than THRH, priority

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Bit(s)	Name	Description
	HRH	control signal will be asserted.
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

150073C4 **CAM_UFEO_BASE_ADDR** **DMA Base ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASE_ADDR[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double Buffer.** start address of a frame

150073C8 **CAM_UFEO_OFST_ADDR** **DMA Offset ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OFFSET_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFFSET_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

150073CC **CAM_UFEO_XSIZE** **DMA XSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			XSIZE													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
13:0	XSIZE	**Double Buffer.** (Number - 1) of bytes per line to write.

150073D0 **CAM_UFEO_YSIZE** **DMA YSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**YSIZE**												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	YSIZE	**Double Buffer.** (Number - 1) of lines to write.

150073D4 **CAM_UFEO_STRIDE** **DMA Stride** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**STRIDE**													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	STRIDE	**Double buffer** Memory address distance from n-th line start address to (n+1)-th line start address. Unit: byte.

150073D8 **CAM_UFEO_CON** **DMA Control Register** **80202020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MAX_BURST_LEN**					**FIFO_PRI_THRH_MSB**	**FIFO_PRI_THRL_MSB**	**FIFO_SIZE_MSB**	**FIFO_PRI_THRH**							
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**FIFO_PRI_THRL**								**FIFO_SIZE**							
Type	W1								W1							

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Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

150073DC CAM_UFEO_CON2 DMA Control Register 2 00202000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FIFO_PRE_PRI_THRH_MSB	FIFO_PRE_PRI_THRL_MSB	FIFO_PRE_PRI_THRH							
Type							W1	W1	W1							
Reset							0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRE_PRI_THRL															
Type	W1															
Reset	0	0	1	0	0	0	0	0								

Bit(s)	Name	Description
25	FIFO_PRE_PRI_THRH_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_THRH	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

150073E0 CAM_MFBO_BASE_ADDR DMA Base ADDR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	BASE_ADDR[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

150073E4 **CAM_MFBO_OFST_ADDR** **DMA Offset ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OFFSET_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFFSET_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

150073E8 **CAM_MFBO_XSIZE** **DMA XSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			XSIZE													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to write

150073EC **CAM_MFBO_YSIZE** **DMA YSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				YSIZE												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
12:0	YSIZE	**Double buffer** (Number - 1) of lines to write

150073F0 **CAM_MFBO_STRIDE** **DMA Stride** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			STRIDE													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	STRIDE	**Double buffer** Memory address distance from n-th line start address to (n+1)-th line start address. Unit: Byte

150073F4 **CAM_MFBO_CON** **DMA Control Register** **80202020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BURST_LEN					FIFO_PRI_THRH_MSB	FIFO_PRI_THRL_MSB	FIFO_SIZE_MSB	FIFO_PRI_THRH							
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRI_THRL								FIFO_SIZE							
Type	W1								W1							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

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150073F8 **CAM_MFBO_CON2** **DMA Control Register 2** **00202000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FIFO_PRE_PRI_THRH_MSB	FIFO_PRE_PRI_THRL_MSB	FIFO_PRE_PRI_THRH							
Type							W1	W1	W1							
Reset							0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRE_PRI_THRL															
Type	W1															
Reset	0	0	1	0	0	0	0	0								

Bit(s)	Name	Description
25	FIFO_PRE_PRI_THRH_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_THRH	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

150073FC **CAM_MFBO_CROP** **DMA Crop Function Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				YOFFSET												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			XOFFSET													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	YOFFSET	**Double buffer** Number of pixels to be discarded from top of the line
13:0	XOFFSET	**Double buffer** Number of pixels to be discarded from the left of the line

15007400 **CAM_IMG3BO_BASE_ADDR** **DMA Base ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															

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Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BASE_ADDR[15:0]**															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

15007404 CAM_IMG3BO_OFST_ADDR DMA Offset ADDR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**OFFSET_ADDR[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**OFFSET_ADDR[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

15007408 CAM_IMG3BO_XSIZE DMA XSIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**XSIZE**													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to write

1500740C CAM_IMG3BO_YSIZE DMA YSIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name				**YSIZE**												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	YSIZE	**Double buffer** (Number - 1) of lines to write

15007410 CAM_IMG3BO_STRIDE DMA Stride 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								**BUS_SIZE_EN**	**FORMAT_EN**		**FORMAT**				**BUS_SIZE**	
Type								RW	RW		RW				RW	
Reset								0	0		0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**STRIDE**													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24	BUS_SIZE_EN	0: Use HW auto setting 1: Enable SW FORMAT setting
23	FORMAT_EN	0: Use HW auto setting 1: Enable SW FORMAT setting
21:20	FORMAT	01: YUV format 10: JPG format 00: Others
17:16	BUS_SIZE	0: 8-bit 1: 16-bit 2: 24-bit 3: 32-bit
13:0	STRIDE	**Double buffer** Memory address distance from n-th line start address to (n+1)-th line start address. Unit: Byte

15007414 CAM_IMG3BO_CON DMA Control Register 80202020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MAX_BURST_LEN**					**FIFO_PRI_THRH_MSB**	**FIFO_PRI_THRL_MSB**	**FIFO_SIZE_MSB**	**FIFO_PRI_THRH**							
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**FIFO_PRI_THRL**								**FIFO_SIZE**							
Type	W1								W1							

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Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

15007418 CAM_IMG3BO_CON2 DMA Control Register 2 00202000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							**FIFO_PRE_PRI_THRH_MSB**	**FIFO_PRE_PRI_THRL_MSB**	**FIFO_PRE_PRI_THRH**							
Type							W1	W1	W1							
Reset							0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**FIFO_PRE_PRI_THRL**															
Type	W1															
Reset	0	0	1	0	0	0	0	0								

Bit(s)	Name	Description
25	FIFO_PRE_PRI_THRH_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_THRH	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

1500741C CAM_IMG3BO_CROP DMA Crop Function Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**YOFFSET**												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**XOFFSET**													
Type			USER0													

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Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	YOFFSET	**Double buffer** Number of pixels to be discarded from top of the line
13:0	XOFFSET	**Double buffer** Number of pixels to be discarded from the left of the line

15007420 CAM_IMG3CO_BASE_ADDR DMA Base ADDR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASE_ADDR[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

15007424 CAM_IMG3CO_OFST_ADDR DMA Offset ADDR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OFFSET_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFFSET_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

15007428 CAM_IMG3CO_XSIZE DMA XSIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			XSIZE													

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Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to write

1500742C CAM_IMG3CO_YSIZE DMA YSIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**YSIZE**												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	YSIZE	**Double buffer** (Number - 1) of lines to write

15007430 CAM_IMG3CO_STRIDE DMA Stride 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								**BUS_SIZE_EN**	**FORMAT_EN**		**FORMAT**				**BUS_SIZE**	
Type								RW	RW		RW				RW	
Reset								0	0		0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**STRIDE**													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24	BUS_SIZE_EN	0: Use HW auto setting 1: Enable SW FORMAT setting
23	FORMAT_EN	0: Use HW auto setting 1: Enable SW FORMAT setting
21:20	FORMAT	01: YUV format 10: JPG format 00: Others
17:16	BUS_SIZE	0: 8-bit 1: 16-bit 2: 24-bit 3: 32-bit
13:0	STRIDE	**Double buffer** Memory address distance from n-th line start address to (n+1)-th line start address.

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Bit(s)	Name	Description
		Unit: Byte

15007434 **CAM_IMG3CO_CON** **DMA Control Register** **80202020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MAX_BURST_LEN**					**FIFO_PRI_THRH_MSB**	**FIFO_PRI_THRL_MSB**	**FIFO_SIZE_MSB**	**FIFO_PRI_THRH**							
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**FIFO_PRI_THRL**								**FIFO_SIZE**							
Type	W1								W1							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

15007438 **CAM_IMG3CO_CON2** **DMA Control Register 2** **00202000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							**FIFO_PRE_PRI_THRH_MSB**	**FIFO_PRE_PRI_THRL_MSB**	**FIFO_PRE_PRI_THRH**							
Type							W1	W1	W1							
Reset							0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**FIFO_PRE_PRI_THRL**															
Type	W1															
Reset	0	0	1	0	0	0	0	0								

Bit(s)	Name	Description
25	FIFO_PRE_PRI_THRH_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.

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Bit(s)	Name	Description
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_THRH	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

1500743C CAM_IMG3CO_CROP DMA Crop Function Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				YOFFSET												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			XOFFSET													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	YOFFSET	**Double buffer** Number of pixels to be discarded from top of the line
13:0	XOFFSET	**Double buffer** Number of pixels to be discarded from the left of the line

15007440 CAM_IMG2O_BASE_ADDR DMA Base ADDR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASE_ADDR[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

15007444 CAM_IMG2O_OFST_ADDR DMA Offset ADDR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OFFSET_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFFSET_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

15007448 CAM_IMG2O_XSIZE DMA XSIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name			XSIZE													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to write

1500744C CAM_IMG2O_YSIZE DMA YSIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				YSIZE												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	YSIZE	**Double buffer** (Number - 1) of lines to write

15007450 CAM_IMG2O_STRIDE DMA Stride 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								BUS_SIZE_EN	FORMAT_EN		FORMAT				BUS_SIZE	
Type								RW	RW		RW				RW	
Reset								0	0		0	0			0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

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Name			STRIDE													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24	BUS_SIZE_EN	0: Use HW auto setting 1: Enable SW FORMAT setting
23	FORMAT_EN	0: Use HW auto setting 1: Enable SW FORMAT setting
21:20	FORMAT	01: YUV format 10: JPG format 00: Others
17:16	BUS_SIZE	0: 8-bit 1: 16-bit 2: 24-bit 3: 32-bit
13:0	STRIDE	**Double buffer** Memory address distance from n-th line start address to (n+1)-th line start address. Unit: Byte

15007454 **CAM_IMG2O_CON** **DMA Control Register** **80606060**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BURST_LEN					FIFO_PRI_THRH_MSB	FIFO_PRI_THRL_MSB	FIFO_SIZE_MSB	FIFO_PRI_THRH							
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	0	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRI_THRL								FIFO_SIZE							
Type	W1								W1							
Reset	0	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

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15007458 CAM_IMG2O_CON2 DMA Control Register 2 00606000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FIFO_PRE_PRI_THRH_MSB	FIFO_PRE_PRI_THRL_MSB	FIFO_PRE_PRI_THRH							
Type							W1	W1	W1							
Reset							0	0	0	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRE_PRI_THRL															
Type	W1															
Reset	0	1	1	0	0	0	0	0								

Bit(s)	Name	Description
25	FIFO_PRE_PRI_THRH_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_THRH	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

1500745C CAM_IMG2O_CROP DMA Crop Function Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				YOFFSET												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			XOFFSET													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	YOFFSET	**Double buffer** Number of pixels to be discarded from top of the line
13:0	XOFFSET	**Double buffer** Number of pixels to be discarded from the left of the line

15007460 CAM_IMG3O_BASE_ADDR DMA Base ADDR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	**BASE_ADDR[15:0]**															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

15007464 **CAM_IMG3O_OFST_ADDR** **DMA Offset ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**OFFSET_ADDR[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**OFFSET_ADDR[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

15007468 **CAM_IMG3O_XSIZE** **DMA XSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**XSIZE**													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to write

1500746C **CAM_IMG3O_YSIZE** **DMA YSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**YSIZE**												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
12:0	YSIZE	**Double buffer** (Number - 1) of lines to write

15007470 **CAM_IMG3O_STRIDE** **DMA Stride** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								BUS_SIZE_EN	FORMAT_EN		FORMAT				BUS_SIZE	
Type								RW	RW		RW				RW	
Reset								0	0		0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			STRIDE													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24	BUS_SIZE_EN	0: Use HW auto setting 1: Enable SW FORMAT setting
23	FORMAT_EN	0: Use HW auto setting 1: Enable SW FORMAT setting
21:20	FORMAT	01: YUV format 10: JPG format 00: Others
17:16	BUS_SIZE	0: 8-bit 1: 16-bit 2: 24-bit 3: 32-bit
13:0	STRIDE	**Double buffer** Memory address distance from n-th line start address to (n+1)-th line start address. Unit: Byte

15007474 **CAM_IMG3O_CON** **DMA Control Register** **80404040**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BURST_LEN					FIFO_PRI_THRH_MSB	FIFO_PRI_THRL_MSB	FIFO_SIZE_MSB	FIFO_PRI_THRH							
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRI_THRL								FIFO_SIZE							
Type	W1								W1							
Reset	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0

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Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

15007478 **CAM_IMG3O_CON2** **DMA Control Register 2** **00404000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FIFO_PRE_PRI_THRH_MSB	FIFO_PRE_PRI_THRL_MSB	FIFO_PRE_PRI_THRH							
Type							W1	W1	W1							
Reset							0	0	0	1	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FIFO_PRE_PRI_THRL															
Type	W1															
Reset	0	1	0	0	0	0	0	0								

Bit(s)	Name	Description
25	FIFO_PRE_PRI_THRH_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_THRH	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

1500747C **CAM_IMG3O_CROP** **DMA Crop Function Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				YOFFSET												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name			XOFFSET													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
28:16	YOFFSET	**Double buffer** Number of pixels to be discarded from top of the line
13:0	XOFFSET	**Double buffer** Number of pixels to be discarded from the left of the line

15007480 CAM_FEO_BASE_ADDR DMA Base ADDR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASE_ADDR[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

15007484 CAM_FEO_OFST_ADDR DMA Offset ADDR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OFFSET_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFFSET_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

15007488 CAM_FEO_XSIZE DMA XSIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XSIZE															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
15:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to write

1500748C CAM_FEO_YSIZE DMA YSIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				YSIZE												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	YSIZE	**Double buffer** (Number - 1) of lines to write

15007490 CAM_FEO_STRIDE DMA Stride 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	STRIDE															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	STRIDE	0: Use HW auto setting 1: Enable SW FORMAT setting

15007494 CAM_FEO_CON DMA Control Register 80202020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BURST_LEN					FIFO_PRI_THRH_MSB	FIFO_PRI_THRL_MSB	FIFO_SIZE_MSB	FIFO_PRI_THRH							
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	0	0	1	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FIFO_PRI_THRL								FIFO_SIZE							
Type	W1								W1							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

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Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

15007498 **CAM_FEO_CON2** **DMA Control Register 2** **00202000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FIFO_PRE_PRI_THRH_MSB	FIFO_PRE_PRI_THRL_MSB	FIFO_PRE_PRI_THRH							
Type							W1	W1	W1							
Reset							0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRE_PRI_THRL															
Type	W1															
Reset	0	0	1	0	0	0	0	0								

Bit(s)	Name	Description
25	FIFO_PRE_PRI_THRH_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_THRH	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

1500749C **CAM_BPCI_D_BASE_ADDR** **DMA Base ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASE_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

150074A0 **CAM_BPCI_D_OFST_ADDR** **DMA Offset ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OFFSET_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFFSET_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

150074A4 **CAM_BPCI_D_XSIZE** **DMA XSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													XSIZE[19:16]			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XSIZE[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to read

150074A8 **CAM_BPCI_D_YSIZE** **DMA YSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				YSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
12:0	YSIZE	**Double buffer** (Number - 1) of lines to read

150074AC CAM_BPCI_D_STRIDE DMA Stride 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SWAP							BUS_SIZE_EN	FORMAT_EN			FORMAT				BUS_SIZE
Type	RW							RW	RW			RW				RW
Reset	0	0						0	0			0				0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name			STRIDE													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	SWAP	**For YUV422 one plane:** 0: UYVY (LSB -> MSB) 1: YUYV 2: VYUY 3: YVYU For RGB/UV one plane: 0, 1: RGB (LSB -> MSB) 2, 3: BGR For others: No effect
24	BUS_SIZE_EN	0: Use HW auto setting 1: Enable SW BUS_SIZE setting
23	FORMAT_EN	0: Use HW auto setting 1: Enable SW FORMAT setting
20	FORMAT	0: Others 1: YUV format
16	BUS_SIZE	0: 8-bit 1: 16-bit
13:0	STRIDE	**Double buffer** Memory address distance from n-th line start address to (n+1)-th line start address. Unit: Byte

150074B0 CAM_BPCI_D_CON DMA Control Register 80202020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BURST_LEN					FIFO_PRI_THRH_MSB	FIFO_PRI_THRL_MSB	FIFO_SIZE_MSB	FIFO_PRI_THRH							
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	0	0	1	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

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Name	FIFO_PRI_THRL								FIFO_SIZE							
Type	W1								W1							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

150074B4 **CAM_BPCI_D_CON2** **DMA Control Register 2** **00202000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FIFO_PRE_PRI_THRH_MSB	FIFO_PRE_PRI_THRL_MSB	FIFO_PRE_PRI_THRH							
Type							W1	W1	W1							
Reset							0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRE_PRI_THRL															
Type	W1															
Reset	0	0	1	0	0	0	0	0								

Bit(s)	Name	Description
25	FIFO_PRE_PRI_THRH_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_THRH	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

150074B8 **CAM_LSCI_D_BASE_ADDR** **DMA Base ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	USER0															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASE_ADDR[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

150074BC **CAM_LSCI_D_OFST_ADDR** **DMA Offset ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OFFSET_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFFSET_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

150074C0 **CAM_LSCI_D_XSIZE** **DMA XSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XSIZE															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to read

150074C4 **CAM_LSCI_D_YSIZE** **DMA YSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				YSIZE												

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Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	YSIZE	**Double buffer** (Number - 1) of lines to read

150074C8 CAM_LSCI_D_STRIDE DMA Stride 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SWAP**							**BUS_SIZE_EN**	**FORMAT_EN**			**FORMAT**		**BUS_SIZE**		
Type	RW							RW	RW			RW		RW		
Reset	0	0						0	0			0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**STRIDE**													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	SWAP	**For YUV422 one plane:** 0: UYVY (LSB -> MSB) 1: YUYV 2: VYUY 3: YVYU For RGB/UV one plane: 0, 1: RGB (LSB -> MSB) 2, 3: BGR For others: No effect
24	BUS_SIZE_EN	0: Use HW auto setting 1: Enable SW BUS_SIZE setting
23	FORMAT_EN	0: Use HW auto setting 1: Enable SW FORMAT setting
20	FORMAT	0: Others 1: YUV format
18:16	BUS_SIZE	0: 8-bit 1: 16-bit 3: 32-bit 7: 64-bit
13:0	STRIDE	**Double buffer** Memory address distance from n-th line start address to (n+1)-th line start address. Unit: Byte

150074CC CAM_LSCI_D_CON DMA Control Register 80202020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MAX_BURST_LEN**					**FIFO_PRI_**	**FIFO_PRI_**	**FIFO_SIZE**	**FIFO_PRI_THRH**							

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						THRH_MSB	THRL_MSB	_MSB								
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRI_THRL								FIFO_SIZE							
Type	W1								W1							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

150074D0 CAM_LSCI_D_CON2 DMA Control Register 2 00202000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FIFO_PRE_PRI_THRH_MSB	FIFO_PRE_PRI_THRL_MSB	FIFO_PRE_PRI_THRH							
Type							W1	W1	W1							
Reset							0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRE_PRI_THRL															
Type	W1															
Reset	0	0	1	0	0	0	0	0								

Bit(s)	Name	Description
25	FIFO_PRE_PRI_THRH_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_THRH	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

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150074D4 **CAM_IMGO_D_BASE_ADDR** **DMA Base ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASE_ADDR[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

150074D8 **CAM_IMGO_D_OFST_ADDR** **DMA Offset ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OFFSET_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFFSET_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

150074DC **CAM_IMGO_D_XSIZE** **DMA XSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			XSIZE													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to write

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150074E0 **CAM_IMGO_D_YSIZE** **DMA YSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				YSIZE												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	YSIZE	**Double buffer** (Number - 1) of lines to write

150074E4 **CAM_IMGO_D_STRIDE** **DMA Stride** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								BUS_SIZE_EN	FORMAT_EN		FORMAT				BUS_SIZE	
Type								RW	RW		RW				RW	
Reset								0	0		0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			STRIDE													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24	BUS_SIZE_EN	0: Use HW auto setting 1: Enable SW BUS_SIZE setting
23	FORMAT_EN	0: Use HW auto setting 1: Enable SW FORMAT setting
21:20	FORMAT	01: YUV format 10: JPG format 00: Others
17:16	BUS_SIZE	0: 8-bit 1: 16-bit 2: 24-bit 3: 32-bit
13:0	STRIDE	**Double buffer** Memory address distance from n-th line start address to (n+1)-th line start address. Unit: Byte

150074E8 **CAM_IMGO_D_CON** **DMA Control Register** **80B0B0B0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BURST_LEN					FIFO_P	FIFO_P	FIFO_S	FIFO_PRI_THRH							

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						RI_THRH_MSB	RI_THRL_MSB	IZE_MSB								
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	1	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRI_THRL								FIFO_SIZE							
Type	W1								W1							
Reset	1	0	1	1	0	0	0	0	1	0	1	1	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

150074EC CAM_IMGO_D_CON2 DMA Control Register 2 00B0B000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FIFO_PRE_PRI_THRH_MSB	FIFO_PRE_PRI_THRL_MSB	FIFO_PRE_PRI_THRH							
Type							W1	W1	W1							
Reset							0	0	1	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRE_PRI_THRL															
Type	W1															
Reset	1	0	1	1	0	0	0	0								

Bit(s)	Name	Description
25	FIFO_PRE_PRI_THRH_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_THRH	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

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150074F0 **CAM_IMGO_D_CROP** **DMA Crop Function Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**YOFFSET**												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**XOFFSET**													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	YOFFSET	**Double buffer** Number of pixels to be discarded from top of the line
13:0	XOFFSET	**Double buffer** Number of pixels to be discarded from the left of the line

150074F4 **CAM_RRZO_D_BASE_ADDR** **DMA Base ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**BASE_ADDR[31:16]**															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BASE_ADDR[15:0]**															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

150074F8 **CAM_RRZO_D_OFST_ADDR** **DMA Offset ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**OFFSET_ADDR[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**OFFSET_ADDR[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

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150074FC CAM_RRZO_D_XSIZE DMA XSIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			XSIZE													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to write

15007500 CAM_RRZO_D_YSIZE DMA YSIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				YSIZE												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	YSIZE	**Double buffer** (Number - 1) of lines to write

15007504 CAM_RRZO_D_STRIDE DMA Stride 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								BUS_SIZE_EN	FORMAT_EN		FORMAT			BUS_SIZE		
Type								RW	RW		RW			RW		
Reset								0	0		0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			STRIDE													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24	BUS_SIZE_EN	0: Use HW auto setting 1: Enable SW FORMAT setting
23	FORMAT_EN	0: Use HW auto setting 1: Enable SW FORMAT setting
21:20	FORMAT	01: YUV format

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Bit(s)	Name	Description
		10: JPG format 00: Others
18:16	BUS_SIZE	0: 8-bit 1: 16-bit 2: 24-bit 3: 32-bit 7: 64-bit
13:0	STRIDE	**Double buffer** Memory address distance from n-th line start address to (n+1)-th line start address. Unit: Byte

15007508 **CAM_RRZO_D_CON** **DMA Control Register** **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BURST_LEN					FIFO_PRI_THRH_MSB	FIFO_PRI_THRL_MSB	FIFO_SIZE_MSB	FIFO_PRI_THRH							
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRI_THRL								FIFO_SIZE							
Type	W1								W1							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

1500750C **CAM_RRZO_D_CON2** **DMA Control Register 2** **00808000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FIFO_PRE_PRI_THRH_MSB	FIFO_PRE_PRI_THRL_MSB	FIFO_PRE_PRI_THRH							

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Type							W1	W1	W1							
Reset							0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRE_PRI_THRL															
Type	W1															
Reset	1	0	0	0	0	0	0	0								

Bit(s)	Name	Description
25	FIFO_PRE_PRI_THRH_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_THRH	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

15007510 CAM_RRZO_D_CROP DMA Crop Function Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				YOFFSET												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			XOFFSET													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	YOFFSET	**Double buffer** Number of pixels to be discarded from top of the line
13:0	XOFFSET	**Double buffer** Number of pixels to be discarded from the left of the line

15007514 CAM_LCSO_D_BASE_ADDR DMA Base ADDR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASE_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

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15007518 **CAM_LCSOD_OFST_ADDR** **DMA Offset ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OFFSET_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFFSET_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

1500751C **CAM_LCSOD_XSIZE** **DMA XSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			XSIZE													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to write

15007520 **CAM_LCSOD_YSIZE** **DMA YSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				YSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	YSIZE	**Double buffer** (Number - 1) of lines to write

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15007524 **CAM_LCSOD_STRIDE** **DMA Stride** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			STRIDE													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	STRIDE	**Double buffer** Memory address distance from n-th line start address to (n+1)-th line start address. Unit: Byte

15007528 **CAM_LCSOD_CON** **DMA Control Register** **80202020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BURST_LEN					FIFO_PRI_THRH_MSB	FIFO_PRI_THRL_MSB	FIFO_SIZE_MSB	FIFO_PRI_THRH							
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRI_THRL								FIFO_SIZE							
Type	W1								W1							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

1500752C **CAM_LCSOD_CON2** **DMA Control Register 2** **00202000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FIF	FIF	FIFO_PRE_PRI_THRH							

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							O_PRE_PRI_THRH_MSB	O_PRE_PRI_THRL_MSB								
Type							W1	W1	W1							
Reset							0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRE_PRI_THRL															
Type	W1															
Reset	0	0	1	0	0	0	0	0								

Bit(s)	Name	Description
25	FIFO_PRE_PRI_THRH_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_THRH	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

15007530 **CAM_AFO_D_BASE_ADDR** **DMA Base ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASE_ADDR[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

15007534 **CAM_AFO_D_XSIZE** **DMA XSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			XSIZE													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	XSIZE	**Double buffer**

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Bit(s)	Name	Description
		(Number - 1) of bytes per line to write

15007538 CAM_AFO_D_OFST_ADDR DMA Offset ADDR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OFFSET_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFFSET_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

1500753C CAM_AFO_D_YSIZE DMA YSIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RSV												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	RSV	**Double buffer** (Number - 1) of lines to write

15007540 CAM_AFO_D_STRIDE DMA Stride 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RSV													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	RSV	**Double buffer** Memory address distance from n-th line start address to (n+1)-th line start

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Bit(s)	Name	Description
		address. Unit: Byte

15007544 **CAM_AFO_D_CON** **DMA Control Register** **80202020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BURST_LEN					FIFO_PRI_THRH_MSB	FIFO_PRI_THRL_MSB	FIFO_SIZE_MSB	FIFO_PRI_THRH							
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRI_THRL								FIFO_SIZE							
Type	W1								W1							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

15007548 **CAM_AFO_D_CON2** **DMA Control Register 2** **00202000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FIFO_PRE_PRI_THRH_MSB	FIFO_PRE_PRI_THRL_MSB	FIFO_PRE_PRI_THRH							
Type							W1	W1	W1							
Reset							0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRE_PRI_THRL															
Type	W1															
Reset	0	0	1	0	0	0	0	0								

Bit(s)	Name	Description
25	FIFO_PRE_PRI_T	For pre-priority control signal: If FIFO amount is larger than THRH, priority

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Bit(s)	Name	Description
	HRH_MSB	control signal will be asserted.
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_THRH	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

1500754C **CAM_AAO_D_BASE_ADDR** **DMA Base ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASE_ADDR[31:16]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASE_ADDR[15:0]															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BASE_ADDR	**Double buffer** Start address of a frame

15007550 **CAM_AAO_D_OFST_ADDR** **DMA Offset ADDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OFFSET_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFFSET_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OFFSET_ADDR	**Tile start address from Start address of a frame** (dipi_base_addr+dipi_offset_addr=tile_start_addr)

15007554 **CAM_AAO_D_XSIZE** **DMA XSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																XSIZE[16:16]
Type																USE

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																R0
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**XSIZE[15:0]**															
Type	USER0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	XSIZE	**Double buffer** (Number - 1) of bytes per line to write

15007558 **CAM_AAO_D_YSIZE** **DMA YSIZE** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**RSV**												
Type				USER0												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	RSV	**Double buffer** (Number - 1) of lines to write

1500755C **CAM_AAO_D_STRIDE** **DMA Stride** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								**BUS_SIZE_EN**							**BUS_SIZE**	
Type								RW							RW	
Reset								0							0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**RSV**													
Type			USER0													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24	BUS_SIZE_EN	0: Use HW auto setting 1: Enable SW BUS_SIZE setting
17:16	BUS_SIZE	1: 16-bit 3: 32-bit
13:0	RSV	**Double buffer** Memory address distance from n-th line start address to (n+1)-th line start address. Unit: Byte

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15007560 CAM_AAO_D_CON DMA Control Register 80202020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BURST_LEN					FIFO_PRI_THRH_MSB	FIFO_PRI_THRL_MSB	FIFO_SIZE_MSB	FIFO_PRI_THRH							
Type	W1					W1	W1	W1	W1							
Reset	1	0	0	0		0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRI_THRL								FIFO_SIZE							
Type	W1								W1							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_BURST_LEN	Max. burst length can be set to 1, 2, 4 and 8.
26	FIFO_PRI_THRH_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
25	FIFO_PRI_THRL_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_SIZE_MSB	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRI_THRH	For priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
15:8	FIFO_PRI_THRL	For priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.
7:0	FIFO_SIZE	FIFO depth

15007564 CAM_AAO_D_CON2 DMA Control Register 2 00202000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FIFO_PRE_PRI_THRH_MSB	FIFO_PRE_PRI_THRL_MSB	FIFO_PRE_PRI_THRH							
Type							W1	W1	W1							
Reset							0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_PRE_PRI_THRL															
Type	W1															
Reset	0	0	1	0	0	0	0	0								

Bit(s)	Name	Description
25	FIFO_PRE_PRI_THRH_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
24	FIFO_PRE_PRI_THRL_MSB	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.
23:16	FIFO_PRE_PRI_THRH	For pre-priority control signal: If FIFO amount is larger than THRH, priority control signal will be asserted.

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Bit(s)	Name	Description
15:8	FIFO_PRE_PRI_THRL	For pre-priority control signal: If FIFO amount is smaller than THRL, priority control signal will be de-asserted.

15007568 **CAM_DMA_ERR_CTRL** **DMA Error Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERR_CLR_MD	AAO_D_ERR	AFO_D_ERR	LCSO_D_ERR	RRZO_D_ERR	IMGO_D_ERR	LSCI_D_ERR	BPCI_D_ERR	FEO_ERR	IMG3O_ERR	RRZO_ERR	IMG3CO_ERR	IMG3BO_ERR	MFBO_ERR	UFEO_ERR	AAO_ERR
Type	RW	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ESFKO_ERR	LCSO_ERR	IMG2O_ERR	IMGO_ERR			VIP3I_ERR	VIP2I_ERR	VIPI_ERR	LCEI_ERR	UFDI_ERR	LSCI_ERR		BPCI_ERR	IMGI_ERR	
Type	RO	RO	RO	RO			RO	RO	RO	RO	RO	RO		RO	RO	
Reset	0	0	0	0			0	0	0	0	0	0		0	0	

Bit(s)	Name	Description
31	ERR_CLR_MD	**Selects method to clear error status registers** 0: CPU read clear 1: Write 1 to clear
30	AAO_D_ERR	There is at least one error in the error status register.
29	AFO_D_ERR	There is at least one error in the error status register.
28	LCSO_D_ERR	There is at least one error in the error status register.
27	RRZO_D_ERR	There is at least one error in the error status register.
26	IMGO_D_ERR	There is at least one error in the error status register.
25	LSCI_D_ERR	There is at least one error in the error status register.
24	BPCI_D_ERR	There is at least one error in the error status register.
23	FEO_ERR	There is at least one error in the error status register.
22	IMG3O_ERR	There is at least one error in the error status register.
21	RRZO_ERR	There is at least one error in the error status register.
20	IMG3CO_ERR	There is at least one error in the error status register.
19	IMG3BO_ERR	There is at least one error in the error status register.
18	MFBO_ERR	There is at least one error in the error status register.
17	UFEO_ERR	There is at least one error in the error status register.
16	AAO_ERR	There is at least one error in the error status register.
15	ESFKO_ERR	There is at least one error in the error status register.
14	LCSO_ERR	There is at least one error in the error status register.
13	IMG2O_ERR	There is at least one error in the error status register.
12	IMGO_ERR	There is at least one error in the error status register.
9	VIP3I_ERR	There is at least one error in the error status register.
8	VIP2I_ERR	There is at least one error in the error status register.
7	VIPI_ERR	There is at least one error in the error status register.
6	LCEI_ERR	There is at least one error in the error status register.
5	UFDI_ERR	There is at least one error in the error status register.
4	LSCI_ERR	There is at least one error in the error status register.

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Bit(s)	Name	Description
2	BPCI_ERR	There is at least one error in the error status register.
1	IMGI_ERR	There is at least one error in the error status register.

1500756C **CAM_IMGI_ERR_STAT** **IMGI Error Status Register** **FFFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERR_EN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERR_STAT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function
15:0	ERR_STAT	DMA error status

15007570 **CAM_BPCI_ERR_STAT** **IMGI Error Status Register** **FFFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERR_EN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERR_STAT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function
15:0	ERR_STAT	DMA error status

15007574 **CAM_LSCI_ERR_STAT** **LSCI Error Status Register** **FFFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERR_EN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERR_STAT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function

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Bit(s)	Name	Description
15:0	ERR_STAT	DMA error status

15007578 **CAM_UFDI_ERR_STAT** **UFDI Error Status Register** **FFFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERR_EN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERR_STAT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function
15:0	ERR_STAT	DMA error status

1500757C **CAM_LCEI_ERR_STAT** **LCEI Error Status Register** **FFFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERR_EN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERR_STAT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function
15:0	ERR_STAT	DMA error status

15007580 **CAM_VIPI_ERR_STAT** **VIPI Error Status Register** **FFFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERR_EN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERR_STAT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function
15:0	ERR_STAT	DMA error status

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15007584 **CAM_VIP2I_ERR_STAT** **VIP2I Error Status Register** **FFFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERR_EN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERR_STAT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function
15:0	ERR_STAT	DMA error status

15007588 **CAM_VIP3I_ERR_STAT** **VIP3I Error Status Register** **FFFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERR_EN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERR_STAT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function
15:0	ERR_STAT	DMA error status

1500758C **CAM_IMGO_ERR_STAT** **IMGO Error Status Register** **FFFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERR_EN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERR_STAT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function
15:0	ERR_STAT	DMA error status

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15007590 **CAM_RRZO_ERR_STAT** **RRZO Error Status Register** **FFFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERR_EN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERR_STAT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function
15:0	ERR_STAT	DMA error status

15007594 **CAM_LCSO_ERR_STAT** **LCEO Error Status Register** **FFFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERR_EN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERR_STAT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function
15:0	ERR_STAT	DMA error status

15007598 **CAM_ESFKO_ERR_STAT** **ESFKO Error Status Register** **FFFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERR_EN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERR_STAT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function
15:0	ERR_STAT	DMA error status

1500759C **CAM_AAO_ERR_STAT** **AAO Error Status Register** **FFFF0000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERR_EN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERR_STAT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function
15:0	ERR_STAT	DMA error status

150075A0 CAM_UFEO_ERR_STAT UFEO Error Status Register FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERR_EN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERR_STAT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function
15:0	ERR_STAT	DMA error status

150075A4 CAM_MFBO_ERR_STAT MFBO Error Status Register FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERR_EN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERR_STAT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function
15:0	ERR_STAT	DMA error status

150075A8 CAM_IMG3BO_ERR_STAT IMG3BO Error Status Register FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERR_EN															

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Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ERR_STAT**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function
15:0	ERR_STAT	DMA error status

150075AC CAM_IMG3CO_ERR_STAT IMG3CO Error Status Register FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**ERR_EN**															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ERR_STAT**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function
15:0	ERR_STAT	DMA error status

150075B0 CAM_IMG2O_ERR_STAT IMG2O Error Status Register FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**ERR_EN**															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ERR_STAT**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function
15:0	ERR_STAT	DMA error status

150075B4 CAM_IMG3O_ERR_STAT IMG3O Error Status Register FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**ERR_EN**															

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Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERR_STAT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function
15:0	ERR_STAT	DMA error status

150075B8 CAM_FEO_ERR_STAT FEO Error Status Register FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERR_EN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERR_STAT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function
15:0	ERR_STAT	DMA error status

150075BC CAM_BPCI_D_ERR_STAT BPCI_D Error Status Register FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERR_EN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERR_STAT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function
15:0	ERR_STAT	DMA error status

150075C0 CAM_LSCI_D_ERR_STAT LSCI_D Error Status Register FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERR_EN															
Type	RW															

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Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ERR_STAT**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function
15:0	ERR_STAT	DMA error status

150075C4 **CAM_IMGO_D_ERR_STAT** **IMGO_D Error Status Register** **FFFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**ERR_EN**															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ERR_STAT**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function
15:0	ERR_STAT	DMA error status

150075C8 **CAM_RRZO_D_ERR_STAT** **RRZO_D Error Status Register** **FFFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**ERR_EN**															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ERR_STAT**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function
15:0	ERR_STAT	DMA error status

150075CC **CAM_LCSO_D_ERR_STAT** **LCSO_D Error Status Register** **FFFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**ERR_EN**															
Type	RW															

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Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERR_STAT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function
15:0	ERR_STAT	DMA error status

150075D0 CAM_AFO_D_ERR_STAT AFO_D Error Statuss Register FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERR_EN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERR_STAT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function
15:0	ERR_STAT	DMA error status

150075D4 CAM_AAO_D_ERR_STAT AAO_D Error Status Register FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERR_EN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERR_STAT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERR_EN	Enables error status function
15:0	ERR_STAT	DMA error status

150075D8 CAM_DMA_DEBUG_ADDR DMA Debug Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_ADDR[31:16]															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DEBUG_ADDR[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_ADDR	Locates debugging port count -> Locates CMD/data

150075DC CAM_DMA_RSV1 Reserve1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RSV[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RSV[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RSV	Reserved

150075E0 CAM_DMA_RSV2 Reserve2 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RSV[31:16]**															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RSV[15:0]**															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	RSV	Reserved

150075E4 CAM_DMA_RSV3 Reserve3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RSV[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RSV[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	RSV	Reserved

150075E8 **CAM_DMA_RSV4** **Reserve4** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RSV[31:16]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV[15:0]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	RSV	Reserved

150075EC **CAM_DMA_RSV5** **Reserve5** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RSV[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RSV	Reserved

150075F0 **CAM_DMA_RSV6** **Reserve6** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RSV[31:16]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV[15:0]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	RSV	Reserved

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150075F4 **CAM_DMA_DEBUG_SEL** **DMA Debug Sel Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ARBITER_COM_FULL	ARBITER_BVALID_FULL	IMGO_UFE_FIFO_FULL_XSIZE	IMGI_UFD_FIFO_FULL_XSIZE	IMGI_UFD_FIFO_FULL_OFFSET	IMGI_ADDR_GEN_WAIT			SUB_MODULE_SEL							
Type	RO	RO	RO	RO	RO	RO			RW							
Reset	0	0	0	0	0	0			0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R_W_DMA_TOP_SEL								DMA_TOP_SEL							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	ARBITER_COM_FULL	Arbiter command FIFO full flag
30	ARBITER_BVALID_FULL	Arbiter bvalid FIFO full flag
29	IMGO_UFE_FIFO_FULL_XSIZE	IMGO UFE encode xsize FIFO full flag
28	IMGI_UFD_FIFO_FULL_XSIZE	IMGI UFD decode xsize FIFO full flag
27	IMGI_UFD_FIFO_FULL_OFFSET	IMGI UFD decode offset FIFO full flag
26	IMGI_ADDR_GEN_WAIT	IMGI wait address gen flag
23:16	SUB_MODULE_SEL	
15:8	R_W_DMA_TOP_SEL	
7:0	DMA_TOP_SEL	

150075F8 **CAM_DMA_BW_SELF_TEST** **DMA BWs Self Test Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																BW_SELF_TEST_EN_ESFKO
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BW_SELF_TES	BW_SELF_TES	BW_SELF_TES	BW_SELF_TES	BW_SELF_TES	BW_SELF_TES	BW_SELF_TES	BW_SELF_TES	BW_SELF_TES	BW_SELF_TES	BW_SELF_TES	BW_SELF_TES	BW_SELF_TES	BW_SELF_TES	BW_SELF_TES	BW_SELF_TES

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	T_EN_FEO	T_EN_MFBO	T_EN_IMG2O	T_EN_AFO_D	T_EN_LCSO_D	T_EN_LCSO	T_EN_AAO_D	T_EN_AAO	T_EN_IMG3CO	T_EN_IMG3BO	T_EN_IMG3O	T_EN_RRZO_D	T_EN_RRZO	T_EN_UFEO	T_EN_IMGO_D	T_EN_IMGO
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	BW_SELF_TEST_EN_ESFKO	0: Disable BW test function 1: Enable BW test function
15	BW_SELF_TEST_EN_FEO	0: Disable BW test function 1: Enable BW test function
14	BW_SELF_TEST_EN_MFBO	0: Disable BW test function 1: Enable BW test function
13	BW_SELF_TEST_EN_IMG2O	0: Disable BW test function 1: Enable BW test function
12	BW_SELF_TEST_EN_AFO_D	0: Disable BW test function 1: Enable BW test function
11	BW_SELF_TEST_EN_LCSO_D	0: Disable BW test function 1: Enable BW test function
10	BW_SELF_TEST_EN_LCSO	0: Disable BW test function 1: Enable BW test function
9	BW_SELF_TEST_EN_AAO_D	0: Disable BW test function 1: Enable BW test function
8	BW_SELF_TEST_EN_AAO	0: Disable BW test function 1: Enable BW test function
7	BW_SELF_TEST_EN_IMG3CO	0: Disable BW test function 1: Enable BW test function
6	BW_SELF_TEST_EN_IMG3BO	0: Disable BW test function 1: Enable BW test function
5	BW_SELF_TEST_EN_IMG3O	0: Disable BW test function 1: Enable BW test function
4	BW_SELF_TEST_EN_RRZO_D	0: Disable BW test function 1: Enable BW test function
3	BW_SELF_TEST_EN_RRZO	0: Disable BW test function 1: Enable BW test function
2	BW_SELF_TEST_EN_UFEO	0: Disable BW test function 1: Enable BW test function
1	BW_SELF_TEST_EN_IMGO_D	0: Disable BW test function 1: Enable BW test function
0	BW_SELF_TEST_EN_IMGO	0: Disable BW test function 1: Enable BW test function

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6.5 SENINF_TOP (Sensor Interface)

6.5.1 Introduction

The seninf_top module transfers sensor signal into image pixels and pass them to ISP.

6.5.2 Features

- MIPI interface
  - Two 4-lanes MIPI interfaces
  - Virtual channel/Data type data interleaving
- Serial interface
  - 1 Serial interface
- Parallel interface
  - 1 parallel interface
- Provides 3 sensor master clocks

6.5.3 Register Definition

Module name: seninf_top Base address: (+15008000h)

Address	Name	Width	Register Function
15008000	SENINF_TOP_CTRL	32	SENINF Top Control Register
15008004	SENINF_TOP_CMODEL_PAR	32	SENINF Top C Model Register
15008008	SENINF_TOP_MUX_CTRL	32	SENINF Top Mux Control Register

15008000 **SENINF_TOP_CTRL** **SENINF Top Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_TOP_DBG_SEL															SENINF_TOP_N3D_SW_RST
Type	RW															RW
Reset	0															0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					SENINF2_PCLK_EN	SENINF1_PCLK_EN	SENINF2_PCLK_SEL	SENINF1_PCLK_SEL								
Type					RW	RW	RW	RW								
Reset					0	0	0	0								

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Bit(s)	Name	Description
31	SENINF_TOP_DBG_SEL	0: SENINF 1 CSI2 1: SENINF 2 CSI2
16	SENINF_TOP_N3D_SW_RST	**N3D software reset** Active high 0: De-assert reset 1: Assert reset
11	SENINF2_PCLK_EN	**Enables parallel sensor clock** 0: Gated 1: Not gated
10	SENINF1_PCLK_EN	**Enables parallel sensor clock** 0: Gated 1: Not gated
9	SENINF2_PCLK_SEL	**Selects parallel sensor clock** 0: pclk 1: mclk
8	SENINF1_PCLK_SEL	**Selects parallel sensor clock** 0: pclk 1: mclk

15008004 **SENINF_TOP_CMODEL_PAR** **SENINF Top C Model Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SENINF4_FORMAT			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF3_FORMAT				SENINF2_FORMAT				SENINF1_FORMAT				SENINF4_EN	SENINF3_EN	SENINF2_EN	SENINF1_EN
Type	RW				RW				RW				RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:16	SENINF4_FORMAT	
15:12	SENINF3_FORMAT	
11:8	SENINF2_FORMAT	
7:4	SENINF1_FORMAT	
3	SENINF4_EN	
2	SENINF3_EN	
1	SENINF2_EN	
0	SENINF1_EN	

15008008 **SENINF_TOP_MUX_CTRL** **SENINF Top Mux Control Register** **00003210**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

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Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF4_MUX_SRC_SEL				SENINF3_MUX_SRC_SEL				SENINF2_MUX_SRC_SEL				SENINF1_MUX_SRC_SEL			
Type	RW				RW				RW				RW			
Reset	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:12	SENINF4_MUX_SRC_SEL	0: SENINF 1 1: SENINF 2 2: SENINF 3 3: SENINF 4
11:8	SENINF3_MUX_SRC_SEL	0: SENINF 1 1: SENINF 2 2: SENINF 3 3: SENINF 4
7:4	SENINF2_MUX_SRC_SEL	0: SENINF 1 1: SENINF 2 2: SENINF 3 3: SENINF 4
3:0	SENINF1_MUX_SRC_SEL	0: SENINF 1 1: SENINF 2 2: SENINF 3 3: SENINF 4

Module name: seninf Base address: (+15008000h)

Address	Name	Width	Register Function
15008100	**SENINF1_CTRL**	32	SENINF 1 Control Register
15008500	**SENINF2_CTRL**	32	SENINF 2 Control Register
15008900	**SENINF3_CTRL**	32	SENINF 3 Control Register
15008D00	**SENINF4_CTRL**	32	SENINF 4 Control Register

15008100 **SENINF1_CTRL** **SENINF 1 Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		PAD2CAM_DATA_SEL														
Type		RW														
Reset		0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_SRC_SEL				SENINF_DEBUG_SEL					SCAM_SW_RST	TEST_MODEL_SW_RST	CKGEN_SW_RST	CCIR_SW_RST	CSI2_SW_RST	NCSI2_SW_RST	SENINF_EN
Type	RW				RW					RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:28	PAD2CAM_DATA_	0: PAD2CAM_DATA[9:0]

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Bit(s)	Name	Description
	SEL	3: {PAD2CAM_DATA[7:0],2'b00} 4: {PAD2CAM_DATA[9:2]2'b00}
15:12	SENINF_SRC_SEL	**Selects SENINF input source** 0: CSI2 1: Test model 2: CCIR656 3: Parallel sensor 4: Serial sensor 8: NCSI2
11:8	SENINF_DEBUG_SEL	**Selects SENINF1 debugging**
6	SCAM_SW_RST	**SCAM software reset** Active high 0: De-assert reset 1: Assert reset
5	TEST_MODEL_SW_RST	**Test model software reset** Active high 0: De-assert reset 1: Assert reset
4	CKGEN_SW_RST	**CKGEN software reset** Active high 0: De-assert reset 1: Assert reset
3	CCIR_SW_RST	**CCIR software reset** Active high 0: De-assert reset 1: Assert reset
2	CSI2_SW_RST	**CSI2 software reset** Active high 0: De-assert reset 1: Assert reset
1	NCSI2_SW_RST	**NCSI2 software reset** Active high 0: De-assert reset 1: Assert reset
0	SENINF_EN	

15008500 **SENINF2_CTRL** **SENINF 2 Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**PAD2CAM_DATA_SEL**														
Type		RW														
Reset		0	0	0												

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SENINF_SRC_SEL**				**SENINF_DEBUG_SEL**					**SCAM_SW_RST**	**TEST_MODEL_SW_RST**	**CKGEN_SW_RST**	**CCIR_SW_RST**	**CSI2_SW_RST**	**NCSI2_SW_RST**	**SENINF_EN**
Type	RW				RW					RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0

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Bit(s)	Name	Description
30:28	PAD2CAM_DATA_SEL	0: PAD2CAM_DATA[9:0] 3: {PAD2CAM_DATA[7:0],2'b00} 4: {PAD2CAM_DATA[9:2]2'b00}
15:12	SENINF_SRC_SEL	**Selects SENINF input source** 0: CSI2 1: Test model 2: CCIR656 3: Parallel sensor 4: Serial sensor 8: NCSI2
11:8	SENINF_DEBUG_SEL	**Selects SENINF2 debugging**
6	SCAM_SW_RST	**SCAM software reset** Active high 0: De-assert reset 1: Assert reset
5	TEST_MODEL_SW_RST	**Test model software reset** Active high 0: De-assert reset 1: Assert reset
4	CKGEN_SW_RST	**CKGEN software reset** Active high 0: De-assert reset 1: Assert reset
3	CCIR_SW_RST	**CCIR software reset** Active high 0: De-assert reset 1: Assert reset
2	CSI2_SW_RST	**CSI2 software reset** Active high 0: De-assert reset 1: Assert reset
1	NCSI2_SW_RST	**NCSI2 software reset** Active high 0: De-assert reset 1: Assert reset
0	SENINF_EN	

15008900 **SENINF3_CTRL** **SENINF 3 Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		PAD2CAM_DATA_SEL														
Type		RW														
Reset		0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_SRC_SEL				SENINF_DEBUG_SEL					SCAM_SW_RST	TEST_MODEL_SW_RST	CKGEN_SW_RST	CCIR_SW_RST	CSI2_SW_RST	NCSI2_SW_RST	SENINF_EN
Type	RW				RW					RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0

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Bit(s)	Name	Description
30:28	PAD2CAM_DATA_SEL	0: PAD2CAM_DATA[9:0] 3: {PAD2CAM_DATA[7:0],2'b00} 4: {PAD2CAM_DATA[9:2]2'b00}
15:12	SENINF_SRC_SEL	**Selects SENINF input source** 0: CSI2 1: Test model 2: CCIR656 3: Parallel sensor 4: Serial sensor 8: NCSI2
11:8	SENINF_DEBUG_SEL	**Selects SENINF3 debugging**
6	SCAM_SW_RST	**SCAM software reset** Active high 0: De-assert reset 1: Assert reset
5	TEST_MODEL_SW_RST	**Test model software reset** Active high 0: De-assert reset 1: Assert reset
4	CKGEN_SW_RST	**CKGEN software reset** Active high 0: De-assert reset 1: Assert reset
3	CCIR_SW_RST	**CCIR software reset** Active high 0: De-assert reset 1: Assert reset
2	CSI2_SW_RST	**CSI2 software reset** Active high 0: De-assert reset 1: Assert reset
1	NCSI2_SW_RST	**NCSI2 software reset** Active high 0: De-assert reset 1: Assert reset
0	SENINF_EN	

15008D00 **SENINF4_CTRL** **SENINF 4 Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**PAD2CAM_DATA_SEL**														
Type		RW														
Reset		0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SENINF_SRC_SEL**				**SENINF_DEBUG_SEL**					**SCAM_SW_RST**	**TEST_MODEL_SW_RST**	**CKGEN_SW_RST**	**CCIR_SW_RST**	**CSI2_SW_RST**	**NCSI2_SW_RST**	**SENINF_EN**
Type	RW				RW					RW	RW	RW	RW	RW	RW	RW

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Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:28	PAD2CAM_DATA_SEL	0: PAD2CAM_DATA[9:0] 3: {PAD2CAM_DATA[7:0],2'b00} 4: {PAD2CAM_DATA[9:2]2'b00}
15:12	SENINF_SRC_SEL	**Selects SENINF input source** 0: CSI2 1: Test model 2: CCIR656 3: Parallel sensor 4: Serial sensor 8: NCSI2
11:8	SENINF_DEBUG_SEL	**Selects SENINF4 debugging**
6	SCAM_SW_RST	**SCAM software reset** Active high 0: De-assert reset 1: Assert reset
5	TEST_MODEL_SW_RST	**Test model software reset** Active high 0: De-assert reset 1: Assert reset
4	CKGEN_SW_RST	**CKGEN software reset** Active high 0: De-assert reset 1: Assert reset
3	CCIR_SW_RST	**CCIR software reset** Active high 0: De-assert reset 1: Assert reset
2	CSI2_SW_RST	**CSI2 software reset** Active high 0: De-assert reset 1: Assert reset
1	NCSI2_SW_RST	**NCSI2 software reset** Active high 0: De-assert reset 1: Assert reset
0	SENINF_EN	

Module name: SENINF_TG Base address: (+15008000h)

Address	Name	Width	Register Function
15008200	TG1_PH_CNT	32	**TG Phase Counter** TG phase counter register
15008204	TG1_SEN_CK	32	TG Sensor Clock Divider
15008208	TG1_TM_CTL	32	**TM Control** Test model control register
1500820C	TG1_TM_SIZE	32	**TM Size** Test model line/pixel count
15008210	TG1_TM_CLK	32	**TM Clock** Test model clock source

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Address	Name	Width	Register Function
15008600	TG2_PH_CNT	32	TG Phase Counter
15008604	TG2_SEN_CK	32	TG Sensor Clock Divider
15008608	TG2_TM_CTL	32	TM Control Test model control register
1500860C	TG2_TM_SIZE	32	**TM Size** Test model line/pixel count
15008610	TG2_TM_CLK	32	**TM Clock** Test model clock source
15008A00	TG3_PH_CNT	32	TG Phase Counter
15008A04	TG3_SEN_CK	32	TG Sensor Clock Divider
15008A08	TG3_TM_CTL	32	**TM Control** Test model control register
15008A0C	TG3_TM_SIZE	32	**TM Size** Test model line/pixel count
15008A10	TG3_TM_CLK	32	**TM Clock** Test model clock source
15008E00	TG4_PH_CNT	32	TG Phase Counter
15008E04	TG4_SEN_CK	32	TG Sensor Clock Divider
15008E08	TG4_TM_CTL	32	**TM Control** Test model control register
15008E0C	TG4_TM_SIZE	32	**TM Size** Test model line/pixel count
15008E10	TG4_TM_CLK	32	**TM Clock** Test model clock source

15008200 **TG1_PH_CNT** **TG Phase Counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PCEN		ADCLK_EN	CLKPOL												
Type	RW		RW	RW												
Reset	0		0	0												
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name									CAM_PCLK_INV	PAD_PCLK_INV	EXT_PWRDN	EXT_RST		CLKFL_POL	TGCLK_SEL	
Type									RW	RW	RW	RW		RW	RW	
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
31	PCEN	**TG phase counter enable control**
29	ADCLK_EN	**Enables sensor master clock (mclk) output to sensor** *Note: Remember to set up sensor master clock driving setting,*
28	CLKPOL	**Controls sensor master clock polarity**
7	CAM_PCLK_INV	**Inverts pixel clock in cam**
6	PAD_PCLK_INV	**Inverts pixel clock in PAD side**
5	EXT_PWRDN	**Powers down sensor**
4	EXT_RST	**Resets sensor**

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Bit(s)	Name	Description
2	CLKFL_POL	**Sensor clock falling edge polarity**
1:0	TGCLK_SEL	**Selects sensor master clock** 0: isp_clk 1: cam_pll 2: 3rd clock source

15008204 **TG1_SEN_CK** **TG Sensor Clock Divider** **00010001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											**CLKCNT**					
Type											RW					
Reset											0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**CLKRS**								**CLKFL**					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	1

Bit(s)	Name	Description
21:16	CLKCNT	**Controls sensor master clock frequency divider** The sensor master clock is ISP_clock/(CLKCNT+1), where CLKCNT >=1.
13:8	CLKRS	**Controls sensor master clock rising edge**
5:0	CLKFL	**Controls sensor master clock falling edge**

15008208 **TG1_TM_CTL** **TM Control** **00300004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									**TM_DUMMYPXL**							
Type									RW							
Reset									0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TM_VSYNC**								**TM_PAT**					**TM_FMT**	**TM_RST**	**TM_EN**
Type	RW								RW					RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0		1	0	0

Bit(s)	Name	Description
23:16	TM_DUMMYPXL	**Test model horizontal dummy pixel**
15:8	TM_VSYNC	**VSYNC high duration** Unit: Line (TM_DUMMYPXL + PIXEL)
7:4	TM_PAT	**Decides test model** 0: White 1: Yellow 2: Cyan 3: Green 4: Magenta 5: Red 6: Blue 7: Black

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Bit(s)	Name	Description
		8: Horizontal gray level (Unit 1) 9: Horizontal gray level (Unit 4) 10: Horizontal gray level (take 1024 pixel as one period) (only bayer) 11: Vertical gray level (Unit 1) 12: Static horizontal color bar 13: Static vertical color bar (only bayer) 14: R, G, B, W flash every two frames (only bayer) 15: Dynamic horizontal colorbar (only bayer)
2	TM_FMT	**Test model format** 0: Bayer 1: YUV
1	TM_RST	**Resets test model** 1'b0: Does not reset test model 1'b1: Reset test model
0	TM_EN	**Enables test model** 0: Disable 1: Enable

15008200C **TG1_TM_SIZE** **TM Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				TM_LINE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				TM_PXL												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	TM_LINE	**Test model line number**
12:0	TM_PXL	**Test model pixel number** Hsync high duration; unit: pixel

15008210 **TG1_TM_CLK** **TM Clock** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		TM_CLRBAR_IDX					TM_CLRBAR_OFT									
Type		RW					RW									
Reset		0	0	0			0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TM_CLK_CNT			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
30:28	TM_CLRBAR_IDX	**Test model colorbar index offset** 0: White 1: Yellow 2: Cyan

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Bit(s)	Name	Description
		3: Green 4: Magenta 5: Red 6: Blue 7: Black
25:16	TM_CLRBAR_OFT	**Test model colorbar offset** This value must be smaller than (TM_PXL>>3).
3:0	TM_CLK_CNT	**Test model clock divided count**

15008600 **TG2_PH_CNT** **TG Phase Counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PCEN		ADCLK_EN	CLKPOL												
Type	RW		RW	RW												
Reset	0		0	0												

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CAM_PCLK_INV	PAD_PCLK_INV	EXT_PWRDN	EXT_RST		CLKFL_POL	TGCLK_SEL	
Type									RW	RW	RW	RW		RW	RW	
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
31	PCEN	**TG phase counter enable control**
29	ADCLK_EN	**Enables sensor master clock (mclk) output to sensor** *Note: Remember to set up sensor master clock driving setting,*
28	CLKPOL	**Controls sensor master clock polarity**
7	CAM_PCLK_INV	**Inverts pixel clock in cam**
6	PAD_PCLK_INV	**Inverts pixel clock in PAD side**
5	EXT_PWRDN	**Powers down sensor**
4	EXT_RST	**Resets sensor**
2	CLKFL_POL	**Sensor clock falling edge polarity**
1:0	TGCLK_SEL	**Selects sensor master clock** 0: isp_clk 1: cam_pll 2: 3rd clock source

15008604 **TG2_SEN_CK** **TG Sensor Clock Divider** **00010001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CLKCNT					
Type											RW					
Reset											0	0	0	0	0	1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			CLKRS								CLKFL					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	1

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Bit(s)	Name	Description
21:16	CLKCNT	**Controls sensor master clock frequency divider** The sensor master clock is ISP_clock/(CLKCNT+1), where CLKCNT >=1.
13:8	CLKRS	**Controls sensor master clock rising edge**
5:0	CLKFL	**Controls sensor master clock falling edge**

15008608 **TG2_TM_CTL** **TM Control** **00300004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									TM_DUMMYPXL							
Type									RW							
Reset									0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TM_VSYNC								TM_PAT					TM_FMT	TM_RST	TM_EN
Type	RW								RW					RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0		1	0	0

Bit(s)	Name	Description
23:16	TM_DUMMYPXL	**Test model horizontal dummy pixel**
15:8	TM_VSYNC	**VSYNC high duration** Unit: Line (TM_DUMMYPXL + PIXEL)
7:4	TM_PAT	**Decides test model** 0: White 1: Yellow 2: Cyan 3: Green 4: Magenta 5: Red 6: Blue 7: Black 8: Horizontal gray level (Unit 1) 9: Horizontal gray level (Unit 4) 10: Horizontal gray level (take 1024 pixel as one period) (only bayer) 11: Vertical gray level (Unit 1) 12: Static horizontal color bar 13: Static vertical color bar (only bayer) 14: R, G, B, W flash every two frames (only bayer) 15: Dynamic horizontal colorbar (only bayer)
2	TM_FMT	**Test model format** 0: Bayer 1: YUV
1	TM_RST	**Resets test model** 1'b0: Does not reset test model 1'b1: Reset test model
0	TM_EN	**Enables test model** 0: Disable 1: Enable

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1500860C **TG2_TM_SIZE** **TM Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				TM_LINE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				TM_PXL												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	TM_LINE	**Test model line number**
12:0	TM_PXL	**Test model pixel number** Hsync high duration; unit: pixel

15008610 **TG2_TM_CLK** **TM Clock** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		TM_CLRBAR_IDX					TM_CLRBAR_OFT									
Type		RW					RW									
Reset		0	0	0			0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TM_CLK_CNT			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
30:28	TM_CLRBAR_IDX	**Test model colorbar index offset** 0: White 1: Yellow 2: Cyan 3: Green 4: Magenta 5: Red 6: Blue 7: Black
25:16	TM_CLRBAR_OFT	**Test model colorbar offset** This value must be smaller than (TM_PXL>>3).
3:0	TM_CLK_CNT	**Test model clock divided count**

15008A00 **TG3_PH_CNT** **TG Phase Counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PCEN		ADCLK_EN	CLKPOL												
Type	RW		RW	RW												
Reset	0		0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CAM	PAD	EXT	EXT		CLK	TGCLK_SE	

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									_PCLK_INV	_PCLK_INV	_PWRDN	_RST		FL_POL	L	
Type									RW	RW	RW	RW		RW	RW	
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
31	PCEN	**TG phase counter enable control**
29	ADCLK_EN	**Enables sensor master clock (mclk) output to sensor** *Note: Remember to set up sensor master clock driving setting,*
28	CLKPOL	**Controls sensor master clock polarity**
7	CAM_PCLK_INV	**Inverts pixel clock in cam**
6	PAD_PCLK_INV	**Inverts pixel clock in PAD side**
5	EXT_PWRDN	**Powers down sensor**
4	EXT_RST	**Resets sensor**
2	CLKFL_POL	**Sensor clock falling edge polarity**
1:0	TGCLK_SEL	**Selects sensor master clock** 0: isp_clk 1: cam_pll 2: 3rd clock source

15008A04 **TG3_SEN_CK** **TG Sensor Clock Divider** **00010001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CLKCNT					
Type											RW					
Reset											0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			CLKRS								CLKFL					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	1

Bit(s)	Name	Description
21:16	CLKCNT	**Controls sensor master clock frequency divider** The sensor master clock is ISP_clock/(CLKCNT+1), where CLKCNT >=1.
13:8	CLKRS	**Controls sensor master clock rising edge**
5:0	CLKFL	**Controls sensor master clock falling edge**

15008A08 **TG3_TM_CTL** **TM Control** **00300004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									TM_DUMMYPXL							
Type									RW							
Reset									0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TM_VSYNC								TM_PAT					TM_FMT	TM_RST	TM_EN
Type	RW								RW					RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0		1	0	0

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Bit(s)	Name	Description
23:16	TM_DUMMYPXL	**Test model horizontal dummy pixel**
15:8	TM_VSYNC	**VSYNC high duration** Unit: Line (TM_DUMMYPXL + PIXEL)
7:4	TM_PAT	**Decides test model** 0: White 1: Yellow 2: Cyan 3: Green 4: Magenta 5: Red 6: Blue 7: Black 8: Horizontal gray level (Unit 1) 9: Horizontal gray level (Unit 4) 10: Horizontal gray level (take 1024 pixel as one period) (only bayer) 11: Vertical gray level (Unit 1) 12: Static horizontal color bar 13: Static vertical color bar (only bayer) 14: R, G, B, W flash every two frames (only bayer) 15: Dynamic horizontal colorbar (only bayer)
2	TM_FMT	**Test model format** 0: Bayer 1: YUV
1	TM_RST	**Resets test model** 1'b0: Does not reset test model 1'b1: Reset test model
0	TM_EN	**Enables test model** 0: Disable 1: Enable

15008A0C **TG3_TM_SIZE** **TM Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				TM_LINE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				TM_PXL												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	TM_LINE	**Test model line number**
12:0	TM_PXL	**Test model pixel number** Hsync high duration; unit: pixel

15008A10 **TG3_TM_CLK** **TM Clock** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		TM_CLRBAR_IDX					TM_CLRBAR_OFT									

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Type		RW					RW									
Reset		0	0	0			0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**TM_CLK_CNT**			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
30:28	TM_CLRBAR_IDX	**Test model colorbar index offset** 0: White 1: Yellow 2: Cyan 3: Green 4: Magenta 5: Red 6: Blue 7: Black
25:16	TM_CLRBAR_OFT	**Test model colorbar offset** This value must be smaller than (TM_PXL>>3).
3:0	TM_CLK_CNT	**Test model clock divided count**

15008E00 **TG4_PH_CNT** **TG Phase Counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**PCEN**		**ADCLK_EN**	**CLKPOL**												
Type	RW		RW	RW												
Reset	0		0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**CAM_PCLK_INV**	**PAD_PCLK_INV**	**EXT_PWRDN**	**EXT_RST**		**CLKFL_POL**	**TGCLK_SEL**	
Type									RW	RW	RW	RW		RW	RW	
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
31	PCEN	**TG phase counter enable control**
29	ADCLK_EN	**Enables sensor master clock (mclk) output to sensor** *Note: Remember to set up sensor master clock driving setting,*
28	CLKPOL	**Controls sensor master clock polarity**
7	CAM_PCLK_INV	**Inverts pixel clock in cam**
6	PAD_PCLK_INV	**Inverts pixel clock in PAD side**
5	EXT_PWRDN	**Powers down sensor**
4	EXT_RST	**Resets sensor**
2	CLKFL_POL	**Sensor clock falling edge polarity**
1:0	TGCLK_SEL	**Selects sensor master clock** 0: isp_clk 1: cam_pll 2: 3rd clock source

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15008E04 **TG4_SEN_CK** **TG Sensor Clock Divider** **00010001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CLKCNT					
Type											RW					
Reset											0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			CLKRS								CLKFL					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	1

Bit(s)	Name	Description
21:16	CLKCNT	**Controls sensor master clock frequency divider** The sensor master clock is ISP_clock/(CLKCNT+1), where CLKCNT >=1.
13:8	CLKRS	**Controls sensor master clock rising edge**
5:0	CLKFL	**Controls sensor master clock falling edge**

15008E08 **TG4_TM_CTL** **TM Control** **00300004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									TM_DUMMYPXL							
Type									RW							
Reset									0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TM_VSYNC								TM_PAT					TM_FMT	TM_RST	TM_EN
Type	RW								RW					RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0		1	0	0

Bit(s)	Name	Description
23:16	TM_DUMMYPXL	**Test model horizontal dummy pixel**
15:8	TM_VSYNC	**VSYNC high duration** Unit: Line (TM_DUMMYPXL + PIXEL)
7:4	TM_PAT	**Decides test model** 0: White 1: Yellow 2: Cyan 3: Green 4: Magenta 5: Red 6: Blue 7: Black 8: Horizontal gray level (Unit 1) 9: Horizontal gray level (Unit 4) 10: Horizontal gray level (take 1024 pixel as one period) (only bayer) 11: Vertical gray level (Unit 1) 12: Static horizontal color bar 13: Static vertical color bar (only bayer) 14: R, G, B, W flash every two frames (only bayer) 15: Dynamic horizontal colorbar (only bayer)
2	TM_FMT	**Test model format** 0: Bayer 1: YUV
1	TM_RST	**Resets test model**

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Bit(s)	Name	Description
		1'b0: Does not reset test model 1'b1: Reset test model
0	TM_EN	**Enables test model** 0: Disable 1: Enable

15008E0C **TG4_TM_SIZE** **TM Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				TM_LINE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				TM_PXL												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	TM_LINE	**Test model line number**
12:0	TM_PXL	**Test model pixel number** Hsync high duration; unit: pixel

15008E10 **TG4_TM_CLK** **TM Clock** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		TM_CLRBAR_IDX					TM_CLRBAR_OFT									
Type		RW					RW									
Reset		0	0	0			0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TM_CLK_CNT			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
30:28	TM_CLRBAR_IDX	**Test model colorbar index offset** 0: White 1: Yellow 2: Cyan 3: Green 4: Magenta 5: Red 6: Blue 7: Black
25:16	TM_CLRBAR_OFT	**Test model colorbar offset** This value must be smaller than (TM_PXL>>3).
3:0	TM_CLK_CNT	**Test model clock divided count**

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Module name: seninf_mux Base address: (+15008000h)

Address	Name	Width	Register Function
15008120	SENINF1_MUX_CTRL	32	SENINF 1 Control Register
15008124	SENINF1_MUX_INTEN	32	SENINF 1 Interrupt Enable Register
15008128	SENINF1_MUX_INTSTA	32	SENINF 1 Interrupt Status Register
1500812C	SENINF1_MUX_SIZE	32	SENINF 1 Image Size Register
15008130	SENINF1_MUX_DEBUG_1	32	SENINF 1 Debug Register 1
15008134	SENINF1_MUX_DEBUG_2	32	SENINF 1 Debug Register 2
15008138	SENINF1_MUX_DEBUG_3	32	SENINF 1 Debug Register 3
1500813C	SENINF1_MUX_DEBUG_4	32	SENINF 1 Debug Register 4
15008140	SENINF1_MUX_DEBUG_5	32	SENINF 1 Debug Register 5
15008144	SENINF1_MUX_DEBUG_6	32	SENINF 1 Debug Register 6
15008148	SENINF1_MUX_DEBUG_7	32	SENINF 1 Debug Register 7
1500814C	SENINF1_MUX_SPARE	32	SENINF 1 Spare Register
15008150	SENINF1_MUX_DATA	32	SENINF 1 Data Register
15008154	SENINF1_MUX_DATA_CNT	32	SENINF 1 Data Count Register
15008158	SENINF1_MUX_CROP	32	SENINF 1 Crop Size Register
15008520	SENINF2_MUX_CTRL	32	SENINF 2 Control Register
15008524	SENINF2_MUX_INTEN	32	SENINF 2 Interrupt Enable Register
15008528	SENINF2_MUX_INTSTA	32	SENINF 2 Interrupt Status Register
1500852C	SENINF2_MUX_SIZE	32	SENINF 2 Image Size Register
15008530	SENINF2_MUX_DEBUG_1	32	SENINF 2 Debug Register 1
15008534	SENINF2_MUX_DEBUG_2	32	SENINF 2 Debug Register 2
15008538	SENINF2_MUX_DEBUG_3	32	SENINF 2 Debug Register 3
1500853C	SENINF2_MUX_DEBUG_4	32	SENINF 2 Debug Register 4
15008540	SENINF2_MUX_DEBUG_5	32	SENINF 2 Debug Register 5
15008544	SENINF2_MUX_DEBUG_6	32	SENINF 2 Debug Register 6
15008548	SENINF2_MUX_DEBUG_7	32	SENINF 2 Debug Register 7
1500854C	SENINF2_MUX_SPARE	32	SENINF 2 Spare Register

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Address	Name	Width	Register Function
15008550	SENINF2_MUX_DATA	32	SENINF 2 Data Register
15008554	SENINF2_MUX_DATA_CNT	32	SENINF 2 Data Count Register
15008558	SENINF2_MUX_CROP	32	SENINF 2 Crop Size Register
15008920	SENINF3_MUX_CTRL	32	SENINF 3 Control Register
15008924	SENINF3_MUX_INTEN	32	SENINF 3 Interrupt Enable Register
15008928	SENINF3_MUX_INTSTA	32	SENINF 3 Interrupt Status Register
1500892C	SENINF3_MUX_SIZE	32	SENINF 3 Image Size Register
15008930	SENINF3_MUX_DEBUG_1	32	SENINF 3 Debug Register 1
15008934	SENINF3_MUX_DEBUG_2	32	SENINF 3 Debug Register 2
15008938	SENINF3_MUX_DEBUG_3	32	SENINF 3 Debug Register 3
1500893C	SENINF3_MUX_DEBUG_4	32	SENINF 3 Debug Register 4
15008940	SENINF3_MUX_DEBUG_5	32	SENINF 3 Debug Register 5
15008944	SENINF3_MUX_DEBUG_6	32	SENINF 3 Debug Register 6
15008948	SENINF3_MUX_DEBUG_7	32	SENINF 3 Debug Register 7
1500894C	SENINF3_MUX_SPARE	32	SENINF 3 Spare Register
15008950	SENINF3_MUX_DATA	32	SENINF 3 Data Register
15008954	SENINF3_MUX_DATA_CNT	32	SENINF 3 Data Count Register
15008958	SENINF3_MUX_CROP	32	SENINF 3 Crop Size Register
15008D20	SENINF4_MUX_CTRL	32	SENINF 4 Control Register
15008D24	SENINF4_MUX_INTEN	32	SENINF 4 Interrupt Enable Register
15008D28	SENINF4_MUX_INTSTA	32	SENINF 4 Interrupt Status Register
15008D2C	SENINF4_MUX_SIZE	32	SENINF 4 Image Size Register
15008D30	SENINF4_MUX_DEBUG_1	32	SENINF 4 Debug Register 1
15008D34	SENINF4_MUX_DEBUG_2	32	SENINF 4 Debug Register 2
15008D38	SENINF4_MUX_DEBUG_3	32	SENINF 4 Debug Register 3
15008D3C	SENINF4_MUX_DEBUG_4	32	SENINF 4 Debug Register 4
15008D40	SENINF4_MUX_DEBUG_5	32	SENINF 4 Debug Register 5
15008D44	SENINF4_MUX_DE	32	SENINF 4 Debug Register 6

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Address	Name	Width	Register Function
	BUG_6		
15008D48	SENINF4_MUX_DEBUG_7	32	SENINF 4 Debug Register 7
15008D4C	SENINF4_MUX_SPARE	32	SENINF 4 Spare Register
15008D50	SENINF4_MUX_DATA	32	SENINF 4 Data Register
15008D54	SENINF4_MUX_DATA_CNT	32	SENINF 4 Data Count Register
15008D58	SENINF4_MUX_CROP	32	SENINF 4 Crop Size Register

15008120 **SENINF1_MUX_CTRL** **SENINF 1 Control Register** **06DF0080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SENINF_MUX_EN**	**CROP_EN**	**FIFO_FULL_WR_EN**		**FIFO_FLUSH_EN**						**FIFO_PUSH_EN**					
Type	RW	RW	RW		RW						RW					
Reset	0	0	0	0	0	1	1	0	1	1	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SENINF_SRC_SEL**				**OVERRUN_RST_EN**	**SENINF_HSYNC_POL**	**SENINF_VSYNC_POL**	**SENINF_PIX_SEL**	**SENINF_HSYNC_MASK**						**SENINF_IRQ_SW_RST**	**SENINF_MUX_SW_RST**
Type	RW				RW	RW	RW	RW	RW						RW	RW
Reset	0	0	0	0	0	0	0	0	1						0	0

Bit(s)	Name	Description
31	SENINF_MUX_EN	**Enables seninf_mux** 0: Disable 1: Enable
30	CROP_EN	**Sensor crop function**
29:28	FIFO_FULL_WR_EN	0: FIFO write operation is prohibited when FIFO is full. 1: FIFO write operation is prohibited after FIFO full occurs. 2: FIFO write operation is allowed when FIFO is full.
27:22	FIFO_FLUSH_EN	**Normal mode: 6'b011011** JPEG two pixels mode: 6'b011000
21:16	FIFO_PUSH_EN	**Normal mode: 6'b011111** JPEG two pixels mode : 6'b011110
15:12	SENINF_SRC_SEL	**Selects SENINF input source** 0: CSI2 VC0 1: Test model 2: CCIR656 3: Parallel sensor 4: Serial sensor 6. CSI2 VC1 8: NCSI2 VC0 9: NCSI2 VC1 A: NCSI2 VC2

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Bit(s)	Name	Description
		B: NCSI2 VC3
11	OVERRUN_RST_EN	**Enables SENINF mux software reset for overrun** 0: No action 1: Auto self-reset for overrun situation
10	SENINF_HSYNC_POL	**SENINF hsync polarity**
9	SENINF_VSYNC_POL	**SENINF vsync polarity**
8	SENINF_PIX_SEL	**SENINF output bus width** 0: One pixel/cycle 1: Two pixels/cycle
7	SENINF_HSYNC_MASK	**Masks hsync** 0: Send hsync when vsync = 1 1: Does not send hsync when vsync = 1
1	SENINF_IRQ_SW_RST	**SENINF IRQ software reset** Active high 0: De-assert reset 1: Assert reset
0	SENINF_MUX_SW_RST	**SENINF mux software reset** Active high 0: De-assert reset 1: Assert reset

15008124 **SENINF1_MUX_INTEN** **SENINF 1 Interrupt Enable Register** **8000007F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_IRQ_CLR_SEL															
Type	RW															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SENINF_SENSOR_HSIZEERR_IRQ_EN	SENINF_SENSOR_VSIZEERR_IRQ_EN	SENINF_HSIZEERR_IRQ_EN	SENINF_VSIZEERR_IRQ_EN	SENINF_FSMERR_IRQ_EN	SENINF_CRCERR_IRQ_EN	SENINF_OVERRUN_IRQ_EN
Type										RW	RW	RW	RW	RW	RW	RW
Reset										1	1	1	1	1	1	1

Bit(s)	Name	Description
31	SENINF_IRQ_CLR_SEL	0: Read clear 1: Write clear
6	SENINF_SENSOR_HSIZEERR_IRQ_EN	Enables sensor HSIZE error IRQ

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Bit(s)	Name	Description
5	SENINF_SENSOR_VSIZEERR_IRQ_EN	Enables sensor VSIZE error IRQ
4	SENINF_HSIZEERR_IRQ_EN	Enables async FIFO HSIZE error IRQ
3	SENINF_VSIZEERR_IRQ_EN	Enables async FIFO VSIZE error IRQ
2	SENINF_FSMERR_IRQ_EN	Enables FSM error IRQ
1	SENINF_CRCERR_IRQ_EN	Enables CRR error IRQ
0	SENINF_OVERRUN_IRQ_EN	Enables FIFO overrun IRQ

15008128 **SENINF1_MUX_INTSTA** **SENINF 1 Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SENINF_SENSOR_HSIZEERR_IRQ_STA	SENINF_SENSOR_VSIZEERR_IRQ_STA	SENINF_HSIZEERR_IRQ_STA	SENINF_VSIZEERR_IRQ_STA	SENINF_FSMERR_IRQ_STA	SENINF_CRCERR_IRQ_STA	SENINF_OVERRUN_IRQ_STA
Type										RO	RO	RO	RO	RO	RO	RO
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	SENINF_SENSOR_HSIZEERR_IRQ_STA	Sensor HSIZE error IRQ status
5	SENINF_SENSOR_VSIZEERR_IRQ_STA	Sensor VSIZE error IRQ status
4	SENINF_HSIZEERR_IRQ_STA	Async FIFO HSIZE error IRQ status
3	SENINF_VSIZEERR_IRQ_STA	Async FIFO VSIZE error IRQ status
2	SENINF_FSMERR_IRQ_STA	FSM error IRQ status
1	SENINF_CRCERR_IRQ_STA	CRR error IRQ status
0	SENINF_OVERRUN_IRQ_STA	FIFO overrun IRQ status

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1500812C **SENINF1_MUX_SIZE** **SENINF 1 Image Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_HSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_VSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_HSIZE	Senor image horizontal size
15:0	SENINF_VSIZE	Senor image vertical size

15008130 **SENINF1_MUX_DEBUG_1** **SENINF 1 Debug Register 1** **0000C303**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO[15:0]															
Type	RO															
Reset	1	1	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

15008134 **SENINF1_MUX_DEBUG_2** **SENINF 1 Debug Register 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

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15008138 **SENINF1_MUX_DEBUG_3** **SENINF 1 Debug Register 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1500813C **SENINF1_MUX_DEBUG_4** **SENINF 1 Debug Register 4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

15008140 **SENINF1_MUX_DEBUG_5** **SENINF 1 Debug Register 5** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

15008144 **SENINF1_MUX_DEBUG_6** **SENINF 1 Debug Register 6** **00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DEBUG_INFO[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DEBUG_INFO[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

15008148 SENINF1_MUX_DEBUG_7 SENINF 1 Debug Register 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DEBUG_INFO[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DEBUG_INFO[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1500814C SENINF1_MUX_SPARE SENINF 1 Spare Register 000E2000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													**SENINF_SPARE[5:2]**			
Type													RW			
Reset													1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SENINF_SPARE[1:0]**		**SENINF_FIFO_FULL_SEL**	**SENINF_VCNT_SEL**		**SENINF_CRC_SEL**										
Type	RW		RW	RW		RW										
Reset	0	0	1	0	0	0	0									

Bit(s)	Name	Description
19:14	SENINF_SPARE	Spare register
13	SENINF_FIFO_FULL_SEL	0: Does not send FIFO full to cam 1: Send FIFO full to cam
12:11	SENINF_VCNT_SEL	0: Vsync rising 1: Vsync rising d1 2. Vsync rising d2 3: Vsync rising d3

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Bit(s)	Name	Description
10:9	SENINF_CRC_SEL	0: Vsync rising 1: Vsync rising d1 2. Vsync rising d2 3: Vsync rising d3

15008150 **SENINF1_MUX_DATA** **SENINF 1 Data Register** **40000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_DATA1															
Type	RO															
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_DATA0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_DATA1	
15:0	SENINF_DATA0	

15008154 **SENINF1_MUX_DATA_CNT** **SENINF 1 Data Count Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_DATA_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_DATA_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENINF_DATA_CNT	

15008158 **SENINF1_MUX_CROP** **SENINF 1 Crop Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_CROP_X2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_CROP_X1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:16	SENINF_CROP_X2	
15:0	SENINF_CROP_X1	

15008520 **SENINF2_MUX_CTRL** **SENINF 2 Control Register** **06DF0080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SENINF_MUX_EN**	**CROP_EN**	**FIFO_FULL_WR_EN**		**FIFO_FLUSH_EN**						**FIFO_PUSH_EN**					
Type	RW	RW	RW		RW						RW					
Reset	0	0	0	0	0	1	1	0	1	1	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SENINF_SRC_SEL**				**OVERRUN_RST_EN**	**SENINF_HSYNC_POL**	**SENINF_VSYNC_POL**	**SENINF_PIX_SEL**	**SENINF_HSYNC_MASK**						**SENINF_IRQ_SW_RST**	**SENINF_MUX_SW_RST**
Type	RW				RW	RW	RW	RW	RW						RW	RW
Reset	0	0	0	0	0	0	0	0	1						0	0

Bit(s)	Name	Description
31	SENINF_MUX_EN	**Enables seninf_mux** 0: Disable 1: Enable
30	CROP_EN	**Sensor crop function**
29:28	FIFO_FULL_WR_EN	**0: FIFO write operation is prohibited when FIFO is full.** 1: FIFO write operation is prohibited after FIFO full occurs. 2: FIFO write operation is allowed when FIFO is full.
27:22	FIFO_FLUSH_EN	**Normal mode: 6'b011011** JPEG two pixels mode: 6'b011000
21:16	FIFO_PUSH_EN	**Normal mode: 6'b011111** JPEG two pixels mode : 6'b011110
15:12	SENINF_SRC_SEL	**Selects SENINF input source** 0: CSI2 VC0 1: Test model 2: CCIR656 3: Parallel sensor 4: Serial sensor 6. CSI2 VC1 8: NCSI2 VC0 9: NCSI2 VC1 A: NCSI2 VC2 B: NCSI2 VC3
11	OVERRUN_RST_EN	**Enables SENINF mux software reset for overrun** 0: No action 1: Auto self-reset for overrun situation
10	SENINF_HSYNC_POL	**SENINF hsync polarity**
9	SENINF_VSYNC_POL	**SENINF vsync polarity**

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Bit(s)	Name	Description
8	SENINF_PIX_SEL	**SENINF output bus width** 0: One pixel/cycle 1: Two pixels/cycle
7	SENINF_HSYNC_MASK	**Masks hsync** 0: Send hsync when vsync = 1 1: Does not send hsync when vsync = 1
1	SENINF_IRQ_SW_RST	**SENINF IRQ software reset** Active high 0: De-assert reset 1: Assert reset
0	SENINF_MUX_SW_RST	**SENINF mux software reset** Active high 0: De-assert reset 1: Assert reset

15008524 **SENINF2_MUX_INTEN** **SENINF 2 Interrupt Enable Register** **8000007F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SENINF_IRQ_CLR_SEL**															
Type	RW															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**SENINF_SENSOR_HSIZEERR_IRQ_EN**	**SENINF_SENSOR_VSIZEERR_IRQ_EN**	**SENINF_HSIZEERR_IRQ_EN**	**SENINF_VSIZEERR_IRQ_EN**	**SENINF_FSMERR_IRQ_EN**	**SENINF_CRCERR_IRQ_EN**	**SENINF_OVERRUN_IRQ_EN**
Type										RW	RW	RW	RW	RW	RW	RW
Reset										1	1	1	1	1	1	1

Bit(s)	Name	Description
31	SENINF_IRQ_CLR_SEL	0: Read clear 1: Write clear
6	SENINF_SENSOR_HSIZEERR_IRQ_EN	Enables sensor HSIZE error IRQ
5	SENINF_SENSOR_VSIZEERR_IRQ_EN	Enables sensor VSIZE error IRQ
4	SENINF_HSIZEERR_IRQ_EN	Enables async FIFO HSIZE error IRQ
3	SENINF_VSIZEERR_IRQ_EN	Enables async FIFO VSIZE error IRQ
2	SENINF_FSMERR_IRQ_EN	Enables FSM error IRQ

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Bit(s)	Name	Description
1	SENINF_CRCERR_IRQ_EN	Enables CRR error IRQ
0	SENINF_OVERRUN_IRQ_EN	Enables FIFO overrun IRQ

15008528 SENINF2_MUX_INTSTA SENINF 2 Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SENINF_SENSOR_HSIZEERR_IRQ_STA	SENINF_SENSOR_VSIZEERR_IRQ_STA	SENINF_HSIZEERR_IRQ_STA	SENINF_VSIZEERR_IRQ_STA	SENINF_FSMERR_IRQ_STA	SENINF_CRCERR_IRQ_STA	SENINF_OVERRUN_IRQ_STA
Type										RO	RO	RO	RO	RO	RO	RO
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	SENINF_SENSOR_HSIZEERR_IRQ_STA	Sensor HSIZE error IRQ status
5	SENINF_SENSOR_VSIZEERR_IRQ_STA	Sensor VSIZE error IRQ status
4	SENINF_HSIZEERR_IRQ_STA	Async FIFO HSIZE error IRQ status
3	SENINF_VSIZEERR_IRQ_STA	Async FIFO VSIZE error IRQ status
2	SENINF_FSMERR_IRQ_STA	FSM error IRQ status
1	SENINF_CRCERR_IRQ_STA	CRR error IRQ status
0	SENINF_OVERRUN_IRQ_STA	FIFO overrun IRQ status

1500852C SENINF2_MUX_SIZE SENINF 2 Image Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_HSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_VSIZE															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_HSIZE	Senor image horizontal size
15:0	SENINF_VSIZE	Senor image vertical size

15008530 SENINF2_MUX_DEBUG_1 SENINF 2 Debug Register 1 0000C303

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO[15:0]															
Type	RO															
Reset	1	1	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

15008534 SENINF2_MUX_DEBUG_2 SENINF 2 Debug Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

15008538 SENINF2_MUX_DEBUG_3 SENINF 2 Debug Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1500853C **SENINF2_MUX_DEBUG_4** **SENINF 2 Debug Register 4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

15008540 **SENINF2_MUX_DEBUG_5** **SENINF 2 Debug Register 5** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

15008544 **SENINF2_MUX_DEBUG_6** **SENINF 2 Debug Register 6** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

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15008548 **SENINF2_MUX_DEBUG_7** **SENINF 2 Debug Register 7** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1500854C **SENINF2_MUX_SPARE** **SENINF 2 Spare Register** **000E2000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SENINF_SPARE[5:2]			
Type													RW			
Reset													1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_SPARE[1:0]		SENINF_FIFO_FULL_SEL	SENINF_VCNT_SEL		SENINF_CRC_SEL										
Type	RW		RW	RW		RW										
Reset	0	0	1	0	0	0	0									

Bit(s)	Name	Description
19:14	SENINF_SPARE	Spare register
13	SENINF_FIFO_FULL_SEL	0: Does not send FIFO full to cam 1: Send FIFO full to cam
12:11	SENINF_VCNT_SEL	0: Vsync rising 1: Vsync rising d1 2. Vsync rising d2 3: Vsync rising d3
10:9	SENINF_CRC_SEL	0: Vsync rising 1: Vsync rising d1 2. Vsync rising d2 3: Vsync rising d3

15008550 **SENINF2_MUX_DATA** **SENINF 2 Data Register** **40000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_DATA1															
Type	RO															

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Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_DATA0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_DATA1	
15:0	SENINF_DATA0	

15008554 **SENINF2_MUX_DATA_CNT** **SENINF 2 Data Count Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_DATA_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_DATA_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENINF_DATA_CNT	

15008558 **SENINF2_MUX_CROP** **SENINF 2 Crop Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_CROP_X2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_CROP_X1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_CROP_X2	
15:0	SENINF_CROP_X1	

15008920 **SENINF3_MUX_CTRL** **SENINF 3 Control Register** **06DF0080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_MUX_EN	CROP_EN	FIFO_FULL_WR_EN		FIFO_FLUSH_EN						FIFO_PUSH_EN					

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Type	RW	RW	RW		RW						RW					
Reset	0	0	0	0	0	1	1	0	1	1	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_SRC_SEL				OVERRUN_RST_EN	SENINF_HSYNC_POL	SENINF_VSYNC_POL	SENINF_PIX_SEL	SENINF_HSYNC_MASK						SENINF_IRQ_SW_RST	SENINF_MUX_SW_RST
Type	RW				RW	RW	RW	RW	RW						RW	RW
Reset	0	0	0	0	0	0	0	0	1						0	0

Bit(s)	Name	Description
31	SENINF_MUX_EN	**Enables seninf_mux** 0: Disable 1: Enable
30	CROP_EN	**Sensor crop function**
29:28	FIFO_FULL_WR_EN	**0: FIFO write operation is prohibited when FIFO is full.** 1: FIFO write operation is prohibited after FIFO full occurs. 2: FIFO write operation is allowed when FIFO is full.
27:22	FIFO_FLUSH_EN	**Normal mode : 6'b011011** JPEG two pixels mode: 6'b011000
21:16	FIFO_PUSH_EN	**Normal mode: 6'b011111** JPEG two pixels mode: 6'b011110
15:12	SENINF_SRC_SEL	**Selects SENINF input source** 0: CSI2 VC0 1: Test model 2: CCIR656 3: Parallel sensor 4: Serial sensor 6. CSI2 VC1 8: NCSI2 VC0 9: NCSI2 VC1 A: NCSI2 VC2 B: NCSI2 VC3
11	OVERRUN_RST_EN	**Enables SENINF mux software reset for overrun** 0: No action 1: Auto self-reset for overrun situation
10	SENINF_HSYNC_POL	**SENINF hsync polarity**
9	SENINF_VSYNC_POL	**SENINF vsync polarity**
8	SENINF_PIX_SEL	**SENINF output bus width** 0: One pixel/cycle 1: Two pixels/cycle
7	SENINF_HSYNC_MASK	**Masks hsync** 0: Send hsync when vsync = 1 1: Does not send hsync when vsync = 1
1	SENINF_IRQ_SW_RST	**SENINF IRQ software reset** Active high 0: De-assert reset 1: Assert reset
0	SENINF_MUX_SW_RST	**SENINF mux software reset** Active high 0: De-assert reset 1: Assert reset

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15008924	SENINF3_MUX_INTEN	SENINF 3 Interrupt Enable Register	8000007F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_IRQ_CLR_SEL															
Type	RW															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SENINF_SENSOR_HSIZEERR_IRQ_EN	SENINF_SENSOR_VSIZEERR_IRQ_EN	SENINF_HSIZEERR_IRQ_EN	SENINF_VSIZEERR_IRQ_EN	SENINF_FSMERR_IRQ_EN	SENINF_CRCERR_IRQ_EN	SENINF_OVERRUN_IRQ_EN
Type										RW	RW	RW	RW	RW	RW	RW
Reset										1	1	1	1	1	1	1

Bit(s)	Name	Description
31	SENINF_IRQ_CLR_SEL	0: Read clear 1: Write clear
6	SENINF_SENSOR_HSIZEERR_IRQ_EN	Enables sensor HSIZE error IRQ
5	SENINF_SENSOR_VSIZEERR_IRQ_EN	Enables sensor VSIZE error IRQ
4	SENINF_HSIZEERR_IRQ_EN	Enables async FIFO HSIZE error IRQ
3	SENINF_VSIZEERR_IRQ_EN	Enables async FIFO VSIZE error IRQ
2	SENINF_FSMERR_IRQ_EN	Enables FSM error IRQ
1	SENINF_CRCERR_IRQ_EN	Enables CRR error IRQ
0	SENINF_OVERRUN_IRQ_EN	Enables FIFO overrun IRQ

15008928	SENINF3_MUX_INTSTA	SENINF 3 Interrupt Status Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SENINF	SENINF	SENINF	SENINF_	SENINF	SENINF	SENINF

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										_SENSOR_HSIZEERR_IRQ_STA	_SENSOR_VSIZEERR_IRQ_STA	_HSIZEERR_IRQ_STA	VSIZEERR_IRQ_STA	_FSMERR_IRQ_STA	_CRCERR_IRQ_STA	_OVERRUN_IRQ_STA
Type										RO	RO	RO	RO	RO	RO	RO
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	SENINF_SENSOR_HSIZEERR_IRQ_STA	Sensor HSIZE error IRQ status
5	SENINF_SENSOR_VSIZEERR_IRQ_STA	Sensor VSIZE error IRQ status
4	SENINF_HSIZEERR_IRQ_STA	Async FIFO HSIZE error IRQ status
3	SENINF_VSIZEERR_IRQ_STA	Async FIFO VSIZE error IRQ status
2	SENINF_FSMERR_IRQ_STA	FSM error IRQ status
1	SENINF_CRCERR_IRQ_STA	CRR error IRQ status
0	SENINF_OVERRUN_IRQ_STA	FIFO overrun IRQ status

1500892C **SENINF3_MUX_SIZE** **SENINF 3 Image Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_HSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_VSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_HSIZE	Senor image horizontal size
15:0	SENINF_VSIZE	Senor image vertical size

15008930 **SENINF3_MUX_DEBUG_1** **SENINF 3 Debug Register 1** **0000C303**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	**DEBUG_INFO[15:0]**															
Type	RO															
Reset	1	1	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

15008934 **SENINF3_MUX_DEBUG_2** **SENINF 3 Debug Register 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DEBUG_INFO[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DEBUG_INFO[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

15008938 **SENINF3_MUX_DEBUG_3** **SENINF 3 Debug Register 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DEBUG_INFO[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DEBUG_INFO[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1500893C **SENINF3_MUX_DEBUG_4** **SENINF 3 Debug Register 4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DEBUG_INFO[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DEBUG_INFO[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

15008940 SENINF3_MUX_DEBUG_5 SENINF 3 Debug Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

15008944 SENINF3_MUX_DEBUG_6 SENINF 3 Debug Register 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

15008948 SENINF3_MUX_DEBUG_7 SENINF 3 Debug Register 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

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1500894C **SENINF3_MUX_SPARE** **SENINF 3 Spare Register** **000E2000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SENINF_SPARE[5:2]			
Type													RW			
Reset													1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_SPARE[1:0]		SENINF_FIFO_FULL_SEL	SENINF_VCNT_SEL		SENINF_CRC_SEL										
Type	RW		RW	RW		RW										
Reset	0	0	1	0	0	0	0									

Bit(s)	Name	Description
19:14	SENINF_SPARE	Spare register
13	SENINF_FIFO_FULL_SEL	0: Does not send FIFO full to cam 1: Send FIFO full to cam
12:11	SENINF_VCNT_SEL	0: Vsync rising 1: Vsync rising d1 2. Vsync rising d2 3: Vsync rising d3
10:9	SENINF_CRC_SEL	0: Vsync rising 1: Vsync rising d1 2. Vsync rising d2 3: Vsync rising d3

15008950 **SENINF3_MUX_DATA** **SENINF 3 Data Register** **40000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_DATA1															
Type	RO															
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_DATA0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_DATA1	
15:0	SENINF_DATA0	

15008954 **SENINF3_MUX_DATA_CNT** **SENINF 3 Data Count Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_DATA_CNT[31:16]															

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Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_DATA_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENINF_DATA_CNT	

15008958 SENINF3_MUX_CROP SENINF 3 Crop Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_CROP_X2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_CROP_X1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_CROP_X2	
15:0	SENINF_CROP_X1	

15008D20 SENINF4_MUX_CTRL SENINF 4 Control Register 06DF0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_MUX_EN	CROP_EN	FIFO_FULL_WR_EN		FIFO_FLUSH_EN						FIFO_PUSH_EN					
Type	RW	RW	RW		RW						RW					
Reset	0	0	0	0	0	1	1	0	1	1	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_SRC_SEL				OVERRUN_RST_EN	SENINF_HSYNC_POL	SENINF_VSYNC_POL	SENINF_PIX_SEL	SENINF_HSYNC_MASK						SENINF_IRQ_SW_RST	SENINF_MUX_SW_RST
Type	RW				RW	RW	RW	RW	RW						RW	RW
Reset	0	0	0	0	0	0	0	0	1						0	0

Bit(s)	Name	Description
31	SENINF_MUX_EN	**Enables seninf_mux** 0: Disable 1: Enable
30	CROP_EN	**Sensor crop function**
29:28	FIFO_FULL_WR_EN	**0: FIFO write operation is prohibited when FIFO is full.** 1: FIFO write operation is prohibited after FIFO full occurs.

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Bit(s)	Name	Description
		2: FIFO write operation is allowed when FIFO is full.
27:22	FIFO_FLUSH_EN	**MIPI: 6'b111011** MIPI JPEG two pixel mode: 6'b111000 Others: 6'b011011 other JPEG two pixel modes: 6'b011000
21:16	FIFO_PUSH_EN	**MIPI: 6'b111111** MIPI JPEG two pixel mode: 6'b111110 Others: 6'b011111 Other JPEG two pixel modes: 6'b011110
15:12	SENINF_SRC_SEL	**Selects SENINF input source** 0: CSI2 VC0 1: Test model 2: CCIR656 3: Parallel sensor 4: Serial sensor 6. CSI2 VC1 8: NCSI2 VC0 9: NCSI2 VC1 A: NCSI2 VC2 B: NCSI2 VC3
11	OVERRUN_RST_EN	**Enables SENINF mux software reset for overrun** 0: No action 1: Auto self-reset for overrun situation
10	SENINF_HSYNC_POL	**SENINF hsync polarity**
9	SENINF_VSYNC_POL	**SENING vsync polarity**
8	SENINF_PIX_SEL	**SENINF output bus width** 0: One pixel/cycle 1: Two pixels/cycle
7	SENINF_HSYNC_MASK	**Masks hsync** 0: Send hsync when vsync = 1 1: Does not send hsync when vsync = 1
1	SENINF_IRQ_SW_RST	**SENINF IRQ software reset** Active high 0: De-assert reset 1: Assert reset
0	SENINF_MUX_SW_RST	**SENINF mux software reset** Active high 0: De-assert reset 1: Assert reset

15008D24 **SENINF4_MUX_INTEN** **SENINF 4 Interrupt Enable Register** **8000007F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_IRQ_CLR_SEL															
Type	RW															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name										SENINF_SENSOR_HSIZEERR_IRQ_EN	SENINF_SENSOR_VSIZEERR_IRQ_EN	SENINF_HSIZEERR_IRQ_EN	SENINF_VSIZEERR_IRQ_EN	SENINF_FSMERR_IRQ_EN	SENINF_CRCERR_IRQ_EN	SENINF_OVERRUN_IRQ_EN
Type										RW	RW	RW	RW	RW	RW	RW
Reset										1	1	1	1	1	1	1

Bit(s)	Name	Description
31	SENINF_IRQ_CLR_SEL	0: Read clear 1: Write clear
6	SENINF_SENSOR_HSIZEERR_IRQ_EN	Enables sensor HSIZE error IRQ
5	SENINF_SENSOR_VSIZEERR_IRQ_EN	Enables sensor VSIZE error IRQ
4	SENINF_HSIZEERR_IRQ_EN	Enables async FIFO HSIZE error IRQ
3	SENINF_VSIZEERR_IRQ_EN	Enables async FIFO VSIZE error IRQ
2	SENINF_FSMERR_IRQ_EN	Enables FSM error IRQ
1	SENINF_CRCERR_IRQ_EN	Enables CRR error IRQ
0	SENINF_OVERRUN_IRQ_EN	Enables FIFO overrun IRQ

15008D28 **SENINF4_MUX_INTSTA** **SENINF 4 Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SENINF_SENSOR_HSIZEERR_IRQ_STA	SENINF_SENSOR_VSIZEERR_IRQ_STA	SENINF_HSIZEERR_IRQ_STA	SENINF_VSIZEERR_IRQ_STA	SENINF_FSMERR_IRQ_STA	SENINF_CRCERR_IRQ_STA	SENINF_OVERRUN_IRQ_STA
Type										RO	RO	RO	RO	RO	RO	RO
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	SENINF_SENSOR_HSIZEERR_IRQ_STA	Sensor HSIZE error IRQ status

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Bit(s)	Name	Description
5	SENINF_SENSOR_VSIZEERR_IRQ_STA	Sensor VSIZE error IRQ status
4	SENINF_HSIZEERR_IRQ_STA	Async FIFO HSIZE error IRQ status
3	SENINF_VSIZEERR_IRQ_STA	Async FIFO VSIZE error IRQ status
2	SENINF_FSMERR_IRQ_STA	FSM error IRQ status
1	SENINF_CRCERR_IRQ_STA	CRR error IRQ status
0	SENINF_OVERRUN_IRQ_STA	FIFO overrun IRQ status

15008D2C **SENINF4_MUX_SIZE** **SENINF 4 Image Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_HSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_VSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_HSIZE	Senor image horizontal size
15:0	SENINF_VSIZE	Senor image vertical size

15008D30 **SENINF4_MUX_DEBUG_1** **SENINF 4 Debug Register 1** **0000C303**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO[15:0]															
Type	RO															
Reset	1	1	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

15008D34 **SENINF4_MUX_DEBUG_2** **SENINF 4 Debug Register 2** **00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

15008D38 **SENINF4_MUX_DEBUG_3** **SENINF 4 Debug Register 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

15008D3C **SENINF4_MUX_DEBUG_4** **SENINF 4 Debug Register 4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

15008D40 **SENINF4_MUX_DEBUG_5** **SENINF 4 Debug Register 5** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

15008D44 **SENINF4_MUX_DEBUG_6** **SENINF 4 Debug Register 6** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

15008D48 **SENINF4_MUX_DEBUG_7** **SENINF 4 Debug Register 7** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

15008D4C **SENINF4_MUX_SPARE** **SENINF 4 Spare Register** **000E2000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SENINF_SPARE[5:2]			
Type													RW			
Reset													1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_SPARE[1:0]		SENINF_FIFO_FULL	SENINF_VCNT_SEL		SENINF_CRC_SEL										

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			_SE L													
Type	RW		RW	RW		RW										
Reset	0	0	1	0	0	0	0									

Bit(s)	Name	Description
19:14	SENINF_SPARE	Spare register
13	SENINF_FIFO_FULL_SEL	0: Does not send FIFO full to cam 1: Send FIFO full to cam
12:11	SENINF_VCNT_SEL	0: Vsync rising 1: Vsync rising d1 2. Vsync rising d2 3: Vsync rising d3
10:9	SENINF_CRC_SEL	0: Vsync rising 1: Vsync rising d1 2. Vsync rising d2 3: Vsync rising d3

15008D50 **SENINF4_MUX_DATA** **SENINF 4 Data Register** **40000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_DATA1															
Type	RO															
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_DATA0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_DATA1	
15:0	SENINF_DATA0	

15008D54 **SENINF4_MUX_DATA_CNT** **SENINF 4 Data Count Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_DATA_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_DATA_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENINF_DATA_CNT	

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15008D58 **SENINF4_MUX_CROP** **SENINF 4 Crop Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_CROP_X2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_CROP_X1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_CROP_X2	
15:0	SENINF_CROP_X1	

Module name: SCAM Base address: (+15008000h)

Address	Name	Width	Register Function
15008220	SCAM1_CFG	32	**SCAM1 Configuration Register** For global configuration of SCAM.
15008224	SCAM1_CON	32	**SCAM1 Control Register** Reset and enable
15008228	SCAM1_INT	32	**SCAM1 Interrupt Register** All INT* will still be toggled even when SCAM_CFG.INTEN* = 0.
1500822C	SCAM1_SIZE	32	SCAM1 Size Register
15008230	SCAM1_CFG2	32	SCAM1 Configuration Register 2
15008234	SCAM1_INFO0	32	SCAM1 INFO0 Register
15008238	SCAM1_INFO1	32	SCAM1 INFO1 Register
1500823C	SCAM1_INFO2	32	SCAM1 INFO2 Register
15008240	SCAM1_INFO3	32	SCAM1 INFO3 Register
15008244	SCAM1_INFO4	32	**SCAM1 INFO4 Register** Counters for debugging
15008248	SCAM1_INFO5	32	SCAM1 INFO5 Register

15008220 **SCAM1_CFG** **SCAM1 Configuration Register** **10000400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				WARN_MASK			CSD_NUM					DBG_MD			CONT	
Type				RW			RW					RW			RW	
Reset				1			0	0				0			0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CLK_INV		CYC				INTEN6	INTEN5	INTEN4	INTEN3	INTEN2	INTEN1	INTEN0
Type				RW		RW				RW	RW	RW	RW	RW	RW	RW
Reset				0		1	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28	**WARN_**	Warning_mask	**Warning mask before the first frame start packet**

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Bit(s)	Mnemonic	Name	Description
	MASK		0: All warnings will be recorded. 1: Warnings before the first frame start packet will not be recorded, i.e. no interrupt and no warning counter increasing.
25:24	**CSD_NUM**	CSD_NUM	**Number of CSD channels** 0: 1 data channel 1: 2 data channels 2: 4 data channels
20	**DBG_MD**	Debug_mode	**Enables debug mode** 0: Normal mode 1: Debug mode. CSD is not parsed or decoded, and raw data are transferred to CAMINF.
17	**CONT**	Continuous_mode	**Enables continuous mode** 0: Single run 1: Continuous run
12	**CLK_INV**	Clock_inverse	**Inverse latch for clock from sensor**
10:8	**CYC**	Cycle	**Cycle counts for rising of serial interface pixel clock after data are valid.**
6	**INTEN6**	INTEN6	**Enables interrupt of wrong size**
5	**INTEN5**	INTEN5	**Enables interrupt of wrong data ID**
4	**INTEN4**	INTEN4	**Enables interrupt of wrong line ID**
3	**INTEN3**	INTEN3	**Enables interrupt of wrong packet ID**
2	**INTEN2**	INTEN2	**Enables interrupt of wrong sync header**
1	**INTEN1**	INTEN1	**Enables interrupt of CRC error**
0	**INTEN0**	INTEN0	**Enables interrupt of frame end**

15008224 SCAM1_CON SCAM1 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RST
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ENA
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
16	**RST**	Reset	**Write 1 to stop SCAM immediately and keep in reset state.** Write 0 to enter the normal state. The software reset will not reset all register settings.
0	**ENA**	Enable	**Write 1 to start the SCAM.** Trigger SCAM before triggering the image sensor and clear RST before setting ENA = 1.

15008228 SCAM1_INT SCAM1 Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**INT6**	**INT5**	**INT4**	**INT3**	**INT2**	**INT1**	**INT0**
Type										RC	RC	RC	RC	RC	RC	RC
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6	**INT6**	INT6	Interrupt of wrong size
5	**INT5**	INT5	Interrupt of wrong data ID
4	**INT4**	INT4	Interrupt of wrong line ID
3	**INT3**	INT3	Interrupt of wrong packet ID
2	**INT2**	INT2	Interrupt of wrong sync header
1	**INT1**	INT1	Interrupt of CRC error
0	**INT0**	INT0	Interrupt of frame end

1500822C **SCAM1_SIZE** SCAM1 Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**HEIGHT**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**WIDTH**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**HEIGHT**	HEIGHT	**Height of picture** Must be set to the same as height information in frame start packet.
11:0	**WIDTH**	WIDTH	**Width of picture** Must be set to the same as width information in frame start packet.

15008230 **SCAM1_CFG2** SCAM1 Configuration Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RSV[30:15]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RSV[14:0]**															**DGC**
Type	RW															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
0	**DGC**	DIS_GATED_CLK	**Disables gated clock** Must be set to 1 when sent to TG2 or TG1 with aync line buffer mode (CAM+0x000 bit 10 = 1). 0: Generated PCLK sent to cam is gated when vsync is high or hsync is low. 1: Generated PCLK sent to cam is not gated when vsync is high or hsync is low.

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15008234	SCAM1_INFO0	SCAM1 INFO0 Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LID															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16	PSIZE	PACKET_SIZE	Packet information size of the most recent data packet
15:0	LID	LINE_ID	Line ID information of the most recent line start packet

15008238	SCAM1_INFO1	SCAM1 INFO1 Register	00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACTIVE	CRC_ON	DID						RSV							
Type	RO	RO	RO						RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:16	DCNT	DATA_CNT	Counter for current packet
15	ACTIVE	ACTIVE	Frame start packet is received, but frame end packet is not yet received.
14	CRC_ON	CRC_ON	CRC_ON information of the most recent frame start packet
13:8	DID	DATA_ID	Data ID information of the most recent frame start packet

1500823C	SCAM1_INFO2	SCAM1 INFO2 Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INFO2[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INFO2[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
31:0	**INFO2**	INFO2	

15008240 **SCAM1_INFO3** **SCAM1 INFO3 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INFO3[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INFO3[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**INFO3**	INFO3	

15008244 **SCAM1_INFO4** **SCAM1 INFO4 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					W_SIZE_CNT				W_DID_CNT				W_LID_CNT			
Type					RO				RO				RO			
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	W_PID_CNT				W_SYNC_CNT				W_CRC_CNT				FEND_CNT			
Type	RO				RO				RO				RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:24	**W_SIZE_CNT**	W_SIZE_CNT	**Counter of wrong size, up to 15** Cleared by SW reset, or write any value to clear all counters.
23:20	**W_DID_CNT**	W_DID_CNT	**Counter of wrong data ID, up to 15** Cleared by SW reset, or write any value to clear all counters.
19:16	**W_LID_CNT**	W_LID_CNT	**Counter of wrong line ID, up to 15** Cleared by SW reset, or write any value to clear all counters.
15:12	**W_PID_CNT**	W_PID_CNT	**Counter of wrong packet ID, up to 15** Cleared by SW reset, or write any value to clear all counters.
11:8	**W_SYNC_CNT**	W_SYNC_CNT	**Counter of wrong sync header, up to 15** Cleared by SW reset, or write any value to clear all counters.
7:4	**W_CRC_CNT**	W_CRC_CNT	**Counter of CRC error, up to 15** Cleared by SW reset, or write any value to clear all counters.
3:0	**FEND_CNT**	FEND_CNT	**Counter of frame end, free running counter** Cleared by SW reset, or write any value to clear all counters.

15008248 **SCAM1_INFO5** **SCAM1 INFO5 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	INFO5[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INFO5[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**INFO5**	INFO5	

Module name: ncsi2 Base address: (+15008000h)

Address	Name	Width	Register Function
150083A0	SENINF1_NCSI2_CTL	32	CSI2 Function Enable
150083A4	SENINF1_NCSI2_LNRC_TIMING	32	CSI2 Clock Lane Timing Parameters
150083A8	SENINF1_NCSI2_LNRD_TIMING	32	CSI2 Data Lane Timing Parameters
150083AC	SENINF1_NCSI2_DPCM	32	CSI2 DPCM Parameters
150083B0	SENINF1_NCSI2_INT_EN	32	CSI2 Interrupt Enable
150083B4	SENINF1_NCSI2_INT_STATUS	32	CSI2 Interrupt Status
150083B8	SENINF1_NCSI2_DGB_SEL	32	CSI2 Debug Selection
150083BC	SENINF1_NCSI2_DBG_PORT	32	CSI2 Debug Port
150083C0	SENINF1_NCSI2_SPARE0	32	SPARE0
150083C4	SENINF1_NCSI2_SPARE1	32	SPARE1
150083C8	SENINF1_NCSI2_LNRC_FSM	32	CSI2 Clock Lane RX FSM
150083CC	SENINF1_NCSI2_LNRD_FSM	32	CSI2 Data Lane RX FSM
150083D0	SENINF1_NCSI2_FRAME_LINE_NUM	32	CSI2 Frame/Line Number
150083D4	SENINF1_NCSI2_GENERIC_SHORT	32	CSI2 Generic Short Packet
150083D8	SENINF1_NCSI2_HSRX_DBG	32	CSI2 HSRX Enable
150083DC	SENINF1_NCSI2_DI	32	CSI2 Data Interleaving Parameters
150083E0	SENINF1_NCSI2_HS_TRAIL	32	CSI2 HS Trail Timing Parameters
150083E4	SENINF1_NCSI2_DI_CTRL	32	CSI2 Data Interleaving Control
150087A0	SENINF2_NCSI2_CTL	32	CSI2 Function Enable
150087A4	SENINF2_NCSI2_LNRC_TIMING	32	CSI2 Clock Lane Timing Parameters

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Address	Name	Width	Register Function
150087A8	SENINF2_NCSI2_LNRD_TIMING	32	CSI2 Data Lane Timing Parameters
150087AC	SENINF2_NCSI2_DPCM	32	CSI2 DPCM Parameters
150087B0	SENINF2_NCSI2_INT_EN	32	CSI2 Interrupt Enable
150087B4	SENINF2_NCSI2_INT_STATUS	32	CSI2 Interrupt Status
150087B8	SENINF2_NCSI2_DGB_SEL	32	CSI2 Debug Selection
150087BC	SENINF2_NCSI2_DBG_PORT	32	CSI2 Debug Port
150087C0	SENINF2_NCSI2_SPARE0	32	SPARE0
150087C4	SENINF2_NCSI2_SPARE1	32	SPARE1
150087C8	SENINF2_NCSI2_LNRC_FSM	32	CSI2 Clock Lane RX FSM
150087CC	SENINF2_NCSI2_LNRD_FSM	32	CSI2 Data Lane RX FSM
150087D0	SENINF2_NCSI2_FRAME_LINE_NUM	32	CSI2 Frame/Line Number
150087D4	SENINF2_NCSI2_GENERIC_SHORT	32	CSI2 Generic Short Packet
150087D8	SENINF2_NCSI2_HSRX_DBG	32	CSI2 HSRX Enable
150087DC	SENINF2_NCSI2_DI	32	CSI2 Data Interleaving Parameters
150087E0	SENINF2_NCSI2_HS_TRAIL	32	CSI2 HS Trail Timing Parameters
150087E4	SENINF2_NCSI2_DI_CTRL	32	CSI2 Data Interleaving Control

150083A0 SENINF1_NCSI2_CTL CSI2 Function Enable 01886160

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			VS_OUT_CYCLE_NUMBER		CLOCK_HS_OPTION	REF_SYNC_DET_EN	HS_TRAIL_EN	ASYNC_FIFO_RST_SCH		SYNC_DET_BITSWAP_EN	SYNC_DET_EN	SYNC_DET_SCHEME	FLUSH_MODE			ED_SEL
Type			RW		RW	RW	RW	RW		RW	RW	RW	RW			RW
Reset			0	0	0	0	0	1	1	0	0	0	1	0		0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VS_TYPE	BYTE2PIXEL_EN	IMAGE_PACKET_EN	GENERIC_LONG_PACKET_EN			HS_END_EN	HS_PRPR_EN	HSRX_DET_EN	CRC_EN	ECC_EN	CLOCK_LANE_EN	DATA_LANE3_EN	DATA_LANE2_EN	DATA_LANE1_EN	DATA_LANE0_EN
Type	RW	RW	RW	RW			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	1	1	0			0	1	0	1	1	0	0	0	0	0

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Bit(s)	Name	Description
29:28	VS_OUT_CYCLE_NUMBER	0: 4T 1: 8T
27	CLOCK_HS_OPTION	0: Enable clock lane HS based on LP11, LP01, LP00 1: Enable clock lane HS based on LP00
26	REF_SYNC_DET_EN	**Reference sync detect signal for analog sync**
25	HS_TRAIL_EN	**Extends HS trail**
24:23	ASYNC_FIFO_RST_SCH	
22	SYNC_DET_BITSWAP_EN	
21	SYNC_DET_EN	**Enables sync sequence detection**
20	SYNC_DET_SCHEME	0: B8 1: 101110
19:18	FLUSH_MODE	0: Disable 1: Flush at first cycle of LP11 2. Flush at LP11 3: Reserved
16	ED_SEL	0: {WCH,WCL,DI} 1: {DI,WCL,WCH}
15	VS_TYPE	**VS type** 0: 4T 1: Frame start to frame end
14	BYTE2PIXEL_EN	**Byte 2 pixel conversion**
13	IMAGE_PACKET_EN	**Image data types**
12	GENERIC_LONG_PACKET_EN	**Generic long packet data types**
9	HS_END_EN	**Enables HS_EX reset at packet end**
8	HS_PRPR_EN	**Enables RX_HS_PRPR state**
7	HSRX_DET_EN	**Enables HSRX termination auto-detection flow**
6	CRC_EN	**Enables checksum**
5	ECC_EN	**Enables packet header ECC**
4	CLOCK_LANE_EN	**Enables clock lane**
3	DATA_LANE3_EN	**Enables Data Lane 3**
2	DATA_LANE2_EN	**Enables Data Lane 2**
1	DATA_LANE1_EN	**Enables Data Lane 1**
0	DATA_LANE0_EN	**Enables Data Lane 0**

150083A4 **SENINF1_NCSI2_LNRC_TIMING** **CSI2 Clock Lane Timing Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	SETTLE_PARAMETER								TERM_PARAMETER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	SETTLE_PARAMETER	TD_SETTLE parameter
7:0	TERM_PARAMETER	TD_TERM_EN parameter

150083A8 **SENINF1_NCSI2_LNRD_TIMING** **CSI2 Data Lane Timing Parameters** **00002000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SETTLE_PARAMETER								TERM_PARAMETER							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	SETTLE_PARAMETER	TD_SETTLE parameter
7:0	TERM_PARAMETER	TD_TERM_EN parameter

150083AC **SENINF1_NCSI2_DPCM** **CSI2 DPCM Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DI_2A_DPCM_EN	DI_37_DPCM_EN	DI_36_DPCM_EN	DI_35_DPCM_EN	DI_34_DPCM_EN	DI_33_DPCM_EN	DI_32_DPCM_EN	DI_31_DPCM_EN	DI_30_DPCM_EN				DPCM_MODE			
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW				RW			
Reset	0	0	0	0	0	0	0	0	0				0	0	0	0

Bit(s)	Name	Description
15	DI_2A_DPCM_EN	Enables DPCM
14	DI_37_DPCM_EN	Enables DPCM
13	DI_36_DPCM_EN	Enables DPCM
12	DI_35_DPCM_EN	Enables DPCM
11	DI_34_DPCM_EN	Enables DPCM
10	DI_33_DPCM_EN	Enables DPCM
9	DI_32_DPCM_EN	Enables DPCM

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Bit(s)	Name	Description
8	DI_31_DPCM_EN	Enables DPCM
7	DI_30_DPCM_EN	Enables DPCM
3:0	DPCM_MODE	0: 10-8-10

150083B0 **SENINF1_NCSI2_INT_EN** **CSI2 Interrupt Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_WCLR_EN												ERR_FRAME_SYNC_S3	ERR_FRAME_SYNC_S2	ERR_FRAME_SYNC_S1	ERR_FRAME_SYNC_S0
Type	RW												RW	RW	RW	RW
Reset	0												0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GS	LS	FS	ERR_SOT_SYNC_HS_LNRD3	ERR_SOT_SYNC_HS_LNRD2	ERR_SOT_SYNC_HS_LNRD1	ERR_SOT_SYNC_HS_LNRD0	ERR_MULTI_LANE_SYNC	ERR_AFIFO	ERR_CRC	ERR_ECC_DOUBLE	ERR_ECC_CORRECTED	ERR_ECC_NO_ERROR	ERR_ID	ERR_FRAME_SYNC
Type		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	INT_WCLR_EN	Enables interrupt write clear
19	ERR_FRAME_SYNC_S3	Enables ERR_FRAME_SYNC interrupt
18	ERR_FRAME_SYNC_S2	Enables ERR_FRAME_SYNC interrupt
17	ERR_FRAME_SYNC_S1	Enables ERR_FRAME_SYNC interrupt
16	ERR_FRAME_SYNC_S0	Enables ERR_FRAME_SYNC interrupt t
14	GS	Enables generic short packet interrupt
13	LS	Enables line start interrupt
12	FS	Enables frame start interrupt
11	ERR_SOT_SYNC_HS_LNRD3	Enables ERR_SOT_SYNC_HS interrupt
10	ERR_SOT_SYNC_HS_LNRD2	Enables ERR_SOT_SYNC_HS interrupt
9	ERR_SOT_SYNC_HS_LNRD1	Enables ERR_SOT_SYNC_HS interrupt
8	ERR_SOT_SYNC_HS_LNRD0	Enables ERR_SOT_SYNC_HS interrupt
7	ERR_MULTI_LANE_SYNC	Enables ERR_MULTI_LANE_SYNC interrupt
6	ERR_AFIFO	Enables ERR_AFIFO interrupt
5	ERR_CRC	Enables ERR_CRC interrupt

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Bit(s)	Name	Description
4	ERR_ECC_DOUBLE	Enables ERR_ECC_DOUBLE interrupt
3	ERR_ECC_CORRECTED	Enables ERR_ECC_CORRECTED interrupt
2	ERR_ECC_NO_ERROR	ERR_ECC_NO_ERROR interrupt
1	ERR_ID	Enables ERR_ID interrupt
0	ERR_FRAME_SYNC	Enables ERR_FRAME_SYNC interrupt

150083B4 **SENINF1_NCSI2_INT_STATUS** **CSI2 Interrupt Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													ERR_FRAME_SYNC_S3	ERR_FRAME_SYNC_S2	ERR_FRAME_SYNC_S1	ERR_FRAME_SYNC_S0
Type													RO	RO	RO	RO
Reset													0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name		GS	LS	FS	ERR_SOT_SYNC_HS_LNRD3	ERR_SOT_SYNC_HS_LNRD2	ERR_SOT_SYNC_HS_LNRD1	ERR_SOT_SYNC_HS_LNRD0	ERR_MULTI_LANE_SYNC	ERR_AFIFO	ERR_CRC	ERR_ECC_DOUBLE	ERR_ECC_CORRECTED	ERR_ECC_NO_ERROR	ERR_ID	ERR_FRAME_SYNC
Type		RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	ERR_FRAME_SYNC_S3	Asserted when a Frame End is not paired with a Frame Start on the same virtual channel
18	ERR_FRAME_SYNC_S2	Asserted when a Frame End is not paired with a Frame Start on the same virtual channel
17	ERR_FRAME_SYNC_S1	Asserted when a Frame End is not paired with a Frame Start on the same virtual channel
16	ERR_FRAME_SYNC_S0	Asserted when a Frame End is not paired with a Frame Start on the same virtual channel
14	GS	Enables generic short packet interrupt
13	LS	Line start interrupt
12	FS	Frame start interrupt
11	ERR_SOT_SYNC_HS_LNRD3	Asserted when proper synchronization cannot be expected
10	ERR_SOT_SYNC_HS_LNRD2	Asserted when proper synchronization cannot be expected
9	ERR_SOT_SYNC_HS_LNRD1	Asserted when proper synchronization cannot be expected
8	ERR_SOT_SYNC_HS_LNRD0	Asserted when proper synchronization cannot be expected

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Bit(s)	Name	Description
7	ERR_MULTI_LANE_SYNC	Asserted when multiple lane synchronization fails
6	ERR_AFIFO	Asserted when error occurs in asynchronous FIFO
5	ERR_CRC	Asserted when the computed CRC code is different from the received CRC code
4	ERR_ECC_DOUBLE	Asserted when an ECC syndrome is computed and two bit-errors are detected in the received packet header
3	ERR_ECC_CORRECTED	Asserted when an ECC syndrome is computed and a single bit-error in the packet header is detected and corrected
2	ERR_ECC_NO_ERROR	**Asserted when an ECC syndrome is computed and the result is 0 indicating a packet header that is considered to be without errors or has more than two bit errors** CSI-2's ECC mechanism cannot detect this type of error.
1	ERR_ID	Asserted when a packet header is decoded with an unrecognized or unimplemented data ID
0	ERR_FRAME_SYNC	Asserted when a Frame End is not paired with a Frame Start on the same virtual channel

150083B8 **SENINF1_NCSI2_DGB_SEL** **CSI2 Debug Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name									DEBUG_SEL							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DEBUG_SEL	Selects debugging

150083BC **SENINF1_NCSI2_DBG_PORT** **CSI2 Debug Port** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CTL_DBG_PORT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	CTL_DBG_PORT	Debugging port

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150083C0 SENINF1_NCSI2_SPARE0 SPARE0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE0	Spare register

150083C4 SENINF1_NCSI2_SPARE1 SPARE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE1	Spare register

150083C8 SENINF1_NCSI2_LNRC_FSM CSI2 Clock Lane RX FSM 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											LNRC_RX_FSM					
Type											RO					
Reset											0	0	0	0	0	1

Bit(s)	Name	Description
5:0	LNRC_RX_FSM	RX FSM of clock lane

150083CC SENINF1_NCSI2_LNRD_FSM CSI2 Data Lane RX FSM 01010101

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		LNRD3_RX_FSM								LNRD2_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		LNRD1_RX_FSM								LNRD0_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1

Bit(s)	Name	Description
30:24	LNRD3_RX_FSM	RX FSM of Data Lane 3
22:16	LNRD2_RX_FSM	RX FSM of Data Lane 2
14:8	LNRD1_RX_FSM	RX FSM of Data Lane 1
6:0	LNRD0_RX_FSM	RX FSM of Data Lane 0

150083D0	SENINF1_NCSI2_FRAME_LINE_NUM	CSI2 Frame/Line Number	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LINE_NUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FRAME_NUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	LINE_NUM	Line number
15:0	FRAME_NUM	Frame number

150083D4	SENINF1_NCSI2_GENERIC_SHORT	CSI2 Generic Short Packet	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GENERIC_SHORT_PACKET_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											GENERIC_SHORT_PACKET_DT					
Type											RO					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
31:16	GENERIC_SHORT_PACKET_DATA	Generic short packet data
5:0	GENERIC_SHORT_PACKET_DT	Generic short packet data

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150083D8 SENINF1_NCSI2_HSRX_DBG CSI2 HSRX Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CLOCK_LANE_HSRX_EN	DATA_LANE3_HSRX_EN	DATA_LANE2_HSRX_EN	DATA_LANE1_HSRX_EN	DATA_LANE0_HSRX_EN
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	CLOCK_LANE_HSRX_EN	Enables clock lane HSRX circuit
3	DATA_LANE3_HSRX_EN	Enables Data Lane 3 HSRX circuit
2	DATA_LANE2_HSRX_EN	Enables Data Lane 2 HSRX circuit
1	DATA_LANE1_HSRX_EN	Enables Data Lane 1 HSRX circuit
0	DATA_LANE0_HSRX_EN	Enables Data Lane 0 HSRX circuit

150083DC SENINF1_NCSI2_DI CSI2 Data Interleaving Parameters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DT3						VC3		DT2						VC2	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DT1						VC1		DT0						VC0	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:26	DT3	Data type identifier
25:24	VC3	Virtual channel identifier
23:18	DT2	Data type identifier
17:16	VC2	Virtual channel identifier
15:10	DT1	Data type identifier
9:8	VC1	Virtual channel identifier
7:2	DT0	Data type identifier
1:0	VC0	Virtual channel identifier

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150083E0 SENINF1_NCSI2_HS_TRAIL CSI2 HS Trail Timing Parameters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									HS_TRAIL_PARAMETER							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	HS_TRAIL_PARAMETER	HS trail parameter

150083E4 SENINF1_NCSI2_DI_CTRL CSI2 Data Interleaving Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						DT3_INTERLEAVING		VC3_INTERLEAVING						DT2_INTERLEAVING		VC2_INTERLEAVING
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DT1_INTERLEAVING		VC1_INTERLEAVING						DT0_INTERLEAVING		VC0_INTERLEAVING
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0

Bit(s)	Name	Description
26:25	DT3_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
24	VC3_INTERLEAVING	**Virtual channel identifier interleaving**
18:17	DT2_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
16	VC2_INTERLEAVING	**Virtual channel identifier interleaving**
10:9	DT1_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude

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Bit(s)	Name	Description
8	VC1_INTERLEAVING	**Virtual channel identifier interleaving**
2:1	DT0_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
0	VC0_INTERLEAVING	**Virtual channel identifier interleaving**

150087A0 **SENINF2_N CSI2_CTL** **CSI2 Function Enable** **01886160**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			VS_OUT_CYCLE_NUMBER		CLOCK_HS_OPTION	REF_SYNC_DET_EN	HS_TRAIL_EN	ASYNC_FIFO_RST_SCH		SYNC_DET_BITSWAP_EN	SYNC_DET_EN	SYNC_DET_SCHEME	FLUSH_MODE			ED_SEL
Type			RW		RW	RW	RW	RW		RW	RW	RW	RW			RW
Reset			0	0	0	0	0	1	1	0	0	0	1	0		0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VS_TYPE	BYTE2PIXEL_EN	IMAGE_PACKET_EN	GENERIC_LONG_PACKET_EN			HS_END_EN	HS_PRPR_EN	HSRX_DET_EN	CRC_EN	ECC_EN	CLOCK_LANE_EN	DATA_LANE3_EN	DATA_LANE2_EN	DATA_LANE1_EN	DATA_LANE0_EN
Type	RW	RW	RW	RW			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	1	1	0			0	1	0	1	1	0	0	0	0	0

Bit(s)	Name	Description
29:28	VS_OUT_CYCLE_NUMBER	0: 4T 1: 8T
27	CLOCK_HS_OPTION	0: Enable clock lane HS based on LP11, LP01, LP00 1: Enable clock lane HS based on LP00
26	REF_SYNC_DET_EN	**Reference sync detect signal for analog sync**
25	HS_TRAIL_EN	**Extends HS trail**
24:23	ASYNC_FIFO_RST_SCH	
22	SYNC_DET_BITSWAP_EN	
21	SYNC_DET_EN	**Enables sync sequence detection**
20	SYNC_DET_SCHEME	0: B8 1: 101110
19:18	FLUSH_MODE	0: Disable 1: Flush at first cycle of LP11 2. Flush at LP11 3: Reserved
16	ED_SEL	0: {WCH,WCL,DI} 1: {DI,WCL,WCH}

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Bit(s)	Name	Description
15	VS_TYPE	**VS type** 0: 4T 1: Frame start to frame end
14	BYTE2PIXEL_EN	**Byte 2 pixel conversion**
13	IMAGE_PACKET_EN	**Image data types**
12	GENERIC_LONG_PACKET_EN	**Generic long packet data types**
9	HS_END_EN	**Enables HS_EX reset at packet end**
8	HS_PRPR_EN	**Enables RX_HS_PRPR state**
7	HSRX_DET_EN	**Enables HSRX termination auto-detection flow**
6	CRC_EN	**Enables checksum**
5	ECC_EN	**Enables packet header ECC**
4	CLOCK_LANE_EN	**Enables clock lane**
3	DATA_LANE3_EN	**Enables Data Lane 3**
2	DATA_LANE2_EN	**Enables Data Lane 2**
1	DATA_LANE1_EN	**Enables Data Lane 1**
0	DATA_LANE0_EN	**Enables Data Lane 0**

150087A4 SENINF2_NCSI2_LNRC_TIMING CSI2 Clock Lane Timing Parameters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SETTLE_PARAMETER								TERM_PARAMETER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	SETTLE_PARAMETER	TD_SETTLE parameter
7:0	TERM_PARAMETER	TD_TERM_EN parameter

150087A8 SENINF2_NCSI2_LNRD_TIMING CSI2 Data Lane Timing Parameters 00002000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SETTLE_PARAMETER								TERM_PARAMETER							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:8	SETTLE_PARAMETER	TD_SETTLE parameter
7:0	TERM_PARAMETER	TD_TERM_EN parameter

150087AC **SENINF2_N CSI2_DPCM** **CSI2 DPCM Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DI_2A_DPCM_EN	DI_37_DPCM_EN	DI_36_DPCM_EN	DI_35_DPCM_EN	DI_34_DPCM_EN	DI_33_DPCM_EN	DI_32_DPCM_EN	DI_31_DPCM_EN	DI_30_DPCM_EN				DPCM_MODE			
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW				RW			
Reset	0	0	0	0	0	0	0	0	0				0	0	0	0

Bit(s)	Name	Description
15	DI_2A_DPCM_EN	Enables DPCM
14	DI_37_DPCM_EN	Enables DPCM
13	DI_36_DPCM_EN	Enables DPCM
12	DI_35_DPCM_EN	Enables DPCM
11	DI_34_DPCM_EN	Enables DPCM
10	DI_33_DPCM_EN	Enables DPCM
9	DI_32_DPCM_EN	Enables DPCM
8	DI_31_DPCM_EN	Enables DPCM
7	DI_30_DPCM_EN	Enables DPCM
3:0	DPCM_MODE	0: 10-8-10

150087B0 **SENINF2_N CSI2_INT_EN** **CSI2 Interrupt Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_WCLR_EN												ERR_FRAME_SYNC_S3	ERR_FRAME_SYNC_S2	ERR_FRAME_SYNC_S1	ERR_FRAME_SYNC_S0
Type	RW												RW	RW	RW	RW
Reset	0												0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name		GS	LS	FS	ERR_SOT_SYNC_HS_LN	ERR_SOT_SYNC_HS_LN	ERR_SOT_SYNC_HS_LN	ERR_SOT_SYNC_HS_LN	ERR_MULTI_LANE_SYNC	ERR_AFIFO	ERR_CRC	ERR_ECC_DOUBLE	ERR_ECC_CORRECTED	ERR_ECC_NO_ERROR	ERR_ID	ERR_FRAME_SYNC

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					RD3	RD2	RD1	RD0								
Type		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	INT_WCLR_EN	Enables interrupt write clear
19	ERR_FRAME_SYNC_S3	Enables ERR_FRAME_SYNC interrupt
18	ERR_FRAME_SYNC_S2	Enables ERR_FRAME_SYNC interrupt
17	ERR_FRAME_SYNC_S1	Enables ERR_FRAME_SYNC interrupt
16	ERR_FRAME_SYNC_S0	Enables ERR_FRAME_SYNC interrupt t
14	GS	Enables generic short packet interrupt
13	LS	Enables line start interrupt
12	FS	Enables frame start interrupt
11	ERR_SOT_SYNC_HS_LNRD3	Enables ERR_SOT_SYNC_HS interrupt
10	ERR_SOT_SYNC_HS_LNRD2	Enables ERR_SOT_SYNC_HS interrupt
9	ERR_SOT_SYNC_HS_LNRD1	Enables ERR_SOT_SYNC_HS interrupt
8	ERR_SOT_SYNC_HS_LNRD0	Enables ERR_SOT_SYNC_HS interrupt
7	ERR_MULTI_LANE_SYNC	Enables ERR_MULTI_LANE_SYNC interrupt
6	ERR_AFIFO	Enables ERR_AFIFO interrupt
5	ERR_CRC	Enables ERR_CRC interrupt
4	ERR_ECC_DOUBLE	Enables ERR_ECC_DOUBLE interrupt
3	ERR_ECC_CORRECTED	Enables ERR_ECC_CORRECTED interrupt
2	ERR_ECC_NO_ERROR	ERR_ECC_NO_ERROR interrupt
1	ERR_ID	Enables ERR_ID interrupt
0	ERR_FRAME_SYNC	Enables ERR_FRAME_SYNC interrupt

150087B4	**SENINF2_NCSI2_INT_STATUS**	**CSI2 Interrupt Status**	**00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													**ERR_FRAME_SYNC_S3**	**ERR_FRAME_SYNC_S2**	**ERR_FRAME_SYNC_S1**	**ERR_FRAME_SYNC_S0**
Type													RO	RO	RO	RO
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name		GS	LS	FS	ERR_SOT_SYNC_HS_LNRD3	ERR_SOT_SYNC_HS_LNRD2	ERR_SOT_SYNC_HS_LNRD1	ERR_SOT_SYNC_HS_LNRD0	ERR_MULTI_LANE_SYNC	ERR_AFIFO	ERR_CRC	ERR_ECC_DOUBLE	ERR_ECC_CORRECTED	ERR_ECC_NO_ERROR	ERR_ID	ERR_FRAME_SYNC
Type		RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	ERR_FRAME_SYNC_S3	Asserted when a Frame End is not paired with a Frame Start on the same virtual channel
18	ERR_FRAME_SYNC_S2	Asserted when a Frame End is not paired with a Frame Start on the same virtual channel
17	ERR_FRAME_SYNC_S1	Asserted when a Frame End is not paired with a Frame Start on the same virtual channel
16	ERR_FRAME_SYNC_S0	Asserted when a Frame End is not paired with a Frame Start on the same virtual channel
14	GS	Enables generic short packet interrupt
13	LS	Line start interrupt
12	FS	Frame start interrupt
11	ERR_SOT_SYNC_HS_LNRD3	Asserted when proper synchronization cannot be expected
10	ERR_SOT_SYNC_HS_LNRD2	Asserted when proper synchronization cannot be expected
9	ERR_SOT_SYNC_HS_LNRD1	Asserted when proper synchronization cannot be expected
8	ERR_SOT_SYNC_HS_LNRD0	Asserted when proper synchronization cannot be expected
7	ERR_MULTI_LANE_SYNC	Asserted when multiple lane synchronization fails
6	ERR_AFIFO	Asserted when error occurs in asynchronous FIFO
5	ERR_CRC	Asserted when the computed CRC code is different from the received CRC code
4	ERR_ECC_DOUBLE	Asserted when an ECC syndrome is computed and two bit-errors are detected in the received packet header
3	ERR_ECC_CORRECTED	Asserted when an ECC syndrome is computed and a single bit-error in the packet header is detected and corrected
2	ERR_ECC_NO_ERROR	**Asserted when an ECC syndrome is computed and the result is 0 indicating a packet header that is considered to be without errors or has more than two bit errors** CSI-2's ECC mechanism cannot detect this type of error.
1	ERR_ID	Asserted when a packet header is decoded with an unrecognized or unimplemented data ID
0	ERR_FRAME_SYNC	Asserted when a Frame End is not paired with a Frame Start on the same virtual channel

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150087B8	SENINF2_NCSI2_DGB_SEL	CSI2 Debug Selection	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

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Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**DEBUG_SEL**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DEBUG_SEL	Selects debugging

150087BC **SENINF2_NCSI2_DBG_PORT** **CSI2 Debug Port** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CTL_DBG_PORT**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	CTL_DBG_PORT	Debugging port

150087C0 **SENINF2_NCSI2_SPARE0** **SPARE0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SPARE0[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SPARE0[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE0	Spare register

150087C4 **SENINF2_NCSI2_SPARE1** **SPARE1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SPARE1[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SPARE1[15:0]**															

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Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE1	Spare register

150087C8 SENINF2_NCSI2_LNRC_FSM CSI2 Clock Lane RX FSM 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											LNRC_RX_FSM					
Type											RO					
Reset											0	0	0	0	0	1

Bit(s)	Name	Description
5:0	LNRC_RX_FSM	RX FSM of clock lane

150087CC SENINF2_NCSI2_LNRD_FSM CSI2 Data Lane RX FSM 01010101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		LNRD3_RX_FSM								LNRD2_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		LNRD1_RX_FSM								LNRD0_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1

Bit(s)	Name	Description
30:24	LNRD3_RX_FSM	RX FSM of Data Lane 3
22:16	LNRD2_RX_FSM	RX FSM of Data Lane 2
14:8	LNRD1_RX_FSM	RX FSM of Data Lane 1
6:0	LNRD0_RX_FSM	RX FSM of Data Lane 0

150087D0 SENINF2_NCSI2_FRAME_LINE_NUM CSI2 Frame/Line Number 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LINE_NUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	FRAME_NUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	LINE_NUM	Line number
15:0	FRAME_NUM	Frame number

150087D4 SENINF2_NCSI2_GENERIC_SHORT CSI2 Generic Short Packet 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GENERIC_SHORT_PACKET_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											GENERIC_SHORT_PACKET_DT					
Type											RO					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
31:16	GENERIC_SHORT_PACKET_DATA	Generic short packet data
5:0	GENERIC_SHORT_PACKET_DT	Generic short packet data

150087D8 SENINF2_NCSI2_HSRX_DBG CSI2 HSRX Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CLOCK_LANE_HSRX_EN	DATA_LANE3_HSRX_EN	DATA_LANE2_HSRX_EN	DATA_LANE1_HSRX_EN	DATA_LANE0_HSRX_EN
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	CLOCK_LANE_HSRX_EN	Enables clock lane HSRX circuit
3	DATA_LANE3_HSRX_EN	Enables Data Lane 3 HSRX circuit
2	DATA_LANE2_HSRX_EN	Enables Data Lane 2 HSRX circuit
1	DATA_LANE1_HSR	Enables Data Lane 1 HSRX circuit

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Bit(s)	Name	Description
0	X_EN DATA_LANE0_HSRX_EN	Enables Data Lane 0 HSRX circuit

150087DC **SENINF2_NCSI2_DI** **CSI2 Data Interleaving Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DT3						VC3		DT2						VC2	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DT1						VC1		DT0						VC0	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:26	DT3	Data type identifier
25:24	VC3	Virtual channel identifier
23:18	DT2	Data type identifier
17:16	VC2	Virtual channel identifier
15:10	DT1	Data type identifier
9:8	VC1	Virtual channel identifier
7:2	DT0	Data type identifier
1:0	VC0	Virtual channel identifier

150087E0 **SENINF2_NCSI2_HS_TRAIL** **CSI2 HS Trail Timing Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									HS_TRAIL_PARAMETER							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	HS_TRAIL_PARAMETER	HS trail parameter

150087E4 **SENINF2_NCSI2_DI_CTRL** **CSI2 Data Interleaving Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						DT3_INTE		VC3						DT2_INTE		VC2

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						RLEAVING		_IN TER LEA VIN G						RLEAVING		_IN TER LEA VIN G
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DT1_INTE RLEAVING		VC1 _IN TER LEA VIN G						DT0_INTE RLEAVING		VC0 _IN TER LEA VIN G
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0

Bit(s)	Name	Description
26:25	DT3_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
24	VC3_INTERLEAVING	**Virtual channel identifier interleaving**
18:17	DT2_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
16	VC2_INTERLEAVING	**Virtual channel identifier interleaving**
10:9	DT1_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
8	VC1_INTERLEAVING	**Virtual channel identifier interleaving**
2:1	DT0_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
0	VC0_INTERLEAVING	**Virtual channel identifier interleaving**

Module name: SENINF_N3D Base address: (+15008C0h)

Address	Name	Width	Register Function
15008C0	SENINF_N3D_CTL	32	N3D_CTL
15008C4	SENINF_N3D_POS	32	N3D_POS
15008C8	SENINF_N3D_TRIG	32	N3D_TRIG
15008CC	SENINF_N3D_INT	32	N3D_INT
15008D0	SENINF_N3D_CNT0	32	N3D_CNT0
15008D4	SENINF_N3D_CNT1	32	N3D_CNT1
15008D8	SENINF_N3D_DBG	32	N3D_DBG
15008DC	SENINF_N3D_DIFF_THR	32	N3D_DIFF_THR

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Address	Name	Width	Register Function
150080E0	SENINF_N3D_DIFF_CNT	32	N3D_DIFF_CNT

150080C0 **SENINF_N3D_CTL** **N3D_CTL** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				MODE1_DBG	DDBG_SEL			DIFF_EN	W1CLR	N3D_EN	I2C2_INT_EN	I2C1_INT_EN	I2C2_EN	I2C1_EN	MODE	
Type				RW	RW			RW	RW	RW	RW	RW	RW	RW	RW	
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12	MODE1_DBG	0: Normal mode 1: DBG mode
11:9	DDBG_SEL	0: DBG port is cnt2_vs1. 1: Internal state machine
8	DIFF_EN	**Enables different count**
7	W1CLR	**Write 1 to clear the interrupt status.**
6	N3D_EN	**Enables N3D**
5	I2C2_INT_EN	**I2C2 RDY interrupt**
4	I2C1_INT_EN	**I2C1 RDY interrupt**
3	I2C2_EN	**Enables I2C2**
2	I2C1_EN	**Enables I2C1**
1:0	MODE	**N3D mode** 0: Immediate trigger 1: Reference VS1 2: I2C1 before I2C2 3: I2C2 before I2C1

150080C4 **SENINF_N3D_POS** **N3D_POS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N3D_POS[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N3D_POS[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	N3D_POS	In mode 2/3, TG1/TG2 time difference (unit: bclk); in mode 1, related to VS1 position

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150080C8 **SENINF_N3D_TRIG** **N3D_TRIG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															I2CB_TRIG	I2CA_TRIG
Type															WO	WO
Reset															0	0

Bit(s)	Name	Description
1	I2CB_TRIG	**Triggers I2CB** Mode 0: Trigger I2C2 Mode 1, 2, 3: Not used
0	I2CA_TRIG	**Triggers I2CA** Mode 0: Trigger I2C1 Mode 1, 2, 3: Trigger I2C 1/2

150080CC **SENINF_N3D_INT** **N3D_INT** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														DIFF_INT	I2C2_INT	I2C1_INT
Type														RO	RO	RO
Reset														0	0	0

Bit(s)	Name	Description
2	DIFF_INT	DIFF interrupt
1	I2C2_INT	I2C2 ready
0	I2C1_INT	I2C1 ready

150080D0 **SENINF_N3D_CNT0** **N3D_CNT0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N3D_CNT0[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N3D_CNT0[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	N3D_CNT0	TG1 period cnt

150080D4	SENINF_N3D_CNT1	N3D_CNT1	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N3D_CNT1[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N3D_CNT1[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	N3D_CNT1	TG2 period cnt

150080D8	SENINF_N3D_DBG	N3D_DBG	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N3D_DBG[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N3D_DBG[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	N3D_DBG	N3D debugging port

150080DC	SENINF_N3D_DIFF_THR	N3D_DIFF_THR	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N3D_DIFF_THR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N3D_DIFF_THR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	N3D_DIFF_THR	If difference of two vsync > this threshold, diff_int will be issued",N3D_DIFF_THR.

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150080E0	SENINF_N3D_DIFF_CNT	N3D_DIFF_CNT	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N3D_DIFF_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N3D_DIFF_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	N3D_DIFF_CNT	**bit[31]:** 0: vs1 after vs2 1: vs2 after vs1 bit[30:0]: Absolute value for diffcnt

Module name: csi2 Base address: (+15008000h)

Address	Name	Width	Register Function
15008360	SENINF1_CSI2_CTRL	32	CSI2 Control Register
15008364	SENINF1_CSI2_DELAY	32	CSI2 Delay Control Register
15008368	SENINF1_CSI2_INTEN	32	CSI2 Interrupt Enable Register
1500836C	SENINF1_CSI2_INTSTA	32	CSI2 Interrupt Status Register
15008370	SENINF1_CSI2_ECCDBG	32	CSI2 ECC Debug Register
15008374	SENINF1_CSI2_CRCDBG	32	CSI2 CRC Debug Register
15008378	SENINF1_CSI2_DBG	32	CSI2 Debug Register
1500837C	SENINF1_CSI2_VER	32	CSI2 Version Code Register
15008380	SENINF1_CSI2_SHORT_INFO	32	CSI2 Short packet information Register
15008384	SENINF1_CSI2_LNFSM	32	CSI2 Lane FSM Register
15008388	SENINF1_CSI2_LNMUX	32	CSI2 Lane Mux Register
1500838C	SENINF1_CSI2_HSYNC_CNT	32	CSI2 Hsync Counter Register
15008390	SENINF1_CSI2_CAL	32	CSI2 Calibration Register
15008394	SENINF1_CSI2_DS	32	CSI2 Downsample Register
15008398	SENINF1_CSI2_VS	32	CSI2 Vsync Register
1500839C	SENINF1_CSI2_BIST	32	CSI2 BIST Register
15008760	SENINF2_CSI2_CTRL	32	CSI2 Control Register
15008764	SENINF2_CSI2_DELAY	32	CSI2 Delay Control Register
15008768	SENINF2_CSI2_INTEN	32	CSI2 Interrupt Enable Register
1500876C	SENINF2_CSI2_INTSTA	32	CSI2 Interrupt Status Register
15008770	SENINF2_CSI2_ECCDBG	32	CSI2 ECC Debug Register
15008774	SENINF2_CSI2_CRCDB	32	CSI2 CRC Debug Register

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Address	Name	Width	Register Function
	G		
15008778	**SENINF2_CSI2_DBG**	32	CSI2 Debug Register
1500877C	**SENINF2_CSI2_VER**	32	CSI2 Version Code Register
15008780	**SENINF2_CSI2_SHORT_INFO**	32	CSI2 Short packet information Register
15008784	**SENINF2_CSI2_LNFSM**	32	CSI2 Lane FSM Register
15008788	**SENINF2_CSI2_LNMUX**	32	CSI2 Lane Mux Register
1500878C	**SENINF2_CSI2_HSYNC_CNT**	32	CSI2 Hsync Counter Register
15008790	**SENINF2_CSI2_CAL**	32	CSI2 Calibration Register
15008794	**SENINF2_CSI2_DS**	32	CSI2 Downsample Register
15008798	**SENINF2_CSI2_VS**	32	CSI2 Vsync Register
1500879C	**SENINF2_CSI2_BIST**	32	CSI2 BIST Register

15008360 **SENINF1_CSI2_CTRL** **CSI2 Control Register** **00002D80**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CSI2_BIST_CSI2_DATA_OK**	**CSI2_LANE_FSM_OK**	**CSI2_HS_FSM_OK**	**CSI2_BIST_DATA_OK**	**CSI2_BIST_START**	**CSI2_BIST_ERROR_COUNT**								**CSI2_DATA_FLOW**		**CSI2_ASYNC_OPTION**
Type	RO	RO	RO	RO	RO	RO								RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CSI2_SYNC_CLR_EXTEND**	**CSI2_HSRXEN_PFOOT_CLR**	**CSI2_VSYNC_TYPE**	**CSI2_SW_RST**	**CSI2_SCLK4X_SEL**	**CSI2_SCLK_SEL**	**CSI2_ESC_EN**	**CSI2_SYNC_RST_EN**	**CSI2_LP11_RST_EN**	**CSI2_CLK_MISS_EN**	**CSI2_ED_SEL**	**CSI2_ECC_EN**	**DLANE3_EN**	**DLANE2_EN**	**DLANE1_EN**	**CSI2_EN**
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	1	0	1	1	0	1	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	CSI2_BIST_CSI2_DATA_OK	**CSI2 BIST CSI2 data ok**
30	CSI2_LANE_FSM_OK	**CSI2 BIST data lane FSM ok**
29	CSI2_HS_FSM_OK	**CSI2 BIST high speed FSM ok**
28	CSI2_BIST_DATA_OK	**CSI2 BIST DPHY data ok**
27	CSI2_BIST_START	**CSI2 BIST start status**
26:19	CSI2_BIST_ERROR_COUNT	**CSI2 BIST test error count**
18:17	CSI2_DATA_FLOW	**CSI2 data flow** 0: Data packet 1: Generic long packet 2: All data packet

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Bit(s)	Name	Description
16	CSI2_ASYNC_OPTION	
15	CSI2_SYNC_CLR_EXTEND	
14	CSI2_HSRXEN_PFOOT_CLR	
13	CSI2_VSYNC_TYPE	**VSYNC type to CAM module** 0: High from short packet "frame start" to short packet "frame end" 1: 4T pulse after short packet "frame start"
12	CSI2_SW_RST	**CSI2 software reset** Active high 0: De-assert reset 1: Assert reset
11	CSI2_SCLK4X_SEL	**Selects CSI2 4x sample clock** 0: Invert 1: Does not invert csi2_clk from D-PHY
10	CSI2_SCLK_SEL	**Selects CSI2 sample clock** 0: Invert 1: Does not invert csi2_clk from D-PHY
9	CSI2_ESC_EN	**Enables CSI2 escape mode**
8	CSI2_SYNC_RST_EN	**When this bit is set to high, the data high speed FSM will enter state "SYNC" whenever sync code is seen.** Used in case packet ends unexpectedly.
7	CSI2_LP11_RST_EN	**When this bit is set to high, the data/clk lane FSM will enter state "STOP" whenever LP-11 is seen.** Used in case low power and high speed state transition occur unexpectedly.
6	CSI2_CLK_MISS_EN	**Enables high speed mode clock miss monitoring**
5	CSI2_ED_SEL	**Selects CSI2 header format**
4	CSI2_ECC_EN	**Enables CSI2 ECC**
3	DLANE3_EN	**Enables CSI2 3 data lane**
2	DLANE2_EN	**Enables CSI2 2 data lane**
1	DLANE1_EN	**Enables CSI2 1 data lane**
0	CSI2_EN	**Enables CSI2 0 data lane**

15008364 **SENINF1_CSI2_DELAY** **CSI2 Delay Control Register** **000A0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LP2HS_DATA_TERM_DELAY								LP2HS_DATA_SETTLE_DELAY							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									LP2HS_CLK_TERM_DELAY							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	LP2HS_DATA_TERM_DELAY	CSI2 data lane low power to high speed termination enable delay count.
23:16	LP2HS_DATA_SET	CSI2 data lane low power to high speed sync code search delay.

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Bit(s)	Name	Description
7:0	TLE_DELAY LP2HS_CLK_TERM_DELAY	CSI2 CLK lane low power to high speed termination enable delay count

15008368 SENINF1_CSI2_INTEN CSI2 Interrupt Enable Register 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VCHANNEL_ID		CSI2_DATA_TYPE						CSI2_WC_NUMBER[15:8]							
Type	RO		RO						RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CSI2_WC_NUMBER[7:0]												CSI2SYNC_NONSYNC_IRQ_EN	ECC_CORRECT_IRQ_EN	ECC_ERR_IRQ_EN	CRC_ERR_IRQ_EN
Type	RO												RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0					0	1	1	1

Bit(s)	Name	Description
31:30	VCHANNEL_ID	CSI2 virtual channel identifier corrected by error correction if ECC is on
29:24	CSI2_DATA_TYPE	CSI2 long packet data type corrected by error correction if ECC is on
23:8	CSI2_WC_NUMBER	CSI2 long packet data size corrected by error correction if ECC is on
3	CSI2SYNC_NONSYNC_IRQ_EN	CSI2SYNC_NONSYNC_IRQ
2	ECC_CORRECT_IRQ_EN	Enables ECC correction interrupt
1	ECC_ERR_IRQ_EN	Enables ECC error interrupt
0	CRC_ERR_IRQ_EN	Enables CRC error interrupt

1500836C SENINF1_CSI2_INTSTA CSI2 Interrupt Status Register 00000070

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CSI2OUT_VSYNC	CSI2OUT_HSYNC				
Type											RO	RO				
Reset											0	0				
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name									CSI2_SPARE			CSI2_IRQ_CLR_SEL	CSI2SYNC_NONSYNC_IRQ	ECC_CORRECT_IRQ	ECC_ERR_IRQ	CRC_ERR_IRQ
Type									RW			RW	RO	RO	RO	RO

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Reset									0	1	1	1	0	0	0	0

Bit(s)	Name	Description
21	CSI2OUT_VSYNC	**CSI2 vsync output to cam** Read only.
20	CSI2OUT_HSYNC	**CSI2 hsync output to cam** Read only.
7:5	CSI2_SPARE	**Spare registers**
4	CSI2_IRQ_CLR_SEL	0: Read clear 1: Write clear
3	CSI2SYNC_NONSYNC_IRQ	**IRQ status bit to indicate that sync between different lanes are not sampled at the same time** Write clear.
2	ECC_CORRECT_IRQ	**ECC correction interrupt status**
1	ECC_ERR_IRQ	**ECC error interrupt status**
0	CRC_ERR_IRQ	**CRC error interrupt status**

15008370 SENINF1_CSI2_ECCDBG CSI2 ECC Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2_ECCDB_BSEL[23:8]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_ECCDB_BSEL[7:0]															CSI2_ECCDB_EN
Type	RW															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CSI2_ECCDB_BSEL	**Selects CSI2 packet header error generation bit** To generate packet header error, set one of the 24 bits to 1. Only one bit error can be corrected; therefore only one bit out of the 24 bits can be 1.
0	CSI2_ECCDB_EN	**Enables CSI2 packet header error generation**

15008374 SENINF1_CSI2_CRCDBG CSI2 CRC Debug Register 0000000E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2_CRCDB_BSEL								CSI2_CRCDB_WSEL[15:8]							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_CRCDB_WSEL[7:0]								CSI2_SPARE							CSI2_CRCDB_EN
Type	RW								RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

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Bit(s)	Name	Description
31:24	CSI2_CRCDB_BSEL	**Selects CSI2 data error generation bit** To generate selected word bit error, set the bit to 1. Note: Only word number selected by csi2_crcdb_wsel will be put error on it.
23:8	CSI2_CRCDB_WSEL	**Selects CSI2 data error generation data word**
7:1	CSI2_SPARE	
0	CSI2_CRCDB_EN	**Enables CSI2 data error generation**

15008378 **SENINF1_CSI2_DBG** **CSI2 Debug Register** **00040820**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LN3_HSRXDB_EN	LN2_HSRXDB_EN	LN1_HSRXDB_EN	LN0_HSRXDB_EN	LNC_HSRXDB_EN	LN3_LPRXDB_EN	LN2_LPRXDB_EN	LN1_LPRXDB_EN	LN0_LPRXDB_EN	LNC_LPRXDB_EN		VCHANNEL_ID_EN	VCHANNEL1_ID		VCHANNEL0_ID	
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0		0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_CLK_LANE_CS					CSI2_DATA_HS_CS						CSI2_DBG_SRC_SEL				CSI2_DEBUG_ON
Type	RO					RO						RW				RW
Reset	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31	LN3_HSRXDB_EN	**Enables Data Lane 1 termination directly** For test only.
30	LN2_HSRXDB_EN	**Enables Data Lane 0 termination directly** For test only.
29	LN1_HSRXDB_EN	**Enables Data Lane 1 termination directly** For test only.
28	LN0_HSRXDB_EN	**Enable Data Lane 0 termination directly** For test only.
27	LNC_HSRXDB_EN	**Enable clock lane termination directly** For test only.
26	LN3_LPRXDB_EN	**Enable Data Lane 3 low power mode directly** For test only.
25	LN2_LPRXDB_EN	**Enable Data Lane 2 low power mode directly** For test only.
24	LN1_LPRXDB_EN	**Enable Data Lane 1 low power mode directly** For test only.
23	LN0_LPRXDB_EN	**Enable Data Lane 0 low power mode directly** For test only.
22	LNC_LPRXDB_EN	**Enable clock lane low power mode directly** For test only.
20	VCHANNEL_ID_EN	**Enables virtual channel**

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Bit(s)	Name	Description
19:18	VCHANNEL1_ID	**Virtual Channel 1 ID**
17:16	VCHANNEL0_ID	**Virtual Channel 0 ID**
15:11	CSI2_CLK_LANE_CS	**Clock lane FSM current state** 1: IDLE 2: STOP 4: HS_REQ 8: HS_PREP 16: HS_RX
10:5	CSI2_DATA_HS_CS	**Data high speed state** 1: IDLE 2: SYNC 4: PHEAD 8: PECC 16: PDATA 32: PFOOT
4:1	CSI2_DBG_SRC_SEL	**Selects CSI2 debugging port source**
0	CSI2_DEBUG_ON	**Enables CSI2 debugging** When CSI2 debugging is enabled, CSI2 output raw data will include the header to cam. *Note: To output CSI2 debugging data,* *1. Set the cam to JPEG interface mode ((CAM + 0024)[14], JPGINF_EN : 1).* *2. Set up vsync polarity ((CAM + 0010)[7], VSPOL : 1).* *3. Set up output type raw data output ((CAM + 0024)[21:20] OUTPATH_TYPE : 0).* *4. Set the raw data type to 8-bit mode ((CAM + 0024)[24] OUTPATH_TYPE : 0).* *5. Enable ISP data output to memory. ((CAM + 0024)[16],OUT_PATH_EN:1)*

1500837C **SENINF1_CSI2_VER** **CSI2 Version Code Register** **20110815**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	YEAR															
Type	RO															
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MONTH								DATE							
Type	RO								RO							
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	1

Bit(s)	Name	Description
31:16	YEAR	Year code
15:8	MONTH	Month code
7:0	DATE	Date code

15008380 **SENINF1_CSI2_SHORT_INFO** **CSI2 Short packet information Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2_FRAME_NO															

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Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CSI2_LINE_NO**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	CSI2_FRAME_NO	Frame number information in short packet data type
15:0	CSI2_LINE_NO	Line number information in short packet data type

15008384 SENINF1_CSI2_LNFSM CSI2 Lane FSM Register 01010101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**CSI2_DATA_LN3_CS**								**CSI2_DATA_LN2_CS**						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**CSI2_DATA_LN1_CS**								**CSI2_DATA_LN0_CS**						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1

Bit(s)	Name	Description
30:24	CSI2_DATA_LN3_CS	**Data Lane 3 FSM current state**
22:16	CSI2_DATA_LN2_CS	**Data Lane 2 FSM current state**
14:8	CSI2_DATA_LN1_CS	**Data Lane 1 FSM current state**
6:0	CSI2_DATA_LN0_CS	**Data Lane 0 FSM current state** 1: IDLE 2: STOP 4: HS_REQ STATE 8: HS_PREP 16: HS_TERM 32: HS_RX 64: HS_ESC

15008388 SENINF1_CSI2_LNMUX CSI2 Lane Mux Register 000000E4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**CSI2_DATA_LN3_MUX**		**CSI2_DATA_LN2_MUX**		**CSI2_DATA_LN1_MUX**		**CSI2_DATA_LN0_MUX**	
Type									RW		RW		RW		RW	
Reset									1	1	1	0	0	1	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
7:6	CSI2_DATA_LN3_MUX	**CSI2 data lane mux** 0: LANE0 1: LANE1 2: LANE2 3: LANE3
5:4	CSI2_DATA_LN2_MUX	**CSI2 data lane mux** 0: LANE0 1: LANE1 2: LANE2 3: LANE3
3:2	CSI2_DATA_LN1_MUX	**CSI2 data lane mux** 0: LANE0 1: LANE1 2: LANE2 3: LANE3
1:0	CSI2_DATA_LN0_MUX	**CSI2 data lane mux** 0: LANE0 1: LANE1 2: LANE2 3: LANE3

1500838C **SENINF1_CSI2_HSYNC_CNT** **CSI2 Hsync Counter Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CSI2_HSYNC_CNT												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	CSI2_HSYNC_CNT	CSI2 hsync counter

15008390 **SENINF1_CSI2_CAL** **CSI2 Calibration Register** **01010000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2_CAL_CNT_2								CSI2_CAL_CNT_1							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										CSI2_CAL_STATE						CSI2_CAL_EN
Type										RO						RW
Reset										0	0	0				0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:24	CSI2_CAL_CNT_2	**CSI2 Calibration Counter 2 (term enable to sync)** Settle delay <= CSI2 Calibration Counter 2 - Term Delay - 3 byte clk - 3 bclk - 1 bclk
23:16	CSI2_CAL_CNT_1	**CSI2 Calibration Counter 1 (term enable to HS00)** Term delay <= CSI2 Calibration Counter 1 - 2 byte clk - 3 bclk
6:4	CSI2_CAL_STATE	**CSI2 calibration current state**
0	CSI2_CAL_EN	**Enables CSI2 calibration**

15008394 SENINF1_CSI2_DS CSI2 Downsample Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CSI2_DS_CTRL		CSI2_DS_EN
Type														RW		RW
Reset														0	0	0

Bit(s)	Name	Description
2:1	CSI2_DS_CTRL	**Controls CSI2 downsample factor** 0: 1 1: 1/2 2: 1/4 3: 1/8
0	CSI2_DS_EN	**Enables CSI2 downsample**

15008398 SENINF1_CSI2_VS CSI2 Vsync Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CSI2_VS_CTRL	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	CSI2_VS_CTRL	**Extends CSI2 vsync period** 0: 4T 1: 8T 2: 12T 3: 16T

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1500839C	SENINF1_CSI2_BIST	CSI2 BIST Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CSI2_BIST_LNR3_DATA_OK	CSI2_BIST_LNR2_DATA_OK	CSI2_BIST_LNR1_DATA_OK	CSI2_BIST_LNR0_DATA_OK
Type													RO	RO	RO	RO
Reset													0	0	0	0

Bit(s)	Name	Description
3	CSI2_BIST_LNR3_DATA_OK	CSI2 BIST Lane 3 DPHY data ok
2	CSI2_BIST_LNR2_DATA_OK	CSI2 BIST Lane 2 DPHY data ok
1	CSI2_BIST_LNR1_DATA_OK	CSI2 BIST Lane 1 DPHY data ok
0	CSI2_BIST_LNR0_DATA_OK	CSI2 BIST Lane 0 DPHY data ok

15008760	SENINF2_CSI2_CTRL	CSI2 Control Register	00002D80

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2_BIST_CSI2_DATA_OK	CSI2_LANE_FSM_OK	CSI2_HS_FSM_OK	CSI2_BIST_DATA_OK	CSI2_BIST_START	CSI2_BIST_ERROR_COUNT								CSI2_DATA_FLOW		CSI2_ASYNC_OPTION
Type	RO	RO	RO	RO	RO	RO								RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_SYNC_CLR_EXTEND	CSI2_HSRXEN_PFOOT_CLR	CSI2_VSYNC_TYPE	CSI2_SW_RST	CSI2_SCLK4X_SEL	CSI2_SCLK_SEL	CSI2_ESC_EN	CSI2_SYNC_RST_EN	CSI2_LP11_RST_EN	CSI2_CLK_MISS_EN	CSI2_ED_SEL	CSI2_EC_EN	DLANE3_EN	DLANE2_EN	DLANE1_EN	CSI2_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	1	0	1	1	0	1	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	CSI2_BIST_CSI2_DATA_OK	**CSI2 BIST CSI2 data ok**
30	CSI2_LANE_FSM_OK	**CSI2 BIST data lane FSM ok**
29	CSI2_HS_FSM_OK	**CSI2 BIST high speed FSM ok**

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Bit(s)	Name	Description
28	CSI2_BIST_DATA_OK	**CSI2 BIST DPHY data ok**
27	CSI2_BIST_START	**CSI2 BIST start status**
26:19	CSI2_BIST_ERROR_COUNT	**CSI2 BIST test error count**
18:17	CSI2_DATA_FLOW	**CSI2 data flow** 0: Data packet 1: Generic long packet 2: All data packet
16	CSI2_ASYNC_OPTION	
15	CSI2_SYNC_CLR_EXTEND	
14	CSI2_HSRXEN_PFOOT_CLR	
13	CSI2_VSYNC_TYPE	**VSYNC type to CAM module** 0: High from short packet "frame start" to short packet "frame end" 1: 4T pulse after short packet "frame start"
12	CSI2_SW_RST	**CSI2 software reset** Active high 0: De-assert reset 1: Assert reset
11	CSI2_SCLK4X_SEL	**Selects CSI2 4x sample clock** 0: Invert 1: Does not invert csi2_clk from D-PHY
10	CSI2_SCLK_SEL	**Selects CSI2 sample clock** 0: Invert 1: Does not invert csi2_clk from D-PHY
9	CSI2_ESC_EN	**Enables CSI2 escape mode**
8	CSI2_SYNC_RST_EN	**When this bit is set to high, the data high speed FSM will enter state "SYNC" whenever sync code is seen.** Used in case packet ends unexpectedly.
7	CSI2_LP11_RST_EN	**When this bit is set to high, the data/clk lane FSM will enter state "STOP" whenever LP-11 is seen.** Used in case low power and high speed state transition occur unexpectedly.
6	CSI2_CLK_MISS_EN	**Enables high speed mode clock miss monitoring**
5	CSI2_ED_SEL	**Selects CSI2 header format**
4	CSI2_ECC_EN	**Enables CSI2 ECC**
3	DLANE3_EN	**Enables CSI2 3 data lane**
2	DLANE2_EN	**Enables CSI2 2 data lane**
1	DLANE1_EN	**Enables CSI2 1 data lane**
0	CSI2_EN	**Enables CSI2 0 data lane**

15008764 **SENINF2_CSI2_DELAY** **CSI2 Delay Control Register** **000A0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LP2HS_DATA_TERM_DELAY								LP2HS_DATA_SETTLE_DELAY							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									LP2HS_CLK_TERM_DELAY							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	LP2HS_DATA_TERM_DELAY	CSI2 data lane low power to high speed termination enable delay count.
23:16	LP2HS_DATA_SETTLE_DELAY	CSI2 data lane low power to high speed sync code search delay.
7:0	LP2HS_CLK_TERM_DELAY	CSI2 CLK lane low power to high speed termination enable delay count

15008768 SENINF2_CSI2_INTEN CSI2 Interrupt Enable Register 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VCHANNEL_ID		CSI2_DATA_TYPE						CSI2_WC_NUMBER[15:8]							
Type	RO		RO						RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_WC_NUMBER[7:0]												CSI2SYNC_NONSYNC_IRQ_EN	ECC_CORRECT_IRQ_EN	ECC_ERR_IRQ_EN	CRC_ERR_IRQ_EN
Type	RO												RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0					0	1	1	1

Bit(s)	Name	Description
31:30	VCHANNEL_ID	CSI2 virtual channel identifier corrected by error correction if ECC is on
29:24	CSI2_DATA_TYPE	CSI2 long packet data type corrected by error correction if ECC is on
23:8	CSI2_WC_NUMBER	CSI2 long packet data size corrected by error correction if ECC is on
3	CSI2SYNC_NONSYNC_IRQ_EN	CSI2SYNC_NONSYNC_IRQ
2	ECC_CORRECT_IRQ_EN	Enables ECC correction interrupt
1	ECC_ERR_IRQ_EN	Enables ECC error interrupt
0	CRC_ERR_IRQ_EN	Enables CRC error interrupt

1500876C SENINF2_CSI2_INTSTA CSI2 Interrupt Status Register 00000070

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CSI2OUT_VSYNC	CSI2OUT_HSYNC				
Type											RO	RO				
Reset											0	0				

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CSI2_SPARE			CSI2_IRQ_CLR_SEL	CSI2SYNC_NONSYNC_IRQ	ECC_CORRECT_IRQ	ECC_ERR_IRQ	CRC_ERR_IRQ
Type									RW			RW	RO	RO	RO	RO
Reset									0	1	1	1	0	0	0	0

Bit(s)	Name	Description
21	CSI2OUT_VSYNC	**CSI2 vsync output to cam** Read only.
20	CSI2OUT_HSYNC	**CSI2 hsync output to cam** Read only
7:5	CSI2_SPARE	**Spare registers**
4	CSI2_IRQ_CLR_SEL	0: Read clear 1: Write clear
3	CSI2SYNC_NONSYNC_IRQ	**IRQ status bit to indicate that sync between different lanes are not sampled at the same time** Write clear.
2	ECC_CORRECT_IRQ	**ECC correction interrupt status**
1	ECC_ERR_IRQ	**ECC error interrupt status**
0	CRC_ERR_IRQ	**CRC error interrupt status**

15008770 SENINF2_CSI2_ECCDBG CSI2 ECC Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2_ECCDB_BSEL[23:8]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_ECCDB_BSEL[7:0]															CSI2_ECCDB_EN
Type	RW															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CSI2_ECCDB_BSEL	**Selects CSI2 packet header error generation bit** To generate packet header error, set one of the 24 bits to 1. Only one bit error can be corrected; therefore only one bit out of the 24 bits can be 1.
0	CSI2_ECCDB_EN	**Enables CSI2 packet header error generation**

15008774 SENINF2_CSI2_CRCDBG CSI2 CRC Debug Register 0000000E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2_CRCDB_BSEL								CSI2_CRCDB_WSEL[15:8]							

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Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_CRCDB_WSEL[7:0]								CSI2_SPARE							CSI2_CRCDB_EN
Type	RW								RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

Bit(s)	Name	Description
31:24	CSI2_CRCDB_BSEL	**Selects CSI2 data error generation bit** To generate selected word bit error, set the bit to 1. Note: Only word number selected by csi2_crcdb_wsel will be put error on it.
23:8	CSI2_CRCDB_WSEL	**Selects CSI2 data error generation data word**
7:1	CSI2_SPARE	**Spare registers.**
0	CSI2_CRCDB_EN	**Enables CSI2 data error generation**

15008778 **SENINF2_CSI2_DBG** **CSI2 Debug Register** **00040820**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LN3_HSRXDB_EN	LN2_HSRXDB_EN	LN1_HSRXDB_EN	LN0_HSRXDB_EN	LNC_HSRXDB_EN	LN3_LPRXDB_EN	LN2_LPRXDB_EN	LN1_LPRXDB_EN	LN0_LPRXDB_EN	LNC_LPRXDB_EN		VCHANNEL_ID_EN	VCHANNEL1_ID		VCHANNEL0_ID	
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0		0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_CLK_LANE_CS					CSI2_DATA_HS_CS						CSI2_DBG_SRC_SEL				CSI2_DEBUG_ON
Type	RO					RO						RW				RW
Reset	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31	LN3_HSRXDB_EN	**Enables Data Lane 1 termination directly** For test only.
30	LN2_HSRXDB_EN	**Enables Data Lane 0 termination directly** For test only.
29	LN1_HSRXDB_EN	**Enables Data Lane 1 termination directly** For test only.
28	LN0_HSRXDB_EN	**Enable Data Lane 0 termination directly** For test only.
27	LNC_HSRXDB_EN	**Enable clock lane termination directly** For test only.
26	LN3_LPRXDB_EN	**Enable Data Lane 3 low power mode directly** For test only.
25	LN2_LPRXDB_EN	**Enable Data Lane 2 low power mode directly** For test only.
24	LN1_LPRXDB_EN	**Enable Data Lane 1 low power mode directly**

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Bit(s)	Name	Description
		For test only.
23	LN0_LPRXDB_EN	**Enable Data Lane 0 low power mode directly** For test only.
22	LNC_LPRXDB_EN	**Enable clock lane low power mode directly** For test only.
20	VCHANNEL_ID_EN	**Enables virtual channel**
19:18	VCHANNEL1_ID	**Virtual Channel 1 ID**
17:16	VCHANNEL0_ID	**Virtual Channel 0 ID**
15:11	CSI2_CLK_LANE_CS	**Clock lane FSM current state** 1: IDLE 2: STOP 4: HS_REQ 8: HS_PREP 16: HS_RX
10:5	CSI2_DATA_HS_CS	**Data high speed state** 1: IDLE 2: SYNC 4: PHEAD 8: PECC 16: PDATA 32: PFOOT
4:1	CSI2_DBG_SRC_SEL	**Selects CSI2 debugging port source**
0	CSI2_DEBUG_ON	**Enables CSI2 debugging** When CSI2 debugging is enabled, CSI2 output raw data will include the header to cam. *Note: To output CSI2 debugging data,* *1. Set the cam to JPEG interface mode ((CAM + 0024)[14], JPGINF_EN : 1).* *2. Set up vsync polarity ((CAM + 0010)[7], VSPOL : 1).* *3. Set up output type raw data output ((CAM + 0024)[21:20] OUTPATH_TYPE : 0).* *4. Set the raw data type to 8-bit mode ((CAM + 0024)[24] OUTPATH_TYPE : 0).* *5. Enable ISP data output to memory. ((CAM + 0024)[16],OUT_PATH_EN:1)*

1500877C **SENINF2_CSI2_VER** **CSI2 Version Code Register** **20110815**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	YEAR															
Type	RO															
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MONTH								DATE							
Type	RO								RO							
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	1

Bit(s)	Name	Description
31:16	YEAR	Year code
15:8	MONTH	Month code
7:0	DATE	Date code

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15008780 SENINF2_CSI2_SHORT_INFO CSI2 Short packet information Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2_FRAME_NO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_LINE_NO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	CSI2_FRAME_NO	Frame number information in short packet data type
15:0	CSI2_LINE_NO	Line number information in short packet data type

15008784 SENINF2_CSI2_LNFSM CSI2 Lane FSM Register 01010101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CSI2_DATA_LN3_CS								CSI2_DATA_LN2_CS						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CSI2_DATA_LN1_CS								CSI2_DATA_LN0_CS						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1

Bit(s)	Name	Description
30:24	CSI2_DATA_LN3_CS	**Data Lane 3 FSM current state**
22:16	CSI2_DATA_LN2_CS	**Data Lane 2 FSM current state**
14:8	CSI2_DATA_LN1_CS	**Data Lane 1 FSM current state**
6:0	CSI2_DATA_LN0_CS	**Data Lane 0 FSM current state** 1: IDLE 2: STOP 4: HS_REQ STATE 8: HS_PREP 16: HS_TERM 32: HS_RX 64: HS_ESC

15008788 SENINF2_CSI2_LNMUX CSI2 Lane Mux Register 000000E4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

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Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CSI2_DATA_LN3_MUX		CSI2_DATA_LN2_MUX		CSI2_DATA_LN1_MUX		CSI2_DATA_LN0_MUX	
Type									RW		RW		RW		RW	
Reset									1	1	1	0	0	1	0	0

Bit(s)	Name	Description
7:6	CSI2_DATA_LN3_MUX	**CSI2 data lane mux** 0: LANE0 1: LANE1 2: LANE2 3: LANE3
5:4	CSI2_DATA_LN2_MUX	**CSI2 data lane mux** 0: LANE0 1: LANE1 2: LANE2 3: LANE3
3:2	CSI2_DATA_LN1_MUX	**CSI2 data lane mux** 0: LANE0 1: LANE1 2: LANE2 3: LANE3
1:0	CSI2_DATA_LN0_MUX	**CSI2 data lane mux** 0: LANE0 1: LANE1 2: LANE2 3: LANE3

1500878C **SENINF2_CSI2_HSYNC_CNT** **CSI2 Hsync Counter Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CSI2_HSYNC_CNT												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	CSI2_HSYNC_CNT	CSI2 hsync counter

15008790 **SENINF2_CSI2_CAL** **CSI2 Calibration Register** **01010000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2_CAL_CNT_2								CSI2_CAL_CNT_1							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name										CSI2_CAL_STATE					CSI2_CAL_EN
Type										RO					RW
Reset										0	0	0			0

Bit(s)	Name	Description
31:24	CSI2_CAL_CNT_2	**CSI2 Calibration Counter 2 (term enable to sync)** Settle delay <= CSI2 Calibration Counter 2 - Term Delay - 3 byte clk - 3 bclk - 1 bclk
23:16	CSI2_CAL_CNT_1	**CSI2 Calibration Counter 1 (term enable to HS00)** Term delay <= CSI2 Calibration Counter 1 - 2 byte clk - 3 bclk
6:4	CSI2_CAL_STATE	**CSI2 calibration current state**
0	CSI2_CAL_EN	**Enables CSI2 calibration**

15008794 SENINF2_CSI2_DS CSI2 Downsample Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CSI2_DS_CTRL		CSI2_DS_EN
Type														RW		RW
Reset														0	0	0

Bit(s)	Name	Description
2:1	CSI2_DS_CTRL	**Controls CSI2 downsample factor** 0: 1 1: 1/2 2: 1/4 3: 1/8
0	CSI2_DS_EN	**Enables CSI2 downsample**

15008798 SENINF2_CSI2_VS CSI2 Vsync Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CSI2_VS_CTRL	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	CSI2_VS_CTRL	**Extends CSI2 vsync period**

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Bit(s)	Name	Description
		0: 4T 1: 8T 2: 12T 3: 16T

1500879C **SENINF2_CSI2_BIST** **CSI2 BIST Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CSI2_BIST_LNR3_DATA_OK	CSI2_BIST_LNR2_DATA_OK	CSI2_BIST_LNR1_DATA_OK	CSI2_BIST_LNR0_DATA_OK
Type													RO	RO	RO	RO
Reset													0	0	0	0

Bit(s)	Name	Description
3	CSI2_BIST_LNR3_DATA_OK	CSI2 BIST Lane 3 DPHY data ok
2	CSI2_BIST_LNR2_DATA_OK	CSI2 BIST Lane 2 DPHY data ok
1	CSI2_BIST_LNR1_DATA_OK	CSI2 BIST Lane 1 DPHY data ok
0	CSI2_BIST_LNR0_DATA_OK	CSI2 BIST Lane 0 DPHY data ok

Module name: mipi_rx_config Base address: (+15008000h)

Address	Name	Width	Register Function
15008300	MIPI_RX_CON00_CSI0	32	MIPI RX Config Register
15008304	MIPI_RX_CON04_CSI0	32	MIPI RX Config Register
15008308	MIPI_RX_CON08_CSI0	32	MIPI RX Config Register
1500830C	MIPI_RX_CON0C_CSI0	32	MIPI RX Config Register
15008310	MIPI_RX_CON10_CSI0	32	MIPI RX Config Register
15008324	MIPI_RX_CON24_CSI0	32	MIPI RX Config Register
15008328	MIPI_RX_CON28_CSI0	32	MIPI RX Config Register
15008334	MIPI_RX_CON34_CSI0	32	MIPI RX Config Register
15008338	MIPI_RX_CON38_CSI0	32	MIPI RX Config Register
1500833C	MIPI_RX_CON3C_CSI0	32	MIPI RX Config Register
15008340	MIPI_RX_CON40_CSI0	32	MIPI RX Config Register
15008344	MIPI_RX_CON44_CSI0	32	MIPI RX Config Register
15008348	MIPI_RX_CON48_CSI0	32	MIPI RX Config Register
15008350	MIPI_RX_CON50_CSI0	32	MIPI RX Config Register
15008700	MIPI_RX_CON00_CSI1	32	MIPI RX Config Register

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Address	Name	Width	Register Function
15008704	MIPI_RX_CON04_CSI1	32	MIPI RX Config Register
15008708	MIPI_RX_CON08_CSI1	32	MIPI RX Config Register
1500870C	MIPI_RX_CON0C_CSI1	32	MIPI RX Config Register
15008710	MIPI_RX_CON10_CSI1	32	MIPI RX Config Register
15008724	MIPI_RX_CON24_CSI1	32	MIPI RX Config Register
15008728	MIPI_RX_CON28_CSI1	32	MIPI RX Config Register
15008734	MIPI_RX_CON34_CSI1	32	MIPI RX Config Register
15008738	MIPI_RX_CON38_CSI1	32	MIPI RX Config Register
1500873C	MIPI_RX_CON3C_CSI1	32	MIPI RX Config Register
15008740	MIPI_RX_CON40_CSI1	32	MIPI RX Config Register
15008744	MIPI_RX_CON44_CSI1	32	MIPI RX Config Register
15008748	MIPI_RX_CON48_CSI1	32	MIPI RX Config Register
15008750	MIPI_RX_CON50_CSI1	32	MIPI RX Config Register

15008300 MIPI_RX_CON00_CSI0 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name									AD_CSI0_LNRC_HSRX_OFFSET_OUT	RG_CSI0_LNRC_HSRX_OFFSET_CODE					RG_CSI0_LNRC_HSRX_CAL_EN	RG_CSI0_LNRC_HSRX_CAL_APPLY
Type									RO	RW					RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	AD_CSI0_LNRC_HSRX_OFFSET_OUT	**CK Lane 0 HSRX offset compared output**
6:2	RG_CSI0_LNRC_HSRX_OFFSET_CODE	**CK Lane 0 HSRX offset calibration code** 5'b0xxxx: Increase positive output voltage 5'b1xxxx: Increase negative output voltage 5'bx0000: Minimum output voltage 5'bx1111: Maximum output voltage
1	RG_CSI0_LNRC_HSRX_CAL_EN	**Enables CK Lane 0 HSRX offset calibration** 1'b0: Disable 1'b1: Enable
0	RG_CSI0_LNRC_HSRX_CAL_APPLY	**Applies CK Lane 0 HSRX offset calibration** 1'b0: Does not use calibration result 1'b1: Use calibration result

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15008304	MIPI_RX_CON04_CSI0	MIPI RX Config Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AD_CSI0_LNRD0_HSRX_OFFSET_OUT	RG_CSI0_LNRD0_HSRX_OFFSET_CODE					RG_CSI0_LNRD0_HSRX_CAL_EN	RG_CSI0_LNRD0_HSRX_CAL_APPLY
Type									RO	RW					RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	AD_CSI0_LNRD0_HSRX_OFFSET_OUT	**Lane 0 HSRX offset compared output**
6:2	RG_CSI0_LNRD0_HSRX_OFFSET_CODE	**Lane0 HSRX offset calibration code** 5'b0xxxx: Increase positive output voltage 5'b1xxxx: Increase negative output voltage 5'bx0000: Minimum output voltage 5'bx1111: Maximum output voltage
1	RG_CSI0_LNRD0_HSRX_CAL_EN	**Enables Lane 0 HSRX offset calibration** 1'b0: Disable 1'b1: Enable
0	RG_CSI0_LNRD0_HSRX_CAL_APPLY	**Applies Lane 0 HSRX offset calibration** 1'b0: Does not use calibration result 1'b1: Use calibration result

15008308	MIPI_RX_CON08_CSI0	MIPI RX Config Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AD_CSI0_LNRD1_HSRX_OFFSET_OUT	RG_CSI0_LNRD1_HSRX_OFFSET_CODE					RG_CSI0_LNRD1_HSRX_CAL_EN	RG_CSI0_LNRD1_HSRX_CAL_APPLY
Type									RO	RW					RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
7	AD_CSI0_LNRD1_HSRX_OFFSET_OUT	**Lane 1 HSRX offset compared output**
6:2	RG_CSI0_LNRD1_HSRX_OFFSET_CODE	**Lane 1 HSRX offset calibration code** 5'b0xxxx: Increase positive output voltage 5'b1xxxx: Increase negative output voltage 5'bx0000: Minimum output voltage 5'bx1111: Maximum output voltage
1	RG_CSI0_LNRD1_HSRX_CAL_EN	**Enables Lane 1 HSRX offset calibration** 1'b0: Disable 1'b1: Enable
0	RG_CSI0_LNRD1_HSRX_CAL_APPLY	**Applies Lane 1 HSRX offset calibration** 1'b0: Does not use calibration result 1'b1: Use calibration result

1500830C **MIPI_RX_CONOC_CSI0** **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name									AD_CSI0_LNRD2_HSRX_OFFSET_OUT	RG_CSI0_LNRD2_HSRX_OFFSET_CODE					RG_CSI0_LNRD2_HSRX_CAL_EN	RG_CSI0_LNRD2_HSRX_CAL_APPLY
Type									RO	RW					RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	AD_CSI0_LNRD2_HSRX_OFFSET_OUT	**Lane 2 HSRX offset compared output**
6:2	RG_CSI0_LNRD2_HSRX_OFFSET_CODE	**Lane 2 HSRX offset calibration code** 5'b0xxxx: Increase positive output voltage 5'b1xxxx: Increase negative output voltage 5'bx0000: Minimum output voltage 5'bx1111: Maximum output voltage
1	RG_CSI0_LNRD2_HSRX_CAL_EN	**Enables Lane 2 HSRX offset calibration** 1'b0: Disable 1'b1: Enable
0	RG_CSI0_LNRD2_HSRX_CAL_APPLY	**Applies Lane 2 HSRX offset calibration** 1'b0: Does not use calibration result 1'b1: Use calibration result

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15008310 MIPI_RX_CON10_CSI0 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AD_CSI0_LNRD3_HSRX_OFFSET_OUT	RG_CSI0_LNRD3_HSRX_OFFSET_CODE					RG_CSI0_LNRD3_HSRX_CAL_EN	RG_CSI0_LNRD3_HSRX_CAL_APPLY
Type									RO	RW					RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	AD_CSI0_LNRD3_HSRX_OFFSET_OUT	**Lane 3 HSRX offset compared output**
6:2	RG_CSI0_LNRD3_HSRX_OFFSET_CODE	**Lane 3 HSRX offset calibration code** 5'b0xxxx: Increase positive output voltage 5'b1xxxx: Increase negative output voltage 5'bx0000: Minimum output voltage 5'bx1111: Maximum output voltage
1	RG_CSI0_LNRD3_HSRX_CAL_EN	**Enables Lane 3 HSRX offset calibration** 1'b0: Disable 1'b1: Enable
0	RG_CSI0_LNRD3_HSRX_CAL_APPLY	**Applies Lane 3 HSRX offset calibration** 1'b0: Does not use calibration result 1'b1: Use calibration result

15008324 MIPI_RX_CON24_CSI0 MIPI RX Config Register E4000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI0_BIST_LN3_MUX		CSI0_BIST_LN2_MUX		CSI0_BIST_LN1_MUX		CSI0_BIST_LN0_MUX		CSI0_BIST_SETTLE_DELAY							
Type	RW		RW		RW		RW		RW							
Reset	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI0_BIST_TERM_DELAY								CSI0_BIST_CLK4X_SEL	CSI0_BIST_CLK_SEL	CSI0_BIST_FIX_PAT			CSI0_BIST_EN	CSI0_BIST_NUM	
Type	RW								RW	RW	RW			RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0			0	0	0

Bit(s)	Name	Description
31:30	CSI0_BIST_LN3_M	**CSI0 lane mux**

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Bit(s)	Name	Description
	UX	
29:28	CSI0_BIST_LN2_MUX	**CSI0 lane mux**
27:26	CSI0_BIST_LN1_MUX	**CSI0 lane mux**
25:24	CSI0_BIST_LN0_MUX	**CSI0 lane mux**
23:16	CSI0_BIST_SETTLE_DELAY	**CSI0 settle delay setting**
15:8	CSI0_BIST_TERM_DELAY	**CSI0 term delay setting**
7	CSI0_BIST_CLK4X_SEL	**Selects CSI0 CLK4X** 0: Inverse 1: No inverse
6	CSI0_BIST_CLK_SEL	**Selects CSI0 CLK** 0: Inverse 1: No inverse
5	CSI0_BIST_FIX_PAT	**CSI0 BIST pattern** 0: Random 1: Fixed
2	CSI0_BIST_EN	**Enables CSI0 BIST**
1:0	CSI0_BIST_NUM	**CSI0 BIST number** 0: 1 lane 1: 2 lane 2: 3 lane 3: 4 lane

15008328 **MIPI_RX_CON28_CSI0** **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CSI0_BIST_CSI2_DATA_OK	CSI0_BIST_LANE_FSM_OK	CSI0_BIST_HS_FSM_OK	CSI0_BIST_DATA_OK	CSI0_BIST_START
Type												RO	RO	RO	RO	RO
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	CSI0_BIST_CSI2_DATA_OK	CSI0 BIST CSI2 data ok
3	CSI0_BIST_LANE_FSM_OK	CSI0 BIST high speed FSM ok
2	CSI0_BIST_HS_FSM_OK	CSI0 BIST data lane FSM ok
1	CSI0_BIST_DATA_	CSI0 BIST DPHY data ok

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Bit(s)	Name	Description
	OK	
0	CSI0_BIST_START	CSI0 BIST start status

15008334 **MIPI_RX_CON34_CSI0** **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name																BIST_MODE
Type																RW
Reset																0

Bit(s)	Name	Description
0	BIST_MODE	Enables BIST mode

15008338 **MIPI_RX_CON38_CSI0** **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name											MIPI_RX_MACRO_SRC_SEL	MIPI_RX_HW_CAL_SW_RST	MIPI_RX_HW_CAL_OPTION	MIPI_RX_HW_CAL_START	MIPI_RX_SW_CAL_MODE	MIPI_RX_SW_CTRL_MODE
Type											RW	RW	RW	RW	RW	RW
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5	MIPI_RX_MACRO_SRC_SEL	0: Internal CSI2 1: External CSI2
4	MIPI_RX_HW_CAL_SW_RST	**HW Calibration SW reset**
3	MIPI_RX_HW_CAL_OPTION	**HW calibration option** 0: 8 cycles 1: 16cycles
2	MIPI_RX_HW_CAL_START	**Triggers HW calibration**
1	MIPI_RX_SW_CAL_MODE	**SW calibration mode**
0	MIPI_RX_SW_CTRL_MODE	**SW control mode**

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1500833C MIPI_RX_CON3C_CSI0 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIPI_RX_SW_CTRL_[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIPI_RX_SW_CTRL_[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MIPI_RX_SW_CTRL_	SW control

15008340 MIPI_RX_CON40_CSI0 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_CSI0_LNRD3_HSRX_INVERT	RG_CSI0_LNRD3_LPRX_SWAP	RG_CSI0_LNRD2_HSRX_INVERT	RG_CSI0_LNRD2_LPRX_SWAP	RG_CSI0_LNRD1_HSRX_INVERT	RG_CSI0_LNRD1_LPRX_SWAP	RG_CSI0_LNRD0_HSRX_INVERT	RG_CSI0_LNRD0_LPRX_SWAP			RG_CSI0_LNRC_HSRX_INVERT	RG_CSI0_LNRC_LPRX_SWAP
Type					RW	RW	RW	RW	RW	RW	RW	RW			RW	RW
Reset					0	0	0	0	0	0	0	0			0	0

Bit(s)	Name	Description
11	RG_CSI0_LNRD3_HSRX_INVERT	
10	RG_CSI0_LNRD3_LPRX_SWAP	
9	RG_CSI0_LNRD2_HSRX_INVERT	
8	RG_CSI0_LNRD2_LPRX_SWAP	
7	RG_CSI0_LNRD1_HSRX_INVERT	
6	RG_CSI0_LNRD1_LPRX_SWAP	
5	RG_CSI0_LNRD0_HSRX_INVERT	
4	RG_CSI0_LNRD0_LPRX_SWAP	
1	RG_CSI0_LNRC_HSRX_INVERT	

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Bit(s)	Name	Description
0	RG_CSI0_LNRC_LPRX_SWAP	

15008344 **MIPI_RX_CON44_CSI0** **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										DA_CSI0_LNRD1_HSRX_OFFSET_CODE					DA_CSI0_LNRD1_HSRX_CAL_EN	DA_CSI0_LNRD1_HSRX_CAL_APPLY
Type										RO					RO	RO
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DA_CSI0_LNRC_HSRX_OFFSET_CODE					DA_CSI0_LNRC_HSRX_CAL_EN	DA_CSI0_LNRC_HSRX_CAL_APPLY		DA_CSI0_LNRD0_HSRX_OFFSET_CODE					DA_CSI0_LNRD0_HSRX_CAL_EN	DA_CSI0_LNRD0_HSRX_CAL_APPLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
22:18	DA_CSI0_LNRD1_HSRX_OFFSET_CODE	
17	DA_CSI0_LNRD1_HSRX_CAL_EN	
16	DA_CSI0_LNRD1_HSRX_CAL_APPLY	
14:10	DA_CSI0_LNRC_HSRX_OFFSET_CODE	
9	DA_CSI0_LNRC_HSRX_CAL_EN	
8	DA_CSI0_LNRC_HSRX_CAL_APPLY	
6:2	DA_CSI0_LNRD0_HSRX_OFFSET_CODE	
1	DA_CSI0_LNRD0_HSRX_CAL_EN	
0	DA_CSI0_LNRD0_HSRX_CAL_APPLY	

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15008348 **MIPI_RX_CON48_CSI0** **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name		DA_CSI0_LNRD3_HSRX_OFFSET_CODE					DA_CSI0_LNRD3_HSRX_CAL_EN	DA_CSI0_LNRD3_HSRX_CAL_APPLY		DA_CSI0_LNRD2_HSRX_OFFSET_CODE					DA_CSI0_LNRD2_HSRX_CAL_EN	DA_CSI0_LNRD2_HSRX_CAL_APPLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
14:10	DA_CSI0_LNRD3_HSRX_OFFSET_CODE	
9	DA_CSI0_LNRD3_HSRX_CAL_EN	
8	DA_CSI0_LNRD3_HSRX_CAL_APPLY	
6:2	DA_CSI0_LNRD2_HSRX_OFFSET_CODE	
1	DA_CSI0_LNRD2_HSRX_CAL_EN	
0	DA_CSI0_LNRD2_HSRX_CAL_APPLY	

15008350 **MIPI_RX_CON50_CSI0** **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name											RG_CSI0_4XCLK_MON	RG_CSI0_BCLK_MON				RG_CSI0_BCLK_INV
Type											RW	RW				RW
Reset											0	0				0

Bit(s)	Name	Description
5	RG_CSI0_4XCLK_MON	**CSI0 4X clock monitor**
4	RG_CSI0_BCLK_MON	**CSI0 byte clock monitor**

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Bit(s)	Name	Description
0	RG_CSI0_BCLK_INV	**CSI0 byte clock** 0: No inverse 1: Inverse

15008700 **MIPI_RX_CON00_CSI1** **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AD_CSI0_LNRC_HSRX_OFFSET_OUT	RG_CSI0_LNRC_HSRX_OFFSET_CODE					RG_CSI0_LNRC_HSRX_CAL_EN	RG_CSI0_LNRC_HSRX_CAL_APPLY
Type									RO	RW					RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	AD_CSI0_LNRC_HSRX_OFFSET_OUT	**CK Lane 0 HSRX offset compared output**
6:2	RG_CSI0_LNRC_HSRX_OFFSET_CODE	**CK Lane 0 HSRX offset calibration code** 5'b0xxxx: Increase positive output voltage 5'b1xxxx: Increase negative output voltage 5'bx0000: Minimum output voltage 5'bx1111: Maximum output voltage
1	RG_CSI0_LNRC_HSRX_CAL_EN	**Enables CK Lane 0 HSRX offset calibration** 1'b0: Disable 1'b1: Enable
0	RG_CSI0_LNRC_HSRX_CAL_APPLY	**Applies CK Lane 0 HSRX offset calibration** 1'b0: Does not use calibration result 1'b1: Use calibration result

15008704 **MIPI_RX_CON04_CSI1** **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AD_CSI0_LNRD0_HSRX_OFFSET_OU	RG_CSI0_LNRD0_HSRX_OFFSET_CODE					RG_CSI0_LNRD0_HSRX_CAL_EN	RG_CSI0_LNRD0_HSRX_CAL_APPLY

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									T							
Type									RO	RW					RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	AD_CSI0_LNRD0_HSRX_OFFSET_OUT	**Lane0 HSRX offset compared output**
6:2	RG_CSI0_LNRD0_HSRX_OFFSET_CODE	**Lane0 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
1	RG_CSI0_LNRD0_HSRX_CAL_EN	**Enables Lane 0 HSRX offset calibration** 1'b0: Disable 1'b1: Enable
0	RG_CSI0_LNRD0_HSRX_CAL_APPLY	**Applies Lane 0 HSRX offset calibration** 1'b0: Does not use calibration result 1'b1: Use calibration result

15008708 **MIPI_RX_CON08_CSI1** **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**AD_CSI0_LNRD1_HSRX_OFFSET_OUT**	**RG_CSI0_LNRD1_HSRX_OFFSET_CODE**					**RG_CSI0_LNRD1_HSRX_CAL_EN**	**RG_CSI0_LNRD1_HSRX_CAL_APPLY**
Type									RO	RW					RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	AD_CSI0_LNRD1_HSRX_OFFSET_OUT	**Lane 1 HSRX offset compared output**
6:2	RG_CSI0_LNRD1_HSRX_OFFSET_CODE	**Lane1 HSRX offset calibration code** 5'b0xxxx: Increase positive output voltage 5'b1xxxx: Increase negative output voltage 5'bx0000: Minimum output voltage 5'bx1111: Maximum output voltage
1	RG_CSI0_LNRD1_HSRX_CAL_EN	**Enables Lane 1 HSRX offset calibration** 1'b0: Disable 1'b1: Enable
0	RG_CSI0_LNRD1_HSRX_CAL_APPLY	**Applies Lane 1 HSRX offset calibration** 1'b0: Does not use calibration result 1'b1: Use calibration result

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1500870C **MIPI_RX_CON0C_CSI1** **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**AD_CSI0_LNRD2_HSRX_OFFSET_OUT**	**RG_CSI0_LNRD2_HSRX_OFFSET_CODE**					**RG_CSI0_LNRD2_HSRX_CAL_EN**	**RG_CSI0_LNRD2_HSRX_CAL_APPLY**
Type									RO	RW					RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	AD_CSI0_LNRD2_HSRX_OFFSET_OUT	**Lane 2 HSRX offset compared output**
6:2	RG_CSI0_LNRD2_HSRX_OFFSET_CODE	**Lane 2 HSRX offset calibration code** 5'b0xxxx: Increase positive output voltage 5'b1xxxx: Increase negative output voltage 5'bx0000: Minimum output voltage 5'bx1111: Maximum output voltage
1	RG_CSI0_LNRD2_HSRX_CAL_EN	**Enables Lane 2 HSRX offset calibration** 1'b0: Disable 1'b1: Enable
0	RG_CSI0_LNRD2_HSRX_CAL_APPLY	**Applies Lane 2 HSRX offset calibration** 1'b0: Does not use calibration result 1'b1: Use calibration result

15008710 **MIPI_RX_CON10_CSI1** **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**AD_CSI0_LNRD3_HSRX_OFFSET_OUT**	**RG_CSI0_LNRD3_HSRX_OFFSET_CODE**					**RG_CSI0_LNRD3_HSRX_CAL_EN**	**RG_CSI0_LNRD3_HSRX_CAL_APPLY**
Type									RO	RW					RW	RW
Reset									0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
7	AD_CSI0_LNRD3_HSRX_OFFSET_OUT	**Lane 3 HSRX offset compared output**
6:2	RG_CSI0_LNRD3_HSRX_OFFSET_CODE	**Lane 3 HSRX offset calibration code** 5'b0xxxx: Increase positive output voltage 5'b1xxxx: Increase negative output voltage 5'bx0000: Minimum output voltage 5'bx1111: Maximum output voltage
1	RG_CSI0_LNRD3_HSRX_CAL_EN	**Enables Lane 3 HSRX offset calibration** 1'b0: Disable 1'b1: Enable
0	RG_CSI0_LNRD3_HSRX_CAL_APPLY	**Applies Lane 3 HSRX offset calibration** 1'b0: Does not use calibration result 1'b1: Use calibration result

15008724 **MIPI_RX_CON24_CSI1** **MIPI RX Config Register** **E4000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI0_BIST_LN3_MUX		CSI0_BIST_LN2_MUX		CSI0_BIST_LN1_MUX		CSI0_BIST_LN0_MUX		CSI0_BIST_SETTLE_DELAY							
Type	RW		RW		RW		RW		RW							
Reset	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI0_BIST_TERM_DELAY								CSI0_BIST_CLK4X_SEL	CSI0_BIST_CLK_SEL	CSI0_BIST_FIX_PAT			CSI0_BIST_EN	CSI0_BIST_NUM	
Type	RW								RW	RW	RW			RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0			0	0	0

Bit(s)	Name	Description
31:30	CSI0_BIST_LN3_MUX	**CSI0 lane mux**
29:28	CSI0_BIST_LN2_MUX	**CSI0 lane mux**
27:26	CSI0_BIST_LN1_MUX	**CSI0 lane mux**
25:24	CSI0_BIST_LN0_MUX	**CSI0 lane mux**
23:16	CSI0_BIST_SETTLE_DELAY	**CSI0 settle delay setting**
15:8	CSI0_BIST_TERM_DELAY	**CSI0 term delay setting**
7	CSI0_BIST_CLK4X_SEL	**Selects CSI0 CLK4X** 0: Inverse 1: No inverse
6	CSI0_BIST_CLK_SEL	**Selects CSI0 CLK** 0: Inverse 1: No inverse

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Bit(s)	Name	Description
5	CSI0_BIST_FIX_PAT	**CSI0 BIST pattern** 0: Random 1: Fixed
2	CSI0_BIST_EN	**Enables CSI0 BIST**
1:0	CSI0_BIST_NUM	**CSI0 BIST number** 0: 1 lane 1: 2 lane 2: 3 lane 3: 4 lane

15008728 **MIPI_RX_CON28_CSI1** **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CSI0_BIST_CSI2_DATA_OK	CSI0_BIST_LANE_FSM_OK	CSI0_BIST_HS_FSM_OK	CSI0_BIST_DATA_OK	CSI0_BIST_START
Type												RO	RO	RO	RO	RO
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	CSI0_BIST_CSI2_DATA_OK	CSI0 BIST CSI2 data ok
3	CSI0_BIST_LANE_FSM_OK	CSI0 BIST high speed FSM ok
2	CSI0_BIST_HS_FSM_OK	CSI0 BIST data lane FSM ok
1	CSI0_BIST_DATA_OK	CSI0 BIST DPHY data ok
0	CSI0_BIST_START	CSI0 BIST start status

15008734 **MIPI_RX_CON34_CSI1** **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BIST_MODE
Type																RW
Reset																0

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Bit(s)	Name	Description
0	BIST_MODE	Enables BIST mode

15008738 **MIPI_RX_CON38_CSI1** **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											**MIPI_RX_MACRO_SRC_SEL**	**MIPI_RX_HW_CAL_SW_RST**	**MIPI_RX_HW_CAL_OPTION**	**MIPI_RX_HW_CAL_START**	**MIPI_RX_SW_CAL_MODE**	**MIPI_RX_SW_CTRL_MODE**
Type											RW	RW	RW	RW	RW	RW
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5	MIPI_RX_MACRO_SRC_SEL	0: Internal CSI2 1: External CSI2
4	MIPI_RX_HW_CAL_SW_RST	**HW calibration SW reset**
3	MIPI_RX_HW_CAL_OPTION	**HW calibration option** 0: 8 cycles 1: 16cycles
2	MIPI_RX_HW_CAL_START	**Triggers HW calibration**
1	MIPI_RX_SW_CAL_MODE	**SW calibration mode**
0	MIPI_RX_SW_CTRL_MODE	**SW control mode**

1500873C **MIPI_RX_CON3C_CSI1** **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MIPI_RX_SW_CTRL_[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MIPI_RX_SW_CTRL_[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MIPI_RX_SW_CTRL_	SW control

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15008740 **MIPI_RX_CON40_CSI1** **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_CSI0_LNRD3_HSRX_INVERT	RG_CSI0_LNRD3_LPRX_SWAP	RG_CSI0_LNRD2_HSRX_INVERT	RG_CSI0_LNRD2_LPRX_SWAP	RG_CSI0_LNRD1_HSRX_INVERT	RG_CSI0_LNRD1_LPRX_SWAP	RG_CSI0_LNRD0_HSRX_INVERT	RG_CSI0_LNRD0_LPRX_SWAP			RG_CSI0_LNRC_HSRX_INVERT	RG_CSI0_LNRC_LPRX_SWAP
Type					RW	RW	RW	RW	RW	RW	RW	RW			RW	RW
Reset					0	0	0	0	0	0	0	0			0	0

Bit(s)	Name	Description
11	RG_CSI0_LNRD3_HSRX_INVERT	
10	RG_CSI0_LNRD3_LPRX_SWAP	
9	RG_CSI0_LNRD2_HSRX_INVERT	
8	RG_CSI0_LNRD2_LPRX_SWAP	
7	RG_CSI0_LNRD1_HSRX_INVERT	
6	RG_CSI0_LNRD1_LPRX_SWAP	
5	RG_CSI0_LNRD0_HSRX_INVERT	
4	RG_CSI0_LNRD0_LPRX_SWAP	
1	RG_CSI0_LNRC_HSRX_INVERT	
0	RG_CSI0_LNRC_LPRX_SWAP	

15008744 **MIPI_RX_CON44_CSI1** **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										DA_CSI0_LNRD1_HSRX_OFFSET_CODE					DA_CSI0_LNRD1_HSRX_CAL_EN	DA_CSI0_LNRD1_HSRX_CAL_APPLY
Type										RO					RO	RO
Reset										0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DA_CSI0_LNRC_HSRX_OFF					DA_	DA_		DA_CSI0_LNRD0_HSRX_OF					DA_	DA_

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		SET_CODE					CSI0_LNRC_HSRX_CAL_EN	CSI0_LNRC_HSRX_CAL_APPLY		FSET_CODE					CSI0_LNRD0_HSRX_CAL_EN	CSI0_LNRD0_HSRX_CAL_APPLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
22:18	DA_CSI0_LNRD1_HSRX_OFFSET_CODE	
17	DA_CSI0_LNRD1_HSRX_CAL_EN	
16	DA_CSI0_LNRD1_HSRX_CAL_APPLY	
14:10	DA_CSI0_LNRC_HSRX_OFFSET_CODE	
9	DA_CSI0_LNRC_HSRX_CAL_EN	
8	DA_CSI0_LNRC_HSRX_CAL_APPLY	
6:2	DA_CSI0_LNRD0_HSRX_OFFSET_CODE	
1	DA_CSI0_LNRD0_HSRX_CAL_EN	
0	DA_CSI0_LNRD0_HSRX_CAL_APPLY	

15008748 **MIPI_RX_CON48_CSI1** **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DA_CSI0_LNRD3_HSRX_OFFSET_CODE					DA_CSI0_LNRD3_HSRX_CAL_EN	DA_CSI0_LNRD3_HSRX_CAL_APPLY		DA_CSI0_LNRD2_HSRX_OFFSET_CODE					DA_CSI0_LNRD2_HSRX_CAL_EN	DA_CSI0_LNRD2_HSRX_CAL_APPLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
14:10	DA_CSI0_LNRD3_HSRX_OFFSET_CO	

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Bit(s)	Name	Description
	DE	
9	DA_CSI0_LNRD3_HSRX_CAL_EN	
8	DA_CSI0_LNRD3_HSRX_CAL_APPLY	
6:2	DA_CSI0_LNRD2_HSRX_OFFSET_CODE	
1	DA_CSI0_LNRD2_HSRX_CAL_EN	
0	DA_CSI0_LNRD2_HSRX_CAL_APPLY	

15008750 **MIPI_RX_CON50_CSI1** **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_CSI0_4XCLK_MON	RG_CSI0_BCLK_MON				RG_CSI0_BCLK_INV
Type											RW	RW				RW
Reset											0	0				0

Bit(s)	Name	Description
5	RG_CSI0_4XCLK_MON	**CSI0 4X clock monitor**
4	RG_CSI0_BCLK_MON	**CSI0 byte clock monitor**
0	RG_CSI0_BCLK_INV	**CSI0 byte clock** 0: No inverse 1: Inverse

Module name: mipi_rx_ana_csi0 Base address: (+10215800h)

Address	Name	Width	Register Function
10215800	MIPI_RX_ANA00_CSI0	32	MIPI RX CSI0 Clock Lane Register
10215804	MIPI_RX_ANA04_CSI0	32	MIPI RX CSI0 Data Lane 0 Register
10215808	MIPI_RX_ANA08_CSI0	32	MIPI RX CSI0 Data Lane 1 Register
1021580C	MIPI_RX_ANA0C_CSI0	32	MIPI RX CSI0 Data Lane 2 Register
10215810	MIPI_RX_ANA10_CSI0	32	MIPI RX CSI0 Data Lane 3 Register
10215820	MIPI_RX_ANA20_CSI0	32	MIPI RX CSI Register
10215824	MIPI_RX_ANA24_CSI0	32	MIPI RX CSI BG Register
10215828	MIPI_RX_ANA28_CSI0	32	MIPI RX CSI BG Register
10215830	MIPI_RX_ANA30_CSI0	32	MIPI RX ADDA Debug Register

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Address	Name	Width	Register Function
10215844	MIPI_RX_ANA44_CSI0	32	MIPI RX Monitor Mux
1021584C	MIPI_RX_ANA4C_CSI0	32	GPI
10215850	MIPI_RX_ANA50_CSI0	32	GPI
10215854	MIPI_RX_ANA54_CSI0	32	GPI

10215800 MIPI_RX_ANA00_CSI0 MIPI RX CSI0 Clock Lane Register 00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							RG_CSI0_LNRC_HSRX2_IMINUS	RG_CSI0_LNRC_HSRX2_IPLUS	RG_CSI0_LNRC_HSRX_DELAY_CODE				RG_CSI0_LNRC_HSRX_DELAY_EN			
Type							RW	RW	RW				RW			
Reset							0	0	0	0	0	0	0			
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RG_CSI0_LNRC_RT_CODE				RG_CSI0_LNRC_HSRX_IMINUS	RG_CSI0_LNRC_HSRX_IPLUS	RG_CSI0_LNRC_LPRX_IMINUS	RG_CSI0_LNRC_LPRX_IPLUS					RG_CSI0_LNRC_INPUT_SEL			RG_CSI0_LNRC_LDO_OUT_EN
Type	RW				RW	RW	RW	RW					RW			RW
Reset	1	0	0	0	0	0	0	0					0			0

Bit(s)	Name	Description
25	RG_CSI0_LNRC_HSRX2_IMINUS	**Adjusts CSI0 CK lane HSRX2 bias current** 1'b0: Normal 1'b1: -10%
24	RG_CSI0_LNRC_HSRX2_IPLUS	**Adjusts CSI0 CK lane HSRX2 bias current** 1'b0: Normal 1'b1: +10%
23:20	RG_CSI0_LNRC_HSRX_DELAY_CODE	**CSI0 CK lane HSRX delay line control code** 4'b0000: Minimum delay 4'b1111: Maximum delay
19	RG_CSI0_LNRC_HSRX_DELAY_EN	**Enables CSI0 CK lane HSRX delay line** 1'b0: Disable delay line for normal operation 1'b1: Enable delay line
15:12	RG_CSI0_LNRC_RT_CODE	**CSI0 CK lane impedance control code** 4'b0000: Maximum impedance 4'b1111: Minimum impedance
11	RG_CSI0_LNRC_HSRX_IMINUS	**Adjusts CSI0 CK lane HSRX bias current** 1'b0: Normal 1'b1: -10%
10	RG_CSI0_LNRC_HSRX_IPLUS	**Adjusts CSI0 CK lane HSRX bias current** 1'b0: Normal 1'b1: +10%
9	RG_CSI0_LNRC_L	**Adjusts CSI0 CK lane LPRX bias current**

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Bit(s)	Name	Description
	PRX_IMINUS	1'b0: Normal 1'b1: -10%
8	RG_CSI0_LNRC_LPRX_IPLUS	**Adjusts CSI0 CK lane LPRX bias current** 1'b0: Normal 1'b1: +10%
3	RG_CSI0_LNRC_INPUT_SEL	**Selects CSI0 CK lane analog mux** 1'b0: High z 1'b1: Select this lane
0	RG_CSI0_LNRC_LDO_OUT_EN	**Enables CSI0 CK lane LDO output** 1'b0: Disable LDO output 1'b1: Enable LDO output

10215804 **MIPI_RX_ANA04_CSI0** **MIPI RX CSI0 Data Lane 0 Register** **00008000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI0_LNRD0_HSRX2_IMINUS	RG_CSI0_LNRD0_HSRX2_IPLUS	RG_CSI0_LNRD0_HSRX_DELAY_CODE				RG_CSI0_LNRD0_HSRX_DELAY_EN	RG_CSI0_LNRD0_HSRX_BYPASS_SYNC		RG_CSI0_LNRD0_HSRX_DET_SEL	RG_CSI0_LNRD0_HSRX_FORCE_SYNC		RG_CSI0_LNRD0_HSRX_EDGE_SEL	
Type			RW	RW	RW				RW	RW		RW	RW		RW	
Reset			0	0	0	0	0	0	0	0		0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI0_LNRD0_RT_CODE				RG_CSI0_LNRD0_HSRX_IMINUS	RG_CSI0_LNRD0_HSRX_IPLUS	RG_CSI0_LNRD0_LPRX_IMINUS	RG_CSI0_LNRD0_LPRX_IPLUS					RG_CSI0_LNRD0_INPUT_SEL			RG_CSI0_LNRD0_LDO_OUT_EN
Type	RW				RW	RW	RW	RW					RW			RW
Reset	1	0	0	0	0	0	0	0					0			0

Bit(s)	Name	Description
29	RG_CSI0_LNRD0_HSRX2_IMINUS	**Adjusts CSI0 Lane 0 HSRX bias current** 1'b0: Normal 1'b1: -10%
28	RG_CSI0_LNRD0_HSRX2_IPLUS	**Adjusts CSI0 Lane 0 HSRX bias current** 1'b0: Normal 1'b1: +10%
27:24	RG_CSI0_LNRD0_HSRX_DELAY_CODE	**CSI0 data Lane 0 HSRX delay line control code** 4'b0000: Minimum delay 4'b1111: Maximum delay
23	RG_CSI0_LNRD0_HSRX_DELAY_EN	**Enables CSI0 data Lane 0 HSRX delay line** 1'b0: Disable delay line for normal operation 1'b1: Enable delay line
22	RG_CSI0_LNRD0_HSRX_BYPASS_SYNC	**CSI0 Lane 0 bypass sync detect function** 1'b0: Use analog sync detect function 1'b1: Disable sync detect; word alignment at digital

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Bit(s)	Name	Description
20	RG_CSI0_LNRD0_HSRX_DET_SEL	**Selects CSI0 Lane 0 HS detect** 1'b0: Detect DIFF-N 1'b1: Detect DIFF-P
19:18	RG_CSI0_LNRD0_HSRX_FORCE_SYNC	**Selects CSI0 Lane 0 HS force sync** 2'b00: Sync with pattern B8 2'b01: Sync falling edge with the first bit 2'b10: Sync rising edge with the first bit 2'b11: Prohibited
17:16	RG_CSI0_LNRD0_HSRX_EDGE_SEL	**Selects CSI0 Lane 0 HS sync edge** 2'b00: Sync both edges 2'b01: Sync falling edge only 2'b10: Sync rising edge only 2'b11: Prohibited
15:12	RG_CSI0_LNRD0_RT_CODE	**CSI0 Lane 0 impedance control code** 4'b0000: Maximum impedance 4'b1111: Minimum impedance
11	RG_CSI0_LNRD0_HSRX_IMINUS	**Adjusts CSI0 Lane 0 HSRX bias current** 1'b0: Normal 1'b1: -10%
10	RG_CSI0_LNRD0_HSRX_IPLUS	**Adjusts CSI0 Lane 0 HSRX bias current** 1'b0: Normal 1'b1: +10%
9	RG_CSI0_LNRD0_LPRX_IMINUS	**Adjusts CSI0 Lane 0 LPRX bias current** 1'b0: Normal 1'b1: -10%
8	RG_CSI0_LNRD0_LPRX_IPLUS	**Adjusts CSI0 Lane 0 LPRX bias current** 1'b0: Normal 1'b1: +10%
3	RG_CSI0_LNRD0_INPUT_SEL	**Selects CSI0 Lane 0 analog mux** 1'b0: High z 1'b1: Select this lane
0	RG_CSI0_LNRD0_LDO_OUT_EN	**Enables CSI0 Lane 0 LDO output** 1'b0: Disable LDO output 1'b1: Enable LDO output

10215808 **<u>MIPI_RX_ANA08_CSI0</u>** **MIPI RX CSI0 Data Lane 1 Register** **00008000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI0_LNRD1_HSRX2_IMINUS	RG_CSI0_LNRD1_HSRX2_IPLUS	RG_CSI0_LNRD1_HSRX_DELAY_CODE				RG_CSI0_LNRD1_HSRX_DELAY_EN	RG_CSI0_LNRD1_HSRX_BYPASS_SYNC		RG_CSI0_LNRD1_HSRX_DET_SEL	RG_CSI0_LNRD1_HSRX_FORCE_SYNC		RG_CSI0_LNRD1_HSRX_EDGE_SEL	
Type			RW	RW	RW				RW	RW		RW	RW		RW	
Reset			0	0	0	0	0	0	0	0		0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI0_LNRD1_RT_CODE				RG_CSI0_LNRD1	RG_CSI0_LNRD1	RG_CSI0_LNRD1	RG_CSI0_LNRD1					RG_CSI0_LNRD1			RG_CSI0_LNRD1

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					_HS RX_ IMI NUS	_HS RX_ IPL US	_LP RX_ IMI NUS	_LP RX_ IPL US					_IN PUT _SE L			_LD O_O UT_ EN
Type	RW				RW	RW	RW	RW					RW			RW
Reset	1	0	0	0	0	0	0	0					0			0

Bit(s)	Name	Description
29	RG_CSI0_LNRD1_ HSRX2_IMINUS	**Adjusts CSI0 Lane 1 HSRX bias current** 1'b0: Normal 1'b1: -10%
28	RG_CSI0_LNRD1_ HSRX2_IPLUS	**Adjusts CSI0 Lane 1 HSRX bias current** 1'b0: Normal 1'b1: +10%
27:24	RG_CSI0_LNRD1_ HSRX_DELAY_CO DE	**CSI0 data Lane 1 HSRX delay line control code** 4'b0000: Minimum delay 4'b1111: Maximum delay
23	RG_CSI0_LNRD1_ HSRX_DELAY_EN	**Enables CSI0 data Lane 1 HSRX delay line** 1'b0: Disable delay line for normal operation 1'b1: Enable delay line
22	RG_CSI0_LNRD1_ HSRX_BYPASS_SY NC	**CSI0 Lane 1 bypass sync detect function** 1'b0: Use analog sync detect function 1'b1: Disable sync detect; word alignment at digital
20	RG_CSI0_LNRD1_ HSRX_DET_SEL	**Selects CSI0 Lane 1 HS detect** 1'b0: Detect DIFF-N 1'b1: Detect DIFF-P
19:18	RG_CSI0_LNRD1_ HSRX_FORCE_SY NC	**Adjusts CSI0 Lane 1 HS force sync** 2'b00: Sync with pattern B8 2'b01: Sync falling edge with the first bit 2'b10: Sync rising edge with the first bit 2'b11: Prohibited
17:16	RG_CSI0_LNRD1_ HSRX_EDGE_SEL	**Selects CSI0 Lane 1 HS sync edge** 2'b00: Sync both edges 2'b01: Sync falling edge only 2'b10: Sync rising edge only 2'b11: Prohibited
15:12	RG_CSI0_LNRD1_ RT_CODE	**CSI0 Lane 1 impedance control code** 4'b0000: Maximum impedance 4'b1111: Minimum impedance
11	RG_CSI0_LNRD1_ HSRX_IMINUS	**Adjusts CSI0 Lane 1 HSRX bias current** 1'b0: Normal 1'b1: -10%
10	RG_CSI0_LNRD1_ HSRX_IPLUS	**Adjusts CSI0 Lane 1 HSRX bias current** 1'b0: Normal 1'b1: +10%
9	RG_CSI0_LNRD1_ LPRX_IMINUS	**Adjusts CSI0 Lane 1 LPRX bias current** 1'b0: Normal 1'b1: -10%
8	RG_CSI0_LNRD1_ LPRX_IPLUS	**Adjusts CSI0 Lane 1 LPRX bias current** 1'b0: Normal 1'b1: +10%
3	RG_CSI0_LNRD1_I NPUT_SEL	**Selects CSI0 Lane 1 analog mux** 1'b0: High z 1'b1: Select this lane
0	RG_CSI0_LNRD1_	**Enables CSI0 Lane 1 LDO output**

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Bit(s)	Name	Description
	LDO_OUT_EN	1'b0: Disable LDO output 1'b1: Enable LDO output

1021580C **MIPI_RX_ANA0C_CSI0** **MIPI RX CSI0 Data Lane 2 Register** **00008000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI0_LNRD2_HSRX2_IMINUS	RG_CSI0_LNRD2_HSRX2_IPLUS	RG_CSI0_LNRD2_HSRX_DELAY_CODE				RG_CSI0_LNRD2_HSRX_DELAY_EN	RG_CSI0_LNRD2_HSRX_BYPASS_SYNC		RG_CSI0_LNRD2_HSRX_DET_SEL	RG_CSI0_LNRD2_HSRX_FORCE_SYNC		RG_CSI0_LNRD2_HSRX_EDGE_SEL	
Type			RW	RW	RW				RW	RW		RW	RW		RW	
Reset			0	0	0	0	0	0	0	0		0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI0_LNRD2_RT_CODE				RG_CSI0_LNRD2_HSRX_IMINUS	RG_CSI0_LNRD2_HSRX_IPLUS	RG_CSI0_LNRD2_LPRX_IMINUS	RG_CSI0_LNRD2_LPRX_IPLUS					RG_CSI0_LNRD2_INPUT_SEL			RG_CSI0_LNRD2_LDO_OUT_EN
Type	RW				RW	RW	RW	RW					RW			RW
Reset	1	0	0	0	0	0	0	0					0			0

Bit(s)	Name	Description
29	RG_CSI0_LNRD2_HSRX2_IMINUS	**Adjusts CSI0 Lane 2 HSRX bias current** 1'b0: Normal 1'b1: -10%
28	RG_CSI0_LNRD2_HSRX2_IPLUS	**Adjusts CSI0 Lane 2 HSRX bias current** 1'b0: Normal 1'b1: +10%
27:24	RG_CSI0_LNRD2_HSRX_DELAY_CODE	**CSI0 data Lane 2 HSRX delay line control code** 4'b0000: Minimum delay 4'b1111: Maximum delay
23	RG_CSI0_LNRD2_HSRX_DELAY_EN	**Enables CSI0 data Lane 2 HSRX delay line** 1'b0: Disable delay line for normal operation 1'b1: Enable delay line
22	RG_CSI0_LNRD2_HSRX_BYPASS_SYNC	**CSI0 Lane 2 bypass sync detect function** 1'b0: Use analog sync detect function 1'b1: Disable sync detect; word alignment at digital
20	RG_CSI0_LNRD2_HSRX_DET_SEL	**Selects CSI0 Lane 2 HS detect** 1'b0: Detect DIFF-N 1'b1: Detect DIFF-P
19:18	RG_CSI0_LNRD2_HSRX_FORCE_SYNC	**Selects CSI0 Lane 2 HS force sync** 2'b00: Sync with pattern B8 2'b01: Sync falling edge with the first bit 2'b10: Sync rising edge with the first bit 2'b11: Prohibited
17:16	RG_CSI0_LNRD2_	**Selects CSI0 Lane 2 HS sync edge**

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Bit(s)	Name	Description
	HSRX_EDGE_SEL	2'b00: Sync both edges 2'b01: Sync falling edge only 2'b10: Sync rising edge only 2'b11: Prohibited
15:12	RG_CSI0_LNRD2_RT_CODE	**CSI0 Lane 2 impedance control code** 4'b0000: Maximum impedance 4'b1111: Minimum impedance
11	RG_CSI0_LNRD2_HSRX_IMINUS	**Adjusts CSI0 Lane 2 HSRX bias current** 1'b0: Normal 1'b1: -10%
10	RG_CSI0_LNRD2_HSRX_IPLUS	**Adjusts CSI0 Lane 2 HSRX bias current** 1'b0: Normal 1'b1: +10%
9	RG_CSI0_LNRD2_LPRX_IMINUS	**Adjusts CSI0 Lane 2 LPRX bias current** 1'b0: Normal 1'b1: -10%
8	RG_CSI0_LNRD2_LPRX_IPLUS	**Adjusts CSI0 Lane 2 LPRX bias current** 1'b0: Normal 1'b1: +10%
3	RG_CSI0_LNRD2_INPUT_SEL	**Selects CSI0 Lane 2 analog mux** 1'b0: High z 1'b1: Select this lane
0	RG_CSI0_LNRD2_LDO_OUT_EN	**Enables CSI0 Lane 2 LDO output** 1'b0: Disable LDO output 1'b1: Enable LDO output

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10215810 **MIPI_RX_ANA10_CSI0** **MIPI RX CSI0 Data Lane 3 Register** **00008000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI0_LNRD3_HSRX2_IMINUS	RG_CSI0_LNRD3_HSRX2_IPLUS	RG_CSI0_LNRD3_HSRX_DELAY_CODE				RG_CSI0_LNRD3_HSRX_DELAY_EN	RG_CSI0_LNRD3_HSRX_BYPASS_SYNC		RG_CSI0_LNRD3_HSRX_DET_SEL	RG_CSI0_LNRD3_HSRX_FORCE_SYNC		RG_CSI0_LNRD3_HSRX_EDGE_SEL	
Type			RW	RW	RW				RW	RW		RW	RW		RW	
Reset			0	0	0	0	0	0	0	0		0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RG_CSI0_LNRD3_RT_CODE				RG_CSI0_LNRD3_HSRX_IMINUS	RG_CSI0_LNRD3_HSRX_IPLUS	RG_CSI0_LNRD3_LPRX_IMINUS	RG_CSI0_LNRD3_LPRX_IPLUS					RG_CSI0_LNRD3_INPUT_SEL			RG_CSI0_LNRD3_LDO_OUT_EN
Type	RW				RW	RW	RW	RW					RW			RW
Reset	1	0	0	0	0	0	0	0					0			0

Bit(s)	Name	Description
29	RG_CSI0_LNRD3_	**Adjusts CSI0 Lane 3 HSRX bias current**

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Bit(s)	Name	Description
	HSRX2_IMINUS	1'b0: Normal 1'b1: -10%
28	RG_CSI0_LNRD3_HSRX2_IPLUS	**Adjusts CSI0 Lane 3 HSRX bias current** 1'b0: Normal 1'b1: +10%
27:24	RG_CSI0_LNRD3_HSRX_DELAY_CODE	**CSI0 data Lane 3 HSRX delay line control code** 4'b0000: Minimum delay 4'b1111: Maximum delay
23	RG_CSI0_LNRD3_HSRX_DELAY_EN	**Enables CSI0 data Lane 3 HSRX delay line** 1'b0: Disable delay line for normal operation 1'b1: Enable delay line
22	RG_CSI0_LNRD3_HSRX_BYPASS_SYNC	**CSI0 Lane 3 bypass sync detect function** 1'b0: Use analog sync detect function 1'b1: Disable sync detect; word alignment at digital
20	RG_CSI0_LNRD3_HSRX_DET_SEL	**Selects CSI0 Lane 3 HS detect** 1'b0: Detect DIFF-N 1'b1: Detect DIFF-P
19:18	RG_CSI0_LNRD3_HSRX_FORCE_SYNC	**Selects CSI0 Lane 3 HS force sync** 2'b00: Sync with pattern B8 2'b01: Sync falling edge with the first bit 2'b10: Sync rising edge with the first bit 2'b11: Prohibited
17:16	RG_CSI0_LNRD3_HSRX_EDGE_SEL	**Selects CSI0 Lane 3 HS sync edge** 2'b00: Sync both edges 2'b01: Sync falling edge only 2'b10: Sync rising edge only 2'b11: Prohibited
15:12	RG_CSI0_LNRD3_RT_CODE	**CSI0 Lane 3 impedance control code** 4'b0000: Maximum impedance 4'b1111: Minimum impedance
11	RG_CSI0_LNRD3_HSRX_IMINUS	**Adjusts CSI0 Lane 3 HSRX bias current** 1'b0: Normal 1'b1: -10%
10	RG_CSI0_LNRD3_HSRX_IPLUS	**Adjusts CSI0 Lane 3 HSRX bias current** 1'b0: Normal 1'b1: +10%
9	RG_CSI0_LNRD3_LPRX_IMINUS	**Adjusts CSI0 Lane 3 LPRX bias current** 1'b0: Normal 1'b1: -10%
8	RG_CSI0_LNRD3_LPRX_IPLUS	**Adjusts CSI0 Lane 3 LPRX bias current** 1'b0: Normal 1'b1: +10%
3	RG_CSI0_LNRD3_INPUT_SEL	**Selects CSI0 Lane 3 analog mux** 1'b0: High z 1'b1: Select this lane
0	RG_CSI0_LNRD3_LDO_OUT_EN	**Enables CSI0 Lane 3 LDO output** 1'b0: Disable LDO output 1'b1: Enable LDO output

10215820	**MIPI_RX_ANA20_CSI0**	**MIPI RX CSI Register**	**FF000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI0_SPARE															
Type	RW															
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_CSI0_PRESERVE					RG_CSI0_4XCLK_DISABLE	RG_CSI0_4XCLK_INVERT	RG_CSI0_HSDET_GATING_EN	RG_CSI0_BCLK_SEL		RG_CSI0_LNRD_HSRX_BCLK_INVERT	RG_CSI0_LDO_CORE_EN
Type					RW					RW	RW	RW	RW		RW	RW
Reset					0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	RG_CSI0_SPARE	**CSI0 spare register**
11:8	RG_CSI0_PRESERVE	**CSI0 preserved register**
6	RG_CSI0_4XCLK_DISABLE	**Disable CSI0 4X clock** 1'b0: Output 4XCLK when sync_detect is enabled. 1'b1: Gate 4XCLK when sync_detect is disabled.
5	RG_CSI0_4XCLK_INVERT	**Enables CSI0 4X clock inversion** 1'b0: Does not invert 1'b1: Invert
4	RG_CSI0_HSDET_GATING_EN	**Enables CSI0 HSDET gating** 1'b0: Disable gating. HSDET may toggle in LP-mode. 1'b1: HSDET active with HSRX_EN
3:2	RG_CSI0_BCLK_SEL	**Selects CSI0 byte clock source** Also used for CSI0 HSDET source selection. 2'b00: From Lane 0 2'b01: From Lane 1 2'b10: From Lane 2 2'b11: From Lane 3
1	RG_CSI0_LNRD_HSRX_BCLK_INVERT	**Inverts CSI0 HSRX byteclk** 1'b0: Falling edge align with data/sync 1'b1: Rising edge align with data/sync
0	RG_CSI0_LDO_CORE_EN	**Enables CSI0 LDO core bias** 1'b0: Disable 1'b1: Enable

10215824 **MIPI_RX_ANA24_CSI0** **MIPI RX CSI BG Register** **24248800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI0_V04_SEL			RG_CSI0_V072_SEL					RG_CSI0_V10_SEL			RG_CSI0_V12_SEL		
Type			RW			RW					RW			RW		
Reset			1	0	0	1	0	0			1	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI0_BG_R2_TRIM				RG_CSI0_BG_R1_TRIM							RG_CSI0_BG_FAST_	RG_CSI0_BG_DIV		RG_CSI0_BG_CKEN	RG_CSI0_BG_CORE_

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												CHARGE				EN
Type	RW				RW							RW	RW		RW	RW
Reset	1	0	0	0	1	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
29:27	RG_CSI0_V04_SEL	**Selects CSI0 0.4V output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage
26:24	RG_CSI0_V072_SEL	**Selects CSI0 0.72V output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage
21:19	RG_CSI0_V10_SEL	**Selects CSI0 AVDD10 output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage
18:16	RG_CSI0_V12_SEL	**Selects CSI0 1.2V output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage
15:12	RG_CSI0_BG_R2_TRIM	**Trims CSI BGR R2** ORed with RG_DSI_BG_R2_TRIM[3:0]. 4'b0000: Maximum resistance 4'b1000: Typical resistance 4'b1111: Minimum resistance
11:8	RG_CSI0_BG_R1_TRIM	**Trims CSI BGR R1** ORed with RG_DSI_BG_R1_TRIM[3:0]. 4'b0000: Maximum resistance 4'b1000: Typical resistance 4'b1111: Minimum resistance
4	RG_CSI0_BG_FAST_CHARGE	**Enables BG bias low-pass filter fast charge** ORed with RG_DSI_BG_FAST_CHARGE. 1'b0: Disable. Settling time is 30us. 1'b1: Enable. Settling time is 1us.
3:2	RG_CSI0_BG_DIV	**BG chopper clock divisor control** ORed with RG_DSI_BG_DIV[1:0] 2'b00: /2 2'b01: /4 2'b10: /8 2'b11: /16
1	RG_CSI0_BG_CKEN	**Enables BG chopper clock** ORed with RG_DSI_BG_CKEN 1'b0: Disable 1'b1: Enable
0	RG_CSI0_BG_CORE_EN	**Enables CSI BG** ORed with RG_DSI_BG_CORE_EN 1'b0: Power off 1'b1: Enable

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10215828	MIPI_RX_ANA28_CSI0	MIPI RX CSI BG Register	00000024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											**RG_CSI0_V02_SEL**			**RG_CSI0_V032_SEL**		
Type											RW			RW		
Reset											1	0	0	1	0	0

Bit(s)	Name	Description
5:3	RG_CSI0_V02_SEL	**Selects CSI0 0.2V output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage
2:0	RG_CSI0_V032_SEL	**Selects CSI0 0.32V output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage

10215830 **MIPI_RX_ANA30_CSI0** **MIPI RX ADDA Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**AD_CSI0_LNRD3_HSRX_OFFSET_OUT**	**DA_CSI0_LNRD3_HSRX_EN**	**AD_CSI0_LNRD3_LPRX_DN**	**AD_CSI0_LNRD3_LPRX_DP**	**DA_CSI0_LNRD3_LPRX_EN**	**AD_CSI0_LNRD2_HSRX_OFFSET_OUT**	**DA_CSI0_LNRD2_HSRX_EN**	**AD_CSI0_LNRD2_LPRX_DN**	**AD_CSI0_LNRD2_LPRX_DP**	**DA_CSI0_LNRD2_LPRX_EN**	**AD_CSI0_LNRD1_HSRX_OFFSET_OUT**	**DA_CSI0_LNRD1_HSRX_EN**	**AD_CSI0_LNRD1_LPRX_DN**
Type				RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AD_CSI0_LNRD1_LPRX_DP**	**DA_CSI0_LNRD1_LPRX_EN**	**AD_CSI0_LNRD0_HSRX_OFFSET_OUT**	**DA_CSI0_LNRD0_HSRX_EN**	**AD_CSI0_LNRD0_LPRX_DN**	**AD_CSI0_LNRD0_LPRX_DP**	**DA_CSI0_LNRD0_LPRX_EN**	**AD_CSI0_LNRC_HSRX_OFFSET_OUT**	**DA_CSI0_LNRC_HSRX_EN**	**AD_CSI0_LNRC_LPRX_DN**	**AD_CSI0_LNRC_LPRX_DP**	**DA_CSI0_LNRC_LPRX_EN**			**AD_CSI0_LNRD_HSDET**	**DA_CSI0_LNRD_HSRX_SYNC_INIT**
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO			RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0			0	0

Bit(s)	Name	Description
28	AD_CSI0_LNRD3_HSRX_OFFSET_OUT	
27	DA_CSI0_LNRD3_HSRX_EN	
26	AD_CSI0_LNRD3_LPRX_DN	
25	AD_CSI0_LNRD3_LPRX_DP	

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Bit(s)	Name	Description
24	DA_CSI0_LNRD3_LPRX_EN	
23	AD_CSI0_LNRD2_HSRX_OFFSET_OUT	
22	DA_CSI0_LNRD2_HSRX_EN	
21	AD_CSI0_LNRD2_LPRX_DN	
20	AD_CSI0_LNRD2_LPRX_DP	
19	DA_CSI0_LNRD2_LPRX_EN	
18	AD_CSI0_LNRD1_HSRX_OFFSET_OUT	
17	DA_CSI0_LNRD1_HSRX_EN	
16	AD_CSI0_LNRD1_LPRX_DN	
15	AD_CSI0_LNRD1_LPRX_DP	
14	DA_CSI0_LNRD1_LPRX_EN	
13	AD_CSI0_LNRD0_HSRX_OFFSET_OUT	
12	DA_CSI0_LNRD0_HSRX_EN	
11	AD_CSI0_LNRD0_LPRX_DN	
10	AD_CSI0_LNRD0_LPRX_DP	
9	DA_CSI0_LNRD0_LPRX_EN	
8	AD_CSI0_LNRC_HSRX_OFFSET_OUT	
7	DA_CSI0_LNRC_HSRX_EN	
6	AD_CSI0_LNRC_LPRX_DN	
5	AD_CSI0_LNRC_LPRX_DP	
4	DA_CSI0_LNRC_LPRX_EN	
1	AD_CSI0_LNRD_HSDET	
0	DA_CSI0_LNRD_HSRX_SYNC_INIT	

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10215844 **MIPI_RX_ANA44_CSI0** **MIPI RX Monitor Mux** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													MIPI_RX_MON_MUX			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	MIPI_RX_MON_MUX	

1021584C **MIPI_RX_ANA4C_CSI0** **GPI** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_MIPI_GPI4_RDSEL		RG_MIPI_GPI4_PD	RG_MIPI_GPI4_PU	RG_MIPI_GPI4_SMT	RG_MIPI_GPI4_IES	RG_MIPI_GPI3_RDSEL		RG_MIPI_GPI3_PD	RG_MIPI_GPI3_PU	RG_MIPI_GPI3_SMT	RG_MIPI_GPI3_IES	RG_MIPI_GPI2_RDSEL	
Type			RW		RW	RW	RW	RW	RW		RW	RW	RW	RW	RW	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_MIPI_GPI2_PD	RG_MIPI_GPI2_PU	RG_MIPI_GPI2_SMT	RG_MIPI_GPI2_IES	RG_MIPI_GPI1_RDSEL		RG_MIPI_GPI1_PD	RG_MIPI_GPI1_PU	RG_MIPI_GPI1_SMT	RG_MIPI_GPI1_IES	RG_MIPI_GPI0_RDSEL		RG_MIPI_GPI0_PD	RG_MIPI_GPI0_PU	RG_MIPI_GPI0_SMT	RG_MIPI_GPI0_IES
Type	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW		RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:28	RG_MIPI_GPI4_RDSEL	**Selects RX duty** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) This register is programmable. Default settings: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
27	RG_MIPI_GPI4_PD	**Controls 75K pull-down resistor** High activated.
26	RG_MIPI_GPI4_PU	**Controls 75K pull-up resistor** High activated.
25	RG_MIPI_GPI4_SMT	**Enables RX input buffer Schmitt trigger hysteresis control** High asserted. When SMT=1, Schmitt trigger will be enabled.
24	RG_MIPI_GPI4_IES	**Enables RX input buffer** High asserted. Datapath: From IO to O. IES=0, O=0. For Vio turn-off applications, IES=0 prevents leakage in VDDIO power domain.
23:22	RG_MIPI_GPI3_R	**Selects RX duty**

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Bit(s)	Name	Description
	DSEL	RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) This register is programmable. Default settings: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
21	RG_MIPI_GPI3_PD	**Controls 75K pull-down resistor** High activated.
20	RG_MIPI_GPI3_PU	**Controls 75K pull-up resistor** High activated.
19	RG_MIPI_GPI3_SMT	**Enables RX input buffer Schmitt trigger hysteresis control** High asserted. When SMT=1, Schmitt trigger will be enabled.
18	RG_MIPI_GPI3_IES	**Enables RX input buffer** High asserted. Datapath: from IO to O. IES=0, O=0. For Vio turn-off applications, IES=0 prevents leakage in VDDIO power domain.
17:16	RG_MIPI_GPI2_RDSEL	**Selects RX duty** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) This register is programmable. Default settings: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
15	RG_MIPI_GPI2_PD	**Controls 75K pull-down resistor** High activated.
14	RG_MIPI_GPI2_PU	**Controls 75K pull-up resistor** High activated.
13	RG_MIPI_GPI2_SMT	**Enables RX input buffer Schmitt trigger hysteresis control** High asserted. When SMT=1, Schmitt trigger will be enabled.
12	RG_MIPI_GPI2_IES	**Enables RX input buffer** High asserted. Datapath: from IO to O. IES=0, O=0 For Vio turn-off applications, IES=0 prevents leakage in VDDIO power domain.
11:10	RG_MIPI_GPI1_RDSEL	**Selects RX duty** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) This register is programmable. Default settings: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
9	RG_MIPI_GPI1_PD	**Controls 75K pull-down resistor** High activated.
8	RG_MIPI_GPI1_PU	**Controls 75K pull-up resistor** High activated.
7	RG_MIPI_GPI1_SMT	**Enables RX input buffer Schmitt trigger hysteresis control** High asserted. When SMT=1, Schmitt trigger will be enabled.
6	RG_MIPI_GPI1_IES	**Enables RX input buffer** High asserted. Datapath: From IO to O. IES=0, O=0. For Vio turn-off applications, IES=0 prevents leakage in VDDIO power domain.

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Bit(s)	Name	Description
5:4	RG_MIPI_GPI0_RDSEL	**Selects RX duty** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) This register is programmable. Default settings: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
3	RG_MIPI_GPI0_PD	**Controls 75K pull-down resistor** High activated.
2	RG_MIPI_GPI0_PU	**Controls 75K pull-up resistor** High activated.
1	RG_MIPI_GPI0_SMT	**Enables RX input buffer Schmitt trigger hysteresis control** High asserted. When SMT=1, Schmitt trigger will be enabled.
0	RG_MIPI_GPI0_IES	**Enables RX input buffer** High asserted. Datapath: From IO to O. IES=0, O=0. For Vio turn-off applications, IES=0 prevents leakage in VDDIO power domain.

10215850 **MIPI_RX_ANA50_CSI0** **GPI** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_MIPI_GPI9_RDSEL		RG_MIPI_GPI9_PD	RG_MIPI_GPI9_PU	RG_MIPI_GPI9_SMT	RG_MIPI_GPI9_IES	RG_MIPI_GPI8_RDSEL		RG_MIPI_GPI8_PD	RG_MIPI_GPI8_PU	RG_MIPI_GPI8_SMT	RG_MIPI_GPI8_IES	RG_MIPI_GPI7_RDSEL	
Type			RW		RW	RW	RW	RW	RW		RW	RW	RW	RW	RW	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RG_MIPI_GPI7_PD	RG_MIPI_GPI7_PU	RG_MIPI_GPI7_SMT	RG_MIPI_GPI7_IES	RG_MIPI_GPI6_RDSEL		RG_MIPI_GPI6_PD	RG_MIPI_GPI6_PU	RG_MIPI_GPI6_SMT	RG_MIPI_GPI6_IES	RG_MIPI_GPI5_RDSEL		RG_MIPI_GPI5_PD	RG_MIPI_GPI5_PU	RG_MIPI_GPI5_SMT	RG_MIPI_GPI5_IES
Type	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW		RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:28	RG_MIPI_GPI9_RDSEL	**Selects RX duty** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) This register is programmable. Default settings: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
27	RG_MIPI_GPI9_PD	**Controls 75K pull-down resistor** High activated.
26	RG_MIPI_GPI9_PU	**Controls 75K pull-up resistor** High activated.
25	RG_MIPI_GPI9_SMT	**Enables RX input buffer Schmitt trigger hysteresis control** High asserted. When SMT=1, Schmitt trigger will be enabled.

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Bit(s)	Name	Description
24	RG_MIPI_GPI9_IES	**Enables RX input buffer** High asserted. Datapath: From IO to O. IES=0, O=0. For Vio turn-off applications, IES=0 prevents leakage in VDDIO power domain.
23:22	RG_MIPI_GPI8_RDSEL	**Selects RX duty** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) This register is programmable. Default settings: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
21	RG_MIPI_GPI8_PD	**Controls 75K pull-down resistor** High activated.
20	RG_MIPI_GPI8_PU	**Controls 75K pull-up resistor** High activated.
19	RG_MIPI_GPI8_SMT	**Enables RX input buffer Schmitt trigger hysteresis control** High asserted. When SMT=1, Schmitt trigger will be enabled.
18	RG_MIPI_GPI8_IES	**Enables RX input buffer** High asserted. Datapath: From IO to O. IES=0, O=0. For Vio turn-off applications, IES=0 prevents leakage in VDDIO power domain.
17:16	RG_MIPI_GPI7_RDSEL	**Selects RX duty** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) This register is programmable. Default settings: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
15	RG_MIPI_GPI7_PD	**Controls 75K pull-down resistor** High activated.
14	RG_MIPI_GPI7_PU	**Controls 75K pull-up resistor** High activated.
13	RG_MIPI_GPI7_SMT	**Enables RX input buffer Schmitt trigger hysteresis control** High asserted. When SMT=1, Schmitt trigger will be enabled.
12	RG_MIPI_GPI7_IES	**Enables RX input buffer** High asserted. Datapath: From IO to O. IES=0, O=0. For Vio turn-off applications, IES=0 prevents leakage in VDDIO power domain.
11:10	RG_MIPI_GPI6_RDSEL	**Selects RX duty** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) This register is programmable. Default settings: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
9	RG_MIPI_GPI6_PD	**Controls 75K pull-down resistor** High activated.
8	RG_MIPI_GPI6_PU	**Controls 75K pull-up resistor** High activated.
7	RG_MIPI_GPI6_SMT	**Enables RX input buffer Schmitt trigger hysteresis control** High asserted. When SMT=1, Schmitt trigger will be enabled.

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Bit(s)	Name	Description
6	RG_MIPI_GPI6_IES	**Enables RX input buffer** High asserted. Datapath: from IO to O. IES=0, O=0. For Vio turn-off applications, IES=0 prevents leakage in VDDIO power domain.
5:4	RG_MIPI_GPI5_RDSEL	**Selects RX duty** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) This register is programmable. Default settings: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
3	RG_MIPI_GPI5_PD	**Controls 75K pull-down resistor** High activated.
2	RG_MIPI_GPI5_PU	**Controls 75K pull-up resistor** High activated.
1	RG_MIPI_GPI5_SMT	**Enables RX input buffer schmit trigger hysteresis control** High asserted. When SMT=1, Schmitt trigger will be enabled.
0	RG_MIPI_GPI5_IES	**Enables RX input buffer** High asserted. Datapath: from IO to O. IES=0, O=0. For Vio turn-off applications, IES=0 prevents leakage in VDDIO power domain.

10215854 **MIPI_RX_ANA54_CSI0** **GPI** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															APB_ASYNC_ERR_ADDR[9:8]	
Type															RO	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	APB_ASYNC_ERR_ADDR[7:0]														APB_ASYNC_ERR	APB_ASYNC_CNT_EN
Type	RO														RO	RW
Reset	0	0	0	0	0	0	0	0							0	0

Bit(s)	Name	Description
17:8	APB_ASYNC_ERR_ADDR	**Enables RX input buffer Schmitt trigger hysteresis control** High asserted. When SMT=1, Schmitt trigger will be enabled.
1	APB_ASYNC_ERR	**Enables RX input buffer Schmitt trigger hysteresis control** High asserted. When SMT=1, Schmitt trigger will be enabled.
0	APB_ASYNC_CNT_EN	**Enables RX input buffer** High asserted. Datapath: From IO to O. IES=0, O=0. For Vio turn-off applications, IES=0 prevents leakage in VDDIO power domain.

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Module name: mipi_rx_ana_csi1 Base address: (+10215C00h)

Address	Name	Width	Register Function
10215C00	MIPI_RX_ANA00_CSI1	32	MIPI RX CSI0 Clock Lane Register
10215C04	MIPI_RX_ANA04_CSI1	32	MIPI RX CSI0 Data Lane 0 Register
10215C08	MIPI_RX_ANA08_CSI1	32	MIPI RX CSI0 Data Lane 1 Register
10215C0C	MIPI_RX_ANA0C_CSI1	32	MIPI RX CSI0 Data Lane 2 Register
10215C10	MIPI_RX_ANA10_CSI1	32	MIPI RX CSI0 Data Lane 3 Register
10215C20	MIPI_RX_ANA20_CSI1	32	MIPI RX CSI Register
10215C24	MIPI_RX_ANA24_CSI1	32	MIPI RX CSI BG Register
10215C28	MIPI_RX_ANA28_CSI1	32	MIPI RX CSI BG Register
10215C30	MIPI_RX_ANA30_CSI1	32	MIPI RX ADDA Debug Register
10215C44	MIPI_RX_ANA44_CSI1	32	MIPI RX Monitor Mux
10215C4C	MIPI_RX_ANA4C_CSI1	32	GPI
10215C50	MIPI_RX_ANA50_CSI1	32	GPI
10215C54	MIPI_RX_ANA54_CSI1	32	GPI

10215C00 MIPI_RX_ANA00_CSI1 MIPI RX CSI0 Clock Lane Register 00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							RG_CSI0_LNRC_HSRX2_IMINUS	RG_CSI0_LNRC_HSRX2_IPLUS	RG_CSI0_LNRC_HSRX_DELAY_CODE				RG_CSI0_LNRC_HSRX_DELAY_EN			
Type							RW	RW	RW				RW			
Reset							0	0	0	0	0	0	0			
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RG_CSI0_LNRC_RT_CODE				RG_CSI0_LNRC_HSRX_IMINUS	RG_CSI0_LNRC_HSRX_IPLUS	RG_CSI0_LNRC_LPRX_IMINUS	RG_CSI0_LNRC_LPRX_IPLUS					RG_CSI0_LNRC_INPUT_SEL			RG_CSI0_LNRC_LDO_OUT_EN
Type	RW				RW	RW	RW	RW					RW			RW
Reset	1	0	0	0	0	0	0	0					0			0

Bit(s)	Name	Description
25	RG_CSI0_LNRC_HSRX2_IMINUS	**Adjusts CSI0 CK lane HSRX2 bias current** 1'b0: Normal 1'b1: -10%
24	RG_CSI0_LNRC_HSRX2_IPLUS	**Adjusts CSI0 CK lane HSRX2 bias current** 1'b0: Normal 1'b1: +10%
23:20	RG_CSI0_LNRC_HSRX_DELAY_CODE	**CSI0 CK lane HSRX delay line control code** 4'b0000: Minimum delay 4'b1111: Maximum delay
19	RG_CSI0_LNRC_HSRX_DELAY_EN	**Enables CSI0 CK lane HSRX delay line** 1'b0: Disable delay line for normal operation

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Bit(s)	Name	Description
		1'b1: Enable delay line
15:12	RG_CSI0_LNRC_RT_CODE	**CSI0 CK lane impedance control code** 4'b0000: Maximum impedance 4'b1111: Minimum impedance
11	RG_CSI0_LNRC_HSRX_IMINUS	**Adjusts CSI0 CK lane HSRX bias current** 1'b0: Normal 1'b1: -10%
10	RG_CSI0_LNRC_HSRX_IPLUS	**Adjusts CSI0 CK lane HSRX bias current** 1'b0: Normal 1'b1: +10%
9	RG_CSI0_LNRC_LPRX_IMINUS	**Adjusts CSI0 CK lane LPRX bias current** 1'b0: Normal 1'b1: -10%
8	RG_CSI0_LNRC_LPRX_IPLUS	**Adjusts CSI0 CK lane LPRX bias current** 1'b0: Normal 1'b1: +10%
3	RG_CSI0_LNRC_INPUT_SEL	**Selects CSI0 CK lane analog mux** 1'b0: High z 1'b1: Select this lane
0	RG_CSI0_LNRC_LDO_OUT_EN	**Enables CSI0 CK lane LDO output** 1'b0: Disable LDO output 1'b1: Enable LDO output

10215C04 **MIPI_RX_ANA04_CSI1** **MIPI RX CSI0 Data Lane 0 Register** **00008000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI0_LNRD0_HSRX2_IMINUS	RG_CSI0_LNRD0_HSRX2_IPLUS	RG_CSI0_LNRD0_HSRX_DELAY_CODE				RG_CSI0_LNRD0_HSRX_DELAY_EN	RG_CSI0_LNRD0_HSRX_BYPASS_SYNC		RG_CSI0_LNRD0_HSRX_DET_SEL	RG_CSI0_LNRD0_HSRX_FORCE_SYNC		RG_CSI0_LNRD0_HSRX_EDGE_SEL	
Type			RW	RW	RW				RW	RW		RW	RW		RW	
Reset			0	0	0	0	0	0	0	0		0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RG_CSI0_LNRD0_RT_CODE				RG_CSI0_LNRD0_HSRX_IMINUS	RG_CSI0_LNRD0_HSRX_IPLUS	RG_CSI0_LNRD0_LPRX_IMINUS	RG_CSI0_LNRD0_LPRX_IPLUS					RG_CSI0_LNRD0_INPUT_SEL			RG_CSI0_LNRD0_LDO_OUT_EN
Type	RW				RW	RW	RW	RW					RW			RW
Reset	1	0	0	0	0	0	0	0					0			0

Bit(s)	Name	Description
29	RG_CSI0_LNRD0_HSRX2_IMINUS	**Adjusts CSI0 Lane 0 HSRX bias current** 1'b0: Normal 1'b1: -10%
28	RG_CSI0_LNRD0_	**Adjusts CSI0 Lane 0 HSRX bias current**

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Bit(s)	Name	Description
	HSRX2_IPLUS	1'b0: Normal 1'b1: +10%
27:24	RG_CSI0_LNRD0_HSRX_DELAY_CODE	**CSI0 data Lane 0 HSRX delay line control code** 4'b0000: Minimum delay 4'b1111: Maximum delay
23	RG_CSI0_LNRD0_HSRX_DELAY_EN	**Enables CSI0 data Lane 0 HSRX delay line** 1'b0: Disable delay line for normal operation 1'b1: Enable delay line
22	RG_CSI0_LNRD0_HSRX_BYPASS_SYNC	**CSI0 Lane 0 bypass sync detect function** 1'b0: Use analog sync detect function 1'b1: Disable sync detect; word alignment at digital
20	RG_CSI0_LNRD0_HSRX_DET_SEL	**Selects CSI0 Lane 0 HS detect** 1'b0: Detect DIFF-N 1'b1: Detect DIFF-P
19:18	RG_CSI0_LNRD0_HSRX_FORCE_SYNC	**Selects CSI0 Lane 0 HS force sync** 2'b00: Sync with pattern B8 2'b01: Sync falling edge with the first bit 2'b10: Sync rising edge with the first bit 2'b11: Prohibited
17:16	RG_CSI0_LNRD0_HSRX_EDGE_SEL	**Selects CSI0 Lane 0 HS sync edge** 2'b00: Sync both edges 2'b01: Sync falling edge only 2'b10: Sync rising edge only 2'b11: Prohibited
15:12	RG_CSI0_LNRD0_RT_CODE	**CSI0 Lane 0 impedance control code** 4'b0000: Maximum impedance 4'b1111: Minimum impedance
11	RG_CSI0_LNRD0_HSRX_IMINUS	**Adjusts CSI0 Lane 0 HSRX bias current** 1'b0: Normal 1'b1: -10%
10	RG_CSI0_LNRD0_HSRX_IPLUS	**Adjusts CSI0 Lane 0 HSRX bias current** 1'b0: Normal 1'b1: +10%
9	RG_CSI0_LNRD0_LPRX_IMINUS	**Adjusts CSI0 Lane 0 LPRX bias current** 1'b0: Normal 1'b1: -10%
8	RG_CSI0_LNRD0_LPRX_IPLUS	**Adjusts CSI0 Lane 0 LPRX bias current** 1'b0: Normal 1'b1: +10%
3	RG_CSI0_LNRD0_INPUT_SEL	**Selects CSI0 Lane 0 analog mux** 1'b0: High z 1'b1: Select this lane
0	RG_CSI0_LNRD0_LDO_OUT_EN	**Enables CSI0 Lane 0 LDO output** 1'b0: Disable LDO output 1'b1: Enable LDO output

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10215C08	MIPI_RX_ANA08_CSI1	MIPI RX CSI0 Data Lane 1 Register	00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI0_LN	RG_CSI0_LN	RG_CSI0_LNRD1_HSRX_DELAY_CODE				RG_CSI0_LN	RG_CSI0_LN		RG_CSI0_LN	RG_CSI0_LNRD1_HSRX_FORC		RG_CSI0_LNRD1_HSRX_EDGE	

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			RD1_HSRX2_IMINUS	RD1_HSRX2_IPLUS					RD1_HSRX_DELAY_EN	RD1_HSRX_BYPASS_SYNC		RD1_HSRX_DET_SEL	E_SYNC		_SEL	
Type			RW	RW	RW				RW	RW		RW	RW		RW	
Reset			0	0	0	0	0	0	0	0		0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI0_LNRD1_RT_CODE				RG_CSI0_LNRD1_HSRX_IMINUS	RG_CSI0_LNRD1_HSRX_IPLUS	RG_CSI0_LNRD1_LPRX_IMINUS	RG_CSI0_LNRD1_LPRX_IPLUS					RG_CSI0_LNRD1_INPUT_SEL			RG_CSI0_LNRD1_LDO_OUT_EN
Type	RW				RW	RW	RW	RW					RW			RW
Reset	1	0	0	0	0	0	0	0					0			0

Bit(s)	Name	Description
29	RG_CSI0_LNRD1_HSRX2_IMINUS	**Adjusts CSI0 Lane 1 HSRX bias current** 1'b0: Normal 1'b1: -10%
28	RG_CSI0_LNRD1_HSRX2_IPLUS	**Adjusts CSI0 Lane 1 HSRX bias current** 1'b0: Normal 1'b1: +10%
27:24	RG_CSI0_LNRD1_HSRX_DELAY_CODE	**CSI0 data Lane 1 HSRX delay line control code** 4'b0000: Minimum delay 4'b1111: Maximum delay
23	RG_CSI0_LNRD1_HSRX_DELAY_EN	**Enables CSI0 data Lane 1 HSRX delay line** 1'b0: Disable delay line for normal operation 1'b1: Enable delay line
22	RG_CSI0_LNRD1_HSRX_BYPASS_SYNC	**CSI0 Lane 1 bypass sync detect function** 1'b0: Use analog sync detect function 1'b1: Disable sync detect; word alignment at digital
20	RG_CSI0_LNRD1_HSRX_DET_SEL	**Selects CSI0 Lane 1 HS detect** 1'b0: Detect DIFF-N 1'b1: Detect DIFF-P
19:18	RG_CSI0_LNRD1_HSRX_FORCE_SYNC	**Adjusts CSI0 Lane 1 HS force sync** 2'b00: Sync with pattern B8 2'b01: Sync falling edge with the first bit 2'b10: Sync rising edge with the first bit 2'b11: Prohibited
17:16	RG_CSI0_LNRD1_HSRX_EDGE_SEL	**Selects CSI0 Lane 1 HS sync edge** 2'b00: Sync both edges 2'b01: Sync falling edge only 2'b10: Sync rising edge only 2'b11: Prohibited
15:12	RG_CSI0_LNRD1_RT_CODE	**CSI0 Lane 1 impedance control code** 4'b0000: Maximum impedance 4'b1111: Minimum impedance
11	RG_CSI0_LNRD1_HSRX_IMINUS	**Adjusts CSI0 Lane 1 HSRX bias current** 1'b0: Normal 1'b1: -10%
10	RG_CSI0_LNRD1_HSRX_IPLUS	**Adjusts CSI0 Lane 1 HSRX bias current** 1'b0: Normal

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Bit(s)	Name	Description
		1'b1: +10%
9	RG_CSI0_LNRD1_LPRX_IMINUS	**Adjusts CSI0 Lane 1 LPRX bias current** 1'b0: Normal 1'b1: -10%
8	RG_CSI0_LNRD1_LPRX_IPLUS	**Adjusts CSI0 Lane 1 LPRX bias current** 1'b0: Normal 1'b1: +10%
3	RG_CSI0_LNRD1_INPUT_SEL	**Selects CSI0 Lane 1 analog mux** 1'b0: High z 1'b1: Select this lane
0	RG_CSI0_LNRD1_LDO_OUT_EN	**Enables CSI0 Lane 1 LDO output** 1'b0: Disable LDO output 1'b1: Enable LDO output

10215C0C **MIPI_RX_ANA0C_CSI1** **MIPI RX CSI0 Data Lane 2 Register** **00008000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI0_LNRD2_HSRX2_IMINUS	RG_CSI0_LNRD2_HSRX2_IPLUS	RG_CSI0_LNRD2_HSRX_DELAY_CODE				RG_CSI0_LNRD2_HSRX_DELAY_EN	RG_CSI0_LNRD2_HSRX_BYPASS_SYNC		RG_CSI0_LNRD2_HSRX_DET_SEL	RG_CSI0_LNRD2_HSRX_FORCE_SYNC		RG_CSI0_LNRD2_HSRX_EDGE_SEL	
Type			RW	RW	RW				RW	RW		RW	RW		RW	
Reset			0	0	0	0	0	0	0	0		0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI0_LNRD2_RT_CODE				RG_CSI0_LNRD2_HSRX_IMINUS	RG_CSI0_LNRD2_HSRX_IPLUS	RG_CSI0_LNRD2_LPRX_IMINUS	RG_CSI0_LNRD2_LPRX_IPLUS					RG_CSI0_LNRD2_INPUT_SEL			RG_CSI0_LNRD2_LDO_OUT_EN
Type	RW				RW	RW	RW	RW					RW			RW
Reset	1	0	0	0	0	0	0	0					0			0

Bit(s)	Name	Description
29	RG_CSI0_LNRD2_HSRX2_IMINUS	**Adjusts CSI0 Lane 2 HSRX bias current** 1'b0: Normal 1'b1: -10%
28	RG_CSI0_LNRD2_HSRX2_IPLUS	**Adjusts CSI0 Lane 2 HSRX bias current** 1'b0: Normal 1'b1: +10%
27:24	RG_CSI0_LNRD2_HSRX_DELAY_CODE	**CSI0 data Lane 2 HSRX delay line control code** 4'b0000: Minimum delay 4'b1111: Maximum delay
23	RG_CSI0_LNRD2_HSRX_DELAY_EN	**Enables CSI0 data Lane 2 HSRX delay line** 1'b0: Disable delay line for normal operation 1'b1: Enable delay line
22	RG_CSI0_LNRD2_	**CSI0 Lane 2 bypass sync detect function**

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Bit(s)	Name	Description
	HSRX_BYPASS_SYNC	1'b0: Use analog sync detect function 1'b1: Disable sync detect; word alignment at digital
20	RG_CSI0_LNRD2_HSRX_DET_SEL	**Selects CSI0 Lane 2 HS detect** 1'b0: Detect DIFF-N 1'b1: Detect DIFF-P
19:18	RG_CSI0_LNRD2_HSRX_FORCE_SYNC	**Selects CSI0 Lane 2 HS force sync** 2'b00: Sync with pattern B8 2'b01: Sync falling edge with the first bit 2'b10: Sync rising edge with the first bit 2'b11: Prohibited
17:16	RG_CSI0_LNRD2_HSRX_EDGE_SEL	**Selects CSI0 Lane 2 HS sync edge** 2'b00: Sync both edges 2'b01: Sync falling edge only 2'b10: Sync rising edge only 2'b11: Prohibited
15:12	RG_CSI0_LNRD2_RT_CODE	**CSI0 Lane2 impedance control code** 4'b0000: Maximum impedance 4'b1111: Minimum impedance
11	RG_CSI0_LNRD2_HSRX_IMINUS	**Adjusts CSI0 Lane 2 HSRX bias current** 1'b0: Normal 1'b1: -10%
10	RG_CSI0_LNRD2_HSRX_IPLUS	**Adjusts CSI0 Lane 2 HSRX bias current** 1'b0: Normal 1'b1: +10%
9	RG_CSI0_LNRD2_LPRX_IMINUS	**Adjusts CSI0 Lane 2 LPRX bias current** 1'b0: Normal 1'b1: -10%
8	RG_CSI0_LNRD2_LPRX_IPLUS	**Adjusts CSI0 Lane 2 LPRX bias current** 1'b0: Normal 1'b1: +10%
3	RG_CSI0_LNRD2_INPUT_SEL	**Selects CSI0 Lane 2 analog mux** 1'b0: High z 1'b1: Select this lane
0	RG_CSI0_LNRD2_LDO_OUT_EN	**Enables CSI0 Lane 2 LDO output** 1'b0: Disable LDO output 1'b1: Enable LDO output

10215C10 **MIPI_RX_ANA10_CSI1** **MIPI RX CSI0 Data Lane 3 Register** **00008000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI0_LNRD3_HSRX2_IMINUS	RG_CSI0_LNRD3_HSRX2_IPLUS	RG_CSI0_LNRD3_HSRX_DELAY_CODE				RG_CSI0_LNRD3_HSRX_DELAY_EN	RG_CSI0_LNRD3_HSRX_BYPASS_SYNC		RG_CSI0_LNRD3_HSRX_DET_SEL	RG_CSI0_LNRD3_HSRX_FORCE_SYNC		RG_CSI0_LNRD3_HSRX_EDGE_SEL	
Type			RW	RW	RW				RW	RW		RW	RW		RW	
Reset			0	0	0	0	0	0	0	0		0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI0_LNRD3_RT_				RG_	RG_	RG_	RG_					RG_			RG_

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	CODE				CSI0_LNRD3_HSRX_IMINUS	CSI0_LNRD3_HSRX_IPLUS	CSI0_LNRD3_LPRX_IMINUS	CSI0_LNRD3_LPRX_IPLUS					CSI0_LNRD3_INPUT_SEL			CSI0_LNRD3_LDO_OUT_EN
Type	RW				RW	RW	RW	RW					RW			RW
Reset	1	0	0	0	0	0	0	0					0			0

Bit(s)	Name	Description
29	RG_CSI0_LNRD3_HSRX2_IMINUS	**Adjusts CSI0 Lane 3 HSRX bias current** 1'b0: Normal 1'b1: -10%
28	RG_CSI0_LNRD3_HSRX2_IPLUS	**Adjusts CSI0 Lane 3 HSRX bias current** 1'b0: Normal 1'b1: +10%
27:24	RG_CSI0_LNRD3_HSRX_DELAY_CODE	**CSI0 data Lane 3 HSRX delay line control code** 4'b0000: Minimum delay 4'b1111: Maximum delay
23	RG_CSI0_LNRD3_HSRX_DELAY_EN	**Enables CSI0 data Lane 3 HSRX delay line** 1'b0: Disable delay line for normal operation 1'b1: Enable delay line
22	RG_CSI0_LNRD3_HSRX_BYPASS_SYNC	**CSI0 Lane 3 bypass sync detect function** 1'b0: Use analog sync detect function 1'b1: Disable sync detect; word alignment at digital
20	RG_CSI0_LNRD3_HSRX_DET_SEL	**Selects CSI0 Lane 3 HS detect** 1'b0: Detect DIFF-N 1'b1: Detect DIFF-P
19:18	RG_CSI0_LNRD3_HSRX_FORCE_SYNC	**Selects CSI0 Lane 3 HS force sync** 2'b00: Sync with pattern B8 2'b01: Sync falling edge with the first bit 2'b10: Sync rising edge with the first bit 2'b11: Prohibited
17:16	RG_CSI0_LNRD3_HSRX_EDGE_SEL	**Selects CSI0 Lane 3 HS sync edge** 2'b00: Sync both edges 2'b01: Sync falling edge only 2'b10: Sync rising edge only 2'b11: Prohibited
15:12	RG_CSI0_LNRD3_RT_CODE	**CSI0 Lane 3 impedance control code** 4'b0000: Maximum impedance 4'b1111: Minimum impedance
11	RG_CSI0_LNRD3_HSRX_IMINUS	**Adjusts CSI0 Lane 3 HSRX bias current** 1'b0: Normal 1'b1: -10%
10	RG_CSI0_LNRD3_HSRX_IPLUS	**Adjusts CSI0 Lane 3 HSRX bias current** 1'b0: Normal 1'b1: +10%
9	RG_CSI0_LNRD3_LPRX_IMINUS	**Adjusts CSI0 Lane 3 LPRX bias current** 1'b0: Normal 1'b1: -10%
8	RG_CSI0_LNRD3_LPRX_IPLUS	**Adjusts CSI0 Lane 3 LPRX bias current** 1'b0: Normal 1'b1: +10%
3	RG_CSI0_LNRD3_INPUT_SEL	**Selects CSI0 Lane 3 analog mux** 1'b0: High z

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Bit(s)	Name	Description
		1'b1: Select this lane
0	RG_CSI0_LNRD3_LDO_OUT_EN	**Enables CSI0 Lane 3 LDO output** 1'b0: Disable LDO output 1'b1: Enable LDO output

10215C20 **MIPI_RX_ANA20_CSI1** **MIPI RX CSI Register** **FF000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI0_SPARE															
Type	RW															
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					RG_CSI0_PRESERVE					RG_CSI0_4XCLK_DISABLE	RG_CSI0_4XCLK_INVERT	RG_CSI0_HSDET_GATING_EN	RG_CSI0_BCLK_SEL		RG_CSI0_LNRD_HSRX_BCLK_INVERT	RG_CSI0_LDO_CORE_EN
Type					RW					RW	RW	RW	RW		RW	RW
Reset					0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	RG_CSI0_SPARE	**CSI0 spare register**
11:8	RG_CSI0_PRESERVE	**CSI0 preserved register**
6	RG_CSI0_4XCLK_DISABLE	**Disable CSI0 4X clock** 1'b0: Output 4XCLK when sync_detect is enabled. 1'b1: Gate 4XCLK when sync_detect is disabled.
5	RG_CSI0_4XCLK_INVERT	**Enables CSI0 4X clock inversion** 1'b0: Does not invert 1'b1: Invert
4	RG_CSI0_HSDET_GATING_EN	**Enables CSI0 HSDET gating** 1'b0: Disable gating. HSDET may toggle in LP-mode. 1'b1: HSDET active with HSRX_EN
3:2	RG_CSI0_BCLK_SEL	**Selects CSI0 byte clock source** Also used for CSI0 HSDET source selection. 2'b00: From Lane 0 2'b01: From Lane 1 2'b10: From Lane 2 2'b11: From Lane 3
1	RG_CSI0_LNRD_HSRX_BCLK_INVERT	**Inverts CSI0 HSRX byteclk** 1'b0: Falling edge align with data/sync 1'b1: Rising edge align with data/sync
0	RG_CSI0_LDO_CORE_EN	**Enables CSI0 LDO core bias** 1'b0: Disable 1'b1: Enable

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10215C24 **MIPI_RX_ANA24_CSI1** **MIPI RX CSI BG Register** **24248800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI0_V04_SEL			RG_CSI0_V072_SEL					RG_CSI0_V10_SEL			RG_CSI0_V12_SEL		
Type			RW			RW					RW			RW		
Reset			1	0	0	1	0	0			1	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI0_BG_R2_TRIM				RG_CSI0_BG_R1_TRIM							RG_CSI0_BG_FAST_CHARGE	RG_CSI0_BG_DIV		RG_CSI0_BG_CKEN	RG_CSI0_BG_CORE_EN
Type	RW				RW							RW	RW		RW	RW
Reset	1	0	0	0	1	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
29:27	RG_CSI0_V04_SEL	**Selects CSI0 0.4V output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage
26:24	RG_CSI0_V072_SEL	**Selects CSI0 0.72V output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage
21:19	RG_CSI0_V10_SEL	**Selects CSI0 AVDD10 output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage
18:16	RG_CSI0_V12_SEL	**Selects CSI0 1.2V output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage
15:12	RG_CSI0_BG_R2_TRIM	**Trims CSI BGR R2** ORed with RG_DSI_BG_R2_TRIM[3:0]. 4'b0000: Maximum resistance 4'b1000: Typical resistance 4'b1111: Minimum resistance
11:8	RG_CSI0_BG_R1_TRIM	**Trims CSI BGR R1** ORed with RG_DSI_BG_R1_TRIM[3:0]. 4'b0000: Maximum resistance 4'b1000: Typical resistance 4'b1111: Minimum resistance
4	RG_CSI0_BG_FAST_CHARGE	**Enables BG bias low-pass filter fast charge** ORed with RG_DSI_BG_FAST_CHARGE. 1'b0: Disable. Settling time is 30us. 1'b1: Enable. Settling time is 1us.
3:2	RG_CSI0_BG_DIV	**BG chopper clock divisor control** ORed with RG_DSI_BG_DIV[1:0] 2'b00: /2 2'b01: /4 2'b10: /8 2'b11: /16
1	RG_CSI0_BG_CKEN	**Enables BG chopper clock** ORed with RG_DSI_BG_CKEN 1'b0: Disable

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Bit(s)	Name	Description
		1'b1: Enable
0	RG_CSI0_BG_CORE_EN	**Enables CSI BG** ORed with RG_DSI_BG_CORE_EN 1'b0: Power off 1'b1: Enable

10215C28 **MIPI_RX_ANA28_CSI1** **MIPI RX CSI BG Register** **00000024**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name											RG_CSI0_V02_SEL			RG_CSI0_V032_SEL		
Type											RW			RW		
Reset											1	0	0	1	0	0

Bit(s)	Name	Description
5:3	RG_CSI0_V02_SEL	**Selects CSI0 0.2V output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage
2:0	RG_CSI0_V032_SEL	**Selects CSI0 0.32V output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage

10215C30 **MIPI_RX_ANA30_CSI1** **MIPI RX ADDA Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AD_CSI0_LNRD3_HSRX_OFFSET_OUT	DA_CSI0_LNRD3_HSRX_EN	AD_CSI0_LNRD3_LPRX_DN	AD_CSI0_LNRD3_LPRX_DP	DA_CSI0_LNRD3_LPRX_EN	AD_CSI0_LNRD2_HSRX_OFFSET_OUT	DA_CSI0_LNRD2_HSRX_EN	AD_CSI0_LNRD2_LPRX_DN	AD_CSI0_LNRD2_LPRX_DP	DA_CSI0_LNRD2_LPRX_EN	AD_CSI0_LNRD1_HSRX_OFFSET_OUT	DA_CSI0_LNRD1_HSRX_EN	AD_CSI0_LNRD1_LPRX_DN
Type				RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	AD_CSI0_LNRD1_LPRX_DP	DA_CSI0_LNRD1_LPRX_EN	AD_CSI0_LNRD0_HSRX_OFFSET_OUT	DA_CSI0_LNRD0_HSRX_EN	AD_CSI0_LNRD0_LPRX_DN	AD_CSI0_LNRD0_LPRX_DP	DA_CSI0_LNRD0_LPRX_EN	AD_CSI0_LNRC_HSRX_OFFSET_OUT	DA_CSI0_LNRC_HSRX_EN	AD_CSI0_LNRC_LPRX_DN	AD_CSI0_LNRC_LPRX_DP	DA_CSI0_LNRC_LPRX_EN			AD_CSI0_LNRD_HSDET	DA_CSI0_LNRD_HSRX_SYNC_INIT
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO			RO	RO

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Reset	0	0	0	0	0	0	0	0	0	0	0	0			0	0

Bit(s)	Name	Description
28	AD_CSI0_LNRD3_HSRX_OFFSET_OUT	
27	DA_CSI0_LNRD3_HSRX_EN	
26	AD_CSI0_LNRD3_LPRX_DN	
25	AD_CSI0_LNRD3_LPRX_DP	
24	DA_CSI0_LNRD3_LPRX_EN	
23	AD_CSI0_LNRD2_HSRX_OFFSET_OUT	
22	DA_CSI0_LNRD2_HSRX_EN	
21	AD_CSI0_LNRD2_LPRX_DN	
20	AD_CSI0_LNRD2_LPRX_DP	
19	DA_CSI0_LNRD2_LPRX_EN	
18	AD_CSI0_LNRD1_HSRX_OFFSET_OUT	
17	DA_CSI0_LNRD1_HSRX_EN	
16	AD_CSI0_LNRD1_LPRX_DN	
15	AD_CSI0_LNRD1_LPRX_DP	
14	DA_CSI0_LNRD1_LPRX_EN	
13	AD_CSI0_LNRD0_HSRX_OFFSET_OUT	
12	DA_CSI0_LNRD0_HSRX_EN	
11	AD_CSI0_LNRD0_LPRX_DN	
10	AD_CSI0_LNRD0_LPRX_DP	
9	DA_CSI0_LNRD0_LPRX_EN	
8	AD_CSI0_LNRC_HSRX_OFFSET_OUT	
7	DA_CSI0_LNRC_HSRX_EN	
6	AD_CSI0_LNRC_LPRX_DN	
5	AD_CSI0_LNRC_L	

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Bit(s)	Name	Description
	PRX_DP	
4	DA_CSI0_LNRC_LPRX_EN	
1	AD_CSI0_LNRD_HSDET	
0	DA_CSI0_LNRD_HSRX_SYNC_INIT	

10215C44 **MIPI_RX_ANA44_CSI1** **MIPI RX Monitor Mux** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													MIPI_RX_MON_MUX			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	MIPI_RX_MON_MUX	

10215C4C **MIPI_RX_ANA4C_CSI1** **GPI** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_MIPI_GPI4_RDSEL		RG_MIPI_GPI4_PD	RG_MIPI_GPI4_PU	RG_MIPI_GPI4_SMT	RG_MIPI_GPI4_IES	RG_MIPI_GPI3_RDSEL		RG_MIPI_GPI3_PD	RG_MIPI_GPI3_PU	RG_MIPI_GPI3_SMT	RG_MIPI_GPI3_IES	RG_MIPI_GPI2_RDSEL	
Type			RW		RW	RW	RW	RW	RW		RW	RW	RW	RW	RW	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_MIPI_GPI2_PD	RG_MIPI_GPI2_PU	RG_MIPI_GPI2_SMT	RG_MIPI_GPI2_IES	RG_MIPI_GPI1_RDSEL		RG_MIPI_GPI1_PD	RG_MIPI_GPI1_PU	RG_MIPI_GPI1_SMT	RG_MIPI_GPI1_IES	RG_MIPI_GPI0_RDSEL		RG_MIPI_GPI0_PD	RG_MIPI_GPI0_PU	RG_MIPI_GPI0_SMT	RG_MIPI_GPI0_IES
Type	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW		RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:28	RG_MIPI_GPI4_RDSEL	**Selects RX duty** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) This register is programmable. Default settings: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
27	RG_MIPI_GPI4_P	**Controls 75K pull-down resistor**

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Bit(s)	Name	Description
	D	High activate.
26	RG_MIPI_GPI4_PU	**Controls 75K pull-up resistor** High activate.
25	RG_MIPI_GPI4_SMT	**Enables RX input buffer Schmitt trigger hysteresis control** High asserted. When SMT=1, Schmitt trigger will be enabled.
24	RG_MIPI_GPI4_IES	**Enables RX input buffer** High asserted. Datapath: From IO to O. IES=0, O=0. For Vio turn-off applications, IES=0 prevents leakage in VDDIO power domain.
23:22	RG_MIPI_GPI3_RDSEL	**Selects RX duty** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) This register is programmable. Default settings: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
21	RG_MIPI_GPI3_PD	**Controls 75K pull-down resistor** High activate.
20	RG_MIPI_GPI3_PU	**Controls 75K pull-up resistor** High activate.
19	RG_MIPI_GPI3_SMT	**Enables RX input buffer Schmitt trigger hysteresis control** High asserted. When SMT=1, Schmitt trigger will be enabled.
18	RG_MIPI_GPI3_IES	**Enables RX input buffer** High asserted. Datapath: from IO to O. IES=0, O=0. For Vio turn-off applications, IES=0 prevents leakage in VDDIO power domain.
17:16	RG_MIPI_GPI2_RDSEL	**Selects RX duty** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) This register is programmable. Default settings: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
15	RG_MIPI_GPI2_PD	**Controls 75K pull-down resistor** High activate.
14	RG_MIPI_GPI2_PU	**Controls 75K pull-up resistor** High activate.
13	RG_MIPI_GPI2_SMT	**Enables RX input buffer Schmitt trigger hysteresis control** High asserted. When SMT=1, Schmitt trigger will be enabled.
12	RG_MIPI_GPI2_IES	**Enables X input buffer** High asserted. Datapath: from IO to O. IES=0, O=0 For Vio turn-off applications, IES=0 prevents leakage in VDDIO power domain.
11:10	RG_MIPI_GPI1_RDSEL	**Selects RX duty** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) This register is programmable. Default settings: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]

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Bit(s)	Name	Description
9	RG_MIPI_GPI1_PD	**Controls 75K pull-down resistor** High activate.
8	RG_MIPI_GPI1_PU	**Controls 75K pull-up resistor** High activate.
7	RG_MIPI_GPI1_SMT	**Enables RX input buffer Schmitt trigger hysteresis control** High asserted. When SMT=1, Schmitt trigger will be enabled.
6	RG_MIPI_GPI1_IES	**Enables RX input buffer** High asserted. Datapath: From IO to O. IES=0, O=0. For Vio turn-off applications, IES=0 prevents leakage in VDDIO power domain.
5:4	RG_MIPI_GPI0_RDSEL	**Selects RX duty** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) This register is programmable. Default settings: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
3	RG_MIPI_GPI0_PD	**Controls 75K pull-down resistor** High activate.
2	RG_MIPI_GPI0_PU	**Controls 75K pull-up resistor** High activate.
1	RG_MIPI_GPI0_SMT	**Enables RX input buffer Schmitt trigger hysteresis control** High asserted. When SMT=1, Schmitt trigger will be enabled.
0	RG_MIPI_GPI0_IES	**Enables RX input buffer** High asserted. Datapath: From IO to O. IES=0, O=0. For Vio turn-off applications, IES=0 prevents leakage in VDDIO power domain.

10215C50 **MIPI_RX_ANA50_CSI1** **GPI** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			**RG_MIPI_GPI9_RDSEL**		**RG_MIPI_GPI9_PD**	**RG_MIPI_GPI9_PU**	**RG_MIPI_GPI9_SMT**	**RG_MIPI_GPI9_IES**	**RG_MIPI_GPI8_RDSEL**		**RG_MIPI_GPI8_PD**	**RG_MIPI_GPI8_PU**	**RG_MIPI_GPI8_SMT**	**RG_MIPI_GPI8_IES**	**RG_MIPI_GPI7_RDSEL**	
Type			RW		RW	RW	RW	RW	RW		RW	RW	RW	RW	RW	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_MIPI_GPI7_PD**	**RG_MIPI_GPI7_PU**	**RG_MIPI_GPI7_SMT**	**RG_MIPI_GPI7_IES**	**RG_MIPI_GPI6_RDSEL**		**RG_MIPI_GPI6_PD**	**RG_MIPI_GPI6_PU**	**RG_MIPI_GPI6_SMT**	**RG_MIPI_GPI6_IES**	**RG_MIPI_GPI5_RDSEL**		**RG_MIPI_GPI5_PD**	**RG_MIPI_GPI5_PU**	**RG_MIPI_GPI5_SMT**	**RG_MIPI_GPI5_IES**
Type	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW		RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:28	RG_MIPI_GPI9_RDSEL	**Selects RX duty** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment)

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Bit(s)	Name	Description
		This register is programmable. Default settings: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
27	RG_MIPI_GPI9_PD	**Controls 75K pull-down resistor** High activate.
26	RG_MIPI_GPI9_PU	**Controls 75K pull-up resistor** High activite.
25	RG_MIPI_GPI9_SMT	**Enables RX input buffer Schmitt trigger hysteresis control** High asserted. When SMT=1, Schmitt trigger will be enabled.
24	RG_MIPI_GPI9_IES	**Enables RX input buffer** High asserted. Datapath: From IO to O. IES=0, O=0. For Vio turn-off applications, IES=0 prevents leakage in VDDIO power domain.
23:22	RG_MIPI_GPI8_RDSEL	**Selects RX duty** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) This register is programmable. Default settings: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
21	RG_MIPI_GPI8_PD	**Controls 75K pull-down resistor** High activate.
20	RG_MIPI_GPI8_PU	**Controls 75K pull-up resistor** High activate.
19	RG_MIPI_GPI8_SMT	**Enables RX input buffer Schmitt trigger hysteresis control** High asserted. When SMT=1, Schmitt trigger will be enabled.
18	RG_MIPI_GPI8_IES	**Enables RX input buffer** High asserted. Datapath: From IO to O. IES=0, O=0. For Vio turn-off applications, IES=0 prevents leakage in VDDIO power domain.
17:16	RG_MIPI_GPI7_RDSEL	**Selects RX duty** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) This register is programmable. Default settings: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
15	RG_MIPI_GPI7_PD	**Controls 75K pull-down resistor** High activate.
14	RG_MIPI_GPI7_PU	**Controls 75K pull-up resistor** High activate.
13	RG_MIPI_GPI7_SMT	**Enables RX input buffer Schmitt trigger hysteresis control** High asserted. When SMT=1, Schmitt trigger will be enabled.
12	RG_MIPI_GPI7_IES	**Enables RX input buffer** High asserted. Datapath: From IO to O. IES=0, O=0. For Vio turn-off applications, IES=0 prevents leakage in VDDIO power domain.
11:10	RG_MIPI_GPI6_RDSEL	**Selects RX duty** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment)

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Bit(s)	Name	Description
		This register is programmable. Default settings: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
9	RG_MIPI_GPI6_PD	**Controls 75K pull-down resistor** High activate.
8	RG_MIPI_GPI6_PU	**Controls 75K pull-up resistor** High activate.
7	RG_MIPI_GPI6_SMT	**Enables RX input buffer Schmitt trigger hysteresis control** High asserted. When SMT=1, Schmitt trigger will be enabled.
6	RG_MIPI_GPI6_IES	**Enables RX input buffer** High asserted. Datapath: from IO to O. IES=0, O=0. For Vio turn-off applications, IES=0 prevents leakage in VDDIO power domain.
5:4	RG_MIPI_GPI5_RDSEL	**Selects RX duty** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) This register is programmable. Default settings: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
3	RG_MIPI_GPI5_PD	**Controls 75K pull-down resistor** High activate.
2	RG_MIPI_GPI5_PU	**Controls 75K pull-up resistor** High activite.
1	RG_MIPI_GPI5_SMT	**Enables RX input buffer Schmitt trigger hysteresis control** High asserted. When SMT=1, Schmitt trigger will be enabled.
0	RG_MIPI_GPI5_IES	**Enables RX input buffer** High asserted. Datapath: from IO to O. IES=0, O=0. For Vio turn-off applications, IES=0 prevents leakage in VDDIO power domain.

10215C54 **MIPI_RX_ANA54_CSI1** **GPI** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															APB_ASYNC_ERR_ADDR[9:8]	
Type															RO	
Reset															0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	APB_ASYNC_ERR_ADDR[7:0]														APB_ASYNC_ERR	APB_ASYNC_CNT_EN
Type	RO														RO	RW
Reset	0	0	0	0	0	0	0	0							0	0

Bit(s)	Name	Description
17:8	APB_ASYNC_ERR_	**Enables RX input buffer Schmitt trigger hysteresis control**

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Bit(s)	Name	Description
	ADDR	High asserted. When SMT=1, Schmitt trigger will be enabled.
1	APB_ASYNC_ERR	**Enables RX input buffer Schmitt trigger hysteresis control** High asserted. When SMT=1, Schmitt trigger will be enabled.
0	APB_ASYNC_CNT_EN	**Enables RX input buffer** High asserted. Datapath: From IO to O. IES=0, O=0. For Vio turn-off applications, IES=0 prevents leakage in VDDIO power domain.

Module name: seninf_ccir656 Base address: (+15008EC0h)

Address	Name	Width	Register Function
15008EC0	CCIR656_CTL	32	**CCIR656_CTL** CCIR656 control
15008EC4	CCIR656_H	32	**CCIR656_H** CCIR656 horizontal valid control
15008EC8	CCIR656_PTGEN_H_1	32	**CCIR656_PTGEN_H_1** CCIR656 pattern gen horizontal control 1
15008ECC	CCIR656_PTGEN_H_2	32	**CCIR656_PTGEN_H_2** CCIR656 pattern gen horizontal control 2
15008ED0	CCIR656_PTGEN_V_1	32	**CCIR656_PTGEN_V_1** CCIR656 pattern gen vertical control 1
15008ED4	CCIR656_PTGEN_V_2	32	**CCIR656_PTGEN_V_2** CCIR656 pattern gen vertical control 2
15008ED8	CCIR656_PTGEN_CTL1	32	**CCIR656_PTGEN_CTL1** CCIR656 pattern gen control 1
15008EDC	CCIR656_PTGEN_CTL2	32	**CCIR656_PTGEN_CTL2** CCIR656 pattern gen control 2
15008EE0	CCIR656_PTGEN_CTL3	32	**CCIR656_PTGEN_CTL3** CCIR656 pattern gen control 3
15008EE4	CCIR656_STATUS	32	**CCIR656_STATUS** CCIR656 status

15008EC0 CCIR656_CTL CCIR656_CTL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					CCIR656_DBG_SEL						CCIR656_EN	CCIR656_PT_EN	CCIR656_VS_POL	CCIR656_HS_POL	CCIR656_REV_1	CCIR656_REV_0
Type					RW						RW	RW	RW	RW	RW	RW
Reset					0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
11:8	CCIR656_DBG_SEL	**Selects CCIR656 debugging port**
5	CCIR656_EN	**Enables CCIR656**

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Bit(s)	Name	Description
4	CCIR656_PT_EN	**Enables CCIR656 internal pattern gen** 0: Disable 1: Enable
3	CCIR656_VS_POL	**CCIR656 VS output polarity** 0: Active high 1: Active low
2	CCIR656_HS_POL	**CCIR656 HS output polarity** 0: Active high 1: Active low
1	CCIR656_REV_1	**CCIR656_REV_1**
0	CCIR656_REV_0	**CCIR656_REV_0**

15008EC4 CCIR656_H CCIR656_H 059A0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CCIR656_HS_END											
Type					RW											
Reset					0	1	0	1	1	0	0	1	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CCIR656_HS_START											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	1	1

Bit(s)	Name	Description
27:16	CCIR656_HS_END	CCIR656 HS end in 27MHz clock rate
11:0	CCIR656_HS_START	CCIR656 HS start in 27MHz clock rate

15008EC8 CCIR656_PTGEN_H_1 CCIR656_PTGEN_H_1 02D0035A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				CCIR656_PT_HACTIVE												
Type				RW												
Reset				0	0	0	1	0	1	1	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CCIR656_PT_HTOTAL												
Type				RW												
Reset				0	0	0	1	1	0	1	0	1	1	0	1	0

Bit(s)	Name	Description
28:16	CCIR656_PT_HACTIVE	CCIR656 pattern gen horizontal active
12:0	CCIR656_PT_HTOTAL	CCIR656 pattern gen horizontal total

15008ECC CCIR656_PTGEN_H_2 CCIR656_PTGEN_H_2 00850085

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name				CCIR656_PT_HSTART												
Type				RW												
Reset				0	0	0	0	0	1	0	0	0	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CCIR656_PT_HWIDTH												
Type				RW												
Reset				0	0	0	0	0	1	0	0	0	0	1	0	1

Bit(s)	Name	Description
28:16	CCIR656_PT_HSTART	CCIR656 pattern gen horizontal start
12:0	CCIR656_PT_HWIDTH	CCIR656 pattern gen horizontal width

15008ED0 CCIR656_PTGEN_V_1 CCIR656_PTGEN_V_1 00F00106

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CCIR656_PT_VACTIVE											
Type					RW											
Reset					0	0	0	0	1	1	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CCIR656_PT_VTOTAL											
Type					RW											
Reset					0	0	0	1	0	0	0	0	0	1	1	0

Bit(s)	Name	Description
27:16	CCIR656_PT_VACTIVE	CCIR656 pattern gen vertical active
11:0	CCIR656_PT_VTOTAL	CCIR656 pattern gen vertical total

15008ED4 CCIR656_PTGEN_V_2 CCIR656_PTGEN_V_2 00160016

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CCIR656_PT_VSTART											
Type					RW											
Reset					0	0	0	0	0	0	0	1	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CCIR656_PT_VWIDTH											
Type					RW											
Reset					0	0	0	0	0	0	0	1	0	1	1	0

Bit(s)	Name	Description
27:16	CCIR656_PT_VSTART	CCIR656 pattern gen vertical start
11:0	CCIR656_PT_VWIDTH	CCIR656 pattern gen vertical width

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15008ED8 CCIR656_PTGEN_CTL1 CCIR656_PTGEN_CTL1 001E0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CCIR656_PT_COLOR_BAR_TH											
Type					RW											
Reset					0	0	0	0	0	0	0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CCIR656_PT_TYPE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	CCIR656_PT_COLOR_BAR_TH	CCIR656 pattern gen color bar threshold
7:0	CCIR656_PT_TYPE	CCIR656 pattern gen type

15008EDC CCIR656_PTGEN_CTL2 CCIR656_PTGEN_CTL2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CCIR656_PT_CR							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CCIR656_PT_CB								CCIR656_PT_Y							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	CCIR656_PT_CR	CCIR656 pattern gen CR value
15:8	CCIR656_PT_CB	CCIR656 pattern gen CB value
7:0	CCIR656_PT_Y	CCIR656 pattern gen Y value

15008EE0 CCIR656_PTGEN_CTL3 CCIR656_PTGEN_CTL3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CCIR656_PT_BD_CR							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CCIR656_PT_BD_CB								CCIR656_PT_BD_Y							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	CCIR656_PT_BD_CR	CCIR656 pattern gen boarder CR value
15:8	CCIR656_PT_BD_CB	CCIR656 pattern gen boarder CB value
7:0	CCIR656_PT_BD_Y	CCIR656 pattern gen boarder Y value

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15008EE4 **CCIR656_STATUS** **CCIR656_STATUS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**CCIR656_IN_VS**	**CCIR656_IN_FIELD**
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	CCIR656_IN_VS	CCIR656 input VS value
0	CCIR656_IN_FIELD	CCIR656 input field value

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6.6 FDVT

6.6.1 Module Introduction

6.6.1.1 Overview

Face Detection and Visual Tracking (FDVT) Engine is used to detect new coming faces and track the existing faces in an image. It has the capability of detecting the faces of Rotation-in-Plane (RIP) from -180° to +180° and Rotation-off-Plane (ROP) from -90° to +90° (see Figure 6-5).

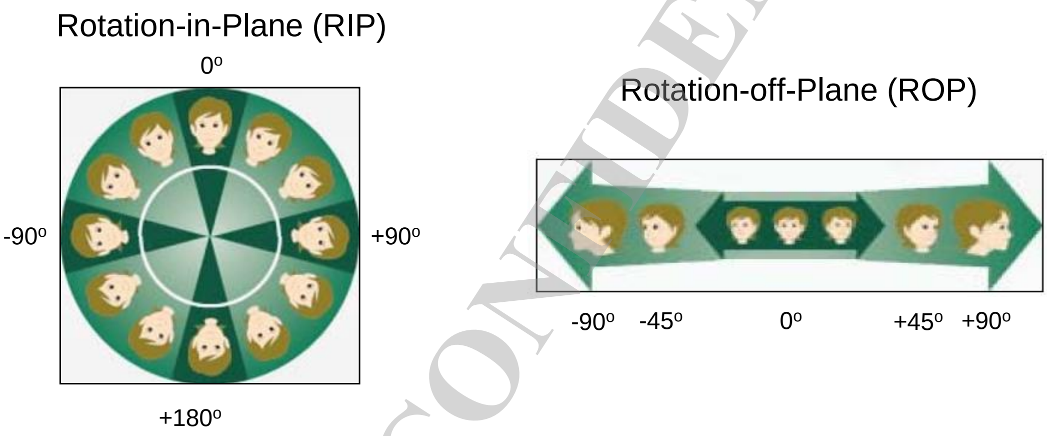

Figure 6-5. Definition of RIP and ROP

The input image of FDVT is the RGB565/YUV420/YUV422 data in the external memory, which is generated by ISP module. FDVT supports images of size up to 1022x1022 pixels. The FDVT outputs are the locations, sizes, estimated pose and confidence values of the detected faces, which are also stored in the external memory.

6.6.1.2 Theory of Operations

FDVT detects the faces in an image with the unit called Macro-window. The Macro-window scans the positions within the image. In each position, FDVT uses the predetermined features to determine if the Macro-window contains the face or not. In order to detect the large faces by using the Macro-window of the same size, FDVT rescales the original gray image into the smaller ones and does the scanning process in the re-scaled images. Figure 6-6Figure 6-6 illustrates the concept of Macro-window detection.

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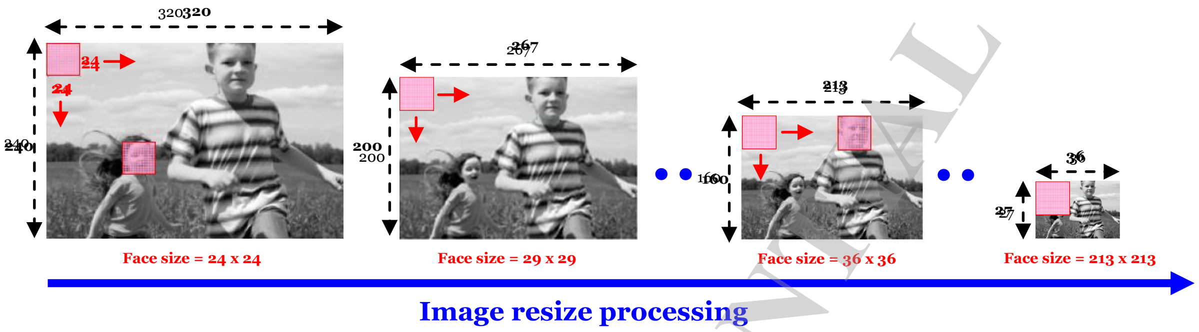

Figure 6-6. Example of face detection with 24x24 Macro-window

In the Macro-window of each position in the image, FDVT calculates the feature values and confidence values to determine if it contains the face. To increase the speed of calculating the values, FDVT uses the concept of integral image, which is generated by IIG module. If the face is detected in the Macro-window, FDVT will write the position, size, estimated pose and confidence value of the face to the external memory via DMA. Once all the re-scaled images are scanned completely, FDVT will send the interrupt signal to notify the firmware to read the face detection. Then, FDVT can prepare to do the detection in the next image. Figure 6-7Figure 6-7 shows the FDVT operation flow mentioned above. Details on the operations are described in the next section.

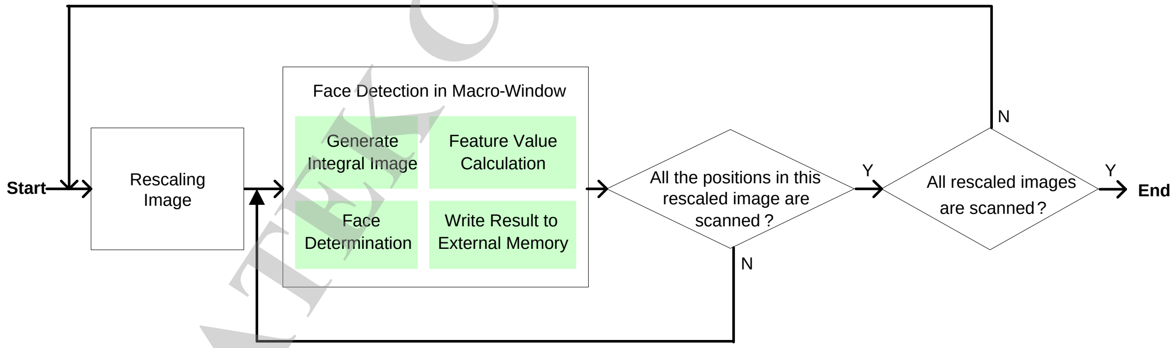

Figure 6-7. FDE operation flow

6.6.2 Software Control Flow and Register Settings

6.6.2.1 Software Control Introduction

Initially SW must initialize all registers (blue part). After that, not all the registers must be updated (only the red part needs to be updated frame by frame) (see Figure 6-8).

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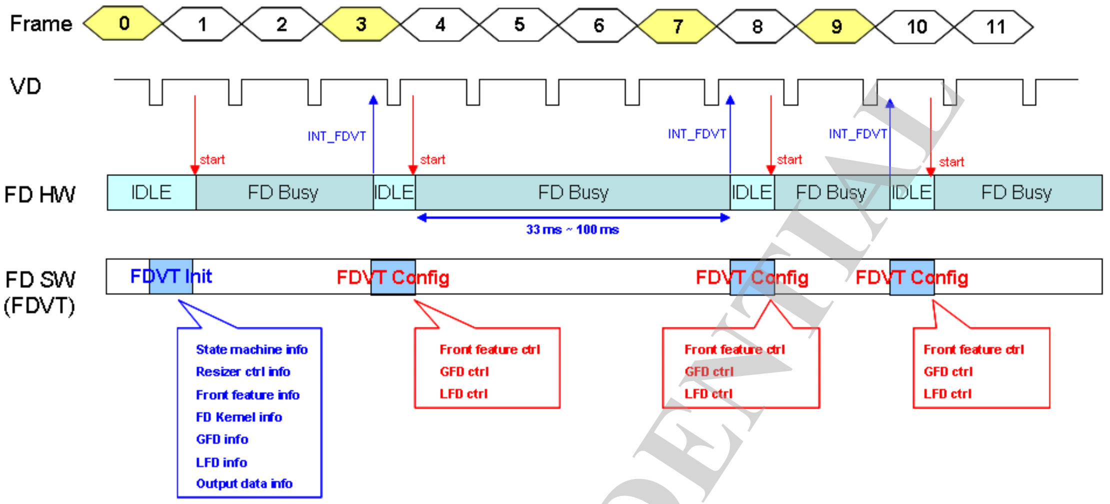

Figure 6-8. Register setting timing diagram

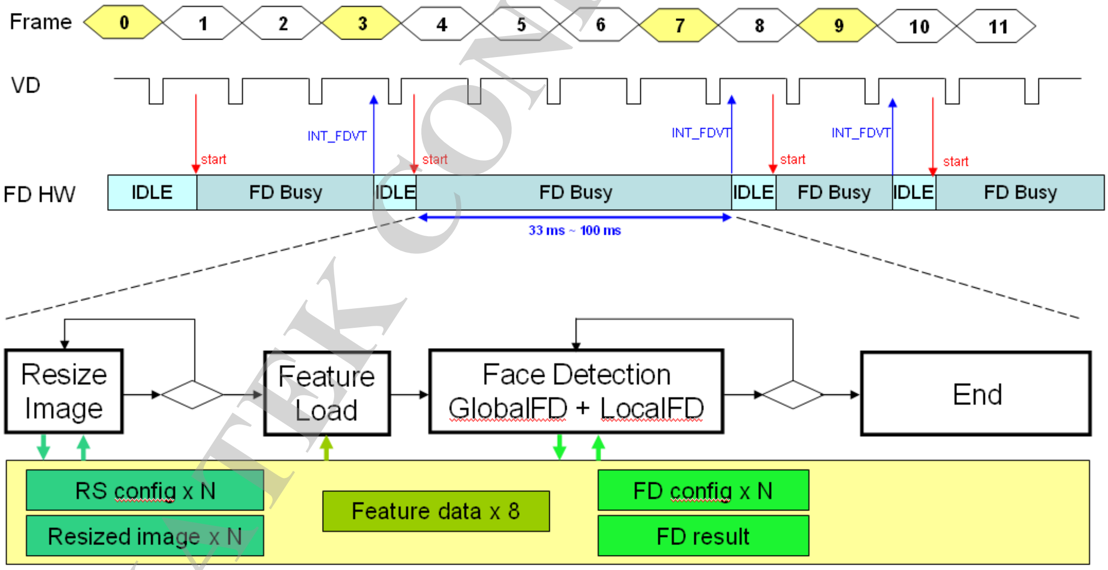

Figure 6-9. Hardware FDVT processing flow in one frame

First the resizer resizes the input image to several smaller images you need. RS_config (RS configuration) contains the resize information of each small image. If you have N small image, set up N RS_config. Hardware will read these configurations and store the corresponding smaller images to DRAM.

Next, HW loads all the front-end features from DRAM to SRAM. SW must set the front-end feature number of each data set (total 8 data sets).

The face detection part will start processing after the front-end feature load is finished. HW will load FD_config (FD configuration) to do GFD (Global Face Detection) and LFD (Local Face Detection)

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process. FD_config contains the face detection information of each small image. If you have N small image, set up N FD_config. Hardware will read these configurations to do further processing. If any face candidate is found, HW will store the face result (information) to DRAM.

Module name: FDVT Base address: (+1500B000h)

Address	Name	Width	Register Function
1500B000	FDVT_START	32	**FDVT Start** FDVT start signal.
1500B004	FDVT_ENABLE	32	**Enables Function** Enables RS/FD/FF and sub-functions.
1500B008	FDVT_RS	32	**Configuration of Resizer** Resizer setting.
1500B00C	FDVT_RSCON_BASE_ADR	32	**Memory Base Address of RS Configuration** RS configuration base address.
1500B010	FDVT_RGB2Y0	32	**Transform Coefficients of RGB2Y** RGB to Y transform coefficient parameter setting.
1500B014	FDVT_RGB2Y1	32	**Transform Coefficients of RGB2Y** RGB to Y transform coefficient parameter setting.
1500B018	FDVT_INVG0	32	**Inverse Gamma Coefficients** Piece-wise linear curve table parameter setting.
1500B01C	FDVT_INVG1	32	**Inverse Gamma Coefficients** Piece-wise linear curve table parameter setting.
1500B020	FDVT_INVG2	32	**Inverse Gamma Coefficients** Piece-wise linear curve table parameter setting.
1500B024	FDVT_FNUM_0	32	**Feature Numbers** Number of learning data.
1500B028	FDVT_FNUM_1	32	**Feature Numbers** Number of learning data.
1500B02C	FDVT_FNUM_2	32	**Feature Numbers** Number of learning data.
1500B030	FDVT_FNUM_3	32	**Feature Numbers** Number of learning data.
1500B034	FDVT_T_FNUM_0	32	**Feature Numbers in Tracking Mode** Number of learning data in tracking mode.
1500B038	FDVT_T_FNUM_1	32	**Feature Numbers in Tracking Mode** Number of learning data in tracking mode.
1500B03C	FDVT_T_FNUM_2	32	**Feature Numbers in Tracking Mode** Number of learning data in tracking mode.
1500B040	FDVT_T_FNUM_3	32	**Feature Numbers in Tracking Mode** Number of learning data in tracking mode.
1500B044	FDVT_FF_NUM_0	32	**Front-End Feature Numbers** Number of learning data placed in SRAM.
1500B048	FDVT_FF_NUM_1	32	**Front-End Feature Numbers** Number of learning data placed in SRAM.
1500B04C	FDVT_FF_NUM_2	32	**Front-End Feature Numbers** Number of learning data placed in SRAM.
1500B050	FDVT_FF_NUM_3	32	**Front-End Feature Numbers** Number of learning data placed in SRAM.
1500B054	FDVT_FF_BASE_ADR_0	32	**Memory Base Address of Learning Data** Learning data base address.
1500B058	FDVT_FF_BASE	32	**Memory Base Address of Learning Data**

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Address	Name	Width	Register Function
	_ADR_1		Learning data base address.
1500B05C	FDVT_FF_BASE_ADR_2	32	**Memory Base Address of Learning Data** Learning data base address.
1500B060	FDVT_FF_BASE_ADR_3	32	**Memory Base Address of Learning Data** Learning data base address.
1500B064	FDVT_FF_BASE_ADR_4	32	**Memory Base Address of Learning Data** Learning data base address.
1500B068	FDVT_FF_BASE_ADR_5	32	**Memory Base Address of Learning Data** Learning data base address.
1500B06C	FDVT_FF_BASE_ADR_6	32	**Memory Base Address of Learning Data** Learning data base address.
1500B070	FDVT_FF_BASE_ADR_7	32	**Memory Base Address of Learning Data** Learning data base address.
1500B074	FDVT_RMAP_0	32	**Configuration of Feature Remap** REMAP parameter setting.
1500B078	FDVT_RMAP_1	32	**Configuration of Feature Remap** REMAP parameter setting.
1500B07C	FDVT_FD	32	**Configuration of Face Detection** Detection kernel setting.
1500B080	FDVT_FD_CON_BASE_ADR	32	**Memory Base Address of FD Configuration** FD configuration base address in DRAM.
1500B084	FDVT_GFD	32	**Configuration of Global Skip Mode of Face Detection** FD setting for global skip mode.
1500B088	FDVT_LFD	32	**Configuration of Local Face Detection** LFD related setting.
1500B08C	FDVT_GFD_POS_0	32	**Region of Interest for Face Detection** GFD detection area (ROI) setting.
1500B090	FDVT_GFD_POS_1	32	**Region of Interest for Face Detection** GFD detection area (ROI) setting.
1500B094	FDVT_GFD_DET_0	32	**Pose Selection of Face Detection** Pose selection of GFD.
1500B098	FDVT_GFD_DET_1	32	**Pose Selection of Face Detection** Pose selection of GFD.
1500B09C	FDVT_FD_RLT_BASE_ADR	32	**Memory Base Address of FD Results** Base address of the face detection result in DRAM.
1500B0A4	FDVT_LFD_INFO_CTRL_0	32	**Information of Local Face Detection #00** LFD #00 face information setting.
1500B0A8	FDVT_LFD_INFO_XPOS_0	32	**Tracking Position of Local Face Detection #00** LFD #00 tracking face position.
1500B0AC	FDVT_LFD_INFO_YPOS_0	32	**Tracking Position of Local Face Detection #00** LFD #00 tracking face position.
1500B0B0	FDVT_LFD_INFO_CTRL_1	32	**Information of Local Face Detection #01** LFD #01 face information setting.
1500B0B4	FDVT_LFD_INFO_XPOS_1	32	**Tracking Position of Local Face Detection #01** LFD #01 tracking face position.
1500B0B8	FDVT_LFD_INFO_YPOS_1	32	**Tracking Position of Local Face Detection #01** LFD #01 tracking face position.
1500B0BC	FDVT_LFD_INFO_CTRL_2	32	**Information of Local Face Detection #02** LFD #02 face information setting.
1500B0C0	FDVT_LFD_INFO_XPOS_2	32	**Tracking Position of Local Face Detection #02** LFD #02 tracking face position.

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Address	Name	Width	Register Function
1500B0C4	FDVT_LFD_INFO_YPOS_2	32	**Tracking Position of Local Face Detection #02** LFD #02 tracking face position.
1500B0C8	FDVT_LFD_INFO_CTRL_3	32	**Information of Local Face Detection #03** LFD #03 face information setting.
1500B0CC	FDVT_LFD_INFO_XPOS_3	32	**Tracking Position of Local Face Detection #03** LFD #03 tracking face position.
1500B0D0	FDVT_LFD_INFO_YPOS_3	32	**Tracking Position of Local Face Detection #03** LFD #03 tracking face position.
1500B0D4	FDVT_LFD_INFO_CTRL_4	32	**Information of Local Face Detection #04** LFD #04 face information setting.
1500B0D8	FDVT_LFD_INFO_XPOS_4	32	**Tracking Position of Local Face Detection #04** LFD #04 tracking face position.
1500B0DC	FDVT_LFD_INFO_YPOS_4	32	**Tracking Position of Local Face Detection #04** LFD #04 tracking face position.
1500B0E0	FDVT_LFD_INFO_CTRL_5	32	**Information of Local Face Detection #05** LFD #05 face information setting.
1500B0E4	FDVT_LFD_INFO_XPOS_5	32	**Tracking Position of Local Face Detection #05** LFD #05 tracking face position.
1500B0E8	FDVT_LFD_INFO_YPOS_5	32	**Tracking Position of Local Face Detection #05** LFD #05 tracking face position.
1500B0EC	FDVT_LFD_INFO_CTRL_6	32	**Information of Local Face Detection #06** LFD #06 face information setting.
1500B0F0	FDVT_LFD_INFO_XPOS_6	32	**Tracking Position of Local Face Detection #06** LFD #06 tracking face position.
1500B0F4	FDVT_LFD_INFO_YPOS_6	32	**Tracking Position of Local Face Detection #06** LFD #06 tracking face position.
1500B0F8	FDVT_LFD_INFO_CTRL_7	32	**Information of Local Face Detection #07** LFD #07 face information setting.
1500B0FC	FDVT_LFD_INFO_XPOS_7	32	**Tracking Position of Local Face Detection #07** LFD #07 tracking face position.
1500B100	FDVT_LFD_INFO_YPOS_7	32	**Tracking Position of Local Face Detection #07** LFD #07 tracking face position.
1500B104	FDVT_LFD_INFO_CTRL_8	32	**Information of Local Face Detection #08** LFD #08 face information setting.
1500B108	FDVT_LFD_INFO_XPOS_8	32	**Tracking Position of Local Face Detection #08** LFD #08 tracking face position.
1500B10C	FDVT_LFD_INFO_YPOS_8	32	**Tracking Position of Local Face Detection #08** LFD #08 tracking face position.
1500B110	FDVT_LFD_INFO_CTRL_9	32	**Information of Local Face Detection #09** LFD #09 face information setting.
1500B114	FDVT_LFD_INFO_XPOS_9	32	**Tracking Position of Local Face Detection #09** LFD #09 tracking face position.
1500B118	FDVT_LFD_INFO_YPOS_9	32	**Tracking Position of Local Face Detection #09** LFD #09 tracking face position.
1500B11C	FDVT_LFD_INFO_CTRL_10	32	**Information of Local Face Detection #10** LFD #10 face information setting.
1500B120	FDVT_LFD_INFO_XPOS_10	32	**Tracking Position of Local Face Detection #10** LFD #10 tracking face position.
1500B124	FDVT_LFD_INFO_YPOS_10	32	**Tracking Position of Local Face Detection #10** LFD #10 tracking face position.
1500B128	FDVT_LFD_INFO_CTRL_11	32	**Information of Local Face Detection #11**

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Address	Name	Width	Register Function
			LFD #11 face information setting.
1500B12C	FDVT_LFD_INFO_XPOS_11	32	**Tracking Position of Local Face Detection #11** LFD #11 tracking face position.
1500B130	FDVT_LFD_INFO_YPOS_11	32	**Tracking Position of Local Face Detection #11** LFD #11 tracking face position.
1500B134	FDVT_LFD_INFO_CTRL_12	32	**Information of Local Face Detection #12** LFD #12 face information setting.
1500B138	FDVT_LFD_INFO_XPOS_12	32	**Tracking Position of Local Face Detection #12** LFD #12 tracking face position.
1500B13C	FDVT_LFD_INFO_YPOS_12	32	**Tracking Position of Local Face Detection #12** LFD #12 tracking face position.
1500B140	FDVT_LFD_INFO_CTRL_13	32	**Information of Local Face Detection #13** LFD #13 face information setting.
1500B144	FDVT_LFD_INFO_XPOS_13	32	**Tracking Position of Local Face Detection #13** LFD #13 tracking face position.
1500B148	FDVT_LFD_INFO_YPOS_13	32	**Tracking Position of Local Face Detection #13** LFD #13 tracking face position.
1500B14C	FDVT_LFD_INFO_CTRL_14	32	**Information of Local Face Detection #14** LFD #14 face information setting.
1500B150	FDVT_LFD_INFO_XPOS_14	32	**Tracking Position of Local Face Detection #14** LFD #14 tracking face position.
1500B154	FDVT_LFD_INFO_YPOS_14	32	**Tracking Position of Local Face Detection #14** LFD #14 tracking face position.
1500B158	FDVT_TC_ENABLE_RESULT	32	**Tracking Compensation Processing Indication** Indicates TC processing.
1500B15C	FDVT_INT_EN	32	**Interrupt Enable and Status** Enables FDVT interrupt and check signals.
1500B160	FDVT_SRC_WD_HT	32	**Source Image Size** FDVT source input image size.
1500B168	FDVT_INT	32	**Interrupt** FDVT interrupt.
1500B16C	FDVT_DEBUG_INFO_1	32	**Debug Information** FDVT debugging information
1500B170	FDVT_DEBUG_INFO_2	32	**Debug Information** FDVT debugging information
1500B174	FDVT_DEBUG_INFO_3	32	**Debug Information** FDVT debugging information
1500B178	FDVT_RESULT	32	**Number of Detected Faces** FDVT result.
1500B198	FDVT_SPARE_CELL	32	**Spare Cell** Spare cell for ECO
1500B19C	FDVT_CTRL	32	**Control Configuration of FDVT** FDVT control setting.
1500B1A0	FDVT_VERSION	32	**Version of FDVT** FDVT version.

1500B000 FDVT_START FDVT Start 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															DMA_STO	HARD_RS

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															P	T
Type															RW	RW
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STAR T
Type																RW
Reset																0

Bit(s)	Name	Description
17	DMA_STOP	**It is recommended to use DMA_STOP before HARD_RST.** When this bit is set to 1, FDVT engine will start to terminate GMC access FDVT engine will clear this bit to 0 automatically when GMC access is completed. The recommended DMA stop flow is setting DMA_STOP to 1 then polling DMA_STOP until it is set to 0.
16	HARD_RST	**Hard reset** Set this bit to 1 to reset FDVT engine immediately. Set this bit to 0 to return to normal mode. GMC access may not be completed immediately when this bit is set to 1. It is safer to wait for a period of time after setting this bit to 1 before setting this bit to 0.
0	START	**FDVT start signal** Set to 1 to start FDVT hardware engine.

1500B004 **FDVT_ENABLE** **Enables Function** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								FF_E NABL E				FD_E NABL E				RS_E ABLE
Type								RW				RW				RW
Reset								0				0				0

Bit(s)	Name	Description
8	FF_ENABLE	**Enables front-end feature loader** 0: Disable 1: Enable
4	FD_ENABLE	**Enables face detection** 0: Disable 1: Enable
0	RS_EABLE	**Enables resizer** 0: Disable 1: Enable

1500B008 **FDVT_RS** **Configuration of Resizer** **00000400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						SCALING_COEFF						RS_LOOP_NUM				

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Type						RW						RW				
Reset						1	0	0				0	0	0	0	0

Bit(s)	Name	Description
10:8	SCALING_COEFF	**Selects scaling coefficient table** Default: 4 0: Lagrange Default for zoom up 1: 4-p linear for zoom down 2: B-spline for zoom down default for zoom down 3: Cubic -0.8 for zoom up 4: Cubic -1.0 5: Cubic -1.4 6: Cubic -1.8 7: Cubic -2.0
4:0	RS_LOOP_NUM	**Loop number of rescaling function**

1500B00C **FDVT_RSCON_BASE_ADR** **Memory Base Address of RS Configuration** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RS_CONFIG_BASE_ADR[27:12]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RS_CONFIG_BASE_ADR[11:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	RS_CONFIG_BASE_ADR	**Configures memory address for storing RS** *Note: The base address should be 16-byte aligned.*

1500B010 **FDVT_RGB2Y0** **Transform Coefficients of RGB2Y** **02590132**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							**RGB2Y_1**									
Type							RW									
Reset							1	0	0	1	0	1	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**RGB2Y_0**									
Type							RW									
Reset							0	1	0	0	1	1	0	0	1	0

Bit(s)	Name	Description
25:16	RGB2Y_1	RGB to Y transform coefficient 1
9:0	RGB2Y_0	RGB to Y transform coefficient 0

1500B014 **FDVT_RGB2Y1** **Transform Coefficients of RGB2Y** **00000075**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

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Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**RGB2Y_2**									
Type							RW									
Reset							0	0	0	1	1	1	0	1	0	1

Bit(s)	Name	Description
9:0	RGB2Y_2	**RGB to Y transform coefficient 2** Y = [(R x RGB2Y0) + (G x RGB2Y1) + (B x RGB2Y2) + 512] >> 10

1500B018 FDVT_INVG0 Inverse Gamma Coefficients 66553520

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**IGMA_03**								**IGMA_02**							
Type	RW								RW							
Reset	0	1	1	0	0	1	1	0	0	1	0	1	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**IGMA_01**								**IGMA_00**							
Type	RW								RW							
Reset	0	0	1	1	0	1	0	1	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31:24	IGMA_03	Piece-wise coefficient of linear curve table
23:16	IGMA_02	Piece-wise coefficient of linear curve table
15:8	IGMA_01	Piece-wise coefficient of linear curve table
7:0	IGMA_00	Piece-wise coefficient of linear curve table

1500B01C FDVT_INVG1 Inverse Gamma Coefficients B8A28D79

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**IGMA_07**								**IGMA_06**							
Type	RW								RW							
Reset	1	0	1	1	1	0	0	0	1	0	1	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**IGMA_05**								**IGMA_04**							
Type	RW								RW							
Reset	1	0	0	0	1	1	0	1	0	1	1	1	1	0	0	1

Bit(s)	Name	Description
31:24	IGMA_07	Piece-wise coefficient of linear curve table
23:16	IGMA_06	Piece-wise coefficient of linear curve table
15:8	IGMA_05	Piece-wise coefficient of linear curve table
7:0	IGMA_04	Piece-wise coefficient of linear curve table

1500B020 FDVT_INVG2 Inverse Gamma Coefficients FFF4E7CF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**IGMA_11**								**IGMA_10**							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGMA_09								IGMA_08							
Type	RW								RW							
Reset	1	1	1	0	0	1	1	1	1	1	0	0	1	1	1	1

Bit(s)	Name	Description
31:24	IGMA_11	Piece-wise coefficient of linear curve table
23:16	IGMA_10	Piece-wise coefficient of linear curve table
15:8	IGMA_09	Piece-wise coefficient of linear curve table
7:0	IGMA_08	Piece-wise coefficient of linear curve table

1500B024 FDVT_FNUM_0 Feature Numbers 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					FNUM_ROP00_RIP30											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					FNUM_ROP00_RIP00											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	FNUM_ROP00_RIP30	**Number of learning data for ROP** RIP = (0, 30)
11:0	FNUM_ROP00_RIP00	**Number of learning data for ROP** RIP = (0, 0)

1500B028 FDVT_FNUM_1 Feature Numbers 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					FNUM_ROP50_RIP30P											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					FNUM_ROP50_RIP00											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	FNUM_ROP50_RIP30P	**Number of learning data for ROP** RIP = (50, 30)
11:0	FNUM_ROP50_RIP00	**Number of learning data for ROP** RIP = (50, 0)

1500B02C FDVT_FNUM_2 Feature Numbers 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					FNUM_ROP90_RIP30P											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					FNUM_ROP90_RIP00											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	FNUM_ROP90_RIP30P	**Number of learning data for ROP** RIP = (90, 30)
11:0	FNUM_ROP90_RIP00	**Number of learning data for ROP** RIP = (90, 0)

1500B030 FDVT_FNUM_3 Feature Numbers 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					FNUM_ROP90_RIP30N											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					FNUM_ROP50_RIP30N											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	FNUM_ROP90_RIP30N	**Number of learning data for ROP** RIP = (90, -30)
11:0	FNUM_ROP50_RIP30N	**Number of learning data for ROP** RIP = (50, -30)

1500B034 FDVT_T_FNUM_0 Feature Numbers in Tracking Mode 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					FNUM_ROP00_RIP30_TRACK											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					FNUM_ROP00_RIP00_TRACK											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	FNUM_ROP00_RIP30_TRACK	**Number of learning data for ROP** RIP = (0, 30) in tracking mode
11:0	FNUM_ROP00_RIP00_TRACK	**Number of learning data for ROP** RIP = (0, 0) in tracking mode

1500B038 FDVT_T_FNUM_1 Feature Numbers in Tracking Mode 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					FNUM_ROP50_RIP30P_TRACK											

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Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**FNUM_ROP50_RIP00_TRACK**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	FNUM_ROP50_RIP30P_TRACK	**Number of learning data for ROP** RIP = (50, 30) in tracking mode
11:0	FNUM_ROP50_RIP00_TRACK	**Number of learning data for ROP** RIP = (50, 0) in tracking mode

1500B03C **FDVT_T_FNUM_2** **Feature Numbers in Tracking Mode** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**FNUM_ROP90_RIP30P_TRACK**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**FNUM_ROP90_RIP00_TRACK**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	FNUM_ROP90_RIP30P_TRACK	**Number of learning data for ROP** RIP = (90, 30) in tracking mode
11:0	FNUM_ROP90_RIP00_TRACK	**Number of learning data for ROP** RIP = (90, 0) in tracking mode

1500B040 **FDVT_T_FNUM_3** **Feature Numbers in Tracking Mode** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**FNUM_ROP90_RIP30N_TRACK**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**FNUM_ROP50_RIP30N_TRACK**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	FNUM_ROP90_RIP30N_TRACK	**Number of learning data for ROP** RIP = (90, -30) in tracking mode
11:0	FNUM_ROP50_RIP30N_TRACK	**Number of learning data for ROP** RIP = (50, -30) in tracking mode

1500B044 **FDVT_FF_NUM** **Front-End Feature Numbers** **00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								FRONT_FEATURE_NUM_1								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								FRONT_FEATURE_NUM_0								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	FRONT_FEATURE_NUM_1	**Number of learning data for ROP** RIP = (0, 30) to be placed in front-end memory.
8:0	FRONT_FEATURE_NUM_0	**Number of learning data for ROP** RIP = (0, 0) to be placed in front-end memory *Note: Sum of FRONT_FEATURE_NUM_0 ~ 7 must ? 192 (FF_ENABLE = 0 => must be 0).*

1500B048 **FDVT_FF_NUM_1** **Front-End Feature Numbers** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								FRONT_FEATURE_NUM_3								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								FRONT_FEATURE_NUM_2								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	FRONT_FEATURE_NUM_3	**Number of learning data for ROP** RIP = (50, 30) to be placed in front-end memory.
8:0	FRONT_FEATURE_NUM_2	**Number of learning data for ROP** RIP = (50, 0) to be placed in front-end memory.

1500B04C **FDVT_FF_NUM_2** **Front-End Feature Numbers** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								FRONT_FEATURE_NUM_5								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								FRONT_FEATURE_NUM_4								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	FRONT_FEATURE_NUM_5	**Number of learning data for ROP** RIP = (90, 30) to be placed in front-end memory.
8:0	FRONT_FEATURE_NUM_4	**Number of learning data for ROP** RIP = (90, 0) to be placed in front-end memory.

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1500B050 **FDVT_FF_NUM_3** **Front-End Feature Numbers** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								FRONT_FEATURE_NUM_7								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								FRONT_FEATURE_NUM_6								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	FRONT_FEATURE_NUM_7	**Number of learning data for ROP** RIP = (90, -30) to be placed in front-end memory
8:0	FRONT_FEATURE_NUM_6	**Number of learning data for ROP** RIP = (50, -30) to be placed in front-end memory

1500B054 **FDVT_FF_BASE_ADR_0** **Memory Base Address of Learning Data** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FF_BASE_ADR_0[27:12]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FF_BASE_ADR_0[11:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	FF_BASE_ADR_0	**Learning data base address for ROP** RIP = (0, 0) *Note: The base address should be 16-byte aligned.*

1500B058 **FDVT_FF_BASE_ADR_1** **Memory Base Address of Learning Data** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FF_BASE_ADR_1[27:12]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FF_BASE_ADR_1[11:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	FF_BASE_ADR_1	**Learning data base address for ROP** RIP = (0, 30) *Note: The base address should be 16-byte aligned.*

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1500B05C **FDVT_FF_BASE_ADR_2** **Memory Base Address of Learning Data** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FF_BASE_ADR_2[27:12]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FF_BASE_ADR_2[11:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	FF_BASE_ADR_2	**Learning data base address for ROP** RIP = (50, 0) *Note: The base address should be 16-byte aligned.*

1500B060 **FDVT_FF_BASE_ADR_3** **Memory Base Address of Learning Data** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FF_BASE_ADR_3[27:12]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FF_BASE_ADR_3[11:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	FF_BASE_ADR_3	**Learning data base address for ROP** RIP = (50, 30) *Note: The base address should be 16-byte aligned.*

1500B064 **FDVT_FF_BASE_ADR_4** **Memory Base Address of Learning Data** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FF_BASE_ADR_4[27:12]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FF_BASE_ADR_4[11:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	FF_BASE_ADR_4	**Learning data base address for ROP** RIP = (90, 0) *Note: The base address should be 16-byte aligned.*

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1500B068 **FDVT_FF_BASE_ADR_5** **Memory Base Address of Learning Data** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FF_BASE_ADR_5[27:12]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FF_BASE_ADR_5[11:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	FF_BASE_ADR_5	**Learning data base address for ROP** RIP = (90, 30) *Note: The base address should be 16-byte aligned.*

1500B06C **FDVT_FF_BASE_ADR_6** **Memory Base Address of Learning Data** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FF_BASE_ADR_6[27:12]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FF_BASE_ADR_6[11:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	FF_BASE_ADR_6	**Learning data address for ROP** RIP = (50, -30) *Note: The base address should be 16-byte aligned.*

1500B070 **FDVT_FF_BASE_ADR_7** **Memory Base Address of Learning Data** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FF_BASE_ADR_7[27:12]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FF_BASE_ADR_7[11:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	FF_BASE_ADR_7	**Learning data address for ROP** RIP = (90, -30) *Note: The base address should be 16-byte aligned.*

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1500B074 FDVT_RMAP_0 Configuration of Feature Remap 2F000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RMAP_2		RMAP_1		RMAP_0		RMP_THRD_2							
Type			RW		RW		RW		RW							
Reset			1	0	1	1	1	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RMP_THRD_1								RMP_THRD_0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:28	RMAP_2	**Enables detector 2 for {LFD,GFD}** 0: Disable. 1: Enable.
27:26	RMAP_1	**Enables detector 1 for {LFD,GFD}** 0: Disable. 1: Enable.
25:24	RMAP_0	**Enables detector 0 for {LFD,GFD}** 0: Disable. 1: Enable.
23:16	RMP_THRD_2	**Adjusts feature threshold for detector 2 (signed 8 bits)**
15:8	RMP_THRD_1	**Adjusts feature threshold for detector 1 (signed 8 bits)**
7:0	RMP_THRD_0	**Adjusts feature threshold for detector 0 (signed 8 bits)**

1500B078 FDVT_RMAP_1 Configuration of Feature Remap 05230401

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RMAP_GAIN_2				RMAP_GAIN_1				RMAP_GAIN_0			
Type					RW				RW				RW			
Reset					0	1	0	1	0	0	1	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RFV_PAR													GFD_ENABLE
Type			RW													RW
Reset			0	0	0	1	0	0								1

Bit(s)	Name	Description
27:24	RMAP_GAIN_2	**CV re-mapping gain setting**
23:20	RMAP_GAIN_1	**CV re-mapping gain setting**
19:16	RMAP_GAIN_0	**CV re-mapping gain setting** The value range is 0 ~ 15, meaning 1/4 ~ 16/4 mapping. Default: RMAP_GAIN0 = 3, RMAP_GAIN1 = 2, RMAP_GAIN2 = 5.
13:8	RFV_PAR	**Parameter of ratio FV calculation**
0	GFD_ENABLE	**Enables global face detection** 0: Disable 1: Enable

1500B07C FDVT_FD Configuration of Face Detection 000F0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								MAX_FACE_NUM								

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Type								RW								
Reset								0	0	0	0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**MERGE_ENABLE**				**FD_LOOP_NUM**				
Type								RW				RW				
Reset								0				0	0	0	0	0

Bit(s)	Name	Description
24:16	MAX_FACE_NUM	**Max. supported face detection number** MAX_FACE_NUM <= 15 MERGE_ENABLE = 1 MAX_FACE_NUM > 15 MERGE_ENABLE = 0
8	MERGE_ENABLE	**Enables hardware face merging function**
4:0	FD_LOOP_NUM	**Loop number of FD**

1500B080 **FDVT_FD_CON_BASE_ADR** **Memory Base Address of FD Configuration** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**FD_CONFIG_BASE_ADR[27:12]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**FD_CONFIG_BASE_ADR[11:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	FD_CONFIG_BASE_ADR	**Base address of FD configuration in DRAM** *Note: The base address should be 16-byte aligned.*

1500B084 **FDVT_GFD** **Configuration of Global Skip Mode of Face Detection** **00000002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**GFD_PATTERN_TYPE**				**GFD_SKIP_MODE**		
Type										RW				RW		
Reset										0	0	0		0	1	0

Bit(s)	Name	Description
6:4	GFD_PATTERN_TYPE	**Detection pattern type setting**
2:0	GFD_SKIP_MODE	**GFD skip mode** 0: Apply face detection in each pixel. 1: Select 1 pixel to apply face detection in every 2 pixels. 2: Select 1 pixel to apply face detection in every 3 pixels. N: Select 1 pixel to apply face detection in every (N+1) pixels.

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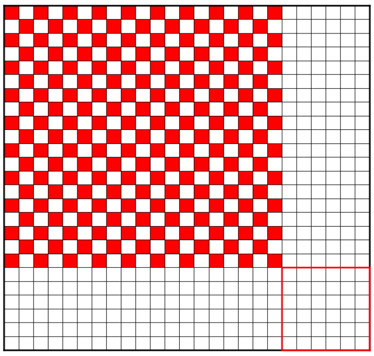
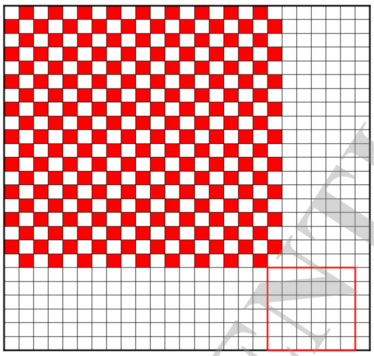
Example: In skip-1 mode, GFD_PATTERN_TYPE value should be 0 ~ 1.

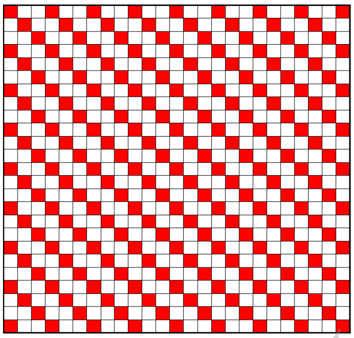


value = 0

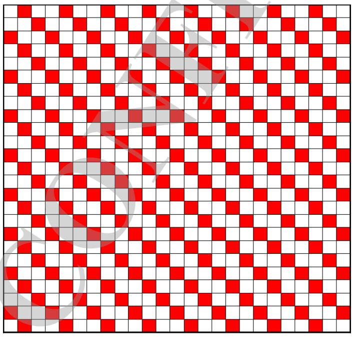


value = 1

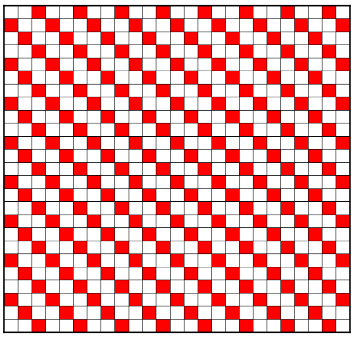
Example: In skip-2 mode, GFD_PATTERN_TYPE value should be 0 ~ 2.



value = 0



value = 1



value = 2

1500B088 **FDVT_LFD** **Configuration of Local Face Detection** **01130000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LFD_RIP_EXT					LFD_SIZE_EXT			LFD_SHRINK_IDX		
Type						RW					RW			RW		
Reset						0	0	1			0	1		0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				LFD_PATTERN_TYPE				LFD_SKIP_MODE					LFD_WINDOW_NUM			
Type				RW				RW					RW			
Reset				0				0					0	0	0	0

Bit(s)	Name	Description
26:24	LFD_RIP_EXT	**Pose extension index of LFD** 0: Not extended (1 pose). 1: Pose extended to neighboring RIP (3 poses). 2: Pose extended to neighboring ROP (max. 3 poses). 3: Pose extended to both neighboring RIP and neighboring ROP (max. 5 poses). 4: Pose extended to neighboring RIP and neighboring ROP with neighboring RIP (max. 9 poses). Others: Reserved

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Bit(s)	Name	Description
21:20	LFD_SIZE_EXT	**Size extension index of LFD** 0: Not extended. 1: Pose extended to size, size +1, size -1. 2: Pose extended to size, size +1, size +2, size -1 , size -2. Others: Reserved
18:16	LFD_SHRINK_IDX	**Shrink index for LFD inactive window** Inactive window = (x0+offset, y0+offset) ~ (x1-offset, y1-offset). 0: Offset = (x1-x0)*0/16. 1: Offset = (x1-x0)*1/16. 2: Offset = (x1-x0)*2/16. 3: Offset = (x1-x0)*3/16. 4: Offset = (x1-x0)*4/16. Others: Reserved
12	LFD_PATTERN_TYPE	**LFD skip pattern type**
8	LFD_SKIP_MODE	**Skip mode of LFD** 0: Does not skip. 1: Skip 1.
3:0	LFD_WINDOW_NUM	**Total window number of LFD**

1500B08C **FDVT_GFD_POS_0** **Region of Interest for Face Detection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							GFD_Y0									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							GFD_X0									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	GFD_Y0	Top left corner Y coordinate of the region of interest
9:0	GFD_X0	Top left corner X coordinate of the region of interest

1500B090 **FDVT_GFD_POS_1** **Region of Interest for Face Detection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							GFD_Y1									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							GFD_X1									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	GFD_Y1	Bottom right corner Y coordinate of the region of interest
9:0	GFD_X1	Bottom right corner X coordinate of the region of interest

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1500B094 **FDVT_GFD_DET_0** **Pose Selection of Face Detection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RIP_ROP_DIR_0[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RIP_ROP_DIR_0[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RIP_ROP_DIR_0	Pose selection of GFD (0~31)

1500B098 **FDVT_GFD_DET_1** **Pose Selection of Face Detection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**RIP_ROP_DIR_1[27:16]**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RIP_ROP_DIR_1[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:0	RIP_ROP_DIR_1	Pose selection of GFD (32~59)

Pose number:

	RIP	**30**	**60**	**90**	**120**	**150**	**180**	**-**	**-**	**-90**	**-60**	**-30**
ROP0	0	1	2	3	4	5	6	7	8	9	10	11
50	12	13	14	15	16	17	18	19	20	21	22	23
-50	24	25	26	27	28	29	30	31	32	33	34	35
90	36	37	38	39	40	41	42	43	44	45	46	47
-90	48	49	50	51	52	53	54	55	56	57	58	59

Note:

1. ***ROP50 and ROP-50 will not be detected if FD_CONFIG.rop_enable_semi is set to 0.***
2. ***ROP90 and ROP-90 will not be detected if FD_CONFIG.rop_enable_full is set to 0.***

1500B09C **FDVT_FD_RLT_BASE_ADR** **Memory Base Address of FD Results** **00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FD_RESULT_BASE_ADR[27:12]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FD_RESULT_BASE_ADR[11:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	FD_RESULT_BASE_ADR	**Base address of the face detection result in DRAM** *Note: The base address should be 16-byte aligned.*

1500B0A4 **FDVT_LFD_INFO_CTRL_0** **Information of Local Face Detection #00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LFD00_EN				LFD00_DETSIZE						LFD00_ROP_DIR		
Type				RW				RW						RW		
Reset				0				0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LFD00_RIP_DIR							LFD00_FACE_IDX								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	LFD00_EN	**Enables LFD00** 0: Disable 1: Enable
24:20	LFD00_DETSIZE	**Detected size index of LFD00**
18:16	LFD00_ROP_DIR	**ROP of LFD00** 0: 0° 1: 50° 2: -50° 3: 90° 4: -90° others: Reserved.
15:12	LFD00_RIP_DIR	**RIP of LFD00** 0: 0° 1: 30° 2: 60° 3: 90° 4: 120° 5: 150° 6: 180° 7: -150° 8: -120° 9: -90° 10: -60° 11: -30° Others: Reserved
8:0	LFD00_FACE_IDX	**Face index number of LFD00**

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1500B0A8 **FDVT_LFD_INFO_XPOS_0** **Tracking Position of Local Face Detection #00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							LFD00_Y0									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							LFD00_X0									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD00_Y0	Y position of top-left corner of LFD00
9:0	LFD00_X0	X position of top-left corner of LFD00

1500B0AC **FDVT_LFD_INFO_YPOS_0** **Tracking Position of Local Face Detection #00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							LFD00_Y1									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							LFD00_X1									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD00_Y1	Y position of bottom-right corner of LFD00
9:0	LFD00_X1	X position of bottom-right corner of LFD00

1500B0B0 **FDVT_LFD_INFO_CTRL_1** **Information of Local Face Detection #01** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LFD01_EN				LFD01_DETSIZE						LFD01_ROP_DIR		
Type				RW				RW						RW		
Reset				0				0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LFD01_RIP_DIR							LFD01_FACE_IDX								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	LFD01_EN	**Enables LFD01** 0: Disable 1: Enable
24:20	LFD01_DETSIZE	**Detected size index of LFD01**
18:16	LFD01_ROP_DIR	**ROP of LFD01** 0: 0° 1: 50° 2: -50°

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Bit(s)	Name	Description
		3: 90° 4: -90° Others: Reserved
15:12	LFD01_RIP_DIR	**RIP of LFD01** 0: 0° 1: 30° 2: 60° 3: 90° 4: 120° 5: 150° 6: 180° 7: -150° 8: -120° 9: -90° 10: -60° 11: -30° Others: Reserved
8:0	LFD01_FACE_IDX	**Face index number of LFD01**

1500B0B4 **FDVT_LFD_INFO_XPOS_1** **Tracking Position of Local Face Detection #01** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							**LFD01_Y0**									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**LFD01_X0**									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD01_Y0	Y position of top-left corner of LFD01
9:0	LFD01_X0	X position of top-left corner of LFD01

1500B0B8 **FDVT_LFD_INFO_YPOS_1** **Tracking Position of Local Face Detection #01** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							**LFD01_Y1**									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**LFD01_X1**									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD01_Y1	Y position of bottom-right corner of LFD01
9:0	LFD01_X1	X position of bottom-right corner of LFD01

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1500B0BC **FDVT_LFD_INFO_CTRL_2** **Information of Local Face Detection #02** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**LFD02_EN**				**LFD02_DETSIZE**						**LFD02_ROP_DIR**		
Type				RW				RW						RW		
Reset				0				0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**LFD02_RIP_DIR**							**LFD02_FACE_IDX**								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	LFD02_EN	**Enables LFD02** 0: Disable 1: Enable
24:20	LFD02_DETSIZE	**Detected size index of LFD02**
18:16	LFD02_ROP_DIR	**ROP of LFD02** 0: 0° 1: 50° 2: -50° 3: 90° 4: -90° Others: Reserved
15:12	LFD02_RIP_DIR	**RIP of LFD02** 0: 0° 1: 30° 2: 60° 3: 90° 4: 120° 5: 150° 6: 180° 7: -150° 8: -120° 9: -90° 10: -60° 11: -30° Others: Reserved
8:0	LFD02_FACE_IDX	**Face index number of LFD02**

1500B0C0 **FDVT_LFD_INFO_XPOS_2** **Tracking Position of Local Face Detection #02** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							**LFD02_Y0**									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**LFD02_X0**									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD02_Y0	Y position of top-left corner of LFD02
9:0	LFD02_X0	X position of top-left corner of LFD02

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1500B0C4 **FDVT_LFD_INFO_YPOS_2** **Tracking Position of Local Face Detection #02** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							LFD02_Y1									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							LFD02_X1									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD02_Y1	Y position of bottom-right corner of LFD02
9:0	LFD02_X1	X position of bottom-right corner of LFD02

1500B0C8 **FDVT_LFD_INFO_CTRL_3** **Information of Local Face Detection #03** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LFD03_EN				LFD03_DETSIZE						LFD03_ROP_DIR		
Type				RW				RW						RW		
Reset				0				0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LFD03_RIP_DIR							LFD03_FACE_IDX								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	LFD03_EN	**Enables LFD03** 0: Disable 1: Enable
24:20	LFD03_DETSIZE	**Detected size index of LFD03**
18:16	LFD03_ROP_DIR	**ROP of LFD03** 0: 0° 1: 50° 2: -50° 3: 90° 4: -90° Others: Reserved
15:12	LFD03_RIP_DIR	**RIP of LFD03** 0: 0° 1: 30° 2: 60° 3: 90° 4: 120° 5: 150° 6: 180° 7: -150° 8: -120° 9: -90° 10: -60° 11: -30°

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Bit(s)	Name	Description
		Others: Reserved
8:0	LFD03_FACE_IDX	**Face index number of LFD03**

1500B0CC **FDVT_LFD_INFO_XPOS_3** **Tracking Position of Local Face Detection #03** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							**LFD03_Y0**									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**LFD03_X0**									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD03_Y0	Y position of top-left corner of LFD03
9:0	LFD03_X0	X position of top-left corner of LFD03

1500B0D0 **FDVT_LFD_INFO_YPOS_3** **Tracking Position of Local Face Detection #03** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							**LFD03_Y1**									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**LFD03_X1**									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD03_Y1	Y position of bottom-right corner of LFD03
9:0	LFD03_X1	X position of bottom-right corner of LFD03

1500B0D4 **FDVT_LFD_INFO_CTRL_4** **Information of Local Face Detection #04** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**LFD04_EN**				**LFD04_DETSIZE**						**LFD04_ROP_DIR**		
Type				RW				RW						RW		
Reset				0				0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**LFD04_RIP_DIR**							**LFD04_FACE_IDX**								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	LFD04_EN	**Enables LFD04** 0: Disable

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Bit(s)	Name	Description
		1: Enable
24:20	LFD04_DETSIZE	**Detected size index of LFD04**
18:16	LFD04_ROP_DIR	**ROP of LFD04** 0: 0° 1: 50° 2: -50° 3: 90° 4: -90° Others: Reserved.
15:12	LFD04_RIP_DIR	**RIP of LFD04** 0: 0° 1: 30° 2: 60° 3: 90° 4: 120° 5: 150° 6: 180° 7: -150° 8: -120° 9: -90° 10: -60° 11: -30° Others: Reserved
8:0	LFD04_FACE_IDX	**Face index number of LFD04**

1500B0D8 **FDVT_LFD_INFO_XPOS_4** **Tracking Position of Local Face Detection #04** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							LFD04_Y0									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							LFD04_X0									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD04_Y0	Y position of top-left corner of LFD04
9:0	LFD04_X0	X position of top-left corner of LFD04

1500B0DC **FDVT_LFD_INFO_YPOS_4** **Tracking Position of Local Face Detection #04** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							LFD04_Y1									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							LFD04_X1									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
25:16	LFD04_Y1	Y position of bottom-right corner of LFD04
9:0	LFD04_X1	X position of bottom-right corner of LFD04

1500B0E0 FDVT_LFD_INFO_CTRL_5 Information of Local Face Detection #05 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LFD05_EN				LFD05_DETSIZE						LFD05_ROP_DIR		
Type				RW				RW						RW		
Reset				0				0	0	0	0	0		0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LFD05_RIP_DIR							LFD05_FACE_IDX								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	LFD05_EN	**Enables LFD05** 0: Disable 1: Enable
24:20	LFD05_DETSIZE	**Detected size index of LFD05**
18:16	LFD05_ROP_DIR	**ROP of LFD05** 0: 0° 1: 50° 2: -50° 3: 90° 4: -90° Others: Reserved
15:12	LFD05_RIP_DIR	**RIP of LFD05** 0: 0° 1: 30° 2: 60° 3: 90° 4: 120° 5: 150° 6: 180° 7: -150° 8: -120° 9: -90° 10: -60° 11: -30° Others: Reserved
8:0	LFD05_FACE_IDX	**Face index number of LFD05**

1500B0E4 FDVT_LFD_INFO_XPOS_5 Tracking Position of Local Face Detection #05 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							LFD05_Y0									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name							LFD05_X0									
Type							RW									

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Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD05_Y0	Y position of top-left corner of LFD05
9:0	LFD05_X0	X position of top-left corner of LFD05

1500B0E8 **FDVT_LFD_INFO_YPOS_5** **Tracking Position of Local Face Detection #05** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							LFD05_Y1									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							LFD05_X1									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD05_Y1	Y position of bottom-right corner of LFD05
9:0	LFD05_X1	X position of bottom-right corner of LFD05

1500B0EC **FDVT_LFD_INFO_CTRL_6** **Information of Local Face Detection #06** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LFD06_EN				LFD06_DETSIZE						LFD06_ROP_DIR		
Type				RW				RW						RW		
Reset				0				0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LFD06_RIP_DIR							LFD06_FACE_IDX								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	LFD06_EN	**Enables LFD06** 0: Disable 1: Enable
24:20	LFD06_DETSIZE	**Detected size index of LFD06**
18:16	LFD06_ROP_DIR	**ROP of LFD06** 0: 0° 1: 50° 2: -50° 3: 90° 4: -90° Others: Reserved
15:12	LFD06_RIP_DIR	**RIP of LFD06** 0: 0° 1: 30° 2: 60° 3: 90° 4: 120°

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Bit(s)	Name	Description
		5: 150° 6: 180° 7: -150° 8: -120° 9: -90° 10: -60° 11: -30° Others: Reserved
8:0	LFD06_FACE_IDX	**Face index number of LFD06**

1500B0F0 **FDVT_LFD_INFO_XPOS_6** **Tracking Position of Local Face Detection #06** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							LFD06_Y0									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							LFD06_X0									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD06_Y0	Y position of top-left corner of LFD06
9:0	LFD06_X0	X position of top-left corner of LFD06

1500B0F4 **FDVT_LFD_INFO_YPOS_6** **Tracking Position of Local Face Detection #06** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							LFD06_Y1									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							LFD06_X1									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD06_Y1	Y position of bottom-right corner of LFD06
9:0	LFD06_X1	X position of bottom-right corner of LFD06

1500B0F8 **FDVT_LFD_INFO_CTRL_7** **Information of Local Face Detection #07** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LFD07_EN				LFD07_DETSIZE						LFD07_ROP_DIR		
Type				RW				RW						RW		
Reset				0				0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LFD07_RIP_DIR							LFD07_FACE_IDX								

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Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	LFD07_EN	**Enables LFD07** 0: Disable 1: Enable
24:20	LFD07_DETSIZE	**Detected size index of LFD07**
18:16	LFD07_ROP_DIR	**ROP of LFD07** 0: 0° 1: 50° 2: -50° 3: 90° 4: -90° Others: Reserved
15:12	LFD07_RIP_DIR	**RIP of LFD07** 0: 0° 1: 30° 2: 60° 3: 90° 4: 120° 5: 150° 6: 180° 7: -150° 8: -120° 9: -90° 10: -60° 11: -30° Others: Reserved
8:0	LFD07_FACE_IDX	**Face index number of LFD07**

1500B0FC **FDVT_LFD_INFO_XPOS_7** **Tracking Position of Local Face Detection #07** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							**LFD07_Y0**									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**LFD07_X0**									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD07_Y0	Y position of top-left corner of LFD07
9:0	LFD07_X0	X position of top-left corner of LFD07

1500B100 **FDVT_LFD_INFO_YPOS_7** **Tracking Position of Local Face Detection #07** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							**LFD07_Y1**									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							LFD07_X1									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD07_Y1	Y position of bottom-right corner of LFD07
9:0	LFD07_X1	X position of bottom-right corner of LFD07

1500B104 **FDVT_LFD_INFO_CTRL_8** **Information of Local Face Detection #08** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LFD08_EN				LFD08_DETSIZE						LFD08_ROP_DIR		
Type				RW				RW						RW		
Reset				0				0	0	0	0	0		0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LFD08_RIP_DIR							LFD08_FACE_IDX								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	LFD08_EN	**Enables LFD08** 0: Disable 1: Enable
24:20	LFD08_DETSIZE	**Detected size index of LFD08**
18:16	LFD08_ROP_DIR	**ROP of LFD08** 0: 0° 1: 50° 2: -50° 3: 90° 4: -90° Others: Reserved
15:12	LFD08_RIP_DIR	**RIP of LFD08** 0: 0° 1: 30° 2: 60° 3: 90° 4: 120° 5: 150° 6: 180° 7: -150° 8: -120° 9: -90° 10: -60° 11: -30° Others: Reserved
8:0	LFD08_FACE_IDX	**Face index number of LFD08**

1500B108 **FDVT_LFD_INFO_XPOS_8** **Tracking Position of Local Face Detection #08** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name							**LFD08_Y0**									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**LFD08_X0**									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD08_Y0	Y position of top-left corner of LFD08
9:0	LFD08_X0	X position of top-left corner of LFD08

1500B10C **FDVT_LFD_INFO_YPOS_8** **Tracking Position of Local Face Detection #08** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							**LFD08_Y1**									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**LFD08_X1**									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD08_Y1	Y position of bottom-right corner of LFD08
9:0	LFD08_X1	X position of bottom-right corner of LFD08

1500B110 **FDVT_LFD_INFO_CTRL_9** **Information of Local Face Detection #09** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**LFD09_EN**				**LFD09_DETSIZE**						**LFD09_ROP_DIR**		
Type				RW				RW						RW		
Reset				0				0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**LFD09_RIP_DIR**							**LFD09_FACE_IDX**								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	LFD09_EN	**Enables LFD09** 0: Disable 1: Enable
24:20	LFD09_DETSIZE	**Detected size index of LFD09**
18:16	LFD09_ROP_DIR	**ROP of LFD09** 0: 0° 1: 50° 2: -50° 3: 90° 4: -90° Others: Reserved

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Bit(s)	Name	Description
15:12	LFD09_RIP_DIR	**RIP of LFD09** 0: 0º 1: 30º 2: 60º 3: 90º 4: 120º 5: 150º 6: 180º 7: -150º 8: -120º 9: -90º 10: -60º 11: -30º Others: Reserved
8:0	LFD09_FACE_IDX	**Face index number of LFD09**

1500B114 **FDVT_LFD_INFO_XPOS_9** **Tracking Position of Local Face Detection #09** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							LFD09_Y0									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							LFD09_X0									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD09_Y0	Y position of top-left corner of LFD09
9:0	LFD09_X0	X position of top-left corner of LFD09

1500B118 **FDVT_LFD_INFO_YPOS_9** **Tracking Position of Local Face Detection #09** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							LFD09_Y1									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							LFD09_X1									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD09_Y1	Y position of bottom-right corner of LFD09
9:0	LFD09_X1	X position of bottom-right corner of LFD09

1500B11C **FDVT_LFD_INFO_CTRL_10** **Information of Local Face Detection #10** **00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LFD10_EN				LFD10_DETSIZE						LFD10_ROP_DIR		
Type				RW				RW						RW		
Reset				0				0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LFD10_RIP_DIR							LFD10_FACE_IDX								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	LFD10_EN	**Enables LFD10** 0: Disable 1: Enable
24:20	LFD10_DETSIZE	**Detected size index of LFD10**
18:16	LFD10_ROP_DIR	**ROP of LFD10** 0: 0° 1: 50° 2: -50° 3: 90° 4: -90° Others: Reserved
15:12	LFD10_RIP_DIR	**RIP of LFD10** 0: 0° 1: 30° 2: 60° 3: 90° 4: 120° 5: 150° 6: 180° 7: -150° 8: -120° 9: -90° 10: -60° 11: -30° Others: Reserved
8:0	LFD10_FACE_IDX	**Face index number of LFD10**

1500B120 **FDVT_LFD_INFO_XPOS_10** **Tracking Position of Local Face Detection #10** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							LFD10_Y0									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							LFD10_X0									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD10_Y0	Y position of top-left corner of LFD10
9:0	LFD10_X0	X position of top-left corner of LFD10

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1500B124	FDVT_LFD_INFO_YPOS_10	Tracking Position of Local Face Detection #10	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							LFD10_Y1									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							LFD10_X1									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD10_Y1	Y position of bottom-right corner of LFD10
9:0	LFD10_X1	X position of bottom-right corner of LFD10

1500B128	FDVT_LFD_INFO_CTRL_11	Information of Local Face Detection #11	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LFD11_EN				LFD11_DETSIZE						LFD11_ROP_DIR		
Type				RW				RW						RW		
Reset				0				0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LFD11_RIP_DIR							LFD11_FACE_IDX								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	LFD11_EN	**Enables LFD11** 0: Disable 1: Enable
24:20	LFD11_DETSIZE	**Detected size index of LFD11**
18:16	LFD11_ROP_DIR	**ROP of LFD11** 0: 0° 1: 50° 2: -50° 3: 90° 4: -90° Others: Reserved
15:12	LFD11_RIP_DIR	**RIP of LFD11** 0: 0° 1: 30° 2: 60° 3: 90° 4: 120° 5: 150° 6: 180° 7: -150° 8: -120° 9: -90° 10: -60° 11: -30° Others: Reserved
8:0	LFD11_FACE_IDX	**Face index number of LFD11**

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1500B12C **FDVT_LFD_INFO_XPOS_11** **Tracking Position of Local Face Detection #11** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							LFD11_Y0									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							LFD11_X0									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD11_Y0	Y position of top-left corner of LFD11
9:0	LFD11_X0	X position of top-left corner of LFD11

1500B130 **FDVT_LFD_INFO_YPOS_11** **Tracking Position of Local Face Detection #11** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							LFD11_Y1									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							LFD11_X1									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD11_Y1	Y position of bottom-right corner of LFD11
9:0	LFD11_X1	X position of bottom-right corner of LFD11

1500B134 **FDVT_LFD_INFO_CTRL_12** **Information of Local Face Detection #12** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LFD12_EN				LFD12_DETSIZE						LFD12_ROP_DIR		
Type				RW				RW						RW		
Reset				0				0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LFD12_RIP_DIR							LFD12_FACE_IDX								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	LFD12_EN	**Enables LFD12** 0: Disable 1: Enable
24:20	LFD12_DETSIZE	**Detected size index of LFD12**
18:16	LFD12_ROP_DIR	**ROP of LFD12**

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Bit(s)	Name	Description
		0: 0° 1: 50° 2: -50° 3: 90° 4: -90° Others: Reserved
15:12	LFD12_RIP_DIR	**RIP of LFD12** 0: 0° 1: 30° 2: 60° 3: 90° 4: 120° 5: 150° 6: 180° 7: -150° 8: -120° 9: -90° 10: -60° 11: -30° Others: Reserved
8:0	LFD12_FACE_IDX	**Face index number of LFD12**

1500B138 **FDVT_LFD_INFO_XPOS_12** **Tracking Position of Local Face Detection #12** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							LFD12_Y0									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							LFD12_X0									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD12_Y0	Y position of top-left corner of LFD12
9:0	LFD12_X0	X position of top-left corner of LFD12

1500B13C **FDVT_LFD_INFO_YPOS_12** **Tracking Position of Local Face Detection #12** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							LFD12_Y1									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							LFD12_X1									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD12_Y1	Y position of bottom-right corner of LFD12
9:0	LFD12_X1	X position of bottom-right corner of LFD12

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1500B140 **FDVT_LFD_INFO_CTRL_13** **Information of Local Face Detection #13** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LFD13_EN				LFD13_DETSIZE						LFD13_ROP_DIR		
Type				RW				RW						RW		
Reset				0				0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LFD13_RIP_DIR							LFD13_FACE_IDX								
Type	RW							RW								
Reset	0	0	0					0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	LFD13_EN	**Enables LFD13** 0: Disable 1: Enable
24:20	LFD13_DETSIZE	**Detected size index of LFD13**
18:16	LFD13_ROP_DIR	**ROP of LFD13** 0: 0° 1: 50° 2: -50° 3: 90° 4: -90° Others: Reserved
15:13	LFD13_RIP_DIR	**RIP of LFD13** 0: 0° 1: 30° 2: 60° 3: 90° 4: 120° 5: 150° 6: 180° 7: -150° 8: -120° 9: -90° 10: -60° 11: -30° Others: Reserved
8:0	LFD13_FACE_IDX	**Face index number of LFD13**

1500B144 **FDVT_LFD_INFO_XPOS_13** **Tracking Position of Local Face Detection #13** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							LFD13_Y0									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							LFD13_X0									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
25:16	LFD13_Y0	Y position of top-left corner of LFD13
9:0	LFD13_X0	X position of top-left corner of LFD13

1500B148 FDVT_LFD_INFO_YPOS_13 Tracking Position of Local Face Detection #13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							LFD13_Y1									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							LFD13_X1									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD13_Y1	Y position of bottom-right corner of LFD13
9:0	LFD13_X1	X position of bottom-right corner of LFD13

1500B14C FDVT_LFD_INFO_CTRL_14 Information of Local Face Detection #14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LFD14_EN				LFD14_DETSIZE						LFD14_ROP_DIR		
Type				RW				RW						RW		
Reset				0				0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LFD14_RIP_DIR							LFD14_FACE_IDX								
Type	RW							RW								
Reset	0	0	0					0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	LFD14_EN	**Enables LFD14** 0: Disable 1: Enable
24:20	LFD14_DETSIZE	**Detected size index of LFD14**
18:16	LFD14_ROP_DIR	**ROP of LFD14** 0: 0° 1: 50° 2: -50° 3: 90° 4: -90° Others: Reserved
15:13	LFD14_RIP_DIR	**RIP of LFD14** 0: 0° 1: 30° 2: 60° 3: 90° 4: 120° 5: 150° 6: 180° 7: -150°

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Bit(s)	Name	Description
		8: -120° 9: -90° 10: -60° 11: -30° Others: Reserved
8:0	LFD14_FACE_IDX	**Face index number of LFD14**

1500B150 **FDVT_LFD_INFO_XPOS_14** **Tracking Position of Local Face Detection #14** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							LFD14_Y0									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							LFD14_X0									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD14_Y0	Y position of top-left corner of LFD14
9:0	LFD14_X0	X position of top-left corner of LFD14

1500B154 **FDVT_LFD_INFO_YPOS_14** **Tracking Position of Local Face Detection #14** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							LFD14_Y1									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							LFD14_X1									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	LFD14_Y1	Y position of bottom-right corner of LFD14
9:0	LFD14_X1	X position of bottom-right corner of LFD14

1500B158 **FDVT_TC_ENABLE_RESULT** **Tracking Compensation Processing Indication** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		LFD14_TC_EN	LFD13_TC_EN	LFD12_TC_EN	LFD11_TC_EN	LFD10_TC_EN	LFD09_TC_EN	LFD08_TC_EN	LFD07_TC_EN	LFD06_TC_EN	LFD05_TC_EN	LFD04_TC_EN	LFD03_TC_EN	LFD02_TC_EN	LFD01_TC_EN	LFD00_TC_EN
Type		RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

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Bit(s)	Name	Description
30	LFD14_TC_EN	
29	LFD13_TC_EN	
28	LFD12_TC_EN	
27	LFD11_TC_EN	
26	LFD10_TC_EN	
25	LFD09_TC_EN	
24	LFD08_TC_EN	
23	LFD07_TC_EN	
22	LFD06_TC_EN	
21	LFD05_TC_EN	
20	LFD04_TC_EN	
19	LFD03_TC_EN	
18	LFD02_TC_EN	
17	LFD01_TC_EN	
16	LFD00_TC_EN	

1500B15C **FDVT_INT_EN** **Interrupt Enable and Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FD_DONE	FD_BUSY			FF_DONE	FF_BUSY			RS_DONE	RS_BUSY
Type							RO	RO			RO	RO			RO	RO
Reset							0	0			0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						INT_RD_CNT						INT_CLR_MODE				INT_ENABLE
Type						RO						RW				RW
Reset						0	0	0				0				0

Bit(s)	Name	Description
25	FD_DONE	**FD is done or not done**
24	FD_BUSY	**FD is busy or not busy**
21	FF_DONE	**FF is done or not done**
20	FF_BUSY	**FF is busy or not busy**
17	RS_DONE	**RS is done or not done**
16	RS_BUSY	**RS is busy or not busy**
10:8	INT_RD_CNT	**Software interrupt times**
4	INT_CLR_MODE	**Interrupt clear mode** 0: Read-clear mode 1: Write-clear mode
0	INT_ENABLE	**Enables hardware interrupt mode** 0: Disable 1: Enable

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1500B160 **FDVT_SRC_WD_HT** **Source Image Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							**INPUT_IMG_WD**									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**INPUT_IMG_HT**									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	INPUT_IMG_WD	Width of the source input image
9:0	INPUT_IMG_HT	Height of the source input image

1500B168 **FDVT_INT** **Interrupt** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**INT_FDVT**
Type																RO
Reset																0

Bit(s)	Name	Description
0	INT_FDVT	**FDVT interrupt signal** Cleared by INT_CLR_MODE = 1.

1500B16C **FDVT_DEBUG_INFO_1** **Debug Information** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**DCM_SHARE_MEM_ST**	**DCM_DMA_ST**	**DCM_FD_ST**	**DCM_RS_ST**	**DCM_SEQ_ST**				**RS_LOOP_CNT**				
Type				RO	RO	RO	RO	RO				RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**FD_LOOP_CNT**				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
28	DCM_SHARE_MEM_ST	DCM status of shared memory
27	DCM_DMA_ST	DCM status of DMA
26	DCM_FD_ST	DCM status of face detection
25	DCM_RS_ST	DCM status of resizer

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Bit(s)	Name	Description
24	DCM_SEQ_ST	DCM status of sequencer
20:16	RS_LOOP_CNT	Loop counter of RS
4:0	FD_LOOP_CNT	Loop counter of FD

1500B170 **FDVT_DEBUG_INFO_2** **Debug Information** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RS_DETECT_H_CNT											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RS_DETECT_V_CNT											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	RS_DETECT_H_CNT	Horizontal counter of RS
11:0	RS_DETECT_V_CNT	Vertical counter of RS

1500B174 **FDVT_DEBUG_INFO_3** **Debug Information** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FD_DETECT_X									
Type							RO									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							FD_DETECT_Y									
Type							RO									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	FD_DETECT_X	Detection X position of FD
9:0	FD_DETECT_Y	Detection Y position of FD

1500B178 **FDVT_RESULT** **Number of Detected Faces** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								LFD_NUM								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								GFD_NUM								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	LFD_NUM	Number of detected face by LFD
8:0	GFD_NUM	Number of detected face by GFD

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1500B198 **FDVT_SPARE_CELL** **Spare Cell** **FFFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE_CELL[31:16]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE_CELL[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE_CELL	Spare cell

1500B19C **FDVT_CTRL** **Control Configuration of FDVT** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											WR_PULTRA	WR_ULTRA	RP_PULTRA	RP_ULTRA	RB_PULTRA	RB_ULTRA
Type											RW	RW	RW	RW	RW	RW
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												DCM_SHARE_MEM_DIS	DCM_DMA_DIS	DCM_FD_DIS	DCM_RS_DIS	DCM_SEQ_DIS
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
21	WR_PULTRA	**WR pre-ultra setting for better DMA access**
20	WR_ULTRA	**WR ultra setting for better DMA access**
19	RP_PULTRA	**RP pre-ultra setting for better DMA access**
18	RP_ULTRA	**RP ultra setting for better DMA access**
17	RB_PULTRA	**RB pre-ultra setting for better DMA access**
16	RB_ULTRA	**RB ultra setting for better DMA access**
4	DCM_SHARE_MEM_DIS	**DCM of shared memory enabling/disabling setting** 0: Enable DCM 1: Disable DCM
3	DCM_DMA_DIS	**DCM of DMA enabling/disabling setting** 0: Enable DCM 1: Disable DCM
2	DCM_FD_DIS	**DCM of face detection enabling/disabling setting** 0: Enable DCM 1: Disable DCM
1	DCM_RS_DIS	**DCM of resizer enabling/disabling setting** 0: Enable DCM 1: Disable DCM
0	DCM_SEQ_DIS	**DCM of sequencer enabling/disabling setting**

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Bit(s)	Name	Description
		0: Enable DCM 1: Disable DCM

1500B1A0 **FDVT_VERSION** **Version of FDVT** **20130528**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**YEAR**															
Type	RO															
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MONTH**								**DAY**							
Type	RO								RO							
Reset	0	0	0	0	0	1	0	1	0	0	1	0	1	0	0	0

Bit(s)	Name	Description
31:16	YEAR	Year of FDVT version
15:8	MONTH	Month of FDVT version
7:0	DAY	Day of FDVT version

6.6.3 Parameter Setting in DRAM

RS_CONFIG (BIT 127 ~ 0)

Bit	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112
Name	**IGMA_EN**	**SRC_FORMAT**			**XMAG_YMAG**											
Bit	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
Name		**DES_IMG_HT**												**DES_IMG_WD**		
Bit	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
Name	**DES_IMG_WD**									**SRC_IMG_HT**						
Bit	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
Name	**SRC_IMG_HT**					**SRC_IMG_WD**										
Bit	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Name	**DES_BASE_ADR**															
Bit	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Name	**DES_BASE_ADR**															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SRC_BASE_ADR**															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SRC_BASE_ADR**															

RS_CONFIG (BIT 255 ~ 128)

Bit	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112
Name																
Bit	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
Name																
Bit	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
Name																
Bit	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
Name																
Bit	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48

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Name																
Bit	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Name	**SRC_IMG_STRIDE**															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**YOFFSET**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**YOFFSET**							**XOFFSET**								

Note:

1. *Base address should be 16-byte aligned.*
2. *FD will not process the resized image width or height that is smaller than 24.*

SRC_BASE_ADR Rescaling source image source base address

DES_BASE_ADR Rescaling destination image destination base address (The size of destination buffer must be multiple of 16.)

SRC_IMG_WD Rescaling source image width

SRC_IMG_HT Rescaling source image height

DES_IMG_WD Rescaling destination image width

DES_IMG_HT Rescaling destination image height

XMAG_YMAG Rescaling ratio (format: Q0.3.9)

SRC_FORMAT Rescaling source image format

- **0** RGB
- **1** Y
- **2** YUYV
- **3** YVYU
- **4** VYUY
- **5** UYVY

IGMA_EN Enables inverse gamma

XOFFSET Beginning sub-pixel x position (less than 504)

YOFFSET Beginning sub-pixel x position (less than 504)

SRC_IMG_STRIDE Rescaling source image stride (Y must be multiple of 16; others must be multiple of 8.)

FD_CONFIG (BIT 127 ~ 0)																
Bit	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112
Name	**IMG_STRIDE**															
Bit	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
Name										**SHIFT_V**						
Bit	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
Name	**SHIFT_H**							**IFACTOR**								
Bit	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
Name	**IFACTOR**	**SFACTOR**														
Bit	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Name											**ROP_ENABLE_FULL**	**ROP_ENABLE_SEMI**	**IMG_HT**			
Bit	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Name	**IMG_HT**						**IMG_WD**									

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**IMG_BASE_ADR**															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**IMG_BASE_ADR**															

Note: Base address should be 16-byte aligned.

IMG_BASE_ADR Base address of the source (luma only) image

IMG_WD Width of source image

IMG_HT Height of source image

ROP_ENABLE_SEMI Enables ROP50 and ROP-50 LFD detection
- **0** pose 12 ~ pose 35 will not be detected by LFD.
- **1** pose 12 ~ pose 35 will be detected by LFD if LFD_POSE is set to detect this pose.

ROP_ENABLE_FULL Enables ROP90 and ROP-90 LFD detection
- **0** pose 36 ~ pose 59 will not be detected by LFD.
- **1** pose 36 ~ pose 59 will be detected by LFD if LFD_POSE is set to detect this pose.

SFACTOR Scaling factor relative to RGB image size. Format is 6.9 (>=1.0)

IFACTOR Inverse scaling factor relative to RGB image size. Format is 1.9 (<=1.0)

SHIFT_H Horizontal search range of active window. LFD searches from (LFDXX.x0-SHIFT_H) to (LFDXX.x0+SHIFT_H).The unit is one pixel of RGB image size.

SHIFT_V Vertical search range of active window. LFD searches from (LFDXX.y0-SHIFT_V) to (LFDXX.y0+SHIFT_V).The unit is one pixel of RGB image size.

IMG_STRIDE Stride of source image

FACE RESULT (BIT 127 ~ 0)																
Bit	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112
Name																
Bit	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
Name																
Bit	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
Name																
Bit	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
Name											**DET_SIZE**					**ROP_DIR**
Bit	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Name	**ROP_DIR**		**RIP_DIR**				**FCV**								**Y1**	
Bit	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Name	**Y1**								**X1**							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**X1**		**Y0**										**X0**			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**X0**						**TYP**	**FACE_INDEX**								

Note: The max. FACE RESULT number is 511.

FACE_INDEX Indicates face index number

TYP Indicates face type
- **0** Face is detected by GFD.

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	1	Face is detected by LFD.
X0, Y0, X1, Y1	Indicates face candidate position	
FCV	Indicates face confidence value of the face candidate	
RIP_DIR	Indicates face RIP (rotate in plane) direction	
	0	0°
	1	30°
	2	60°
	...	
	11	-30°
	Others	Reserved
ROP_DIR	Indicates face ROP (rotate out of plane) direction	
	0	0°
	1	50°
	2	-50°
	3	90°
	4	-90°
	Others	Reserved
DET_SIZE	Indicates face size index	

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6.7 MDP_RDMA

6.7.1 Introduction

MDP RDMA is used to read images of multiple source format in memory and then output in scan-line sequence to the following engine. It supports several functions, such as

- Input image clipping, as illustrated in Figure 6-10.
- Different input formats, as listed in Table 6-2.
- Color conversion for RGB to YUV.
- Chroma upsample for cosited or non-consited YUV422/420 source

To support larger image size with cost burden, tile mode scheme is applied in MDP. MDP_RDMA is fully tile mode ready and can fulfill the single or tile mode operation. It also has a 3x3 color conversion inside. When the input is in RGB domain and output is in YCbCr domain, the 3x3 color conversion should be set well to get the correct data.

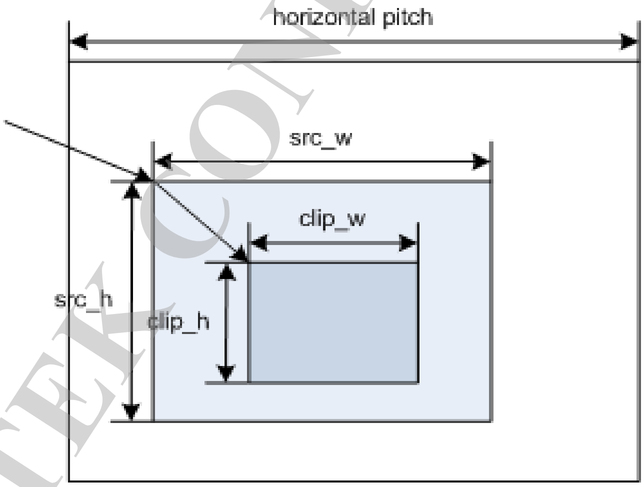

Figure 6-10. Support clipping from source frame buffer

Table 6-2. Input format list

Input domain	Supported format
YCbCr	YCbCr_420_P_SW YCbCr_420_SP_SW YCbCr_420_SP_HW_BLOCK YCbCr_420_SP_HW_BLOCK_INTERLACE YCbCr_422_P_SW YCbCr_422_SP_SW YCbCr_422_I_SW YCbCr_422_I_HW_BLOCK Y Only
RGB	RGB565 RGB(BGR)888

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Input domain	Supported format
	ARGB(RGBA)8888 XRGB(RGBX)8888

6.7.2 Features

- Supports multiple format of input images
- Supports up to Full HD resolution 1920x1200@60 fps without tile mode
- Supports YUV420/422 scanline 1/2/3 planes and RGB 16/24/32 bits
- Supports arbitrary byte swap for YUV or RGB source
- Supports cropping/clipping.
- Supports chroma up-sample filter to YUV444
- Supports default optimized or programmable RGB2YUV
- Tile mode ready; supports source width up to 131072 pixels
- Direct link to RSZ with YUV 444

6.7.3 Block Diagram

The internal pipeline of MDP_RDMA is shown in the following diagram, the input is from external memory via SMI read port, and output is direct linked to the next engine depending on the dispsys data-path setting, e.g. RSZ. There is also APB interface for S/W control, following the mutex protocol for advanced S/W control from disp_mutex.

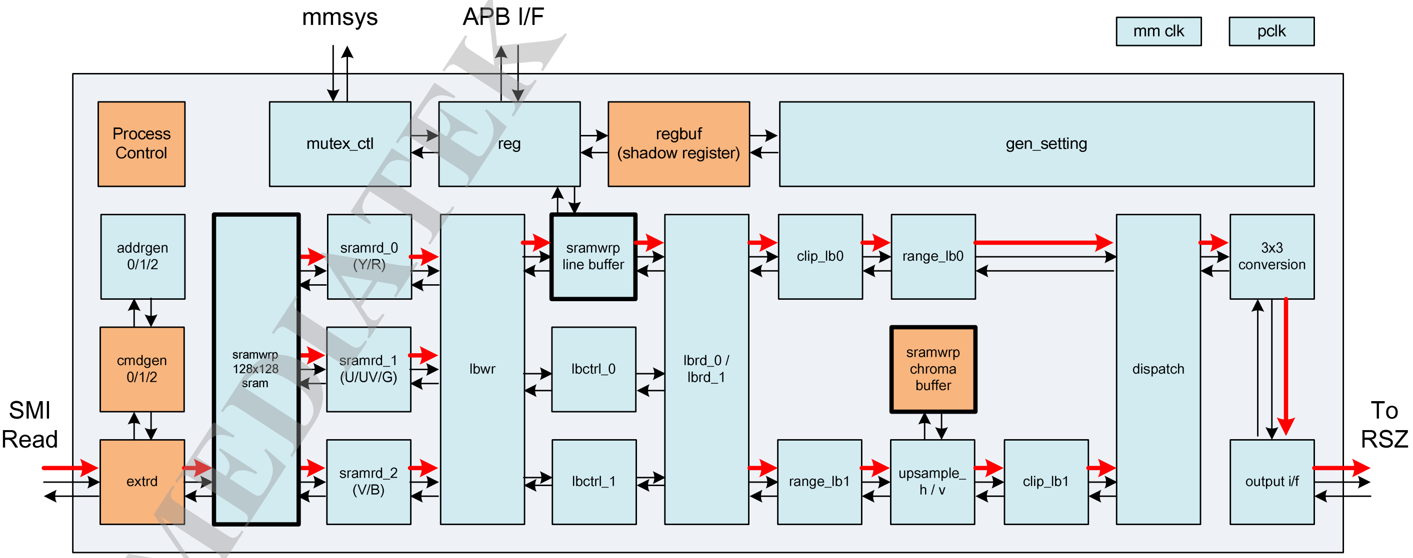

Figure 6-11. Block diagram of DISP MDP_RDMA

6.7.4 Register Definition

Module name: MDP_RDMA Base address: (+14001000h)

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Address	Name	Width	Register Function
14001000	EN	32	**Enable Register** Rotator enabling signal
14001008	RESET	32	**Reset Register** Resets rotator internal
14001010	INTERRUPT_ENABLE	32	**Interrupt Enable Register** Enables rotator interrupt
14001018	INTERRUPT_STATUS	32	**Interrupt Status Register** Status of rotator interrupt
14001020	CON	32	**Control Register** Controls behavior of rotator
14001028	GMCIF_CON	32	**GMC Interface Control Register** Controls behavior of GMC interface of rotator
14001030	SRC_CON	32	**Source Control Register** Sets up format of source frame buffer
14001060	MF_BKGD_SIZE_IN_BYTE	32	**Main Frame Background Size In Byte Register** Rotator main frame background size in byte
14001068	MF_BKGD_SIZE_IN_PXL	32	**Main Frame Background Size In Pixel Register** Rotator main frame background size in pixel
14001070	MF_SRC_SIZE	32	**Main Frame Source Size Register** Rotator main frame source size
14001078	MF_CLIP_SIZE	32	**Main Frame Clip Size Register** Rotator main frame clip size
14001080	MF_OFFSET_1	32	**Main Frame Offset 1 Register** Rotator main frame offset 1
14001088	MF_PAR	32	**Main Frame Parameter Register** Rotator main frame parameter
14001090	SF_BKGD_SIZE_IN_BYTE	32	**Sub Frame Background Size In Byte Register** Rotator sub frame background size in byte
140010B8	SF_PAR	32	**Sub Frame Parameter Register** Rotator sub frame parameter
140010C0	MB_DEPTH	32	**Main Line Buffer Depth Control Register** Rotator main line buffer depth control
140010C8	MB_BASE	32	**Main Buffer Base Address Register** Rotator main buffer base address
140010D0	MB_CON	32	**Main Line Buffer Control Register** Rotator main line buffer control
140010D8	SB_DEPTH	32	**Sub Line Buffer Depth Control Register** Rotator sub line buffer depth control
140010E0	SB_BASE	32	**Sub Buffer Base Address Register** Rotator sub buffer base address.
140010E8	SB_CON	32	**Sub Line Buffer Control Register** Rotator sub line buffer control
140010F0	VC1_RANGE	32	**VC1 Range Control Register** Rotator VC1 range reduction and mapping control
14001100	SRC_END_0	32	**Source End Address 0 Register** Ring buffer read scheme bottom address 0
14001108	SRC_END_1	32	**Source End Address 1 Register** Ring buffer read scheme bottom address 1
14001110	SRC_END_2	32	**Source End Address 2 Register** Ring buffer read scheme bottom address 2
14001118	SRC_OFFSET_0	32	**Source Address Offset 0 Register**

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Address	Name	Width	Register Function
			Source starting address offset from base 0
14001120	SRC_OFFSET_1	32	**Source Address Offset 1 Register** Source starting address offset from base 1
14001128	SRC_OFFSET_2	32	**Source Address Offset 2 Register** Source starting address offset from base 2
14001130	SRC_OFFSET_W_0	32	**Source Address Ring Buffer Start Offset 0 Register** Ring buffer read scheme source starting address offset from base 0 when roll-back
14001138	SRC_OFFSET_W_1	32	**Source Address Ring Buffer Start Offset 1 Register** Ring buffer read scheme source starting address offset from base 1 when roll-back
14001140	SRC_OFFSET_W_2	32	**Source Address Ring Buffer Start Offset 2 Register** Ring buffer read scheme source starting address offset from base 2 when roll-back
14001148	SRC_OFFSET_0_P	32	**Source Address Offset 0 in Pixel Register** Source starting address offset from base 0 in pixel
14001200	TRANSFORM_0	32	**Color Transform Control 0** Color transform control 0
14001208	TRANSFORM_1	32	**Color Transform Control 1** Color transform control 1
14001210	TRANSFORM_2	32	**Color Transform Control 2** Color transform control 2
14001218	TRANSFORM_3	32	**Color Transform Control 3** Color transform control 3
14001220	TRANSFORM_4	32	**Color Transform Control 4** Color transform control 4
14001228	TRANSFORM_5	32	**Color Transform Control 5** Color transform control 5
14001230	TRANSFORM_6	32	**Color Transform Control 6** Color transform control 6
14001238	TRANSFORM_7	32	**Color Transform Control 7** Color transform control 7
14001240	DMABUF_CON_0	32	**DMA Buffer 0 Control Register** Controls behavior of GMC DMA buffer 0 of rotator
14001248	DMAULTRA_CON_0	32	**DMA Buffer 0 Ultra Control Register** Controls behavior of GMC DMA buffer 0 ultra and pre-ultra of rotator
14001250	DMABUF_CON_1	32	**DMA Buffer 1 Control Register** Controls behavior of GMC DMA buffer 1 of rotator
14001258	DMAULTRA_CON_1	32	**DMA Buffer 1 Ultra Control Register** Controls behavior of GMC DMA buffer 1 ultra and pre-ultra of rotator
14001260	DMABUF_CON_2	32	**DMA Buffer 2 Control Register** Controls behavior of GMC DMA buffer 2 of rotator
14001268	DMAULTRA_CON_2	32	**DMA Buffer 2 Ultra Control Register** Controls behavior of GMC DMA buffer 2 ultra and pre-ultra of rotator
14001270	RESV_DUMMY_0	32	**Reserved Dummy Register** Reserved dummy register
14001300	CHKS_EXTR	32	**Checksum For EXT Read** Checksum for EXT read
14001308	CHKS_INTW	32	**Checksum For INT Writer** Checksum for INT write

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Address	Name	Width	Register Function
14001310	CHKS_INTR	32	**Checksum For INT Read** Checksum for INT read
14001318	CHKS_ROTO	32	**Checksum For Rotator Output**
14001320	CHKS_SRIY	32	**Checksum For SRAM Input Y** Checksum for SRAM input Y
14001328	CHKS_SRIU	32	**Checksum For SRAM Input U** Checksum for SRAM input U
14001330	CHKS_SRIV	32	**Checksum For SRAM Input V** Checksum for SRAM input V
14001338	CHKS_SROY	32	**Checksum For SRAM Output Y** Checksum for SRAM output Y
14001340	CHKS_SROU	32	**Checksum For SRAM Output U** Checksum for SRAM output U
14001348	CHKS_SROV	32	**Checksum For SRAM Output V** Checksum for SRAM output V
14001350	CHKS_VUPI	32	**Checksum For Vertical Upsample Input** Checksum for vertical upsample input
14001358	CHKS_VUPO	32	**Checksum For Vertical Upsample Output** Checksum for vertical upsample output
14001380	DEBUG_CON	32	**Debug Control** Controls debugging
14001400	MON_STA_0	32	**Monitor For Status 0** Monitors status 0
14001408	MON_STA_1	32	**Monitor For Status 1** Monitors status 1
14001410	MON_STA_2	32	**Monitor For Status 2** Monitors status 2
14001418	MON_STA_3	32	**Monitor For Status 3** Monitors status 3
14001420	MON_STA_4	32	**Monitor For Status 4** Monitors status 4
14001428	MON_STA_5	32	**Monitor For Status 5** Monitors status 5
14001430	MON_STA_6	32	**Monitor For Status 6** Monitors status 6
14001438	MON_STA_7	32	**Monitor For Status 7** Monitors status 7
14001440	MON_STA_8	32	**Monitor For Status 8** Monitors status 8
14001448	MON_STA_9	32	**Monitor For Status 9** Monitors status 9
14001450	MON_STA_10	32	**Monitor For Status 10** Monitors status 10
14001458	MON_STA_11	32	**Monitor For Status 11** Monitors status 11
14001460	MON_STA_12	32	**Monitor For Status 12** Monitors status 12
14001468	MON_STA_13	32	**Monitor For Status 13** Monitors status 13
14001470	MON_STA_14	32	**Monitor For Status 14** Monitors status 14

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Address	Name	Width	Register Function
14001478	MON_STA_15	32	**Monitor For Status 15** Monitors status 15
14001480	MON_STA_16	32	**Monitor For Status 16** Monitors status 16
14001488	MON_STA_17	32	**Monitor For Status 17** Monitors status 17
14001490	MON_STA_18	32	**Monitor For Status 18** Monitors status 18
14001498	MON_STA_19	32	**Monitor For Status 19** Monitors status 19
140014A0	MON_STA_20	32	**Monitor For Status 20** Monitors status 20
140014A8	MON_STA_21	32	**Monitor For Status 21** Monitors status 21
140014B0	MON_STA_22	32	**Monitor For Status 22** Monitors status 22
140014B8	MON_STA_23	32	**Monitor For Status 23** Monitors status 23
140014C0	MON_STA_24	32	**Monitor For Status 24** Monitors status 24
140014C8	MON_STA_25	32	**Monitor For Status 25** Monitors status 25
140014D0	MON_STA_26	32	**Monitor For Status 26** Monitors status 26
14001F00	SRC_BASE_0	32	**Source Base Address 0 Register** Rotator source starting base address 0
14001F08	SRC_BASE_1	32	**Source Base Address 1 Register** Rotator source starting base address 1
14001F10	SRC_BASE_2	32	**Source Base Address 2 Register** Rotator source starting base address 2

14001000 EN Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name																ROT_ENABLE
Type																RW
Reset																0

Bit(s)	Name	Description
0	ROT_ENABLE	**Rotator enabling signal** Only 1 can be written. 0: No rotator operation 1: Rotator is enabled to rotate a frame.

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14001008 **RESET** **Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**WARM_RESET**
Type																A0
Reset																0

Bit(s)	Name	Description
0	WARM_RESET	**Resets rotator inner states after no pending bus transactions are left** Hardware will de-assert this signal after reset is done. 0: De-assert reset 1: Assert reset

14001010 **INTERRUPT_ENABLE** **Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**UNDERRUN_INT_EN**	**REG_UPDATE_INT_EN**	**FRAME_COMPLETE_INT_EN**
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	UNDERRUN_INT_EN	**Enables rotator under-run interrupt** 0: Disable 1: Enable
1	REG_UPDATE_INT_EN	**Enables rotator register updated interrupt** 0: Disable 1: Enable
0	FRAME_COMPLETE_INT_EN	**Enables rotator frame completed interrupt** 0: Disable 1: Enable

14001018 **INTERRUPT_STATUS** **Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

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Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														UNDERRUN_INT	REG_UPDATE_INT	FRAME_COMPLETE_INT
Type														RU	RU	RU
Reset														0	0	0

Bit(s)	Name	Description
2	UNDERRUN_INT	**Rotator under-run interrupt** SW can only write 0 to clear the interrupt. Writing 1 is ineffective.
1	REG_UPDATE_INT	**Rotator register updated interrupt** SW can only write 0 to clear the interrupt. Writing 1 is ineffective.
0	FRAME_COMPLETE_INT	**Rotator frame completed interrupt** SW can only write 0 to clear the interrupt. Writing 1 is ineffective.

14001020 CON Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				LB_2B_MODE				BUFFER_MODE				SIMPLE_MODE				
Type				RW				RW				RW				
Reset				0				0				0				

Bit(s)	Name	Description
12	LB_2B_MODE	**Enables line-buffer (2) byte write merge mode to improve performance and reduce BW waste** Only works for scan-line source since they are the worst case compared to block source. 0: Disable 1: Enable
8	BUFFER_MODE	**Enables buffer mode** When buffer mode is 1, rotator will use a little more buffer to enhance performance. 0: Disable 1: Enable
4	SIMPLE_MODE	**MDP_RDMA simple configure mode.** 0: turn off simple mode. 1: turn on simple mode.

14001028 GMCIF_CON GMC Interface Control Register 00000330

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	THROTTLE_PERIOD												THROTTLE_		PRE_ULTRA_EN	

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													EN			
Type	RW												RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**ULTRA_EN**			**WRITE_REQUEST_TYPE**				**READ_REQUEST_TYPE**						**COMMAND_DIV**
Type			RW			RW				RW						RW
Reset			0	0		0	1	1		0	1	1				0

Bit(s)	Name	Description
31:20	THROTTLE_PERIOD	**Period of throttle control** Delayed cycles between two requests is 4*THROTTLE_PERIOD.
19	THROTTLE_EN	**Controls throttle of rotator** When it is enabled, cycles between two requests will be throttled by the value of THROTTLE_PERIOD. 0: Disable 1: Enable
17:16	PRE_ULTRA_EN	**Enables pre_ultra high request for read port** 0: Disable 1: Enable according to ultra_th_low/ultra_th_high 2: Always enable 3: Reserved
13:12	ULTRA_EN	**Enables ultra high request for read port** 0: Disable 1: Enable according to ultra_th_low/ultra_th_high 2: Always enable 3: Reserved
10:8	WRITE_REQUEST_TYPE	**Controls maximum request burst length** 0: Single access 1: Burst 2 access 2: Burst 3 access 3: Burst 4 access 4: Burst 5 access 5: Burst 6 access 6: Burst 7 access 7: Burst 8 access
6:4	READ_REQUEST_TYPE	**Controls maximum request burst length** The real burst length is according to the rotation. 0: Single access 1: Burst 2 access 2: Burst 3 access 3: Burst 4 access 4: Burst 5 access 5: Burst 6 access 6: Burst 7 access 7: Burst 8 access
0	COMMAND_DIV	**Controls if command across 256-byte boundary needs to be divided to 2 separate commands** 0: No division 1: Division is necessary.

14001030 SRC_CON Source Control Register 000A0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**TOP**	**BOT**	**LEF**	**RIG**				**RIN**				**BYT**	**UFO**	**UFO**	**UNI**	**IS_Y**

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	_BOUNDARY	_BOUNDARY	T_BOUNDARY	HT_BOUNDARY				G_BUF_READ				E_SWAP	_DATA_IN_NOT_REV	_DATA_OUT_NOT_REV	FORM_CONFIG	_LSB
Type	RW	RW	RW	RW				RW				RW	RW	RW	RW	RW
Reset	0	0	0	0				0				0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BLOCK	SWAP	VDO_FIELD	VDO_MODE		CUS_REP		COSITE	RGB_PAD	SRC_SWAP			SRC_FORMAT			
Type	RW	RW	RW	RW		RW		RW	RW	RW			RW			
Reset	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TOP_BOUNDARY	**If the boundary is the entire frame boundary, upsample filter of boundary-pixels will be processed with boundary repeated. If the boundary is simply tile boundary, upsample filter of the boundary-pixels will be processed with the adjacent line or pixel.** 0: The top boundary of the current tile is the tile boundary. 1: The top boundary of the current tile is the frame boundary.
30	BOT_BOUNDARY	**If the boundary is the entire frame boundary, upsample filter of boundary-pixels will be processed with boundary repeated. If the boundary is simply tile boundary, upsample filter of the boundary-pixels will be processed with the adjacent line or pixel.** 0: The bottom boundary of the current tile is the tile boundary. 1: The bottom boundary of the current tile is the frame boundary.
29	LEFT_BOUNDARY	**If the boundary is the whole frame boundary, upsample filter of the boundary-pixels will be processed with boundary repeated. If the boundary is just a tile boundary, upsample filter of the boundary-pixels will be processed with the adjacent line or pixel.** 0: The left boundary of the current tile is the tile boundary. 1: The left boundary of the current tile is the frame boundary
28	RIGHT_BOUNDARY	**If the boundary is the entire frame boundary, upsample filter of boundary-pixels will be processed with boundary repeated. If the boundary is simply tile boundary, upsample filter of the boundary-pixels will be processed with the adjacent line or pixel.** 0: The right boundary of the current tile is the tile boundary. 1: The right boundary of the current tile is the frame boundary.
24	RING_BUF_READ	**Enables ring buffer read scheme** 0: Off. Normal read 1: Ring buffer read on. Address will be turned around between SRC_BASE + SRC_OFFSET and SRC_END.
20	BYTE_SWAP	**Only when legacy mode and src_format = RGB565 will this bit take effect.** 0: Little-endian input. 1: Big-endian input; do byte swap for input.
19	UFO_DATA_IN_NOT_REV	**Only works in UFO mode** Do not modify this bit. 0: Reverse the byte order of the UFO core input data 1: Does not reverse the byte order of the UFO core input data
18	UFO_DATA_OUT_NOT_REV	**Only works in UFO mode** Do not modify this bit. 0: Reverse the byte order of the UFO core output data 1: Does not reverse the byte order of the UFO core output data
17	UNIFORM_CONFIG	**Swaps between uniform config mode and legacy mode** Do not modify this bit.

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Bit(s)	Name	Description
		0: Legacy mode 1: Uniform config
16	IS_Y_LSB	**Only when legacy mode and src_format = 422_I_SW will this bit take effect** 0: Y is packed in MSB byte. 1: Y is packed in LSB byte.
15	BLOCK	**Only works in uniform confing mode** 0: Raster scan mode 1: Block mode
14	SWAP	**Only works in uniform config mode** 0: No swap 1: Swap
13	VDO_FIELD	**Only when VDO_MODE is set to 1 will the bit take effect.** 0: Top field 1: Bottom field
12	VDO_MODE	**Only when source format is HW video block YCbCr_420_SP will the bit take effect.** 0: Frame mode 1: Field mode
10:9	CUS_REP	**UV horizontal sample method** 0: Filter 1: V repeat, H filter 2: H repeat, V filter 3: No V/H filter; will repeat the data
8	COSITE	**UV horizontal sample position for YUV420** 0: Non-cosited 1: Cosited
7	RGB_PAD	**Rotator RGB565 padding option** 0: Padding MSB 1: Padding 0
6:4	SRC_SWAP	**Only works in legacy mode.** Rotator YUV/RGB source swap. If the source is YUV/RGB order, then output can be re-order as: 0: YUV/RGB 1: VUY/BGR, R/B swap 2: YVU/RBG, U/V swap 3: UVY/GBR 4: UYV/GRB 5: VYU/BRG
3:0	SRC_FORMAT	**Rotator source frame format** 0: RGB565 1: RGB888 2: BGRA8888 3: ARGB8888 4: UYVY 5: YUY2 7: Y8 8: I420 (YV12) 9: I422 (YV16) 10: YV24 12: NV12 13: NV16 14: NV24

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14001060	MF_BKGD_SIZE_IN_BYTE	Main Frame Background Size In Byte Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												MF_BKGD_WB[20:16]				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MF_BKGD_WB[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	MF_BKGD_WB	**Rotator main frame background width in byte** Please enter the pitch of the main frame.

14001068	MF_BKGD_SIZE_IN_PXL	Main Frame Background Size In Pixel Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												MF_BKGD_WP[20:16]				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MF_BKGD_WP[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	MF_BKGD_WP	**Rotator main frame background width in pixel** Please enter the pixel number of the main frame. Only used in 10-bit mode.

14001070	MF_SRC_SIZE	Main Frame Source Size Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MF_SRC_H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				MF_SRC_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	MF_SRC_H	**Rotator main frame source height** If its value is H, there will be H lines in a frame.
12:0	MF_SRC_W	**Rotator main frame source width** If its value is W, there will be W pixels in a line.

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14001078 **MF_CLIP_SIZE** **Main Frame Clip Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MF_CLIP_H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				MF_CLIP_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	MF_CLIP_H	**Rotator main frame clip height** If its value is H, there will be H lines in a frame.
12:0	MF_CLIP_W	**Rotator main frame clip width** If its value is W, there will be W pixels in a line.

14001080 **MF_OFFSET_1** **Main Frame Offset 1 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											MF_OFFSET_H_1					
Type											RW					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												MF_OFFSET_W_1				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
21:16	MF_OFFSET_H_1	Rotator main frame height offset
4:0	MF_OFFSET_W_1	Rotator main frame width offset

14001088 **MF_PAR** **Main Frame Parameter Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MF_SB[16:4]												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MF_SB[3:0]						MF_JUMP									
Type	RW						RW									
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:12	MF_SB	**Rotator main frame seg size in byte.** No need to configure this parameter in simple mode.
9:0	MF_JUMP	**Rotator main frame jump in byte.** No need to configure this parameter in simple mode.

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14001090 **SF_BKGD_SIZE_IN_BYTE** **Sub Frame Background Size In Byte Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												SF_BKGD_WB[20:16]				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SF_BKGD_WB[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	SF_BKGD_WB	**Rotator sub frame background width in byte** Please enter the pitch of the sub frame.

140010B8 **SF_PAR** **Sub Frame Parameter Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				SF_SB[16:4]												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SF_SB[3:0]						SF_JUMP									
Type	RW						RW									
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:12	SF_SB	**Rotator sub frame seg size in byte** No need to configure this parameter in simple mode.
9:0	SF_JUMP	**Rotator sub frame jump in byte** No need to configure this parameter in simple mode.

140010C0 **MB_DEPTH** **Main Line Buffer Depth Control Register** **00000010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										MB_DEPTH						
Type										RW						
Reset										0	0	1	0	0	0	0

Bit(s)	Name	Description
6:0	MB_DEPTH	**Rotator main buffer depth** The min. value is 2 and max. 8. No need to configure this parameter in simple mode.

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140010C8 MB_BASE Main Buffer Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MB_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	MB_BASE	**Rotator main buffer base address** The buffer size should be"RGB565: MB_LP*(SB_DEPTH + BUFFER_MODE)*2. Others: MB_LP*(SB_DEPTH + BUFFER_MODE) For MT6583/6517, set it to 0.

140010D0 MB_CON Main Line Buffer Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			MB_LP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				MB_PPS												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	MB_LP	**Rotator main buffer line pixel** No need to configure this parameter in simple mode.
12:0	MB_PPS	**Rotator main buffer pixel number per segment** It is equal to MB_LP/(MB_DEPTH + BUFFER_MODE).

140010D8 SB_DEPTH Sub Line Buffer Depth Control Register 00000010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SB_DEPTH						
Type										RW						
Reset										0	0	1	0	0	0	0

Bit(s)	Name	Description
6:0	SB_DEPTH	**Rotator sub buffer depth** The min. value is 2 and max. 8. No need to configure this parameter in simple mode.

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140010E0 SB_BASE Sub Buffer Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SB_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SB_BASE	**Rotator sub buffer base address** Valid for all modes except for RGB565. The buffer size should be SB_LP*(SB_DEPTH + BUFFER_MODE)*2. For MT6583/MT6517: RGB565: 0x0 VDO 420 && vertical rotate: 0x5600 Others: 0x4400

140010E8 SB_CON Sub Line Buffer Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SB_LP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				SB_PPS												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	SB_LP	**Rotator sub buffer line pixel** No need to configure this parameter in simple mode.
12:0	SB_PPS	**Rotator sub buffer pixel number per segment** It is equal to SB_LP/(SB_DEPTH + BUFFER_MODE).

140010F0 VC1_RANGE VC1 Range Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												VC1_MAP_PARA_C				
Type												RW				
Reset												0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				VC1_MAP_PARA_Y								VC1_MAP_EN				VC1_RED_EN
Type				RW								RW				RW
Reset				0	0	0	0	0				0				0

Bit(s)	Name	Description
20:16	VC1_MAP_PARA_C	**VC1 range mapping parameter for C** Range: N+9 (N = 0~7) 0: Disable

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Bit(s)	Name	Description
		1: Enable
12:8	VC1_MAP_PARA_Y	**VC1 range mapping parameter for Y** Range: N+9 (N = 0~7)
4	VC1_MAP_EN	**VC1 range mapping enable** 0: Disable 1: Enable
0	VC1_RED_EN	**VC1 range reduction enable** 0: Disable 1: Enable

14001100 SRC_END_0 Source End Address 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_END_0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_END_0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_END_0	**Ring buffer read scheme bottom address 0** SRC_BASE_0 <= read ptr < SRC_END_0

14001108 SRC_END_1 Source End Address 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_END_1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_END_1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_END_1	**Ring buffer read scheme bottom address 1** SRC_BASE_1 <= read ptr < SRC_END_1

14001110 SRC_END_2 Source End Address 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_END_2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_END_2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	SRC_END_2	**Ring buffer read scheme bottom address 2** SRC_BASE_2 <= read ptr < SRC_END_2

14001118 SRC_OFFSET_0 Source Address Offset 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_OFFSET_0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_OFFSET_0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_OFFSET_0	Source starting address = SRC_BASE_0 + SRC_OFFSET_0

14001120 SRC_OFFSET_1 Source Address Offset 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_OFFSET_1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_OFFSET_1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_OFFSET_1	Source starting address = SRC_BASE_1 + SRC_OFFSET_1

14001128 SRC_OFFSET_2 Source Address Offset 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_OFFSET_2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_OFFSET_2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_OFFSET_2	Source starting address = SRC_BASE_2 + SRC_OFFSET_2

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14001130	SRC_OFFSET_W_0	Source Address Ring Buffer Start Offset 0 Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_OFFSET_W_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SRC_OFFSET_W_0	In ring buffer mode, address will roll back to SRC_BASE0 + SRC_OFFSET_W_0 when crossing SRC_END0.

14001138	SRC_OFFSET_W_1	Source Address Ring Buffer Start Offset 1 Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_OFFSET_W_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SRC_OFFSET_W_1	In ring buffer mode, address will roll back to SRC_BASE1 + SRC_OFFSET_W_1 when crossing SRC_END1.

14001140	SRC_OFFSET_W_2	Source Address Ring Buffer Start Offset 2 Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_OFFSET_W_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SRC_OFFSET_W_2	In ring buffer mode, address will roll back to SRC_BASE2 + SRC_OFFSET_W_2 when crossing SRC_END2.

14001148	SRC_OFFSET_0_P	Source Address Offset 0 in Pixel Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	SRC_OFFSET_0_P[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_OFFSET_0_P[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_OFFSET_0_P	**Source starting address offset** Unit: Pixel

14001200 **TRANSFORM_0** **Color Transform Control 0** **00010660**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					int_matrix_sel							ext_matrix_en				TRANS_EN
Type					RW							RW				RW
Reset					0	0	0	0				0				1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						OUT_S_2	OUT_S_1	OUT_S_0		CLAMP_S_2	CLAMP_S_1	CLAMP_S_0		IN_S_2	IN_S_1	IN_S_0
Type						RW	RW	RW		RW	RW	RW		RW	RW	RW
Reset						1	1	0		1	1	0		0	0	0

Bit(s)	Name	Description
27:24	int_matrix_sel	**If ext_matrix_en = 0, select build-in matrix table** 4'b0000: RGB to JPEG 4'b0010: RGB to BT601 4'b0011: RGB to BT709 4'b0100: JPEG to RGB 4'b0110: BT601 to RGB 4'b0111: BT709 to RGB 4'b1000: JPEG to BT601 4'b1001: JPEG to BT709 4'b1010: BT601 to JPEG 4'b1011: BT709 to JPEG 4'b1100: BT709 to BT601 4'b1101: BT601 to BT709 Others: Reserved
20	ext_matrix_en	**Selects external matrix with programmable coefficient** 0: Use internal build-in matrix table 1: Use programmable coefficients
16	TRANS_EN	**Transform function enabling control** 0: Disable 1: Enable
10	OUT_S_2	**Output sign 2**
9	OUT_S_1	**Output sign 1**
8	OUT_S_0	**Output sign 0**
6	CLAMP_S_2	**Clamping sign 2**
5	CLAMP_S_1	**Clamping sign 1**
4	CLAMP_S_0	**Clamping sign 0**

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Bit(s)	Name	Description
2	IN_S_2	**Input sign 2**
1	IN_S_1	**Input sign 1**
0	IN_S_0	**Input sign 0**

14001208 TRANSFORM_1 Color Transform Control 1 18060000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				IN_OFFSET_2										IN_OFFSET_1[8:6]		
Type				RW										RW		
Reset				1	1	0	0	0	0	0	0	0		1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IN_OFFSET_1[5:0]							IN_OFFSET_0								
Type	RW							RW								
Reset	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:20	IN_OFFSET_2	Input offset 2
18:10	IN_OFFSET_1	Input offset 1
8:0	IN_OFFSET_0	Input offset 0

14001210 TRANSFORM_2 Color Transform Control 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				OUT_OFFSET_2										OUT_OFFSET_1[8:6]		
Type				RW										RW		
Reset				0	0	0	0	0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OUT_OFFSET_1[5:0]							OUT_OFFSET_0								
Type	RW							RW								
Reset	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:20	OUT_OFFSET_2	Output offset 2
18:10	OUT_OFFSET_1	Output offset 1
8:0	OUT_OFFSET_0	Output offset 0

14001218 TRANSFORM_3 Color Transform Control 3 00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_01												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_00												
Type				RW												

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Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	C_01	**Transform coefficient 01, s2.10** Value range: -4 ~ 3.99
12:0	C_00	**Transform coefficient 00, s2.10** Value range: -4 ~ 3.99

14001220 TRANSFORM_4 Color Transform Control 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_10												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_02												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	C_10	**Transform coefficient 10, s2.10** Value range: -4 ~ 3.99
12:0	C_02	**Transform coefficient 02, s2.10** Value range: -4 ~ 3.99

14001228 TRANSFORM_5 Color Transform Control 5 00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_12												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_11												
Type				RW												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	C_12	**Transform coefficient 12, s2.10** Value range: -4 ~ 3.99
12:0	C_11	**Transform coefficient 11, s2.10** Value range: -4 ~ 3.99

14001230 TRANSFORM_6 Color Transform Control 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_21												
Type				RW												

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Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**C_20**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	C_21	**Transform coefficient 21, s2.10** Value range: -4 ~ 3.99
12:0	C_20	**Transform coefficient 20, s2.10** Value range: -4 ~ 3.99

14001238 TRANSFORM_7 Color Transform Control 7 00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**C_22**												
Type				RW												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	C_22	**Transform coefficient 22, s2.10** Value range: -4 ~ 3.99

14001240 DMABUF_CON_0 DMA Buffer 0 Control Register 03000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						**EXTRD_ARB_MAX_0**				**BUF_RESV_SIZE_0**						
Type						RW				RW						
Reset						0	1	1		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**ISSUE_REQ_TH_0**						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	EXTRD_ARB_MAX_0	**Maximum outstanding ability for DMA buffer 0** 0-7 denotes outstanding number 1-8.
22:16	BUF_RESV_SIZE_0	**Buffer size reserved for overflow prevention and FIFO size testing** fifo_pseudo_size = (fifo_real_size-buf_resv_size)
6:0	ISSUE_REQ_TH_0	**Issues normal requests when FIFO valid data <= fifo_pseudo_size - issue_req_th and keeps issuing requests until valid data in command phase = fifo_pseudo_size**

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14001248 **DMAULTRA_CON_0** **DMA Buffer 0 Ultra Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		PRE_ULTRA_TH_HIGH_OFS_0								ULTRA_TH_HIGH_OFS_0						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PRE_ULTRA_TH_LOW_OFS_0								ULTRA_TH_LOW_0						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	PRE_ULTRA_TH_HIGH_OFS_0	**pre_ultra_th_high = ultra_th_high + pre_ultra_th_high_ofs**
22:16	ULTRA_TH_HIGH_OFS_0	**ultra_th_high = pre_ultra_th_low + ultra_th_high_ofs**
14:8	PRE_ULTRA_TH_LOW_OFS_0	**pre_ultra_th_low = ultra_th_low + pre_ultra_th_low_ofs** Issues pre-ultra high requests when FIFO valid data <= pre_ultra_th_low and keeps it asserted until FIFO valid data >= pre_ultra_th_high
6:0	ULTRA_TH_LOW_0	**Issues ultra high requests when FIFO valid data <= ultra_th_low** and keeps it asserted until FIFO valid data >= ultra_th_high

14001250 **DMABUF_CON_1** **DMA Buffer 1 Control Register** **03000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						EXTRD_ARB_MAX_1					BUF_RESV_SIZE_1					
Type						RW					RW					
Reset						0	1	1			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											ISSUE_REQ_TH_1					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
26:24	EXTRD_ARB_MAX_1	**Maximum outstanding ability for DMA buffer 1** 0-7 denotes outstanding number 1-8.
21:16	BUF_RESV_SIZE_1	**Buffer size reserved for overflow prevention and FIFO size testing** fifo_pseudo_size = (fifo_real_size-buf_resv_size)
5:0	ISSUE_REQ_TH_1	**Issues normal requests when FIFO valid data <= fifo_pseudo_size - issue_req_th and keeps issuing requests until valid data in command phase = fifo_pseudo_size**

14001258 **DMAULTRA_CON_1** **DMA Buffer 1 Ultra Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			PRE_ULTRA_TH_HIGH_OFS_1								ULTRA_TH_HIGH_OFS_1					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name			PRE_ULTRA_TH_LOW_OFS_1								ULTRA_TH_LOW_1					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
29:24	PRE_ULTRA_TH_HIGH_OFS_1	**pre_ultra_th_high = ultra_th_high + pre_ultra_th_high_ofs**
21:16	ULTRA_TH_HIGH_OFS_1	**ultra_th_high = pre_ultra_th_low + ultra_th_high_ofs**
13:8	PRE_ULTRA_TH_LOW_OFS_1	**pre_ultra_th_low = ultra_th_low + pre_ultra_th_low_ofs** Issues pre-ultra high requests when FIFO valid data <= pre_ultra_th_low and keeps it asserted until FIFO valid data >= pre_ultra_th_high
5:0	ULTRA_TH_LOW_1	**Issues ultra high requests when FIFO valid data <= ultra_th_low,** and keeps it asserted until FIFO valid data >= ultra_th_high

14001260 DMABUF_CON_2 DMA Buffer 2 Control Register 03000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						EXTRD_ARB_MAX_2						BUF_RESV_SIZE_2				
Type						RW						RW				
Reset						0	1	1				0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name												ISSUE_REQ_TH_2				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
26:24	EXTRD_ARB_MAX_2	**Maximum outstanding ability for DMA buffer 2** 0-7 denotes outstanding number 1-8.
20:16	BUF_RESV_SIZE_2	**Buffer size reserved for overflow prevention and FIFO size testing** fifo_pseudo_size = (fifo_real_size-buf_resv_size)
4:0	ISSUE_REQ_TH_2	**Issues normal requests when FIFO valid data <= fifo_pseudo_size - issue_req_th and keeps issuing requests until valid data in command phase = fifo_pseudo_size**

14001268 DMAULTRA_CON_2 DMA Buffer 2 Ultra Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				PRE_ULTRA_TH_HIGH_OFS_2								ULTRA_TH_HIGH_OFS_2				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				PRE_ULTRA_TH_LOW_OFS_2								ULTRA_TH_LOW_2				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
28:24	PRE_ULTRA_TH_	**pre_ultra_th_high = ultra_th_high + pre_ultra_th_high_ofs**

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Bit(s)	Name	Description
	HIGH_OFS_2	
20:16	ULTRA_TH_HIGH_OFS_2	**ultra_th_high = pre_ultra_th_low + ultra_th_high_ofs**
12:8	PRE_ULTRA_TH_LOW_OFS_2	**pre_ultra_th_low = ultra_th_low + pre_ultra_th_low_ofs** Issues pre-ultra high requests when FIFO valid data <= pre_ultra_th_low and keeps it asserted until FIFO valid data >= pre_ultra_th_high
4:0	ULTRA_TH_LOW_2	**Issues ultra high requests when FIFO valid data <= ultra_th_low** and keeps it asserted until FIFO valid data >= ultra_th_high

14001270 RESV_DUMMY_0 Reserved Dummy Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_DUMMY_0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_DUMMY_0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_DUMMY_0	**Dummy register** Reserved

14001300 CHKS_EXTR Checksum For EXT Read 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKS_EXTR_CRC[23:8]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKS_EXTR_CRC[7:0]															CHKS_EXTR_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_EXTR_CRC	Checksum result for external (EMI) read data
0	CHKS_EXTR_CLR	Clears checksum to 0

14001308 CHKS_INTW Checksum For INT Writer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKS_INTW_CRC[23:8]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	**CHKS_INTW_CRC[7:0]**															**CHKS_INTW_CLR**
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_INTW_CRC	Checksum result for internal (SYSRAM) write data
0	CHKS_INTW_CLR	Clears checksum to 0

14001310 CHKS_INTR Checksum For INT Read 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CHKS_INTR_CRC[23:8]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CHKS_INTR_CRC[7:0]**															**CHKS_INTR_CLR**
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_INTR_CRC	Checksum result for internal (SYSRAM) read data
0	CHKS_INTR_CLR	Clears checksum to 0

14001318 CHKS_ROTO Checksum For Rotator Output 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CHKS_ROTO_CRC[23:8]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CHKS_ROTO_CRC[7:0]**															**CHKS_ROTO_CLR**
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_ROTO_CRC	Checksum result for rotator output data to SCL
0	CHKS_ROTO_CLR	Clears checksum to 0

14001320 CHKS_SRIY Checksum For SRAM Input Y 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CHKS_SRIY_CRC[23:8]**															

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Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CHKS_SRIY_CRC[7:0]**															**CHKS_SRIY_CLR**
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_SRIY_CRC	Checksum result for EMI data buffer SRAM input Y
0	CHKS_SRIY_CLR	Clears checksum to 0

14001328 CHKS_SRIU Checksum For SRAM Input U 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CHKS_SRIU_CRC[23:8]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CHKS_SRIU_CRC[7:0]**															**CHKS_SRIU_CLR**
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_SRIU_CRC	Checksum result for EMI data buffer SRAM input U
0	CHKS_SRIU_CLR	Clears checksum to 0

14001330 CHKS_SRIV Checksum For SRAM Input V 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CHKS_SRIV_CRC[23:8]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CHKS_SRIV_CRC[7:0]**															**CHKS_SRIV_CLR**
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_SRIV_CRC	Checksum result for EMI data buffer SRAM input V
0	CHKS_SRIV_CLR	Clears checksum to 0

14001338 CHKS_SROY Checksum For SRAM Output Y 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CHKS_SROY_CRC[23:8]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CHKS_SROY_CRC[7:0]**															**CHKS_SROY_CLR**
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_SROY_CRC	Checksum result for EMI data buffer SRAM output Y
0	CHKS_SROY_CLR	Clears checksum to 0

14001340 CHKS_SROU Checksum For SRAM Output U 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CHKS_SROU_CRC[23:8]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CHKS_SROU_CRC[7:0]**															**CHKS_SROU_CLR**
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_SROU_CRC	Checksum result for EMI data buffer SRAM output U
0	CHKS_SROU_CLR	Clears checksum to 0

14001348 CHKS_SROV Checksum For SRAM Output V 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CHKS_SROV_CRC[23:8]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CHKS_SROV_CRC[7:0]**															**CHKS_SROV_CLR**
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_SROV_CRC	Checksum result for EMI data buffer SRAM output V
0	CHKS_SROV_CLR	Clears checksum to 0

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14001350 CHKS_VUPI Checksum For Vertical Upsample Input 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKS_VUPI_CRC[23:8]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKS_VUPI_CRC[7:0]															CHKS_VUPI_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_VUPI_CRC	Checksum result for vertical chroma upsample line buffer (SRAM) input
0	CHKS_VUPI_CLR	Clears checksum to 0

14001358 CHKS_VUPO Checksum For Vertical Upsample Output 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKS_VUPO_CRC[23:8]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKS_VUPO_CRC[7:0]															CHKS_VUPO_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_VUPO_CRC	Checksum result for vertical chroma upsample line buffer (SRAM) output
0	CHKS_VUPO_CLR	Clears checksum to 0

14001380 DEBUG_CON Debug Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				debug_out_sel								CHKS_TRB_SEL				CHKS_CRC_EN
Type				RW								RW				RW
Reset				0	0	0	0	0				0				0

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Bit(s)	Name	Description
12:8	debug_out_sel	**Debugging output sel 0-22 mapped to MON_STA0-22**
4	CHKS_TRB_SEL	**Controls all checksum registers** 0: CHKS_INTW/CHKS_INTR sel transpose buffer 0 1: CHKS_INTW/CHKS_INTR sel transpose buffer 1
0	CHKS_CRC_EN	**Controls all checksum registers** 0: Disable. Default to omit power consumption 1: Enable checksum for debugging

14001400 MON_STA_0 Monitor For Status 0 00000810

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_0[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_0[15:0]															
Type	RU															
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_0	Monitor mdp_rdma status

14001408 MON_STA_1 Monitor For Status 1 00600101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_1[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_1[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:0	MON_STA_1	Monitor mdp_rdma status

14001410 MON_STA_2 Monitor For Status 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_2[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_2[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_2	Monitor mdp_rdma status

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14001418 MON_STA_3 Monitor For Status 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_3[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_3[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_3	Monitor mdp_rdma status

14001420 MON_STA_4 Monitor For Status 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_4[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_4[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_4	Monitor mdp_rdma status

14001428 MON_STA_5 Monitor For Status 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_5[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_5[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_5	Monitor mdp_rdma status

14001430 MON_STA_6 Monitor For Status 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_6[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_6[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	MON_STA_6	Monitor mdp_rdma status

14001438 MON_STA_7 Monitor For Status 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_7[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_7[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_7	Monitor mdp_rdma status

14001440 MON_STA_8 Monitor For Status 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_8[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_8[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_8	Monitor mdp_rdma status

14001448 MON_STA_9 Monitor For Status 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_9[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_9[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_9	Monitor mdp_rdma status

14001450 MON_STA_10 Monitor For Status 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	**MON_STA_10[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MON_STA_10[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_10	Monitor mdp_rdma status

14001458 MON_STA_11 Monitor For Status 11 00002000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MON_STA_11[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MON_STA_11[15:0]**															
Type	RU															
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_11	Monitor mdp_rdma status

14001460 MON_STA_12 Monitor For Status 12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MON_STA_12[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MON_STA_12[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_12	Monitor mdp_rdma status

14001468 MON_STA_13 Monitor For Status 13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MON_STA_13[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MON_STA_13[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	MON_STA_13	Monitor mdp_rdma status

14001470 MON_STA_14 Monitor For Status 14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_14[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_14[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_14	Monitor mdp_rdma status

14001478 MON_STA_15 Monitor For Status 15 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_15[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_15[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_15	Monitor mdp_rdma status

14001480 MON_STA_16 Monitor For Status 16 00002000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_16[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_16[15:0]															
Type	RU															
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_16	Monitor mdp_rdma status

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14001488 **MON_STA_17** **Monitor For Status 17** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_17[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_17[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_17	Monitor mdp_rdma status

14001490 **MON_STA_18** **Monitor For Status 18** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_18[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_18[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_18	Monitor mdp_rdma status

14001498 **MON_STA_19** **Monitor For Status 19** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_19[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_19[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_19	Monitor mdp_rdma status

140014A0 **MON_STA_20** **Monitor For Status 20** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_20[31:16]															
Type	RU															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MON_STA_20[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_20	Monitor mdp_rdma status

140014A8 MON_STA_21 Monitor For Status 21 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MON_STA_21[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MON_STA_21[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_21	Monitor mdp_rdma status

140014B0 MON_STA_22 Monitor For Status 22 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MON_STA_22[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MON_STA_22[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:0	MON_STA_22	Monitor mdp_rdma status

140014B8 MON_STA_23 Monitor For Status 23 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MON_STA_23[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MON_STA_23[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

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Bit(s)	Name	Description
31:0	MON_STA_23	Monitor mdp_rdma status

140014C0 MON_STA_24 Monitor For Status 24 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MON_STA_24[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MON_STA_24[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:0	MON_STA_24	Monitor mdp_rdma status

140014C8 MON_STA_25 Monitor For Status 25 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MON_STA_25[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MON_STA_25[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:0	MON_STA_25	Monitor mdp_rdma status

140014D0 MON_STA_26 Monitor For Status 26 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MON_STA_26[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MON_STA_26[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:0	MON_STA_26	Monitor mdp_rdma status

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14001F00 SRC_BASE_0 Source Base Address 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_BASE_0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_BASE_0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_BASE_0	**Rotator source starting base address 0** Base address of the first plane of source frame. In 2- or 3-plane mode, the first plane should be Y plane.

14001F08 SRC_BASE_1 Source Base Address 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_BASE_1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_BASE_1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_BASE_1	**Rotator source starting base address 1** When the source frame has 2 or 3 planes, it represents the base address of the second plane. In 2-plane mode, the second plane should be UV plane. In 3-plane mode, the second plane should be U plane.

14001F10 SRC_BASE_2 Source Base Address 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_BASE_2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_BASE_2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_BASE_2	**Rotator source starting base address 2** When the source frame has 3 planes, it represents the base address of the third plane. The existing third plane should be V plane.

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6.7.5 Programming Guide

To enable MDP_RDMA to read a frame, SW can be programmed by the following method. Here we offer a quick example: With an YCbCr_420_P_SW 1920x1080 frame provided in DRAM, MDP_RDMA will try to clip it into 256x256 as the following example settings:

1. Release reset and enable all interrupt
   DISP_ROT_RESET = 0x0000_0000
   DISP_ROT_INTERRUPT_ENABLE = 0x0000_0007
2. Set up controls to determine the behavior of MDP_RDMA.
   DISP_ROT_CON = 0x0000_0000
3. Set up SMI configuration for performance issues.
   DISP_ROT_GMCIF_CON = 0x0000_1771
4. Set up input format.
   DISP_ROT_SRC_CON = 0x0000_0000
5. Set up base address 0 for the first plane of the source frame. If the source frame contains more than one plane, base address 1 and base address 2 should be set as well. Note that the offset of start address is relative to operations. Refer to appendix for the start address offset cases.
   DISP_ROT_SRC_BASE_0 = 0x0007_7880
   DISP_ROT_SRC_BASE_1 = 0x0080_6c40
   DISP_ROT_SRC_BASE_2 = 0x00A0_1040
6. Calculate the byte number of the line pitch. It is the distance from the first byte of the current line to the first byte of the next line. The value for sub frame is required for multiple planar source.
   DISP_ROT_MF_BKGD_SIZE_IN_BYTE = 0x0000_0780
   DISP_ROT_SF_BKGD_SIZE_IN_BYTE = 0x0000_0780
7. Set up the width and the height of the source frame before it is rotated.
   DISP_ROT_MF_SRC_SIZE = 0x0100_0100
8. Set up the clip size if necessary.
   DISP_ROT_MF_CLIP_SIZE = 0x0100_0100
9. Set up offset in source format if necessary.
   DISP_ROT_MF_OFFSET_1 = 0x0000_0000
10. Set up option for RGB to YUV color transform control registers and parameters if necessary.
    DISP_ROT_TRANSFORM_0 = 0x0000_0000
11. Assert ROTEN to enable MDP_RDMA to wait for update of the shadow register.
    DISP_ROT_EN = 0x0000_0001
12. Assert register update to start operation of MDP_RDMA. This control signal comes from dispsys mutex control.

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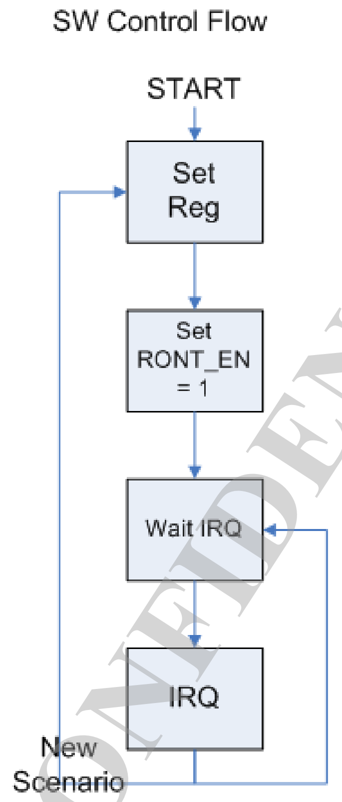

Figure 6-12. SW control flow

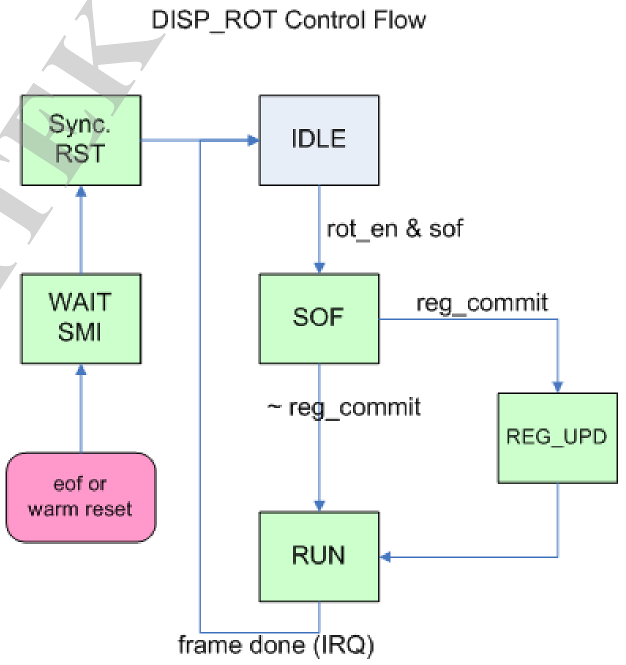

Figure 6-13. HW FSM and mutex control flow

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6.8 MDP RSZ

6.8.1 Introduction

There are two resizer modules for MT6735 MDP, including MDP_RSZ0 and MDP_RSZ1. The algorithm of each may be slightly different for different project requirements. The table lists the corresponding algorithm spec. Table 6-3 shows the functional specification of MDP_RSZ0 and MDP_RSZ1. MDP_RSZ0 and MDP_RSZ1 scale for multiple purposes in MDP 2.0 structure, mainly for generating image for display, video codec, jpeg codec and FD. Digital zoom is accomplished by MDP_RSZ0 or MDP_RSZ1 in MDP 2.0. MDP_RSZ0 and MDP_RSZ1 supports YUV444 input and YUV444 output.

Table 6-4 shows the hardware specifications of MDP_RSZ0 and MDP_RSZ1. They support three scaling algorithms including 6-tap FIR, 4n-tap cubic accumulation and n-tap source accumulation. The maximum image width is 544.

Table 6-3. Functional specifications of resizers

	MDP_RSZ0	MDP_RSZ1
Input data format	8-bit YUV444 (unsigned)	8-bit YUV444 (unsigned)
Output data format	8-bit YUV444 (unsigned)	8-bit YUV444 (unsigned)
Scaling ratio	Between 1/128x and 64x	Between 1/128x and 64x
Crop function	Supported	Supported
Function	1. Digital zoom 2. MDP general-purpose resizing	1. Digital zoom 2. MDP general-purpose resizing
Supported width (OTF)	N/A	N/A
Supported width (tile mode)	6tap: 544 ntap: 544 4ntap:272	6tap: 544 ntap: 544 4ntap:272

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Table 6-4. Hardware specifications of resizers

	MDP_RSZ0	MDP_RSZ1
Luma interpolation method (H)	(1) 6 tap FIR (2) 4n tap CA (3) n tap SA	(1) 6 tap FIR (2) 4n tap CA (3) n tap SA
Luma interpolation method (V)	(1) 6 tap FIR (2) 4n tap CA (3) n tap SA	(1) 6 tap FIR (2) 4n tap CA (3) n tap SA
Chroma interpolation method (H)	(1) 6 tap FIR (2) 2n tap TA (3) n tap SA	(1) 6 tap FIR (2) 2n tap TA (3) n tap SA
Chroma interpolation method (V)	(1) 6 tap FIR (2) 2n tap TA (3) n tap SA	(1) 6 tap FIR (2) 2n tap TA (3) n tap SA
Interpolation order	H->V (xn tap) V->H (6 tap)	H->V (xn tap) V->H (6 tap)
Line buffer (frame mode)	N/A	N/A
Line buffer (tile mode)	272x48x6 (Logical) -> 136x96x6	272x48x6 (Logical) -> 136x96x6

6.8.2 Theory of Operations

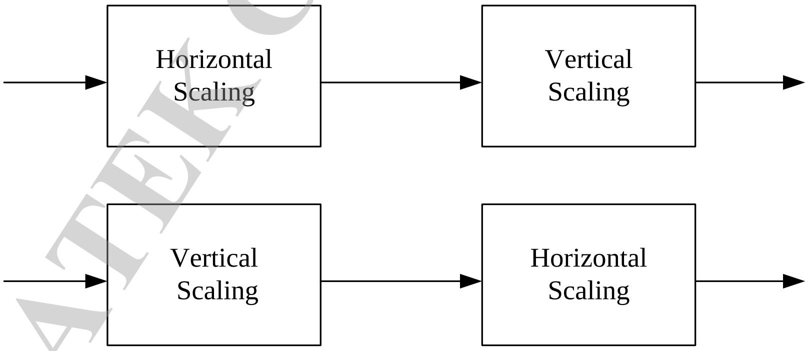

Figure 6-14. Separate 1D FIR operaiton

Basically, the rescaling procedure is composed of two separate 1D FIR operations (see Figure 6-14). There are three major types of 1D FIR operation, 6 tap FIR, 4n tap cubic accumulation and n tap source accumulation. These three algorithms have different rescaling characters and tap numbers. 6 tap is suitable for up-scaling and down-scaling (1X~1/2X). It is a fixed 6 tap FIR operation and needs 18-line buffer to do vertical scaling operation (see Figure 6-15).

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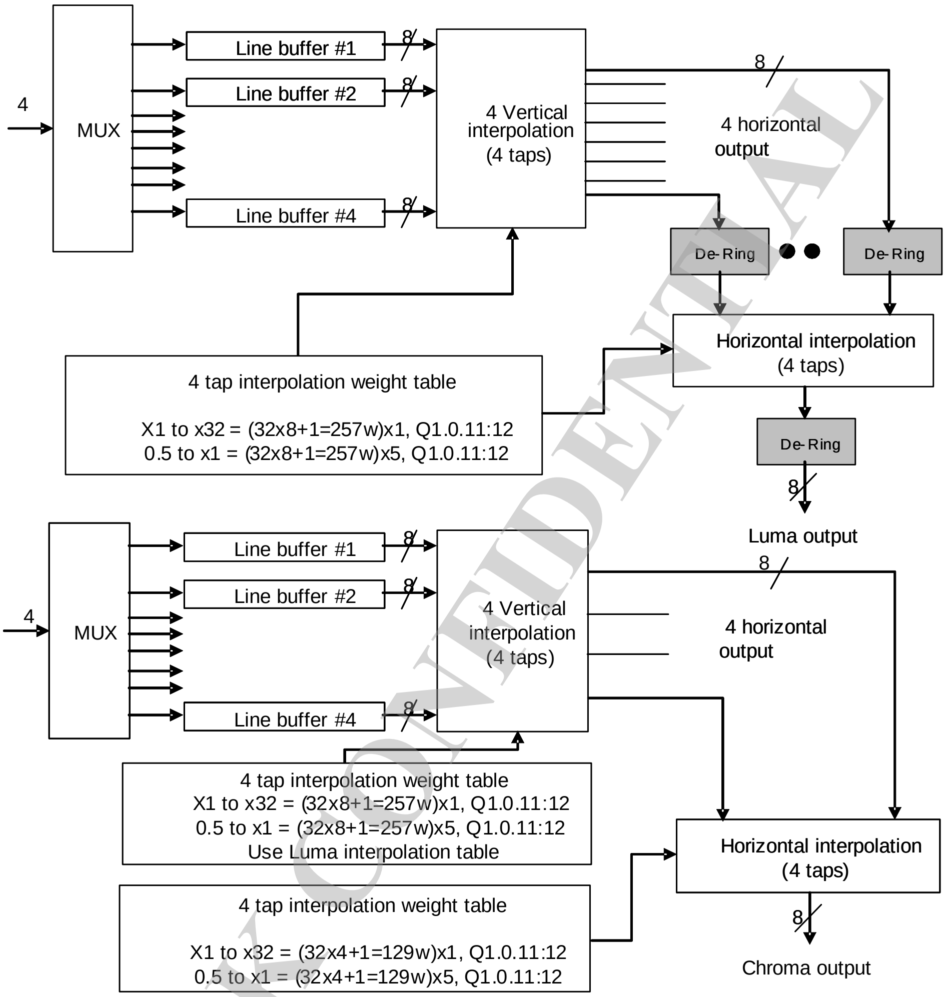

Figure 6-15. 4 tap cubic block diagram (Luma and Chroma data, in MT6735 4tap changes to 6tap)

4n tap cubic accumulation has better quality than 6 tap FIR when the down-scaling ratio is bigger than 1/2X. It is essential a variable tap FIR operation and its tap number is determined by scaling ratio (4 times n, n is scaling ratio). For example, when the scaling ratio is 1, the tap number is 4 (see Figure 6-16). When the scaling ratio is 1/2, the tap number is 8 (see Figure 6-17). In addition, n tap source accumulation is also a variable tap number FIR algorithm. It has poor sharpness and is an extremely low cost solution.

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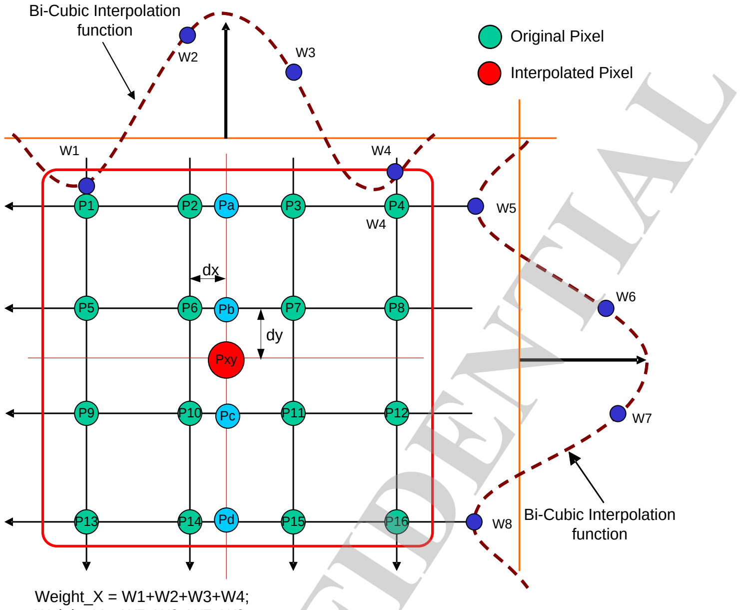
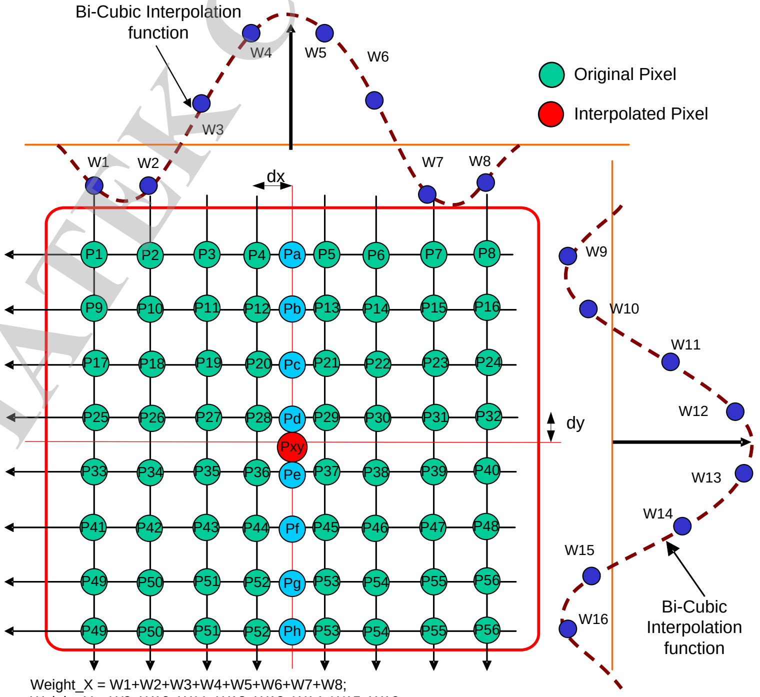


Weight_X = W1+W2+W3+W4;
Weight_Y = W5+W6+W7+W8;
Pa=(P1*W1 + P2*W2 + P3*W3 + P4*W4+Weight_X/2)/Weight_X
Pb=(P5*W1 + P6*W2 + P7*W3 + P8*W4+Weight_X/2)/Weight_X
Pc=(P9*W1 + P10*W2 + P11*W3 + P12*W4+Weight_X/2)/Weight_X
Pd=(P13*W1 + P14*W2 + P15*W3 + P16*W4+Weight_X/2)/Weight_X
Pxy=(Pa*W5 + Pb*W6 + Pc*W7 + Pd*W8+Weight_Y/2)/Weight_Y

Figure 6-16. Cubic accumulation (scaling ratio = 1x)



Weight_X = W1+W2+W3+W4+W5+W6+W7+W8;
Weight_Y = W9+W10+W11+W12+W13+W14+W15+W16;
Pa=(P1*W1 + P2*W2 + P3*W3 + P4*W4 + P5*W5 + P6*W6 + P7*W7 + P8*W8 + Weight_X/2)/Weight_X
Pb, Pc, Pd, Pe, Pf, Pg, Ph Is Interpolated In the same way
Pxy=(Pa*W9 + Pb*W10 + Pc*W11 + Pd*W12 + Pe*W13 + Pf*W14 + Pg*W15 + Ph*W16+ Weight_Y/2)/Weight_Y

Figure 6-17. Cubic accumulation (scaling ratio = 1/2x)

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6.8.3 Programming Guide

6.8.3.1 Suggested Algorithm

Corresponding to applied scaling ratio, here is the suggested algorithm for the resizer to choose from. The algorithm is suggested for the best quality. The principles are:

- 6tap: 32x ~ 1/2x
- 4ntap: 1/2x ~ 1/64x
- ntap: 1x ~ 1/128x

However, the suggested algorithm may contradict with limited supporting size in each resizer engine. Take CDRZ for example, as described in the figure below, if a certain application needs to use CDRZ to resize from 3000 to 1400, it is suggested to use 4ntap cubic accumulation algorithm. However, the supported size of 4ntap in CDRZ is 1152, which is smaller than 1400. Therefore, in this case choose ntap to be applied.

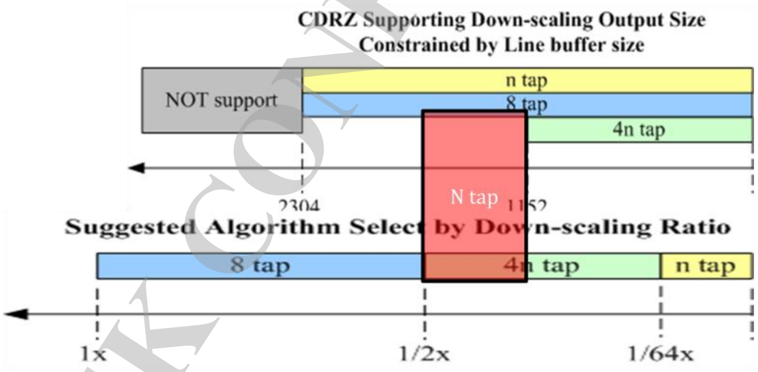

Figure 6-18. Suggested algorithm v.s. supported size

6.8.3.2 Coefficient Step Calculation

The coefficient step is calculated in different way for different algorithms. Refer to the descriptions below.

- 6tap:
  - Unit base: 32768 (2^15)
  - M_m1 = Input_size **– In_Int_Ofst – (In_Sub_Ofst==0? 0 : 1)** -1
  - N_m1 = Output_size -1
  - Cstep = (M_m1*UNIT+(N_m1>>1))/N_m1
- 6tap:
  - Unit base: **65536** (2^16) (note the offset settings)
- 4ntap:
  - Unit base: 1048576 (2^20)
  - M_m1 = Input_size **– In_Int_Ofst – (In_Sub_Ofst==0? 0 : 1)** -1
  - N_m1 = Output_size -1

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  - Cstep = (N_m1*UNIT+(M_m1-1))/M_m1
  - Transfer offset from input to output
- N-tap:
  - Unit base: 1048576 (2^20)
  - M_m1 = Input_size **– In_Int_Ofst – (In_Sub_Ofst==0? 0 : 1)** -1
  - N_m1 = Output_size -1
  - Cstep = (N_m1*UNIT+(M_m1-1))/M_m1
  - Transfer offset from input to output

6.8.3.3 Input/Output Offset Transfer

- For 6 tap interpolation, set "Input Offset" into register.
  - Set register Int_Ofst = In_Int_Ofst ;
  - Set register Sub_Ofst = In_Sub_Ofst ;
- For Accumulation, set "Output Offset" into register.
  - Transfer Input Offset to Output Offset
  - Out_Int_Ofst = (In_Int_Ofst*Cstep + In_Sub_Ofst*Cstep/Unit)/Unit
  - Out_Sub_Ofst = (In_Int_Ofst*Cstep + In_Sub_Ofst*Cstep/Unit) % Unit

6.8.3.4 Table Selection

- 6tap/6tap: Depends on scaling ratio
  - [1~32768]: Table 27 or Table 0~19
  - (32768:36409): Table 20
  - [36409:40961): Table 21
  - [40961:46812): Table 22
  - [46812:54614): Table 23
  - [46812:59579): Table 24
  - [59579:65537): Table 25
  - [65537~∞): Table 26
- 4n tap (downscaling only)
  - 1~19 (blur ~ sharp), 15 is recommended
- N tap (downscaling only): No table selection required

The entire programming guide is as the following steps:
- Decide input/output size.
- Check "Maximum Size" constraint.
- Calculate the ratio.
- Choose algorithm from "Suggested Algorithm".
- Check "Supporting Size" constraint.
- Trigger Resizer and wait for IRQ.

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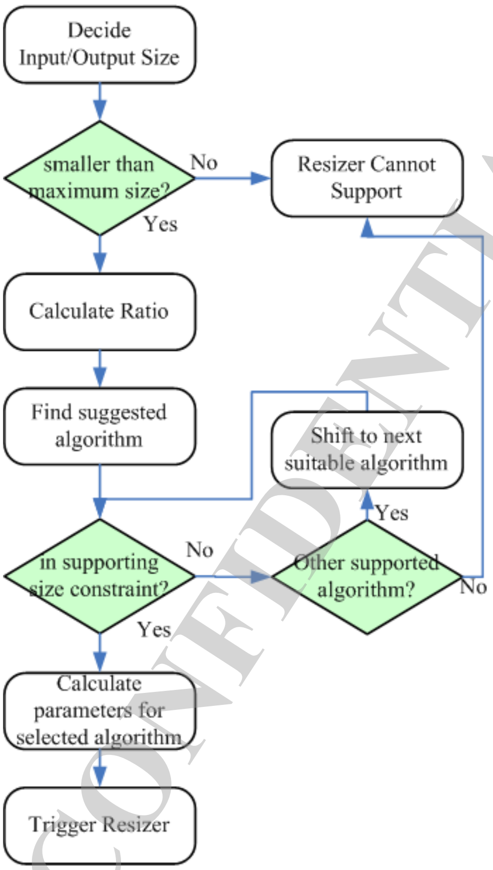

Figure 6-19. Programming guide

6.8.3.5 Programming Method

In MT6735, there are two programming methods

- CPU program through APB bus
- Command queue

Please use proper programming method for different applications. In the video recording application, program CDRZ and MDP_RSZ0/MDP_RSZ1 by command queue to synchronize frame level setting between ISP and MDP processing.

6.8.4 Register Definition

Module name: MDP_RSZ Base address: (+14002000h)

Address	Name	Width	Register Function
14002000	MDP_RSZ_RSZ_ENABLE	32	**RSZ Enable AND Reset** RSZ enable register
14002004	MDP_RSZ_RSZ_CONTROL	32	**RSZ Control** RSZ control register
14002008	MDP_RSZ_RSZ_	32	**RSZ Interrupt Flag**

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Address	Name	Width	Register Function
	INT_FLAG		RSZ interrupt flag
1400200C	MDP_RSZ_RSZ_INPUT_IMAGE	32	**RSZ Input Image** RSZ input image size register
14002010	MDP_RSZ_RSZ_OUTPUT_IMAGE	32	**RSZ Output Image** RSZ output image size register
14002014	MDP_RSZ_RSZ_HORIZONTAL_COEFF_STEP	32	**RSZ_HORIZONTAL_COEFF_STEP** RSZ horizontal coefficient step
14002018	MDP_RSZ_RSZ_VERTICAL_COEFF_STEP	32	**RSZ_VERTICAL_COEFF_STEP** RSZ vertical coefficient step
1400201C	MDP_RSZ_RSZ_LUMA_HORIZONTAL_INTEGER_OFFSET	32	**RSZ_LUMA_HORIZONTAL_INTEGER_OFFSET** RSZ horizontal integer offset
14002020	MDP_RSZ_RSZ_LUMA_HORIZONTAL_SUBPIXEL_OFFSET	32	**RSZ_LUMA_HORIZONTAL_SUBPIXEL_OFFSET** RSZ horizontal sub-pixel offset
14002024	MDP_RSZ_RSZ_LUMA_VERTICAL_INTEGER_OFFSET	32	**RSZ_LUMA_VERTICAL_INTEGER_OFFSET** RSZ vertical integer offset
14002028	MDP_RSZ_RSZ_LUMA_VERTICAL_SUBPIXEL_OFFSET	32	**RSZ_LUMA_VERTICAL_SUBPIXEL_OFFSET** RSZ vertical sub-pixel offset
1400202C	MDP_RSZ_RSZ_CHROMA_HORIZONTAL_INTEGER_OFFSET	32	**RSZ_CHROMA_HORIZONTAL_INTEGER_OFFSET** RSZ horizontal integer offset
14002030	MDP_RSZ_RSZ_CHROMA_HORIZONTAL_SUBPIXEL_OFFSET	32	**RSZ_CHROMA_HORIZONTAL_SUBPIXEL_OFFSET** RSZ horizontal sub-pixel offset
14002034	MDP_RSZ_RSZ_CHROMA_VERTICAL_INTEGER_OFFSET	32	**RSZ_CHROMA_VERTICAL_INTEGER_OFFSET** RSZ vertical integer offset
14002038	MDP_RSZ_RSZ_CHROMA_VERTICAL_SUBPIXEL_OFFSET	32	**RSZ_CHROMA_VERTICAL_SUBPIXEL_OFFSET** RSZ vertical sub-pixel offset
1400203C	MDP_RSZ_RSZ_RSV	32	**RSZ_RSV** RSZ reserved register
14002040	MDP_RSZ_RSZ_DEBUG_SEL	32	**RSZ_DEBUG_SEL** Selects RSZ debugging
14002044	MDP_RSZ_RSZ_DEBUG	32	**RSZ_DEBUG** RSZ debugging register

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14002000 **MDP_RSZ_RSZ_ENABLE** **RSZ Enable AND Reset** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RSZ_RS

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																T
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RSZ_EN
Type																RW
Reset																0

Bit(s)	Name	Description
16	RSZ_RST	Resizer reset bit
0	RSZ_EN	Resizer enabling bit

14002004 MDP_RSZ_RSZ_CONTROL RSZ Control 80000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RSZ_INT_WCLR_EN	RSZ_INTEN				RSZ_C42_CONV	RSZ_VERTICAL_TABLE_SELECT					RSZ_HORIZONTAL_TABLE_SELECT				
Type	RW	RW				RW	RW					RW				
Reset	1	0	0	0		0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSZ_TRUNCATION_BIT_V			RSZ_TRUNCATION_BIT_H			RSZ_LBCSON_MODE	RSZ_VERTICAL_ALGORITHM		RSZ_HORIZONTAL_ALGORITHM		RSZ_VERTICAL_FIRST			RSZ_VERTICAL_EN	RSZ_HORIZONTAL_EN
Type	RW			RW			RW	RW		RW		RW			RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0			0	0

Bit(s)	Name	Description
31	RSZ_INT_WCLR_EN	**Enables interrupt write-clear** 0: Interrupt read-clear 1: Interrupt write-clear
30:28	RSZ_INTEN	**Enables interrupt** Bit 2: Error interrupt Bit 1: Frame end interrupt Bit 0: Frame start interrupt
26	RSZ_C42_CONV	**C42 conversion method** 0: Drop 1: [1 2 1] interpolation
25:21	RSZ_VERTICAL_TABLE_SELECT	**Double buffer** Selects vertical scaling coefficient table 4 tap: [0:25] (1x up ~ 1/2x down) Cubic accumulation: [0:19] (blur ~ sharp)
20:16	RSZ_HORIZONTAL_TABLE_SELECT	**Double buffer** Selects horizontal scaling coefficient table 4 tap: [0:25] (1x up ~ 1/2x down) Cubic accumulation: [0:19] (blur ~ sharp)
15:13	RSZ_TRUNCATION_BIT_V	**Double buffer** Cubic accumulation parameter Truncate weighting bit for high ratio down-

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Bit(s)	Name	Description
		sample
12:10	RSZ_TRUNCATION_BIT_H	**Double buffer** Cubic accumulation parameter Truncate weighting bit for high ratio down-sample
9	RSZ_LBCSON_MODE	**Double buffer** Line buffer control CS on mode
8:7	RSZ_VERTICAL_ALGORITHM	**Double buffer** Vertical scaling algorithm 0: 4 tap 1: n tap source accumulation 2: 4n tap cubic accumulation 3: Reserved
6:5	RSZ_HORIZONTAL_ALGORITHM	**Double buffer** Horizontal scaling algorithm 0: 4 tap 1: n tap source accumulation 2: 4n tap cubic accumulation 3: Reserved
4	RSZ_VERTICAL_FIRST	**Double buffer** 0: Horiznotal first then vertical scaling 1: Vertical first then horizontal scaling
1	RSZ_VERTICAL_EN	**Double buffer** Enables vertical scaling function.
0	RSZ_HORIZONTAL_EN	**Double buffer** Enables horizontal scaling function.

14002008 **MDP_RSZ_RSZ_INT_FLAG** **RSZ Interrupt Flag** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RSZ_SOF_RESET	RSZ_SIZE_ERR			RSZ_FRAME_END	RSZ_FRAME_START
Type											RU	RU			RU	RU
Reset											0	0			0	0

Bit(s)	Name	Description
5	RSZ_SOF_RESET	SOF reset interrupt
4	RSZ_SIZE_ERR	Size error Interrupt
1	RSZ_FRAME_END	Frame end interrupt
0	RSZ_FRAME_START	Frame start interrupt

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1400200C **MDP_RSZ_RSZ_INPUT_IMAGE** **RSZ Input Image** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RSZ_DRS_PADDING_DIS	RSZ_DRS_LCLIP_EN		RSZ_INPUT_IMAGE_H												
Type	RW	RW		RW												
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RSZ_INPUT_IMAGE_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RSZ_DRS_PADDING_DIS	**Double buffer** Disables C42 padding
30	RSZ_DRS_LCLIP_EN	**Double buffer** Enables C42 left two pixels crop
28:16	RSZ_INPUT_IMAGE_H	**Double buffer** Height of imput image
12:0	RSZ_INPUT_IMAGE_W	**Double buffer** Width of input image

14002010 **MDP_RSZ_RSZ_OUTPUT_IMAGE** **RSZ Output Image** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RSZ_URS_CLIP_EN			RSZ_OUTPUT_IMAGE_H												
Type	RW			RW												
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RSZ_OUTPUT_IMAGE_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RSZ_URS_CLIP_EN	**Double buffer** Enables C24 crop
28:16	RSZ_OUTPUT_IMAGE_H	**Double buffer** Height of output image
12:0	RSZ_OUTPUT_IMAGE_W	**Double buffer** Width of output image

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14002014 **MDP_RSZ_RSZ_HORIZONTAL_COEFF_STEP** **RSZ_HORIZONTAL_COEFF_STEP** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										RSZ_HORIZONTAL_COEFF_STEP[22:16]						
Type										RW						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSZ_HORIZONTAL_COEFF_STEP[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
22:0	RSZ_HORIZONTAL_COEFF_STEP	**Double buffer** Horiznotal scaling ratio

14002018 **MDP_RSZ_RSZ_VERTICAL_COEFF_STEP** **RSZ_VERTICAL_COEFF_STEP** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										RSZ_VERTICAL_COEFF_STEP[22:16]						
Type										RW						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSZ_VERTICAL_COEFF_STEP[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
22:0	RSZ_VERTICAL_COEFF_STEP	**Double buffer** Vertical scaling ratio

1400201C **MDP_RSZ_RSZ_LUMA_HORIZONTAL_INTEGER_OFFSET** **RSZ_LUMA_HORIZONTAL_INTEGER_OFFSET** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RSZ_LUMA_HORIZONTAL_INTEGER_OFFSET												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	RSZ_LUMA_HORI	**Double buffer**

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Bit(s)	Name	Description
	ZONTAL_INTEGER_OFFSET	Horizontal luma integer offset

14002020	MDP_RSZ_RSZ_LUMA_HORIZONTAL_SUBPIXEL_OFFSET	RSZ_LUMA_HORIZONTAL_SUBPIXEL_OFFSET	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												RSZ_LUMA_HORIZONTAL_SUBPIXEL_OFFSET[20:16]				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSZ_LUMA_HORIZONTAL_SUBPIXEL_OFFSET[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	RSZ_LUMA_HORIZONTAL_SUBPIXEL_OFFSET	**Double buffer** Horizontal luma sub-pixel offset

14002024	MDP_RSZ_RSZ_LUMA_VERTICAL_INTEGER_OFFSET	RSZ_LUMA_VERTICAL_INTEGER_OFFSET	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RSZ_LUMA_VERTICAL_INTEGER_OFFSET												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	RSZ_LUMA_VERTICAL_INTEGER_OFFSET	**Double buffer** Vertical luma integer offset

14002028	MDP_RSZ_RSZ_LUMA_VERTICAL_SUBPIXEL_OFFSET	RSZ_LUMA_VERTICAL_SUBPIXEL_OFFSET	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name												RSZ_LUMA_VERTICAL_SUBPIXEL_OFFSET[20:16]				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSZ_LUMA_VERTICAL_SUBPIXEL_OFFSET[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	RSZ_LUMA_VERTICAL_SUBPIXEL_OFFSET	**Double buffer** Vertical luma sub-pixel offset

1400202C	MDP_RSZ_RSZ_CHROMA_HORIZONTAL_INTEGER_OFFSET	RSZ_CHROMA_HORIZONTAL_INTEGER_OFFSET	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RSZ_CHROMA_HORIZONTAL_INTEGER_OFFSET												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	RSZ_CHROMA_HORIZONTAL_INTEGER_OFFSET	**Double buffer** Horizontal chroma integer offset

14002030	MDP_RSZ_RSZ_CHROMA_HORIZONTAL_SUBPIXEL_OFFSET	RSZ_CHROMA_HORIZONTAL_SUBPIXEL_OFFSET	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												RSZ_CHROMA_HORIZONTAL_SUBPIXEL_OFFSET[20:16]				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSZ_CHROMA_HORIZONTAL_SUBPIXEL_OFFSET[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
20:0	RSZ_CHROMA_HORIZONTAL_SUBPIXEL_OFFSET	**Double buffer** Horizontal chroma sub-pixel offset

14002034	MDP_RSZ_RSZ_CHROMA_VERTICAL_INTEGER_OFFSET	RSZ_CHROMA_VERTICAL_INTEGER_OFFSET	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				RSZ_CHROMA_VERTICAL_INTEGER_OFFSET												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	RSZ_CHROMA_VERTICAL_INTEGER_OFFSET	**Double buffer** Vertical chroma integer offset

14002038	MDP_RSZ_RSZ_CHROMA_VERTICAL_SUBPIXEL_OFFSET	RSZ_CHROMA_VERTICAL_SUBPIXEL_OFFSET	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												RSZ_CHROMA_VERTICAL_SUBPIXEL_OFFSET[20:16]				
Type												RW				
Reset												0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RSZ_CHROMA_VERTICAL_SUBPIXEL_OFFSET[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	RSZ_CHROMA_VERTICAL_SUBPIXEL_OFFSET	**Double buffer** Vertical chroma sub-pixel offset

1400203C	MDP_RSZ_RSZ_RSV	RSZ_RSV	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RSZ_RSV[31:16]															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RSZ_RSV[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RSZ_RSV	**Dering parameter** In projects without dering function, this register is reserved.

14002040 MDP_RSZ_RSZ_DEBUG_SEL RSZ_DEBUG_SEL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**RSZ_DEBUG_SEL**			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RSZ_DEBUG_SEL	Selects debugging

14002044 MDP_RSZ_RSZ_DEBUG RSZ_DEBUG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RSZ_DEBUG[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RSZ_DEBUG[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RSZ_DEBUG	Debugging register

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6.9 MDP ROT_DMA (Multimedia Data Path-Rotation DMA)

6.9.1 Introduction

ROT_DMA is a write rotate DMA agent supporting 8 rotation/flip options for users holding the phone in any orientation to rotate the image in the correct direction.

6.9.2 Features

- Rotation Angels: 0°, 0° + H_Flip, 90°, 90° + H_Flip, 180°, 180° + H_Flip, 270°, and 270° + H_Flip as illustrated in **Error! Reference source not found.**.
- Format and Footprint: YUV422 1/2/3 plane, YUV420 2/3 plane, RGB888, ARGB8888, RGB565, Y only
- Programmable RGB color matrix
- Dither engine

6.9.3 Block Diagram

See the figure below for the engine architecture, including color matrix, dither, sub-sampling, rotator and DMA engines.

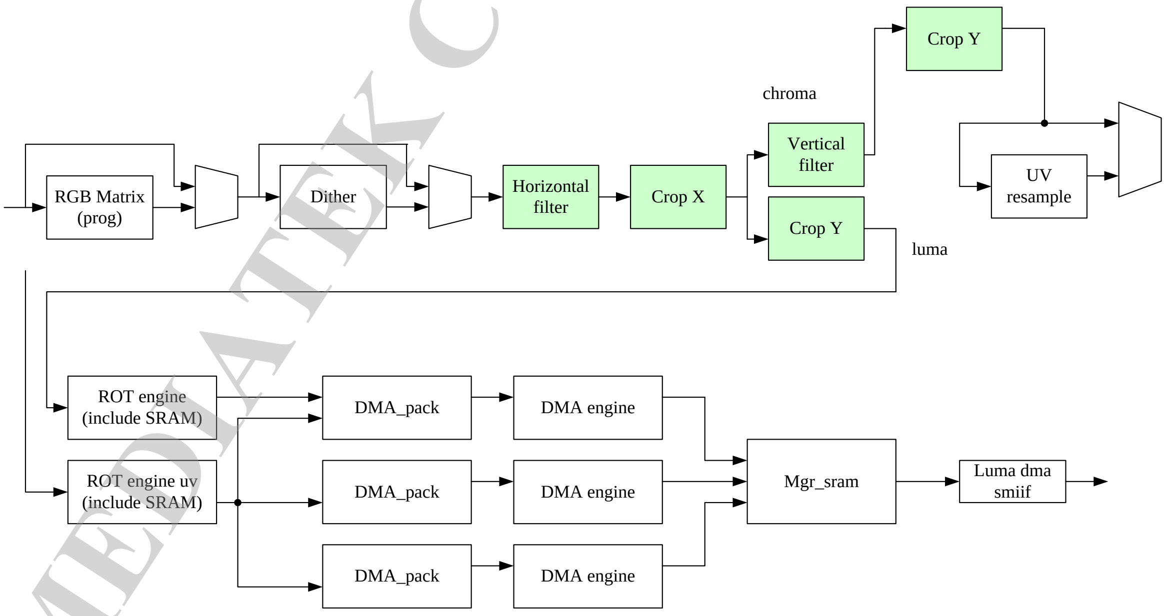

Figure 6-20. Block diagram of ROT_DMA

6.9.4 Register Definition

Module name: MDP_WROT Base address: (+14005000h)

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Address	Name	Width	Register Function
14005000	MDP_WROT_VIDO_CTRL	32	VIDO Control
14005004	MDP_WROT_VIDO_DMA_PERF	32	VIDO DMA Performance
14005008	MDP_WROT_VIDO_MAIN_BUF_SIZE	32	VIDO DMA Main Buffer Size
14005010	MDP_WROT_VIDO_SOFT_RST	32	VIDO Software Reset
14005014	MDP_WROT_VIDO_SOFT_RST_STAT	32	VIDO Software Reset Status
14005018	MDP_WROT_VIDO_INT_EN	32	VIDO Interrupt Enable
1400501C	MDP_WROT_VIDO_INT	32	VIDO Interrupt
14005020	MDP_WROT_VIDO_CROP_OFST	32	VIDO Image Cropping Offset
14005024	MDP_WROT_VIDO_TAR_SIZE	32	VIDO Target Image Size
1400502C	MDP_WROT_VIDO_OFST_ADDR	32	VIDO Offset Address
14005030	MDP_WROT_VIDO_STRIDE	32	VIDO Stride
14005038	MDP_WROT_VIDO_OFST_ADDR_C	32	VIDO Offset Address Chroma
1400503C	MDP_WROT_VIDO_STRIDE_C	32	VIDO Stride Chroma
14005054	MDP_WROT_VIDO_DITHER	32	VIDO Dithering
14005068	MDP_WROT_VIDO_OFST_ADDR_V	32	VIDO Offset Address Chroma 2
1400506C	MDP_WROT_VIDO_STRIDE_V	32	VIDO Stride Chroma 2
14005070	MDP_WROT_VIDO_RSV_1	32	VIDO Spare Registers
14005074	MDP_WROT_VIDO_DMA_PREULTRA	32	VIDO Pre Ultra Setting
14005078	MDP_WROT_VIDO_IN_SIZE	32	VIDO Input Image Size
1400507C	MDP_WROT_VIDO_ROT_EN	32	VIDO Rotation Enable
14005080	MDP_WROT_VIDO_FIFO_TEST	32	DMA FIFO Test
14005084	MDP_WROT_VIDO_MAT_CTRL	32	VIDO Matrix Control
14005088	MDP_WROT_VIDO_MAT_RMY	32	VIDO Y2R Conversion Parameter R0
1400508C	MDP_WROT_VIDO_MAT_RMV	32	VIDO Y2R Conversion Parameter R1
14005090	MDP_WROT_VIDO_MAT_GMY	32	VIDO Y2R Conversion Parameter G0
14005094	MDP_WROT_VI	32	VIDO Y2R Conversion Parameter B0

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Address	Name	Width	Register Function
	DO_MAT_BMY		
14005098	MDP_WROT_VIDO_MAT_BMV	32	VIDO Y2R Conversion Parameter B1
1400509C	MDP_WROT_VIDO_MAT_PREADD	32	VIDO Y2R Conversion Parameter Extended Add on YUV
140050A0	MDP_WROT_VIDO_MAT_POSTADD	32	VIDO Y2R Conversion Parameter Extended Add on RGB
140050A4	MDP_WROT_VIDO_DITHER_00	32	VIDO Dithering Control Register 0
140050AC	MDP_WROT_VIDO_DITHER_02	32	VIDO Dithering Control Register 2
140050B0	MDP_WROT_VIDO_DITHER_03	32	VIDO Dithering Control Register 3
140050B4	MDP_WROT_VIDO_DITHER_04	32	VIDO Dithering Control Register 4
140050B8	MDP_WROT_VIDO_DITHER_05	32	VIDO Dithering Control Register 5
140050BC	MDP_WROT_VIDO_DITHER_06	32	VIDO Dithering Control Register 6
140050C0	MDP_WROT_VIDO_DITHER_07	32	VIDO Dithering Control Register 7
140050C4	MDP_WROT_VIDO_DITHER_08	32	VIDO Dithering Control Register 8
140050C8	MDP_WROT_VIDO_DITHER_09	32	VIDO Dithering Control Register 9
140050CC	MDP_WROT_VIDO_DITHER_10	32	VIDO Dithering Control Register 10
140050D0	MDP_WROT_VIDO_DEBUG	32	VIDO Debug Register
140050D4	MDP_WROT_VIDO_ARB_SW_CTL	32	VIDO DMA Arbiter Software Control
140050E0	MDP_WROT_TRACK_CTL	32	MDP WROT Pre-ultra Track Control
140050E4	MDP_WROT_TRACK_WINDOW	32	MDP WROT Pre-ultra Track Window
140050E8	MDP_WROT_TRACK_TARGET	32	MDP WROT Pre-ultra Track Target
140050EC	MDP_WROT_TRACK_STOP	32	MDP WROT Pre-ultra Track Stop
140050F0	MDP_WROT_TRACK_PROC_CNT0	32	MDP WROT Pre-ultra Track Proc Counter 0
140050F4	MDP_WROT_TRACK_PROC_CNT1	32	MDP WROT Pre-ultra Track Proc Counter 1
14005F00	MDP_WROT_VIDO_BASE_ADDR	32	VIDO Base Address
14005F04	MDP_WROT_VIDO_BASE_ADDR_C	32	VIDO Base Address Chroma
14005F08	MDP_WROT_VIDO_BASE_ADDR_V	32	VIDO Base Address Chroma 2

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14005000 **MDP_WROT_VIDO_CTRL** **VIDO Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VIDO_UV_YSEL		VIDO_UV_XSEL			VIDO_SOF_RESET_EN		VIDO_FLIP			VIDO_ROTATION					
Type	RW		RW			RW		RW			RW					
Reset	0	0	0	0		0		0			0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		VIDO_PREULTRA_EN	VIDO_PRI_EN	VIDO_CROP_EN				VIDO_UNIFORM_SWAP				VIDO_BLK_OPTION	VIDO_UNIFORM_FORMAT			
Type		RW	RW	RW				RW				RW	RW			
Reset		0	0	0				0				0	0	0	0	0

Bit(s)	Name	Description
31:30	VIDO_UV_YSEL	**Selects vertical UV** 0: Pick from 0. 0,2,4... 1: Pick from 1. 1,3,5... 2: Pick every pixel
29:28	VIDO_UV_XSEL	**Selects horizontal UV** 0: Pick from 0. 0,2,4... 1: Pick from 1. 1,3,5... 2: Pick every pixel
26	VIDO_SOF_RESET_EN	**Enables SOF reset** 0: No SOF reset 1: Do Soft reset process on receiving SOF
24	VIDO_FLIP	**Enables horizontal flip** 0: No flip 1: Flip Note: The flip action is done after horizontal
21:20	VIDO_ROTATION	**Rotation angle** 0: 0 degree 1: 90 degree 2: 180 degree 3: 270 degree
14	VIDO_PREULTRA_EN	**Enables pre-ultra**
13	VIDO_PRI_EN	**Enables PRI threshold**
12	VIDO_CROP_EN	**Double buffer** VIDO cropping function enabling bit
8	VIDO_UNIFORM_SWAP	
4	VIDO_BLK_OPTION	**Performance improve option** 0: Disable 1: Enable
3:0	VIDO_UNIFORM_FORMAT	

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14005004 MDP_WROT_VIDO_DMA_PERF VIDO DMA Performance 3F000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			VIDO_CH2_SMI_GROUP_NUM		VIDO_CH1_SMI_GROUP_NUM		VIDO_CH0_SMI_GROUP_NUM		VIDO_FIFO_PRI_THR[11:4]							
Type			RW		RW		RW		RW							
Reset			1	1	1	1	1	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_FIFO_PRI_THR[3:0]				VIDO_FIFO_PRI_LOW_THR											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:28	VIDO_CH2_SMI_GROUP_NUM	**SMI request grouping number** It will launch consecutive SMI requests by this number for this channel. 0: 1 consecutive request 1: 2 consecutive requests 2: 3 consecutive requests 3: 4 consecutive requests
27:26	VIDO_CH1_SMI_GROUP_NUM	**SMI request grouping number** It will launch consecutive SMI requests by this number for this channel. 0: 1 consecutive request 1: 2 consecutive requests 2: 3 consecutive requests 3: 4 consecutive requests
25:24	VIDO_CH0_SMI_GROUP_NUM	**SMI request grouping number** It will launch consecutive SMI requests by this number for this channel. 0: 1 consecutive request 1: 2 consecutive requests 2: 3 consecutive requests 3: 4 consecutive requests
23:12	VIDO_FIFO_PRI_THR	**For priority control signal** If the FIFO amount is bigger than THR, the priority control signal will be asserted.
11:0	VIDO_FIFO_PRI_LOW_THR	**PRI low threshold**

14005008 MDP_WROT_VIDO_MAIN_BUF_SIZE VIDO DMA Main Buffer Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_MAIN_BLK_WIDTH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		VIDO_MAIN_BUF_LINE_NUM								VIDO_FILT_TYPE_V				VIDO_FILT_TYPE_H		
Type		RW								RW				RW		
Reset		0	0	0	0	0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
28:16	VIDO_MAIN_BLK_W	**Width of line block in main working buffer**

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Bit(s)	Name	Description
	IDTH	Unit: Pixel
14:8	VIDO_MAIN_BUF_LINE_NUM	**Line number of main working buffer in FIFO or single buffer mode**
6:4	VIDO_FILT_TYPE_V	**Chroma horizontal down sample filter type** 0: Bypass 1: Forward [1 2 1] filter 2: Backward [1 2 1] filter 3: Forward [1 1] filter 4: Backward [1 1] filter
2:0	VIDO_FILT_TYPE_H	**Chroma horizontal down sample filter type** 0: Bypass 1: Forward [1 2 1] filter 2: Backward [1 2 1] filter 3: Forward [1 1] filter 4: Backward [1 1] filter

14005010 **MDP_WROT_VIDO_SOFT_RST** **VIDO Software Reset** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																VIDO_SOFT_RST
Type																RW
Reset																0

Bit(s)	Name	Description
0	VIDO_SOFT_RST	**VIDO software reset** For software reset is required, write 1 until VIDO_SOFT_RST_STAT = 1 . When VIDO_SOFT_RST_STAT = 1, write 0. Then, polling until VIDO_SOFT_RST_STAT = 0.

14005014 **MDP_WROT_VIDO_SOFT_RST_STAT** **VIDO Software Reset Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																VIDO_SOFT_RST_STAT
Type																RU
Reset																0

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Bit(s)	Name	Description
0	VIDO_SOFT_RST_ST AT	**VIDO software reset status** This status will be 1 when soft reset is active, and be 0 when soft reset is completed.

14005018 MDP_WROT_VIDO_INT_EN VIDO Interrupt Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			VIDO_CSR_DEBUG											VIDO_INT_WC_3_EN	VIDO_INT_WC_2_EN	VIDO_INT_1_EN
Type			RW											RW	RW	RW
Reset			0	0	0	0	0	0						0	0	0

Bit(s)	Name	Description
13:8	VIDO_CSR_DEBUG	**Controls VIDO debugging register**
2	VIDO_INT_WC_3_E N	**Enables VIDO rotate finish status clear**
1	VIDO_INT_WC_2_E N	**Controls VIDO frame done status**
0	VIDO_INT_1_EN	**Enables VIDO interrupt 1** Interrupt situation: Crop setting is not correct.

1400501C MDP_WROT_VIDO_INT VIDO Interrupt 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														VIDO_INT_3	VIDO_INT_2	VIDO_INT_1
Type														A0	A0	A0
Reset														1	1	1

Bit(s)	Name	Description
2	VIDO_INT_3	**VIDO status** Situation: Luma rotation done. Turn on VIDO_INT_WC_3_EN and write 1 to clear.
1	VIDO_INT_2	**VIDO status** Situation: Frame done = 0. INT turns on VIDO_INT_WC_2_EN and write 1 to clear
0	VIDO_INT_1	**VIDO interrupt 1** Interrupt situation: Crop setting is not correct

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Bit(s)	Name	Description
		Turn on VIDO_INT_WC_EN and write 1 to clear.

14005020 MDP_WROT_VIDO_CROP_OFST VIDO Image Cropping Offset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_CROP_OFST_Y												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VIDO_CROP_OFST_X												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	VIDO_CROP_OFST_Y	**Double buffer** Y channel offset position for cropping. If VIDO_FORMAT is YUV422 or YUV422V, y channel width must be multiple of 2.
12:0	VIDO_CROP_OFST_X	**Double buffer** Y channel offset position for cropping. If VIDO_FORMAT is YUV422 or YUV422V, y channel width must be multiple of 2.

14005024 MDP_WROT_VIDO_TAR_SIZE VIDO Target Image Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_YSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VIDO_XSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	VIDO_YSIZE	**Double buffer** Y channel height of target image
12:0	VIDO_XSIZE	**Double buffer** Y channel width of Target image If VIDO_FORMAT is YUV422 or YUV422V, y channel width must be multiple of 2.

1400502C MDP_WROT_VIDO_OFST_ADDR VIDO Offset Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name					VIDO_OFST_ADDR[27:16]											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_OFST_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:0	VIDO_OFST_ADDR	**Double buffer** VIDO offset address 1. It follows the definition of Base Address 1.

14005030 MDP_WROT_VIDO_STRIDE VIDO Stride 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_STRIDE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	VIDO_STRIDE	**Double buffer** VIDO stride 1. It follows the definition of Base Address 2.

14005038 MDP_WROT_VIDO_OFST_ADDR_C VIDO Offset Address Chroma 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					VIDO_OFST_ADDR_C[27:16]											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_OFST_ADDR_C[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:0	VIDO_OFST_ADDR_C	**Double buffer** VIDO offset address 2. It follows the definition of Base Address 2.

1400503C MDP_WROT_VIDO_STRIDE_C VIDO Stride Chroma 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

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Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_STRIDE_C															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	VIDO_STRIDE_C	**Double buffer** VIDO stride 2. It follows the definition of Base Address 2.

14005054 **MDP_WROT_VIDO_DITHER** **VIDO Dithering** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VIDO_XRGB_DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																VIDO_DIT_EN
Type																RW
Reset																0

Bit(s)	Name	Description
31:24	VIDO_XRGB_DUMMY	XRGB format 8-bit dummy data
0	VIDO_DIT_EN	Enables VIDO dithering

14005068 **MDP_WROT_VIDO_OFST_ADDR_V** **VIDO Offset Address Chroma 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					VIDO_OFST_ADDR_V[27:16]											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_OFST_ADDR_V[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:0	VIDO_OFST_ADDR_V	**Double buffer** VIDO offset address 3. It follows the definition of Base Address 3.

1400506C **MDP_WROT_VIDO_STRIDE_V** **VIDO Stride Chroma 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_STRIDE_V															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	VIDO_STRIDE_V	**Double buffer** VIDO stride 3. It follows the definition of Base Address 3.

14005070 MDP_WROT_VIDO_RSV_1 VIDO Spare Registers 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VIDO_RSV_1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_RSV_1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VIDO_RSV_1	VIDO spare registers

14005074 MDP_WROT_VIDO_DMA_PREULTRA VIDO Pre Ultra Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									VIDO_FIFO_PREULTRA_THR[11:4]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_FIFO_PREULTRA_THR[3:0]				VIDO_FIFO_PREULTRA_THR_LOW											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:12	VIDO_FIFO_PREULTRA_THR	Pre-ultra high threshold
11:0	VIDO_FIFO_PREULTRA_THR_LOW	Pre-ultra low threshold

14005078 MDP_WROT_VIDO_IN_SIZE VIDO Input Image Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name				**VIDO_IN_YSIZE**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**VIDO_IN_XSIZE**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	VIDO_IN_YSIZE	**Double buffer** Y channel height of input image
12:0	VIDO_IN_XSIZE	**Double buffer** Y channel width of Input image If VIDO_FORMAT is YUV422 or YUV422V, y channel width must be multiple of 2.

14005070C **MDP_WROT_VIDO_ROT_EN** **VIDO Rotation Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**VIDO_ROT_EN**
Type																RW
Reset																0

Bit(s)	Name	Description
0	VIDO_ROT_EN	Enables rotation

14005080 **MDP_WROT_VIDO_FIFO_TEST** **DMA FIFO Test** **00000080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**VIDO_FIFO_SIZE**											
Type					RW											
Reset					0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	VIDO_FIFO_SIZE	ROT FIFO size

14005084 **MDP_WROT_VIDO_MAT_C** **VIDO Matrix Control** **00000040**

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TRL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									VIDO_MTX_SEL						VIDO_EXT_MTX_EN	VIDO_MAT_EN
Type									RW						RW	RW
Reset									0	1	0	0			0	0

Bit(s)	Name	Description
7:4	VIDO_MTX_SEL	**Double buffer** Selects color matrix format 0: RGB to JPEG 2: RGB to 601 3: RGB to 709 4: JPEG to RGB 6: 601 to RGB 7: 709 to RGB 8: JPEG to 601 9: JPEG to 709 10: 601 to JPEG 11: 709 to JPEG 12: 709 to 601 Default: 601 to 709
1	VIDO_EXT_MTX_EN	**Double buffer** Selects color matrix auto mode 0: Use auto mode 1: Use programmable coeff
0	VIDO_MAT_EN	**Double buffer** Enables matrix 0: Bypass 1: Enable

14005088 MDP_WROT_VIDO_MAT_RMY VIDO Y2R Conversion Parameter R0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_RMU												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VIDO_RMY												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	VIDO_RMU	VIDO YUV2RGB program parameter for R color of U component
12:0	VIDO_RMY	VIDO YUV2RGB program parameter for R color of Y component

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1400508C MDP_WROT_VIDO_MAT_RMV VIDO Y2R Conversion Parameter R1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_GMY												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VIDO_RMV												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	VIDO_GMY	VIDO YUV2RGB program parameter for G color of Y component
12:0	VIDO_RMV	VIDO YUV2RGB program parameter for R color of V component

14005090 MDP_WROT_VIDO_MAT_GMY VIDO Y2R Conversion Parameter G0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_GMV												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VIDO_GMU												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	VIDO_GMV	VIDO YUV2RGB program parameter for G color of V component
12:0	VIDO_GMU	VIDO YUV2RGB program parameter for G color of U component

14005094 MDP_WROT_VIDO_MAT_BMY VIDO Y2R Conversion Parameter B0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_BMU												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VIDO_BMY												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	VIDO_BMU	VIDO YUV2RGB program parameter for B color of U component
12:0	VIDO_BMY	VIDO YUV2RGB program parameter for B color of Y component

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14005098 **MDP_WROT_VIDO_MAT_BMV** **VIDO Y2R Conversion Parameter B1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VIDO_BMV												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	VIDO_BMV	VIDO YUV2RGB program parameter for B color of V component

1400509C **MDP_WROT_VIDO_MAT_PREADD** **VIDO Y2R Conversion Parameter Extended Add on YUV** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_VA										VIDO_UA[8:6]		
Type				RW										RW		
Reset				0	0	0	0	0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_UA[5:0]							VIDO_YA								
Type	RW							RW								
Reset	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:20	VIDO_VA	VIDO YUV2RGB program parameter for V to add extended offset
18:10	VIDO_UA	VIDO YUV2RGB program parameter for U to add extended offset
8:0	VIDO_YA	VIDO YUV2RGB program parameter for Y to add extended offset

140050A0 **MDP_WROT_VIDO_MAT_POSTADD** **VIDO Y2R Conversion Parameter Extended Add on RGB** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_BA										VIDO_GA[8:6]		
Type				RW										RW		
Reset				0	0	0	0	0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_GA[5:0]							VIDO_RA								
Type	RW							RW								
Reset	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:20	VIDO_BA	VIDO YUV2RGB program parameter for B to add extended offset
18:10	VIDO_GA	VIDO YUV2RGB program parameter for G to add extended offset
8:0	VIDO_RA	VIDO YUV2RGB program parameter for R to add extended offset

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140050A4 MDP_WROT_VIDO_DITHER_00 VIDO Dithering Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	frame_done_del										crc_clr	crc_start	crc_cen	wrap_mode	out_sel	start
Type	RW										RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
15:8	frame_done_del	**Frame done return delay**
5	crc_clr	**Write 1 to clear CRC result.**
4	crc_start	**Write 1 to start CRC counting.**
3	crc_cen	0: Turn off CRC engine CG 1: Turn on CRC engine CG
2	wrap_mode	**Enables rounding for dithering function** When the rounding method is used, both running order and error dispersion cannot be used.
1	out_sel	0: Bypass dither 1: Through dither
0	start	0: No dither 1: Start dither engine

140050AC MDP_WROT_VIDO_DITHER_02 VIDO Dithering Control Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	w_demo															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			round_en	rdither_en	lfsr_en	edither_en	left_en		fphase_r	fphase_en	fphase					
Type			RW	RW	RW	RW	RW		RW	RW	RW					
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	w_demo	**Short line length**
13	round_en	**Enables rounding for dithering function** When the rounding method is used, both running order and error dispersion cannot be used.
12	rdither_en	**Enables running order dithering** The running order dithering must be set when ROUND_EN is set to 0. The running order dithering can run with error dispersion when EDOTHER_EN is set to 1.
11	lfsr_en	**Enables LFSR-type dithering**
10	edither_en	**Enables error dispersion dithering**

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Bit(s)	Name	Description
		The error dispersion dithering must be set when ROUND_EN is set to 0. The running order dithering can run with error dispersion when RDITHER_EN is set to 1.
9:8	left_en	**Enables left part of screen dither** 0: Dither runs at full screen. 1: Dither runs at left part of screen.
7	fphase_r	**Dither SubPixel addend**
6	fphase_en	**Running order dithering frame** Enables phase control
5:0	fphase	**Running order dithering frame phase increment** *Note:* *If ROUND_EN = 1, the output will be rounding only (no matter what RDITHER_EN and EDITHER_EN setting are). RDITHER_EN and EDITHER_EN can work together.*

140050B0 **MDP_WROT_VIDO_DITHER_03** **VIDO Dithering Control Register 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name											drmod_b		drmod_g		drmod_r	
Type											RW		RW		RW	
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:4	drmod_b	**Selects dither mode** 0: No dither 1: 12-bit dither to 10-bit 2: 12-bit dither to 8-bit 3: 12-bit dither to 6-bit
3:2	drmod_g	**Selects dither mode** 0: No dither 1: 12-bit dither to 10-bit 2: 12-bit dither to 8-bit 3: 12-bit dither to 6-bit
1:0	drmod_r	**Selects dither mode** 0: No dither 1: 12-bit dither to 10-bit 2: 12-bit dither to 8-bit 3: 12-bit dither to 6-bit

140050B4 **MDP_WROT_VIDO_DITHER_04** **VIDO Dithering Control Register 4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ink		ink_data_b										ink_data_g[9:6]			
Type	RW		RW										RW			
Reset	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ink_data_g[5:0]						ink_data_r									
Type	RW						RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	ink	Enables ink
29:20	ink_data_b	Ink data for B
19:10	ink_data_g	Ink data for G
9:0	ink_data_r	Ink data for R

140050B8 MDP_WROT_VIDO_DITHER_05 VIDO Dithering Control Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	h_active															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		lsb_off	sub_b		sub_g		sub_r		subpix_en	fphase_bit			fphase_sel		fphase_ctrl	
Type		RW	RW		RW		RW		RW	RW			RW		RW	
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	h_active	**Active region of dither IP**
14	lsb_off	**Turns off LSB for dither function**
13:12	sub_b	**Dither SubPixel addend**
11:10	sub_g	**Dither SubPixel addend**
9:8	sub_r	**Dither SubPixel addend**
7	subpix_en	**Enables sub pix dither mode** 0: Pix dither mode 1: Sub pix dither mode
6:4	fphase_bit	**fphase_bit XOR bus number** *Note: This function checks reg_fphase_sel. Only 0, 1, 2, 4 and 6 are available.* 0: No effect on fphase (XOR disabled)
3:2	fphase_sel	**fphase XOR function: fphase does self bit-wise xor** *Note: This function checks reg_fphase_sel. Only bit 2, bit 4 and bit 6 are available.* 0: Disable fphase XOR 1: Effect fphase[0]~[1] base on the value of reg_fphase_sel is 1 or 2 2: Effect fphase[0]~[3] base on the value of reg_fphase_sel is 1, 2 or 4 3: Effect fphase[0]~[5] base on the value of reg_fphase_sel is 1, 2, 4 or 6
1:0	fphase_ctrl	**Selects fphase range to add with rdither table** 00: 0~63 01: 0~16 10: 0~3

140050BC MDP_WROT_VIDO_DITHE VIDO Dithering Control Register 6 00000000

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R_06

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											**debug_mode**		**new_bit_mode**	**diff_shift**		
Type											RW		RW	RW		
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**testpin_en**	**rshift_b**				**rshift_g**				**rshift_r**					**table_en**	
Type	RW	RW				RW				RW					RW	
Reset	0	0	0	0		0	0	0		0	0	0			0	0

Bit(s)	Name	Description
21:20	debug_mode	**1: Enable debugging mode**
19	new_bit_mode	**1: Enable modified test algorithm**
18:16	diff_shift	**Debugging mode difference shift positions**
15	testpin_en	**Enables testpin input**
14:12	rshift_b	**B right shift position after IP output**
10:8	rshift_g	**G right shift position after IP output**
6:4	rshift_r	**R right shift position after IP output**
1:0	table_en	**Active bit of magic table for running order** 01: Phase active in bit3 ~ bit0 10: Phase active in bit1 ~ bit0 Else phase active in bit5 ~ bit0

140050C0 **MDP_WROT_VIDO_DITHER_07** **VIDO Dithering Control Register 7** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**lsb_err_shift_r**				**ovflw_bit_r**				**add_lshift_r**				**input_rshift_r**		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
14:12	lsb_err_shift_r	Selects RED LSB error bit
10:8	ovflw_bit_r	Selects RED overflow bit
6:4	add_lshift_r	RED addend left shift bits
2:0	input_rshift_r	RED input right shift bits

140050C4 **MDP_WROT_VIDO_DITHER_08** **VIDO Dithering Control Register 8** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

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Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		lsb_err_shift_g				ovflw_bit_g				add_lshift_g				input_rshift_g		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
14:12	lsb_err_shift_g	Selects BLUE LSB error bit
10:8	ovflw_bit_g	Selects BLUE overflow bit
6:4	add_lshift_g	BLUE addend left shift bits
2:0	input_rshift_g	BLUE input right shift bits

140050C8 MDP_WROT_VIDO_DITHER_09 VIDO Dithering Control Register 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		lsb_err_shift_b				ovflw_bit_b				add_lshift_b				input_rshift_b		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
14:12	lsb_err_shift_b	Selects GREEN LSB error bit
10:8	ovflw_bit_b	Selects GREEN overflow bit
6:4	add_lshift_b	GREEN addend left shift bits
2:0	input_rshift_b	GREEN input right shift bits

140050CC MDP_WROT_VIDO_DITHER_10 VIDO Dithering Control Register 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																crc_rdy
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	crc_out															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	crc_rdy	CRC ready
15:0	crc_out	CRC result

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140050D0 **MDP_WROT_VIDO_DEBUG** **VIDO Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	debug_out[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	debug_out[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	debug_out	Debug out

140050D4 **MDP_WROT_VIDO_ARB_SW_CTL** **VIDO DMA Arbiter Software Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														dma_arb_sw_ctl_sel		dma_arb_sw_ctl_en
Type														RW		RW
Reset														0	0	0

Bit(s)	Name	Description
2:1	dma_arb_sw_ctl_sel	Selects DMA arbiter channel
0	dma_arb_sw_ctl_en	Enables software control DMA arbiter.

140050E0 **MDP_WROT_TRACK_CTL** **MDP WROT Pre-ultra Track Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												proc_track_pre_ultra_mux	proc_track_pause_track	proc_track_ignore_init_latency	proc_track_stop_greq_en	proc_track_pre_ultra_en
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	proc_track_pre_ultra_mux	Selects the pre-ultra signal from FIFO or proc_track engine

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Bit(s)	Name	Description
3	proc_track_pause_track	Pause tracking
2	proc_track_ignore_init_latency	Ignores the initial latency from SOF to the first pixel
1	proc_track_stop_greq_en	Enables proc_track stop greq function
0	proc_track_pre_ultra_en	Enables proc_track pre-ultra function

140050E4 **MDP_WROT_TRACK_WINDOW** **MDP WROT Pre-ultra Track Window** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					proc_track_window											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	proc_track_window	Proc_track window

140050E8 **MDP_WROT_TRACK_TARGET** **MDP WROT Pre-ultra Track Target** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									proc_track_target_cnt[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	proc_track_target_cnt[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	proc_track_target_cnt	Proc_track target count

140050EC **MDP_WROT_TRACK_STOP** **MDP WROT Pre-ultra Track Stop** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									proc_track_stop_cnt[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	proc_track_stop_cnt[15:0]															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	proc_track_stop_cnt	Proc_track stop count

140050F0 **MDP_WROT_TRACK_PROC_CNT0** **MDP WROT Pre-ultra Track Proc Counter 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**proc_track_proc_cnt_0[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**proc_track_proc_cnt_0[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	proc_track_proc_cnt_0	Proc_track processing count low byte

140050F4 **MDP_WROT_TRACK_PROC_CNT1** **MDP WROT Pre-ultra Track Proc Counter 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**proc_track_proc_cnt_1**
Type																RU
Reset																0

Bit(s)	Name	Description
0	proc_track_proc_cnt_1	Proc_track processing count high byte

14005F00 **MDP_WROT_VIDO_BASE_ADDR** **VIDO Base Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**VIDO_BASE_ADDR[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**VIDO_BASE_ADDR[15:0]**															

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Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VIDO_BASE_ADDR	**Double buffer** VIDO base address 1. The definition of this base address depends on the format: 1. One plane format: Base address of plane-1 2. Two plane format: Base address of plane-1

14005F04 **MDP_WROT_VIDO_BASE_ADDR_C** **VIDO Base Address Chroma** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VIDO_BASE_ADDR_C[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_BASE_ADDR_C[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VIDO_BASE_ADDR_C	**Double buffer** VIDO base address 2. The definition of this base address depends on the format: 1. One plane format: Don't care. 2. Two plane format: Base address of plane-2

14005F08 **MDP_WROT_VIDO_BASE_ADDR_V** **VIDO Base Address Chroma 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VIDO_BASE_ADDR_V[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_BASE_ADDR_V[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VIDO_BASE_ADDR_V	**Double buffer** VIDO base address 3. The definition of this base address depends on the format: 1. One plane format, two plane format: Don't care. 2. Three plane format: V plane

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6.9.5 Programming Guide

6.9.5.1 Firmware Settings for Rotation/Flip

To output data to DRAM with rotation/flip, ROT_DMA should calculate the correct address to put the first data. Then the next data can be written in certain order which also depends on rotation/flip settings. However, the circuit for calculating the address to put the first data is only applied in the beginning of the entire image or tile. For cost effectiveness, the address offset for the first data compared to BASE_ADDR can be calculated by firmware and transferred into hardware by register OFST_ADDR. For all kinds of rotation/flip settings, the required positions of OFST_ADDR are different. The illustrations for the position of OFST_ADDR on DRAM footprint is shown in Figure 6-21 to Figure 6-24. Note that the xsize and ysize are defined according to input data scan-line direction. The direction of xsize is parallel to input scan-line direction, and the direction of ysize is perpendicular to input scan-line direction. The stride setting is defined according to DRAM footprint, which is the direction after rotation/flip.

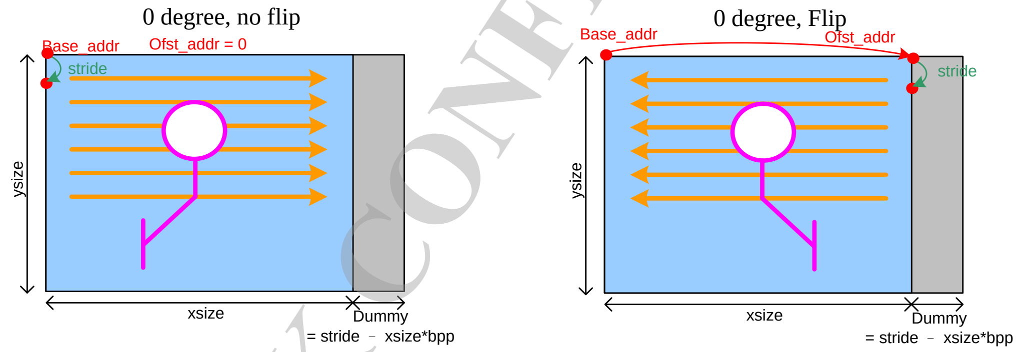

Figure 6-21. Firmware settings of OFST_ADDR in 0° rotation (scan-line)

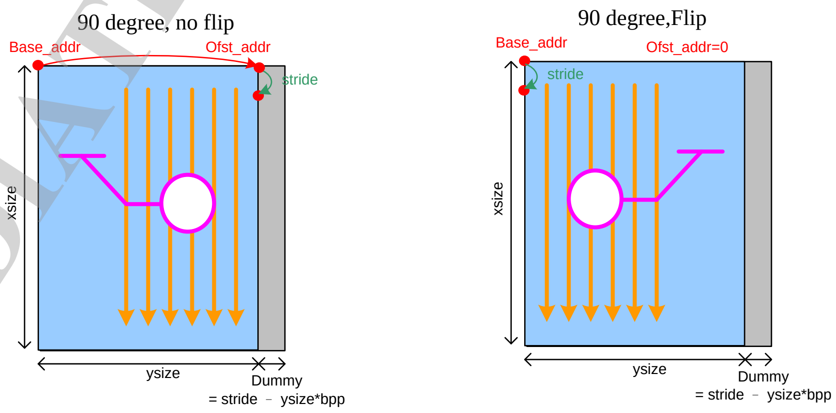

Figure 6-22. Firmware settings of OFST_ADDR in 90° rotation (scan-line)

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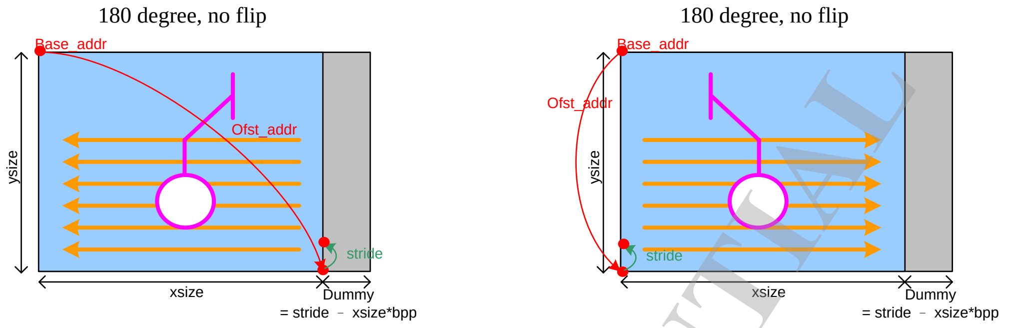

Figure 6-23. Firmware settings of OFST_ADDR in 180° rotation (scan-line)

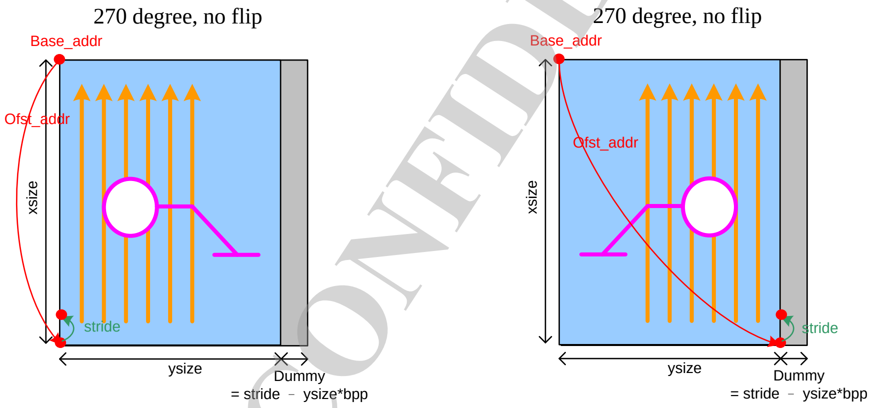

Figure 6-24. Firmware settings of OFST_ADDR in 270° rotation (scan-line)

Summary is given in Table 6-5.

Table 6-5. ROT_DMA OFST_ADDR settings for rotation/flip

Rotation	No Flip (Flip = 0)	Horizontal Flip (Flip = 1)
0 degree (Rotation=0)	0	Xsize-1
90 degree (Rotation=1)	Ysize-1	0
180 degree (Rotation=2)	Stride*(Ysize-1) +(Xsize-1)	Stride*(Ysize-1)
270 degree (Rotation=3)	Stride*(xsize-1)	Stride*(Xsize-1) +(Ysize-1)

For an interpolation based UV-resampler, which can perform better quality for YUV420, VIDO UVSEL should be set corresponding to different rotation/flip settings. According to Table 6-6, the suggested settings provide the proper chroma sampled points.

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Table 6-6. VIDO UV SEL for YUV420 format cooperated with CRSP

Rotation	Flip	UV_SELX	UV_SELY
0	0	0	1
0	1	1	1
1	0	0	0
1	1	0	0
2	0	1	1
2	1	0	1
3	0	0	1
3	1	0	1

6.9.5.2 Working Buffer Height Setting

Setting up the buffer width and buffer height for ROT_DMA is necessary, no matter the rotation is enabled or not. Set N mod M = 0 for better performance. If N mod M is not 0, and you would like the efficiency to drop as little as possible, derive an algorithm for height calculation.

First of all, you need to know the buffer size for each format.

```
if (UYVY 2-plane or 3-plane)
     y_max_buf_size = 256x48
    uv_max_buf_size = 128x48
else if (YUV420)
     y_max_buf_size = 256x64
    uv_max_buf_size = 128x32
else
     y_max_buf_size = 256x32
    uv_max_buf_size = 256x32
```

Algorithm: (Width is tile width.)

Phase 1:

We can apply the algorithm on Y channel first to get the approximation first.

Coeff 1= floor (MAX_BUF_SIZE / WIDTH/2) *2
Coeff 2= Ceiling (WIDTH / Coeff1)
Buf_line_num= Ceiling (WIDTH/Coeff 2/ 4) *4 (To make sure if Buf_line_num mod 4 = 0)

If (buf_line_num > width)
Buf_line_num = ceiling (width / 4) * 4 (To make sure width >= Buf_line_num)

else if (Buf_line_num * Buf_line_num * Coeff 2 > MAX_BUF_SIZE) (buffer overflow)
Buf_line_num = buf_height.

Phase 2:

Check if the setting is over the buffer size or not.

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```
Y_buf_check =0
Uv_buf_check =0

//internal buffer check
while ((y_buf_check !=0) | (uv_buf_check!=0)){

        // Y buffer check
        Internal_y_buf_width = Ceiling(width/buf_line_num) x buf_line_num //multiple of
buf_line_num and >= width
        Internal_y_buf_usage = Internal_y_buf_width x buf_line_num
        If (internal_y_buf_usage > y_max_buf_size){
              buf_line_num = buf_line_num -4
             Y_buf_check =0
               Uv_buf_check =0
        }else{
              Y_buf_check =1
        }

        // UV buffer check
        if (YUV422 rotate 0/180)
              Uv_blk_width = main_blk_width/2
              Uv_blk_line     = main_buf_line_num
        Else if ((YUV422 rotate 90/270)
              Uv_blk_width = main_blk_width
              Uv_blk_line     = main_buf_line_num/2
        Else if (YUV420)
              Uv_blk_width = main_blk_width/2
              Uv_blk_line     = main_buf_line_num/2
      Else
               Uv_blk_width = main_blk_width
              Uv_blk_line     = main_buf_line_num

        Internal_uv_buf_width = Ceiling(Uv_blk_width / Uv_blk_line)x Uv_blk_line

        Internal_uv_buf_usage = Uv_blk_width x Uv_blk_line
        If (internal_uv_buf_usage > uv_max_buf_size){
              Main_buf_line_num = maian_buf_line_num -4
             Y_buf_check =0
               Uv_buf_check =0
        }else{
              uv_buf_check =1
        }
}
```


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6.9.5.3 SMI 256 Byte Boundary Restriction

6.9.5.3.1 Methods to Handle Boundary Restriction

SMI has a restriction that any burst issued from DMA cannot cross the 256-byte address boundary, no matter in read or write action. The reason is from the bank configuration in SMI, where the 256-byte address is only the bank switching point.

Here we try to analyze the probability of crossing the 256-byte boundary by random access. As illustrated in Figure 6-25. The probability P is

P = (byte per burst length)/256

It depends on the designed burst length of ROT_DMA. For example, if the minimum burst length 4-16, the probability P = 64/256 = ¼, which means that 25% burst request will be separated. Though the total data amount is fixed, it increases 25% burst request times and will reduce DRAM access utility.

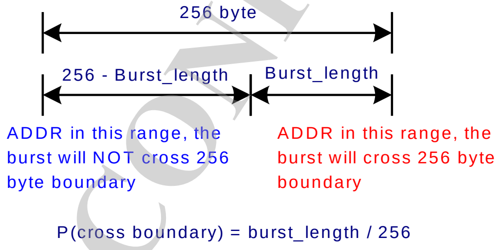

Figure 6-25. Probability of crossing 256-byte boundary by random access

To handle this restriction from SMI, there are two common solutions. One is adopting a burst separator between ROT_DMA and SMI port. As illustrated in Figure 6-26, the original DMA requests are represented in black arrow. Because it is not considered 256 byte boundary restriction, some requests should be cross the 256-byte boundary. The burst separator filters all requests from ROT_DMA, which allows the legal request pass as represented in blue arrows but separate the illegal request into two requests as represented in yellow arrows. Although it is simple to implement, it increases the total request number.

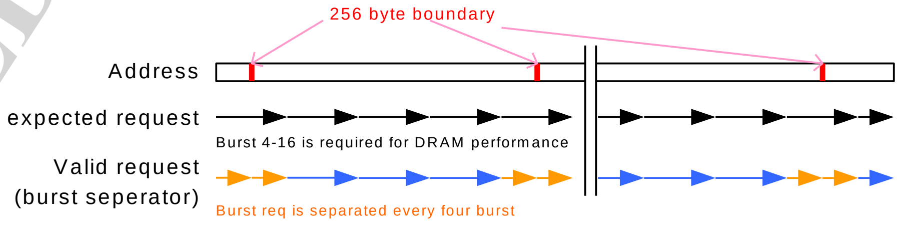

Figure 6-26. Scan-line request without considering 256-byte boundary

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The second method is handling the 256-byte boundary restriction inside the control logics of ROT_DMA. After the data are stored in burst accumulator, ROT_DMA will adjust the burst length to meet the boundary when the target address is close to the 256-byte boundary. In common cases, the minimum burst length is a factor of 256 bytes; therefore the requests after the adjusted request will automatically align with the 256-byte boundary. This method is difficult to implement but can efficiently reduce the overhead of DMA requests (see Figure 6-27).

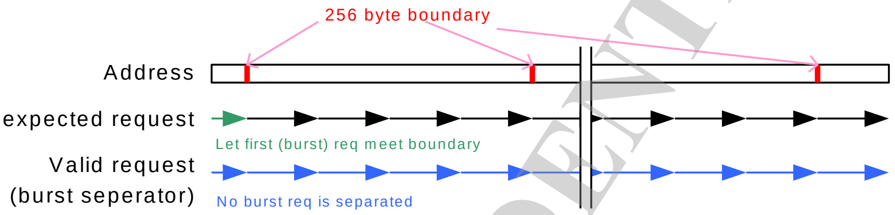

Figure 6-27. Scan-line request considering 256-byte boundary

6.9.5.3.2 SMI Boundary Restriction In Case of Rotation

The method described in the previous section is based on continuous scan-line access of DMA. It works only in 0° or 180° rotation with or without flip. Unfortunately, it does not always work in 90° or 270° rotation with or without flip. Considering a general condition with 90° or 270° rotation, if the stride is not multiple of 256 bytes, the distribution of 256-byte boundary will differ in every line as described in Figure 6-28. To handle this, the SMI_IF controller issues requests with different burst lengths according to the current address.

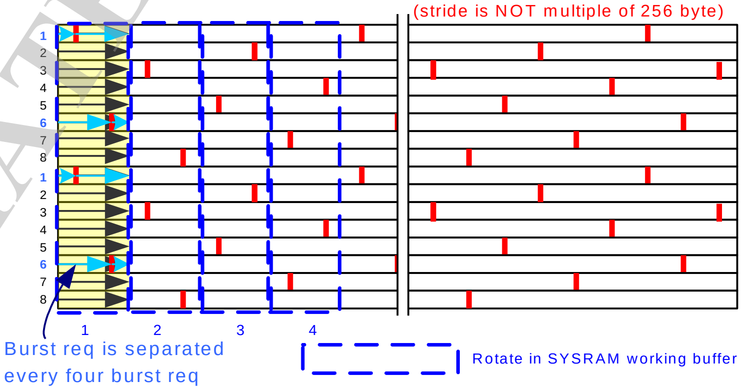

Figure 6-28. 4-16 burst in 270° rotation with/without flip

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6.10 Display 2D Sharpness

6.10.1 Introduction

The sharpness function provides better picture quality for panel display. It restores the image details, sharpens the edge and provides a vivid feeling for pictures and videos.

6.10.2 Features

- 2-dimensional sharpness filter
- Peaking by color (PBC)

6.10.3 Block Diagram

Figure 6-29 is the block diagram of display 2D sharpness. The FIFO unit is used to pre-fetch pixel data, and thus the overall throughput can be improved in some situations.

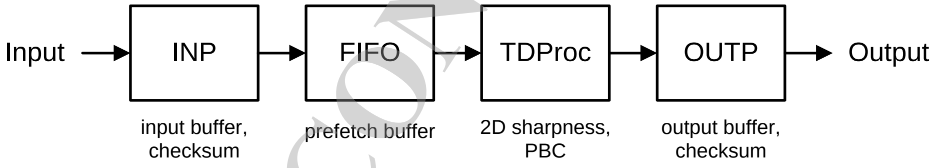

Figure 6-29. Block diagram of display 2D sharpness

Figure 6-30 is the block diagram of the sharpness core. The luminance data will be processed and modified in the sharpness function. The chrominance data will flow into PBC, but no modification at the output.

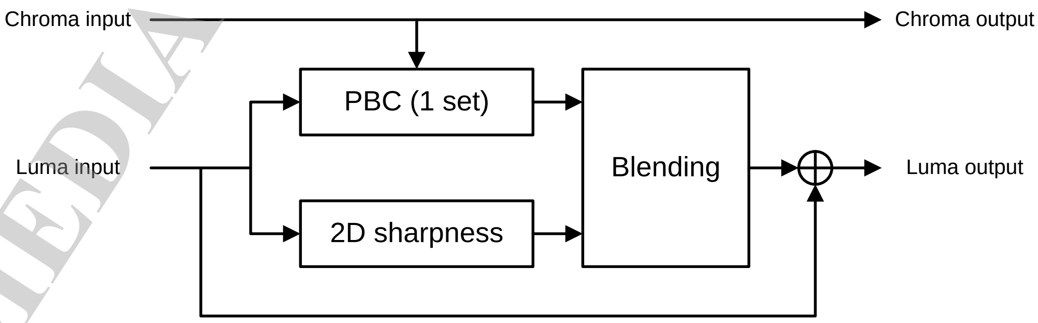

Figure 6-30. Block diagram of sharpness core

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6.10.3.1 2-dimensional Sharpness

The 2D filters are used to extract middle/high-frequency components from the input signal. Each extracted AC component is enhanced individually and then added back to the input signal. The enhancement units are composed by coring, gain, limit and clip.

Before 2-dimensional sharpness After 2-dimensional sharpness

Figure 6-31. Visual effect of 2-dimensional sharpness

6.10.3.2 Peaking by Color

Sometimes you may prefer different sharpness levels in different color tones. PBC is used for such preference. PBC detects at most three different colors and applies different sharpness levels to them.

Before green PBC After green PBC

Figure 6-32. Visual effect of peaking by color

6.10.4 Register Definition

Module name: MDP_TDSHP Base address: (+14006000h)

Address	Name	Width	Register Function

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Address	Name	Width	Register Function
14006000	**MDP_TDSHP_00**	32	MDP_TDSHP_00
14006004	**MDP_TDSHP_01**	32	MDP_TDSHP_01
14006008	**MDP_TDSHP_02**	32	MDP_TDSHP_02
1400600C	**MDP_TDSHP_03**	32	MDP_TDSHP_03
14006014	**MDP_TDSHP_05**	32	MDP_TDSHP_05
14006018	**MDP_TDSHP_06**	32	MDP_TDSHP_06
1400601C	**MDP_TDSHP_07**	32	MDP_TDSHP_07
14006020	**MDP_TDSHP_08**	32	MDP_TDSHP_08
14006024	**MDP_TDSHP_09**	32	MDP_TDSHP_09
14006040	**MDP_PBC_00**	32	MDP_PBC_00
14006044	**MDP_PBC_01**	32	MDP_PBC_01
14006048	**MDP_PBC_02**	32	MDP_PBC_02
1400604C	**MDP_PBC_03**	32	MDP_PBC_03
14006050	**MDP_PBC_04**	32	MDP_PBC_04
14006054	**MDP_PBC_05**	32	MDP_PBC_05
14006058	**MDP_PBC_06**	32	MDP_PBC_06
1400605C	**MDP_PBC_07**	32	MDP_PBC_07
14006060	**MDP_PBC_08**	32	MDP_PBC_08
14006064	**MDP_HIST_CFG_00**	32	MDP_HIST_CFG_00
14006068	**MDP_HIST_CFG_01**	32	MDP_HIST_CFG_01
1400606C	**MDP_LUMA_HIST_00**	32	Result of Luma Histogram 0
14006070	**MDP_LUMA_HIST_01**	32	Result of Luma Histogram 1
14006074	**MDP_LUMA_HIST_02**	32	Result of Luma Histogram 2
14006078	**MDP_LUMA_HIST_03**	32	Result of Luma Histogram 3
1400607C	**MDP_LUMA_HIST_04**	32	Result of Luma Histogram 4
14006080	**MDP_LUMA_HIST_05**	32	Result of Luma Histogram 5
14006084	**MDP_LUMA_HIST_06**	32	Result of Luma Histogram 6
1400608C	**MDP_LUMA_HIST_07**	32	Result of Luma Histogram 7
14006090	**MDP_LUMA_HIST_08**	32	Result of Luma Histogram 8
14006094	**MDP_LUMA_HIST_09**	32	Result of Luma Histogram 9
14006098	**MDP_LUMA_HIST_10**	32	Result of Luma Histogram 10
1400609C	**MDP_LUMA_HIST_11**	32	Result of Luma Histogram 11
140060A0	**MDP_LUMA_HIST_12**	32	Result of Luma Histogram 12
140060A4	**MDP_LUMA_HIST_13**	32	Result of Luma Histogram 13
140060A8	**MDP_LUMA_HIST_14**	32	Result of Luma Histogram 14
140060AC	**MDP_LUMA_HIST_15**	32	Result of Luma Histogram 15
140060B0	**MDP_LUMA_HIST_16**	32	Result of Luma Histogram 16
140060B4	**MDP_LUMA_SUM**	32	Result of Luma Sum
140060BC	**MDP_Y_FTN_1_0_MAIN**	32	2nd Y Transfer Function 1, 0
140060C0	**MDP_Y_FTN_3_2_MAIN**	32	2nd Y Transfer Function 3, 2
140060C4	**MDP_Y_FTN_5_4_MAIN**	32	2nd Y Transfer Function 5, 4
140060C8	**MDP_Y_FTN_7_6_MAIN**	32	2nd Y Transfer Function 7, 6
140060CC	**MDP_Y_FTN_9_8_MAIN**	32	2nd Y Transfer Function 9, 8

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Address	Name	Width	Register Function
140060D0	MDP_Y_FTN_11_10_MAIN	32	2nd Y Transfer Function 11, 10
140060D4	MDP_Y_FTN_13_12_MAIN	32	2nd Y Transfer Function 13, 12
140060D8	MDP_Y_FTN_15_14_MAIN	32	2nd Y Transfer Function 15, 14
140060DC	MDP_Y_FTN_17_16_MAIN	32	2nd Y Transfer Function 17, 16
140060E0	MDP_C_BOOST_MAIN	32	Chroma Boost
140060E4	MDP_C_BOOST_MAIN_2	32	Chroma Boost 2
14006100	MDP_TDSHP_CTRL	32	MDP_TDSHP_CTRL
14006104	MDP_TDSHP_INTEN	32	MDP_TDSHP_INTEN
14006108	MDP_TDSHP_INTSTA	32	MDP_TDSHP_INTSTA
1400610C	MDP_TDSHP_STATUS	32	MDP_TDSHP_STATUS
14006110	MDP_TDSHP_CFG	32	MDP_TDSHP_CFG
14006114	MDP_TDSHP_INPUT_COUNT	32	TDSHP Input I/F Debug Counter Register
14006118	MDP_TDSHP_CHKSUM	32	TDSHP Checksum Register
1400611C	MDP_TDSHP_OUTPUT_COUNT	32	TDSHP Output I/F Debug Counter Register
14006120	MDP_TDSHP_INPUT_SIZE	32	MDP_TDSHP_INPUT_SIZE
14006124	MDP_TDSHP_OUTPUT_OFFSET	32	MDP_TDSHP_OUTPUT_OFFSET
14006128	MDP_TDSHP_OUTPUT_SIZE	32	MDP_TDSHP_OUTPUT_SIZE
1400612C	MDP_TDSHP_BLANK_WIDTH	32	MDP_TDSHP_BLANK_WIDTH
14006130	MDP_TDSHP_DEMO_HMASK	32	MDP_TDSHP_DEMO_HMASK
14006134	MDP_TDSHP_DEMO_VMASK	32	MDP_TDSHP_DEMO_VMASK
14006200	MDP_LUMA_HIST_INIT_00	32	MDP_LUMA_HIST_INIT_00
14006204	MDP_LUMA_HIST_INIT_01	32	MDP_LUMA_HIST_INIT_01
14006208	MDP_LUMA_HIST_INIT_02	32	MDP_LUMA_HIST_INIT_02
1400620C	MDP_LUMA_HIST_INIT_03	32	MDP_LUMA_HIST_INIT_03
14006210	MDP_LUMA_HIST_INIT_04	32	MDP_LUMA_HIST_INIT_04
14006214	MDP_LUMA_HIST_INIT_05	32	MDP_LUMA_HIST_INIT_05
14006218	MDP_LUMA_HIST_INIT_06	32	MDP_LUMA_HIST_INIT_06
1400621C	MDP_LUMA_HIST_INIT_07	32	MDP_LUMA_HIST_INIT_07
14006220	MDP_LUMA_HIST_INIT_08	32	MDP_LUMA_HIST_INIT_08
14006224	MDP_LUMA_HIST_INIT_09	32	MDP_LUMA_HIST_INIT_09
14006228	MDP_LUMA_HIST_INIT_10	32	MDP_LUMA_HIST_INIT_10

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Address	Name	Width	Register Function
1400622C	**MDP_LUMA_HIST_INIT_11**	32	MDP_LUMA_HIST_INIT_11
14006230	**MDP_LUMA_HIST_INIT_12**	32	MDP_LUMA_HIST_INIT_12
14006234	**MDP_LUMA_HIST_INIT_13**	32	MDP_LUMA_HIST_INIT_13
14006238	**MDP_LUMA_HIST_INIT_14**	32	MDP_LUMA_HIST_INIT_14
1400623C	**MDP_LUMA_HIST_INIT_15**	32	MDP_LUMA_HIST_INIT_15
14006240	**MDP_LUMA_HIST_INIT_16**	32	MDP_LUMA_HIST_INIT_16
14006244	**MDP_LUMA_SUM_INIT**	32	MDP_LUMA_SUM_INIT

14006000 **MDP_TDSHP_00** **MDP_TDSHP_00** **00102010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**TDS_EN**	**TDS_BYPASS_MID**	**TDS_BYPASS_HIGH**	**TDS_ADAP_LUMA_BP**			**TDS_INK_SEL**		**TDS_GAIN_MID**							
Type	RW	RW	RW	RW			RW		RW							
Reset	0	0	0	0			0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TDS_GAIN_HIGH**								**TDS_COR_GAIN**							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31	TDS_EN	**Enables 2D sharpness**
30	TDS_BYPASS_MID	**Bypasses middle band**
29	TDS_BYPASS_HIGH	**Bypasses high band**
28	TDS_ADAP_LUMA_BP	**Bypasses adaptive luma** 0: Normal function 1: Bypass
25:24	TDS_INK_SEL	**Selects ink mode** 2'd0: Disable ink mode 2'd1: Ink mode of difference at final output 2'd2: PBC coverage ink 2'd3: PBC strength ink
23:16	TDS_GAIN_MID	**Mid-band gain before merge**
15:8	TDS_GAIN_HIGH	**High-band gain before merge**
7:0	TDS_COR_GAIN	**Final AC soft coring gain** TDS_GAIN*[(TDS_COR_RATIO + 8) >> 4]

14006004 **MDP_TDSHP_01** **MDP_TDSHP_01** **04020208**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**TDS_COR_THR**								**TDS_COR_ZERO**							

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Type	RW								RW							
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**TDS_GAIN**								**TDS_LIMIT_RATIO**			
Type					RW								RW			
Reset					0	0	1	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
31:24	TDS_COR_THR	**Final AC coring threshold**
23:16	TDS_COR_ZERO	**Final AC zero threshold**
11:4	TDS_GAIN	**Final AC gain** Gain = reg/0x20
3:0	TDS_LIMIT_RATIO	**Final AC soft limit ratio**

14006008 MDP_TDSHP_02 MDP_TDSHP_02 18300300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**TDS_LIMIT**								**TDS_BOUND**							
Type	RW								RW							
Reset	0	0	0	1	1	0	0	0	0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TDS_COR_VALUE**															
Type	RW															
Reset	0	0	0	0	0	0	1	1								

Bit(s)	Name	Description
31:24	TDS_LIMIT	**Final AC positive limit**
23:16	TDS_BOUND	**Final AC postive bound**
15:8	TDS_COR_VALUE	**Final AC coring value** TDS_COR_ZERO + [(TDS_COR_THR - TDS_COR_ZERO)*(16 - TDS_COR_RATIO) + 8] >> 4

1400600C MDP_TDSHP_03 MDP_TDSHP_03 8802080A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**TDS_CLIP_EN**				**TDS_CLIP_RATIO**				**TDS_CLIP_THR**							
Type	RW				RW				RW							
Reset	1				1	0	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**TDS_AC_LPF_COE**						**TDS_SAT_PROC**					
Type					RW						RW					
Reset					1	0	0	0			0	0	1	0	1	0

Bit(s)	Name	Description
31	TDS_CLIP_EN	**Final AC clip enable**
27:24	TDS_CLIP_RATIO	**Final AC clip ratio**
23:16	TDS_CLIP_THR	**Final AC clip positive threshold**
11:8	TDS_AC_LPF_COE	**0: Disable**

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Bit(s)	Name	Description
		1~15: As old design
5:0	TDS_SAT_PROC	**Saturation process strength** Max. value: 32

14006014 MDP_TDSHP_05 MDP_TDSHP_05 00183048

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDS_YLEV_P000								TDS_YLEV_P016							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDS_YLEV_P032								TDS_YLEV_P048							
Type	RW								RW							
Reset	0	0	1	1	0	0	0	0	0	1	0	0	1	0	0	0

Bit(s)	Name	Description
31:24	TDS_YLEV_P000	**Y level dependent sharpness point 0** Gain = reg/0x80
23:16	TDS_YLEV_P016	**Y level dependent sharpness point 64** Gain = reg/0x80
15:8	TDS_YLEV_P032	**Y level dependent sharpness point 128** Gain = reg/0x80
7:0	TDS_YLEV_P048	**Y level dependent sharpness point 192** Gain = reg/0x80

14006018 MDP_TDSHP_06 MDP_TDSHP_06 60687078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDS_YLEV_P064								TDS_YLEV_P080							
Type	RW								RW							
Reset	0	1	1	0	0	0	0	0	0	1	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDS_YLEV_P096								TDS_YLEV_P112							
Type	RW								RW							
Reset	0	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0

Bit(s)	Name	Description
31:24	TDS_YLEV_P064	**Y level dependent sharpness point 256** Gain = reg/0x80
23:16	TDS_YLEV_P080	**Y level dependent sharpness point 320** Gain = reg/0x80
15:8	TDS_YLEV_P096	**Y level dependent sharpness point 384** Gain = reg/0x80
7:0	TDS_YLEV_P112	**Y level dependent sharpness point 448** Gain = reg/0x80

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14006 01C **MDP_TDSHP_07** **MDP_TDSHP_07** **807B7670**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDS_YLEV_P128								TDS_YLEV_P144							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDS_YLEV_P160								TDS_YLEV_P176							
Type	RW								RW							
Reset	0	1	1	1	0	1	1	0	0	1	1	1	0	0	0	0

Bit(s)	Name	Description
31:24	TDS_YLEV_P128	**Y level dependent sharpness point 512** Gain = reg/0x80
23:16	TDS_YLEV_P144	**Y level dependent sharpness point 576** Gain = reg/0x80
15:8	TDS_YLEV_P160	**Y level dependent sharpness point 640** Gain = reg/0x80
7:0	TDS_YLEV_P176	**Y level dependent sharpness point 704** Gain = reg/0x80

14006020 **MDP_TDSHP_08** **MDP_TDSHP_08** **6B66605B**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDS_YLEV_P192								TDS_YLEV_P208							
Type	RW								RW							
Reset	0	1	1	0	1	0	1	1	0	1	1	0	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDS_YLEV_P224								TDS_YLEV_P240							
Type	RW								RW							
Reset	0	1	1	0	0	0	0	0	0	1	0	1	1	0	1	1

Bit(s)	Name	Description
31:24	TDS_YLEV_P192	**Y level dependent sharpness point 768** Gain = reg/0x80
23:16	TDS_YLEV_P208	**Y level dependent sharpness point 832** Gain = reg/0x80
15:8	TDS_YLEV_P224	**Y level dependent sharpness point 896** Gain = reg/0x80
7:0	TDS_YLEV_P240	**Y level dependent sharpness point 960** Gain = reg/0x80

14006024 **MDP_TDSHP_09** **MDP_TDSHP_09** **56104000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDS_YLEV_P256										TDS_YLEV_ALPHA					
Type	RW										RW					
Reset	0	1	0	1	0	1	1	0			0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TDS_														

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		YLEV_EN														
Type		RW														
Reset		1														

Bit(s)	Name	Description
31:24	TDS_YLEV_P256	**Y level dependent sharpness point 1024** Gain = reg/0x80
21:16	TDS_YLEV_ALPHA	**Y level dependent sharpness blending alpha**
14	TDS_YLEV_EN	**Enables Y level dependent sharpness**

14006040 MDP_PBC_00 MDP_PBC_00 8C02730C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**PBC1_EN**	**PBC1_LPF_EN**	**PBC1_GAIN**								**PBC1_RSLOPE_1[9:4]**					
Type	RW	RW	RW								RW					
Reset	1	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**PBC1_RSLOPE_1[3:0]**				**PBC1_THETA_R**						**PBC1_RADIUS_R**					
Type	RW				RW						RW					
Reset	0	1	1	1	0	0	1	1	0	0	0	0	1	1	0	0

Bit(s)	Name	Description
31	PBC1_EN	0: Disable 1: Enable
30	PBC1_LPF_EN	Enables PBC low-pass filter
29:22	PBC1_GAIN	PBC band gain
21:12	PBC1_RSLOPE_1	For (PBC_RADIUS_C < PBC_RADIUS_RANGE); 1024/PBC_RADIUS_C
11:6	PBC1_THETA_R	Theta range for PBC
5:0	PBC1_RADIUS_R	Radius range for PBC

14006044 MDP_PBC_01 MDP_PBC_01 7F1A1550

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**PBC1_THETA_C**								**PBC1_RADIUS_C**							
Type	RW								RW							
Reset	0	1	1	1	1	1	1	1	0	0	0	1	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**PBC1_TSLOPE**										**PBC1_LPF_GAIN**					
Type	RW										RW					
Reset	0	0	0	1	0	1	0	1	0	1	0	1	0	0	0	0

Bit(s)	Name	Description
31:24	PBC1_THETA_C	Theta center for PBC
23:16	PBC1_RADIUS_C	Radius center for PBC
15:6	PBC1_TSLOPE	1024/PBC_THETA_RANGE
5:0	PBC1_LPF_GAIN	PBC low-pass filter gain

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14006048 MDP_PBC_02 MDP_PBC_02 15410C20

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PBC1_RSLOPE												PBC1_CONF_GAIN			
Type	RW												RW			
Reset	0	0	0	1	0	1	0	1	0	1			0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PBC1_EDGE_EN	PBC1_EDGE_THR								PBC1_EDGE_SLOPE					
Type		RW	RW								RW					
Reset		0	0	0	1	1	0	0			1	0	0	0	0	0

Bit(s)	Name	Description
31:22	PBC1_RSLOPE	1024/PBC_RADIUS_RANGE
19:16	PBC1_CONF_GAIN	PBC confidence gain
14	PBC1_EDGE_EN	Enables PBC edge preservation
13:8	PBC1_EDGE_THR	PBC edge threshold
5:0	PBC1_EDGE_SLOPE	PBC edge slope

1400604C MDP_PBC_03 MDP_PBC_03 C4020618

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PBC2_EN	PBC2_LPF_EN	PBC2_GAIN								PBC2_RSLOPE_1[9:4]					
Type	RW	RW	RW								RW					
Reset	1	1	0	0	0	1	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PBC2_RSLOPE_1[3:0]				PBC2_THETA_R						PBC2_RADIUS_R					
Type	RW				RW						RW					
Reset	0	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0

Bit(s)	Name	Description
31	PBC2_EN	0: Disable 1: Enable
30	PBC2_LPF_EN	Enables PBC low-pass filter
29:22	PBC2_GAIN	PBC band gain
21:12	PBC2_RSLOPE_1	For (PBC_RADIUS_C < PBC_RADIUS_RANGE); 1024/PBC_RADIUS_C
11:6	PBC2_THETA_R	Theta range for PBC
5:0	PBC2_RADIUS_R	Radius range for PBC

14006050 MDP_PBC_04 MDP_PBC_04 60200AD0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PBC2_THETA_C								PBC2_RADIUS_C							
Type	RW								RW							
Reset	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PBC2_TSLOPE										PBC2_LPF_GAIN					
Type	RW										RW					
Reset	0	0	0	0	1	0	1	0	1	1	0	1	0	0	0	0

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Bit(s)	Name	Description
31:24	PBC2_THETA_C	Theta center for PBC
23:16	PBC2_RADIUS_C	Radius center for PBC
15:6	PBC2_TSLOPE	1024/PBC_THETA_RANGE
5:0	PBC2_LPF_GAIN	PBC low-pass filter gain

14006054 MDP_PBC_05 MDP_PBC_05 0AC54C20

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PBC2_RSLOPE												PBC2_CONF_GAIN			
Type	RW												RW			
Reset	0	0	0	0	1	0	1	0	1	1			0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PBC2_EDGE_EN	PBC2_EDGE_THR								PBC2_EDGE_SLOPE					
Type		RW	RW								RW					
Reset		1	0	0	1	1	0	0			1	0	0	0	0	0

Bit(s)	Name	Description
31:22	PBC2_RSLOPE	1024/PBC_RADIUS_RANGE
19:16	PBC2_CONF_GAIN	PBC confidence gain
14	PBC2_EDGE_EN	Enables PBC edge preservation
13:8	PBC2_EDGE_THR	PBC edge threshold
5:0	PBC2_EDGE_SLOPE	PBC edge slope

14006058 MDP_PBC_06 MDP_PBC_06 89011420

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PBC3_EN	PBC3_LPF_EN	PBC3_GAIN								PBC3_RSLOPE_1[9:4]					
Type	RW	RW	RW								RW					
Reset	1	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PBC3_RSLOPE_1[3:0]				PBC3_THETA_R						PBC3_RADIUS_R					
Type	RW				RW						RW					
Reset	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31	PBC3_EN	0: Disable 1: Enable
30	PBC3_LPF_EN	Enables PBC low-pass filter
29:22	PBC3_GAIN	PBC band gain
21:12	PBC3_RSLOPE_1	For (PBC_RADIUS_C < PBC_RADIUS_RANGE); 1024/PBC_RADIUS_C
11:6	PBC3_THETA_R	Theta range for PBC
5:0	PBC3_RADIUS_R	Radius range for PBC

1400605C MDP_PBC_07 MDP_PBC_07 E03C1010

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PBC3_THETA_C								PBC3_RADIUS_C							
Type	RW								RW							
Reset	1	1	1	0	0	0	0	0	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PBC3_TSLOPE										PBC3_LPF_GAIN					
Type	RW										RW					
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:24	PBC3_THETA_C	Theta center for PBC
23:16	PBC3_RADIUS_C	Radius center for PBC
15:6	PBC3_TSLOPE	1024/PBC_THETA_RANGE
5:0	PBC3_LPF_GAIN	PBC low-pass filter gain

14006060 MDP_PBC_08 MDP_PBC_08 08010C20

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PBC3_RSLOPE												PBC3_CONF_GAIN			
Type	RW												RW			
Reset	0	0	0	0	1	0	0	0	0	0			0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PBC3_EDGE_EN	PBC3_EDGE_THR								PBC3_EDGE_SLOPE					
Type		RW	RW								RW					
Reset		0	0	0	1	1	0	0			1	0	0	0	0	0

Bit(s)	Name	Description
31:22	PBC3_RSLOPE	1024/PBC_RADIUS_RANGE
19:16	PBC3_CONF_GAIN	PBC confidence gain
14	PBC3_EDGE_EN	Enables PBC edge preservation
13:8	PBC3_EDGE_THR	PBC edge threshold
5:0	PBC3_EDGE_SLOPE	PBC edge slope

14006064 MDP_HIST_CFG_00 MDP_HIST_CFG_00 FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HIST_WIN_X_END															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_WIN_X_START															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	HIST_WIN_X_END	**Histogram window** X end position
15:0	HIST_WIN_X_START	**Histogram window** X start position

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14006068 **MDP_HIST_CFG_01** **MDP_HIST_CFG_01** **FFFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HIST_WIN_Y_END															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_WIN_Y_START															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	HIST_WIN_Y_END	**Histogram window** Y end position
15:0	HIST_WIN_Y_START	**Histogram window** Y start position

1400606C **MDP_LUMA_HIST_00** **Result of Luma Histogram 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_00[26:16]										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_00[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_00	Luma histogram bin 0

14006070 **MDP_LUMA_HIST_01** **Result of Luma Histogram 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_01[26:16]										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_01[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_01	Luma histogram bin 1

14006074 **MDP_LUMA_** **Result of Luma Histogram 2** **00000000**

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HIST_02

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_02[26:16]										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_02[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_02	Luma histogram bin 2

14006078 MDP_LUMA_HIST_03 Result of Luma Histogram 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_03[26:16]										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_03[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_03	**Luma histogram bin 3**

1400607C MDP_LUMA_HIST_04 Result of Luma Histogram 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_04[26:16]										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_04[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_04	Luma histogram bin 4

14006080 MDP_LUMA_HIST_05 Result of Luma Histogram 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_05[26:16]										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_05[15:0]															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_05	Luma histogram bin 5

14006084 MDP_LUMA_HIST_06 Result of Luma Histogram 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_06[26:16]										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_06[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_06	Luma histogram bin 6

1400608C MDP_LUMA_HIST_07 Result of Luma Histogram 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_07[26:16]										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_07[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_07	Luma histogram bin 7

14006090 MDP_LUMA_HIST_08 Result of Luma Histogram 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_08[26:16]										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_08[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_08	Luma histogram bin 8

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14006094 **MDP_LUMA_HIST_09** **Result of Luma Histogram 9** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_09[26:16]										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_09[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_09	Luma histogram bin 9

14006098 **MDP_LUMA_HIST_10** **Result of Luma Histogram 10** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_10[26:16]										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_10[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_10	Luma histogram bin 10

1400609C **MDP_LUMA_HIST_11** **Result of Luma Histogram 11** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_11[26:16]										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_11[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_11	Luma histogram bin 11

140060A0 **MDP_LUMA_HIST_12** **Result of Luma Histogram 12** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_12[26:16]										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	LUMA_HIST_12[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_12	Luma histogram bin 12

140060A4 MDP_LUMA_HIST_13 Result of Luma Histogram 13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_13[26:16]										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_13[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_13	Luma histogram bin 13

140060A8 MDP_LUMA_HIST_14 Result of Luma Histogram 14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_14[26:16]										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_14[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_14	Luma histogram bin 14

140060AC MDP_LUMA_HIST_15 Result of Luma Histogram 15 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_15[26:16]										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_15[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_15	Luma histogram bin 15

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140060B0 MDP_LUMA_HIST_16 Result of Luma Histogram 16 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_16[26:16]										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_16[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_16	Luma histogram bin 16

140060B4 MDP_LUMA_SUM Result of Luma Sum 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LUMA_SUM[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_SUM[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LUMA_SUM	Luma sum of current frame

140060BC MDP_Y_FTN_1_0_MAIN 2nd Y Transfer Function 1, 0 00200000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								Y_FTN_1								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								Y_FTN_0								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	Y_FTN_1	Control point of luma curve on luma level 16 (8 bits)
8:0	Y_FTN_0	Control point of luma curve on luma level 0 (8 bits)

140060C0 MDP_Y_FTN_3_2_MAIN 2nd Y Transfer Function 3, 2 00600040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								Y_FTN_3								

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Type								RW								
Reset								0	0	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								Y_FTN_2								
Type								RW								
Reset								0	0	1	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	Y_FTN_3	Control point of luma curve on luma level 48 (8 bits)
8:0	Y_FTN_2	Control point of luma curve on luma level 32 (8 bits)

140060C4 MDP_Y_FTN_5_4_MAIN 2nd Y Transfer Function 5, 4 00A00080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								Y_FTN_5								
Type								RW								
Reset								0	1	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								Y_FTN_4								
Type								RW								
Reset								0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	Y_FTN_5	Control point of luma curve on luma level 80 (8 bits)
8:0	Y_FTN_4	Control point of luma curve on luma level 64 (8 bits)

140060C8 MDP_Y_FTN_7_6_MAIN 2nd Y Transfer Function 7, 6 00E000C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								Y_FTN_7								
Type								RW								
Reset								0	1	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								Y_FTN_6								
Type								RW								
Reset								0	1	1	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	Y_FTN_7	Control point of luma curve on luma level 112 (8 bits)
8:0	Y_FTN_6	Control point of luma curve on luma level 96 (8 bits)

140060CC MDP_Y_FTN_9_8_MAIN 2nd Y Transfer Function 9, 8 01200100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								Y_FTN_9								
Type								RW								
Reset								1	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								Y_FTN_8								

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Type								RW								
Reset								1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	Y_FTN_9	Control point of luma curve on luma level 144 (8 bits)
8:0	Y_FTN_8	Control point of luma curve on luma level 128 (8 bits)

140060D0 MDP_Y_FTN_11_10_MAIN 2nd Y Transfer Function 11, 10 01600140

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								Y_FTN_11								
Type								RW								
Reset								1	0	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								Y_FTN_10								
Type								RW								
Reset								1	0	1	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	Y_FTN_11	Control point of luma curve on luma level 176 (8 bits)
8:0	Y_FTN_10	Control point of luma curve on luma level 160 (8 bits)

140060D4 MDP_Y_FTN_13_12_MAIN 2nd Y Transfer Function 13, 12 01A00180

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								Y_FTN_13								
Type								RW								
Reset								1	1	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								Y_FTN_12								
Type								RW								
Reset								1	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	Y_FTN_13	Control point of luma curve on luma level 208 (8 bits)
8:0	Y_FTN_12	Control point of luma curve on luma level 192 (8 bits)

140060D8 MDP_Y_FTN_15_14_MAIN 2nd Y Transfer Function 15, 14 01E001C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								Y_FTN_15								
Type								RW								
Reset								1	1	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								Y_FTN_14								
Type								RW								
Reset								1	1	1	0	0	0	0	0	0

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Bit(s)	Name	Description
24:16	Y_FTN_15	Control point of luma curve on luma level 240 (8 bits)
8:0	Y_FTN_14	Control point of luma curve on luma level 224 (8 bits)

140060DC **MDP_Y_FTN_17_16_MAIN** **2nd Y Transfer Function 17, 16** **00000200**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							Y_FTN_16									
Type							RW									
Reset							1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	Y_FTN_16	Control point of luma curve on luma level 256 (8 bits)

140060E0 **MDP_C_BOOST_MAIN** **Chroma Boost** **FF402080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NEW_CBOOST_LMT_U								NEW_CBOOST_LMT_L							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			NEW_CBOOST_EN						CBOOST_GAIN							
Type			RW						RW							
Reset			1						1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	NEW_CBOOST_LMT_U	Chroma boost gain upper bound
23:16	NEW_CBOOST_LMT_L	Chroma boost gain lower bound
13	NEW_CBOOST_EN	0: Disable new chroma boost 1: Enable new chroma boost
7:0	CBOOST_GAIN	128 denotes 1.0

140060E4 **MDP_C_BOOST_MAIN_2** **Chroma Boost 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															CBOOST_YOFFSET_SEL	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name										CBOOST_YOFFSET						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
17:16	CBOOST_YOFFSET_SEL	Limit function of CBOOST_YOFFSET
6:0	CBOOST_YOFFSET	Y offset value of chroma boost

14006100 **MDP_TDSHP_CTRL** **MDP_TDSHP_CTRL** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															TDSHP_RESET	TDSHP_CTRL_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	TDSHP_RESET	0: De-assert software reset 1: Assert software reset
0	TDSHP_CTRL_EN	Enables TDSHP

14006104 **MDP_TDSHP_INTEN** **MDP_TDSHP_INTEN** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FRAME_UNDERRUN_EN	OF_END_INT_EN	IF_END_INT_EN
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FRAME_UNDERRUN_EN	Enables frame underrun interrupt
1	OF_END_INT_EN	Enables output frame end interrupt
0	IF_END_INT_EN	Enables input frame end interrupt

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14006108 **MDP_TDSHP_INTSTA** **MDP_TDSHP_INTSTA** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**FRAME_UNDERRUN**	**OF_END_INT**	**IF_END_INT**
Type														RO	RO	RO
Reset														0	0	0

Bit(s)	Name	Description
2	FRAME_UNDERRUN	1: Frame underrun (write 0 to clear)
1	OF_END_INT	1: Output frame end (write 0 to clear)
0	IF_END_INT	1: Input frame end (write 0 to clear)

1400610C **MDP_TDSHP_STATUS** **MDP_TDSHP_STATUS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**in_valid**	**in_ready**	**out_valid**	**out_ready**			**OF_UNFINISHED**	**IF_UNFINISHED**
Type									RO	RO	RO	RO			RO	RO
Reset									0	0	0	0			0	0

Bit(s)	Name	Description
7	in_valid	For debugging: in_valid from the previous engine
6	in_ready	For debugging: in_ready to the previous engine
5	out_valid	For debugging: out_valid to the next engine
4	out_ready	For debugging: out_ready from the next engine
1	OF_UNFINISHED	1: Output I/F under-run
0	IF_UNFINISHED	1: Input I/F under-run

14006110 **MDP_TDSHP_CFG** **MDP_TDSHP_CFG** **00000040**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**LUMA_HIST_E**	**DEMO_SWAP**	**DEMO_EN**		**FIFO_POSIT**	**FIFO_EN**	**RELAY_MODE**

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										N						
Type										RW	RW	RW		RW	RW	RW
Reset										1	0	0		0	0	0

Bit(s)	Name	Description
6	LUMA_HIST_EN	0: Disable luma histogram 1: Enable luma histogram
5	DEMO_SWAP	0: Sharpness inside window 1: Sharpness outside window
4	DEMO_EN	0: Disable 1: Enable
2	FIFO_POSIT	0: Before TDSHP (input prefetch) 1: Behind TDSHP (output buffer)
1	FIFO_EN	0: Disable 1: Enable
0	RELAY_MODE	0: Disable 1: Enable

14006114 MDP_TDSHP_INPUT_COUNT TDSHP Input I/F Debug Counter Register 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LINE_CNT												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PIX_CNT												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
28:16	LINE_CNT	Line counter value of input (input interface)
12:0	PIX_CNT	Pixel number counter value of input (input interface)

14006118 MDP_TDSHP_CHKSUM TDSHP Checksum Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKSUM_EN		CHKSUM_SEL						CHKSUM[23:16]							
Type	RW		RW						RU							
Reset	0		0	0					0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKSUM[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	CHKSUM_EN	0: Disable 1: Enable

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Bit(s)	Name	Description
29:28	CHKSUM_SEL	0: Input 1: Output 2: Output before crop
23:0	CHKSUM	Checksum result

1400611C MDP_TDSHP_OUTPUT_COUNT TDSHP Output I/F Debug Counter Register 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LINE_CNT												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PIX_CNT												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
28:16	LINE_CNT	Line counter value of output (output interface)
12:0	PIX_CNT	Pixel number counter value of output (output interface)

14006120 MDP_TDSHP_INPUT_SIZE MDP_TDSHP_INPUT_SIZE 01080190

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				IN_HSIZE												
Type				RW												
Reset				0	0	0	0	1	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				IN_VSIZE												
Type				RW												
Reset				0	0	0	0	1	1	0	0	1	0	0	0	0

Bit(s)	Name	Description
28:16	IN_HSIZE	Input active width
12:0	IN_VSIZE	Input active height

14006124 MDP_TDSHP_OUTPUT_OFFSET MDP_TDSHP_OUTPUT_OFFSET 00040000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									OUT_HOFFSET							
Type									RW							
Reset									0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									OUT_VOFFSET							
Type									RW							
Reset									0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
23:16	OUT_HOFFSET	Output active width offset
7:0	OUT_VOFFSET	Output active height offset

14006128 MDP_TDSHP_OUTPUT_SIZE MDP_TDSHP_OUTPUT_SIZE 01000190

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				OUT_HSIZE												
Type				RW												
Reset				0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OUT_VSIZE												
Type				RW												
Reset				0	0	0	0	1	1	0	0	1	0	0	0	0

Bit(s)	Name	Description
28:16	OUT_HSIZE	Output active width
12:0	OUT_VSIZE	Output active height

1400612C MDP_TDSHP_BLANK_WIDTH MDP_TDSHP_BLANK_WIDTH 00130202

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									HSYNC_WIDTH							
Type									RW							
Reset									0	0	0	1	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VSYNC_HSYNC_WIDTH								VSYNC_HACT_WIDTH							
Type	RW								RW							
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0

Bit(s)	Name	Description
23:16	HSYNC_WIDTH	Hsync width
15:8	VSYNC_HSYNC_WIDTH	Hsync width in vsync region
7:0	VSYNC_HACT_WIDTH	Hactive width in vsync region

14006130 MDP_TDSHP_DEMO_HMASK MDP_TDSHP_DEMO_HMASK 00010084

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DEMO_MASK_HSTART												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DEMO_MASK_HEND												
Type				RW												
Reset				0	0	0	0	0	1	0	0	0	0	1	0	0

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Bit(s)	Name	Description
28:16	DEMO_MASK_HSTART	Horizontal start position of demo window
12:0	DEMO_MASK_HEND	Horizontal end position of demo window

14006134 MDP_TDSHP_DEMO_VMASK MDP_TDSHP_DEMO_VMASK 00010190

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DEMO_MASK_VSTART												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				DEMO_MASK_VEND												
Type				RW												
Reset				0	0	0	0	1	1	0	0	1	0	0	0	0

Bit(s)	Name	Description
28:16	DEMO_MASK_VSTART	Vertical start position of demo window
12:0	DEMO_MASK_VEND	Vertical end position of demo window

14006200 MDP_LUMA_HIST_INIT_00 MDP_LUMA_HIST_INIT_00 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_00[26:16]										
Type						WO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	HIST_BIN_INIT_00[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_00	Initial value of luma histogram bin 0

14006204 MDP_LUMA_HIST_INIT_01 MDP_LUMA_HIST_INIT_01 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_01[26:16]										
Type						WO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	HIST_BIN_INIT_01[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
26:0	HIST_BIN_INIT_01	Initial value of luma histogram bin 1

14006208 **MDP_LUMA_HIST_INIT_02** **MDP_LUMA_HIST_INIT_02** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_02[26:16]										
Type						WO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_02[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_02	Initial value of luma histogram bin 2

1400620C **MDP_LUMA_HIST_INIT_03** **MDP_LUMA_HIST_INIT_03** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_03[26:16]										
Type						WO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_03[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_03	Initial value of luma histogram bin 3

14006210 **MDP_LUMA_HIST_INIT_04** **MDP_LUMA_HIST_INIT_04** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_04[26:16]										
Type						WO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_04[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_04	Initial value of luma histogram bin 4

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14006214 **MDP_LUMA_HIST_INIT_05** **MDP_LUMA_HIST_INIT_05** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_05[26:16]										
Type						WO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_05[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_05	Initial value of luma histogram bin 5

14006218 **MDP_LUMA_HIST_INIT_06** **MDP_LUMA_HIST_INIT_06** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_06[26:16]										
Type						WO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_06[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_06	Initial value of luma histogram bin 6

1400621C **MDP_LUMA_HIST_INIT_07** **MDP_LUMA_HIST_INIT_07** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_07[26:16]										
Type						WO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_07[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_07	Initial value of luma histogram bin 7

14006220 **MDP_LUMA_HIST_INIT_08** **MDP_LUMA_HIST_INIT_08** **00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_08[26:16]										
Type						WO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_08[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_08	Initial value of luma histogram bin 8

14006224 MDP_LUMA_HIST_INIT_09 MDP_LUMA_HIST_INIT_09 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_09[26:16]										
Type						WO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_09[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_09	Initial value of luma histogram bin 9

14006228 MDP_LUMA_HIST_INIT_10 MDP_LUMA_HIST_INIT_10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_10[26:16]										
Type						WO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_10[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_10	Initial value of luma histogram bin 10

1400622C MDP_LUMA_HIST_INIT_11 MDP_LUMA_HIST_INIT_11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_11[26:16]										
Type						WO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_11[15:0]															
Type	WO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_11	Initial value of luma histogram bin 11

14006230 **MDP_LUMA_HIST_INIT_12** **MDP_LUMA_HIST_INIT_12** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_12[26:16]										
Type						WO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_12[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_12	Initial value of luma histogram bin 12

14006234 **MDP_LUMA_HIST_INIT_13** **MDP_LUMA_HIST_INIT_13** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_13[26:16]										
Type						WO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_13[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_13	Initial value of luma histogram bin 13

14006238 **MDP_LUMA_HIST_INIT_14** **MDP_LUMA_HIST_INIT_14** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_14[26:16]										
Type						WO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_14[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_14	Initial value of luma histogram bin 14

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1400623C **MDP_LUMA_HIST_INIT_15** **MDP_LUMA_HIST_INIT_15** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_15[26:16]										
Type						WO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_15[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_15	Initial value of luma histogram bin 15

14006240 **MDP_LUMA_HIST_INIT_16** **MDP_LUMA_HIST_INIT_16** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_16[26:16]										
Type						WO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_16[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_16	Initial value of luma histogram bin 16

14006244 **MDP_LUMA_SUM_INIT** **MDP_LUMA_SUM_INIT** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HIST_SUM_INIT[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_SUM_INIT[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	HIST_SUM_INIT	Initial value of luma sum

6.10.5 Programming Guide

6.10.5.1 Sharpness Adjustment

There are total three possible usage scenarios for different situations.

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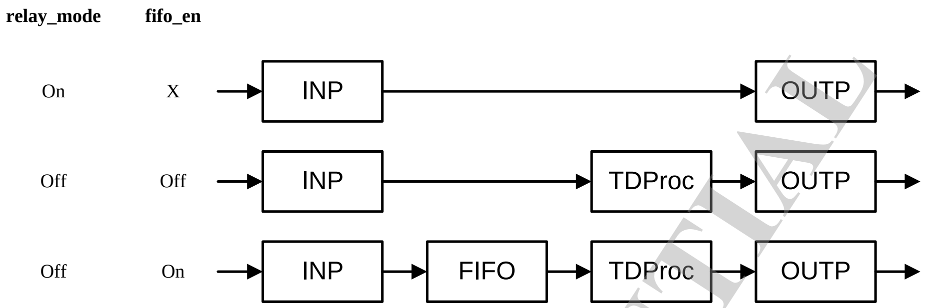

Figure 6-33. Usage scenarios

The sharpness function is designed to provide different sharpness levels. The sharpness level can be programmed by the gain curve control in the 2-dimensional sharpness unit. Higher sharpness level enhances more details of the image and sharpens the edge. However, sharpness setting that is too strong will induce some artificial side effects. Therefore, balance setting with enough sharpness level is preferred.

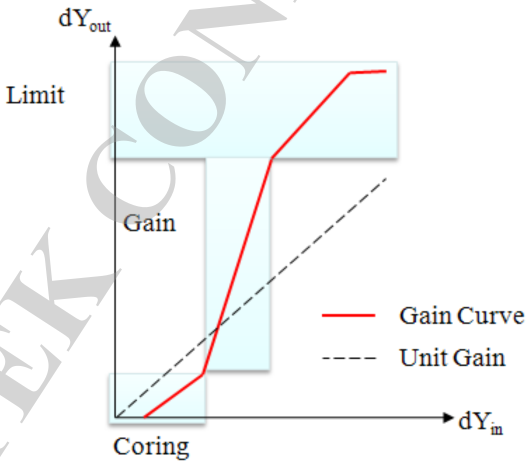

Figure 6-34. Gain curve control of sharpness

6.10.5.2 Luma Adjustment

The color processor applies a luma mapping curve to the input luma (see Figure 6-35). The full luma range is equally divided into 16 segments, and registers Y_FTN_*are responsible for the adjustments.

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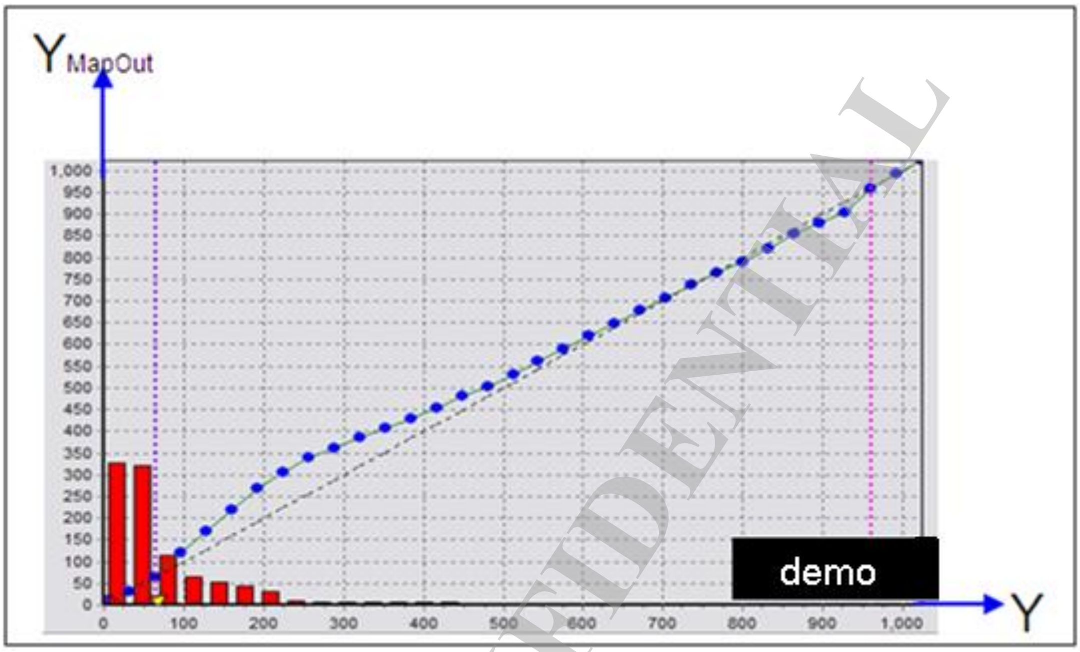

Figure 6-35. Luma mapping curve example

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6.11 DISP_OVL

6.11.1 Introduction

The display OVERLAY can do alpha blending up to 4 layers. The 4 layer sources can be from MEMORY/constant layer color. Four RDMA is included in overlay and 4 sets of color transform are also included.

6.11.2 Features

The following table describes the features of DISP_OVL.

Item	Main function	Description
1	4K2K resolution	Supports 4096x2160
2	4 layer overlay	Supports 4 layers of blending (w/o multiplier)
3	Color format uniform	Supports color format uniform and swap control (RGB565/RGB888/RGBA8888/ARGB8888/YUYV/YUV2)
4	3D display	Interleave left and right image for 3D display (landscape and portrait mode)
5	Color conversion	Wide-gamma : sRGB/GPU/Adobe mode
6	Layer constant color	Constant color input for each layer source
7	Alpha blending	Supports pixel alpha blending + SurfaceFlinger alpha blending (G2D)
8	Flexible ROI system	Supports individual color depth, window size, vertical and horizontal offset
9	Flip function	Vertical/Horizontal/180 degree flip function

6.11.3 Block Diagram

There are four OVL_RDMA in DISP_OVL, and each OVL_RDMA contains a 128x128 single port SRAM (ping-pung buffer).

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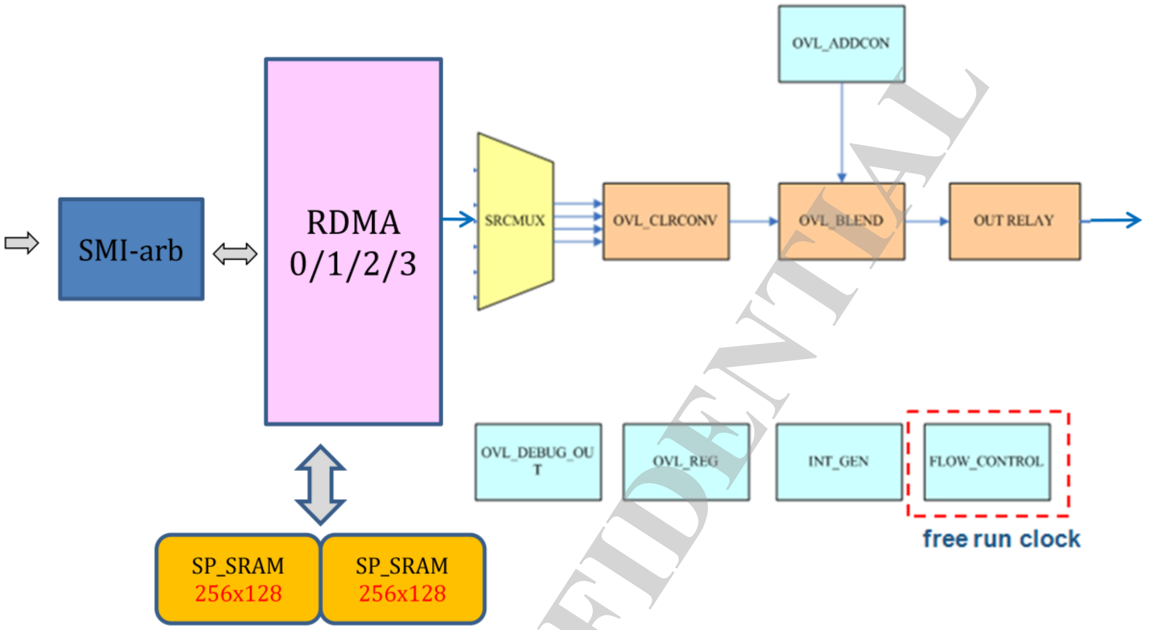

Figure 6-36. Block diagram of DISP_OVL

6.11.4 Register Definition

Module name: DISP_OVL Base address: (+0h)

Address	Name	Width	Register Function
00000000	OVL_STA	32	**Overlay Status Monitor** OVL status
00000004	OVL_INTEN	32	**Overlay Interrupt Enable** Enables OVL interrupt
00000008	OVL_INTSTA	32	**Overlay Interrupt Status** OVL interrupt status
0000000C	OVL_EN	32	**Overlay Enable** Enables overlay engine
00000010	OVL_TRIG	32	**Overlay Trigger** SW trigger to enable overlay engine
00000014	OVL_RST	32	**Overlay Reset** Overlay SW reset
00000020	OVL_ROI_SIZE	32	**Overlay ROI Size** Overlay region of interest width and height
00000024	OVL_DATAPATH_CON	32	**Overlay Datapath Control** Controls overlay datapath
00000028	OVL_ROI_BGCLR	32	Overlay Background Color
0000002C	OVL_SRC_CON	32	**Overlay Source Control** Controls overlay layer enable
00000030	OVL_L0_CON	32	Overlay Layer 0 Control
00000034	OVL_L0_SRCKEY	32	Overlay Layer 0 Source Key
00000038	OVL_L0_SRC_SIZE	32	Overlay Layer 0 Source Size
0000003C	OVL_L0_OFFSET	32	Overlay Layer 0 Offset

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Address	Name	Width	Register Function
00000044	OVL_L0_PITCH	32	**Overlay Layer 0 Pitch** Overlay Layer 0 SRC and PIC pitch
00000048	OVL_L0_TILE	32	Overlay Layer 0 Tile Control
00000050	OVL_L1_CON	32	Overlay Layer 1 Control
00000054	OVL_L1_SRCKEY	32	Overlay Layer 1 Source Key
00000058	OVL_L1_SRC_SIZE	32	Overlay Layer 1 Source Size
0000005C	OVL_L1_OFFSET	32	Overlay Layer 1 Offset
00000064	OVL_L1_PITCH	32	**Overlay Layer1 Pitch** Overlay Layer 1 SRC and PIC pitch
00000068	OVL_L1_TILE	32	**Overlay Layer 1 Tile Control** Overlay Layer 1 tile control
00000070	OVL_L2_CON	32	Overlay Layer 2 Control
00000074	OVL_L2_SRCKEY	32	Overlay Layer 2 Source Key
00000078	OVL_L2_SRC_SIZE	32	Overlay Layer 2 Source Size
0000007C	OVL_L2_OFFSET	32	Overlay Layer 2 Offset
00000084	OVL_L2_PITCH	32	**Overlay Layer 2 Pitch** Overlay Layer 2 SRC and PIC pitch
00000088	OVL_L2_TILE	32	Overlay Layer 2 Tile Control
00000090	OVL_L3_CON	32	Overlay Layer 3 Control
00000094	OVL_L3_SRCKEY	32	Overlay Layer 3 Source Key
00000098	OVL_L3_SRC_SIZE	32	Overlay Layer 3 Source Size
0000009C	OVL_L3_OFFSET	32	Overlay Layer 3 Offset
000000A4	OVL_L3_PITCH	32	**Overlay Layer 3 Pitch** Overlay Layer 3 SRC and PIC pitch
000000A8	OVL_L3_TILE	32	Overlay Layer 3 Tile Control
000000C0	OVL_RDMA0_CTRL	32	Overlay RDMA0 Control
000000C8	OVL_RDMA0_MEM_GMC_SETTING1	32	Overlay RDMA0 Memory GMC Setting
000000CC	OVL_RDMA0_MEM_SLOW_CON	32	Overlay RDMA0 Memory Slow Control
000000D0	OVL_RDMA0_FIFO_CTRL	32	Overlay RDMA0 FIFO Control
000000E0	OVL_RDMA1_CTRL	32	Overlay RDMA1 Control
000000E8	OVL_RDMA1_MEM_GMC_SETTING1	32	Overlay RDMA1 Memory GMC Setting
000000EC	OVL_RDMA1_MEM_SLOW_CON	32	Overlay RDMA1 Memory Slow Control
000000F0	OVL_RDMA1_FIFO_CTRL	32	Overlay RDMA1 FIFO Control
00000100	OVL_RDMA2_CTRL	32	Overlay RDMA2 Control
00000108	OVL_RDMA2_MEM_GMC_SETTING1	32	Overlay RDMA2 Memory GMC Setting
0000010C	OVL_RDMA2_MEM_SLOW_CON	32	Overlay RDMA2 Memory Slow Control

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Address	Name	Width	Register Function
00000110	OVL_RDMA2_FIFO_CTRL	32	Overlay RDMA2 FIFO Control
00000120	OVL_RDMA3_CTRL	32	Overlay RDMA3 Control
00000128	OVL_RDMA3_MEM_GMC_SETTING1	32	Overlay RDMA3 Memory GMC Setting
0000012C	OVL_RDMA3_MEM_SLOW_CON	32	Overlay RDMA3 Memory Slow Control
00000130	OVL_RDMA3_FIFO_CTRL	32	Overlay RDMA3 FIFO Control
00000134	OVL_L0_Y2R_PARA_R0	32	Overlay L0 Y2R Conversion Parameter R0
00000138	OVL_L0_Y2R_PARA_R1	32	Overlay L0 Y2R Conversion Parameter R1
0000013C	OVL_L0_Y2R_PARA_G0	32	Overlay L0 Y2R Conversion Parameter G0
00000140	OVL_L0_Y2R_PARA_G1	32	Overlay L0 Y2R Conversion Parameter G1
00000144	OVL_L0_Y2R_PARA_B0	32	Overlay L0 Y2R Conversion Parameter B0
00000148	OVL_L0_Y2R_PARA_B1	32	Overlay L0 Y2R Conversion Parameter B1
0000014C	OVL_L0_Y2R_PARA_YUV_A_0	32	Overlay L0 Y2R Conversion Parameter Extended Add on YUV 0
00000150	OVL_L0_Y2R_PARA_YUV_A_1	32	Overlay L0 Y2R Conversion Parameter Extended Add on YUV 1
00000154	OVL_L0_Y2R_PARA_RGB_A_0	32	Overlay L0 Y2R Conversion Parameter Extended Add on RGB 0
00000158	OVL_L0_Y2R_PARA_RGB_A_1	32	Overlay L0 Y2R Conversion Parameter Extended Add on RGB 1
0000015C	OVL_L1_Y2R_PARA_R0	32	Overlay L1 Y2R Conversion Parameter R0
00000160	OVL_L1_Y2R_PARA_R1	32	Overlay L1 Y2R Conversion Parameter R1
00000164	OVL_L1_Y2R_PARA_G0	32	Overlay L1 Y2R Conversion Parameter G0
00000168	OVL_L1_Y2R_PARA_G1	32	Overlay L1 Y2R Conversion Parameter G1
0000016C	OVL_L1_Y2R_PARA_B0	32	Overlay L1 Y2R Conversion Parameter B0
00000170	OVL_L1_Y2R_PARA_B1	32	Overlay L1 Y2R Conversion Parameter B1
00000174	OVL_L1_Y2R_PARA_YUV_A_0	32	Overlay L1 Y2R Conversion Parameter Extended Add on YUV 0
00000178	OVL_L1_Y2R_PARA_YUV_A_1	32	Overlay L1 Y2R Conversion Parameter Extended Add on YUV 1
0000017C	OVL_L1_Y2R_PARA_RGB_A_0	32	Overlay L1 Y2R Conversion Parameter Extended Add on RGB 0
00000180	OVL_L1_Y2R_PARA_RGB_A_1	32	Overlay L1 Y2R Conversion Parameter Extended Add on RGB 1
00000184	OVL_L2_Y2R_PARA_R0	32	Overlay L2 Y2R Conversion Parameter R0
00000188	OVL_L2_Y2R_PARA_R1	32	Overlay L2 Y2R Conversion Parameter R1

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Address	Name	Width	Register Function
0000018C	OVL_L2_Y2R_PARA_G0	32	Overlay L2 Y2R Conversion Parameter G0
00000190	OVL_L2_Y2R_PARA_G1	32	Overlay L2 Y2R Conversion Parameter G1
00000194	OVL_L2_Y2R_PARA_B0	32	Overlay L2 Y2R Conversion Parameter B0
00000198	OVL_L2_Y2R_PARA_B1	32	Overlay L2 Y2R Conversion Parameter B1
0000019C	OVL_L2_Y2R_PARA_YUV_A_0	32	Overlay L2 Y2R Conversion Parameter Extended Add on YUV 0
000001A0	OVL_L2_Y2R_PARA_YUV_A_1	32	Overlay L2 Y2R Conversion Parameter Extended Add on YUV 1
000001A4	OVL_L2_Y2R_PARA_RGB_A_0	32	Overlay L2 Y2R Conversion Parameter Extended Add on RGB 0
000001A8	OVL_L2_Y2R_PARA_RGB_A_1	32	Overlay L2 Y2R Conversion Parameter Extended Add on RGB 1
000001AC	OVL_L3_Y2R_PARA_R0	32	Overlay L3 Y2R Conversion Parameter R0
000001B0	OVL_L3_Y2R_PARA_R1	32	Overlay L3 Y2R Conversion Parameter R1
000001B4	OVL_L3_Y2R_PARA_G0	32	Overlay L3 Y2R Conversion Parameter G0
000001B8	OVL_L3_Y2R_PARA_G1	32	Overlay L3 Y2R Conversion Parameter G1
000001BC	OVL_L3_Y2R_PARA_B0	32	Overlay L3 Y2R Conversion Parameter B0
000001C0	OVL_L3_Y2R_PARA_B1	32	Overlay L3 Y2R Conversion Parameter B1
000001C4	OVL_L3_Y2R_PARA_YUV_A_0	32	Overlay L3 Y2R Conversion Parameter Extended Add on YUV 0
000001C8	OVL_L3_Y2R_PARA_YUV_A_1	32	Overlay L3 Y2R Conversion Parameter Extended Add on YUV 1
000001CC	OVL_L3_Y2R_PARA_RGB_A_0	32	Overlay L3 Y2R Conversion Parameter Extended Add on RGB 0
000001D0	OVL_L3_Y2R_PARA_RGB_A_1	32	Overlay L3 Y2R Conversion Parameter Extended Add on RGB 1
000001D4	OVL_DEBUG_MON_SEL	32	Overlay Debug Monitor Select
000001E0	OVL_RDMA0_MEM_GMC_SETTING2	32	Overlay RDMA0 Memory GMC Setting
000001E4	OVL_RDMA1_MEM_GMC_SETTING2	32	Overlay RDMA1 Memory GMC Setting
000001E8	OVL_RDMA2_MEM_GMC_SETTING2	32	Overlay RDMA2 Memory GMC Setting
000001EC	OVL_RDMA3_MEM_GMC_SETTING2	32	Overlay RDMA3 Memory GMC Setting
00000200	OVL_DUMMY_REG	32	Overlay Dummy Register
00000230	OVL_SMI_DBG	32	Overlay SMI Arbiter Debug Monitor
00000234	OVL_GREQ_LAYER_CNT	32	Overlay Layer Greq Counter
00000240	OVL_FLOW_CTR	32	Overlay Flow Control Debug Monitor

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Address	Name	Width	Register Function
	L_DBG		
00000244	OVL_ADDCON_DBG	32	Overlay Address Control Debug
0000024C	OVL_RDMA0_DBG	32	Overlay RDMA0 Debug Monitor
00000250	OVL_RDMA1_DBG	32	Overlay RDMA1 Debug Monitor
00000254	OVL_RDMA2_DBG	32	Overlay RDMA2 Debug Monitor
00000258	OVL_RDMA3_DBG	32	Overlay RDMA3 Debug Monitor
0000025C	OVL_L0_CLR	32	Overlay Layer 0 Constant Color
00000260	OVL_L1_CLR	32	Overlay Layer 1 Constant Color
00000264	OVL_L2_CLR	32	Overlay Layer 2 Constant Color
00000268	OVL_L3_CLR	32	Overlay Layer 3 Constant Color
00000F40	OVL_L0_ADDR	32	Overlay Layer 0 Memory Address
00000F60	OVL_L1_ADDR	32	Overlay Layer 1 Memory Address
00000F80	OVL_L2_ADDR	32	Overlay Layer 2 Memory Address
00000FA0	OVL_L3_ADDR	32	Overlay Layer 3 Memory Address
00000FC0	OVL_SECURE	32	Overlay Layer Secure Bit

00000000 OVL_STA Overlay Status Monitor 0000001E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RDMA3_IDLE	RDMA2_IDLE	RDMA1_IDLE	RDMA0_IDLE	OVL_RUN
Type												RU	RU	RU	RU	RU
Reset												1	1	1	1	0

Bit(s)	Mnemonic	Name	Description
4		RDMA3_IDLE	**Status of overlay RDMA3** 0: RDMA is running. 1: All overlay RDMA are idle.
3		RDMA2_IDLE	**Status of overlay RDMA2** 0: RDMA is running. 1: All overlay RDMA are idle.
2		RDMA1_IDLE	**Status of overlay RDMA1** 0: RDMA is running. 1: All overlay RDMA are idle.
1		RDMA0_IDLE	**Status of overlay RDMA0** 0: RDMA is running. 1: All overlay RDMA are idle.
0		OVL_RUN	**Status of overlay engine** 0: Overlay is idle. 1: Overlay is running.

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0000000 4 **OVL_INTEN** **Overlay Interrupt Enable** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RDMA3_SMI_UNDERFLOW_INTEN	RDMA2_SMI_UNDERFLOW_INTEN	RDMA1_SMI_UNDERFLOW_INTEN	RDMA0_SMI_UNDERFLOW_INTEN	RDMA3_EOF_ABNORMAL_INTEN	RDMA2_EOF_ABNORMAL_INTEN	RDMA1_EOF_ABNORMAL_INTEN	RDMA0_EOF_ABNORMAL_INTEN	OVL_FME_HWRST_DONE_INTEN	OVL_FME_SWRST_DONE_INTEN	OVL_FME_UND_INTEN	OVL_FME_CPL_INTEN	OVL_REG_CMT_INTEN
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12		RDMA3_SMI_UNDERFLOW_INTEN	**Control RDMA3 SMI underflow interrupt** 0: Disable RDMA3 SMI data underflow interrupt 1: Enable RDMA3 SMI data underflow interrupt
11		RDMA2_SMI_UNDERFLOW_INTEN	**Control RDMA2 SMI underflow interrupt** 0: Disable RDMA2 SMI data underflow interrupt 1: Enable RDMA2 SMI data underflow interrupt
10		RDMA1_SMI_UNDERFLOW_INTEN	**Control RDMA1 SMI underflow interrupt** 0: Disable RDMA1 SMI data underflow interrupt 1: Enable RDMA1 SMI data underflow interrupt
9		RDMA0_SMI_UNDERFLOW_INTEN	**Control RDMA0 SMI underflow interrupt** 0: Disable RDMA0 SMI data underflow interrupt 1: Enable RDMA0 SMI data underflow interrupt
8		RDMA3_EOF_ABNORMAL_INTEN	**Control RDMA3 EOF abnormal interrupt** 0: Disable RDMA3 EOF abnormal interrupt 1: Enable RDMA3 EOF abnormal interrupt
7		RDMA2_EOF_ABNORMAL_INTEN	**Control RDMA2 EOF abnormal interrupt** 0: Disable RDMA2 EOF abnormal interrupt 1: Enable RDMA2 EOF abnormal interrupt
6		RDMA1_EOF_ABNORMAL_INTEN	**Control RDMA1 EOF abnormal interrupt** 0: Disable RDMA1 EOF abnormal interrupt 1: Enable RDMA1 EOF abnormal interrupt
5		RDMA0_EOF_ABNORMAL_INTEN	**Control RDMA0 EOF abnormal interrupt** 0: Disable RDMA0 EOF abnormal interrupt 1: Enable RDMA0 EOF abnormal interrupt
4		OVL_FME_HWRST_DONE_INTEN	**Control frame HW reset done interrupt** 0: Disable frame HW reset done interrupt 1: Enable frame HW reset done interrupt
3		OVL_FME_SWRST_DONE_INTEN	**Control frame SW reset done interrupt** 0: Disable frame SW reset done interrupt 1: Enable frame SW reset done interrupt
2		OVL_FME_UND_INTEN	**Control frame underflow interrupt** 0: Disable frame underflow interrupt 1: Enable frame underflow interrupt
1		OVL_FME_CPL_	**Control frame completed interrupt**

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Bit(s)	Mnemonic	Name	Description
		INTEN	0: Disable frame complete interrupt 1: Enable frame complete interrupt
0		OVL_REG_CMT_INTEN	**Control register setting completed interrupt** 0: Disable register commit interrupt 1: Enable register commit interrupt

00000008	OVL_INTSTA	Overlay Interrupt Status	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				RDMA3_SMI_UNDERFLOW_INTSTA	RDMA2_SMI_UNDERFLOW_INTSTA	RDMA1_SMI_UNDERFLOW_INTSTA	RDMA0_SMI_UNDERFLOW_INTSTA	RDMA3_EOF_ABNORMAL_INTSTA	RDMA2_EOF_ABNORMAL_INTSTA	RDMA1_EOF_ABNORMAL_INTSTA	RDMA0_EOF_ABNORMAL_INTSTA	OVL_FME_HWRST_DONE_INTSTA	OVL_FME_SWRST_DONE_INTSTA	OVL_FME_UND_INTSTA	OVL_FME_CPL_INTSTA	OVL_REG_CMT_INTSTA
Type				A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12		RDMA3_SMI_UNDERFLOW_INTSTA	**RDMA3 SMI status** Controls interrupt write clear. Write 0 to clear it; writing 1 is useless. 0: RDMA3 SMI data are not underflow. 1: RDMA3 SMI data are underflow.
11		RDMA2_SMI_UNDERFLOW_INTSTA	**RDMA2 SMI status** Controls interrupt write clear. Write 0 to clear it; writing 1 is useless. 0: RDMA2 SMI data are not underflow. 1: RDMA2 SMI data are underflow.
10		RDMA1_SMI_UNDERFLOW_INTSTA	**RDMA1 SMI status** Controls interrupt write clear. Write 0 to clear it; writing 1 is useless. 0: RDMA1 SMI data are not underflow. 1: RDMA1 SMI data are underflow.
9		RDMA0_SMI_UNDERFLOW_INTSTA	**RDMA0 SMI status** Controls interrupt write clear. Write 0 to clear it; writing 1 is useless. 0: RDMA0 SMI data are not underflow. 1: RDMA0 SMI data are underflow.
8		RDMA3_EOF_ABNORMAL_INTSTA	**RDMA3 status** Controls interrupt write clear. Write 0 to clear it; writing 1 is useless. 0: RDMA3 completed normally 1: RDMA3 not completed till EOF
7		RDMA2_EOF_ABNORMAL_INTSTA	**RDMA2 status** Controls interrupt write clear. Write 0 to clear it; writing 1 is useless. 0: RDMA2 completed normally

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Bit(s)	Mnemonic	Name	Description
			1: RDMA2 not completed till EOF
6		RDMA1_EOF_ABNORMAL_INTSTA	**RDMA1 status** Controls interrupt write clear. Write 0 to clear it; writing 1 is useless. 0: RDMA1 completed normally 1: RDMA1 not completed till EOF
5		RDMA0_EOF_ABNORMAL_INTSTA	**RDMA0 status** Controls interrupt write clear. Write 0 to clear it; writing 1 is useless. 0: RDMA0 completed normally 1: RDMA0 not completed till EOF
4		OVL_FME_HWRST_DONE_INTSTA	**Overlay HW reset done status** Controls interrupt write clear. Write 0 to clear it; writing 1 is useless. 0: No HW reset or HW reset is not done. 1: HW reset is done.
3		OVL_FME_SWRST_DONE_INTSTA	**Overlay SW reset done status** Controls interrupt write clear. Write 0 to clear it; writing 1 is useless. 0: No SW reset or SW reset is not done. 1: SW reset is done.
2		OVL_FME_UND_INTSTA	**Overlay frame underflow status** Controls interrupt write clear. Write 0 to clear it; writing 1 is useless. 0: Frame completed w/o underflow 1: Frame not completed w/ underflow
1		OVL_FME_CPL_INTSTA	**Overlay frame complete status** Controls interrupt write clear. Write 0 to clear it; writing 1 is useless. 0: Frame not completed 1: Frame completed
0		OVL_REG_CMT_INTSTA	**Overlay register commit status** Controls interrupt write clear. Write 0 to clear it; writing 1 is useless. 0: Register is not set from shadow register to working register. 1: Register is set to working register done.

0000000C <u>**OVL_EN**</u> **Overlay Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																OVEN
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**OVEN**	OVL_EN	**Enables overlay engine** 0: Disable overlay 1: Enable overlay

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00000010 **OVL_TRIG** **Overlay Trigger** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**OVTR**
Type																WO
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**OVTR**	OVL_SW_TRIG	**SW trigger to enable overlay engine** 0: When using HW trigger (SOF), this bit should be 0. 1: SW control to enable overlay engine

00000014 **OVL_RST** **Overlay Reset** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**OVL_SMI_FORCE_RST**															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**OVL_RST**
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
31		OVL_SMI_FORCE_RST	**OVL force RESET, when SMI BUSY hang issue** 0: Disable 1: Force SMI busy reset when FSM = H_W_RST/S_W_RST
0		OVL_RST	**Controls overlay SW reset for engine (high active)** 1: Reset engine

00000020 **OVL_ROI_SIZE** **Overlay ROI Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**ROIH**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**ROIW**												

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Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**ROIH**	ROI_H	**Overlay ROI width** Range: 1~8191. For 3D display, this value should be 2~8191.
12:0	**ROIW**	ROI_W	**Overlay ROI width** Range: 1~8191. For 3D display, this value should be 2~8191.

00000024 OVL_DATAPATH_CON Overlay Datapath Control 60000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LAYER_GREQ_NUM								RDMA3SEL	RDMA2SEL	RDMA1SEL	RDMA0SEL			PQSEL	
Type	RW								Other	Other	Other	Other			Other	
Reset	0	1	1						0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OVL_GAMMA_OUT	ADOBE_LAYER		ADOBE	L3_GPU	L2_GPU	L1_GPU	L0_GPU						BGCLR_IN_SEL	OVL_RANDOM_BGCLR_EN	LAYER_SMI_ID_EN
Type	RW	RW		RW	RW	RW	RW	RW						RW	RW	RW
Reset	0	0	0	0	0	0	0	0						0	0	0

Bit(s)	Mnemonic	Name	Description
31:29	**LAYER_GREQ_NUM**	LAYER_GREQ_NUM	**OVL each layer multi-greq number** Max. 7.
23	**RDMA3SEL**	RDMA3_OUT_SEL	**Selects output path of RDMA3** 0: OVL Layer 3 1: PQ direct link output
22	**RDMA2SEL**	RDMA2_OUT_SEL	**Selects output path of RDMA2** 0: OVL Layer 2 1: PQ direct link output
21	**RDMA1SEL**	RDMA1_OUT_SEL	**Selects output path of RDMA1** 0: OVL Layer 1 1: PQ direct link output
20	**RDMA0SEL**	RDMA0_OUT_SEL	**Selects output path of RDMA0** 0: OVL Layer 0 1: PQ direct link output
17:16	**PQSEL**	PQ_OUT_SEL	**Selects PQ direct link output data** 00: RDMA0 01: RDMA1 10: RDMA2 11: RDMA3
15	**OVL_GAMMA_OUT**	OVL_GAMMA_OUT	**Wide-gamut OVL output GAMMA table path** Shares GAMMA-table with layer adobe_mode. 0: Disable OVL output GAMMA table 1: Enable OVL output GAMMA table

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Bit(s)	Mnemonic	Name	Description
14:13	**ADOBE_LAYER**	ADOBE_LAYER	**Selects wide-gamut layer adobe** 0: Select Layer 0 adobe_path 1: Select Layer 1 adobe_path 2: Select Layer 2 adobe_path 3: Select Layer 3 adobe_path
12	**ADOBE**	ADOBE_MODE	**Wide-gamut layer adobe mode** Shares GAMMA-table with ovl_gamma_out mode. 0: Disable layer Adobe path 1: Enable layer Adobe path
11	**L3_GPU**	L3_GPU_MODE	**Wide-gamut Layer 3 GPU path mode** 0: Disable Layer 3 GPU path 1: Enable Layer 3 GPU path
10	**L2_GPU**	L2_GPU_MODE	**Wide-gamut Layer 2 GPU path mode** 0: Disable Layer 2 GPU path 1: Enable Layer 2 GPU path
9	**L1_GPU**	L1_GPU_MODE	**Wide-gamut Layer 1 GPU path mode** 0: Disable Layer 1 GPU path 1: Enable Layer 1 GPU path
8	**L0_GPU**	L0_GPU_MODE	**Wide-gamut Layer 0 GPU path mode** 0: Disable Layer 0 GPU path 1: Enable Layer 0 GPU path
2		BGCLR_IN_SEL	**OVL BGCLR direct link path** 0: Disable OVL BGCLR direct link input 1: Enable OVL BGCLR direct link input
1		OVL_RANDOM_BGCLR_EN	**When OVL_RANDOM_BGCLR_EN=1, layer_en[i] should be set to 0 to allow the background color pass through the blend engine.** 0: Disable random background color pattern 1: Enable random background color pattern
0	**LAYER_SMI_ID_EN**	LAYER_SMI_ID_EN	**Supports OVL SMI ID function** 0: Disable SMI ID 1: Enable SMI ID

00000028 **OVL_ROI_BGCLR** **Overlay Background Color** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BGDA								BGDR							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BGDG								BGDB							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24	**BGDA**	ALPHA	Alpha component of ROI window background color
23:16	**BGDR**	RED	Red component of ROI window background color
15:8	**BGDG**	GREEN	Green component of ROI window background color
7:0	**BGDB**	BLUE	Blue component of ROI window background color

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0000002C **OVL_SRC_CON** **Overlay Source Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**L3EN**	**L2EN**	**L1EN**	**L0EN**
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3	**L3EN**	L3_EN	**Set up this bit to enable overlay Layer 3.** 0: Disable Layer 3 1: Enable Layer 3
2	**L2EN**	L2_EN	**Set up this bit to enable overlay Layer 2.** 0: Disable Layer 2 1: Enable Layer 2
1	**L1EN**	L1_EN	**Set up this bit to enable overlay Layer 1.** 0: Disable Layer 1 1: Enable Layer 1
0	**L0EN**	L0_EN	**Set up this bit to enable overlay Layer 0.** 0: Disable Layer 0 1: Enable Layer 0

00000030 **OVL_L0_CON** **Overlay Layer 0 Control** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DKEN**	**SKEN**	**LSRC**				**RGSW**	**BTSW**		**R_FIRST**	**LANDSCAPE**	**EN_3D**	**MTX**			
Type	RW	RW	RW				RW	RW		RW	RW	RW	RW			
Reset	0	0	0	0			0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CFMT**				**MTXEN**	**HFE**	**VFE**	**AEN**	**APHA**							
Type	RW				Other	RW	RW	RW	RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**DKEN**	DSTKEY_EN	**Enables destination color key** SRCKEY_EN and DSTKEY_EN are exclusive settings which cannot be enabled at the same time. 0: Disable destination color key 1: Enable destination color key
30	**SKEN**	SRCKEY_EN	**Enables source color key** SRCKEY_EN and DSTKEY_EN are exclusive settings which cannot be enabled at the same time. 0: Disable source color key 1: Enable source color key
29:28	**LSRC**	LAYER_SRC	**Selects layer pixel from memory/constant color/SCL/PQ** 00: Layer pixel from memory RDMA0

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Bit(s)	Mnemonic	Name	Description
			01: Layer pixel from constant color 10: Layer pixel from UFOd
25	**RGSW**	RGB_SWAP	**Not used**
24	**BTSW**	BYTE_SWAP	**Swaps unified color format** 0: RGB565, BGR888, BGRA8888, ABGR8888, UYVY, YUYV 1: BGR565, RGB888, RGBA8888, ARGB8888, VYUY, YVYU
22		R_FIRST	**Right eye image first when in 3D mode** 0: Show left eye image first in 3D mode 1: Show right eye image first in 3D mode
21		LANDSCAPE	**Enables 3D landscape mode** 0: 3D portrait mode 1: 3D landscape mode
20		EN_3D	**Enables 3D mode** 0: 2D mode 1: 3D mode
19:16	**MTX**	INT_MTX_SEL	**Selects color matrix table** 0100: MTX_JPEG_TO_RGB 0110: MTX_BT601_TO_RGB 0111: MTX_BT709_TO_RGB Others: HW default (JPEG_TO_RGB)
15:12	**CFMT**	CLRFMT	**//--OLD definition** For reference only. 0000: RGB888 0001: RGB565 0010: ARGB8888 0011: PARGB8888 0100: xARGB8888 1000: YUYV 1001: UYVY 1010: YVYU 1011: VYUY 1111: YUV444 Others: Reserved color format 0000: RGB565 0001: RGB888 0010: RGBA8888/BGRA8888 0011: ARGB8888/ABGR8888 0100: UVVY, VYUY 0101: YUYV, YVYU
11	**MTXEN**	EXT_MTX_EN	**Enables external programmable coeff** 0: Matrix coeff 1: Programmable coeff
10	**HFE**	HORIZONTAL_FLIP_EN	**Enables horizontal flip function** 0: Disable horizontal flip function 1: Enable horizontal flip function
9	**VFE**	VERTICAL_FLIP_EN	**Enables vertical flip function** 0: Disable vertical flip function 1: Enable vertical flip function
8	**AEN**	ALPHA_EN	**Enables alpha blending** 0: Disable alpha blending 1: Enable alpha blending
7:0	**APHA**	ALPHA	**Constant alpha value**

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0000003 4 OVL_L0_SRCKEY Overlay Layer 0 Source Key 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SKEY[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SKEY[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SKEY**	SRCKEY	**Layer source color key** Active when source color key is enabled.

0000003 8 OVL_L0_SRC_SIZE Overlay Layer 0 Source Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				L0H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				L0W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**L0H**	L0_SRC_H	**Layer source height** Range: 0~8191
12:0	**L0W**	L0_SRC_W	**Layer source width** Range: 0~8191

0000003 C OVL_L0_OFFSET Overlay Layer0 Offset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				L0H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				L0XO												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**L0H**	L0_YOFF	**Layer vertical Y offset** Range: 0~8191
12:0	**L0XO**	L0_XOFF	**Layer horizontal X offset** Range: 0~8191

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00000044 OVL_L0_PITCH Overlay Layer 0 Pitch 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L0SP								L0SP		L0SP		L0SP		L0SP	
Type	RW								RW		RW		RW		RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L0SP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	L0SP	SURFL_EN	**Enables layer surface flinger alpha_blending** 0: Disable surface flinger alpha_blending 1: Enable surface flinger alpha_blending
23:22	L0SP	L0_DRGB_SEL	**Selects layer Destination_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
21:20	L0SP	L0_DA_SEL	**Selects layer Destination_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
19:18	L0SP	L0_SRGB_SEL	**Selects layer Source_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
17:16	L0SP	L0_SA_SEL	**Selects layer Source_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
15:0	L0SP	L0_SRC_PITCH	**Layer source pitch**

00000048 OVL_L0_TILE Overlay Layer 0 Tile Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TILE_BLKS										TILE_EN	TILE_W	TILE_H[19:16]			
Type	Other										Other	Other	Other			
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TILE_H[15:0]															
Type	Other															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	TILE_BL	TILE_HORI_BL	**Number of horizontal blocks**

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Bit(s)	Mnemonic	Name	Description
	KS	OCK_NUM	
21	TILE_EN	TILE_EN	**Enables tile mode** 0: Disable 1: Enable
20	TILE_W	TILE_WIDTH_SEL	**Width of tile** 0: Width = 16 1: Width = 32
19:0	TILE_H	TILE_HEIGHT	**Height of source tile mode**

00000050 **OVL_L1_CON** **Overlay Layer 1 Control** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DKEN	SKEN	LSRC				RGSW	BTSW		R_FIRST	LANDSCAPE	EN_3D	MTX			
Type	RW	RW	RW				RW	RW		RW	RW	RW	RW			
Reset	0	0	0	0			0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFMT				MTXEN	HFE	VFE	AEN	APHA							
Type	RW				Other	RW	RW	RW	RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	DKEN	DSTKEY_EN	**Enables destination color key** SRCKEY_EN and DSTKEY_EN are exclusive settings which cannot be enabled at the same time. 0: Disable destination color key 1: Enable destination color key
30	SKEN	SRCKEY_EN	**Enables source color key** SRCKEY_EN and DSTKEY_EN are exclusive settings which cannot be enabled at the same time. 0: Disable source color key 1: Enable source color key
29:28	LSRC	LAYER_SRC	**Selects layer pixel from memory/constant color/SCL/PQ** 00: Layer pixel from memory RDMA1 01: Layer pixel from constant color 10: Layer pixel from UFOd
25	RGSW	RGB_SWAP	**Not used**
24	BTSW	BYTE_SWAP	**Swaps unified color format** 0: RGB565, BGR888, BGRA8888, ABGR8888, UYVY, YUYV 1: BGR565, RGB888, RGBA8888, ARGB8888, VYUY, YVYU
22		R_FIRST	**Right eye image first when in 3D mode** 0: Show left eye image first in 3D mode 1: Show right eye image first in 3D mode
21		LANDSCAPE	**Enables 3D landscape mode** 0: 3D portrait mode 1: 3D landscape mode
20		EN_3D	**Enables 3D mode** 0: 2D mode 1: 3D mode

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Bit(s)	Mnemonic	Name	Description
19:16	**MTX**	INT_MTX_SEL	**Selects color matrix table** 0100: MTX_JPEG_TO_RGB 0110: MTX_BT601_TO_RGB 0111: MTX_BT709_TO_RGB Others: HW default (JPEG_TO_RGB)
15:12	**CFMT**	CLRFMT	**//--OLD definition** For reference only. 0000: RGB888 0001: RGB565 0010: ARGB8888 0011: PARGB8888 0100: xARGB8888 1000: YUYV 1001: UYVY 1010: YVYU 1011: VYUY 1111: YUV444 Others: Reserved color format 0000: RGB565 0001: RGB888 0010: RGBA8888/BGRA8888 0011: ARGB8888/ABGR8888 0100: UVVY, VYUY 0101: YUYV, YVYU
11	**MTXEN**	EXT_MTX_EN	**Enables external programmable coeff** 0: Matrix coeff 1: Programmable coeff
10	**HFE**	HORIZONTAL_FLIP_EN	**Enables horizontal flip function** 0: Disable horizontal flip function 1: Enable horizontal flip function
9	**VFE**	VERTICAL_FLIP_EN	**Enables vertical flip function** 0: Disable vertical flip function 1: Enable vertical flip function
8	**AEN**	ALPHA_EN	**Enables alpha blending** 0: Disable alpha blending 1: Enable alpha blending
7:0	**APHA**	ALPHA	**Constant alpha value**

00000054 **OVL_L1_SRCKEY** **Overlay Layer 1 Source Key** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SKEY[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SKEY[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SKEY**	SRCKEY	**Layer source color key** Active when source color key is enabled.

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00000058 OVL_L1_SRC_SIZE Overlay Layer 1 Source Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				L1H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				L1W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	L1H	L1_SRC_H	**Layer source height** Range: 0~8191
12:0	L1W	L1_SRC_W	**Layer source width** Range: 0~8191

0000005C OVL_L1_OFFSET Overlay Layer 1 Offset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				L1H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				L1XO												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	L1H	L1_YOFF	**Layer vertical Y offset** Range: 0~8191
12:0	L1XO	L1_XOFF	**Layer horizontal X offset** Range: 0~8191

00000064 OVL_L1_PITCH Overlay Layer1 Pitch 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L1SP								L1SP		L1SP		L1SP		L1SP	
Type	RW								RW		RW		RW		RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L1SP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	L1SP	SURFL_EN	**Enables layer surface flinger alpha_blending** 0: Disable surface flinger alpha_blending 1: Enable surface flinger alpha_blending

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Bit(s)	Mnemonic	Name	Description
23:22	L1SP	L1_DRGB_SEL	**Selects layer Destination_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
21:20	L1SP	L1_DA_SEL	**Selects layer Destination_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
19:18	L1SP	L1_SRGB_SEL	**Selects layer Source_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
17:16	L1SP	L1_SA_SEL	**Selects layer Source_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
15:0	L1SP	L1_SRC_PITCH	**Layer source pitch**

00000068 **OVL_L1_TILE** **Overlay Layer 1 Tile Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TILE_BLKS										TILE_EN	TILE_W	TILE_H[19:16]			
Type	Other										Other	Other	Other			
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TILE_H[15:0]															
Type	Other															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	TILE_BLKS	TILE_HORI_BLOCK_NUM	**Number of horizontal blocks**
21	TILE_EN	TILE_EN	**Enables tile mode** 0: Disable 1: Enable
20	TILE_W	TILE_WIDTH_SEL	**Width of tile** 0: Width = 16 1: Width = 32
19:0	TILE_H	TILE_HEIGHT	**Height of source tile mode**

00000070 **OVL_L2_CON** **Overlay Layer 2 Control** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DKEN	SKEN	LSRC				RGSW	BTSW		R_FIRST	LANDSC	EN_3D	MTX			

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											APE					
Type	RW	RW	RW				RW	RW		RW	RW	RW	RW			
Reset	0	0	0	0			0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFMT				MTX EN	HFE	VFE	AEN	APHA							
Type	RW				Other	RW	RW	RW	RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**DKEN**	DSTKEY_EN	**Enables destination color key** SRCKEY_EN and DSTKEY_EN are exclusive settings which cannot be enabled at the same time. 0: Disable destination color key 1: Enable destination color key
30	**SKEN**	SRCKEY_EN	**Enables source color key** SRCKEY_EN and DSTKEY_EN are exclusive settings which cannot be enabled at the same time. 0: Disable source color key 1: Enable source color key
29:28	**LSRC**	LAYER_SRC	**Selects layer pixel from memory/constant color/SCL/PQ** 00: Layer pixel from memory RDMA2 01: Layer pixel from constant color 10: Layer pixel from UFOd
25	**RGSW**	RGB_SWAP	**Not used**
24	**BTSW**	BYTE_SWAP	**Swaps unified color format** 0: RGB565, BGR888, BGRA8888, ABGR8888, UYVY, YUYV 1: BGR565, RGB888, RGBA8888, ARGB8888, VYUY, YVYU
22		R_FIRST	**Right eye image first when in 3D mode** 0: Show left eye image first in 3D mode 1: Show right eye image first in 3D mode
21		LANDSCAPE	**Enables 3D landscape mode** 0: 3D portrait mode 1: 3D landscape mode
20		EN_3D	**Enables 3D mode** 0: 2D mode 1: 3D mode
19:16	**MTX**	INT_MTX_SEL	**Selects color matrix table** 0100: MTX_JPEG_TO_RGB 0110: MTX_BT601_TO_RGB 0111: MTX_BT709_TO_RGB Others: HW default (JPEG_TO_RGB)
15:12	**CFMT**	CLRFMT	**//--OLD definition** For reference only. 0000: RGB888 0001: RGB565 0010: ARGB8888 0011: PARGB8888 0100: xARGB8888 1000: YUYV 1001: UYVY 1010: YVYU 1011: VYUY 1111: YUV444 Others: Reserved color format 0000: RGB565 0001: RGB888

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Bit(s)	Mnemonic	Name	Description
			0010: RGBA8888/BGRA8888 0011: ARGB8888/ABGR8888 0100: UVVY, VYUY 0101: YUYV, YVYU
11	**MTXEN**	EXT_MTX_EN	**Enables external programmable coeff** 0: Matrix coeff 1: Programmable coeff
10	**HFE**	HORIZONTAL_FLIP_EN	**Enables horizontal flip function** 0: Disable horizontal flip function 1: Enable horizontal flip function
9	**VFE**	VERTICAL_FLIP_EN	**Enables vertical flip function** 0: Disable vertical flip function 1: Enable vertical flip function
8	**AEN**	ALPHA_EN	**Enables alpha blending** 0: Disable alpha blending 1: Enable alpha blending
7:0	**APHA**	ALPHA	**Constant alpha value**

00000074 **OVL_L2_SRCKEY** **Overlay Layer 2 Source Key** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SKEY[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SKEY[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SKEY**	SRCKEY	**Layer source color key** Active when source color key is enabled.

00000078 **OVL_L2_SRC_SIZE** **Overlay Layer 2 Source Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				L2H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				L2W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**L2H**	L2_SRC_H	**Layer source height** Range: 0~8191
12:0	**L2W**	L2_SRC_W	**Layer source width** Range: 0~8191

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0000007C **OVL_L2_OFFSET** **Overlay Layer 2 Offset** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				L2H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				L2XO												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**L2H**	L2_YOFF	**Layer vertical Y offset** Range: 0~8191
12:0	**L2XO**	L2_XOFF	**Layer horizontal X offset** Range: 0~8191

00000084 **OVL_L2_PITCH** **Overlay Layer 2 Pitch** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L2SP								L2SP		L2SP		L2SP		L2SP	
Type	RW								RW		RW		RW		RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L2SP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**L2SP**	SURFL_EN	**Enables layer surface flinger alpha_blending** 0: Disable surface flinger alpha_blending 1: Enable surface flinger alpha_blending
23:22	**L2SP**	L2_DRGB_SEL	**Selects layer Destination_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
21:20	**L2SP**	L2_DA_SEL	**Selects layer Destination_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
19:18	**L2SP**	L2_SRGB_SEL	**Selects layer Source_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
17:16	**L2SP**	L2_SA_SEL	**Selects layer Source_Alpha alpha** 00: ONE 01: Src_Alpha

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Bit(s)	Mnemonic	Name	Description
			10: 1-Src_Alpha 11: Reserved
15:0	**L2SP**	L2_SRC_PITCH	**Layer source pitch**

00000088 **OVL_L2_TILE** **Overlay Layer 2 Tile Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**TILE_BLKS**										**TILE_EN**	**TILE_W**	**TILE_H[19:16]**			
Type	Other										Other	Other	Other			
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TILE_H[15:0]**															
Type	Other															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**TILE_BLKS**	TILE_HORI_BLOCK_NUM	**Number of horizontal blocks**
21	**TILE_EN**	TILE_EN	**Enables tile mode** 0: Disable 1: Enable
20	**TILE_W**	TILE_WIDTH_SEL	**Width of tile** 0: Width = 16 1: Width = 32
19:0	**TILE_H**	TILE_HEIGHT	**Height of source tile mode**

00000090 **OVL_L3_CON** **Overlay Layer 3 Control** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DKEN**	**SKEN**	**LSRC**				**RGSW**	**BTSW**		**R_FIRST**	**LANDSCAPE**	**EN_3D**	**MTX**			
Type	RW	RW	RW				RW	RW		RW	RW	RW	RW			
Reset	0	0	0	0			0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CFMT**				**MTXEN**	**HFE**	**VFE**	**AEN**	**APHA**							
Type	RW				Other	RW	RW	RW	RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**DKEN**	DSTKEY_EN	**Enables destination color key** SRCKEY_EN and DSTKEY_EN are exclusive settings which cannot be enabled at the same time. 0: Disable destination color key 1: Enable destination color key
30	**SKEN**	SRCKEY_EN	**Enables source color key** SRCKEY_EN and DSTKEY_EN are exclusive settings which cannot

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Bit(s)	Mnemonic	Name	Description
			be enabled at the same time. 0: Disable source color key 1: Enable source color key
29:28	**LSRC**	LAYER_SRC	**Select layer pixel from memory/constant color/SCL/PQ** 00: Layer pixel from Memory RDMA3 01: Layer pixel from Constant color 10: Layer pixel from UFOd 11: Layer pixel from PQ
25	**RGSW**	RGB_SWAP	**Not used**
24	**BTSW**	BYTE_SWAP	**Swaps unified color format** 0: RGB565, BGR888, BGRA8888, ABGR8888, UYVY, YUYV 1: BGR565, RGB888, RGBA8888, ARGB8888, VYUY, YVYU
22		R_FIRST	**Right eye image first when in 3D mode** 0: Show left eye image first in 3D mode 1: Show right eye image first in 3D mode
21		LANDSCAPE	**Enables 3D landscape mode** 0: 3D portrait mode 1: 3D landscape mode
20		EN_3D	**Enables 3D mode** 0: 2D mode 1: 3D mode
19:16	**MTX**	INT_MTX_SEL	**Selects color matrix table** 0100: MTX_JPEG_TO_RGB 0110: MTX_BT601_TO_RGB 0111: MTX_BT709_TO_RGB Others: HW default (JPEG_TO_RGB)
15:12	**CFMT**	CLRFMT	**//--OLD definition** For reference only. 0000: RGB888 0001: RGB565 0010: ARGB8888 0011: PARGB8888 0100: xARGB8888 1000: YUYV 1001: UYVY 1010: YVYU 1011: VYUY 1111: YUV444 Others: Reserved color format 0000: RGB565 0001: RGB888 0010: RGBA8888/BGRA8888 0011: ARGB8888/ABGR8888 0100: UVVY, VYUY 0101: YUYV, YVYU
11	**MTXEN**	EXT_MTX_EN	**Enables external programmable coeff** 0: Matrix coeff 1: Programmable coeff
10	**HFE**	HORIZONTAL_FLIP_EN	**Enables horizontal flip function** 0: Disable horizontal flip function 1: Enable horizontal flip function
9	**VFE**	VERTICAL_FLIP_EN	**Enables vertical flip function** 0: Disable vertical flip function 1: Enable vertical flip function
8	**AEN**	ALPHA_EN	**Enables alpha blending** 0: Disable alpha blending

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Bit(s)	Mnemonic	Name	Description
			1: Enable alpha blending
7:0	APHA	ALPHA	**Constant alpha value**

00000094 OVL_L3_SRCKEY Overlay Layer 3 Source Key 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SKEY[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SKEY[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	SKEY	SRCKEY	**Layer source color key** Active when source color key is enabled.

00000098 OVL_L3_SRC_SIZE Overlay Layer 3 Source Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				L3H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				L3W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	L3H	L3_SRC_H	**Layer source height** Range: 0~8191
12:0	L3W	L3_SRC_W	**Layer source width** Range: 0~8191

0000009C OVL_L3_OFFSET Overlay Layer 3 Offset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				L3H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				L3XO												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
28:16	**L3H**	L3_YOFF	**Layer vertical Y offset** Range: 0~8191
12:0	**L3XO**	L3_XOFF	**Layer horizontal X offset** Range: 0~8191

000000A4 OVL_L3_PITCH Overlay Layer3 Pitch 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L3SP								L3SP		L3SP		L3SP		L3SP	
Type	RW								RW		RW		RW		RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L3SP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**L3SP**	SURFL_EN	**Enables layer surface flinger alpha_blending** 0: Disable surface flinger alpha_blending 1: Enable surface flinger alpha_blending
23:22	**L3SP**	L3_DRGB_SEL	**Selects layer Destination_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
21:20	**L3SP**	L3_DA_SEL	**Selects layer Destination_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
19:18	**L3SP**	L3_SRGB_SEL	**Selects layer Source_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
17:16	**L3SP**	L3_SA_SEL	**Selects layer Source_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
15:0	**L3SP**	L3_SRC_PITCH	**Layer source pitch**

000000A8 OVL_L3_TILE Overlay Layer 3 Tile Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TILE_BLKS										TILE_EN	TILE_W	TILE_H[19:16]			
Type	Other										Other	Other	Other			
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TILE_H[15:0]															
Type	Other															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	TILE_BLKS	TILE_HORI_BLOCK_NUM	**Number of horizontal blocks**
21	TILE_EN	TILE_EN	**Enables tile mode** 0: Disable 1: Enable
20	TILE_W	TILE_WIDTH_SEL	**Width of tile** 0: Width = 16 1: Width = 32
19:0	TILE_H	TILE_HEIGHT	**Height of source tile mode**

000000C0 **OVL_RDMA0_CTRL** **Overlay RDMA0 Control** **03FF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						RDMA0_FIFO_USED_SIZE										
Type						RU										
Reset						0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RDMA0_INTERLACE				RDMA0_EN
Type												Other				RW
Reset												0				0

Bit(s)	Mnemonic	Name	Description
26:16		RDMA0_FIFO_USED_SIZE	**Overlay RDMA0 used size**
4		RDMA0_INTERLACE	**Overlay RDMA0 interlace** 0: Disable 1: Enable
0		RDMA0_EN	**Enables overlay RDMA0** 0: Disable 1: Enable

000000C8 **OVL_RDMA0_MEM_GMC_SETTING1** **Overlay RDMA0 Memory GMC Setting** **1010FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA0_PRE_ULTRA_THRESHOLD_HIGH_OFS								RDMA0_ULTRA_THRESHOLD_HIGH_OFS							
Type	Other								Other							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA0_PRE_ULTRA_THRESHOLD								RDMA0_ULTRA_THRESHOLD							

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Type	Other								Other							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		RDMA0_PRE_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA0 pre_ultra threshold high offset
23:16		RDMA0_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA0 ultra threshold high offset
15:8		RDMA0_PRE_ULTRA_THRESHOLD	Overlay RDMA0 pre_ultra threshold
7:0		RDMA0_ULTRA_THRESHOLD	Overlay RDMA0 ultra threshold

000000CC **OVL_RDMA0_MEM_SLOW_CON** **Overlay RDMA0 Memory Slow Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RDMA0_SLOW_CNT**															
Type	Other															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**RDMA0_SLOW_EN**
Type																Other
Reset																0

Bit(s)	Mnemonic	Name	Description
31:16		RDMA0_SLOW_CNT	**Overlay RDMA0 memory slow-down counter** After SLOW_CNT, SMI will raise greq again. 10: 10 cycles between 2 greq at least 33: 33 cycles between 2 greq at least
0		RDMA0_SLOW_EN	**Enables overlay RDMA0 memory slow-down** 0: Disable slow-down 1: Enable slow-down

000000D0 **OVL_RDMA0_FIFO_CTRL** **Overlay RDMA0 FIFO Control** **00800000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RDMA0_FIFO_UND_EN**						**RDMA0_FIFO_SIZE**									
Type	Oth						RW									

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	er															
Reset	0						0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**RDMA0_FIFO_THRD**									
Type							Other									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		RDMA0_FIFO_UND_EN	**Controls overlay RDMA0 FIFO underflow** 0: Disable FIFO underflow 1: Enable FIFO underflow
25:16		RDMA0_FIFO_SIZE	**Overlay RDMA0 FIFO size** Unit: 16 bytes 128: FIFO size is 128x128.
9:0		RDMA0_FIFO_THRD	**Overlay RDMA0 FIFO output valid threshold** Unit: 16 bytes. This value should be smaller than SRC_W*SRC_H*bpp >> 2. 0/1: If FIFO pointer >= 1, RDMA will send data valid to OVL. 2: If FIFO pointer >= 2, RDMA will send data valid to OVL.

000000E0 OVL_RDMA1_CTRL Overlay RDMA1 Control 03FF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						**RDMA1_FIFO_USED_SIZE**										
Type						RU										
Reset						0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**RDMA1_INTERLACE**				**RDMA1_EN**
Type												Other				RW
Reset												0				0

Bit(s)	Mnemonic	Name	Description
26:16		RDMA1_FIFO_USED_SIZE	**Overlay RDMA1 used size**
4		RDMA1_INTERLACE	**Overlay RDMA1 interlace** 0: Disable 1: Enable
0		RDMA1_EN	**Enables overlay RDMA1** 0: Disable 1: Enable

000000E8 OVL_RDMA1_MEM_GMC_SETTING1 Overlay RDMA1 Memory GMC Setting 1010FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RDMA1_PRE_ULTRA_THRESHOLD_HIGH_OFS**								**RDMA1_ULTRA_THRESHOLD_HIGH_OFS**							

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Type	Other								Other							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RDMA1_PRE_ULTRA_THRESHOLD**								**RDMA1_ULTRA_THRESHOLD**							
Type	Other								Other							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		RDMA1_PRE_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA1 pre_ultra threshold high offset
23:16		RDMA1_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA1 ultra threshold high offset
15:8		RDMA1_PRE_ULTRA_THRESHOLD	Overlay RDMA1 pre_ultra threshold
7:0		RDMA1_ULTRA_THRESHOLD	Overlay RDMA1 ultra threshold

000000EC **OVL_RDMA1_MEM_SLOW_CON** **Overlay RDMA1 Memory Slow Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RDMA1_SLOW_CNT**															
Type	Other															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**RDMA1_SLOW_EN**
Type																Other
Reset																0

Bit(s)	Mnemonic	Name	Description
31:16		RDMA1_SLOW_CNT	**Overlay RDMA1 memory slow-down counter** After SLOW_CNT, SMI will raise greq again. 10: 10 cycles between 2 greq at least 33: 33 cycles between 2 greq at least
0		RDMA1_SLOW_EN	**Enables overlay RDMA1 memory slow-down** 0: Disable slow-down 1: Enable slow-down

000000F0 **OVL_RDMA1_FIFO_CTRL** **Overlay RDMA1 FIFO Control** **00800000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RDMA1_FIFO_U**						**RDMA1_FIFO_SIZE**									

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	ND_ EN															
Type	Other						RW									
Reset	0						0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**RDMA1_FIFO_THRD**									
Type							Other									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		RDMA1_FIFO_UND_EN	**Controls overlay RDMA1 FIFO underflow** 0: Disable FIFO underflow 1: Enable FIFO underflow
25:16		RDMA1_FIFO_SIZE	**Overlay RDMA1 FIFO size** Unit: 16 bytes 128: FIFO size is 128x128.
9:0		RDMA1_FIFO_THRD	**Overlay RDMA1 FIFO output valid threshold** Unit: 16 bytes. This value should be smaller than SRC_W*SRC_H*bpp >> 2. 0/1: If FIFO pointer >= 1, RDMA will send data valid to OVL. 2: If FIFO pointer >= 2, RDMA will send data valid to OVL.

00000100 **OVL_RDMA2_CTRL** **Overlay RDMA2 Control** **03FF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						**RDMA2_FIFO_USED_SIZE**										
Type						RU										
Reset						0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**RDMA2_INTERLACE**				**RDMA2_EN**
Type												Other				RW
Reset												0				0

Bit(s)	Mnemonic	Name	Description
26:16		RDMA2_FIFO_USED_SIZE	**Overlay RDMA2 used size**
4		RDMA2_INTERLACE	**Overlay RDMA2 interlace** 0: Disable 1: Enable
0		RDMA2_EN	**Enables overlay RDMA2** 0: Disable 1: Enable

00000108 **OVL_RDMA2_MEM_GMC_SETTING1** **Overlay RDMA2 Memory GMC Setting** **1010FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	RDMA2_PRE_ULTRA_THRESHOLD_HIGH_OFS								RDMA2_ULTRA_THRESHOLD_HIGH_OFS							
Type	Other								Other							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA2_PRE_ULTRA_THRESHOLD								RDMA2_ULTRA_THRESHOLD							
Type	Other								Other							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		RDMA2_PRE_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA2 pre_ultra threshold high offset
23:16		RDMA2_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA2 ultra threshold high offset
15:8		RDMA2_PRE_ULTRA_THRESHOLD	Overlay RDMA2 pre_ultra threshold
7:0		RDMA2_ULTRA_THRESHOLD	Overlay RDMA2 ultra threshold

0000010C **OVL_RDMA2_MEM_SLOW_CON** **Overlay RDMA2 Memory Slow Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA2_SLOW_CNT															
Type	Other															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RDMA2_SLOW_EN
Type																Other
Reset																0

Bit(s)	Mnemonic	Name	Description
31:16		RDMA2_SLOW_CNT	**Overlay RDMA2 memory slow-down counter** After SLOW_CNT, SMI will raise greq again. 10: 10 cycles between 2 greq at least 33: 33 cycles between 2 greq at least
0		RDMA2_SLOW_EN	**Enables overlay RDMA2 memory slow-down** 0: Disable slow-down 1: Enable slow-down

00000110 **OVL_RDMA2_FIFO_CTRL** **Overlay RDMA2 FIFO Control** **00800000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RD						RDMA2_FIFO_SIZE									

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	MA2_FIFO_UND_EN															
Type	Other						RW									
Reset	0						0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RDMA2_FIFO_THRD									
Type							Other									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		RDMA2_FIFO_UND_EN	**Controls overlay RDMA2 FIFO underflow** 0: Disable FIFO underflow 1: Enable FIFO underflow
25:16		RDMA2_FIFO_SIZE	**Overlay RDMA2 FIFO size** Unit: 16 bytes 128: FIFO size is 128x128.
9:0		RDMA2_FIFO_THRD	**Overlay RDMA2 FIFO output valid threshold** Unit: 16 bytes. This value should be smaller than SRC_W*SRC_H*bpp >> 2. 0/1: If FIFO pointer >= 1, RDMA will send data valid to OVL. 2: If FIFO pointer >= 2, RDMA will send data valid to OVL.

00000120 **OVL_RDMA3_CTRL** **Overlay RDMA3 Control** **03FF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						RDMA3_FIFO_USED_SIZE										
Type						RU										
Reset						0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RDMA3_INTERLACE				RDMA3_EN
Type												Other				RW
Reset												0				0

Bit(s)	Mnemonic	Name	Description
26:16		RDMA3_FIFO_USED_SIZE	**Overlay RDMA3 used size**
4		RDMA3_INTERLACE	**Overlay RDMA3 interlace** 0: Disable 1: Enable
0		RDMA3_EN	**Enables overlay RDMA3** 0: Disable 1: Enable

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0000128 **OVL_RDMA3_MEM_GMC_SETTING1** **Overlay RDMA3 Memory GMC Setting** **1010FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA3_PRE_ULTRA_THRESHOLD_HIGH_OFS								RDMA3_ULTRA_THRESHOLD_HIGH_OFS							
Type	Other								Other							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA3_PRE_ULTRA_THRESHOLD								RDMA3_ULTRA_THRESHOLD							
Type	Other								Other							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		RDMA3_PRE_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA3 pre_ultra threshold high offset
23:16		RDMA3_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA3 ultra threshold high offset
15:8		RDMA3_PRE_ULTRA_THRESHOLD	Overlay RDMA3 pre_ultra threshold
7:0		RDMA3_ULTRA_THRESHOLD	Overlay RDMA3 ultra threshold

000012C **OVL_RDMA3_MEM_SLOW_CON** **Overlay RDMA3 Memory Slow Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA3_SLOW_CNT															
Type	Other															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RDMA3_SLOW_EN
Type																Other
Reset																0

Bit(s)	Mnemonic	Name	Description
31:16		RDMA3_SLOW_CNT	**Overlay RDMA3 memory slow-down counter** After SLOW_CNT, SMI will raise greq again. 10: 10 cycles between 2 greq at least 33: 33 cycles between 2 greq at least
0		RDMA3_SLOW_EN	**Enables overlay RDMA3 memory slow-down** 0: Disable slow-down 1: Enable slow-down

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00000130 OVL_RDMA3_FIFO_CTRL Overlay RDMA3 FIFO Control 00800000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA3_FIFO_UND_EN						RDMA3_FIFO_SIZE									
Type	Other						RW									
Reset	0						0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RDMA3_FIFO_THRD									
Type							Other									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		RDMA3_FIFO_UND_EN	**Controls overlay RDMA3 FIFO underflow** 0: Disable FIFO underflow 1: Enable FIFO underflow
25:16		RDMA3_FIFO_SIZE	**Overlay RDMA3 FIFO size** Unit: 16 bytes 128: FIFO size is 128x128.
9:0		RDMA3_FIFO_THRD	**Overlay RDMA3 FIFO output valid threshold** Unit: 16 bytes. This value should be smaller than SRC_W*SRC_H*bpp >> 2. 0/1: If FIFO pointer >= 1, RDMA will send data valid to OVL. 2: If FIFO pointer >= 2, RDMA will send data valid to OVL.

00000134 OVL_L0_Y2R_PARA_R0 Overlay L0 Y2R Conversion Parameter R0 00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_RMU												
Type				Other												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMY												
Type				Other												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_RMU	Overlay L0 YUV2RGB program parameter for R color of U component
12:0		C_CF_RMY	Overlay L0 YUV2RGB program parameter for R color of Y component

00000138 OVL_L0_Y2R_PARA_R1 Overlay L0 Y2R Conversion Parameter R1 0000057C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

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Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMV												
Type				Other												
Reset				0	0	1	0	1	0	1	1	1	1	1	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_RMV	Overlay L0 YUV2RGB program parameter for R color of V component

0000013C OVL_L0_Y2R_PARA_G0 Overlay L0 Y2R Conversion Parameter G0 1EA80400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_GMU												
Type				Other												
Reset				1	1	1	1	0	1	0	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMY												
Type				Other												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_GMU	Overlay L0 YUV2RGB program parameter for G color of U component
12:0		C_CF_GMY	Overlay L0 YUV2RGB program parameter for G color of Y component

00000140 OVL_L0_Y2R_PARA_G1 Overlay L0 Y2R Conversion Parameter G1 00001D35

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMV												
Type				Other												
Reset				1	1	1	0	1	0	0	1	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_GMV	Overlay L0 YUV2RGB program parameter for G color of V component

00000144 OVL_L0_Y2R_PARA_B0 Overlay L0 Y2R Conversion Parameter B0 06EE0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_BMU												
Type				Other												
Reset				0	0	1	1	0	1	1	1	0	1	1	1	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMY												
Type				Other												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_BMU	Overlay L0 YUV2RGB program parameter for B color of U component
12:0		C_CF_BMY	Overlay L0 YUV2RGB program parameter for B color of Y component

00000148 **OVL_L0_Y2R_PARA_B1** **Overlay L0 Y2R Conversion Parameter B1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMV												
Type				Other												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_BMV	Overlay L0 YUV2RGB program parameter for B color of V component

0000014C **OVL_L0_Y2R_PARA_YUV_A_0** **Overlay L0 Y2R Conversion Parameter Extended Add on YUV 0** **01800000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_UA								
Type								Other								
Reset								1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_YA								
Type								Other								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_UA	Overlay L0 YUV2RGB program parameter for U to add extended offset
8:0		C_CF_YA	Overlay L0 YUV2RGB program parameter for Y to add extended offset

00000150 **OVL_L0_Y2R_PARA_YUV_A_1** **Overlay L0 Y2R Conversion Parameter Extended Add on YUV 1** **00000180**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_VA								
Type								Other								
Reset								1	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_VA	Overlay L0 YUV2RGB program parameter for V to add extended offset

00000154 OVL_L0_Y2R_PARA_RGB_A_0 Overlay L0 Y2R Conversion Parameter Extended Add on RGB 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_GA								
Type								Other								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_RA								
Type								Other								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_GA	Overlay L0 YUV2RGB program parameter for G to add extended offset
8:0		C_CF_RA	Overlay L0 YUV2RGB program parameter for R to add extended offset

00000158 OVL_L0_Y2R_PARA_RGB_A_1 Overlay L0 Y2R Conversion Parameter Extended Add on RGB 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_BA								
Type								Other								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_BA	Overlay L0 YUV2RGB program parameter for B to add extended offset

0000015C OVL_L1_Y2R_PARA_R0 Overlay L1 Y2R Conversion Parameter R0 00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name				C_CF_RMU												
Type				Other												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMY												
Type				Other												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_RMU	Overlay L1 YUV2RGB program parameter for R color of U component
12:0		C_CF_RMY	Overlay L1 YUV2RGB program parameter for R color of Y component

00000160 OVL_L1_Y2R_PARA_R1 Overlay L1 Y2R Conversion Parameter R1 0000057C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMV												
Type				Other												
Reset				0	0	1	0	1	0	1	1	1	1	1	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_RMV	Overlay L1 YUV2RGB program parameter for R color of V component

00000164 OVL_L1_Y2R_PARA_G0 Overlay L1 Y2R Conversion Parameter G0 1EA80400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_GMU												
Type				Other												
Reset				1	1	1	1	0	1	0	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMY												
Type				Other												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_GMU	Overlay L1 YUV2RGB program parameter for G color of U component
12:0		C_CF_GMY	Overlay L1 YUV2RGB program parameter for G color of Y component

00000168 OVL_L1_Y2R_PARA_G1 Overlay L1 Y2R Conversion Parameter G1 00001D35

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMV												
Type				Other												
Reset				1	1	1	0	1	0	0	1	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_GMV	Overlay L1 YUV2RGB program parameter for G color of V component

0000016C **OVL_L1_Y2R_PARA_B0** **Overlay L1 Y2R Conversion Parameter B0** **06EE0400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_BMU												
Type				Other												
Reset				0	0	1	1	0	1	1	1	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMY												
Type				Other												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_BMU	Overlay L1 YUV2RGB program parameter for B color of U component
12:0		C_CF_BMY	Overlay L1 YUV2RGB program parameter for B color of Y component

00000170 **OVL_L1_Y2R_PARA_B1** **Overlay L1 Y2R Conversion Parameter B1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMV												
Type				Other												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_BMV	Overlay L1 YUV2RGB program parameter for B color of V component

00000174 **OVL_L1_Y2R_PARA_YUV_A_0** **Overlay L1 Y2R Conversion Parameter Extended Add on YUV 0** **01800000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_UA								

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Type								Other								
Reset								1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_YA								
Type								Other								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_UA	Overlay L1 YUV2RGB program parameter for U to add extended offset
8:0		C_CF_YA	Overlay L1 YUV2RGB program parameter for Y to add extended offset

00000178 OVL_L1_Y2R_PARA_YUV_A_1 Overlay L1 Y2R Conversion Parameter Extended Add on YUV 1 00000180

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_VA								
Type								Other								
Reset								1	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_VA	Overlay L1 YUV2RGB program parameter for V to add extended offset

0000017C OVL_L1_Y2R_PARA_RGB_A_0 Overlay L1 Y2R Conversion Parameter Extended Add on RGB 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_GA								
Type								Other								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_RA								
Type								Other								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_GA	Overlay L1 YUV2RGB program parameter for G to add extended offset
8:0		C_CF_RA	Overlay L1 YUV2RGB program parameter for R to add extended offset

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00000180 OVL_L1_Y2R_PARA_RGB_A_1 Overlay L1 Y2R Conversion Parameter Extended Add on RGB 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**C_CF_BA**								
Type								Other								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_BA	Overlay L1 YUV2RGB program parameter for B to add extended offset

00000184 OVL_L2_Y2R_PARA_R0 Overlay L2 Y2R Conversion Parameter R0 00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**C_CF_RMU**												
Type				Other												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**C_CF_RMY**												
Type				Other												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_RMU	Overlay L2 YUV2RGB program parameter for R color of U component
12:0		C_CF_RMY	Overlay L2 YUV2RGB program parameter for R color of Y component

00000188 OVL_L2_Y2R_PARA_R1 Overlay L2 Y2R Conversion Parameter R1 0000057C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**C_CF_RMV**												
Type				Other												
Reset				0	0	1	0	1	0	1	1	1	1	1	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_RMV	Overlay L2 YUV2RGB program parameter for R color of V component

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0000018C OVL_L2_Y2R_PARA_G0 Overlay L2 Y2R Conversion Parameter G0 1EA80400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_GMU												
Type				Other												
Reset				1	1	1	1	0	1	0	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMY												
Type				Other												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_GMU	Overlay L2 YUV2RGB program parameter for G color of U component
12:0		C_CF_GMY	Overlay L2 YUV2RGB program parameter for G color of Y component

00000190 OVL_L2_Y2R_PARA_G1 Overlay L2 Y2R Conversion Parameter G1 00001D35

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMV												
Type				Other												
Reset				1	1	1	0	1	0	0	1	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_GMV	Overlay L2 YUV2RGB program parameter for G color of V component

00000194 OVL_L2_Y2R_PARA_B0 Overlay L2 Y2R Conversion Parameter B0 06EE0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_BMU												
Type				Other												
Reset				0	0	1	1	0	1	1	1	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMY												
Type				Other												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_BMU	Overlay L2 YUV2RGB program parameter for B color of U component
12:0		C_CF_BMY	Overlay L2 YUV2RGB program parameter for B color of Y component

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00000198	OVL_L2_Y2R_PARA_B1	Overlay L2 Y2R Conversion Parameter B1	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMV												
Type				Other												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_BMV	Overlay L2 YUV2RGB program parameter for B color of V component

0000019C	OVL_L2_Y2R_PARA_YUV_A_0	Overlay L2 Y2R Conversion Parameter Extended Add on YUV 0	01800000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_UA								
Type								Other								
Reset								1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_YA								
Type								Other								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_UA	Overlay L2 YUV2RGB program parameter for U to add extended offset
8:0		C_CF_YA	Overlay L2 YUV2RGB program parameter for Y to add extended offset

000001A0	OVL_L2_Y2R_PARA_YUV_A_1	Overlay L2 Y2R Conversion Parameter Extended Add on YUV 1	00000180

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_VA								
Type								Other								
Reset								1	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_VA	Overlay L2 YUV2RGB program parameter for V to add extended offset

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000001A4 OVL_L2_Y2R_PARA_RGB_A_0 — Overlay L2 Y2R Conversion Parameter Extended Add on RGB 0 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_GA								
Type								Other								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_RA								
Type								Other								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_GA	Overlay L2 YUV2RGB program parameter for G to add extended offset
8:0		C_CF_RA	Overlay L2 YUV2RGB program parameter for R to add extended offset

000001A8 OVL_L2_Y2R_PARA_RGB_A_1 — Overlay L2 Y2R Conversion Parameter Extended Add on RGB 1 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_BA								
Type								Other								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_BA	Overlay L2 YUV2RGB program parameter for B to add extended offset

000001AC OVL_L3_Y2R_PARA_R0 — Overlay L3 Y2R Conversion Parameter R0 — 00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_RMU												
Type				Other												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMY												
Type				Other												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_RMU	Overlay L3 YUV2RGB program parameter for R color of U component
12:0		C_CF_RMY	Overlay L3 YUV2RGB program parameter for R color of Y component

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000001B0 OVL_L3_Y2R_PARA_R1 Overlay L3 Y2R Conversion Parameter R1 0000057C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMV												
Type				Other												
Reset				0	0	1	0	1	0	1	1	1	1	1	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_RMV	Overlay L3 YUV2RGB program parameter for R color of V component

000001B4 OVL_L3_Y2R_PARA_G0 Overlay L3 Y2R Conversion Parameter G0 1EA80400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_GMU												
Type				Other												
Reset				1	1	1	1	0	1	0	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMY												
Type				Other												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_GMU	Overlay L3 YUV2RGB program parameter for G color of U component
12:0		C_CF_GMY	Overlay L3 YUV2RGB program parameter for G color of Y component

000001B8 OVL_L3_Y2R_PARA_G1 Overlay L3 Y2R Conversion Parameter G1 00001D35

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMV												
Type				Other												
Reset				1	1	1	0	1	0	0	1	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_GMV	Overlay L3 YUV2RGB program parameter for G color of V component

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000001BC OVL_L3_Y2R_PARA_B0 Overlay L3 Y2R Conversion Parameter B0 06EE0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_BMU												
Type				Other												
Reset				0	0	1	1	0	1	1	1	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMY												
Type				Other												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_BMU	Overlay L3 YUV2RGB program parameter for B color of U component
12:0		C_CF_BMY	Overlay L3 YUV2RGB program parameter for B color of Y component

000001C0 OVL_L3_Y2R_PARA_B1 Overlay L3 Y2R Conversion Parameter B1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMV												
Type				Other												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_BMV	Overlay L3 YUV2RGB program parameter for B color of V component

000001C4 OVL_L3_Y2R_PARA_YUV_A_0 Overlay L3 Y2R Conversion Parameter Extended Add on YUV 0 01800000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_UA								
Type								Other								
Reset								1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_YA								
Type								Other								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_UA	Overlay L3 YUV2RGB program parameter for U to add extended offset
8:0		C_CF_YA	Overlay L3 YUV2RGB program parameter for Y to add extended offset

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000001C8 **OVL_L3_Y2R_PARA_YUV_A_1** **Overlay L3 Y2R Conversion Parameter Extended Add on YUV 1** **00000180**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_VA								
Type								Other								
Reset								1	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_VA	Overlay L3 YUV2RGB program parameter for V to add extended offset

000001CC **OVL_L3_Y2R_PARA_RGB_A_0** **Overlay L3 Y2R Conversion Parameter Extended Add on RGB 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_GA								
Type								Other								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_RA								
Type								Other								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_GA	Overlay L3 YUV2RGB program parameter for G to add extended offset
8:0		C_CF_RA	Overlay L3 YUV2RGB program parameter for R to add extended offset

000001D0 **OVL_L3_Y2R_PARA_RGB_A_1** **Overlay L3 Y2R Conversion Parameter Extended Add on RGB 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_BA								
Type								Other								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_BA	Overlay L3 YUV2RGB program parameter for B to add extended offset

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000001D4	OVL_DEBUG_MON_SEL	Overlay Debug Monitor Select	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DBG_MON_SEL			
Type													WO			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0		DBG_MON_SEL	Selects overlay debugging monitor

000001E0	OVL_RDMA0_MEM_GMC_SETTING2	Overlay RDMA0 Memory GMC Setting	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RDMA0_ISSUE_REQ_THRESHOLD							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		RDMA0_ISSUE_REQ_THRESHOLD	**Overlay RDMA0 issue request threshold** 0 is for the best performance.

000001E4	OVL_RDMA1_MEM_GMC_SETTING2	Overlay RDMA1 Memory GMC Setting	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RDMA1_ISSUE_REQ_THRESHOLD							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		RDMA1_ISSUE_REQ_THRESHOLD	**Overlay RDMA1 issue request threshold** 0 is for the best performance.

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000001E8	OVL_RDMA2_MEM_GMC_SETTING2	Overlay RDMA2 Memory GMC Setting	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RDMA2_ISSUE_REQ_THRESHOLD							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		RDMA2_ISSUE_REQ_THRESHOLD	**Overlay RDMA2 issue request threshold** 0 is for the best performance.

000001EC	OVL_RDMA3_MEM_GMC_SETTING2	Overlay RDMA3 Memory GMC Setting	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RDMA3_ISSUE_REQ_THRESHOLD							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		RDMA3_ISSUE_REQ_THRESHOLD	**Overlay RDMA3 issue request threshold** 0 is for the best performance.

00000200	OVL_DUMMY_REG	Overlay Dummy Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OVERLAY_DUMMY[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OVERLAY_DUMMY[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		OVERLAY_DUMMY	Overlay dummy register

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00000230	OVL_SMI_DBG	Overlay SMI Arbiter Debug Monitor	00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name							**SMI_FSM**									
Type							RU									
Reset							0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
9:0		SMI_FSM	Overlay SMI arbiter FSM state

00000234	OVL_GREQ_LAYER_CNT	Overlay Layer Greq Counter	01010101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			**LAYER3_GREQ_CNT**								**LAYER2_GREQ_CNT**					
Type			RU								RU					
Reset			0	0	0	0	0	1			0	0	0	0	0	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name			**LAYER1_GREQ_CNT**								**LAYER0_GREQ_CNT**					
Type			RU								RU					
Reset			0	0	0	0	0	1			0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
29:24		LAYER3_GREQ_CNT	RDMA Layer 3 greq counter
21:16		LAYER2_GREQ_CNT	RDMA Layer 2 greq counter
13:8		LAYER1_GREQ_CNT	RDMA Layer 1 greq counter
5:0		LAYER0_GREQ_CNT	RDMA Layer 0 greq counter

00000240	OVL_FLOW_CTRL_DBG	Overlay Flow Control Debug Monitor	000FBC01

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**OVL_UPD_REG**	**REG_UPDATE**	**OVL_CLR**	**OVL_START**	**OVL_RUNNING**	**FRAME_DONE**	**FRAME_UNDERRUN**	**FRAME_SWRST_DONE**	**FRAME_HWRST_DONE**		**TRIG**	**RST**	**RDMA0_IDLE**	**RDMA1_IDLE**	**RDMA2_IDLE**	**RDMA3_IDLE**
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU		RU	RU	RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0		0	0	1	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	**OUT_IDLE**		**OVL_OUT_R**	**OVL_OUT_V**	**BLEND_IDL**	**ADDCON_ID**	**FSM_STATE**									

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			EADY	ALID	E	LE										
Type	RU		RU	RU	RU	RU	RU									
Reset	1		1	1	1	1	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31		OVL_UPD_REG	Overlay prepare to update register
30		REG_UPDATE	Updates overlay register
29		OVL_CLR	Clears overlay
28		OVL_START	Starts overlay
27		OVL_RUNNING	Overlay running
26		FRAME_DONE	Overlay frame completed
25		FRAME_UNDERRUN	Overlay frame underrun
24		FRAME_SWRST_DONE	Overlay frame reset done
23		FRAME_HWRST_DONE	Overlay EOF reset done
21		TRIG	Triggers overlay
20		RST	Resets overlay
19		RDMA0_IDLE	Overlay RDMA0 idle state
18		RDMA1_IDLE	Overlay RDMA1 idle state
17		RDMA2_IDLE	Overlay RDMA2 idle state
16		RDMA3_IDLE	Overlay RDMA3 idle state
15		OUT_IDLE	Overlay output relay idle state
13		OVL_OUT_READY	Overlay out_ready
12		OVL_OUT_VALID	Overlay out_valid
11		BLEND_IDLE	Overlay alpha blending idle state
10		ADDCON_IDLE	Overlay addcon idle state
9:0		FSM_STATE	Overlay flow control FSM state 0x1: IDLE 0x2: WAIT 0x4: PREPARE 0x8: UPD_REG 0x10: ENG_CLR 0x20: ENG_ACT 0x40: H_WAIT_W_RST 0x80: S_WAIT_W_RST 0x100: H_W_RST 0x200: S_W_RST

00000244 **OVL_ADDCON_DBG** **Overlay Address Control Debug** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L3_WIN_HIT	L2_WIN_HIT		ROI_Y												
Type	RU	RU		RU												
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L1_WIN_HIT	L0_WIN_HIT		ROI_X												
Type	RU	RU		RU												
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		L3_WIN_HIT	Overlay Layer 3 pixel hit
30		L2_WIN_HIT	Overlay Layer 2 pixel hit
28:16		ROI_Y	Overlay pixel process vertical Y position
15		L1_WIN_HIT	Overlay Layer 1 pixel hit
14		L0_WIN_HIT	Overlay Layer 0 pixel hit
12:0		ROI_X	Overlay pixel process horizontal X position

0000024C **OVL_RDMA0_DBG** **Overlay RDMA0 Debug Monitor** **10000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SMI_GREQ	RDMA0_SMI_BUSY	RDMA0_OUT_VALID	RDMA0_OUT_READY	RDMA0_OUT_DATA[23:12]											
Type	RU	RU	RU	RU	RU											
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RDMA0_OUT_DATA[11:0]												RDMA0_LAYER_GREQ	RDMA0_WRAM_RST_CS		
Type	RU												RU	RU		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31		SMI_GREQ	Overlay 4-to-1 SMI request
30		RDMA0_SMI_BUSY	Overlay RDMA0 SMI busy
29		RDMA0_OUT_VALID	Overlay RDMA0 output valid
28		RDMA0_OUT_READY	Overlay RDMA0 output ready
27:4		RDMA0_OUT_DATA	Overlay RDMA0 output data
3		RDMA0_LAYER_GREQ	Overlay RDMA0 SMI request
2:0		RDMA0_WRAM_RST_CS	Overlay RDMA0 warm reset current state

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00000250 OVL_RDMA1_DBG Overlay RDMA1 Debug Monitor 10000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SMI_GREQ	RDMA1_SMI_BUSY	RDMA1_OUT_VALID	RDMA1_OUT_READY	RDMA1_OUT_DATA[23:12]											
Type	RU	RU	RU	RU	RU											
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA1_OUT_DATA[11:0]												RDMA1_LAYER_GREQ	RDMA1_WRAM_RST_CS		
Type	RU												RU	RU		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31		SMI_GREQ	Overlay 4-to-1 SMI request
30		RDMA1_SMI_BUSY	Overlay RDMA1 SMI busy
29		RDMA1_OUT_VALID	Overlay RDMA1 output valid
28		RDMA1_OUT_READY	Overlay RDMA1 output ready
27:4		RDMA1_OUT_DATA	Overlay RDMA1 output data
3		RDMA1_LAYER_GREQ	Overlay RDMA1 SMI request
2:0		RDMA1_WRAM_RST_CS	Overlay RDMA1 warm reset current state

00000254 OVL_RDMA2_DBG Overlay RDMA2 Debug Monitor 10000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SMI_GREQ	RDMA2_SMI_BUSY	RDMA2_OUT_VALID	RDMA2_OUT_READY	RDMA2_OUT_DATA[23:12]											
Type	RU	RU	RU	RU	RU											
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA2_OUT_DATA[11:0]												RDMA2_LAYER_GREQ	RDMA2_WRAM_RST_CS		
Type	RU												RU	RU		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
31		SMI_GREQ	Overlay 4-to-1 SMI request
30		RDMA2_SMI_BUSY	Overlay RDMA2 SMI busy
29		RDMA2_OUT_VALID	Overlay RDMA2 output valid
28		RDMA2_OUT_READY	Overlay RDMA2 output ready
27:4		RDMA2_OUT_DATA	Overlay RDMA2 output data
3		RDMA2_LAYER_GREQ	Overlay RDMA2 SMI request
2:0		RDMA2_WRAM_RST_CS	Overlay RDMA2 warm reset current state

00000258 **OVL_RDMA3_DBG** **Overlay RDMA3 Debug Monitor** **10000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SMI_GREQ	RDMA3_SMI_BUSY	RDMA3_OUT_VALID	RDMA3_OUT_READY	RDMA3_OUT_DATA[23:12]											
Type	RU	RU	RU	RU	RU											
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA3_OUT_DATA[11:0]												RDMA3_LAYER_GREQ	RDMA3_WRAM_RST_CS		
Type	RU												RU	RU		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31		SMI_GREQ	Overlay 4-to-1 SMI request
30		RDMA3_SMI_BUSY	Overlay RDMA3 SMI busy
29		RDMA3_OUT_VALID	Overlay RDMA3 output valid
28		RDMA3_OUT_READY	Overlay RDMA3 output ready
27:4		RDMA3_OUT_DATA	Overlay RDMA3 output data
3		RDMA3_LAYER_GREQ	Overlay RDMA3 SMI request
2:0		RDMA3_WRAM_RST_CS	Overlay RDMA3 warm reset current state

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0000025C OVL_L0_CLR Overlay Layer 0 Constant Color FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ALPHA								RED							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GREEN								BLUE							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		ALPHA	Alpha component of L0 constant color
23:16		RED	Red component of L0 constant color
15:8		GREEN	Green component of L0 constant color
7:0		BLUE	Blue component of L0 constant color

00000260 OVL_L1_CLR Overlay Layer 1 Constant Color FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ALPHA								RED							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GREEN								BLUE							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		ALPHA	Alpha component of L1 constant color
23:16		RED	Red component of L1 constant color
15:8		GREEN	Green component of L1 constant color
7:0		BLUE	Blue component of L1 constant color

00000264 OVL_L2_CLR Overlay Layer 2 Constant Color FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ALPHA								RED							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GREEN								BLUE							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		ALPHA	Alpha component of L2 constant color
23:16		RED	Red component of L2 constant color
15:8		GREEN	Green component of L2 constant color

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Bit(s)	Mnemonic	Name	Description
7:0		BLUE	Blue component of L2 constant color

00000268 **OVL_L3_CLR** **Overlay Layer 3 Constant Color** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ALPHA								RED							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GREEN								BLUE							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		ALPHA	Alpha component of L3 constant color
23:16		RED	Red component of L3 constant color
15:8		GREEN	Green component of L3 constant color
7:0		BLUE	Blue component of L3 constant color

00000F40 **OVL_L0_ADDR** **Overlay Layer 0 Memory Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L0AD[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L0AD[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**L0AD**	L0_ADDR	Layer memory buffer address

00000F60 **OVL_L1_ADDR** **Overlay Layer 1 Memory Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L1AD[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L1AD[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**L1AD**	L1_ADDR	Layer memory buffer address

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00000F80	OVL_L2_ADDR	Overlay Layer 2 Memory Address	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L2AD[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L2AD[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	L2AD	L2_ADDR	Layer memory buffer address

00000FA0	OVL_L3_ADDR	Overlay Layer 3 Memory Address	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L3AD[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L3AD[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	L3AD	L3_ADDR	Layer memory buffer address

00000FC0	OVL_SECURE	Overlay Layer Secure Bit	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													L3_SECURE	L2_SECURE	L1_SECURE	L0_SECURE
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3		L3_SECURE	Layer 3 secure bit
2		L2_SECURE	Layer 2 secure bit
1		L1_SECURE	Layer 1 secure bit
0		L0_SECURE	Layer 0 secure bit

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6.11.5 Programming Guide

Register settings:

1. Configure DATAPATH (number of layers, layer source, color format, etc).
2. Configure RDMA parameters (addr/size/fmt/swap).
3. Configure layer parameters (layer size/offset/roi size).

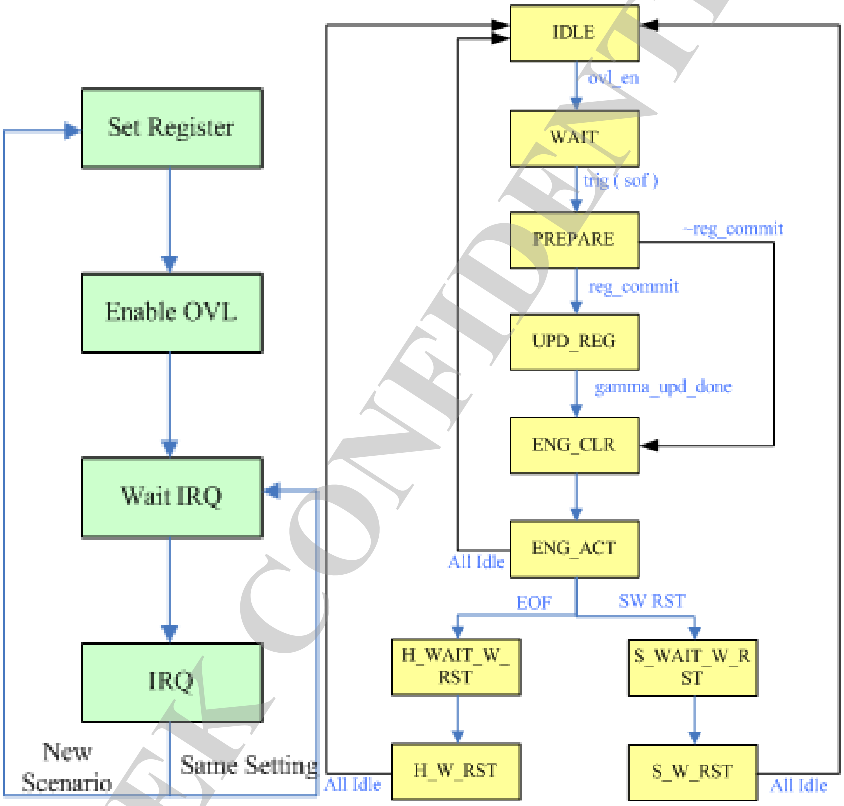

Figure 6-37. Typical DISP_OVL programming procedure

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6.12 DISP RDMA (Display Read Direct Memory Access)

6.12.1 Introduction

The RDMA engine is responsible of providing data to the interface engines, e.g. DSI, DBI and DPI. Because the interface engines need the real time service, the RDMA engine contains one line buffer to store the sufficient pixel data. It also detects the usage of data buffer to trigger the deep sleep mode of EMI.

6.12.2 Features

- Direct link input mode
- Memory input mode
  - Input format: YUYV422, UYVY422, YVYU422, UYVY422, RGB565, RGB888, ARGB8888
  - Input footprint: Raster-scan mode, 64 byte-aligned tile mode
  - Slow down mode
- Output control
  - Byte swap, RGB swap
  - Progressive mode, Interlace mode
  - Programmable YUV to RGB matrix
  - Non-stop output mode if the data buffer is under-running
- Buffer control
  - 240x16 byte data buffer (1280 pixels with RGB888 format)
  - Programmable request/pre-ultra/ultra control mechanism

6.12.3 Block Diagram

The following figure shows the detailed block diagram of RDMA engine. The clocks are automatically configured and one asynchronous FIFO is used for the output clock domain.

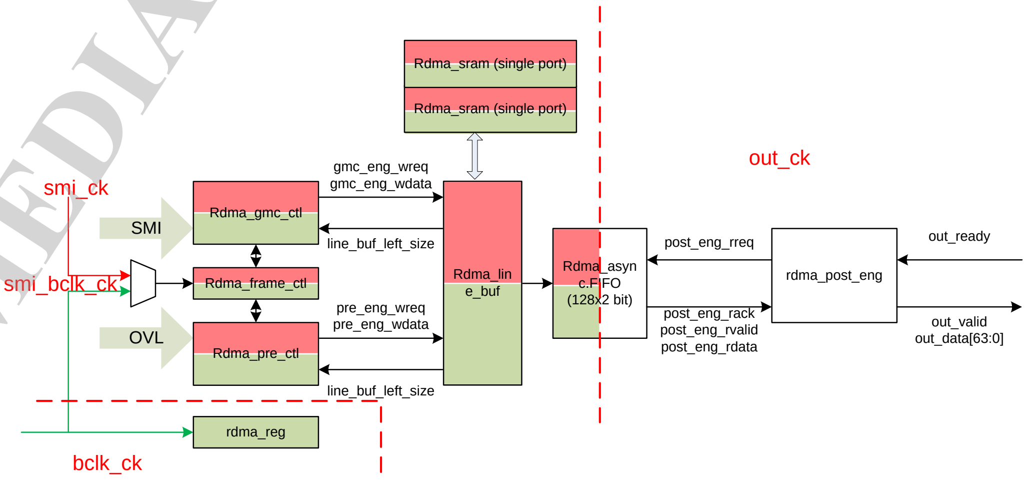

Figure 6-38. Block diagram of RDMA engine

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6.12.4 Register Definition

Module name: DISP_RDMA Base address: (+14008000h)

Address	Name	Width	Register Function
14008000	DISP_RDMA_INT_ENABLE	32	RDMA Interrupt Enable
14008004	DISP_RDMA_INT_STATUS	32	RDMA Interrupt Status
14008010	DISP_RDMA_GLOBAL_CON	32	RDMA Global Control
14008014	DISP_RDMA_SIZE_CON_0	32	RDMA Size Control 0
14008018	DISP_RDMA_SIZE_CON_1	32	RDMA Size Control 1
1400801C	DISP_RDMA_TARGET_LINE	32	RDMA Target Line
14008024	DISP_RDMA_MEM_CON	32	RDMA Memory Mode Control
1400802C	DISP_RDMA_MEM_SRC_PITCH	32	RDMA Memory Mode Line Pitch
14008030	DISP_RDMA_MEM_GMC_SETTING_0	32	RDMA Memory Mode GMC Setting 0
14008034	DISP_RDMA_MEM_SLOW_CON	32	RDMA Memory Mode Slow Control
14008038	DISP_RDMA_MEM_GMC_SETTING_1	32	RDMA Memory Mode GMC Setting 1
14008040	DISP_RDMA_FIFO_CON	32	RDMA FIFO Control
14008044	DISP_RDMA_FIFO_LOG	32	RDMA_FIFO_LOG
14008054	DISP_RDMA_C00	32	RDMA YUV to RGB Coefficient
14008058	DISP_RDMA_C01	32	RDMA YUV to RGB Coefficient
1400805C	DISP_RDMA_C02	32	RDMA YUV to RGB Coefficient
14008060	DISP_RDMA_C10	32	RDMA YUV to RGB Coefficient
14008064	DISP_RDMA_C11	32	RDMA YUV to RGB Coefficient
14008068	DISP_RDMA_C12	32	RDMA YUV to RGB Coefficient
1400806C	DISP_RDMA_C20	32	RDMA YUV to RGB Coefficient
14008070	DISP_RDMA_C21	32	RDMA YUV to RGB Coefficient
14008074	DISP_RDMA_C22	32	RDMA YUV to RGB Coefficient
14008078	DISP_RDMA_PRE_ADD_0	32	RDMA YUV to RGB Coefficient
1400807C	DISP_RDMA_P	32	RDMA YUV to RGB Coefficient

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Address	Name	Width	Register Function
	RE_ADD_1		
14008080	DISP_RDMA_PRE_ADD_2	32	RDMA YUV to RGB Coefficient
14008084	DISP_RDMA_POST_ADD_0	32	RDMA YUV to RGB Coefficient
14008088	DISP_RDMA_POST_ADD_1	32	RDMA YUV to RGB Coefficient
1400808C	DISP_RDMA_POST_ADD_2	32	RDMA YUV to RGB Coefficient
14008090	DISP_RDMA_DUMMY	32	RDMA Dummy Register
14008094	DISP_RDMA_DEBUG_OUT_SEL	32	RDMA Debug Output Selection
14008F00	DISP_RDMA_MEM_START_ADDR	32	RDMA Memory Mode Start Address

14008000 DISP_RDMA_INT_ENABLE RDMA Interrupt Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										FIFO_EMPTY_INT_EN	TARGET_LINE_INT_EN	FIFO_UNDERFLOW_INT_EN	EOF_ABNORMAL_INT_EN	FRAME_END_INT_EN	FRAME_START_INT_EN	REG_UPDATE_INT_EN
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	FIFO_EMPTY_INT_EN	**Enables FIFO empty interrupt** 0: Disable 1: Enable
5	TARGET_LINE_INT_EN	**Enables target line interrupt** 0: Disable 1: Enable
4	FIFO_UNDERFLOW_INT_EN	**Enables FIFO underflow interrupt** 0: Disable 1: Enable
3	EOF_ABNORMAL_INT_EN	**Enables abnormal EOF interrupt** 0: Disable 1: Enable
2	FRAME_END_INT_EN	**Enables frame end interrupt** 0: Disable 1: Enable
1	FRAME_START_INT_EN	**Enables frame start interrupt** 0: Disable 1: Enable
0	REG_UPDATE_INT_	**Enables working register update done interrupt**

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Bit(s)	Name	Description
	EN	0: Disable 1: Enable

14008004 DISP_RDMA_INT_STATUS RDMA Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name										FIFO_EMPTY_INT_FLAG	TARGET_LINE_INT_FLAG	FIFO_UNDERFLOW_INT_FLAG	EOF_ABNORMAL_INT_FLAG	FRAME_END_INT_FLAG	FRAME_START_INT_FLAG	REG_UPDATE_INT_FLAG
Type										A1	A1	A1	A1	A1	A1	A1
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	FIFO_EMPTY_INT_FLAG	**FIFO empty interrupt status** If FIFO is empty, this flag will be asserted.
5	TARGET_LINE_INT_FLAG	**Target line interrupt status** If line number reach the target line, this flag will be asserted.
4	FIFO_UNDERFLOW_INT_FLAG	**FIFO underflow interrupt status** If FIFO underflow is enabled and FIFO is exhausted, this flag will be asserted.
3	EOF_ABNORMAL_INT_FLAG	**Abnormal EOF interrupt status** If EOF is coming but one frame is not finished, this flag will be asserted.
2	FRAME_END_INT_FLAG	**Frame end interrupt status**
1	FRAME_START_INT_FLAG	**Frame start interrupt status**
0	REG_UPDATE_INT_FLAG	**Working register update done interrupt status**

14008010 DISP_RDMA_GLOBAL_CON RDMA Global Control 00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				SMI_BUSY		RESET_STATE						SOFT_RESET			MODE_SEL	ENGINE_EN
Type				RU		RU						RW			RW	RW
Reset				0		0	0	1				0			0	0

Bit(s)	Name	Description
12	SMI_BUSY	**GMC busy**

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Bit(s)	Name	Description
		If GMC request is accepted but GMC data not yet completely returned, this bit will be asserted. 0: Idle 1: Busy
10:8	RESET_STATE	**Soft reset state machine**
4	SOFT_RESET	**Soft reset** Write 1 to soft reset and write 0 to it, the polling reset state machine will be done (0x1). 0: Disable soft reset 1: Enable soft reset
1	MODE_SEL	**Selects mode** 0: Direct link mode 1: Memory mode
0	ENGINE_EN	**Controls engine enabling** 0: Engine off 1: Engine on

14008014 **DISP_RDMA_SIZE_CON_0** **RDMA Size Control 0** **00B00280**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									MATRIX_INT_MTX_SEL					MATRIX_WIDE_GAMUT_EN	MATRIX_ENABLE	MATRIX_EXT_MTX_EN
Type									RW					RW	RW	RW
Reset									1	0	1	1		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OUTPUT_FRAME_WIDTH												
Type				RW												
Reset				0	0	0	1	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:20	MATRIX_INT_MTX_SEL	**Selects pre-defined color transform coefficient** 4'b0000: RGB to JPEG 4'b0010: RGB to BT601 4'b0011: RGB to BT709 4'b0100: JPEG to RGB 4'b0110: BT601 to RGB 4'b0111: BT709 to RGB 4'b1000: JPEG to BT601 4'b1001: JPEG to BT709 4'b1010: BT601 to JPEG 4'b1011: BT709 to JPEG 4'b1100: BT709 to BT601 4'b1101: BT601 to BT709
18	MATRIX_WIDE_GAMUT_EN	**When MATRIX_EANBLE, the output data can be chosen.** 0: sRGB [0:255] 1: ext-sRGB [-512:511]
17	MATRIX_ENABLE	**Enables color format transformation** The output data are XRGB or XYUV. 0: Bypass color matrix 1: Does color matrix transformation
16	MATRIX_EXT_MTX_	**Enables color transformation external coefficients or not**

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Bit(s)	Name	Description
	EN	For internal coefficient, use INT_MTX_SEL to select the pre-defined coefficients. 0: Use internal coefficients for color transformation 1: Use external coefficients for color transformation
12:0	OUTPUT_FRAME_WIDTH	**Width of output frame**

14008018 **DISP_RDMA_SIZE_CON_1** **RDMA Size Control 1** **000001E0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													**OUTPUT_FRAME_HEIGHT[19:16]**			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**OUTPUT_FRAME_HEIGHT[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0

Bit(s)	Name	Description
19:0	OUTPUT_FRAME_HEIGHT	Height of output frame

1400801C **DISP_RDMA_TARGET_LINE** **RDMA Target Line** **000000F0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													**TARGET_LINE[19:16]**			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TARGET_LINE[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bit(s)	Name	Description
19:0	TARGET_LINE	Target line number to interrupt

14008024 **DISP_RDMA_MEM_CON** **RDMA Memory Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MEM_MODE_HORI_BLOCK_NUM**															
Type	RW															
Reset	0	0	0	0	0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**MEM_MODE_UV_COSITE**	**MEM_MODE_UV_UPSAMP**				**MEM_MODE_INPUT_SW**	**MEM_MODE_INPUT_FORMAT**						**MEM_MODE_TILE_INTER**	**MEM_MODE_TILE_EN**

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				LE				AP							LACE	
Type			RW	RW				RW	RW						RW	RW
Reset			0	0				0	0	0	0	0			0	0

Bit(s)	Name	Description
31:24	MEM_MODE_HORI_BLOCK_NUM	**Block number in horizontal direction** Only for tile-based memory mode.
13	MEM_MODE_UV_COSITE	**If UV_UPSAMPLE is on, choose the pixel to be cosited or not.** 0: Non-cosited 1: Cosited
12	MEM_MODE_UV_UPSAMPLE	**If input format is YUV422, UV channel can be duplicated or averaged.** 0: Duplicated 1: Averaged
8	MEM_MODE_INPUT_SWAP	**Memory mode input format** The engine translates the memory data according to the format. For direct link mode, keep it to 0.
7:4	MEM_MODE_INPUT_FORMAT	**Memory mode input format** The engine translates the memory data according to the format. For direct link mode, keep it to 0. RGB565, RGB888, ARGB8888 and UYVY are supported.
1	MEM_MODE_TILE_INTERLACE	**If tile mode is enabled, the output frame cab be selected to be progressive or interlaced.** 0: Progressive 1: Interlace
0	MEM_MODE_TILE_EN	**When memory mode is enabled, tile-base memory allocation is supported.** 0: Raster scan mode 1: Tile mode

14008O2C **DISP_RDMA_MEM_SRC_PITCH** **RDMA Memory Mode Line Pitch** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEM_MODE_SRC_PITCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	MEM_MODE_SRC_PITCH	**Memory mode source image pitch** Refer to the "Memory Mode Control" section in Programming Guide.

14008030 **DISP_RDMA_MEM_GMC_SETTING_0** **RDMA Memory Mode GMC Setting 0** **10101010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PRE_ULTRA_THRESHOLD_HIGH_OFS								ULTRA_THRESHOLD_HIGH_OFS							
Type	RW								RW							

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Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRE_ULTRA_THRESHOLD_LOW_OFS								ULTRA_THRESHOLD_LOW							
Type	RW								RW							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:24	PRE_ULTRA_THRESHOLD_HIGH_OFS	Unit: 16 bytes
23:16	ULTRA_THRESHOLD_HIGH_OFS	
15:8	PRE_ULTRA_THRESHOLD_LOW_OFS	
7:0	ULTRA_THRESHOLD_LOW	Unit: 16 bytes

14008034 DISP_RDMA_MEM_SLOW_CON RDMA Memory Mode Slow Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEM_MODE_SLOW_COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MEM_MODE_SLOW_EN
Type																RW
Reset																0

Bit(s)	Name	Description
31:16	MEM_MODE_SLOW_COUNT	**GMC request slow-down counter** When MEM_MODE_SLOW_EN is 1, GMC request will not be continuous and the interval controlled by this register. Unit: Engine clock cycle time
0	MEM_MODE_SLOW_EN	**Enables GMC request slow-down** The bandwidth usage can be limited by this bit. 0: Disable slow-down 1: Enable slow-down

14008038 DISP_RDMA_MEM_GMC_SETTING_1 RDMA Memory Mode GMC Setting 1 00000010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ISSUE_REQ_THRESHOLD							
Type									RW							
Reset									0	0	0	1	0	0	0	0

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Bit(s)	Name	Description
7:0	ISSUE_REQ_THRESHOLD	

14008040 **DISP_RDMA_FIFO_CON** **RDMA FIFO Control** **01000010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO_UNDERFLOW_EN						FIFO_PSEUDO_SIZE									
Type	RW						RW									
Reset	0						0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							OUTPUT_VALID_FIFO_THRESHOLD									
Type							RW									
Reset							0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31	FIFO_UNDERFLOW_EN	**Enables FIFO underflow** If FIFO is exhausted, the data output will be stopped. If the downstream engines need the non-blocked data, set up this bit; it will keep the non-blocked output, but the data will not be correct. 0: Disable underflow 1: Enable underflow
25:16	FIFO_PSEUDO_SIZE	**FIFO pseudo size** Unit: 16 bytes. In this project, the recommended FIFO size is 480 (RDMA0, RDMA2) or 320 (RDMA1) depending on the SRAM size.
9:0	OUTPUT_VALID_FIFO_THRESHOLD	**Controls FIFO output threshold** Unit: 16 bytes. The register can hold the output data until the amount of data is over the threshold.

14008044 **DISP_RDMA_FIFO_LOG** **RDMA_FIFO_LOG** **000003FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RDMA_FIFO_LOG									
Type							RU									
Reset							1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
9:0	RDMA_FIFO_LOG	FIFO minimal depth

14008054 **DISP_RDMA_** **RDMA YUV to RGB Coefficient** **00000000**

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C00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C00												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C00	Color matrix coefficient

14008058 DISP_RDMA_C01 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C01												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C01	Color matrix coefficient

1400805C DISP_RDMA_C02 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C02												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C02	Color matrix coefficient

14008060 DISP_RDMA_C10 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C10												
Type				RW												

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Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C10	Color matrix coefficient

14008064 DISP_RDMA_C11 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C11												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C11	Color matrix coefficient

14008068 DISP_RDMA_C12 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C12												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C12	Color matrix coefficient

1400806C DISP_RDMA_C20 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C20												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C20	Color matrix coefficient

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14008070 **DISP_RDMA_C21** **RDMA YUV to RGB Coefficient** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C21												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C21	Color matrix coefficient

14008074 **DISP_RDMA_C22** **RDMA YUV to RGB Coefficient** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C22												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C22	Color matrix coefficient

14008078 **DISP_RDMA_PRE_ADD_0** **RDMA YUV to RGB Coefficient** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DISP_RDMA_PRE_ADD_0								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	DISP_RDMA_PRE_ADD_0	Color matrix coefficient

1400807C **DISP_RDMA_PRE_ADD_1** **RDMA YUV to RGB Coefficient** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DISP_RDMA_PRE_ADD_1								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	DISP_RDMA_PRE_ADD_1	Color matrix coefficient

14008080 DISP_RDMA_PRE_ADD_2 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DISP_RDMA_PRE_ADD_2								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	DISP_RDMA_PRE_ADD_2	Color matrix coefficient

14008084 DISP_RDMA_POST_ADD_0 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DISP_RDMA_POST_ADD_0								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	DISP_RDMA_POST_ADD_0	Color matrix coefficient

14008088 DISP_RDMA_POST_ADD_1 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DISP_RDMA_POST_ADD_1								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
8:0	DISP_RDMA_POST_ADD_1	Color matrix coefficient

1400808C **DISP_RDMA_POST_ADD_2** **RDMA YUV to RGB Coefficient** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DISP_RDMA_POST_ADD_2								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	DISP_RDMA_POST_ADD_2	Color matrix coefficient

14008090 **DISP_RDMA_DUMMY** **RDMA Dummy Register** **FFF00000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DISP_RDMA_DUMMY[31:16]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DISP_RDMA_DUMMY[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DISP_RDMA_DUMMY	Reserved

14008094 **DISP_RDMA_DEBUG_OUT_SEL** **RDMA Debug Output Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DISP_RDMA_DEBUG_OUT_SEL			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	DISP_RDMA_DEBUG	Reserved

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Bit(s)	Name	Description
	_OUT_SEL	

14008F00 **DISP_RDMA_MEM_START_ADDR** **RDMA Memory Mode Start Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEM_MODE_START_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEM_MODE_START_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MEM_MODE_START_ADDR	Memory mode source image start address

6.12.5 Programming Guide

The figure below shows the general programming sequence.

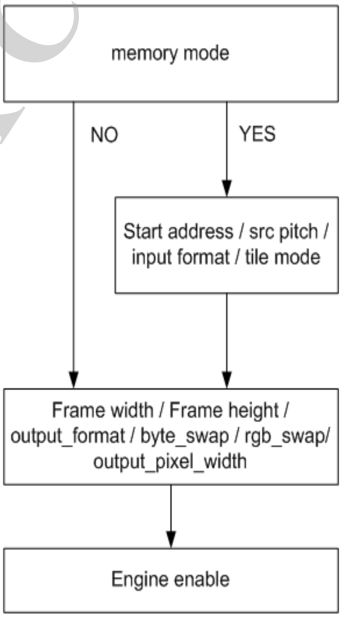

Figure 6-39. General programming sequence

The direct link mode can be easily configured by output frame width and height. On the other hand, the memory mode has several modes, which will be discussed in sub-sections.

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6.12.5.1 Memory Mode Control: Raster Scan Input, Progressive Output

1. Set 'MEM_MODE_START_ADDR' = Address of the first pixel.
2. Set 'MEM_MODE_SRC_PITCH' = Width of the source frame.

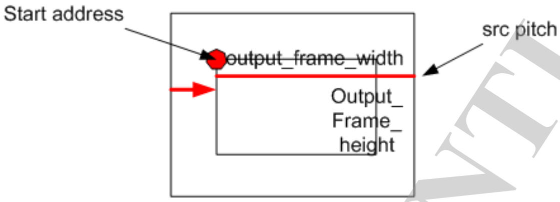

Figure 6-40. Basic memory mode configuration

6.12.5.2 Memory Mode Control: Raster Scan Input, Interlace Output

1. Set 'MEM_MODE_START_ADDR' = Address of the first pixel.
2. Set 'MEM_MODE_SRC_PITCH' = ***Double*** of the width of the source frame.

6.12.5.3 YUV to RGB Transfer Formula

$$\begin{pmatrix} Y_out \\ U_out \\ V_out \end{pmatrix} = \begin{pmatrix} C00 & C01 & C02 \\ C10 & C11 & C12 \\ C20 & C21 & C22 \end{pmatrix} \times \begin{pmatrix} Y_input + pre_add_0 \\ U_input + pre_add_1 \\ V_input + pre_add_2 \end{pmatrix} + \begin{pmatrix} post_add_0 \\ post_add_1 \\ post_add_2 \end{pmatrix}$$

Figure 6-41. Programmable color matrix

6.12.5.4 Byte Swap/RGB Swap

Set up the corresponding registers according to the data format on the memory.

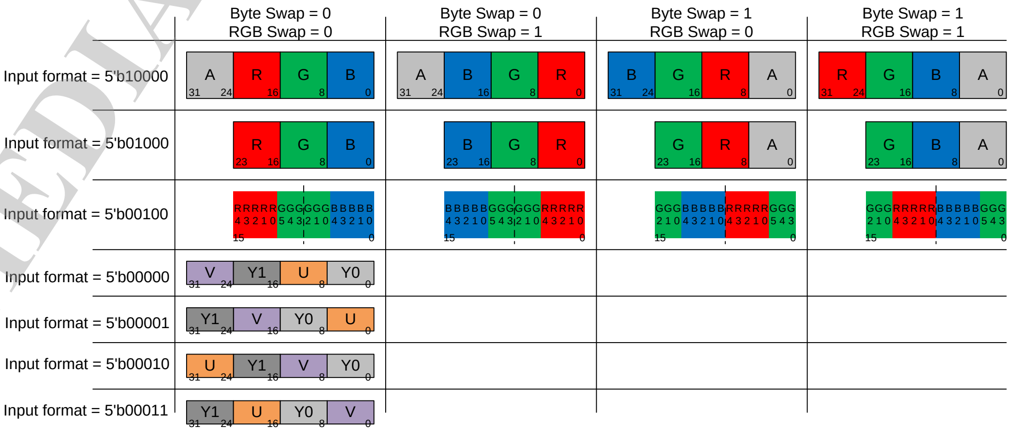

Figure 6-42. Byte/RGB swap

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6.13 DISP_WDMA

6.13.1 Introduction

MDP_WDMA and DISP_WDMA have the same hardware architecture but slightly differ in SRAM size, which influences the line-width support and outstanding ability. WDMA does the job of DMA writing out the data in display/MDP pipeline into DRAM. In the following sections, WDMA is called DISP_WDMA.

6.13.2 Features

- Dither
- Programmable parameter color transform
- Input color format YUV444/RGB888
- Output format RGB565/RGB888/ARGB8888/UYVY/YV12/NV12/NV21
- 3-tap filter in horizontal and 2-tap filter in vertical for YUV420 down sample
- Byte swap/color swap/UV swap functions

6.13.3 Block Diagram

DISP_WDMA has a 256x128 two-port SRAM for DMA FIFO. One 320x64 single-port SRAM is for vertical filtering line_buffer (2560 pixels). For line-width larger than 2560, YUV420 vertical down sample must be drop-pixel scheme.

MDP_WDMA has a 128x128 two-port SRAM for DMA FIFO. One 64x64 single-port SRAM is for vertical filtering line_buffer (512 pixels). For line-width larger than 512, YUV420 vertical down sample must be drop-pixel scheme.

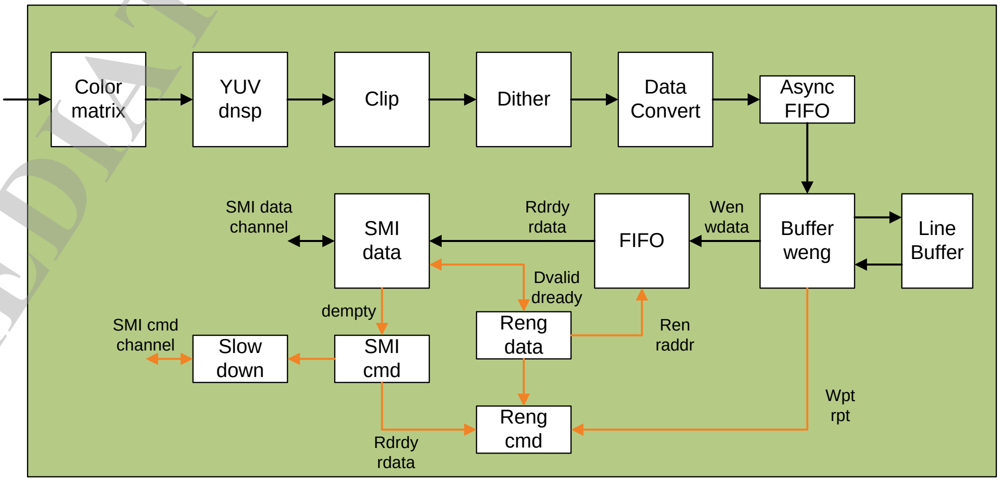

Figure 6-43. Block diagram of DISP_WDMA

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6.13.4 Register Definition

Module name:

MDP_WDMA Base address: (+14004000h)

DISP_WDMA0 Base address: (+1400b000h)

DISP_WDMA1 Base address: (+14018000h)

Address	Name	Width	Register Function
00000000	WDMA_INTEN	32	**WDMA Interrupt Enable** Enables interrupt
00000004	WDMA_INTSTA	32	**WDMA Interrupt Status** Interrupt status
00000008	WDMA_EN	32	WDMA Enable
0000000C	WDMA_RST	32	**WDMA Reset** Controls software reset
00000010	WDMA_SMI_CON	32	**WDMA SMI Control** Controls SMI
00000014	WDMA_CFG	32	**WDMA Config Register** Configures WDMA
00000018	WDMA_SRC_SIZE	32	**WDMA Source Size Register** Setting of source width and height
0000001C	WDMA_CLIP_SIZE	32	**WDMA Clip Size Register** Setting of clip width and height
00000020	WDMA_CLIP_COORD	32	**WDMA Clip Coordinate Register** Setting of clip coordinate
00000028	WDMA_DST_W_IN_BYTE	32	**WDMA Destination Width in Byte** Setting of destination width in byte
0000002C	WDMA_ALPHA	32	**WDMA Alpha** Setting of alpha value
00000038	WDMA_BUF_CON1	32	**WDMA Buffer Control 1** Buffer Control 1
0000003C	WDMA_BUF_CON2	32	**WDMA Buffer Control 2** Buffer Control 2
00000040	WDMA_C00	32	**WDMA Matrix Coefficient** Setting of matrix coefficient
00000044	WDMA_C02	32	**WDMA Matrix Coefficient** Setting of matrix coefficient
00000048	WDMA_C10	32	**WDMA Matrix Coefficient** Setting of matrix coefficient
0000004C	WDMA_C12	32	**WDMA Matrix Coefficient** Setting of matrix coefficient
00000050	WDMA_C20	32	**WDMA Matrix Coefficient** Setting of matrix coefficient
00000054	WDMA_C22	32	**WDMA Matrix Coefficient** Setting of matrix coefficient
00000058	WDMA_PRE_ADD0	32	**WDMA Matrix Coefficient** Setting of matrix coefficient
0000005C	WDMA_PRE_ADD2	32	**WDMA Matrix Coefficient** Setting of matrix coefficient
00000060	WDMA_POST_A	32	**WDMA Matrix Coefficient**

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Address	Name	Width	Register Function
	DD0		Setting of matrix coefficient
00000064	WDMA_POST_ADD2	32	**WDMA Matrix Coefficient** Setting of matrix coefficient
00000078	WDMA_DST_UV_PITCH	32	**WDMA UV Destination Width in Byte** WDMA UV destination width in byte
00000080	WDMA_DST_ADDR_OFFSET0	32	**WDMA Destination Address Offset 0** WDMA destination address offset 0
00000084	WDMA_DST_ADDR_OFFSET1	32	**WDMA Destination Address Offset 1** WDMA destination address offset 1
00000088	WDMA_DST_ADDR_OFFSET2	32	**WDMA Destination Address Offset 2** WDMA destination address offset 2
00000090	PROC_TRACK_CON_0	32	**DMA Processing Tracking Control 0** Controls the parameters of the DMA processing tracking
00000094	PROC_TRACK_CON_1	32	**DMA Processing Tracking Control 1** Controls the parameters of the DMA processing tracking
00000098	PROC_TRACK_CON_2	32	**DMA Processing Tracking Control 2** Controls the parameters of the DMA processing tracking
000000A0	WDMA_FLOW_CTRL_DBG	32	**WDMA Debug Port of flow_ctrl** Debugging status of flow_ctrl
000000A4	WDMA_EXEC_DBG	32	**WDMA Debug Port of Exec Count** Debugging status of exec count
000000A8	WDMA_CT_DBG	32	**WDMA Debug Port of Input Counter** Debugging status of input counter
000000AC	WDMA_SMI_TRAFFIC_DBG	32	**WDMA Debug Port for SMI Traffic** Debugging status between SMI and WDMA
000000B0	WDMA_PROC_TRACK_DBG_0	32	**WDMA Debug Port for Process Track 0** Debugging status of process tracking
000000B4	WDMA_PROC_TRACK_DBG_1	32	**WDMA Debug Port for Process Track 1** Debugging status of process tracking
000000B8	WDMA_DEBUG	32	**WDMA Debug Port** Debugging status
00000100	WDMA_DUMMY	32	**WDMA Dummy Register** WDMA dummy register
00000E00	WDMA_DITHER_0	32	WDMA Dithering Control Register 0
00000E14	WDMA_DITHER_5	32	WDMA Dithering Control Register 5
00000E18	WDMA_DITHER_6	32	WDMA Dithering Control Register 6
00000E1C	WDMA_DITHER_7	32	WDMA Dithering Control Register 7
00000E20	WDMA_DITHER_8	32	WDMA Dithering Control Register 8
00000E24	WDMA_DITHER_9	32	WDMA Dithering Control Register 9
00000E28	WDMA_DITHER_10	32	WDMA Dithering Control Register 10
00000E2C	WDMA_DITHER_11	32	WDMA Dithering Control Register 11
00000E30	WDMA_DITHER_12	32	WDMA Dithering Control Register 12
00000E34	WDMA_DITHER_13	32	WDMA Dithering Control Register 13

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Address	Name	Width	Register Function
00000E38	WDMA_DITHER_14	32	WDMA Dithering Control Register 14
00000E3C	WDMA_DITHER_15	32	WDMA Dithering Control Register 15
00000E40	WDMA_DITHER_16	32	WDMA Dithering Control Register 16
00000E44	WDMA_DITHER_17	32	WDMA Dithering Control Register 17
00000F00	WDMA_DST_ADDR0	32	**WDMA Destination Address 0** Setting of destination address 0
00000F04	WDMA_DST_ADDR1	32	**WDMA Destination Address 1** WDMA U destination address 1
00000F08	WDMA_DST_ADDR2	32	**WDMA Destination Address 2** WDMA V destination address 2

00000000 WDMA_INT_EN WDMA Interrupt Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name															FUE	FCE
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	FUE	Frame_Underrun	**Enables frame underrun interrupt** 0: Disable interrupt 1: Enable interrupt
0	FCE	Frame_Complete	**Enables frame completed interrupt** 0: Disable interrupt 1: Enable interrupt

00000004 WDMA_INT_STA WDMA Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name															FU	FC
Type															A1	A1
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	FU	Frame_Underrun	**Incompletes one frame when WDMA receives EOF** SW writes this bit to clear IRQ. 0: WDMA idle or busy 1: WDMA incompletes one frame

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Bit(s)	Mnemonic	Name	Description
0	FC	Frame_Complete	**Completes one frame before WDMA receives EOF** SW writes this bit to clear IRQ. 0: WDMA idle or busy 1: WDMA completes one frame

00000008 **WDMA_EN** **WDMA Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	EN	Enable	**Enables WDMA or not** 0: Disable WDMA 1: Enable WDMA

0000000C **WDMA_RST** **WDMA Reset** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RST
Type																A0
Reset																0

Bit(s)	Mnemonic	Name	Description
0	RST	Soft_Reset	**Soft reset to WDMA** Write this bit to trigger soft reset. WDMA will reset itself when bus transaction is done. SW must keep polling bit 0 of register WDMA_FLOW_CTRL_DBG until it is 1 to determine if the reset flow is done. 0: Write: No effect; Read: Reset is done . 1: Write: Trigger reset; Read: Reset is on-going.

00000010 **WDMA_SMI_CON** **WDMA SMI Control** **02240007**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					V_NUM				U_NUM				Y_NUM			
Type					RW				RW				RW			
Reset					0	0	1	0	0	0	1	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SC								SL			SE	TH			

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Type	RW								RW			RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
27:24	**V_NUM**	SMI_V_REPEAT_NUM	**Number of continuous V SMI commands** Only takes effects when out_format=YV12/NV12/NV21.
23:20	**U_NUM**	SMI_U_REPEAT_NUM	**Number of continuous U SMI commands** Only takes effects when out_format=YV12/NV12/NV21.
19:16	**Y_NUM**	SMI_Y_REPEAT_NUM	**Number of continuous Y SMI commands** Only takes effects when out_format=YV12/NV12/NV21.
15:8	**SC**	Slow_Count	**Slow-down counter of each write request** The actual slow-down count of each request is (slow_count*slow_level).
7:5	**SL**	Slow_Level	**Slow-down level of each write request** 0: slow_level=1 1: slow_level=2 2: slow_level=4 4: slow_level=8
4	**SE**	Slow_Enable	**Enables slow-down of each write request or not** 0: Disable slow-down 1: Enable slow-down
3:0	**TH**	Threshold	**Restricts max. burst length of each write request** Max. burst length: Threshold + 1

00000014 **WDMA_CFG** **WDMA Config Register** **03020000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DEBUG_SEL**				**INT_MTX_SEL**										**UNICON**	**SWAP**
Type	RW				RW										RW	RW
Reset	0	0	0	0	0	0	1	1							1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DNSP_SEL**		**EXT_MTX_EN**	**V_AVG**	**CT_EN**	**UVS**	**RGBS**	**BYTES**	**OF**							
Type	RW		RW	RW	RW	RW	RW	RW	RW							
Reset	0		0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:28	**DEBUG_SEL**	DEBUG_SEL	**For WDMA debugging selection**
27:24	**INT_MTX_SEL**	INT_MTX_SEL	**Selects pre-defined color transformation coefficient** 4'b0000: RGB to JPEG 4'b0010: RGB to BT601 4'b0011: RGB to BT709 4'b0100: JPEG to RGB 4'b0110: BT601 to RGB 4'b0111: BT709 to RGB 4'b1000: JPEG to BT601 4'b1001: JPEG to BT709 4'b1010: BT601 to JPEG 4'b1011: BT709 to JPEG 4'b1100: BT709 to BT601

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Bit(s)	Mnemonic	Name	Description
			4'b1101: BT601 to BT709
17	**UNICON**	UNI_CONFIG	**Uses uniform config or not** Do not modify this bit. 0: Disable uniform config 1: Enable uniform config
16	**SWAP**	SWAP	**Enables swap function to translate the output data format** Translated output data format: RGB565 -> BGR565 RGB888 -> BGR888 RGBA8888 -> BGRA8888 ARGB8888 -> ABGR8888 UYVY -> VYUY YUY2 -> YVYU IYUV -> YV12 NV12 -> NV21 0: Disable swap 1: Enable swap
15	**DNSP_SEL**	DNSP_SEL	**Selects YUV444 to YUV422 mode** 0: Drop odd pixel U/V 1: Apply [1 2 1] filter for U/V
13	**EXT_MTX_EN**	EXT_MTX_EN	**Enables color transformation external coefficients or not** For internal coefficient, use INT_MTX_SEL to select the pre-defined coefficients. For external coefficient, use register WDMA_C00 -> WDMA_POST_ADD. 0: Use internal coefficients for color transformation 1: Use External coefficients for color transformation
12	**V_AVG**	VERTICAL_AVG	**Enables vertical average or not** 0: Drop odd line pixels 1: Average in vertical while YUV444->YUV420
11	**CT_EN**	CT_EN	**Enables color transformation matrix or not** 0: Bypass color transformation matrix 1: Do color transformation
10	**UVS**	UV_SWAP	**Enables uv_swap or not** If the output format is UYVY (y1 v0 y0 u0), it will become (y1 u0 y0 v0) after UV swap. It takes no effect only when legacy mode and the output format is in RGB domain. 0: Disable UV swap 1: Enable UV swap
9	**RGBS**	RGB_SWAP	**Enables rgb_swap or not** If the output format is ARGB, it will become ABGR after RGB swap. It takes no effect only when legacy mode and the output format is in YUV domain. 0: Disable RGB swap 1: Enable RGB swap
8	**BYTES**	BYTE_SWAP	**Enables byte_swap or not** Takes no effect when output format is RGB565 or RGB888. If the output format is ARGB, it will become BGRA after byte swap. If the output format is UYVY(y1 v0 y0 u0), it will become (v0 y1 u0 y0) after byte swap. Only works in legacy mode. 0: Disable byte swap 1: Enable byte swap
7:4	**OF**	Out_Format	**Specifies output format of WDMA** 0: RGB565 1: RGB888 2: BGRA8888 3: ARGB8888

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Bit(s)	Mnemonic	Name	Description
			4: UYVY 5: YUY2 7: Y-only 8: IYUV (I420) 12: NV12

00000018 WDMA_SRC_SIZE WDMA Source Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			HGT													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			WTH													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:16	HGT	Height	**Source height in pixels** Range: 0 ~ 2,047
13:0	WTH	Width	**Source width in pixels** Range: 0 ~ 2,047

0000001C WDMA_CLIP_SIZE WDMA Clip Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			HGT													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			WTH													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:16	HGT	Height	**Clip height in pixels** Range: 0 ~ 2,047
13:0	WTH	Width	**Clip width in pixels** Range: 0 ~ 2,047

00000020 WDMA_CLIP_COORD WDMA Clip Coordinate Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			CY													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			CX													

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Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:16	**CY**	Y_coord	**Y coordinate in pixels of clipped image** Range: 0 ~ 2,047
13:0	**CX**	X_coord	**X coordinate in pixels of clipped image** Range: 0 ~ 2,047

00000020 WDMA_CLIP_COORD WDMA Clip Coordinate Register 00000000

00000028 WDMA_DST_W_IN_BYTE WDMA Destination Width in Byte 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DWB															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**DWB**	Dst_W_in_Byte	**Destination width in bytes of each scan line** It is width*bpp. bpp: RGB565 -> 2, RGB888->3, ARGB->4, YV12->1, NV12->1, NV21->1

0000002C WDMA_ALPHA WDMA Alpha 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ASEL															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									A							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**ASEL**	A_Sel	**Selects A source from pixel alpha or specified alpha** 0: Select pixel alpha from OVL 1: Select specified A value
7:0	**A**	A_Value	**Specified A value**

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00000038 WDMA_BUF_CON1 WDMA Buffer Control 1 10100100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	UE	PUE		FEU				REQ_TH								
Type	RW	RW		RW				RW								
Reset	0	0		1				0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								FIFO_SIZE								
Type								RW								
Reset								1	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	UE	Ultra_Enable	**Enables ultra high request not**
30	PUE	Pre_Ultra_Enable	**Enables pre-ultra high request**
28	FEU	Frame_End_Ultra	**WDMA issues ultra high command at the end of the frame.**
24:16	REQ_TH	issue_req_th	**Threshold of data amount to release data from WDMA** WDMA starts sending data only when data amount in FIFO is larger than the set value.
8:0	FIFO_SIZE	fifo_pseudo_size	**Actually used FIFO entries** Keep it at default value. MDP_WDMA: 128. DISP_WDMA: 256.

0000003C WDMA_BUF_CON2 WDMA Buffer Control 2 10101010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	UL_H_OFFSET								PUL_H_OFFSET							
Type	RW								RW							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UL_L_OFFSET								PUL_L_OFFSET							
Type	RW								RW							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	UL_H_OFFSET	ultra_th_high_ofs	**UH (ultra high threshold) = PUH + ultra_th_high_ofs** If FIFO size of WMDA > UH, WDMA will assert ultra high request.
23:16	PUL_H_OFFSET	pre_ultra_th_high_ofs	**PUH (pre_ultra high threshold) = UL + pre_ultra_th_high_ofs** If FIFO size of WMDA > PUH, WDMA will assert pre-ultra high request.
15:8	UL_L_OFFSET	ultra_th_low_ofs	**UL (ultra low threshold) = PUL + ultra_th_low_ofs** If FIFO size of WMDA < UL, WDMA will de-assert ultra high request.
7:0	PUL_L_OFFSET	pre_ultra_th_low	**PUL (pre_ultra low threshold) = pre_ultra_th_low** If FIFO size of WMDA < PUL, WDMA will de-assert pre-ultra high request.

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00000040 WDMA_C00 WDMA Matrix Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										C01						
Type										RW						
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										C00						
Type										RW						
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**C01**	C01	Matrix coefficient of C01
12:0	**C00**	C00	Matrix coefficient of C00

00000044 WDMA_C02 WDMA Matrix Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										C02						
Type										RW						
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0	**C02**	C02	Matrix coefficient of C02

00000048 WDMA_C10 WDMA Matrix Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										C11						
Type										RW						
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										C10						
Type										RW						
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**C11**	C11	Matrix coefficient of C11
12:0	**C10**	C10	Matrix coefficient of C10

0000004C WDMA_C12 WDMA Matrix Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**C12**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0	**C12**	C12	Matrix coefficient of C12

00000050 WDMA_C20 WDMA Matrix Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**C21**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**C20**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**C21**	C21	Matrix coefficient of C21
12:0	**C20**	C20	Matrix coefficient of C20

00000054 WDMA_C22 WDMA Matrix Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**C22**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0	**C22**	C22	Matrix coefficient of C22

00000058 WDMA_PRE_ADD0 WDMA Matrix Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								**PREADD1**								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**PREADD0**								
Type								RW								

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Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16	**PREADD1**	PRE_ADD_1	Matrix coefficient of pre add1
8:0	**PREADD0**	PRE_ADD_0	Matrix coefficient of pre add0

0000005C **WDMA_PRE_ADD2** **WDMA Matrix Coefficient** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**PREADD2**								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0	**PREADD2**	PRE_ADD_2	Matrix coefficient of pre add2

00000060 **WDMA_POST_ADD0** **WDMA Matrix Coefficient** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								**POSTADD1**								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**POSTADD0**								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16	**POSTADD1**	POST_ADD_1	Matrix coefficient of post add1
8:0	**POSTADD0**	POST_ADD_0	Matrix coefficient of post add0

00000064 **WDMA_POST_ADD2** **WDMA Matrix Coefficient** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**POSTADD2**								
Type								RW								

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Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0	**POSTAD D2**	POST_ADD_2	Matrix coefficient of post add2

00000078 **WDMA_DST_UV_PITCH** WDMA UV Destination Width in Byte 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UV_Dst_W_in_Byte															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**UV_Dst_W_in_Byte**	UV_Dst_W_in_Byte	UV pitch for YV12/NV12/NV21 output

00000080 **WDMA_DST_ADDR_OFFSET0** WDMA Destination Address Offset 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					Address_offset0[27:16]											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Address_offset0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:0	**Address_offset0**	WDMA_Destination_Address_offset0	**WDMA destination address offset 0** Final destination address = DST_ADDR + DST_ADDR_OFFSET

00000084 **WDMA_DST_ADDR_OFFSET1** WDMA Destination Address Offset 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					Address_offset1[27:16]											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Address_offset1[15:0]															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:0	**Address_offset1**	WDMA_Destination_Address_offset1	**WDMA destination address offset 1** U address offset for YV12 output; UV address offset for NV12/NV21 output

00000088 **WDMA_DST_ADDR_OFFSET2** **WDMA Destination Address Offset 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					Address_offset2[27:16]											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Address_offset2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:0	**Address_offset2**	WDMA_Destination_Address_offset2	**WDMA destination address offset 2** V address offset for YV12 output

00000090 **PROC_TRACK_CON_0** **DMA Processing Tracking Control 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		IGNORE_INIT_LATENCY	STOP_GREQ_EN	PROC_PRE_ULTRA_EN												
Type		RW	RW	RW												
Reset		0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TRACK_WINDOW											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30		IGNORE_INIT_LATENCY	**Ignores initial latency from SOF to the first proc_one**
29		STOP_GREQ_EN	**Enables stop_greq of the process tracking**
28		PROC_PRE_ULTRA_EN	**Enables pre_ultra of process tracking** If this bit is enabled, pre_ultra will be controlled by process tracking unit.
11:0		TRACK_WINDOW	**Tracking window** Unit: bclk_ck cycle

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00000094	PROC_TRACK_CON_1	DMA Processing Tracking Control 1	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									TARGET_CNT[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TARGET_CNT[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		TARGET_CNT	**Targets process count during a TRACK_WINDOW** It is s a 16.8 fix point number.

00000098	PROC_TRACK_CON_2	DMA Processing Tracking Control 2	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									STOP_CNT[23:16]							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STOP_CNT[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		STOP_CNT	If processing counter > STOP_CNT, stops issuing greq

000000A0	WDMA_FLOW_CTRL_DBG	WDMA Debug Port of flow_ctrl	00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_IN_REQ	WDMA_IN_ACK	WDMA_GREQ	WDMA_FIFO_FULL			WDMA_STATE									
Type	RU	RU	RU	RU			RU									
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
15	**WDMA_IN_REQ**	WDMA_IN_REQ	**WDMA input request** IN_REQ=1 means the previous engine is sending data to WDMA and waiting for response from WDMA.
14	**WDMA_I**	WDMA_IN_ACK	**Acknowledges WDMA input**

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Bit(s)	Mnemonic	Name	Description
	N_ACK		IN_ACK=1 means WDMA is ready for the next pixel and is waiting for the previous engine to send the next pixel.
13	WDMA_GREQ	WDMA_GREQ	**WDMA SMI request** GREQ=1 means that WDMA is sending out an SMI request but no response from LARB.
12	WDMA_FIFO_FULL	WDMA_FIFO_FULL	**WDMA FIFO status is full or not**
9:0	WDMA_STATE	WDMA_STATE	**WDMA state machine** Read the current status of WDMA here. 00_0000_0001: Idle state 00_0000_0010: Clear state 00_0000_0100: Prepare state 1 00_0000_1000: Prepare state 2 00_0001_0000: Data transmit state 00_0010_0000: EOF prepare state 00_0100_0000: SW reset prepare state 00_1000_0000: EOF wait idle state 01_0000_0000: SW reset wait idle state 10_0000_0000: Frame completed state

000000A4 **WDMA_EXEC_DBG** **WDMA Debug Port of Exec Count** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CDBG					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											EDBG					
Type											RU					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:16	CDBG	WDMA_FRAME_COMPLETE_CNT	**Debugging status of complete cnt** When WDMA completes one frame (not SW reset or EOF reset), this counter will increase.
5:0	EDBG	WDMA_FRAME_RUN_CNT	**Debugging status of exec cnt** When WDMA receives SOF signal (Start Of Frame) from the MUTEX, this counter will increase.

000000A8 **WDMA_CT_DBG** **WDMA Debug Port of Input Counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			WDMA_INPUT_CNT_Y													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			WDMA_INPUT_CNT_X													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
29:16	**WDMA_INPUT_CNT_Y**	WDMA_INPUT_CNT_Y	**WDMA input counter in Y axis**
13:0	**WDMA_INPUT_CNT_X**	WDMA_INPUT_CNT_X	**WDMA input counter in X axis** How many pixels in a line are received by the WDMA. The total amount of received pixels is WDMA_INPUT_CNT_Y*SRC_W + WDMA_INPUT_CNT_X.

000000AC **WDMA_SMI_TRAFFIC_DBG** **WDMA Debug Port for SMI Traffic** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_SMI_STATUS[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_SMI_STATUS[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**WDMA_SMI_STATUS**	WDMA_SMI_TRAFFIC	**Traffic status between WDMA and SMI** This counter should be 0 when WDMA is being SW reset.

000000B0 **WDMA_PROC_TRACK_DBG_0** **WDMA Debug Port for Process Track 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_PROC_TRACK_MAX[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_PROC_TRACK_MAX[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**WDMA_PROC_TRACK_MAX**	WDMA_PROC_CNT_MAX	**Process tracking status counter max. value** Write this register to clear the counter.

000000B4 **WDMA_PROC_TRACK_DBG_1** **WDMA Debug Port for Process Track 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_PROC_TRACK_MIN[31:16]															

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Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**WDMA_PROC_TRACK_MIN[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**WDMA_PROC_TRACK_MIN**	WDMA_PROC_CNT_MIN	**Process tracking status counter min. value** Write this register to clear the counter.

000000B8 **WDMA_DEBUG** **WDMA Debug Port** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CDBG[31:16]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CDBG[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CDBG**	WDMA_STA_DEBUG	Trivil debugging status of WDMA

00000100 **WDMA_DUMMY** **WDMA Dummy Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DUMMY[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DUMMY[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DUMMY**	WDMA_DUMMY	WDMA dummy register

00000E00 **WDMA_DITHER_0** **WDMA Dithering Control Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								**crc_clr**				**crc_start**				**crc_cen**
Type								RW				RW				RW
Reset								0				0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	frame_done_del											out_sel				start
Type	RW											RW				RW
Reset	0	0	0	0	0	0	0	0				0				0

Bit(s)	Mnemonic	Name	Description
24		crc_clr	Write 1 to clear CRC result
20		crc_start	Write 1 to start CRC counting
16		crc_cen	0: Turn off CRC engine CG 1: Turn on CRC engine CG
15:8		frame_done_del	Frame done return delay
4		out_sel	0: Through dither 1: Bypass dither
0		start	0: No dither 1: Start dither engine

00000E14 WDMA_DITHER_5 WDMA Dithering Control Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	w_demo															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		w_demo	Short line length

00000E18 WDMA_DITHER_6 WDMA Dithering Control Register 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																wrap_mode
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	left_en		fphase_r	fphase_en			fphase						round_en	rdither_en	lfsr_en	edither_en
Type	RW		RW	RW			RW						RW	RW	RW	RW
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16		wrap_mode	**Enables rounding for dithering function** When rounding method is used, both running order and error dispersion cannot be used.
15:14		left_en	**Enables left part of screen dither**

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Bit(s)	Mnemonic	Name	Description
			0: Dither runs at full screen. 1: Dither runs at left part of screen.
13		fphase_r	**Dither SubPixel addend**
12		fphase_en	**Enables running order dithering frame phase control**
9:4		fphase	**Running order dithering frame phase increment** *Note:* *1. If ROUND_EN = 1, the output will only be rounding (no matter what RDITHER_EN and EDITHER_EN settings are).* *2. RDITHER_EN and EDITHER_EN can work together.*
3		round_en	**Enables rounding for dithering function** When rounding method is used, both running order and error dispersion cannot be used.
2		rdither_en	**Enables running order dithering** Running order dithering must be set when ROUND_EN is set to 0. Running order dithering can run with error dispersion when EDOTHER_EN is set to 1.
1		lfsr_en	**Enables LFSR-type dithering**
0		edither_en	**Enables error dispersion dithering** Error dispersion dithering must be set when ROUND_EN is set to 0. Running order dithering can run with error dispersion when RDITHER_EN is set to 1.

00000E1C **WDMA_DITHER_7** **WDMA Dithering Control Register 7** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							drmod_b				drmod_g				drmod_r	
Type							RW				RW				RW	
Reset							0	0			0	0			0	0

Bit(s)	Mnemonic	Name	Description
9:8		drmod_b	**Selects dither mode** 0: No dither 1: 12-bit dither to 10-bit 2: 12-bit dither to 8-bit 3: 12-bit dither to 6-bit
5:4		drmod_g	**Selects dither mode** 0: No dither 1: 12-bit dither to 10-bit 2: 12-bit dither to 8-bit 3: 12-bit dither to 6-bit
1:0		drmod_r	**Selects dither mode** 0: No dither 1: 12-bit dither to 10-bit 2: 12-bit dither to 8-bit 3: 12-bit dither to 6-bit

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00000E20 **WDMA_DITHER_8** **WDMA Dithering Control Register 8** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ink_data_r									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ink
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
25:16		ink_data_r	Ink data for R
0		ink	Enables ink

00000E24 **WDMA_DITHER_9** **WDMA Dithering Control Register 9** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ink_data_b									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							ink_data_g									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
25:16		ink_data_b	Ink data for B
9:0		ink_data_g	Ink data for G

00000E28 **WDMA_DITHER_10** **WDMA Dithering Control Register 10** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						fphase_bit					fphase_sel				fphase_ctrl	
Type						RW					RW				RW	
Reset						0	0	0			0	0			0	0

Bit(s)	Mnemonic	Name	Description
10:8		fphase_bit	**fphase_bit XOR bus number** *Note: This function checks reg_fphase_sel.* Only 0, 1, 2, 4 and 6 are available. 0: No effect on fphase (XOR disabled)
5:4		fphase_sel	**fphase XOR function: fphase do self bit-wise xor** *Note: This function checks reg_fphase_sel. Only bit 2, bit 4 and bit 6 are available.* 0: Disable fphase XOR

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Bit(s)	Mnemonic	Name	Description
			1: Effect fphase[0]~[1] based on the value of reg_fphase_sel is 1 or 2 2: Effect fphase[0]~[3] based on the value of reg_fphase_sel is 1, 2 or 4 3: Effect fphase[0]~[5] based on the value of reg_fphase_sel is 1, 2, 4 or 6
1:0		fphase_ctrl	**Selects fphase range to add with rdither table** 00: 0~63 01: 0~16 10: 0~3

00000E2C **WDMA_DITHER_11** **WDMA Dithering Control Register 11** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			sub_b				sub_g				sub_r					subpix_en
Type			RW				RW				RW					RW
Reset			0	0			0	0			0	0				0

Bit(s)	Mnemonic	Name	Description
13:12		sub_b	**Dither SubPixel addend**
9:8		sub_g	**Dither SubPixel addend**
5:4		sub_r	**Dither SubPixel addend**
0		subpix_en	**Enables sub pix dither mode** 0: Pix dither mode 1: Sub pix dither mode

00000E30 **WDMA_DITHER_12** **WDMA Dithering Control Register 12** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	h_active															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											table_en					lsb_off
Type											RW					RW
Reset											0	0				0

Bit(s)	Mnemonic	Name	Description
31:16		h_active	**Active region of dither IP**
5:4		table_en	**Active bit of magic table for running order** 01: Phase active in bit 3 ~ bit 0 10: Phase active in bit 1 ~ bit 0 Others: Phase active in bit 5 ~ bit 0
0		lsb_off	**Turns off LSB for dither function**

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00000E34	WDMA_DITHER_13	WDMA Dithering Control Register 13	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						rshift_b				rshift_g				rshift_r		
Type						RW				RW				RW		
Reset						0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
10:8		rshift_b	B right shift position after IP output
6:4		rshift_g	G right shift position after IP output
2:0		rshift_r	R right shift position after IP output

00000E38	WDMA_DITHER_14	WDMA Dithering Control Register 14	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							debug_mode			diff_shift						testpin_en
Type							RW			RW						RW
Reset							0	0		0	0	0				0

Bit(s)	Mnemonic	Name	Description
9:8		debug_mode	1: Enables debugging mode
6:4		diff_shift	Debugging mode difference shift positions
0		testpin_en	Enables testpin input

00000E3C	WDMA_DITHER_15	WDMA Dithering Control Register 15	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		lsb_err_shift_r				ovflw_bit_r				add_lshift_r				input_rshift_r		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																new_bit_mode
Type																RW
Reset																0

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Bit(s)	Mnemonic	Name	Description
30:28		lsb_err_shift_r	RED LSB error bit select
26:24		ovflw_bit_r	RED overflow bit select
22:20		add_lshift_r	RED addend left shift bits
18:16		input_rshift_r	RED input right shift bits
0		new_bit_mode	1: Enables modified test algorithm

00000E40 WDMA_DITHER_16 WDMA Dithering Control Register 16 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		lsb_err_shift_b				ovflw_bit_b				add_lshift_b				input_rshift_b		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name		lsb_err_shift_g				ovflw_bit_g				add_lshift_g				input_rshift_g		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		lsb_err_shift_b	Selects GREEN LSB error bit
26:24		ovflw_bit_b	Selects GREEN overflow bit
22:20		add_lshift_b	GREEN addend left shift bits
18:16		input_rshift_b	GREEN input right shift bits
14:12		lsb_err_shift_g	Selects BLUE LSB error bit
10:8		ovflw_bit_g	Selects BLUE overflow bit
6:4		add_lshift_g	BLUE addend left shift bits
2:0		input_rshift_g	BLUE input right shift bits

00000E44 WDMA_DITHER_17 WDMA Dithering Control Register 17 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																crc_rdy
Type																RO
Reset																0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	crc_out															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16		crc_rdy	CRC ready
15:0		crc_out	CRC result

00000F00 WDMA_DST_ADDR0 WDMA Destination Address 0 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADDR0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADDR0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ADDR0**	Address0	**Destination address of image** There is no alignment restriction. For YV12/NV12/NV21 data format, address 0 means the destination of Y.

00000F04 **WDMA_DST_ADDR1** **WDMA Destination Address 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Address1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Address1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**Address1**	Address1	U address for YV12 output; UV address for NV12/NV21 output

00000F08 **WDMA_DST_ADDR2** **WDMA Destination Address 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Address2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Address2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**Address2**	Address2	V address for YV12 output

6.13.5 Programming Guide

The fundamental key parts are base address/input output format/data strides in memory. If color transform is needed, color transform matrix will also be needed. Other setting such as dither/filter are optional.

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MUST program

WDMA_CFG
WDMA_SRC_SIZE
WDMA_CLIP_SIZE
WDMA_CLIP_COORD
WDMA_DST_ADDR0
WDMA_DST_W_IN_BYTE
WDMA_DST_ADDR1
WDMA_DST_ADDR2
WDMA_DST_UV_PITCH
WDMA_DST_ADDR_OFFSET0
WDMA_DST_ADDR_OFFSET1
WDMA_DST_ADDR_OFFSET2

The read result of WDMA_CT_DBG means the input counter of the WDMA.
The MSB part is line counter and the LSB part is pixel counter.
This can be used as debugging register.

The read result of WDMA_FLOW_CTRL_DBG means the current state of WDMA.

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The state machine of the WDMA is as the following:

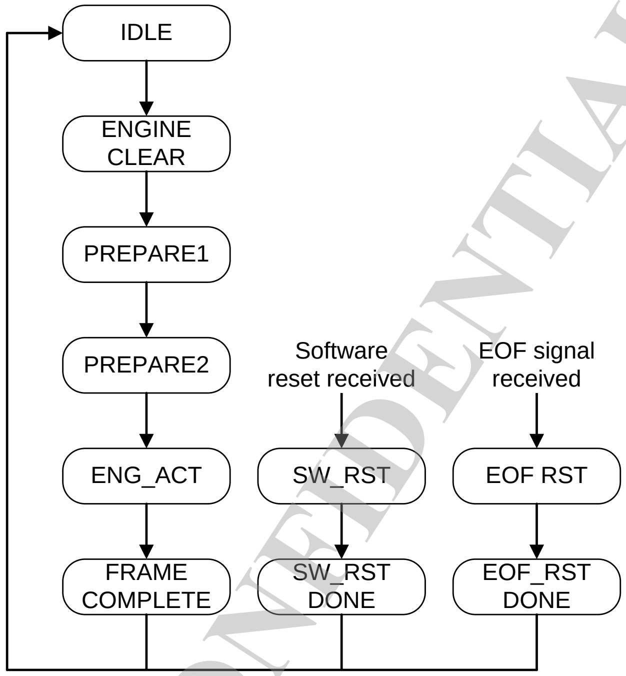

Figure 6-44. Typical DISP_WDMA programming sequence

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6.14 Color Processor

6.14.1 Introduction

The color management engine is highly configurable and programmable; it fits different display panels and satisfies different user preferences for various purposes.

Color management is designed for two applications, getting better picture quality, and having one panel resemble the other in their output characteristics. With color processor, you can obtain better picture quality experience, and manufactures have identical and controllable production quality more easily.

A GUI tool is also provided as an easy and intuitive interface to color management.

6.14.2 Features

The color processor is very flexible for luma/saturation/hue adjustments. Main features are:

- Flexible architecture: PQ processing at many possible stages
- Input/output color space conversion
- Hue engine:
  - Partial hue: Modifies hue angle of specific hue phase
- Y engine:
  - Adaptive luma: Adaptively adjusts Y curve according to image content
  - Global contrast/brightness adjustment
  - Chroma boost: Compensates saturation value due to Y change
- Sat engine:
  - Partial S: Modifies saturation value of specific hue phase
  - Global saturation adjustment
- Histogram statistics: Includes Y histogram and chroma histogram

6.14.3 Block Diagram

The color engine provides various luma/saturation/hue adjustments. See Figure 6-45 for the block diagram.

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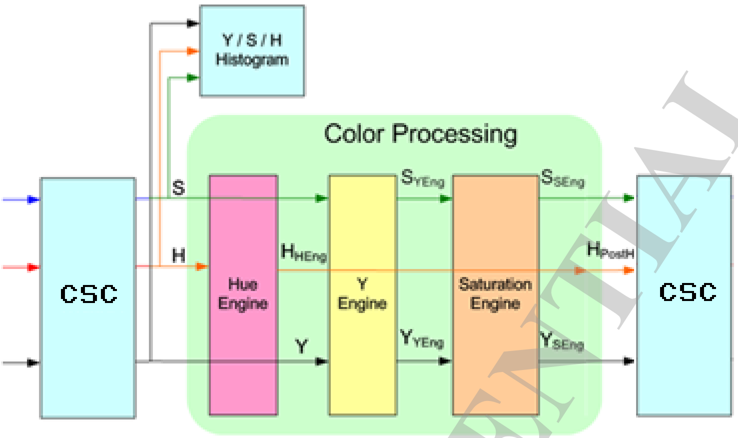

Figure 6-45. Block diagram of color processor

6.14.4 Register Definition

Module name: DISP_COLOR Base address: (+1400B000h)

Address	Name	Width	Register Function
1400B400	DISP_COLOR_CFG_MAIN	32	Configuration
1400B404	DISP_COLOR_PXL_CNT_MAIN	32	Pixel Counter
1400B408	DISP_COLOR_LINE_CNT_MAIN	32	Line Counter
1400B40C	DISP_COLOR_WIN_X_MAIN	32	Window X
1400B410	DISP_COLOR_WIN_Y_MAIN	32	Window Y
1400B418	DISP_COLOR_TIMING_DETECTION_0	32	Timing Detection 0
1400B41C	DISP_COLOR_TIMING_DETECTION_1	32	Timing Detection 1
1400B420	DISP_COLOR_DBG_CFG_MAIN	32	Debug Mode Config
1400B428	DISP_COLOR_C_BOOST_MAIN	32	Chroma Boost
1400B42C	DISP_COLOR_C_BOOST_MAIN_2	32	Chroma Boost 2
1400B430	DISP_COLOR_LUMA_ADJ	32	Input Y Level Adjust
1400B434	DISP_COLOR_G_PIC_ADJ_MAIN_1	32	Global Picture Adjustment
1400B438	DISP_COLOR_G_PIC_ADJ_MAIN_2	32	Global Picture Adjustment
1400B484	DISP_COLOR_POS_MAIN	32	Position X
1400B488	DISP_COLOR_INK_DATA_MAIN	32	Ink Data Y
1400B48C	DISP_COLOR_INK_DATA_MAIN_CR	32	Ink Data Cr

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Address	Name	Width	Register Function
1400B490	DISP_COLOR_CAP_IN_DATA_MAIN	32	Capture In Data Y
1400B494	DISP_COLOR_CAP_IN_DATA_MAIN_CR	32	Capture In Data Cr
1400B498	DISP_COLOR_CAP_OUT_DATA_MAIN	32	Capture Out Data Y
1400B49C	DISP_COLOR_CAP_OUT_DATA_MAIN_CR	32	Capture Out Data Cr
1400B4A0	DISP_COLOR_Y_SLOPE_1_0_MAIN	32	Y Slope 1, 0
1400B4A4	DISP_COLOR_Y_SLOPE_3_2_MAIN	32	Y Slope 3, 2
1400B4A8	DISP_COLOR_Y_SLOPE_5_4_MAIN	32	Y Slope 5, 4
1400B4AC	DISP_COLOR_Y_SLOPE_7_6_MAIN	32	Y Slope 7, 6
1400B4B0	DISP_COLOR_Y_SLOPE_9_8_MAIN	32	Y Slope 9, 8
1400B4B4	DISP_COLOR_Y_SLOPE_11_10_MAIN	32	Y Slope 11, 10
1400B4B8	DISP_COLOR_Y_SLOPE_13_12_MAIN	32	Y Slope 13, 12
1400B4BC	DISP_COLOR_Y_SLOPE_15_14_MAIN	32	Y Slope 15, 14
1400B620	DISP_COLOR_LOCAL_HUE_CD_0	32	Local Hue Cost Down 0
1400B624	DISP_COLOR_LOCAL_HUE_CD_1	32	Local Hue Cost Down 1
1400B628	DISP_COLOR_LOCAL_HUE_CD_2	32	Local Hue Cost Down 2
1400B62C	DISP_COLOR_LOCAL_HUE_CD_3	32	Local Hue Cost Down 3
1400B630	DISP_COLOR_LOCAL_HUE_CD_4	32	Local Hue Cost Down 4
1400B740	DISP_COLOR_TWO_D_WINDOW_1	32	Two D Window 1
1400B74C	DISP_COLOR_TWO_D_W1_RESULT	32	Two D Window 1 Result
1400B768	DISP_COLOR_SAT_HIST_X_CFG_MAIN	32	Saturation Histogram Horizontal Range
1400B76C	DISP_COLOR_SAT_HIST_Y_CFG_MAIN	32	Saturation Histogram Vertical Range
1400B79C	DISP_COLOR_BWS_2	32	Black White Stretch 2
1400B7E0	DISP_COLOR_CRC_0	32	CRC_0
1400B7E4	DISP_COLOR_CRC_1	32	CRC_1
1400B7E8	DISP_COLOR_CRC_2	32	CRC_2
1400B7EC	DISP_COLOR_CRC_3	32	CRC_3
1400B7F0	DISP_COLOR_CRC_4	32	CRC_4
1400B7FC	DISP_COLOR_PARTIAL_SAT_GAIN1_0	32	Partial Sat Gain1 from Hue Phase 0 to 3
1400B800	DISP_COLOR_PARTIAL_SAT_GAIN1_1	32	Partial Sat Gain1 from Hue Phase 4 to 7
1400B804	DISP_COLOR_PARTIAL_SAT_GAIN1_2	32	Partial Sat Gain1 from Hue Phase 8 to 11
1400B808	DISP_COLOR_PARTIA	32	Partial Sat Gain1 from Hue Phase 12 to 15

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Address	Name	Width	Register Function
	L_SAT_GAIN1_3		
1400B80C	DISP_COLOR_PARTIAL_SAT_GAIN1_4	32	Partial Sat Gain1 from Hue Phase 16 to 19
1400B810	DISP_COLOR_PARTIAL_SAT_GAIN2_0	32	Partial Sat Gain2 from Hue Phase 0 to 3
1400B814	DISP_COLOR_PARTIAL_SAT_GAIN2_1	32	Partial Sat Gain2 from Hue Phase 4 to 7
1400B818	DISP_COLOR_PARTIAL_SAT_GAIN2_2	32	Partial Sat Gain2 from Hue Phase 8 to 11
1400B81C	DISP_COLOR_PARTIAL_SAT_GAIN2_3	32	Partial Sat Gain2 from Hue Phase 12 to 15
1400B820	DISP_COLOR_PARTIAL_SAT_GAIN2_4	32	Partial Sat Gain2 from Hue Phase 16 to 19
1400B824	DISP_COLOR_PARTIAL_SAT_GAIN3_0	32	Partial Sat Gain3 from Hue Phase 0 to 3
1400B828	DISP_COLOR_PARTIAL_SAT_GAIN3_1	32	Partial Sat Gain3 from Hue Phase 4 to 7
1400B82C	DISP_COLOR_PARTIAL_SAT_GAIN3_2	32	Partial Sat Gain3 from Hue Phase 8 to 11
1400B830	DISP_COLOR_PARTIAL_SAT_GAIN3_3	32	Partial Sat Gain3 from Hue Phase 12 to 15
1400B834	DISP_COLOR_PARTIAL_SAT_GAIN3_4	32	Partial Sat Gain3 from Hue Phase 16 to 19
1400B838	DISP_COLOR_PARTIAL_SAT_POINT1_0	32	Partial Sat Point1 from Hue Phase 0 to 3
1400B83C	DISP_COLOR_PARTIAL_SAT_POINT1_1	32	Partial Sat Point1 from Hue Phase 4 to 7
1400B840	DISP_COLOR_PARTIAL_SAT_POINT1_2	32	Partial Sat Point1 from Hue Phase 8 to 11
1400B844	DISP_COLOR_PARTIAL_SAT_POINT1_3	32	Partial Sat Point1 from Hue Phase 12 to 15
1400B848	DISP_COLOR_PARTIAL_SAT_POINT1_4	32	Partial Sat Point1 from Hue Phase 16 to 19
1400B84C	DISP_COLOR_PARTIAL_SAT_POINT2_0	32	Partial Sat Point2 from Hue Phase 0 to 3
1400B850	DISP_COLOR_PARTIAL_SAT_POINT2_1	32	Partial Sat Point2 from Hue Phase 4 to 7
1400B854	DISP_COLOR_PARTIAL_SAT_POINT2_2	32	Partial Sat Point2 from Hue Phase 8 to 11
1400B858	DISP_COLOR_PARTIAL_SAT_POINT2_3	32	Partial Sat Point2 from Hue Phase 12 to 15
1400B85C	DISP_COLOR_PARTIAL_SAT_POINT2_4	32	Partial Sat Point2 from Hue Phase 16 to 19
1400BC00	DISP_COLOR_START	32	Configuration
1400BC04	DISP_COLOR_INTEN	32	Interrupt Enable
1400BC08	DISP_COLOR_INTSTA	32	Interrupt Status
1400BC0C	DISP_COLOR_OUT_SEL	32	Output Bits Configuration
1400BC10	DISP_COLOR_FRAME_DONE_DEL	32	Frame Done Delay Select
1400BC14	DISP_COLOR_CRC	32	CRC Enable
1400BC18	DISP_COLOR_SW_SCRATCH	32	Software Scratch
1400BC20	DISP_COLOR_RDY_SEL	32	APB Ready Delay Select

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Address	Name	Width	Register Function
1400BC24	DISP_COLOR_RDY_SEL_EN	32	APB Ready Delay Enable
1400BC28	DISP_COLOR_CK_ON	32	Clock Force On
1400BC50	DISP_COLOR_INTERNAL_IP_WIDTH	32	Wrapper Internal IP Width
1400BC54	DISP_COLOR_INTERNAL_IP_HEIGHT	32	Wrapper Internal IP Height
1400BC60	DISP_COLOR_CM1_EN	32	Front Color Transform Enable
1400BCA0	DISP_COLOR_CM2_EN	32	Back Color Transform Enable
1400BCF0	DISP_COLOR_R0_CRC	32	Wrapper R0 CRC

1400B400 DISP_COLOR_CFG_MAIN Configuration 00002080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	M_REG_RESET	M_DISP_RESET											c_pp_cm_dbg_sel			
Type	RW	RW											RW			
Reset	0	0											0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name			SEQ_SEL					wide_gamut_en	ALLBP			HEBP	SEBP	YEBP	P2CBP	C2PBP
Type			RW					RW	RW			RW	RW	RW	RW	RW
Reset			1					0	1			0	0	0	0	0

Bit(s)	Name	Description
31	M_REG_RESET	**Resets bclk domain**
30	M_DISP_RESET	**Resets display clock domain**
19:16	c_pp_cm_dbg_sel	**Selects debugging signals**
13	SEQ_SEL	
8	wide_gamut_en	**Enables wide gamut transformation**
7	ALLBP	**Bypasses all engine** 0: Normal function 1: Bypass
4	HEBP	**Bypasses hue engine** 0: Normal function 1: Bypass
3	SEBP	**Bypasses saturation engine** 0: Normal function 1: Bypass
2	YEBP	**Bypasses luma engine** 0: Normal function 1: Bypass
1	P2CBP	**Bypasses polar to cartesian engine** 0: Normal function 1: Bypass
0	C2PBP	**Bypasses cartesian to polar engine** 0: Normal function

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Bit(s)	Name	Description
		1: Bypass

1400B404 **DISP_COLOR_PXL_CNT_MAIN** **Pixel Counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	H_CONT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	H_CONT	Current horizontal pixel counter

1400B408 **DISP_COLOR_LINE_CNT_MAIN** **Line Counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	V_CONT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LINE_CONT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	V_CONT	Current vertical pixel counter
15:0	LINE_CONT	Current vertical line counter

1400B40C **DISP_COLOR_WIN_X_MAIN** **Window X** **FFFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WIN_X_END															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WIN_X_START															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	WIN_X_END	X end for processing window

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Bit(s)	Name	Description
15:0	WIN_X_START	X start for processing window

1400B410 **DISP_COLOR_WIN_Y_MAIN** **Window Y** **FFFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WIN_Y_END															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WIN_Y_START															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	WIN_Y_END	Y end for processing window
15:0	WIN_Y_START	Y start for processing window

1400B418 **DISP_COLOR_TIMING_DETECTION_0** **Timing Detection 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	vtotal_cnt															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	htotal_cnt															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	vtotal_cnt	Information of input V total
15:0	htotal_cnt	Information of input H total

1400B41C **DISP_COLOR_TIMING_DETECTION_1** **Timing Detection 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	vde_cnt															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hde_cnt															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:16	vde_cnt	Information of input V DE
15:0	hde_cnt	Information of input H DE

1400B420 **DISP_COLOR_DBG_CFG_MAIN** **Debug Mode Config** **00000700**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CR_INK_SHIFT		CB_INK_SHIFT		Y_INK_SHIFT		CR_INK_MODE			CB_INK_MODE			Y_INK_MODE		
Type		RW		RW		RW		RW			RW			RW		
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					W1_INK_EN	CR_REPLACE	CB_REPLACE	Y_REPLACE					SPLIT_EN	CAP_EN		INK_EN
Type					RW	RW	RW	RW					RW	RW		RW
Reset					0	1	1	1					0	0		0

Bit(s)	Name	Description
30:29	CR_INK_SHIFT	**For Cr ink mode 4, 5, 6**
28:27	CB_INK_SHIFT	**For Cb ink mode 4, 5, 6**
26:25	Y_INK_SHIFT	**For Y ink mode 4, 5, 6**
24:22	CR_INK_MODE	0: Single pixel ink mode 1: Full screen ink mode 2: Ramp pattern 1 (00112233) 3: Ramp pattern 2 (02468) 4: Ramp pattern 3 (0X4,8X4) 5: Ramp pattern 4 (0X8,16X8) 6: Ramp pattern 5 (0X16, 32X16)
21:19	CB_INK_MODE	0: Single pixel ink mode 1: Full screen ink mode 2: Ramp pattern 1 (00112233) 3: Ramp pattern 2 (02468) 4: Ramp pattern 3 (0X4,8X4) 5: Ramp pattern 4 (0X8,16X8) 6: Ramp pattern 5 (0X16, 32X16)
18:16	Y_INK_MODE	0: Single pixel ink mode 1: Full screen ink mode 2: Ramp pattern 1 (00112233) 3: Ramp pattern 2 (02468) 4: Ramp pattern 3 (0X4,8X4) 5: Ramp pattern 4 (0X8,16X8) 6: Ramp pattern 5 (0X16, 32X16)
11	W1_INK_EN	**Enables ink for 2D counter 1**
10	CR_REPLACE	0: Cr data not replaced in ink mode 1: Cr data replaced
9	CB_REPLACE	0: Cb data not replaced in ink mode 1: Cb data replaced
8	Y_REPLACE	0: Y data not replaced in ink mode 1: Y data replaced
3	SPLIT_EN	**Enables split window for demo mode or not** 0: Full window is processed.

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Bit(s)	Name	Description
		1: Enable window split function; range is defined in [26:16].
2	CAP_EN	**Enables data capture** Capture coordinate is defined in POS_X and POS_Y. 0: Disable 1: Enable
0	INK_EN	**Enables ink mode or not** 0: Disable 1: Enable

1400B428 **DISP_COLOR_C_BOOST_MAIN** **Chroma Boost** **FF402080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NEW_CBOOST_LMT_U								NEW_CBOOST_LMT_L							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name			NEW_CBOOST_EN						CBOOST_GAIN							
Type			RW						RW							
Reset			1						1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	NEW_CBOOST_LMT_U	**Chroma boost gain upper bound**
23:16	NEW_CBOOST_LMT_L	**Chroma boost gain lower bound**
13	NEW_CBOOST_EN	0: Disable new chroma boost 1: Enable new chroma boost
7:0	CBOOST_GAIN	**128 denotes 1.0**

1400B42C **DISP_COLOR_C_BOOST_MAIN_2** **Chroma Boost 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															CBOOST_YOFFSET_SEL	
Type															RW	
Reset															0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name									CBOOST_YOFFSET							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:16	CBOOST_YOFFSET_SEL	Limit function of CBOOST_YOFFSET

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Bit(s)	Name	Description
7:0	CBOOST_YOFFSET	Y offset value of chroma boost

1400B430 **DISP_COLOR_LUMA_ADJ** **Input Y Level Adjust** **0000FF40**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Y_SLOPE_LMT									Y_LEV_ADJ						
Type	RW									RW						
Reset	1	1	1	1	1	1	1	1		1	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	Y_SLOPE_LMT	**Limitation value of delta related to y slope, +- Y_SLOPE_LMT**
6:0	Y_LEV_ADJ	Adjusts Y level before global contrast. 0x40: No adjustment 0x3F: Minus 1 before global contrast and brightness (will be added back after global contrast and brightness) 0x41: Plus 1 before global contrast and brightness (will be subtracted after global contrast and brightness)

1400B434 **DISP_COLOR_G_PIC_ADJ_MAIN_1** **Global Picture Adjustment** **04000080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						BRIGHTNESS										
Type						RW										
Reset						1	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name							CONTRAST									
Type							RW									
Reset							0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:16	BRIGHTNESS	**Adjusts global brightness value** Brightness = (value-1024)
9:0	CONTRAST	**Adjusts global contrast** 0: Multiplied by 0.0 128: Multiplied by 1.0 255: multiplied by 1.992

1400B438 **DISP_COLOR_G_PIC_ADJ_MAIN_2** **Global Picture Adjustment** **00000080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

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Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SATURATION									
Type							RW									
Reset							0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	SATURATION	**Adjusts global saturation** 0: Multiplied by 0.0 128: Multiplied by 1.0 255 Multiplied by 1.992

1400B484 DISP_COLOR_POS_MAIN Position X 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	POS_Y															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	POS_X															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	POS_Y	Capture or ink Y coordinate
15:0	POS_X	Capture or ink X coordinate

1400B488 DISP_COLOR_INK_DATA_MAIN Ink Data Y 020003FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							INK_DATA_CB									
Type							RW									
Reset							1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							INK_DATA_Y									
Type							RW									
Reset							1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
25:16	INK_DATA_CB	Cb value of ink data
9:0	INK_DATA_Y	Y value of ink data

1400B48C DISP_COLOR_INK_DATA_MAIN_CR Ink Data Cr 00000200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

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Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**INK_DATA_CR**									
Type							RW									
Reset							1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	INK_DATA_CR	Cr value of ink data

1400B490 DISP_COLOR_CAP_IN_DATA_MAIN Capture In Data Y 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							**CAP_IN_CB**									
Type							RO									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**CAP_IN_Y**									
Type							RO									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	CAP_IN_CB	Capture data of input Cb
9:0	CAP_IN_Y	Capture data of input Y

1400B494 DISP_COLOR_CAP_IN_DATA_MAIN_CR Capture In Data Cr 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**CAP_IN_CR**									
Type							RO									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	CAP_IN_CR	Capture data of input Cr

1400B498 DISP_COLOR_CAP_OUT_DATA_MAIN Capture Out Data Y 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**CAP_OUT_CB**											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**CAP_OUT_Y**									

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Type							RO									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	CAP_OUT_CB	Capture data of output Cb
9:0	CAP_OUT_Y	Capture data of output Y

1400B49C DISP_COLOR_CAP_OUT_DATA_MAIN_CR Capture Out Data Cr 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CAP_OUT_CR												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	CAP_OUT_CR	Capture data of output Cr

1400B4A0 DISP_COLOR_Y_SLOPE_1_0_MAIN Y Slope 1, 0 00800080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									Y_Slope_1							
Type									RW							
Reset									1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									Y_Slope_0							
Type									RW							
Reset									1	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	Y_Slope_1	**Y slope 1** 255: 0.992 128: 0.0 0: -10
7:0	Y_Slope_0	**Y slope 0** 255: 0.992 128: 0.0 0: -1.0

1400B4A4 DISP_COLOR_Y_SLOPE_3_2_MAIN Y Slope 3, 2 00800080

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									Y_Slope_3							
Type									RW							
Reset									1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									Y_Slope_2							
Type									RW							
Reset									1	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	Y_Slope_3	**Y slope 3** 255: 0.992 128: 0.0 0: -1.0
7:0	Y_Slope_2	**Y slope 2** 255: 0.992 128: 0.0 0: -1.0

1400B4A8 **DISP_COLOR_Y_SLOPE_5_4_MAIN** **Y Slope 5, 4** **00800080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									Y_Slope_5							
Type									RW							
Reset									1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									Y_Slope_4							
Type									RW							
Reset									1	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	Y_Slope_5	**Y slope 5** 255: 0.992 128: 0.0 0: -1.0
7:0	Y_Slope_4	**Y slope 4** 255: 0.992 128: 0.0 0: -1.0

1400B4AC **DISP_COLOR_Y_SLOPE_7_6_MAIN** **Y Slope 7, 6** **00800080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									Y_Slope_7							
Type									RW							
Reset									1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									Y_Slope_6							
Type									RW							
Reset									1	0	0	0	0	0	0	0

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Bit(s)	Name	Description
23:16	Y_Slope_7	**Y slope 7** 255: 0.992 128: 0.0 0: -1.0
7:0	Y_Slope_6	**Y slope 6** 255: 0.992 128: 0.0 0: -1.0

1400B4B0 DISP_COLOR_Y_SLOPE_9_8_MAIN Y Slope 9, 8 00800080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									Y_Slope_9							
Type									RW							
Reset									1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									Y_Slope_8							
Type									RW							
Reset									1	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	Y_Slope_9	**Y slope 9** 255: 0.992 128: 0.0 0: -1.0
7:0	Y_Slope_8	**Y slope 8** 255: 0.992 128: 0.0 0: -1.0

1400B4B4 DISP_COLOR_Y_SLOPE_11_10_MAIN Y Slope 11, 10 00800080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									Y_Slope_11							
Type									RW							
Reset									1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									Y_Slope_10							
Type									RW							
Reset									1	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	Y_Slope_11	**Y slope 11** 255: 0.992 128: 0.0 0: -1.0
7:0	Y_Slope_10	**Y slope 10** 255: 0.992 128: 0.0

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Bit(s)	Name	Description
		0: -1.0

1400B4B8 **DISP_COLOR_Y_SLOPE_13_12_MAIN** **Y Slope 13, 12** **00800080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									Y_Slope_13							
Type									RW							
Reset									1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									Y_Slope_12							
Type									RW							
Reset									1	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	Y_Slope_13	**Y slope 13** 255: 0.992 128: 0.0 0: -1.0
7:0	Y_Slope_12	**Y slope 12** 255: 0.992 128: 0.0 0: -1.0

1400B4BC **DISP_COLOR_Y_SLOPE_15_14_MAIN** **Y Slope 15, 14** **00800080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									Y_Slope_15							
Type									RW							
Reset									1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									Y_Slope_14							
Type									RW							
Reset									1	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	Y_Slope_15	**Y slope 15** 255: 0.992 128: 0.0 0: -1.0
7:0	Y_Slope_14	**Y slope 14** 255: 0.992 128: 0.0 0: -1.0

1400B620 **DISP_COLOR_LOCAL_HUE** **Local Hue Cost Down 0** **80808080**

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_CD_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	hue_to_hue_3								hue_to_hue_2							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hue_to_hue_1								hue_to_hue_0							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	hue_to_hue_3	0x01: -127 0x80: 0 0xFF: +127
23:16	hue_to_hue_2	0x01: -127 0x80: 0 0xFF: +127
15:8	hue_to_hue_1	0x01: -127 0x80: 0 0xFF: +127
7:0	hue_to_hue_0	0x01: -127 0x80: 0 0xFF: +127

1400B624 DISP_COLOR_LOCAL_HUE_CD_1 Local Hue Cost Down 1 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	hue_to_hue_7								hue_to_hue_6							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hue_to_hue_5								hue_to_hue_4							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	hue_to_hue_7	0x01: -127 0x80: 0 0xFF: +127
23:16	hue_to_hue_6	0x01: -127 0x80: 0 0xFF: +127
15:8	hue_to_hue_5	0x01: -127 0x80: 0 0xFF: +127
7:0	hue_to_hue_4	0x01: -127 0x80: 0 0xFF: +127

1400B628 DISP_COLOR Local Hue Cost Down 2 80808080

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_LOCAL_HUE_CD_2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	hue_to_hue_11								hue_to_hue_10							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hue_to_hue_9								hue_to_hue_8							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	hue_to_hue_11	0x01: -127 0x80: 0 0xFF: +127
23:16	hue_to_hue_10	0x01: -127 0x80: 0 0xFF: +127
15:8	hue_to_hue_9	0x01: -127 0x80: 0 0xFF: +127
7:0	hue_to_hue_8	0x01: -127 0x80: 0 0xFF: +127

1400B62C **DISP_COLOR_LOCAL_HUE_CD_3** **Local Hue Cost Down 3** **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	hue_to_hue_15								hue_to_hue_14							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hue_to_hue_13								hue_to_hue_12							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	hue_to_hue_15	0x01: -127 0x80: 0 0xFF: +127
23:16	hue_to_hue_14	0x01: -127 0x80: 0 0xFF: +127
15:8	hue_to_hue_13	0x01: -127 0x80: 0 0xFF: +127
7:0	hue_to_hue_12	0x01: -127 0x80: 0 0xFF: +127

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1400B630 **DISP_COLOR_LOCAL_HUE_CD_4** **Local Hue Cost Down 4** **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	hue_to_hue_19								hue_to_hue_18							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hue_to_hue_17								hue_to_hue_16							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	hue_to_hue_19	0x01: -127 0x80: 0 0xFF: +127
23:16	hue_to_hue_18	0x01: -127 0x80: 0 0xFF: +127
15:8	hue_to_hue_17	0x01: -127 0x80: 0 0xFF: +127
7:0	hue_to_hue_16	0x01: -127 0x80: 0 0xFF: +127

1400B740 **DISP_COLOR_TWO_D_WINDOW_1** **Two D Window 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	W1_SAT_UPPER								W1_SAT_LOWER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	W1_HUE_UPPER								W1_HUE_LOWER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	W1_SAT_UPPER	Saturation upper bound for accumulation
23:16	W1_SAT_LOWER	Saturation lower bound for accumulation
15:8	W1_HUE_UPPER	Hue upper bound for accumulation
7:0	W1_HUE_LOWER	Hue lower bound for accumulation

1400B74C **DISP_COLOR_TWO_D_W1_RESULT** **Two D Window 1 Result** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										W1_RESULT[22:16]						
Type										RO						

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Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	W1_RESULT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
22:0	W1_RESULT	Result of window 1

1400B768 DISP_COLOR_SAT_HIST_X_CFG_MAIN Saturation Histogram Horizontal Range FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SAT_WIN_X_END															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SAT_WIN_X_START															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SAT_WIN_X_END	**Saturation histogram window** X end position
15:0	SAT_WIN_X_START	**Saturation histogram window** X start position

1400B76C DISP_COLOR_SAT_HIST_Y_CFG_MAIN Saturation Histogram Vertical Range FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SAT_WIN_Y_END															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SAT_WIN_Y_START															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SAT_WIN_Y_END	**Saturation histogram window** Y end position
15:0	SAT_WIN_Y_START	**Saturation histogram window** Y start position

1400B79C DISP_COLOR_BWS_2 Black White Stretch 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name					PPMCM_ATPG_CT	PPMCM_ATPG_OB										
Type					RW	RW										
Reset					0	0										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
27	PPMCM_ATPG_CT	HW debugging register
26	PPMCM_ATPG_OB	HW debugging register

1400B7E0 **DISP_COLOR_CRC_0** **CRC_0** **00000000B**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													crc_src_sel			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	crc_still_check_max								crc_non_still_cnt				crc_still_check_done	c_crc_still_check_trig	crc_l_en	crc_r_en
Type	RW								RO				RO	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1

Bit(s)	Name	Description
19:16	crc_src_sel	**Selects CRC source** 0: Color engine output 1: Channel delay output 2: C2P output 3: Hue output 4: Luma output 5: Sat output
15:8	crc_still_check_max	**Max. count of CRC still frame check**
7:4	crc_non_still_cnt	**Count status of CRC non still field/frame**
3	crc_still_check_done	**Ready status of CRC still frame check**
2	c_crc_still_check_trig	**Triggers CRC still frame check**
1	crc_l_en	**Enables CRC for left frame**
0	crc_r_en	**Enables CRC for right frame**

1400B7E4 **DISP_COLOR_CRC_1** **CRC_1** **1FFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				crc_clip_h_end												
Type				RW												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				crc_clip_h_start												

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Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	crc_clip_h_end	CRC calculation range: H end
12:0	crc_clip_h_start	CRC calculation range: H start

1400B7E8 DISP_COLOR_CRC_2 CRC_2 0FFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					crc_clip_v_end											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					crc_clip_v_start											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	crc_clip_v_end	CRC calculation range: V end
11:0	crc_clip_v_start	CRC calculation range: V start

1400B7EC DISP_COLOR_CRC_3 CRC_3 3FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			crc_y_mask										crc_c_mask[9:6]			
Type			RW										RW			
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	crc_c_mask[5:0]						crc_v_mask									
Type	RW						RW									
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
29:20	crc_y_mask	Masks CRC for Y channel
19:10	crc_c_mask	Masks CRC for Cb channel
9:0	crc_v_mask	Masks CRC for Cr channel

1400B7F0 DISP_COLOR_CRC_4 CRC_4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	crc_result[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	crc_result[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	crc_result	CRC result of one frame

1400B7FC **DISP_COLOR_PARTIAL_SAT_GAIN1_0** **Partial Sat Gain1 from Hue Phase 0 to 3** **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain1_hue_3								sat_gain1_hue_2							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain1_hue_1								sat_gain1_hue_0							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain1_hue_3	Partial Sat Gain1 in Hue Phase 3
23:16	sat_gain1_hue_2	Partial Sat Gain1 in Hue Phase 2
15:8	sat_gain1_hue_1	Partial Sat Gain1 in Hue Phase 1
7:0	sat_gain1_hue_0	Partial Sat Gain1 in Hue Phase 0

1400B800 **DISP_COLOR_PARTIAL_SAT_GAIN1_1** **Partial Sat Gain1 from Hue Phase 4 to 7** **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain1_hue_7								sat_gain1_hue_6							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain1_hue_5								sat_gain1_hue_4							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain1_hue_7	Partial Sat Gain1 in Hue Phase 7
23:16	sat_gain1_hue_6	Partial Sat Gain1 in Hue Phase 6
15:8	sat_gain1_hue_5	Partial Sat Gain1 in Hue Phase 5
7:0	sat_gain1_hue_4	Partial Sat Gain1 in Hue Phase 4

1400B804 **DISP_COLOR_PARTIAL_SAT_GAIN1_2** **Partial Sat Gain1 from Hue Phase 8 to 11** **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain1_hue_11								sat_gain1_hue_10							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain1_hue_9								sat_gain1_hue_8							

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Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain1_hue_11	Partial Sat Gain1 in Hue Phase 11
23:16	sat_gain1_hue_10	Partial Sat Gain1 in Hue Phase 10
15:8	sat_gain1_hue_9	Partial Sat Gain1 in Hue Phase 9
7:0	sat_gain1_hue_8	Partial Sat Gain1 in Hue Phase 8

1400B808 DISP_COLOR_PARTIAL_SAT_GAIN1_3 Partial Sat Gain1 from Hue Phase 12 to 15 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain1_hue_15								sat_gain1_hue_14							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain1_hue_13								sat_gain1_hue_12							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain1_hue_15	Partial Sat Gain1 in Hue Phase 15
23:16	sat_gain1_hue_14	Partial Sat Gain1 in Hue Phase 14
15:8	sat_gain1_hue_13	Partial Sat Gain1 in Hue Phase 13
7:0	sat_gain1_hue_12	Partial Sat Gain1 in Hue Phase 12

1400B80C DISP_COLOR_PARTIAL_SAT_GAIN1_4 Partial Sat Gain1 from Hue Phase 16 to 19 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain1_hue_19								sat_gain1_hue_18							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain1_hue_17								sat_gain1_hue_16							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain1_hue_19	Partial Sat Gain1 in Hue Phase 19
23:16	sat_gain1_hue_18	Partial Sat Gain1 in Hue Phase 18
15:8	sat_gain1_hue_17	Partial Sat Gain1 in Hue Phase 17
7:0	sat_gain1_hue_16	Partial Sat Gain1 in Hue Phase 16

1400B810 DISP_COLOR_PARTIAL_SA Partial Sat Gain2 from Hue Phase 0 to 3 80808080

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T_GAIN2_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain2_hue_3								sat_gain2_hue_2							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain2_hue_1								sat_gain2_hue_0							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain2_hue_3	Partial Sat Gain2 in Hue Phase 3
23:16	sat_gain2_hue_2	Partial Sat Gain2 in Hue Phase 2
15:8	sat_gain2_hue_1	Partial Sat Gain2 in Hue Phase 1
7:0	sat_gain2_hue_0	Partial Sat Gain2 in Hue Phase 0

1400B814 DISP_COLOR_PARTIAL_SAT_GAIN2_1 Partial Sat Gain2 from Hue Phase 4 to 7 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain2_hue_7								sat_gain2_hue_6							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain2_hue_5								sat_gain2_hue_4							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain2_hue_7	Partial Sat Gain2 in Hue Phase 7
23:16	sat_gain2_hue_6	Partial Sat Gain2 in Hue Phase 6
15:8	sat_gain2_hue_5	Partial Sat Gain2 in Hue Phase 5
7:0	sat_gain2_hue_4	Partial Sat Gain2 in Hue Phase 4

1400B818 DISP_COLOR_PARTIAL_SAT_GAIN2_2 Partial Sat Gain2 from Hue Phase 8 to 11 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain2_hue_11								sat_gain2_hue_10							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain2_hue_9								sat_gain2_hue_8							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain2_hue_11	Partial Sat Gain2 in Hue Phase 11
23:16	sat_gain2_hue_10	Partial Sat Gain2 in Hue Phase 10
15:8	sat_gain2_hue_9	Partial Sat Gain2 in Hue Phase 9

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Bit(s)	Name	Description
7:0	sat_gain2_hue_8	Partial Sat Gain2 in Hue Phase 8

1400B81C **DISP_COLOR_PARTIAL_SAT_GAIN2_3** **Partial Sat Gain2 from Hue Phase 12 to 15** **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain2_hue_15								sat_gain2_hue_14							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain2_hue_13								sat_gain2_hue_12							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain2_hue_15	Partial Sat Gain2 in Hue Phase 15
23:16	sat_gain2_hue_14	Partial Sat Gain2 in Hue Phase 14
15:8	sat_gain2_hue_13	Partial Sat Gain2 in Hue Phase 13
7:0	sat_gain2_hue_12	Partial Sat Gain2 in Hue Phase 12

1400B820 **DISP_COLOR_PARTIAL_SAT_GAIN2_4** **Partial Sat Gain2 from Hue Phase 16 to 19** **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain2_hue_19								sat_gain2_hue_18							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain2_hue_17								sat_gain2_hue_16							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain2_hue_19	Partial Sat Gain2 in Hue Phase 19
23:16	sat_gain2_hue_18	Partial Sat Gain2 in Hue Phase 18
15:8	sat_gain2_hue_17	Partial Sat Gain2 in Hue Phase 17
7:0	sat_gain2_hue_16	Partial Sat Gain2 in Hue Phase 16

1400B824 **DISP_COLOR_PARTIAL_SAT_GAIN3_0** **Partial Sat Gain3 from Hue Phase 0 to 3** **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain3_hue_3								sat_gain3_hue_2							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain3_hue_1								sat_gain3_hue_0							

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Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain3_hue_3	Partial Sat Gain3 in Hue Phase 3
23:16	sat_gain3_hue_2	Partial Sat Gain3 in Hue Phase 2
15:8	sat_gain3_hue_1	Partial Sat Gain3 in Hue Phase 1
7:0	sat_gain3_hue_0	Partial Sat Gain3 in Hue Phase 0

1400B828 **DISP_COLOR_PARTIAL_SAT_GAIN3_1** **Partial Sat Gain3 from Hue Phase 4 to 7** **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain3_hue_7								sat_gain3_hue_6							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain3_hue_5								sat_gain3_hue_4							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain3_hue_7	Partial Sat Gain3 in Hue Phase 7
23:16	sat_gain3_hue_6	Partial Sat Gain3 in Hue Phase 6
15:8	sat_gain3_hue_5	Partial Sat Gain3 in Hue Phase 5
7:0	sat_gain3_hue_4	Partial Sat Gain3 in Hue Phase 4

1400B82C **DISP_COLOR_PARTIAL_SAT_GAIN3_2** **Partial Sat Gain3 from Hue Phase 8 to 11** **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain3_hue_11								sat_gain3_hue_10							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain3_hue_9								sat_gain3_hue_8							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain3_hue_11	Partial Sat Gain3 in Hue Phase 11
23:16	sat_gain3_hue_10	Partial Sat Gain3 in Hue Phase 10
15:8	sat_gain3_hue_9	Partial Sat Gain3 in Hue Phase 9
7:0	sat_gain3_hue_8	Partial Sat Gain3 in Hue Phase 8

1400B830 **DISP_COLOR_PARTIAL_SA** **Partial Sat Gain3 from Hue Phase 12 to 15** **80808080**

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T_GAIN3_3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**sat_gain3_hue_15**								**sat_gain3_hue_14**							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**sat_gain3_hue_13**								**sat_gain3_hue_12**							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain3_hue_15	Partial Sat Gain3 in Hue Phase 15
23:16	sat_gain3_hue_14	Partial Sat Gain3 in Hue Phase 14
15:8	sat_gain3_hue_13	Partial Sat Gain3 in Hue Phase 13
7:0	sat_gain3_hue_12	Partial Sat Gain3 in Hue Phase 12

1400B834 **DISP_COLOR_PARTIAL_SAT_GAIN3_4** **Partial Sat Gain3 from Hue Phase 16 to 19** **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**sat_gain3_hue_19**								**sat_gain3_hue_18**							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**sat_gain3_hue_17**								**sat_gain3_hue_16**							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain3_hue_19	Partial Sat Gain3 in Hue Phase 19
23:16	sat_gain3_hue_18	Partial Sat Gain3 in Hue Phase 18
15:8	sat_gain3_hue_17	Partial Sat Gain3 in Hue Phase 17
7:0	sat_gain3_hue_16	Partial Sat Gain3 in Hue Phase 16

1400B838 **DISP_COLOR_PARTIAL_SAT_POINT1_0** **Partial Sat Point1 from Hue Phase 0 to 3** **1E1E1E1E**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**sat_point1_hue_3**								**sat_point1_hue_2**							
Type	RW								RW							
Reset	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**sat_point1_hue_1**								**sat_point1_hue_0**							
Type	RW								RW							
Reset	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0

Bit(s)	Name	Description
31:24	sat_point1_hue_3	Partial Sat Point1 in Hue Phase 3
23:16	sat_point1_hue_2	Partial Sat Point1 in Hue Phase 2
15:8	sat_point1_hue_1	Partial Sat Point1 in Hue Phase 1

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Bit(s)	Name	Description
7:0	sat_point1_hue_0	Partial Sat Point1 in Hue Phase 0

1400B83C **DISP_COLOR_PARTIAL_SAT_POINT1_1** **Partial Sat Point1 from Hue Phase 4 to 7** **1E1E1E1E**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_point1_hue_7								sat_point1_hue_6							
Type	RW								RW							
Reset	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_point1_hue_5								sat_point1_hue_4							
Type	RW								RW							
Reset	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0

Bit(s)	Name	Description
31:24	sat_point1_hue_7	Partial Sat Point1 in Hue Phase 7
23:16	sat_point1_hue_6	Partial Sat Point1 in Hue Phase 6
15:8	sat_point1_hue_5	Partial Sat Point1 in Hue Phase 5
7:0	sat_point1_hue_4	Partial Sat Point1 in Hue Phase 4

1400B840 **DISP_COLOR_PARTIAL_SAT_POINT1_2** **Partial Sat Point1 from Hue Phase 8 to 11** **1E1E1E1E**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_point1_hue_11								sat_point1_hue_10							
Type	RW								RW							
Reset	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_point1_hue_9								sat_point1_hue_8							
Type	RW								RW							
Reset	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0

Bit(s)	Name	Description
31:24	sat_point1_hue_11	Partial Sat Point1 in Hue Phase 11
23:16	sat_point1_hue_10	Partial Sat Point1 in Hue Phase 10
15:8	sat_point1_hue_9	Partial Sat Point1 in Hue Phase 9
7:0	sat_point1_hue_8	Partial Sat Point1 in Hue Phase 8

1400B844 **DISP_COLOR_PARTIAL_SAT_POINT1_3** **Partial Sat Point1 from Hue Phase 12 to 15** **1E1E1E1E**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_point1_hue_15								sat_point1_hue_14							
Type	RW								RW							
Reset	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_point1_hue_13								sat_point1_hue_12							

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Type	RW								RW							
Reset	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0

Bit(s)	Name	Description
31:24	sat_point1_hue_15	Partial Sat Point1 in Hue Phase 15
23:16	sat_point1_hue_14	Partial Sat Point1 in Hue Phase 14
15:8	sat_point1_hue_13	Partial Sat Point1 in Hue Phase 13
7:0	sat_point1_hue_12	Partial Sat Point1 in Hue Phase 12

1400B848 **DISP_COLOR_PARTIAL_SAT_POINT1_4** **Partial Sat Point1 from Hue Phase 16 to 19** **1E1E1E1E**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**sat_point1_hue_19**								**sat_point1_hue_18**							
Type	RW								RW							
Reset	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**sat_point1_hue_17**								**sat_point1_hue_16**							
Type	RW								RW							
Reset	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0

Bit(s)	Name	Description
31:24	sat_point1_hue_19	Partial Sat Point1 in Hue Phase 19
23:16	sat_point1_hue_18	Partial Sat Point1 in Hue Phase 18
15:8	sat_point1_hue_17	Partial Sat Point1 in Hue Phase 17
7:0	sat_point1_hue_16	Partial Sat Point1 in Hue Phase 16

1400B84C **DISP_COLOR_PARTIAL_SAT_POINT2_0** **Partial Sat Point2 from Hue Phase 0 to 3** **3C3C3C3C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**sat_point2_hue_3**								**sat_point2_hue_2**							
Type	RW								RW							
Reset	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**sat_point2_hue_1**								**sat_point2_hue_0**							
Type	RW								RW							
Reset	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0

Bit(s)	Name	Description
31:24	sat_point2_hue_3	Partial Sat Point2 in Hue Phase 3
23:16	sat_point2_hue_2	Partial Sat Point2 in Hue Phase 2
15:8	sat_point2_hue_1	Partial Sat Point2 in Hue Phase 1
7:0	sat_point2_hue_0	Partial Sat Point2 in Hue Phase 0

1400B850 **DISP_COLOR_PARTIAL_SA** **Partial Sat Point2 from Hue Phase 4 to 7** **3C3C3C3C**

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T_POINT2_1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_point2_hue_7								sat_point2_hue_6							
Type	RW								RW							
Reset	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_point2_hue_5								sat_point2_hue_4							
Type	RW								RW							
Reset	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0

Bit(s)	Name	Description
31:24	sat_point2_hue_7	Partial Sat Point2 in Hue Phase 7
23:16	sat_point2_hue_6	Partial Sat Point2 in Hue Phase 6
15:8	sat_point2_hue_5	Partial Sat Point2 in Hue Phase 5
7:0	sat_point2_hue_4	Partial Sat Point2 in Hue Phase 4

1400B854	DISP_COLOR_PARTIAL_SAT_POINT2_2	Partial Sat Point2 from Hue Phase 8 to 11	3C3C3C3C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_point2_hue_11								sat_point2_hue_10							
Type	RW								RW							
Reset	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_point2_hue_9								sat_point2_hue_8							
Type	RW								RW							
Reset	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0

Bit(s)	Name	Description
31:24	sat_point2_hue_11	Partial Sat Point2 in Hue Phase 11
23:16	sat_point2_hue_10	Partial Sat Point2 in Hue Phase 10
15:8	sat_point2_hue_9	Partial Sat Point2 in Hue Phase 9
7:0	sat_point2_hue_8	Partial Sat Point2 in Hue Phase 8

1400B858	DISP_COLOR_PARTIAL_SAT_POINT2_3	Partial Sat Point2 from Hue Phase 12 to 15	3C3C3C3C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_point2_hue_15								sat_point2_hue_14							
Type	RW								RW							
Reset	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_point2_hue_13								sat_point2_hue_12							
Type	RW								RW							
Reset	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0

Bit(s)	Name	Description
31:24	sat_point2_hue_15	Partial Sat Point2 in Hue Phase 15
23:16	sat_point2_hue_14	Partial Sat Point2 in Hue Phase 14
15:8	sat_point2_hue_13	Partial Sat Point2 in Hue Phase 13

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Bit(s)	Name	Description
7:0	sat_point2_hue_12	Partial Sat Point2 in Hue Phase 12

1400B85C DISP_COLOR_PARTIAL_SAT_POINT2_4 Partial Sat Point2 from Hue Phase 16 to 19 3C3C3C3C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_point2_hue_19								sat_point2_hue_18							
Type	RW								RW							
Reset	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_point2_hue_17								sat_point2_hue_16							
Type	RW								RW							
Reset	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0

Bit(s)	Name	Description
31:24	sat_point2_hue_19	Partial Sat Point2 in Hue Phase 19
23:16	sat_point2_hue_18	Partial Sat Point2 in Hue Phase 18
15:8	sat_point2_hue_17	Partial Sat Point2 in Hue Phase 17
7:0	sat_point2_hue_16	Partial Sat Point2 in Hue Phase 16

1400BC00 DISP_COLOR_START Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									disp_color_dbg_sel							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								disp_color_sw_rst_engine					disp_color_dbuf_vsync	disp_color_wrap_mode	disp_color_out_sel	disp_color_start
Type								RW					RW	RW	RW	RW
Reset								0					0	0	0	0

Bit(s)	Name	Description
23:16	disp_color_dbg_sel	Selects debugging
8	disp_color_sw_rst_engine	Reset engine
3	disp_color_dbuf_vsync	Color engine shadow at vsync
2	disp_color_wrap_mode	Wrapper_mode
1	disp_color_out_sel	Selects output
0	disp_color_start	Starts disp_color engine

1400BC04 DISP_COLOR Interrupt Enable 00000000

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_INTEN

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**disp_color_inten_fr_underrun**	**disp_color_inten_fr_done**	**disp_color_inten_fr_complete**
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	disp_color_inten_fr_underrun	**Enables interrupt** frame_underrun
1	disp_color_inten_fr_done	**Enables interrupt** frame_done
0	disp_color_inten_fr_complete	**Enables interrupt** frame_complete

1400BC08 DISP_COLOR_INTSTA Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**disp_color_intsta_fr_underrun**	**disp_color_intsta_fr_done**	**disp_color_intsta_fr_complete**
Type														WoC	WoC	WoC
Reset														0	0	0

Bit(s)	Name	Description
2	disp_color_intsta_fr_underrun	**Interrupt status** Frame underrun
1	disp_color_intsta_fr_done	**Interrupt status** Frame done
0	disp_color_intsta_fr_complete	**Interrupt status** Frame completed

1400BC0C DISP_COLOR_OUT_SEL Output Bits Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						reg_chc_uv	reg_chc_round	reg_chc_sel		reg_chb_uv	reg_chb_round	reg_chb_sel		reg_cha_uv	reg_cha_round	reg_cha_sel
Type						RW	RW	RW		RW	RW	RW		RW	RW	RW
Reset						0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
10	reg_chc_uv	channel_c UV output
9	reg_chc_round	channel_c rounding to 8 bits
8	reg_chc_sel	Selects channel_c 8 bits/10 bits
6	reg_chb_uv	channel_b UV output
5	reg_chb_round	channel_b rounding to 8 bits
4	reg_chb_sel	Selects channel_b 8 bits/10 bits
2	reg_cha_uv	channel_a UV output
1	reg_cha_round	channel_a rounding to 8 bits
0	reg_cha_sel	Selects channel_a 8 bits/10 bits

1400BC10 DISP_COLOR_FRAME_DONE_DEL Frame Done Delay Select 00000010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									disp_color_frame_done_del							
Type									RW							
Reset									0	0	0	1	0	0	0	0

Bit(s)	Name	Description
7:0	disp_color_frame_done_del	Selects frame done delay

1400BC14 DISP_COLOR_CRC CRC Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														disp_color_crc_clr	disp_color_crc_start	disp_color_crc_cen
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	disp_color_crc_clr	Clears CRC

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Bit(s)	Name	Description
1	disp_color_crc_start	Starts CRC
0	disp_color_crc_cen	Enables CRC

1400BC18 **DISP_COLOR_SW_SCRATCH** **Software Scratch** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	disp_color_sw_scratch[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	disp_color_sw_scratch[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	disp_color_sw_scratch	disp_color_sw_scratch

1400BC20 **DISP_COLOR_RDY_SEL** **APB Ready Delay Select** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																disp_color_rdy_sel
Type																RW
Reset																0

Bit(s)	Name	Description
0	disp_color_rdy_sel	Selects APB ready delay

1400BC24 **DISP_COLOR_RDY_SEL_EN** **APB Ready Delay Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																disp_color_rdy_sel_en
Type																RO

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Reset																0

Bit(s)	Name	Description
0	disp_color_rdy_sel_en	Enables APB ready delay

1400BC28 DISP_COLOR_CK_ON Clock Force On 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																disp_color_ck_on
Type																RW
Reset																0

Bit(s)	Name	Description
0	disp_color_ck_on	Forces clock on

1400BC50 DISP_COLOR_INTERNAL_IP_WIDTH Wrapper Internal IP Width 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			disp_color_internal_ip_width													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	disp_color_internal_ip_width	Wrapper Internal IP width

1400BC54 DISP_COLOR_INTERNAL_IP_HEIGHT Wrapper Internal IP Height 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			disp_color_internal_ip_height													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
13:0	disp_color_internal_ip_height	Wrapper Internal IP height

1400BC60 DISP_COLOR_CM1_EN Front Color Transform Enable 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name																disp_color_cm1_en
Type																RW
Reset																1

Bit(s)	Name	Description
0	disp_color_cm1_en	Enables front color transformation

1400BCA0 DISP_COLOR_CM2_EN Back Color Transform Enable 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name												disp_color_cm2_round_off		disp_color_cm2_clip_sel		disp_color_cm2_en
Type												RW		RW		RW
Reset												0		0	0	1

Bit(s)	Name	Description
4	disp_color_cm2_round_off	0: No rouding during Y2R conversion 1: Round during Y2R conversion
2:1	disp_color_cm2_clip_sel	0: No mandatory effect. Clip range depends on the wide_gamut_en value. 1: RGB values are forced to be clipped to [511, 0]. 2. RGB values are forced to be clipped to [1023, -1024].
0	disp_color_cm2_en	**Enables back color transformation**

1400BCF0 DISP_COLOR_R0_CRC Wrapper R0 CRC 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															disp_	disp_

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															color_engine_end	color_crc_rdy_o
Type															RO	RO
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**disp_color_crc_out_0**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	disp_color_engine_end	Engine end
16	disp_color_crc_rdy_0	Wrapper R0 CRC ready
15:0	disp_color_crc_out_0	Wrapper R0 CRC data

6.14.5 Programming Guide

6.14.5.1 Hue Adjustment

There are 20 hue phases for partial hue adjustment.

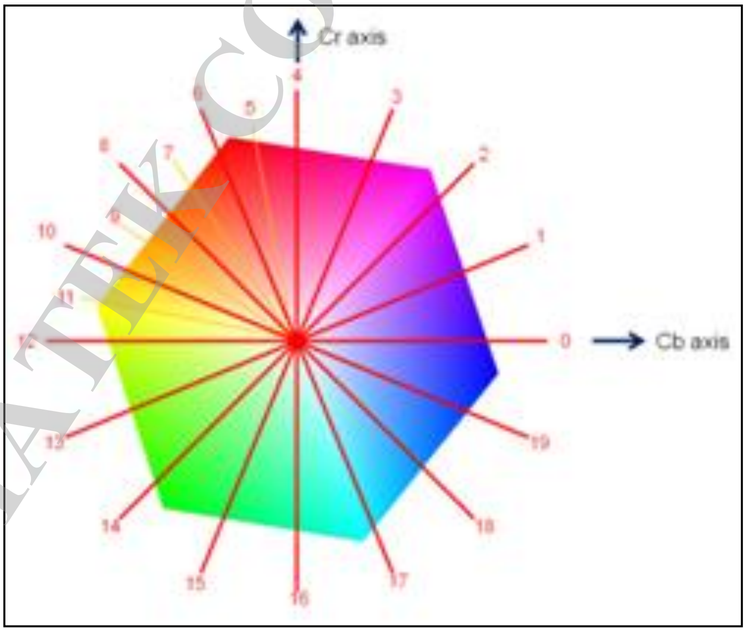

Figure 6-46. 20 hue phases distribution

Partial hue adjustment is achieved by HUE_TO_HUE_W_* registers. An example of partial hue adjustment is shown in Figure 6-47.

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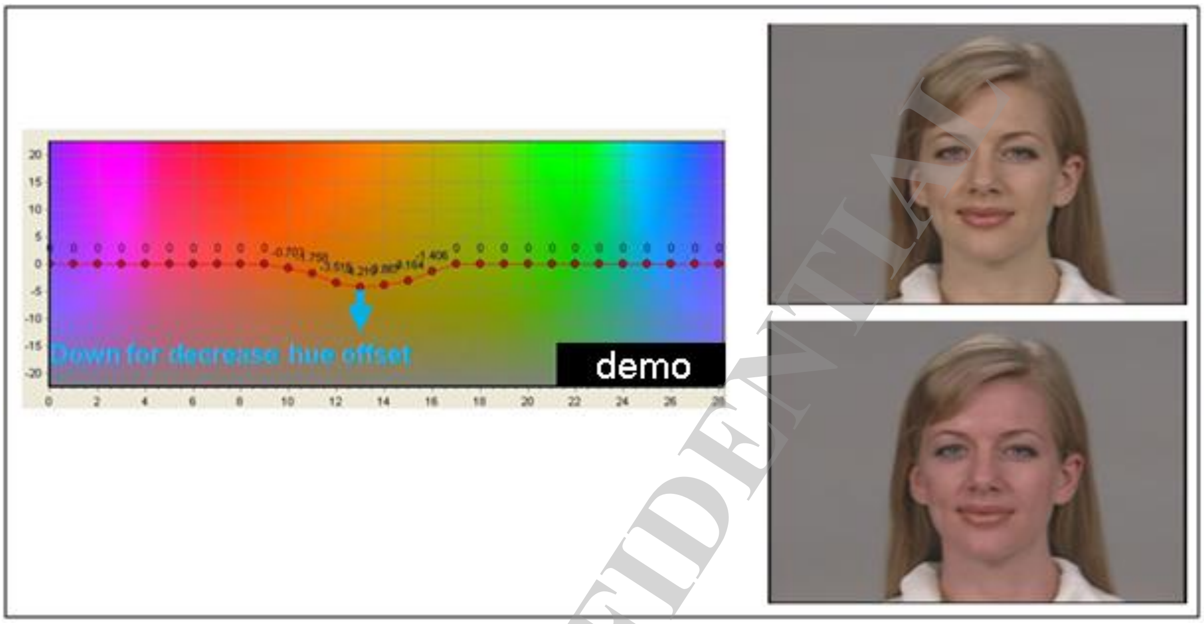

Figure 6-47. Partial hue adjustment example

6.14.5.2 Luma Adjustment

Global contrast and brightness adjustment are also provided for intuitive luma adjustment. The registers are G_CONTRAST and G_BRIGHTNESS (see Figure 6-48).

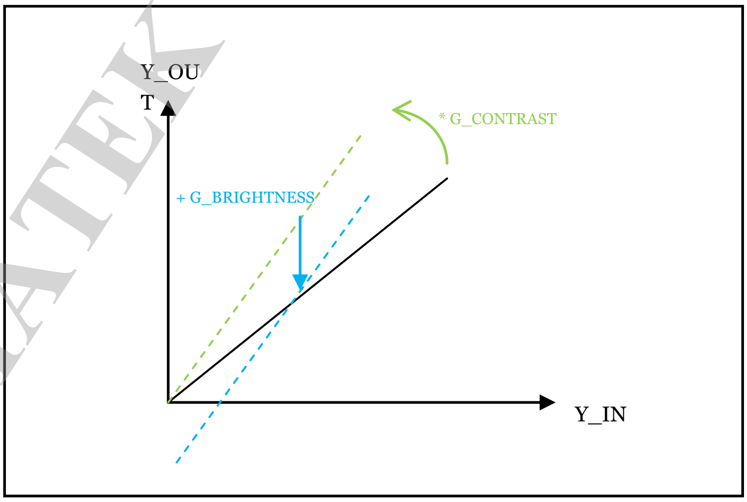

Figure 6-48. Contrast/brightness adjustment example

6.14.5.3 Saturation Adjustment

In human vision system, luminance increase results in pale images even the saturation is not decreased. Therefore, the color processor provides a "Chroma Boost" mechanism to detect the

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luminance increasing amount and decides the corresponding saturation boost level. The control registers are *_CBOOST_*, and the formula is illustrated in Figure 6-49.

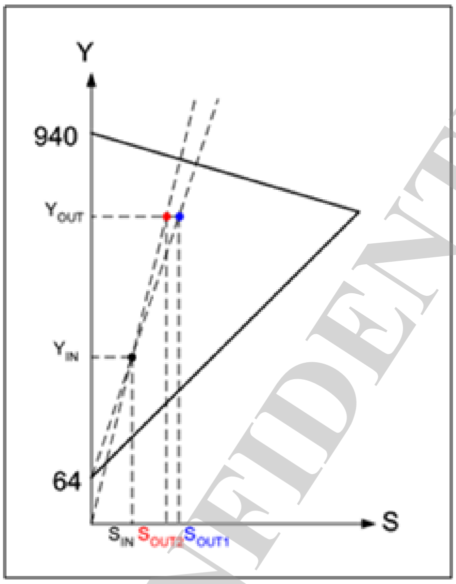

Figure 6-49. Chroma boost demonstration

For saturation adjustment, the color processor provides a flexible partial saturation adjustment. Similar to PartialHue, the hue plan is equally divided into 20 hue phases and saturation corresponding to each hue phase can be customized by three gains and two turning points. The adjustment for each hue phase are controlled by PARTIAL_SAT_GAIN*, PARTIAL_SAT_POINT*. Figure 6-50 shows the saturation adjustment in one hue phase.

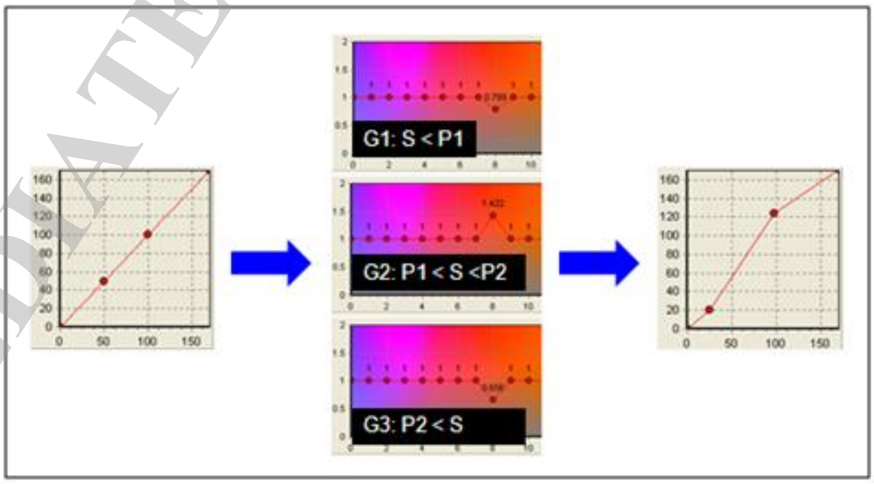

Figure 6-50. Example of partial S adjustment for one hue phase

A global saturation gain is provided for intuitive saturation adjustment. The control register is G_SATURATION (see Figure 6-51).

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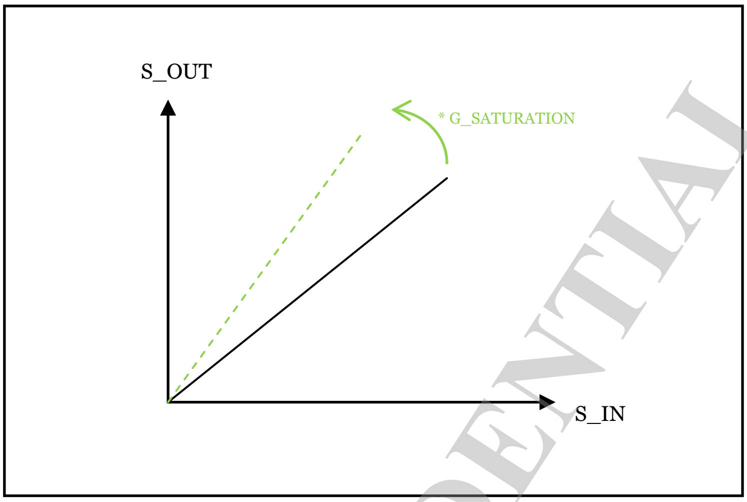

Figure 6-51. Illustration of global saturation adjustment

6.14.5.4 Color Matrix Conversion Programming

The color engine is equipped with input/output color matrix conversions. This makes possible that the color engine can operate in selectable processing stage. For example, the color engine can operate by RDMA engine's RGB or YCbCr outputs.

If RGB data are fed to the color engine, RGB to YCbCr conversion should be performed before color processing, and YCbCr to RGB conversion can be applied to the following engines.

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6.15 DISP CCORR (Display Color Correction Engine)

6.15.1 Introduction

The color correction engine changes the overall mixture of RGB colors to fit the characteristics of target panel.

6.15.2 Features

- Fixed-coefficient inverse gamma table with wide-gamut support
- Programmable 3X3 matrix
- Fixed-coefficient gamma table

6.15.3 Block Diagram

Figure 6-52 is the block diagram of color correction core.

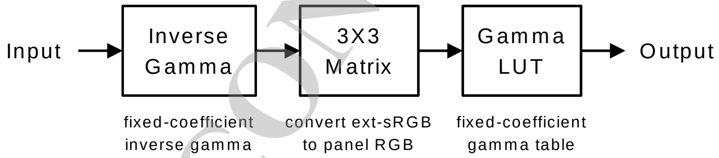
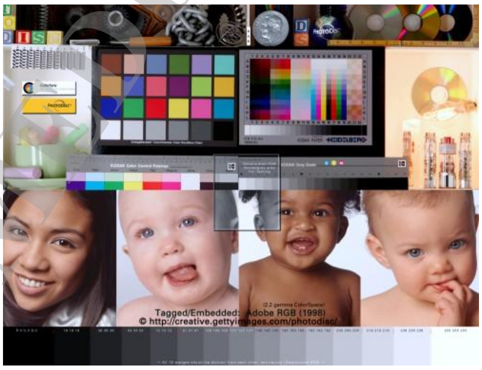


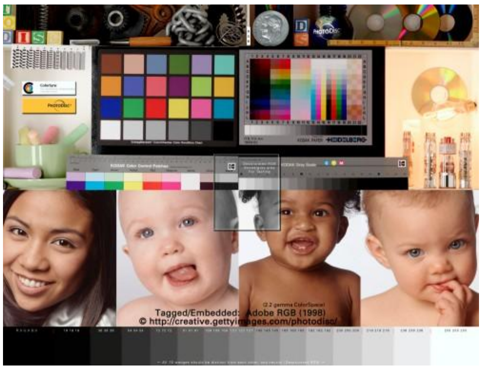
Figure 6-52. Block diagram of color correction

6.15.4 Color Correction

In order to display accurate image colors, the panel needs to match the standard sRGB color gamut. However, most LCD panels only display 65 to 80 percent of the sRGB color gamut. The OLED panels, on the other hand, can display over 130 percent of sRGB color gamut. With color correction, you can reproduce correct color on panels with different color gamuts.



Wide-gamut panel without color correction



Wide-gamut panel with color correction

Figure 6-53. Visual effect of color correction

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6.15.5 Register Definition

Module name: DISP_CCORR Base address: (+1400C000h)

Address	Name	Width	Register Function
1400C000	DISP_CCORR_EN	32	CCORR Enable Register
1400C004	DISP_CCORR_RESET	32	CCORR Reset Register
1400C008	DISP_CCORR_INTEN	32	CCORR Interrupt Enable Register
1400C00C	DISP_CCORR_INTSTA	32	CCORR Interrupt Status Register
1400C010	DISP_CCORR_STATUS	32	CCORR Status Register
1400C020	DISP_CCORR_CFG	32	CCORR Configuration Register
1400C024	DISP_CCORR_INPUT_COUNT	32	CCORR Input Count Register
1400C028	DISP_CCORR_OUTPUT_COUNT	32	CCORR Output Count Register
1400C02C	DISP_CCORR_CHKSUM	32	CCORR Checksum Register
1400C030	DISP_CCORR_SIZE	32	CCORR Size Register
1400C080	DISP_CCORR_COEF_0	32	CCORR Color Coefficient 0
1400C084	DISP_CCORR_COEF_1	32	CCORR Color Coefficient 1
1400C088	DISP_CCORR_COEF_2	32	CCORR Color Coefficient 2
1400C08C	DISP_CCORR_COEF_3	32	CCORR Color Coefficient 3
1400C090	DISP_CCORR_COEF_4	32	CCORR Color Coefficient 4
1400C0C0	DISP_CCORR_DUMMY_REG	32	CCORR Dummy Register

1400C000 DISP_CCORR_EN CCORR Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CCORR_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	CCORR_EN	**Enables CCORR** 0: Disable 1: Enable

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1400C004 **DISP_CCORR_RESET** **CCORR Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CCORR_RESET
Type																RW
Reset																0

Bit(s)	Name	Description
0	CCORR_RESET	**Software reset** 0: De-assert software reset 1: Assert software reset

1400C008 **DISP_CCORR_INTEN** **CCORR Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															OF_END_INT_EN	IF_END_INT_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	OF_END_INT_EN	**Enables output frame end interrupt** 0: Disable 1: Enable
0	IF_END_INT_EN	**Enables input frame end interrupt** 0: Disable 1: Enable

1400C00C **DISP_CCORR_INTSTA** **CCORR Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															OF_END_INT	IF_END_INT
Type															Other	Other
Reset															0	0

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Bit(s)	Name	Description
1	OF_END_INT	**Output frame end interrupt status** 1: Output frame end (write 0 to clear)
0	IF_END_INT	**Input frame end interrupt status** 1: Input frame end (write 0 to clear)

1400C010 DISP_CCORR_STATUS CCORR Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					HANDSHAKE[23:12]											
Type					RU											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	HANDSHAKE[11:0]														OF_UNFINISH	IF_UNFINISH
Type	RU														Other	Other
Reset	0	0	0	0	0	0	0	0	0	0	0	0			0	0

Bit(s)	Name	Description
27:4	HANDSHAKE	**Handshake signals for debugging**
1	OF_UNFINISH	**Output frame unfinished but EOF arrives** 0: Normal 1: Output frame unfinished (write 0 to clear)
0	IF_UNFINISH	**Input frame unfinished but EOF arrives** 0: Normal 1: Input frame unfinished (write 0 to clear)

1400C020 DISP_CCORR_CFG CCORR Configuration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CHKSUM_SEL		CHKSUM_EN												
Type		RW		RW												
Reset		0	0	0												
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name														CCORR_GAMMA_OFF	CCORR_ENGINE_EN	RELAY_MODE
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
30:29	CHKSUM_SEL	**Selects checksum source** 0: Output 1: Input
28	CHKSUM_EN	**Enables checksum** 0: Disable 1: Enable

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Bit(s)	Name	Description
2	CCORR_GAMMA_OFF	**Enables color correction without Gamma** 0: Disable 1: Enable
1	CCORR_ENGINE_EN	**Enables color correction** 0: Disable 1: Enable
0	RELAY_MODE	**Switches to RELAY mode** 0: Disable 1: Enable

1400C024 **DISP_CCORR_INPUT_COUNT** **CCORR Input Count Register** **00010001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				INP_LINE_CNT												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				INP_PIX_CNT												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
28:16	INP_LINE_CNT	Input frame line counter
12:0	INP_PIX_CNT	Input frame pixel counter

1400C028 **DISP_CCORR_OUTPUT_COUNT** **CCORR Output Count Register** **00010001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				OUTP_LINE_CNT												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OUTP_PIX_CNT												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
28:16	OUTP_LINE_CNT	Output frame line counter
12:0	OUTP_PIX_CNT	Output frame pixel counter

1400C02C **DISP_CCORR_CHKSUM** **CCORR Checksum Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			CHKSUM[29:16]													
Type			RU													

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Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CHKSUM[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:0	CHKSUM	Checksum

1400C030 **DISP_CCORR_SIZE** **CCORR Size Register** **01E00320**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**HSIZE**												
Type				RW												
Reset				0	0	0	0	1	1	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**VSIZE**												
Type				RW												
Reset				0	0	0	1	1	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
28:16	HSIZE	Active width
12:0	VSIZE	Active height

1400C080 **DISP_CCORR_COEF_0** **CCORR Color Coefficient 0** **04000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**CCORR_C00**											
Type					RW											
Reset					0	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**CCORR_C01**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	CCORR_C00	Color coefficient C00
11:0	CCORR_C01	Color coefficient C01

1400C084 **DISP_CCORR_COEF_1** **CCORR Color Coefficient 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**CCORR_C02**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**CCORR_C10**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
27:16	CCORR_C02	Color coefficient C02
11:0	CCORR_C10	Color coefficient C10

1400C088 DISP_CCORR_COEF_2 CCORR Color Coefficient 2 04000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CCORR_C11											
Type					RW											
Reset					0	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CCORR_C12											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	CCORR_C11	Color coefficient C11
11:0	CCORR_C12	Color coefficient C12

1400C08C DISP_CCORR_COEF_3 CCORR Color Coefficient 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CCORR_C20											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CCORR_C21											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	CCORR_C20	Color coefficient C20
11:0	CCORR_C21	Color coefficient C21

1400C090 DISP_CCORR_COEF_4 CCORR Color Coefficient 4 04000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CCORR_C22											
Type					RW											
Reset					0	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
27:16	CCORR_C22	Color coefficient C22

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1400C0C0	DISP_CCORR_DUMMY_REG	CCORR Dummy Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY_REG[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY_REG[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DUMMY_REG	Dummy register

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6.16 DISP AAL (Display Adaptive Ambient Light Controller)

6.16.1 Introduction

The AAL processor, composed of content adaptive and ambient light adaptive, is responsible for backlight power saving and sunlight visibility improvement.

6.16.2 Features

- 33-bin weighted histogram
- DRE enhancement for sunlight visibility
- CABC compensation for backlight power saving

6.16.3 Block Diagram

Figure 6-54 is the block diagram of AAL processor.

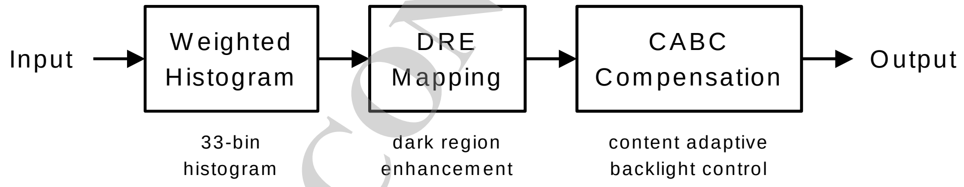

Figure 6-54. Block diagram of AAL processor

6.16.4 DRE Enhancement

Dark region enhancement improves the visibility under sunlight.

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Without DRE enhancement — With DRE enhancement

Figure 6-55.Visual effect of DRE enhancement

6.16.5 Register Definition

Module name: DISP_AAL Base address: (+1400D000h)

Address	Name	Width	Register Function
1400D000	DISP_AAL_EN	32	AAL Enable Register
1400D004	DISP_AAL_RESET	32	AAL Reset Register
1400D008	DISP_AAL_INTEN	32	AAL Interrupt Enable Register
1400D00C	DISP_AAL_INTSTA	32	AAL Interrupt Status Register
1400D010	DISP_AAL_STATUS	32	AAL Status Register
1400D020	DISP_AAL_CFG	32	AAL Configuration Register
1400D024	DISP_AAL_INPUT_COUNT	32	AAL Input Count Register
1400D028	DISP_AAL_OUTPUT_COUNT	32	AAL Output Count Register
1400D02C	DISP_AAL_CHKSUM	32	AAL Checksum Register
1400D030	DISP_AAL_SIZE	32	AAL Size Register
1400D0C0	DISP_AAL_DUMMY_REG	32	AAL Dummy Register
1400D204	DISP_AAL_MAX_HIST_CONFIG_00	32	
1400D20C	DISP_AAL_CABC_00	32	
1400D214	DISP_AAL_CABC_02	32	
1400D21C	DISP_AAL_CABC_04	32	

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Address	Name	Width	Register Function
1400D224	DISP_AAL_STATUS_00	32	
1400D228	DISP_AAL_STATUS_01	32	
1400D22C	DISP_AAL_STATUS_02	32	
1400D230	DISP_AAL_STATUS_03	32	
1400D234	DISP_AAL_STATUS_04	32	
1400D238	DISP_AAL_STATUS_05	32	
1400D23C	DISP_AAL_STATUS_06	32	
1400D240	DISP_AAL_STATUS_07	32	
1400D244	DISP_AAL_STATUS_08	32	
1400D248	DISP_AAL_STATUS_09	32	
1400D24C	DISP_AAL_STATUS_10	32	
1400D250	DISP_AAL_STATUS_11	32	
1400D254	DISP_AAL_STATUS_12	32	
1400D258	DISP_AAL_STATUS_13	32	
1400D25C	DISP_AAL_STATUS_14	32	
1400D260	DISP_AAL_STATUS_15	32	
1400D264	DISP_AAL_STATUS_16	32	
1400D268	DISP_AAL_STATUS_17	32	
1400D26C	DISP_AAL_STATUS_18	32	
1400D270	DISP_AAL_STATUS_19	32	
1400D274	DISP_AAL_STATUS_20	32	
1400D278	DISP_AAL_STATUS_21	32	
1400D27C	DISP_AAL_STATUS_22	32	
1400D280	DISP_AAL_STATUS_23	32	
1400D284	DISP_AAL_STATUS_24	32	
1400D288	DISP_AAL_STATUS_25	32	
1400D28C	DISP_AAL_STATUS_26	32	
1400D290	DISP_AAL_STATUS_27	32	

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Address	Name	Width	Register Function
1400D294	DISP_AAL_STATUS_28	32	
1400D298	DISP_AAL_STATUS_29	32	
1400D29C	DISP_AAL_STATUS_30	32	
1400D2A0	DISP_AAL_STATUS_31	32	
1400D2A4	DISP_AAL_STATUS_32	32	
1400D358	DISP_AAL_DRE_FLT_FORCE_00	32	
1400D35C	DISP_AAL_DRE_FLT_FORCE_01	32	
1400D360	DISP_AAL_DRE_FLT_FORCE_02	32	
1400D364	DISP_AAL_DRE_FLT_FORCE_03	32	
1400D368	DISP_AAL_DRE_FLT_FORCE_04	32	
1400D36C	DISP_AAL_DRE_FLT_FORCE_05	32	
1400D370	DISP_AAL_DRE_FLT_FORCE_06	32	
1400D374	DISP_AAL_DRE_FLT_FORCE_07	32	
1400D378	DISP_AAL_DRE_FLT_FORCE_08	32	
1400D37C	DISP_AAL_DRE_FLT_FORCE_09	32	
1400D380	DISP_AAL_DRE_FLT_FORCE_10	32	
1400D3B0	DISP_AAL_DRE_MAPPING_00	32	
1400D40C	DISP_AAL_CABC_GAINLMT_TBL_00	32	
1400D410	DISP_AAL_CABC_GAINLMT_TBL_01	32	
1400D414	DISP_AAL_CABC_GAINLMT_TBL_02	32	
1400D418	DISP_AAL_CABC_GAINLMT_TBL_03	32	
1400D41C	DISP_AAL_CABC_GAINLMT_TBL_04	32	
1400D420	DISP_AAL_CABC_GAINLMT_TBL_05	32	
1400D424	DISP_AAL_CABC_GAINLMT_TBL_06	32	
1400D428	DISP_AAL_CABC_GAINLMT_TBL_07	32	
1400D42C	DISP_AAL_CABC_GAINLMT_TBL_08	32	
1400D430	DISP_AAL_CABC_GAINLMT_TBL_09	32	
1400D434	DISP_AAL_CABC_GAINLMT_TBL_10	32	

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1400D000 DISP_AAL_EN AAL Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																AAL_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	AAL_EN	**Enables AAL** 0: Disable 1: Enable

1400D004 DISP_AAL_RESET AAL Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																AAL_RESET
Type																RW
Reset																0

Bit(s)	Name	Description
0	AAL_RESET	**Software reset** 0: De-assert software reset 1: Assert software reset

1400D008 DISP_AAL_INTEN AAL Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															OF_END_INT_EN	IF_END_INT_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
1	OF_END_INT_EN	**Enables output frame end interrupt** 0: Disable 1: Enable
0	IF_END_INT_EN	**Enables input frame end interrupt** 0: Disable 1: Enable

1400D00C **DISP_AAL_INTSTA** **AAL Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**OF_END_INT**	**IF_END_INT**
Type															Other	Other
Reset															0	0

Bit(s)	Name	Description
1	OF_END_INT	**Output frame end interrupt status** 1: Output frame end (write 0 to clear)
0	IF_END_INT	**Input frame end interrupt status** 1: Input frame end (write 0 to clear)

1400D010 **DISP_AAL_STATUS** **AAL Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					HANDSHAKE[23:12]											
Type					RU											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HANDSHAKE[11:0]														**OF_UNFINISH**	**IF_UNFINISH**
Type	RU														Other	Other
Reset	0	0	0	0	0	0	0	0	0	0	0	0			0	0

Bit(s)	Name	Description
27:4	HANDSHAKE	**Handshake signals for debugging**
1	OF_UNFINISH	**Output frame unfinished but EOF arrives** 0: Normal 1: Output frame unfinished (write 0 to clear)
0	IF_UNFINISH	**Input frame unfinished but EOF arrives** 0: Normal 1: Input frame unfinished (write 0 to clear)

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1400D020 DISP_AAL_CFG AAL Configuration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CHKSUM_SEL		CHKSUM_EN												
Type		RW		RW												
Reset		0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													AAL_HIST_LOCK	AAL_HIST_EN	AAL_ENGINE_EN	RELAY_MODE
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
30:29	CHKSUM_SEL	**Selects checksum source** 0: Output 1: Input
28	CHKSUM_EN	**Enables checksum** 0: Disable 1: Enable
3	AAL_HIST_LOCK	**Locks AAL histogram** 0: Disable 1: Enable
2	AAL_HIST_EN	**Enables AAL histogram** 0: Disable 1: Enable
1	AAL_ENGINE_EN	**Enables AAL engine** 0: Disable 1: Enable
0	RELAY_MODE	**Switches to RELAY mode** 0: Disable 1: Enable

1400D024 DISP_AAL_INPUT_COUNT AAL Input Count Register 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				INP_LINE_CNT												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				INP_PIX_CNT												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
28:16	INP_LINE_CNT	Input frame line counter
12:0	INP_PIX_CNT	Input frame pixel counter

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1400D028 DISP_AAL_OUTPUT_COUNT AAL Output Count Register 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				OUTP_LINE_CNT												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OUTP_PIX_CNT												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
28:16	OUTP_LINE_CNT	Output frame line counter
12:0	OUTP_PIX_CNT	Output frame pixel counter

1400D02C DISP_AAL_CHKSUM AAL Checksum Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						CHKSUM[26:16]										
Type						RU										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKSUM[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	CHKSUM	Checksum

1400D030 DISP_AAL_SIZE AAL Size Register 01E00320

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				HSIZE												
Type				RW												
Reset				0	0	0	0	1	1	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VSIZE												
Type				RW												
Reset				0	0	0	1	1	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
28:16	HSIZE	Active width
12:0	VSIZE	Active height

1400D0C0 DISP_AAL_DUMMY_REG AAL Dummy Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	DUMMY_REG[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY_REG[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DUMMY_REG	Dummy register

1400D204 **DISP_AAL_MAX_HIST_CONFIG_00** **00080000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													aal_maxhist_rgb_weight			
Type													RW			
Reset													1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
19:16	aal_maxhist_rgb_weight	

1400D20C **DISP_AAL_CABC_00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	cabc_en															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31	cabc_en	

1400D214 **DISP_AAL_CABC_02** **00000100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name							**cabc_fltgain_force**									
Type							RW									
Reset							0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	cabc_fltgain_force	

1400D21C **DISP_AAL_CABC_04** **07FFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**cabc_ink**					**cabc_out_b_force**									**cabc_out_g_force[8:7]**	
Type	RW					RW									RW	
Reset	0					1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**cabc_out_g_force[6:0]**							**cabc_out_r_force**								
Type	RW							RW								
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31	cabc_ink	
26:18	cabc_out_b_force	
17:9	cabc_out_g_force	
8:0	cabc_out_r_force	

1400D224 **DISP_AAL_STATUS_00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											**aal_max_hist_00[21:16]**					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**aal_max_hist_00[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_00	

1400D228 **DISP_AAL_STATUS_01** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											**aal_max_hist_01[21:16]**					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**aal_max_hist_01[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
21:0	aal_max_hist_01	

1400D22C **DISP_AAL_STATUS_02** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_02[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aal_max_hist_02[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_02	

1400D230 **DISP_AAL_STATUS_03** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_03[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aal_max_hist_03[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_03	

1400D234 **DISP_AAL_STATUS_04** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_04[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aal_max_hist_04[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_04	

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1400D238 **DISP_AAL_STATUS_05** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_05[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aal_max_hist_05[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_05	

1400D23C **DISP_AAL_STATUS_06** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_06[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aal_max_hist_06[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_06	

1400D240 **DISP_AAL_STATUS_07** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_07[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aal_max_hist_07[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_07	

1400D244 **DISP_AAL_STATUS_08** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_08[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	aal_max_hist_08[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_08	

1400D248 DISP_AAL_STATUS_09 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_09[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aal_max_hist_09[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_09	

1400D24C DISP_AAL_STATUS_10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_10[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aal_max_hist_10[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_10	

1400D250 DISP_AAL_STATUS_11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_11[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aal_max_hist_11[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_11	

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1400D254 **DISP_AAL_STATUS_12** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_12[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aal_max_hist_12[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_12	

1400D258 **DISP_AAL_STATUS_13** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_13[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aal_max_hist_13[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_13	

1400D25C **DISP_AAL_STATUS_14** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_14[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aal_max_hist_14[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_14	

1400D260 **DISP_AAL_STATUS_15** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_15[21:16]					
Type											RU					
Reset											0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aal_max_hist_15[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_15	

1400D264 **DISP_AAL_STATUS_16** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_16[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aal_max_hist_16[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_16	

1400D268 **DISP_AAL_STATUS_17** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_17[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aal_max_hist_17[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_17	

1400D26C **DISP_AAL_STATUS_18** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_18[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aal_max_hist_18[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_18	

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1400D270 **DISP_AAL_STATUS_19** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_19[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aal_max_hist_19[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_19	

1400D274 **DISP_AAL_STATUS_20** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_20[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aal_max_hist_20[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_20	

1400D278 **DISP_AAL_STATUS_21** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_21[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aal_max_hist_21[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_21	

1400D27C **DISP_AAL_STATUS_22** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_22[21:16]					

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Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**aal_max_hist_22[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_22	

1400D280 DISP_AAL_STATUS_23 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											**aal_max_hist_23[21:16]**					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**aal_max_hist_23[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_23	

1400D284 DISP_AAL_STATUS_24 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											**aal_max_hist_24[21:16]**					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**aal_max_hist_24[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_24	

1400D288 DISP_AAL_STATUS_25 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											**aal_max_hist_25[21:16]**					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**aal_max_hist_25[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
21:0	aal_max_hist_25	

1400D28C **DISP_AAL_STATUS_26** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_26[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aal_max_hist_26[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_26	

1400D290 **DISP_AAL_STATUS_27** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_27[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aal_max_hist_27[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_27	

1400D294 **DISP_AAL_STATUS_28** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_28[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aal_max_hist_28[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_28	

1400D298 **DISP_AAL_ST** **00000000**

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ATUS_29

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_29[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aal_max_hist_29[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_29	

1400D29C **DISP_AAL_STATUS_30** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_30[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aal_max_hist_30[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_30	

1400D2A0 **DISP_AAL_STATUS_31** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_31[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aal_max_hist_31[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	aal_max_hist_31	

1400D2A4 **DISP_AAL_STATUS_32** **003FFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											aal_max_hist_32[21:16]					
Type											RU					
Reset											1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aal_max_hist_32[15:0]															
Type	RU															

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Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
21:0	aal_max_hist_32	

1400D358 **DISP_AAL_DRE_FLT_FORCE_00** **00100100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									**dre_gain_flt_01_force[11:4]**							
Type									RW							
Reset									0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**dre_gain_flt_01_force[3:0]**				**dre_gain_flt_00_force**											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:12	dre_gain_flt_01_force	
11:0	dre_gain_flt_00_force	

1400D35C **DISP_AAL_DRE_FLT_FORCE_01** **00100100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										**dre_gain_flt_03_force[10:4]**						
Type										RW						
Reset										0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**dre_gain_flt_03_force[3:0]**				**dre_gain_flt_02_force**											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
22:12	dre_gain_flt_03_force	
11:0	dre_gain_flt_02_force	

1400D360 **DISP_AAL_DRE_FLT_FORCE_02** **00080100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											**dre_gain_flt_05_force[10:5]**					
Type											RW					
Reset											0	0	1	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dre_gain_flt_05_force[4:0]					dre_gain_flt_04_force										
Type	RW					RW										
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:11	dre_gain_flt_05_force	
10:0	dre_gain_flt_04_force	

1400D364 DISP_AAL_DRE_FLT_FORCE_03 20080100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		dre_gain_flt_08_force										dre_gain_flt_07_force[9:5]				
Type		RW										RW				
Reset		0	1	0	0	0	0	0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dre_gain_flt_07_force[4:0]					dre_gain_flt_06_force										
Type	RW					RW										
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:21	dre_gain_flt_08_force	
20:11	dre_gain_flt_07_force	
10:0	dre_gain_flt_06_force	

1400D368 DISP_AAL_DRE_FLT_FORCE_04 10040100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			dre_gain_flt_11_force										dre_gain_flt_10_force[9:6]			
Type			RW										RW			
Reset			0	1	0	0	0	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dre_gain_flt_10_force[5:0]						dre_gain_flt_09_force									
Type	RW						RW									
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:20	dre_gain_flt_11_force	
19:10	dre_gain_flt_10_force	
9:0	dre_gain_flt_09_force	

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1400D36C **DISP_AAL_DRE_FLT_FORCE_05** 10040100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			dre_gain_flt_14_force										dre_gain_flt_13_force[9:6]			
Type			RW										RW			
Reset			0	1	0	0	0	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dre_gain_flt_13_force[5:0]						dre_gain_flt_12_force									
Type	RW						RW									
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:20	dre_gain_flt_14_force	
19:10	dre_gain_flt_13_force	
9:0	dre_gain_flt_12_force	

1400D370 **DISP_AAL_DRE_FLT_FORCE_06** 10040100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			dre_gain_flt_17_force										dre_gain_flt_16_force[9:6]			
Type			RW										RW			
Reset			0	1	0	0	0	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dre_gain_flt_16_force[5:0]						dre_gain_flt_15_force									
Type	RW						RW									
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:20	dre_gain_flt_17_force	
19:10	dre_gain_flt_16_force	
9:0	dre_gain_flt_15_force	

1400D374 **DISP_AAL_DRE_FLT_FORCE_07** 04020100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						dre_gain_flt_20_force									dre_gain_flt_19_force[8:7]	
Type						RW									RW	
Reset						1	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dre_gain_flt_19_force[6:0]							dre_gain_flt_18_force								
Type	RW							RW								
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
26:18	dre_gain_flt_20_force	
17:9	dre_gain_flt_19_force	
8:0	dre_gain_flt_18_force	

1400D378 **DISP_AAL_DRE_FLT_FORCE_08** **04020100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						dre_gain_flt_23_force									dre_gain_flt_22_force[8:7]	
Type						RW									RW	
Reset						1	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dre_gain_flt_22_force[6:0]							dre_gain_flt_21_force								
Type	RW							RW								
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:18	dre_gain_flt_23_force	
17:9	dre_gain_flt_22_force	
8:0	dre_gain_flt_21_force	

1400D37C **DISP_AAL_DRE_FLT_FORCE_09** **04020100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						dre_gain_flt_26_force									dre_gain_flt_25_force[8:7]	
Type						RW									RW	
Reset						1	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dre_gain_flt_25_force[6:0]							dre_gain_flt_24_force								
Type	RW							RW								
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:18	dre_gain_flt_26_force	
17:9	dre_gain_flt_25_force	
8:0	dre_gain_flt_24_force	

1400D380 **DISP_AAL_DRE_FLT_FORCE_10** **00020100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name															**dre_gain_flt_28_force[8:7]**	
Type															RW	
Reset															1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**dre_gain_flt_28_force[6:0]**							**dre_gain_flt_27_force**								
Type	RW							RW								
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:9	dre_gain_flt_28_force	
8:0	dre_gain_flt_27_force	

1400D3B0 **DISP_AAL_DRE_MAPPING_00** **00000018**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**dre_map_bypass**	**dre_map_rgb_weight**			
Type												RW	RW			
Reset												1	1	0	0	0

Bit(s)	Name	Description
4	dre_map_bypass	
3:0	dre_map_rgb_weight	

1400D40C **DISP_AAL_CABC_GAINLMT_TBL_00** **3FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			**cabc_gainlmt_02**										**cabc_gainlmt_01[9:6]**			
Type			RW										RW			
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**cabc_gainlmt_01[5:0]**						**cabc_gainlmt_00**									
Type	RW						RW									
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
29:20	cabc_gainlmt_02	
19:10	cabc_gainlmt_01	
9:0	cabc_gainlmt_00	

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1400D410 DISP_AAL_CABC_GAINLMT_TBL_01 3FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			cabc_gainlmt_05										cabc_gainlmt_04[9:6]			
Type			RW										RW			
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cabc_gainlmt_04[5:0]						cabc_gainlmt_03									
Type	RW						RW									
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
29:20	cabc_gainlmt_05	
19:10	cabc_gainlmt_04	
9:0	cabc_gainlmt_03	

1400D414 DISP_AAL_CABC_GAINLMT_TBL_02 3FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			cabc_gainlmt_08										cabc_gainlmt_07[9:6]			
Type			RW										RW			
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cabc_gainlmt_07[5:0]						cabc_gainlmt_06									
Type	RW						RW									
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
29:20	cabc_gainlmt_08	
19:10	cabc_gainlmt_07	
9:0	cabc_gainlmt_06	

1400D418 DISP_AAL_CABC_GAINLMT_TBL_03 3FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			cabc_gainlmt_11										cabc_gainlmt_10[9:6]			
Type			RW										RW			
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cabc_gainlmt_10[5:0]						cabc_gainlmt_09									
Type	RW						RW									
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
29:20	cabc_gainlmt_11	
19:10	cabc_gainlmt_10	

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Bit(s)	Name	Description
9:0	cabc_gainlmt_09	

1400D41C **DISP_AAL_CABC_GAINLMT_TBL_04** **3FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			cabc_gainlmt_14										cabc_gainlmt_13[9:6]			
Type			RW										RW			
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cabc_gainlmt_13[5:0]						cabc_gainlmt_12									
Type	RW						RW									
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
29:20	cabc_gainlmt_14	
19:10	cabc_gainlmt_13	
9:0	cabc_gainlmt_12	

1400D420 **DISP_AAL_CABC_GAINLMT_TBL_05** **3FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			cabc_gainlmt_17										cabc_gainlmt_16[9:6]			
Type			RW										RW			
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cabc_gainlmt_16[5:0]						cabc_gainlmt_15									
Type	RW						RW									
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
29:20	cabc_gainlmt_17	
19:10	cabc_gainlmt_16	
9:0	cabc_gainlmt_15	

1400D424 **DISP_AAL_CABC_GAINLMT_TBL_06** **3FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			cabc_gainlmt_20										cabc_gainlmt_19[9:6]			
Type			RW										RW			
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cabc_gainlmt_19[5:0]						cabc_gainlmt_18									
Type	RW						RW									
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

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Bit(s)	Name	Description
29:20	cabc_gainlmt_20	
19:10	cabc_gainlmt_19	
9:0	cabc_gainlmt_18	

1400D428 **DISP_AAL_CABC_GAINLMT_TBL_07** **3FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			cabc_gainlmt_23										cabc_gainlmt_22[9:6]			
Type			RW										RW			
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cabc_gainlmt_22[5:0]						cabc_gainlmt_21									
Type	RW						RW									
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
29:20	cabc_gainlmt_23	
19:10	cabc_gainlmt_22	
9:0	cabc_gainlmt_21	

1400D42C **DISP_AAL_CABC_GAINLMT_TBL_08** **3FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			cabc_gainlmt_26										cabc_gainlmt_25[9:6]			
Type			RW										RW			
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cabc_gainlmt_25[5:0]						cabc_gainlmt_24									
Type	RW						RW									
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
29:20	cabc_gainlmt_26	
19:10	cabc_gainlmt_25	
9:0	cabc_gainlmt_24	

1400D430 **DISP_AAL_CABC_GAINLMT_TBL_09** **3FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			cabc_gainlmt_29										cabc_gainlmt_28[9:6]			
Type			RW										RW			
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cabc_gainlmt_28[5:0]						cabc_gainlmt_27									

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Type	RW						RW									
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
29:20	cabc_gainlmt_29	
19:10	cabc_gainlmt_28	
9:0	cabc_gainlmt_27	

1400D434 **DISP_AAL_CABC_GAINLMT_TBL_10** **3FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			**cabc_gainlmt_32**										**cabc_gainlmt_31[9:6]**			
Type			RW										RW			
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**cabc_gainlmt_31[5:0]**						**cabc_gainlmt_30**									
Type	RW						RW									
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
29:20	cabc_gainlmt_32	
19:10	cabc_gainlmt_31	
9:0	cabc_gainlmt_30	

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6.17 DISP GAMMA (Display GAMMA Processing Engine)

6.17.1 Introduction

The GAMMA engine changes the overall mixture of RGB colors to fit the characteristics of target panel.

6.17.2 Features

- 10-bit gamma table with 512 entries
- Non-block gamma LUT programming

6.17.3 Gamma correction

For accurate image reproduction, the transfer function of the panel should have a standard 2.20 gamma value. The gamma correction consists of three programmable look-up tables for RGB colors. It applies arbitrary mapping curve to compensate the incorrect transfer function of the panel.

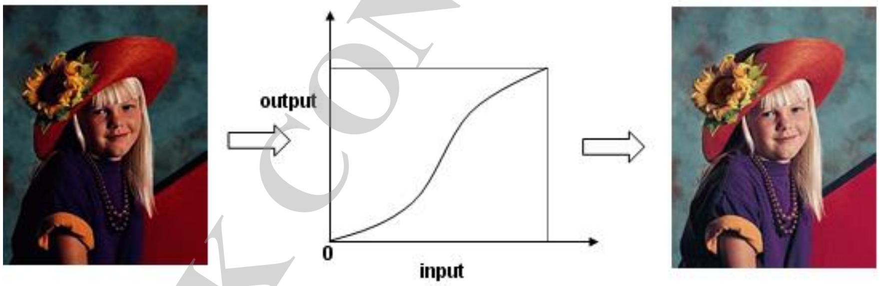

Figure 6-56. Visual effect of gamma correction

6.17.4 Register Definition

Module name: DISP_GAMMA Base address: (+1400E000h)

Address	Name	Width	Register Function
1400E000	DISP_GAMMA_EN	32	GAMMA Enable Register
1400E004	DISP_GAMMA_RESET	32	GAMMA Reset Register
1400E008	DISP_GAMMA_INTEN	32	GAMMA Interrupt Enable Register
1400E00C	DISP_GAMMA_INTSTA	32	GAMMA Interrupt Status Register
1400E010	DISP_GAMMA_STATUS	32	GAMMA Status Register
1400E020	DISP_GAMMA_CFG	32	GAMMA Configuration Register
1400E024	DISP_GAMMA_INPUT_COUNT	32	GAMMA Input Count Register
1400E028	DISP_GAMMA_OUTPUT_COUNT	32	GAMMA Output Count Register
1400E02C	DISP_GAMMA_CHKSUM	32	GAMMA Checksum Register

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Address	Name	Width	Register Function
1400E030	DISP_GAMMA_SIZE	32	GAMMA Size Register
1400E0C0	DISP_GAMMA_DUMMY_REG	32	GAMMA Dummy Register
1400E700 ~ 1400EEFC	DISP_GAMMA_LUT[n] (n=0~511)	32	GAMMA LUT Entries

1400E000 DISP_GAMMA_EN GAMMA Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																GAMMA_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	GAMMA_EN	**Enables GAMMA** 0: Disable 1: Enable

1400E004 DISP_GAMMA_RESET GAMMA Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																GAMMA_RESET
Type																RW
Reset																0

Bit(s)	Name	Description
0	GAMMA_RESET	**Software reset** 0: De-assert software reset 1: Assert software reset

1400E008 DISP_GAMMA_INTEN GAMMA Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name															OF_END_INT_EN	IF_END_INT_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	OF_END_INT_EN	**Enables output frame end interrupt** 0: Disable 1: Enable
0	IF_END_INT_EN	**Enables input frame end interrupt** 0: Disable 1: Enable

1400E00C DISP_GAMMA_INTSTA GAMMA Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															OF_END_INT	IF_END_INT
Type															Other	Other
Reset															0	0

Bit(s)	Name	Description
1	OF_END_INT	**Output frame end interrupt status** 1: Output frame end (write 0 to clear)
0	IF_END_INT	**Input frame end interrupt status** 1: Input frame end (write 0 to clear)

1400E010 DISP_GAMMA_STATUS GAMMA Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													HANDSHAKE[15:12]			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HANDSHAKE[11:0]														OF_UNFINISH	IF_UNFINISH
Type	RU														Other	Other
Reset	0	0	0	0	0	0	0	0	0	0	0	0			0	0

Bit(s)	Name	Description
19:4	HANDSHAKE	**Handshake signals for debugging**
1	OF_UNFINISH	**Output frame unfinished but EOF arrives** 0: Normal 1: Output frame unfinished (write 0 to clear)

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Bit(s)	Name	Description
0	IF_UNFINISH	**Input frame unfinished but EOF arrives** 0: Normal 1: Input frame unfinished (write 0 to clear)

1400E020 **DISP_GAMMA_CFG** **GAMMA Configuration Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CHKSUM_SEL		CHKSUM_EN												
Type		RW		RW												
Reset		0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															GAMMA_LUT_EN	RELAY_MODE
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
30:29	CHKSUM_SEL	**Selects checksum source** 0: Output 1: Input
28	CHKSUM_EN	**Enables checksum** 0: Disable 1: Enable
1	GAMMA_LUT_EN	**Enables gamma table** 0: Disable 1: Enable
0	RELAY_MODE	**Switches to RELAY mode** 0: Disable 1: Enable

1400E024 **DISP_GAMMA_INPUT_COUNT** **GAMMA Input Count Register** **00010001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				INP_LINE_CNT												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				INP_PIX_CNT												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
28:16	INP_LINE_CNT	Input frame line counter
12:0	INP_PIX_CNT	Input frame pixel counter

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1400E028 **DISP_GAMMA_OUTPUT_COUNT** **GAMMA Output Count Register** **00010001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				OUTP_LINE_CNT												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OUTP_PIX_CNT												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
28:16	OUTP_LINE_CNT	Output frame line counter
12:0	OUTP_PIX_CNT	Output frame pixel counter

1400E02C **DISP_GAMMA_CHKSUM** **GAMMA Checksum Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			CHKSUM[29:16]													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKSUM[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:0	CHKSUM	Checksum

1400E030 **DISP_GAMMA_SIZE** **GAMMA Size Register** **01E00320**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				HSIZE												
Type				RW												
Reset				0	0	0	0	1	1	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VSIZE												
Type				RW												
Reset				0	0	0	1	1	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
28:16	HSIZE	Active width
12:0	VSIZE	Active height

1400E0C0 **DISP_GAMMA_DUMMY_RE** **GAMMA Dummy Register** **00000000**

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G

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DUMMY_REG[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DUMMY_REG[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DUMMY_REG	Dummy register

1400E700~ 1400EEFC **DISP_GAMMA_LUT[n] (n=0~511)** **GAMMA LUT Entries** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			**GAMMA_LUT_R**										**GAMMA_LUT_G[9:6]**			
Type			RW										RW			
Reset			x	x	x	x	x	x	x	x	x	x	x	x	x	x
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**GAMMA_LUT_G[5:0]**						**GAMMA_LUT_B**									
Type	RW						RW									
Reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit(s)	Name	Description
29:20	GAMMA_LUT_R	9-bit to 10-bit gamma correction for R channel
19:10	GAMMA_LUT_G	9-bit to 10-bit gamma correction for G channel
9:0	GAMMA_LUT_B	9-bit to 10-bit gamma correction for B channel

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6.18 DISP Dither

6.18.1 Introduction

The dither engine decreases the RGB depth while migrating the loss of quality at the same time.

6.18.2 Register Definition

Module name: DISP_DITHER Base address: (+1400F000h)

Address	Name	Width	Register Function
1400F000	DISP_DITHER_EN	32	DITHER Enable Register
1400F004	DISP_DITHER_RESET	32	DITHER Reset Register
1400F008	DISP_DITHER_INTEN	32	DITHER Interrupt Enable Register
1400F00C	DISP_DITHER_INTSTA	32	DITHER Interrupt Status Register
1400F010	DISP_DITHER_STATUS	32	DITHER Status Register
1400F020	DISP_DITHER_CFG	32	DITHER Configuration Register
1400F024	DISP_DITHER_INPUT_COUNT	32	DITHER Input Count Register
1400F028	DISP_DITHER_OUTPUT_COUNT	32	DITHER Output Count Register
1400F02C	DISP_DITHER_CHKSUM	32	DITHER Checksum Register
1400F030	DISP_DITHER_SIZE	32	DITHER Size Register
1400F0C0	DISP_DITHER_DUMMY_REG	32	DITHER Dummy Register
1400F100	DISP_DITHER_0	32	DITHER Dither Setting 0
1400F114	DISP_DITHER_5	32	DITHER Dither Setting 5
1400F118	DISP_DITHER_6	32	DITHER Dither Setting 6
1400F11C	DISP_DITHER_7	32	DITHER Dither Setting 7
1400F120	DISP_DITHER_8	32	DITHER Dither Setting 8
1400F124	DISP_DITHER_9	32	DITHER Dither Setting 9
1400F128	DISP_DITHER_10	32	DITHER Dither Setting 10
1400F12C	DISP_DITHER_11	32	DITHER Dither Setting 11
1400F130	DISP_DITHER_12	32	DITHER Dither Setting 12
1400F134	DISP_DITHER_13	32	DITHER Dither Setting 13
1400F138	DISP_DITHER_14	32	DITHER Dither Setting 14
1400F13C	DISP_DITHER_15	32	DITHER Dither Setting 15
1400F140	DISP_DITHER_16	32	DITHER Dither Setting 16
1400F144	DISP_DITHER_17	32	DITHER Dither Setting 17

1400F000 DISP_DITHER_EN DITHER Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DITHER_E

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																N
Type																RW
Reset																0

Bit(s)	Name	Description
0	DITHER_EN	**Enables DITHER** 0: Disable 1: Enable

1400F004 DISP_DITHER_RESET DITHER Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DITHER_RESET
Type																RW
Reset																0

Bit(s)	Name	Description
0	DITHER_RESET	**Software reset** 0: De-assert software reset 1: Assert software reset

1400F008 DISP_DITHER_INTEN DITHER Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															OF_END_INT_EN	IF_END_INT_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	OF_END_INT_EN	**Enables output frame end interrupt** 0: Disable 1: Enable
0	IF_END_INT_EN	**Enables input frame end interrupt** 0: Disable 1: Enable

1400F00C DISP_DITHER DITHER Interrupt Status Register 00000000

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INTSTA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															OF_END_INT	IF_END_INT
Type															Other	Other
Reset															0	0

Bit(s)	Name	Description
1	OF_END_INT	**Output frame end interrupt status** 1: Output frame end (write 0 to clear)
0	IF_END_INT	**Input frame end interrupt status** 1: Input frame end (write 0 to clear)

1400F010 DISP_DITHER_STATUS DITHER Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													HANDSHAKE[15:12]			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HANDSHAKE[11:0]														OF_UNFINISH	IF_UNFINISH
Type	RU														Other	Other
Reset	0	0	0	0	0	0	0	0	0	0	0	0			0	0

Bit(s)	Name	Description
19:4	HANDSHAKE	**Handshake signals for debugging**
1	OF_UNFINISH	**Output frame unfinished but EOF arrives** 0: Normal 1: Output frame unfinished (write 0 to clear)
0	IF_UNFINISH	**Input frame unfinished but EOF arrives** 0: Normal 1: Input frame unfinished (write 0 to clear)

1400F020 DISP_DITHER_CFG DITHER Configuration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CHKSUM_SEL		CHKSUM_EN												
Type		RW		RW												
Reset		0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															DITHER_ENGINE_EN	RELAY_MODE

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Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
30:29	CHKSUM_SEL	**Selects checksum source** 0: Output 1: Input 2: After dithering
28	CHKSUM_EN	**Enables checksum** 0: Disable 1: Enable
1	DITHER_ENGINE_EN	**Enables dithering** 0: Disable 1: Enable
0	RELAY_MODE	**Switches to RELAY mode** 0: Disable 1: Enable

1400F024 **DISP_DITHER_INPUT_COUNT** **DITHER Input Count Register** **00010001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**INP_LINE_CNT**												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**INP_PIX_CNT**												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
28:16	INP_LINE_CNT	Input frame line counter
12:0	INP_PIX_CNT	Input frame pixel counter

1400F028 **DISP_DITHER_OUTPUT_COUNT** **DITHER Output Count Register** **00010001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**OUTP_LINE_CNT**												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**OUTP_PIX_CNT**												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
28:16	OUTP_LINE_CNT	Output frame line counter
12:0	OUTP_PIX_CNT	Output frame pixel counter

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1400F02C **DISP_DITHER_CHKSUM** **DITHER Checksum Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			**CHKSUM[29:16]**													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CHKSUM[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:0	CHKSUM	Checksum

1400F030 **DISP_DITHER_SIZE** **DITHER Size Register** **01E00320**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**HSIZE**												
Type				RW												
Reset				0	0	0	0	1	1	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**VSIZE**												
Type				RW												
Reset				0	0	0	1	1	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
28:16	HSIZE	Active width
12:0	VSIZE	Active height

1400F0C0 **DISP_DITHER_DUMMY_REG** **DITHER Dummy Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DUMMY_REG[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DUMMY_REG[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DUMMY_REG	Dummy register

1400F100 **DISP_DITHER_0** **DITHER Dither Setting 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name								crc_clr				crc_start				crc_cen
Type								RW				RW				RW
Reset								0				0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	frame_done_del											out_sel				
Type	RW											RW				
Reset	0	0	0	0	0	0	0	0				0				

Bit(s)	Name	Description
24	crc_clr	**Write 1 to clear CRC result.**
20	crc_start	**Write 1 to start CRC counting.**
16	crc_cen	**Enables CRC engine CG** 0: Disable 1: Enable
15:8	frame_done_del	**Frame done return delay**
4	out_sel	**Selects dither output** 0: Through dither 1: Bypass dither

1400F114 DISP_DITHER_5 DITHER Dither Setting 5 000000F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	w_demo															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bit(s)	Name	Description
15:0	w_demo	Short line length

1400F118 DISP_DITHER_6 DITHER Dither Setting 6 00003004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																wrap_mode
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	left_en		fphase_r	fphase_en			fphase						round_en	rdither_en	lfsr_en	edither_en
Type	RW		RW	RW			RW						RW	RW	RW	RW
Reset	0	0	1	1			0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
16	wrap_mode	**Enables 2-channel mode** 0: Disable

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Bit(s)	Name	Description
		1: Enable
15:14	left_en	**Enables left part of screen dither** 0: Dither run at full screen 1: Dither run at left part of screen
13	fphase_r	
12	fphase_en	**Enables running order dither frame phase control**
9:4	fphase	**Running order dither frame phase increment.** Note: 1. If ROUND_EN = 1, the output will only be rounded (no matter what RDITHER_EN and EDITHER_EN settings are). 2. RDITHER_EN and EDITHER_EN can work together.
3	round_en	**Enables rounding for dither function** When rounding method is used, both running order and error dispersion cannot be used.
2	rdither_en	**Enables running order dither** Running order dither must be set when ROUND_EN is set to 0. Running order dither can run with error dispersion when EDOTHER_EN is set to 1.
1	lfsr_en	**Enables LFSR-type dither**
0	edither_en	**Enables error dispersion dither** Error dispersion dither must be set when ROUND_EN is set to 0. Running order dither can run with error dispersion when RDITHER_EN is set to 1.

1400F11C **DISP_DITHER_7** **DITHER Dither Setting 7** **00000111**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							drmod_b				drmod_g				drmod_r	
Type							RW				RW				RW	
Reset							0	1			0	1			0	1

Bit(s)	Name	Description
9:8	drmod_b	**Selects dither mode for B channel** 0: No dither 1: 10-bit dither to 8-bit 2: 10-bit dither to 6-bit 3: 10-bit dither to 4-bit
5:4	drmod_g	**Selects dither mode for G channel** 0: No dither 1: 10-bit dither to 8-bit 2: 10-bit dither to 6-bit 3: 10-bit dither to 4-bit
1:0	drmod_r	**Selects dither mode for R channel** 0: No dither 1: 10-bit dither to 8-bit 2: 10-bit dither to 6-bit 3: 10-bit dither to 4-bit

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1400F120 **DISP_DITHER_8** **DITHER Dither Setting 8** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ink_data_r									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ink
Type																RW
Reset																0

Bit(s)	Name	Description
25:16	ink_data_r	Ink data for R
0	ink	Enables ink

1400F124 **DISP_DITHER_9** **DITHER Dither Setting 9** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ink_data_b									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							ink_data_g									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	ink_data_b	Ink data for B
9:0	ink_data_g	Ink data for G

1400F128 **DISP_DITHER_10** **DITHER Dither Setting 10** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						fphase_bit					fphase_sel				fphase_ctrl	
Type						RW					RW				RW	
Reset						0	0	0			0	0			0	0

Bit(s)	Name	Description
10:8	fphase_bit	**fphase_bit XOR bus number** Note: This function checks reg_fphase_sel. Only 0, 1, 2, 4 and 6 are available. 0: No effect on fphase (XOR disabled)
5:4	fphase_sel	**fphase XOR function: fphase does self bit-wise xor.** Note: This function checks reg_fphase_sel. Only bit 2, bit 4 and bit 6 are available. 0: Disable fphase XOR 1: Effect fphase[0]~[1] based on the value of reg_fphase_sel is 1 or 2

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Bit(s)	Name	Description
		2: Effect fphase[0]~[3] based on the value of reg_fphase_sel is 1, 2 or 4 3: Effect fphase[0]~[5] based on the value of reg_fphase_sel is 1, 2, 4 or 6
1:0	fphase_ctrl	**Selects fphase range add with rdither table** 00: 0~63 01: 0~16 10: 0~3

1400F12C <u>DISP_DITHER_11</u> DITHER Dither Setting 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**sub_b**				**sub_g**				**sub_r**					**subpix_en**
Type			RW				RW				RW					RW
Reset			0	0			0	0			0	0				0

Bit(s)	Name	Description
13:12	sub_b	
9:8	sub_g	
5:4	sub_r	
0	subpix_en	**Enables sub-pixel dither mode** 0: Disable 1: Enable

1400F130 <u>DISP_DITHER_12</u> DITHER Dither Setting 12 00000011

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**h_active**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											**table_en**					**lsb_off**
Type											RW					RW
Reset											0	1				1

Bit(s)	Name	Description
31:16	h_active	**Reserved**
5:4	table_en	**Active bit of magic table for running order** 01: Phase active in bit3 ~ bit0 10: Phase active in bit1 ~ bit0 Others: Phase active in bit5 ~ bit0
0	lsb_off	**Turns off LSB for dither function**

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1400F134 **DISP_DITHER_13** **DITHER Dither Setting 13** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**rshift_b**				**rshift_g**				**rshift_r**		
Type						RW				RW				RW		
Reset						0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
10:8	rshift_b	
6:4	rshift_g	
2:0	rshift_r	

1400F138 **DISP_DITHER_14** **DITHER Dither Setting 14** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**debug_mode**			**diff_shift**						**testpin_en**
Type							RW			RW						RW
Reset							0	0		0	0	0				0

Bit(s)	Name	Description
9:8	debug_mode	**Enables debugging mode** 0: Disable 1: Enable
6:4	diff_shift	**Debugging mode difference shift positions**
0	testpin_en	**Enables testpin input**

1400F13C **DISP_DITHER_15** **DITHER Dither Setting 15** **20200001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**lsb_err_shift_r**				**ovflw_bit_r**				**add_lshift_r**				**input_rshift_r**		
Type		RW				RW				RW				RW		
Reset		0	1	0		0	0	0		0	1	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**new_bit_mode**
Type																RW
Reset																1

Bit(s)	Name	Description
30:28	lsb_err_shift_r	**Selects RED LSB error bit**

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Bit(s)	Name	Description
26:24	ovflw_bit_r	**Selects RED overflow bit**
22:20	add_lshift_r	
18:16	input_rshift_r	
0	new_bit_mode	**Enables modified test algorithm** 0: Disable 1: Enable

1400F140 **DISP_DITHER_16** **DITHER Dither Setting 16** **20202020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**lsb_err_shift_b**				**ovflw_bit_b**				**add_lshift_b**				**input_rshift_b**		
Type		RW				RW				RW				RW		
Reset		0	1	0		0	0	0		0	1	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**lsb_err_shift_g**				**ovflw_bit_g**				**add_lshift_g**				**input_rshift_g**		
Type		RW				RW				RW				RW		
Reset		0	1	0		0	0	0		0	1	0		0	0	0

Bit(s)	Name	Description
30:28	lsb_err_shift_b	Selects GREEN LSB error bit
26:24	ovflw_bit_b	Selects GREEN overflow bit
22:20	add_lshift_b	
18:16	input_rshift_b	
14:12	lsb_err_shift_g	Selects BLUE LSB error bit
10:8	ovflw_bit_g	Selects BLUE overflow bit
6:4	add_lshift_g	BLUE addend left shift bits
2:0	input_rshift_g	BLUE input right shift bits

1400F144 **DISP_DITHER_17** **DITHER Dither Setting 17** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**crc_rdy**
Type																RU
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**crc_out**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	crc_rdy	CRC ready
15:0	crc_out	CRC result

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6.19 DISPLAY PWM Generator

6.19.1 Introduction

The PWM generator provides PWM signals for the LED driver of mobile LCM.

6.19.2 Features

- Operating clock: 26MHz (default) or 104MHz
- Gradual PWM control

6.19.3 Register Definition

Module name: DISP_PWM Base address: (+1100E000h)

Address	Name	Width	Register Function
1100E000	DISP_PWM_EN	32	**PWM Enable** Enables PWM
1100E004	DISP_PWM_RST	32	**PWM Reset** Resets PWM
1100E008	DISP_PWM_COMMIT	32	**PWM Commit** Commits PWM
1100E010	DISP_PWM_CON_0	32	**PWM Control 0** PWM control 0
1100E014	DISP_PWM_CON_1	32	**PWM Control 1** PWM control 1
1100E018	DISP_PWM_GRADUAL	32	**PWM Gradual Control** PWM gradual control
1100E01C	DISP_PWM_GRADUAL_RO	32	**PWM Gradual Control Output** PWM gradual control output
1100E020	DISP_PWM_DEBUG	32	**PWM Debug Register** PWM debugging register
1100E030	DISP_PWM_DUMMY	32	**PWM Dummy Register** PWM dummy register

1100E000 DISP_PWM_EN PWM Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																PWM_EN
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0		PWM_EN	Enables PWM or not

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1100E004 DISP_PWM_RST PWM Reset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																PWM_RST
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0		PWM_RST	SW resets PWM

1100E008 DISP_PWM_COMMIT PWM Commit 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																PWM_COMMIT
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0		PWM_COMMIT	Commits shadow register values to working registers

1100E010 DISP_PWM_CON_0 PWM Control 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							PWM_CLKDIV									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									PWM_DONT_UPDATE	TE_EDGE_SEL	PWM_UPDATE_SEL		PWM_FRAME_SYNC	PWM_POLARITY		PWM_AUTO_MODE
Type									RW	RW	RW		RW	RW		RW
Reset									0	0	0	0	0	0		0

Bit(s)	Mnemonic	Name	Description
25:16		PWM_CLKDIV	**Selects PWM clock division** PWM clock frequency = 26MHz/(PWM_CLKDIV + 1)

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Bit(s)	Mnemonic	Name	Description
7		PWM_DONT_UPDATE	**Disables PWM setting update** 0: PWM setting can be normally updated. 1: PWM setting cannot be updated.
6		TE_EDGE_SEL	**Selects TE edge** 0: Rising edge 1: Falling edge
5:4		PWM_UPDATE_SEL	**Selects PWM setting update source** 00: PWM setting is updated by mutex SOF. 01: PWM setting is updated by DSI internal TE. 10: PWM setting is updated by DSI external TE. 11: PWM setting is updated by DBI external TE.
3		PWM_FRAME_SYNC	**PWM waveform frame synchronization** 0: PWM waveform is free-run. 1: PWM waveform rising edge is synchronized with SOF.
2		PWM_POLARITY	**PWM waveform polarity** 0: Default=0; duty = high level/period 1: Default=1; duty = low level/period
0		PWM_AUTO_MODE	**PWM generator auto mode** 0: Manual mode (defined by DISP_PWM_CON_1) 1: Auto mode (from BLS)

1100E014 **DISP_PWM_CON_1** **PWM Control 1** **000003FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				PWM_HIGH_WIDTH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					PWM_PERIOD											
Type					RW											
Reset					0	0	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
28:16		PWM_HIGH_WIDTH	**PWM high width = PWM_HIGH_WIDTH + 1** Unit: clk Only for manual mode.
11:0		PWM_PERIOD	**PWM period = PWM_PERIOD + 1 (unit: clk)** (Only for manual mode)

1100E018 **DISP_PWM_GRADUAL** **PWM Gradual Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									PWM_GRADUAL_STEP							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			PWM_GRADUAL_FRAME													PWM_GRADUAL_EN
Type			RW													RW

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Reset			0	0	0	0	0	0								0

Bit(s)	Mnemonic	Name	Description
23:16		PWM_GRADUAL_STEP	**PWM duty gradual step** PWM_GRADUAL_STEP needs to be > 0.
13:8		PWM_GRADUAL_FRAME	**PWM duty gradual frame** PWM duty updates every (PWM_GRADUAL_FRAME + 1) frames.
0		PWM_GRADUAL_EN	**Enables PWM duty gradual**

1100E01C **DISP_PWM_GRADUAL_RO** **PWM Gradual Control Output** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**PWM_HIGH_WIDTH_GRAD**												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0		PWM_HIGH_WIDTH_GRAD	PWM high width after gradual control

1100E020 **DISP_PWM_DEBUG** **PWM Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**PWM_DOUBLE_BUFFER_DIS**	**DOUBLE_BUFFER_DIS**
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1		PWM_DOUBLE_BUFFER_DIS	Disables PWM setting double buffer
0		DOUBLE_BUFFER_DIS	Disables register double buffer

1100E030 **DISP_PWM_DUMMY** **PWM Dummy Register** **00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		DUMMY	Reserved

6.19.4 Programming Guide

1. Turn on DISP_PWM operating clock.
2. Get MMSYS mutex.
3. Set up DISP_PWM_CON_0 and DISP_PWM_CON_1.
4. Write DISP_PWM_EN = 1.
5. Release MMSYS mutex.

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6.20 DPI (Digital Parallel Interface)

6.20.1 Introduction

The DPI controller provides data to the companion chip, such as HDMI, MHL, or other bridge chips.

6.20.2 Features

- Programmable 2D/3D, progressive/interlaced timing generator
- Programmable EAV, SAV embedded sync. Timing
- Fixed-coefficient color space transform
- Supports RGB 8-bit/YUV444 8-bit/YUV422 8-bit,10-bit,12-bit output data format
- Supports YC MUX (CCIR656-like) output format
- Support s dual edge output format
- Supports secure display
- 3-tap chroma LPF
- Internal pattern generator

6.20.3 Register Definition

Module name: DISP_DPI Base address: (+14013000h)

Address	Name	Width	Register Function
14013000	DPI_EN	32	**DPI Enable Register** DPI enable signal
14013004	DPI_RST	32	DPI Software Reset Register
14013008	DPI_INTEN	32	**DPI IRQ Enable Register** DPI interrupt enable of individual interrupt source
1401300C	DPI_INTSTA	32	**DPI IRQ Status Register** DPI interrupt status
14013010	DPI_CON	32	**DPI Control Register** Controls DPI
14013014	DPI_OUTPUT_SETTING	32	DPI Output Stage Setting Register
14013018	DPI_SIZE	32	DPI Size Register
1401301C	DPI_DDR_SETTING	32	DPI DDR Register
14013020	DPI_TGEN_HWIDTH	32	**DPI Timing Generator Horizontal Sync Pulse Width Control Register** Controls DPI timing generator horizontal sync pulse width.
14013024	DPI_TGEN_HPORCH	32	**DPI Timing Generator Horizontal Front/Back Porch Control Register** Controls DPI timing generator horizontal front/back porch.
14013028	DPI_TGEN_VWIDTH	32	**DPI Timing Generator Vertical Sync Pulse Width Control Register** Controls DPI timing generator vertical sync pulse width (left frame, odd field).
1401302C	DPI_TGEN_VPORCH	32	**DPI Timing Generator Vertical Front/Back Porch Control Register**

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Address	Name	Width	Register Function
			Controls DPI timing generator vertical front/back porch (left frame, odd field).
14013030	DPI_BG_HCNTL	32	**DPI Background Horizontal Control Register** Controls DPI background horizontal
14013034	DPI_BG_VCNTL	32	DPI Background Vertical Control Register
14013038	DPI_BG_COLOR	32	DPI Background Color Register
1401303C	DPI_FIFO_CTL	32	**DPI FIFO CTL** Controls DPI FIFO
14013040	DPI_STATUS	32	**DPI Status Register** DPI current status
14013044	DPI_TMODE	32	**DPI Test Mode Register** Controls DPI test mode
14013048	DPI_CHKSUM	32	**DPI Checksum Register** Controls DPI checksum
14013050	DPI_DUMMY	32	
14013068	DPI_TGEN_VWIDTH_LEVEN	32	DPI Timing Generator Vertical Sync Pulse Width Control Register (Left Frame, Even Field)
1401306C	DPI_TGEN_VPORCH_LEVEN	32	DPI Timing Generator Vertical Front/Back Porch Control Register (Left Frame, Even Field)
14013070	DPI_TGEN_VWIDTH_RODD	32	DPI Timing Generator Vertical Sync Pulse Width Control Register (Right Frame, Odd Field)
14013074	DPI_TGEN_VPORCH_RODD	32	DPI Timing Generator Vertical Front/Back Porch Control Register (Right Frame, Odd Field)
14013078	DPI_TGEN_VWIDTH_REVEN	32	DPI Timing Generator Vertical Sync Pulse Width Control Register (Right Frame, Even Field)
1401307C	DPI_TGEN_VPORCH_REVEN	32	DPI Timing Generator Vertical Front/Back Porch Control Register (Right Frame, Even Field)
14013080	DPI_ESAV_VTIM_LODD	32	**EAV/SAV V Timing Control Register (Left ODD Frame)** Controls EAV/SAV V timing (left odd frame)
14013084	DPI_ESAV_VTIM_LEVEN	32	**EAV/SAV V Timing Control Register (Left EVEN Frame)** Controls EAV/SAV V timing (left even frame)
14013088	DPI_ESAV_VTIM_RODD	32	**EAV/SAV V Timing Control Register (Right ODD Frame)** Controls EAV/SAV V timing (right odd frame)
1401308C	DPI_ESAV_VTIM_REVEN	32	**EAV/SAV V Timing Control Register (Right EVEN Frame)** Controls EAV/SAV V timing (right even frame)
14013090	DPI_ESAV_FTIM	32	**EAV/SAV F Timing Control Register** Controls EAV/SAV F timing
14013094	DPI_CLPF_SETTING	32	Chroma Low-Pass Filter Setting Register
14013098	DPI_Y_LIMIT	32	Y (G) Channel Limit Setting Register
1401309C	DPI_C_LIMIT	32	C (R, B) Channel Limit Setting Register
140130A0	DPI_YUV422_SETTING	32	YUV444 To YUV422 Transform Setting Register
140130A4	DPI_EMBSYNC_SETTING	32	Embedded Sync Setting Register
140130A8	DPI_ESAV_CODE_SET0	32	Embedded Sync Setting Register
140130AC	DPI_ESAV_CODE_SET1	32	Embedded Sync Setting Register
140130B0	DPI_BLANK_CODE	32	Blanking Code Setting Register

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Address	Name	Width	Register Function
	SET		
140130B4	DPI_MATRIX_SET	32	Color Matrix Setting Register
140130B8	DPI_MATRIX_COEF_00	32	Color Matrix Coefficient Register
140130BC	DPI_MATRIX_COEF_02	32	Color Matrix Coefficient Register
140130C0	DPI_MATRIX_COEF_11	32	Color Matrix Coefficient Register
140130C4	DPI_MATRIX_COEF_20	32	Color Matrix Coefficient Register
140130C8	DPI_MATRIX_COEF_22	32	Color Matrix Coefficient Register
140130CC	DPI_MATRIX_IN_OFFSET_0	32	Color Matrix Input Offset Register
140130D0	DPI_MATRIX_IN_OFFSET_2	32	Color Matrix Input Offset Register
140130D4	DPI_MATRIX_OUT_OFFSET_0	32	Color Matrix Output Offset Register
140130D8	DPI_MATRIX_OUT_OFFSET_2	32	Color Matrix Output Offset Register
14013F00	DPI_PATTERN	32	**DPI Internal Pattern Register** Controls DPI internal pattern

14013000 DPI_EN DPI Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	EN	EN	**Turns on/off DPI controller** 0: DPI controller off 1: DPI controller on

14013004 DPI_RST DPI Software Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RST
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	RST	RST	**Resets DPI controller or not**

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Bit(s)	Mnemonic	Name	Description
			0: Release DPI reset 1: Assert DPI reset

14013008 DPI_INTEN DPI IRQ Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														INT_UNDERFLOW_EN	INT_VDE_EN	INT_VSYNC_EN
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2	INT_UNDERFLOW_EN	INT_UNDERFLOW_EN	**If FIFO is underflow, an interrupt request will be generated.** 0: Disable 1: Enable
1	INT_VDE_EN	INT_VDE_EN	**If VDE is activated, an interrupt request will be generated.** 0: Disable 1: Enable
0	INT_VSYNC_EN	INT_VSYNC_EN	**If VSYNC is activated, an interrupt request will be generated.** 0: Disable 1: Enable

1401300C DPI_INTSTA DPI IRQ Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														INTSTA_UNDERFLOW	INTSTA_VDE_EN	INTSTA_VSYNC_EN
Type														A1	A1	A1
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2	INTSTA_UNDERFLOW	INTSTA_UNDERFLOW	**If FIFO is underflow, an interrupt request will be generated.** SW can only write 0 to clear the interrupt. Writing 1 is ineffective.
1	INTSTA_VDE_EN	INTSTA_VDE_EN	**If VDE falling edge, an interrupt request will be generated.** SW can only write 0 to clear the interrupt. Writing 1 is ineffective.
0	INTSTA_	INTSTA_VSYNC	**If VSYNC is activated, an interrupt request will be**

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Bit(s)	Mnemonic	Name	Description
	VSYNC_EN	_EN	**generated.** SW can only write 0 to clear the interrupt. Writing 1 is ineffective.

14013010 DPI_CON DPI Control Register 00030000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FAKE_DE_REVEN	FAKE_DE_RODD	FAKE_DE_LEVEN	FAKE_DE_LODD	VS_REVEN_EN	VS_RODD_EN	VS_LEVEN_EN	VS_LODD_EN
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	1	1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PIXREP							EMBSYNC_EN		MATRIX_EN	YUV422_EN	CLPF_EN	TDFP_EN	INTL_EN	IN_RB_SWAP	BG_ENABLE
Type	RW							RW		RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0				0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23	FAKE_DE_REVEN	FAKE_DE_REVEN	**Fake DE for REVEN frame**
22	FAKE_DE_RODD	FAKE_DE_RODD	**Fake DE for RODD frame**
21	FAKE_DE_LEVEN	FAKE_DE_LEVEN	**Fake DE for LEVEN frame**
20	FAKE_DE_LODD	FAKE_DE_LODD	**Fake DE for LODD frame**
19	VS_REVEN_EN	VS_REVEN_EN	**VS_EN for REVEN frame**
18	VS_RODD_EN	VS_RODD_EN	**VS_EN for RODD frame**
17	VS_LEVEN_EN	VS_LEVEN_EN	**VS_EN for LEVEN frame**
16	VS_LODD_EN	VS_LODD_EN	**VS_EN for LODD frame**
15:12	PIXREP	PIXREP	**Enables embedded sync**
8	EMBSYNC_EN	EMBSYNC_EN	
6	MATRIX_EN	MATRIX_EN	**Enables color space conversion**
5	YUV422_EN	YUV422_EN	**Enables YUV444-to-422**
4	CLPF_EN	CLPF_EN	**Enables chroma low pass filter**
3	TDFP_EN	TDFP_EN	**Enables 3D frame packet** 0: Disable 3D frame packing 1: Enable 3D frame packing
2	INTL_EN	INTL_EN	**Enables interlace** 0: Progressive mode

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Bit(s)	Mnemonic	Name	Description
			1: Interlace mode
1	**IN_RB_SWAP**	IN_RB_SWAP	**Swaps input RB channel** 0: RGB 1: BGR
0	**BG_ENABLE**	BG_ENABLE	**Enables frame** 0: No background frame 1: Background frame

14013014 **DPI_OUTPUT_SETTING** **DPI Output Stage Setting Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										**YC_MAP**			**OUT_BIT**		**DUAL_EDGE_SEL**	**DPI_OEN_OFF**
Type										RW			RW		RW	RW
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DPI_CK_POL**	**VSYNC_POL**	**HSYNC_POL**	**DE_POL**		**VS_MASK**	**HS_MASK**	**DE_MASK**		**R_MASK**	**G_MASK**	**B_MASK**	**OUT_BIT_SWAP**	**OUT_CH_SWAP**		
Type	RW	RW	RW	RW		RW	RW	RW		RW	RW	RW	RW	RW		
Reset	0	0	0	0		0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
22:20	**YC_MAP**	YC_MAP	**YUV422 bit mapping** 0XX: {R[7:4],G[7:4],B[7:4]} (or {Cr[7: 4],Y[7:4],Cb[7:4]}) 100: {C[11:4],Y[11:4],C[3:0],Y[3:0]} 101: {Y[11:4],C[11:4],Y[3:0],C[3:0]} 110: {C[11:0],Y[11:0]} 111: {Y[11:0],C[11:0]}
19:18	**OUT_BIT**	OUT_BIT	**Output bit number** 00: 8 bits 01: 10 bits 10: 12 bits 11: 12 bits
17	**DUAL_EDGE_SEL**	EDGE_SEL	**Selects output dual edge** 0: First edge: {R[7:0], G[7:4]} Second edge: {G[3:0], B[7:0]} 1: First edge: {G[3:0], B[7:0]} Second edge: {R[7:0], G[7:4]}
16	**DPI_OEN_OFF**	DPI_OEN_OFF	**Turns off DPI output enabling** 0: Does not turn off 1: Turn off
15	**DPI_CK_POL**	CK_POL	0: Polarity is the same as internal DPI clock. 1: Invert polarity
14	**VSYNC_POL**	VSYNC_POL	**Vsync polarity** 0: Negative 1: Positive
13	**HSYNC_POL**	HSYNC_POL	**Hsync polarity** 0: Negative

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Bit(s)	Mnemonic	Name	Description
			1: Positive
12	**DE_POL**	DE_POL	**Data enabling polarity** 0: Positive 1: Negative
10	**VS_MASK**	VS_MASK	**Controls Vsync mask** 0: Enable Vsync 1: Mask Vsync
9	**HS_MASK**	HS_MASK	**Controls Hsync mask** 0: Enable Hsync 1: Mask Hsync
8	**DE_MASK**	DE_MASK	**Controls DE mask** 0: Enable DE 1: Mask DE
6	**R_MASK**	R_MASK	**Controls R channel mask** 0: Enable R channel 1: Mask R channel
5	**G_MASK**	G_MASK	**Controls G channel mask** 0: Enable G channel 1: Mask G channel
4	**B_MASK**	B_MASK	**Controls B channel mask** 0: Enable B channel 1: Mask B channel
3	**OUT_BIT_SWAP**	BIT_SWAP	**Inverts output bit order**
2:0	**OUT_CH_SWAP**	CH_SWAP	**Swaps output channel** 000: RGB 001: GBR 010: BRG 011: RBG 100: GRB 101: BGR

14013018 **DPI_SIZE** **DPI Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				HSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**VSIZE**	VSIZE	DPI vertical size
12:0	**HSIZE**	HSIZE	DPI horizontal size

1401301C **DPI_DDR_SETTING** **DPI DDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DDR_PAD_MODE			DDR_WIDTH		DATA_THROT	DDR_4PHASE	DDR_SEL	DDR_EN
Type								RW			RW		RW	RW	RW	RW
Reset								0			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8	DDR_PAD_MODE	DDR_PAD_MODE	**DPI dual edge padding mode** 0: Padding by MSB 1: Padding by 0's
5:4	DDR_WIDTH	DDR_WIDTH	**DPI dual edge output width** 0: RGB888 DDR (12 bits) 1: RGB101010 DDR (15 bits) 2: RGB121212 DDR (18 bits) 3: RGB161616 DDR (24 bits)
3	DATA_THROT	DATA_THROT	
2	DDR_4PHASE	DDR_4PHASE	**DPI dual edge central align clock**
1	DDR_SEL	DDR_SEL	**Selects DPI dual edge output**
0	DDR_EN	DDR_EN	**Enables DPI dual edge**

14013020 **DPI_TGEN_HWIDTH** **DPI Timing Generator Horizontal Sync Pulse Width Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					HPW											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0	HPW	HPW	**Horizontal sync pulse width** Unit: Pixel. Must be > 0.

14013024 **DPI_TGEN_HPORCH** **DPI Timing Generator Horizontal Front/Back Porch Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					HFP											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					HBP											
Type					RW											

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Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**HFP**	HFP	**Horizontal front porch width** Unit: Pixel. Must be > 0.
11:0	**HBP**	HBP	**Horizontal back porch width** Unit: Pixel. Must be > 0.

14013028 **DPI_TGEN_VWIDTH** **DPI Timing Generator Vertical Sync Pulse Width Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**VPW_HALF**
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**VPW**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	**VPW_HALF**	VPW_HALF	**Controls vertical sync pulse width (left frame, even field).** 0: VS puls width aligned to HS puls 1: VS puls width shifts 0.5 lines
11:0	**VPW**	VPW	**Vertical sync pulse width (left frame, odd field)** Unit: Line. Must be > 0.

1401302C **DPI_TGEN_VPORCH** **DPI Timing Generator Vertical Front/Back Porch Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**VFP**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**VBP**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**VFP**	VFP	**Vertical front porch width (left frame, odd field)** Unit: Line. Must be > 0.
11:0	**VBP**	VBP	**Vertical back porch width (left frame, odd field)** Unit: Line. Must be > 0.

14013030 **DPI_BG_HCNTL** **DPI Background Horizontal Control Register** **00010001**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				BG_LEFT												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				BG_RIGHT												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
28:16	BG_LEFT	BG_LEFT	Left DPI frame boundary
12:0	BG_RIGHT	BG_RIGHT	Right DPI frame boundary

14013034 **DPI_BG_VCNTL** **DPI Background Vertical Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				BG_TOP												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				BG_BOT												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	BG_TOP	BG_TOP	Top DPI frame boundary
12:0	BG_BOT	BG_BOT	Bottom DPI frame boundary

14013038 **DPI_BG_COLOR** **DPI Background Color Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BG_R							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BG_G								BG_B							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:16	BG_R	BG_R	DPI background color R
15:8	BG_G	BG_G	DPI background color G
7:0	BG_B	BG_B	DPI background color B

1401303C **DPI_FIFO_CTL** **DPI FIFO CTL** **00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**FIFO_RST_SEL**				**FIFO_VALID_SET**				
Type								RW				RW				
Reset								0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8	**FIFO_RST_SEL**	FIFO_RST_SEL	Controls DPI FIFO
4:0	**FIFO_VALID_SET**	FIFO_VALID_SET	Controls DPI FIFO

14013040 **DPI_STATUS** **DPI Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											**TDLR**	**FIELD**			**OUTEN**	**DPI_BUSY**
Type											RU	RU			RU	RU
Reset											0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**V_COUNTER**												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21	**TDLR**	TDLR	3DLR signal
20	**FIELD**	FIELD	Field signal
17	**OUTEN**	OUTEN	Output pad of DPI signals is enabled to output.
16	**DPI_BUSY**	DPI_BUSY	DPI is busy.
12:0	**V_COUNTER**	V_COUNTER	Line counter

14013044 **DPI_TMODE** **DPI Test Mode Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**DPI_OEN_ON**
Type																RW
Reset																0

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Bit(s)	Mnemonic	Name	Description
0	**DPI_OEN_ON**	DPI_OEN_ON	**Turns on DPI output enabling** Only takes effect when DPI_OEN_OFF = 0.

14013048 **DPI_CHKSUM** **DPI Checksum Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DPI_CHKSUM_EN**	**DPI_CHKSUM_RDY**							**DPI_CHKSUM[23:16]**							
Type	WO	RU							RU							
Reset	0	0							0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DPI_CHKSUM[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**DPI_CHKSUM_EN**	DPI_CHKSUM_EN	**Enables DPI checksum** 0: Disable 1: Enable
30	**DPI_CHKSUM_RDY**	DPI_CHKSUM_READY	**DPI checksum ready**
23:0	**DPI_CHKSUM**	DPI_CHKSUM	**DPI checksum**

14013050 **DPI_DUMMY** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DPI_DUMMY[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DPI_DUMMY[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DPI_DUMMY**	DPI_DUMMY	

14013068 **DPI_TGEN_VWIDTH_LEVEN** **DPI Timing Generator Vertical Sync Pulse Width Control Register (Left Frame, Even Field)** **00010000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**VPW**

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																_HALF_LEVEN
Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**VPW_LEVEN**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	**VPW_HALF_LEVEN**	VPW_HALF_LEVEN	**Controls vertical sync pulse width (left frame, even field).** 0: LEVEN VS puls width aligned to HS puls 1: LEVEN VS puls width shifts 0.5 lines
11:0	**VPW_LEVEN**	VPW_LEVEN	**Vertical sync pulse width (left frame, even field)** Unit: Line. Must be > 0.

1401306C **DPI_TGEN_VPORCH_LEVEN** **DPI Timing Generator Vertical Front/Back Porch Control Register (Left Frame, Even Field)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**VFP_LEVEN**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**VBP_LEVEN**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**VFP_LEVEN**	VFP_LEVEN	**Vertical front porch width (left frame, even field)** Unit: Line. Must be > 0.
11:0	**VBP_LEVEN**	VBP_LEVEN	**Vertical back porch width (left frame, even field)** Unit: Line. Must be > 0.

14013070 **DPI_TGEN_VWIDTH_RODD** **DPI Timing Generator Vertical Sync Pulse Width Control Register (Right Frame, Odd Field)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**VPW_HALF_RODD**
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**VPW_RODD**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
16	**VPW_HALF_RODD**	VPW_HALF_RODD	**Controls vertical sync pulse width (right frame, odd field).** 0: RODD VS puls width aligned to HS puls 1: RODD VS puls width shifts 0.5 lines
11:0	**VPW_RODD**	VPW_RODD	**Vertical sync pulse width (right frame, odd field)** Unit: Line. Must be > 0.

14013074 **DPI_TGEN_VPORCH_RODD** **DPI Timing Generator Vertical Front/Back Porch Control Register (Right Frame, Odd Field)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					VFP_RODD											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					VBP_RODD											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**VFP_RODD**	VFP_RODD	**Vertical front porch width (right frame, odd field)** Unit: Line. Must be > 0.
11:0	**VBP_RODD**	VBP_RODD	**Vertical back porch width (right frame, odd field)** Unit: Line. Must be > 0.

14013078 **DPI_TGEN_VWIDTH_REVEN** **DPI Timing Generator Vertical Sync Pulse Width Control Register (Right Frame, Even Field)** **00010000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																VPW_HALF_REVEN
Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					VPW_REVEN											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	**VPW_HALF_REVEN**	VPW_HALF_REVEN	**Controls vertical sync pulse width (right frame, even field).** 0: REVEN VS puls width aligned to HS puls 1: REVEN VS puls width shifts 0.5 lines
11:0	**VPW_REVEN**	VPW_REVEN	**Vertical sync pulse width (right frame, even field)** Unit: Line. Must be > 0.

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1401307C	DPI_TGEN_VPORCH_R_EVEN	DPI Timing Generator Vertical Front/Back Porch Control Register (Right Frame, Even Field)	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					VFP_REVEN											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					VBP_REVEN											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	VFP_REVEN	VFP_REVEN	**Vertical front porch width (right frame, even field)** Unit: Line. Must be > 0.
11:0	VBP_REVEN	VBP_REVEN	**Vertical back porch width (right frame, even field)** Unit: Line. Must be > 0.

14013080	DPI_ESAV_VTIM_LODD	EAV/SAV V Timing Control Register (Left ODD Frame)	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					ESAV_VWID_LODD											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ESAV_VOFST_LODD											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	ESAV_VWID_LODD	ESAV_VWID_LODD	**EAV/SAV V width (left frame, odd field)** Unit: Line.
11:0	ESAV_VOFST_LODD	ESAV_VOFST_LODD	**Enables EAV/SAV V offset from the end of data (left frame, odd field)** Unit: Line.

14013084	DPI_ESAV_VTIM_LEVEN	EAV/SAV V Timing Control Register (Left EVEN Frame)	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					ESAV_VWID_LEVEN											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ESAV_VOFST_LEVEN											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
27:16	**ESAV_VWID_LEVEN**	ESAV_VWID_LEVEN	**EAV/SAV V width (left frame, even field)** Unit: Line.
11:0	**ESAV_VOFST_LEVEN**	ESAV_VOFST_LEVEN	**Enables EAV/SAV V offset from the end of data (left frame, even field)** Unit: Line.

14013088 **DPI_ESAV_VTIM_RODD** **EAV/SAV V Timing Control Register (Right ODD Frame)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					ESAV_VWID_RODD											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ESAV_VOFST_RODD											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**ESAV_VWID_RODD**	ESAV_VWID_RODD	**EAV/SAV V width (right frame, odd field)** Unit: Line.
11:0	**ESAV_VOFST_RODD**	ESAV_VOFST_RODD	**Enables EAV/SAV V offset from the end of data (right frame, odd field).** Unit: Line.

1401308C **DPI_ESAV_VTIM_REVEN** **EAV/SAV V Timing Control Register (Right EVEN Frame)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					ESAV_VWID_REVEN											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ESAV_VOFST_REVEN											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**ESAV_VWID_REVEN**	ESAV_VWID_REVEN	**EAV/SAV V width (right frame, even field).** Unit: Line.
11:0	**ESAV_VOFST_REVEN**	ESAV_VOFST_REVEN	**Enables EAV/SAV V offset from the end of data (right frame, even field)** Unit: Line.

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14013090 DPI_ESAV_FTIM EAV/SAV F Timing Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					ESAV_FOFST_EVEN											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ESAV_FOFST_ODD											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	ESAV_FOFST_EVEN	ESAV_FOFST_EVEN	**EAV/SAV F offset from the end of data enable (even field)** Unit: Line.
11:0	ESAV_FOFST_ODD	ESAV_FOFST_ODD	**EAV/SAV F offset from the end of data enable (odd field)** Unit: Line.

14013094 DPI_CLPF_SETTING Chroma Low-Pass Filter Setting Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												ROUND_EN			CLPF_TYPE	
Type												RW			RW	
Reset												0			0	0

Bit(s)	Mnemonic	Name	Description
4	ROUND_EN	ROUND_EN	**Enables chroma LPF output rounding** 0: Disable rounding 1: Enable rounding
1:0	CLPF_TYPE	CLPF_TYPE	**Chroma LPF type** 00: out = 1/2*(in + in_d1) 01: out = 1/2*(in_d1 + in_d2) 10: out = 1/4*(in + 2*in_d1 + in_d2) 11: out = 1/4*(in + 2*in_d1 + in_d2)

14013098 DPI_Y_LIMIT Y (G) Channel Limit Setting Register 0FFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					Y_LIMIT_TOP											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					Y_LIMIT_BOT											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
27:16	**Y_LIMIT_TOP**	Y_LIMIT_TOP	Y (G) channel value top limit
11:0	**Y_LIMIT_BOT**	Y_LIMIT_BOT	Y (G) channel value bottom limit

1401309C **DPI_C_LIMIT** **C (R, B) Channel Limit Setting Register** **0FFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					C_LIMIT_TOP											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					C_LIMIT_BOT											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**C_LIMIT_TOP**	C_LIMIT_TOP	C (R,B) channel value top limit
11:0	**C_LIMIT_BOT**	C_LIMIT_BOT	C (R,B) channel value bottom limit

140130A0 **DPI_YUV422_SETTING** **YUV444 To YUV422 Transform Setting Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DE_DELSEL	Y_DELSEL	CB_DELSEL	CR_DELSEL				UV_SWAP
Type									RW	RW	RW	RW				RW
Reset									0	0	0	0				0

Bit(s)	Mnemonic	Name	Description
7	**DE_DELSEL**	DE_DELSEL	**Selects data enable and control signal deley** 0: Delay 0 T 1: Delay 1 T
6	**Y_DELSEL**	Y_DELSEL	**Selects Y channel delay** 0: Delay 0 T 1: Delay 1 T
5	**CB_DELSEL**	CB_DELSEL	**Selects Cb channel delay** 0: Delay 0 T 1: Delay 1 T
4	**CR_DELSEL**	CR_DELSEL	**Selects Cr channel delay** 0: Delay 0 T 1: Delay 1 T

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Bit(s)	Mnemonic	Name	Description
0	UV_SWAP	UV_SWAP	**Swaps Cb, Cr channel** 0: CbCr 1: CrCb

140130A4 **DPI_EMBSYNC_SETTING** **Embedded Sync Setting Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**EMBSYNC_OPT**
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**VS_OSEL**						**ESAV_CODE_MAN**		**ESAV_H_INV**	**ESAV_V_INV**	**ESAV_F_INV**		**EMBSYNC_B_CB_EN**	**EMBSYNC_G_Y_EN**	**EMBSYNC_R_CR_EN**
Type		RW						RW		RW	RW	RW		RW	RW	RW
Reset		0	0	0				0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
16	**EMBSYNC_OPT**	EMBSYNC_OPT	
14:12	**VS_OSEL**	VS_OUT_SEL	**Selects vsync output** 000: Vsync of timing generator 100: ESAV_V 101: ESAV_F 110: Hsync aligned ESAV_V 111: Hsync aligned ESAV_F
8	**ESAV_CODE_MAN**	ESAV_CODE_MAN	**EAV/SAV code definition** 0: Use default EAV/SAV definition 1: Use manual code defined by 0xA0~0xA4
6	**ESAV_H_INV**	ESAV_H_INV	**Inverts H bit**
5	**ESAV_V_INV**	ESAV_V_INV	**Inverts V bit**
4	**ESAV_F_INV**	ESAV_F_INV	**Inverts F bit**
2	**EMBSYNC_B_CB_EN**	EMBSYNC_B_CB_EN	**Embedded sync in Cb (B) Channel**
1	**EMBSYNC_G_Y_EN**	EMBSYNC_G_Y_EN	**Embedded sync in Y (G) Channel**
0	**EMBSYNC_R_CR_EN**	EMBSYNC_R_CR_EN	**Embedded sync in Cr (R) Channel**

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140130A8 **DPI_ESAV_CODE_SET0** **Embedded Sync Setting Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					ESAV_CODE1											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ESAV_CODE0											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	ESAV_CODE1	ESAV_CODE1	EAV/SAV manual code 1
11:0	ESAV_CODE0	ESAV_CODE0	EAV/SAV manual code 0

140130AC **DPI_ESAV_CODE_SET1** **Embedded Sync Setting Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																ESAV_CODE3_MSB
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ESAV_CODE2											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	ESAV_CODE3_MSB	ESAV_CODE3_MSB	EAV/SAV manual code 3 (bit 7)
11:0	ESAV_CODE2	ESAV_CODE2	EAV/SAV manual code 2

140130B0 **DPI_BLANK_CODE_SET** **Blanking Code Setting Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							BLANK_PAD_OPT	BLANK_CODE_EN	BLANK_B_CB							
Type							RW	RW	RW							
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BLANK_G_Y								BLANK_R_CR							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
25	**BLANK_PAD_OPT**	BLANK_PAD_OPT	
24	**BLANK_CODE_EN**	BLANK_CODE_EN	
23:16	**BLANK_B_CB**	BLANK_B	
15:8	**BLANK_G_Y**	BLANK_G	
7:0	**BLANK_R_CR**	BLANK_R	

140130B4 **DPI_MATRIX_SET** **Color Matrix Setting Register** **00000203**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				EXT_MATRIX_EN			MATRIX_BIT					INT_MATRIX_SEL				
Type				RW			RW					RW				
Reset				0			1	0				0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
12	**EXT_MATRIX_EN**	EXT_MATRIX_EN	
9:8	**MATRIX_BIT**	MATRIX_BIT	
4:0	**INT_MATRIX_SEL**	INT_MATRIX_SEL	**Selects internal matrix coefficients** 0: RGB_TO_JPEG 1: RGB_TO_FULL709 2: RGB_TO_BT601 3: RGB_TO_BT709 4: JPEG_TO_RGB 5: FULL709_TO_RGB 6: BT601_TO_RGB 7: BT709_TO_RGB 8: JPEG_TO_BT601 9: JPEG_TO_BT709 10: BT601_TO_JPEG 11: BT709_TO_JPEG 12: BT709_TO_BT601 13: BT601_TO_BT709 20: JPEG_TO_CERGB 21: FULL709_TO_CERGB 22: BT601_TO_CERGB 23: BT709_TO_CERGB 28: RGB_TO_CERGB

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Bit(s)	Mnemonic	Name	Description
			Default: Bypass

140130B8 **DPI_MATRIX_COEF_00** **Color Matrix Coefficient Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**MATRIX_COEF_01**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**MATRIX_COEF_00**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**MATRIX_COEF_01**	MATRIX_COEF_01	Color matrix coefficient 01
12:0	**MATRIX_COEF_00**	MATRIX_COEF_00	Color matrix coefficient 00

140130BC **DPI_MATRIX_COEF_02** **Color Matrix Coefficient Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**MATRIX_COEF_10**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**MATRIX_COEF_02**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**MATRIX_COEF_10**	MATRIX_COEF_10	Color matrix coefficient 10
12:0	**MATRIX_COEF_02**	MATRIX_COEF_02	Color matrix coefficient 02

140130C0 **DPI_MATRIX_COEF_11** **Color Matrix Coefficient Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**MATRIX_COEF_12**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**MATRIX_COEF_11**												
Type				RW												

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Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**MATRIX_COEF_12**	MATRIX_COEF_12	Color matrix coefficient 12
12:0	**MATRIX_COEF_11**	MATRIX_COEF_11	Color matrix coefficient 11

140130C4 DPI_MATRIX_COEF_20 Color Matrix Coefficient Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MATRIX_COEF_21												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				MATRIX_COEF_20												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**MATRIX_COEF_21**	MATRIX_COEF_21	Color matrix coefficient 21
12:0	**MATRIX_COEF_20**	MATRIX_COEF_20	Color matrix coefficient 20

140130C8 DPI_MATRIX_COEF_22 Color Matrix Coefficient Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				MATRIX_COEF_22												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0	**MATRIX_COEF_22**	MATRIX_COEF_22	Color matrix coefficient 22

140130CC DPI_MATRIX_IN_OFFSET_0 Color Matrix Input Offset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name								MATRIX_IN_OFFSET_1								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MATRIX_IN_OFFSET_0								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16	**MATRIX_IN_OFFSET_1**	MATRIX_IN_OFFSET_1	Color matrix input offset 1
8:0	**MATRIX_IN_OFFSET_0**	MATRIX_IN_OFFSET_0	Color matrix input offset 0

140130D0 DPI_MATRIX_IN_OFFSET_2 Color Matrix Input Offset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MATRIX_IN_OFFSET_2								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0	**MATRIX_IN_OFFSET_2**	MATRIX_IN_OFFSET_2	Color matrix input offset 2

140130D4 DPI_MATRIX_OUT_OFFSET_0 Color Matrix Output Offset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								MATRIX_IN_OFFSET_1								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MATRIX_IN_OFFSET_0								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16	**MATRIX_IN_OFFSET_1**	MATRIX_OUT_OFFSET_1	Color matrix output offset 1
8:0	**MATRIX_IN_OFFSET_0**	MATRIX_OUT_OFFSET_0	Color matrix output offset 0

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140130D8 DPI_MATRIX_OUT_OFFSET_2 Color Matrix Output Offset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name								MATRIX_IN_OFFSET_2								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0	MATRIX_IN_OFFSET_2	MATRIX_OUT_OFFSET_2	Color matrix output offset 2

14013F00 DPI_PATTERN DPI Internal Pattern Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DPI_PAT_B								DPI_PAT_G							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DPI_PAT_R									DPI_PAT_SEL						PAT_EN
Type	RW									RW						RW
Reset	0	0	0	0	0	0	0	0		0	0	0				0

Bit(s)	Mnemonic	Name	Description
31:24	DPI_PAT_B	PAT_R_MAN	**User defined color (red)**
23:16	DPI_PAT_G	PAT_G_MAN	**User defined color (green)**
15:8	DPI_PAT_R	PAT_B_MAN	**User defined color (blue)**
6:4	DPI_PAT_SEL	PAT_SEL	**Selects internal pattern** 000: 256 vertical gray 001: 64 vertical gray 010: 256 horizontal gray 011: 64 horizontal gray 100: Color bar 101: User defined color 110: Frame border 111: Dot morei
0	PAT_EN	PAT_EN	**Enables internal pattern**

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6.20.4 Programming Guide

6.20.4.1 General Timing Programming

Programming DPI for one frame timing is easy. Figure 6-57 is illustration of the general timing relationship in DPI. The optional BG defines the region of background color in the image frame. The polarities of VS/HS/DE are all adjustable.

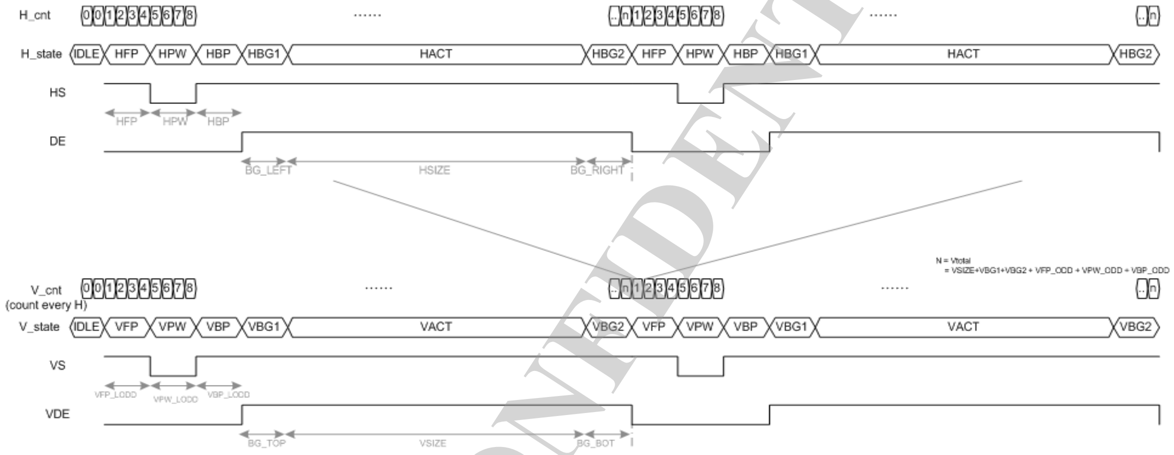

Figure 6-57. Illustration of general timing relationship

6.20.4.2 Data Timing Programming

The DPI engine supports four data/clock timing combinations in dual edge mode. In dual edge mode, one pixel is sent by 2 clock edges, and the order of sending MSB (High bits) and LSB (Low bits) is configurable. Another option is determining sending first half pixel by rising or falling clock edge. Figure 6-58 shows the data/clock timing and their corresponding settings in 4 cases.

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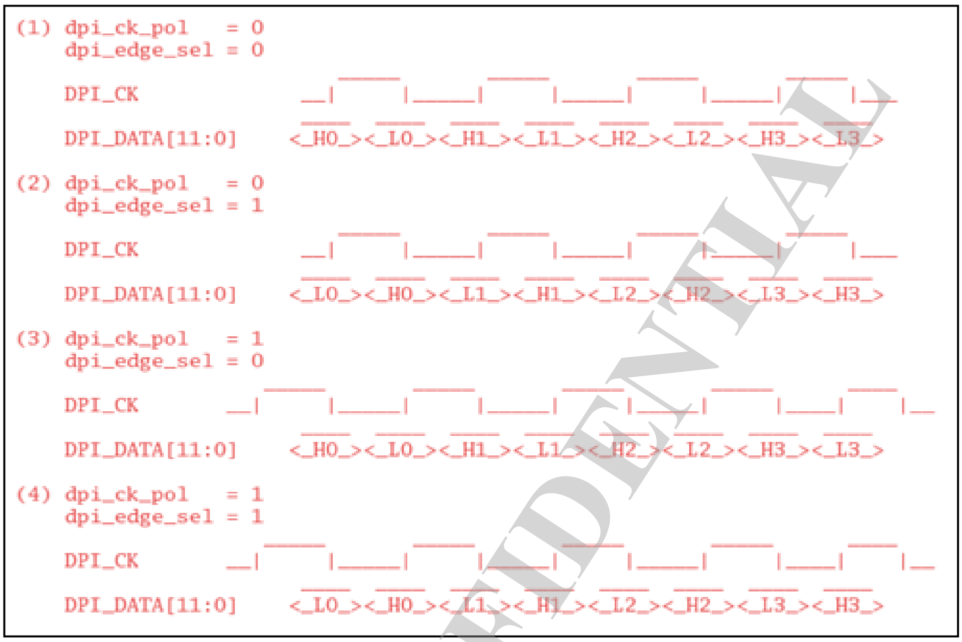

Figure 6-58. Data/Clock timing

Table 6-7 shows explicitly the data map of the 4 cases above.

Table 6-7. Data map

	Case 1		Case 2		Case 3		Case 4	
Pin name	**Rising edge**	**Falling edge**	**Rising edge**	**Falling edge**	**Falling edge**	**Rising edge**	**Falling edge**	**Rising edge**
D0	G4	B0	B0	G4	G4	B0	B0	G4
D1	G5	B1	B1	G5	G5	B1	B1	G5
D2	G6	B2	B2	G6	G6	B2	B2	G6
D3	G7	B3	B3	G7	G7	B3	B3	G7
D4	R0	B4	B4	R0	R0	B4	B4	R0
D5	R1	B5	B5	R1	R1	B5	B5	R1
D6	R2	B6	B6	R2	R2	B6	B6	R2
D7	R3	B7	B7	R3	R3	B7	B7	R3
D8	R4	G0	G0	R4	R4	G0	G0	R4
D9	R5	G1	G1	R5	R5	G1	G1	R5
D10	R6	G2	G2	R6	R6	G2	G2	R6
D11	R7	G3	G3	R7	R7	G3	G3	R7

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6.20.4.3 Programming Flow

Figure 6-59 shows the DPI programming flow diagram. First, configure each timing register based on the target frame timing. Next, reset and enable DPI.

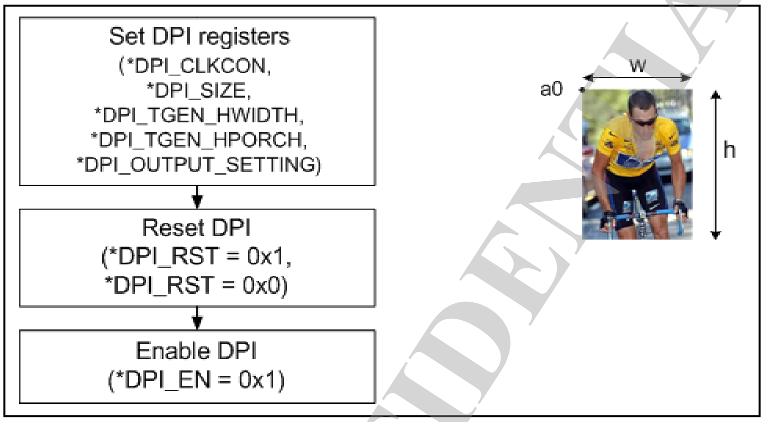

Figure 6-59. Programming flow diagram

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6.21 Display Serial Interface

6.21.1 Introduction

The Display Serial Interface (DSI) is based on MIPI Alliance Specification, supporting high-speed serial data transfer between host processor and peripheral devices such as display modules. DSI supports both video mode and command mode data transfer defined in MIPI spec, and it also provides bidirectional transmission with low-power mode to receive messages from the peripheral. DSI should work with MIPI_TX_Config module to obtain its engine clock to analog DPHY macro, and it should work with DMA engines in the previous stage of DISP path to read frame pixels from memory.

6.21.2 Features

The DSI engine has the following features for display serial interface:

- 1 clock lane and up to 4 data lanes
- Throughput up to 1G bps for 1 data lane
- Bidirectional data transmission in low-power mode in data lane 0
- Uni-directional data transmission in high-speed mode in data lane 0 ~ 3
- 128-enrty command queue for command transmission
- Supports 3 types of video modes: sync-event, sync-pulse, burst mode
- Pixel format of RGB565/RGB666/loosely RGB666/RGB888
- Supports non-continuous high-speed transmission in both clock/data lanes
- Supports command mode frame transmission free-run
- Supports peripheral TE and external TE signal detection
- Supports limited high-speed residual packet transmission during video mode blanking period
- Supports ultra-low power mode control
- Supports frame compression with UFOE module
- Supports low frame-rate (LFR) technique

6.21.3 Register Definition

Module name: DISP_DSI Base address: (+14011000h)

Address	Name	Width	Register Function
14011000	DSI_START	32	DSI Start Register
14011004	DSI_STATUS	32	DSI Status Register
14011008	DSI_INTEN	32	DSI Interrupt Enable Register
1401100C	DSI_INTSTA	32	DSI Interrupt Status Register
14011010	DSI_COM_CON	32	DSI Common Control Register
14011014	DSI_MODE_CON	32	DSI Mode Control Register
14011018	DSI_TXRX_CON	32	DSI TX RX Control Register
1401101C	DSI_PSCON	32	DSI Pixel Stream Control Register
14011020	DSI_VSA_NL	32	DSI Vertical Sync Active Register
14011024	DSI_VBP_NL	32	DSI Vertical Back Porch Register

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Address	Name	Width	Register Function
14011028	DSI_VFP_NL	32	DSI Vertical Front Porch Register
1401102C	DSI_VACT_NL	32	DSI Vertical Active Register
14011030	DSI_LFR_CON	32	DSI Low Frame Rate Control Register
14011034	DSI_LFR_STA	32	DSI Low Frame Rate Status Register
14011050	DSI_HSA_WC	32	DSI Horizontal Sync Active Word Count Register
14011054	DSI_HBP_WC	32	DSI Horizontal Back Porch Word Count Register
14011058	DSI_HFP_WC	32	DSI Horizontal Front Porch Word Count Register
1401105C	DSI_BLLP_WC	32	DSI Horizontal Blanking or Low Power Mode Word Count Register
14011060	DSI_CMDQ_CON	32	DSI Command Queue Control Register
14011064	DSI_HSTX_CKLP_WC	32	DSI HSTX Clock Low-power Mode Word Count Register
14011068	DSI_HSTX_CKLP_WC_AUTO_RESULT	32	DSI HSTX Clock Low-power Mode Automatic Calculation result
14011074	DSI_RX_DATA03	32	DSI Receive Packet Data Byte 0 ~ 3 Register
14011078	DSI_RX_DATA47	32	DSI Receive Packet Data Byte 4 ~ 7 Register
1401107C	DSI_RX_DATA8B	32	DSI Receive Packet Data Byte 8 ~ 11 Register
14011080	DSI_RX_DATAC	32	DSI Receive Packet Data Byte 12 ~ 15 Register
14011084	DSI_RX_RACK	32	DSI Read Data Acknowledge Register
14011088	DSI_RX_TRIG_STA	32	DSI Receiver Status Register
14011090	DSI_MEM_CONTI	32	DSI Memory Continue Command Register
14011094	DSI_FRM_BC	32	DSI Frame Byte Count Register
14011098	DSI_V3D_CON	32	DSI Vsync 3D Control Register
140110A0	DSI_TIME_CON0	32	DSI Timing Control 0 Register
140110A4	DSI_TIME_CON1	32	DSI Timing Control 1 Register
14011100	DSI_PHY_LCPAT	32	DSI PHY Lane Clock Pattern Register
14011104	DSI_PHY_LCCON	32	DSI PHY Lane Clock Control Register
14011108	DSI_PHY_LD0CON	32	DSI PHY Lane 0 Control Register
1401110C	DSI_PHY_SYNCON	32	DSI PHY Sync Control Register
14011110	DSI_PHY_TIMCON0	32	DSI PHY Timing Control 0 Register
14011114	DSI_PHY_TIMCON1	32	DSI PHY Timing Control 1 Register
14011118	DSI_PHY_TIMCON2	32	DSI PHY Timing Control 2 Register
1401111C	DSI_PHY_TIMCON3	32	DSI PHY Timing Control 3 Register
14011130	DSI_VM_CMD_CON	32	DSI Video Mode Command Packet Control Register
14011134	DSI_VM_CMD_DATA0	32	DSI Video Mode Command Packet Data Byte 0~3 Register

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Address	Name	Width	Register Function
14011138	DSI_VM_CMD_DATA4	32	DSI Video Mode Command Packet Data Byte 4~7 Register
1401113C	DSI_VM_CMD_DATA8	32	DSI Video Mode Command Packet Data Byte 8~11 Register
14011140	DSI_VM_CMD_DATAC	32	DSI Video Mode Command Packet Data Byte 12~15 Register
14011144	DSI_CKSM_OUT	32	DSI Checksum Output
14011148	DSI_STATE_DBG0	32	DSI State Machine Debug 0
1401114C	DSI_STATE_DBG1	32	DSI State Machine Debug 1
14011150	DSI_STATE_DBG2	32	DSI State Machine Debug 2
14011154	DSI_STATE_DBG3	32	DSI State Machine Debug 3
14011158	DSI_STATE_DBG4	32	DSI State Machine Debug 4
1401115C	DSI_STATE_DBG5	32	DSI State Machine Debug 5
14011160	DSI_STATE_DBG6	32	DSI State Machine Debug 6
14011164	DSI_STATE_DBG7	32	DSI State Machine Debug 7
14011168	DSI_STATE_DBG8	32	DSI State Machine Debug 8
1401116C	DSI_STATE_DBG9	32	DSI State Machine Debug 9
14011170	DSI_DEBUG_SEL	32	DSI Debug Output Selection
14011174	DSI_RESERVED	32	Reserved Register
14011178	DSI_BIST_PATTERN	32	DSI Bist Pattern Register
1401117C	DSI_BIST_CON	32	DSI Bist Control Register
14011180	DSI_VM_CMD_DATA10	32	DSI Video Mode Command Packet Data Byte 16~19 Register
14011184	DSI_VM_CMD_DATA14	32	DSI Video Mode Command Packet Data Byte 20~23 Register
14011188	DSI_VM_CMD_DATA18	32	DSI Video Mode Command Packet Data Byte 24~27 Register
1401118C	DSI_VM_CMD_DATA1C	32	DSI Video Mode Command Packet Data Byte 28~31 Register
14011200 ~ 140113FC	DSI_CMDQ[n] (n=0~127)	32	DSI Command Queue

14011000 DSI_START DSI Start Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																VM_CMD_START
Type																RW

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Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**SKEWCAL_START**		**SLEEPOUT_START**		**DSI_START**
Type												RW		RW		RW
Reset												0		0		0

Bit(s)	Name	Description
16	VM_CMD_START	**Starts DSI VM command transmission** Set up this bit to start command transmission in video mode. This bit is only available when VM_CMD_EN = 1. 0: No effect 1: Start
4	SKEWCAL_START	**DSI skew calibration operation** Set this bit to start de-skew calibration process for RX. This bit is only available when DSI_BUSY = 0 0: No effect 1: Start
2	SLEEPOUT_START	**DSI sleep-out operation** Set up this bit to wake up DSI from ULPS mode. This bit is only available when SLEEP_MODE = 1. 0: No effect 1: Start
0	DSI_START	**Starts DSI controller operation** Set up this bit to start DSI control. 0: No effect 1: Start

14011004 **DSI_STATUS** **DSI Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**CONTENTION_ERR**	**FALSE_CTRL_ERR**	**ESC_SYNC_ERR**	**ESC_ENTRY_ERR**			**BUFFER_UNDERRUN**	
Type									RU	RU	RU	RU			RU	
Reset									0	0	0	0			0	

Bit(s)	Name	Description
7	CONTENTION_ERR	**Contention error** This error indicates a contention error happened during transmission
6	FALSE_CTRL_ERR	**False control error** This error indicates a LP-Rqst is not followed by a valid escape or turnaround sequence, or a HS-Rqst is not correctly followed by a bridge state from RX
5	ESC_SYNC_ERR	**Escape mode sync error** This error indicates the last bit of a transmission does not match a byte boundary

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Bit(s)	Name	Description
4	ESC_ENTRY_ERR	**Escape mode entry error** This error indicates an invalid escape entry command from RX
1	BUFFER_UNDERRUN	**Buffer underrun error** This error indicates the DSI throughput exceeds data throughput and makes invalid data transmission

14011008 **DSI_INTEN** **DSI Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					SKEWCAL_DONE_INT_EN	VM_VFP_STR_INT_EN	VM_VACT_STR_INT_EN	VM_VBP_STR_INT_EN	TE_TIMEOUT_INT_EN	SLEEPOUT_DONE_INT_EN	VM_CMD_DONE_INT_EN	FRAME_DONE_INT_EN	VM_DONE_INT_EN	TE_RDY_INT_EN	CMD_DONE_INT_EN	LPRX_RD_RDY_INT_EN
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	SKEWCAL_DONE_INT_EN	**Skew-calibration done interrupt** This interrupt will be issued when skew-calibration process started by SKEWCAL_START is done 0: Disable 1: Enable
10	VM_VFP_STR_INT_EN	**Video mode VFP period start interrupt** This interrupt will be issued when VFP period start during video mode transmission 0: Disable 1: Enable
9	VM_VACT_STR_INT_EN	**Video mode VACT period start interrupt** This interrupt will be issued when VACT period start during video mode transmission 0: Disable 1: Enable
8	VM_VBP_STR_INT_EN	**Video mode VBP period start interrupt** This interrupt will be issued when VBP period start during video mode transmission 0: Disable 1: Enable
7	TE_TIMEOUT_INT_EN	**TE timeout interrupt** This interrupt will be issued when the wait time of TE signal exceeds SW-configured threshold 0: Disable 1: Enable
6	SLEEPOUT_DONE_INT_EN	**Enables ULPS sleep-out interrupt** The interrupt will be issued when ULPS sleep out procedure is completed 0: Disable 1: Enable
5	VM_CMD_DONE_I	**Enables DSI video mode command packet transmission interrupt**

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Bit(s)	Name	Description
	NT_EN	This interrupt will be issued when command packet transmission during video mode is completed 0: Disable 1: Enable
4	FRAME_DONE_INT_EN	**Frame done interrupt** This interrupt will be issued when the frame transmission is done, both for video and command mode 0: Disable 1: Enable
3	VM_DONE_INT_EN	**Enables DSI video mode finished interrupt** This interrupt will be issued when video mode transmission is finished 0: Disable 1: Enable
2	TE_RDY_INT_EN	**DSI TE ready interrupt** This interrupt will be issued when either BTA TE or external TE is received 0: Disable 1: Enable
1	CMD_DONE_INT_EN	**Enables DSI command mode finished interrupt** This interrupt will be issued when all commands set in command queue are executed 0: Disable 1: Enable
0	LPRX_RD_RDY_INT_EN	**Enables RX data-ready interrupt** This interrupt will be issued when RX data are received through read commands. It is recommended to enable this interrupt to receive data because the read response may be overwritten if another read command exists. An RACK operation should be set after reading data to allow HW continue execution 0: Disable 1: Enable

1401100C **DSI_INTSTA** **DSI Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DSI_BUSY															
Type	RU															
Reset	0															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					SKEWCAL_DONE_INT_FLAG	VM_VFP_STR_INT_FLAG	VM_VACT_STR_INT_FLAG	VM_VBP_STR_INT_FLAG	TE_TIMEOUT_INT_FLAG	SLEEPOUT_DONE_INT_FLAG	VM_CMD_DONE_INT_FLAG	FRAME_DONE_INT_FLAG	VM_DONE_INT_FLAG	TE_RDY_INT_FLAG	CMD_DONE_INT_FLAG	LPRX_RD_RDY_INT_FLAG
Type					A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	DSI_BUSY	**DSI busy status** 0: Idle 1: Busy

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Bit(s)	Name	Description
11	SKEWCAL_DONE_INT_FLAG	**Skew-calibration done interrupt status** 0: Clear interrupt 1: No effect
10	VM_VFP_STR_INT_FLAG	**Video mode VFP period start interrupt status** 0: Clear interrupt 1: No effect
9	VM_VACT_STR_INT_FLAG	**Video mode VACT period start interrupt status** 0: Clear interrupt 1: No effect
8	VM_VBP_STR_INT_FLAG	**Video mode VBP period start interrupt status** 0: Clear interrupt 1: No effect
7	TE_TIMEOUT_INT_FLAG	**TE time-out interrupt status** 0: Clear interrupt 1: No effect
6	SLEEPOUT_DONE_INT_FLAG	**ULPS sleep-out done interrupt status.** 0: Clear interrupt 1: No effect
5	VM_CMD_DONE_INT_FLAG	**DSI video mode command packet transmission interrupt status** 0: Clear interrupt 1: No effect
4	FRAME_DONE_INT_FLAG	**Frame done interrupt status** 0: Clear interrupt 1: No effect
3	VM_DONE_INT_FLAG	**DSI video mode finish interrupt status** 0: Clear interrupt 1: No effect
2	TE_RDY_INT_FLAG	**DSI TE ready interrupt status** 0: Clear interrupt 1: No effect
1	CMD_DONE_INT_FLAG	**DSI command mode finish interrupt status** 0: Clear interrupt 1: No effect
0	LPRX_RD_RDY_INT_FLAG	**RX data-ready interrupt status** 0: Clear interrupt 1: No effect

14011010 **DSI_COM_CON** **DSI Common Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												DSI_DUAL_EN		DPHY_RESET		DSI_RESET
Type												RW		RW		RW
Reset												0		0		0

Bit(s)	Name	Description

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Bit(s)	Name	Description
4	DSI_DUAL_EN	**Enables DSI dual module** Enable this bit to start dual-DSI display simultaneously. 0: Disable dual start 1: Enable dual start
2	DPHY_RESET	**DIG_MIPI_TX software reset** 0: De-assert software reset 1: Assert software reset
0	DSI_RESET	**DSI module software reset** 0: De-assert software reset 1: Assert software reset

14011014 **DSI_MODE_CON** **DSI Mode Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												**SLEEP_MODE**	**C2V_SWITCH_ON**	**V2C_SWITCH_ON**	**MIX_MODE**	**FRAME_MODE**
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**MODE_CON**	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
20	SLEEP_MODE	**DSI sleep mode for ULPS wake-up operation** This mode is used during wake-up stage to leave ULPS. Set this bit to 1 before setting LANE_NUM to enable output data lane to LP-00; then set up SLEEPOUT_START to start the ULPS-exit process. 0: Disable 1: Enable
19	C2V_SWITCH_ON	**DSI auto-switch from command mode to video mode.** Set up this bit to wait for last TE and start video mode when running in command mode with TE 0: Disable 1: Enable
18	V2C_SWITCH_ON	**DSI auto-switch from video mode to command mode** Set up this bit to send last vsync and switch to command idle when running in video mode 0: Disable 1: Assert
17	MIX_MODE	**Mixed mode for command / video transmission.** Set up this bit to allow command packets in command queue transmitted after every VFP period in video mode 0: Disable 1: Enable
16	FRAME_MODE	**Single frame mode for video mode** Set up this bit to make DSI return to idle after each frame transmitted in video mode. 0: Disable 1: Enable

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Bit(s)	Name	Description
1:0	MODE_CON	**DSI mode control** Set DSI_EN = 1 when changing this register 0: Command mode 1: Sync-pulse video mode 2: Sync-event video mode 3: Burst video mode

14011018 **DSI_TXRX_CON** **DSI TX RX Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													**TE_TIMEOUT_CHK_EN**	**TE_WITH_CMD_EN**	**TYPE1_BTA_SEL**	**HSTX_CKLP_EN**
Type													RW	RW	RW	RW
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MAX_RTN_SIZE**				**TE_AUTO_SYNC**	**EXT_TE_EDGE_SEL**	**EXT_TE_EN**	**TE_FREERUN**	**HSTX_BLLP_EN**	**HSTX_DIS_EOT**	**LANE_NUM**				**VC_NUM**	
Type	RW				RW	RW	RW	RW	RW	RW	RW				RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	TE_TIMEOUT_CHK_EN	**Enables TE time-out check mechanism** Enable this bit to turn on DSI TE and external TE time-out check mechansim based on wait time of TE_TIMEOUT. 0: Disable 1: Enable
18	TE_WITH_CMD_EN	**In the tradition design, TE command excutes 'bus turnaround' and ignores other settings in the same command column. Combine the TE bit and other commands if this bit is asserted.** 0: Disable 1: Enable
17	TYPE1_BTA_SEL	**Selects TYPE1 BTA machenism** 0: TYPE1 BTA by frame 1: TYPE1 BTA by packet
16	HSTX_CKLP_EN	**Enables non-continuous clock lane** 0: Disable 1: Enable
15:12	MAX_RTN_SIZE	**Maximum return packet size** This register constrains maximum return packet that the slave side will send back to the host. It takes effect after the host sends 'Set Maximum Return Packet Size' packet to slave.
11	TE_AUTO_SYNC	**Enables TE auto-sync** Turn-on this register to automatically receive TE signals when command mode is idle. This bit is useful in command mode only. 0: Disable TE auto sync 1: Enable TE auto sync
10	EXT_TE_EDGE_SEL	**Selects trigger edge type of external TE** 0: Rising edge

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Bit(s)	Name	Description
		1: Falling edge
9	EXT_TE_EN	**Enables external TE signal** This bit should be set to receive external TE if LPTE pin is used as external TE pin 0: Disable 1: Enable
8	TE_FREERUN	**TE free-run mode** If disabled, SW needs to wait for TE, write RACK and re-trigger DSI_START for the next transmission. If enabled, HW will detect TE and automatically to start the next transmission until it is disabled 0: Disable free-run mode 1: Enable free-run mode
7	HSTX_BLLP_EN	**Enables null packet transfer in BLLP.** 0: Disable 1: Enable
6	HSTX_DIS_EOT	**Disables end of transmission packet.** 0: Enable EoTp 1: Disable EoTp
5:2	LANE_NUM	**Lane number** Set up this bit to turn on PRE_OE to enable lane circuit. 4'b0000: Disable all lanes 4'b0001: Enable 1 lane 4'b0011: Enable 2 lanes 4'b0111: Enable 3 lanes 4'b1111: Enable 4 lanes
1:0	VC_NUM	**Virtual channel parameter in video mode.**

1401101C DSI_PSCON DSI Pixel Stream Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							BYTE_SWAP	RGB_SWAP							DSI_PS_SEL	
Type							RW	RW							RW	
Reset							0	0							0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DSI_PS_WC													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25	BYTE_SWAP	**Selects byte order** For RGB565 type, it select to swap bytes between MSB and LSB. For other stream typs, this bit is not used. 0: Normal case 1: Byte order change
24	RGB_SWAP	**Selects order of RGB** For all color types, it changes the color order in format of RGB or BGR. 0: Normal case 1: R/B order change
17:16	DSI_PS_SEL	**Selects pixel stream type** 0: Packed pixel stream with 16-bit RGB 5-6-5 format 1: Packed pixel stream with 18-bit RGB 6-6-6 format

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Bit(s)	Name	Description
		2: Loosely pixel stream with 24-bit RGB 6-6-6 format 3: Packed pixel stream with 24-bit RGB 8-8-8 format
13:0	DSI_PS_WC	**Word count of long packet in valid pixel data duration** Unit: Byte This value must be (H_SIZE*BPP). Take the QVGA display as an example, the value of PS_WC is (240*3) = 720 in decimal.

14011020 **DSI_VSA_NL** **DSI Vertical Sync Active Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							VSA_NL									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	VSA_NL	**Vertical sync active duration** Unit: Line

14011024 **DSI_VBP_NL** **DSI Vertical Back Porch Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							VBP_NL									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	VBP_NL	**Vertical back porch duration** Unit: Line

14011028 **DSI_VFP_NL** **DSI Vertical Front Porch Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							VFP_NL									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
9:0	VFP_NL	**Vertical front porch duration** Unit: Line

1401102C DSI_VACT_NL DSI Vertical Active Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					VACT_NL											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	VACT_NL	**Vertical active duration** Configures frame height of pixels in video mode and command mode.

14011030 DSI_LFR_CON DSI Low Frame Rate Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name			DSI_LFR_SKIP_NUM							DSI_LFR_VSE_DIS	DSI_LFR_UPDATE	DSI_LFR_EN	DSI_LFR_TYPE		DSI_LFR_MODE	
Type			RW							RW	RW	RW	RW		RW	
Reset			0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
13:8	DSI_LFR_SKIP_NUM	**Low frame rate skip frame number** Configure this register to control the number of frames to skip in LFR static mode.
6	DSI_LFR_VSE_DIS	**Disables low frame rate VSE** Set this bit to 1 to disable Vsync End packet transmission when low frame rate type is vsync only. 0: Enable VSE packet 1: Disable VSE packet
5	DSI_LFR_UPDATE	**Low frame rate update in dynamic mode** Set this bit from 0 to 1 to send one normal frame in LFR dynamic mode. In both modes, updating frames will reset the skip frame counter. 0: No effect 1: Update frame
4	DSI_LFR_EN	**Enables low frame rate** Set this bit to 1 to enable LFR (Low Frame Rate) mode. 0: Disable 1: Enable

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Bit(s)	Name	Description
3:2	DSI_LFR_TYPE	**Low frame rate transmission type** Selects packet types to be transmitted in skip frame 0: LP mode (no transmission) 1: Vsync only 2: Hsync only 3: Vsync + Hsync
1:0	DSI_LFR_MODE	**Low frame rate mode** Selects which mode is used for LFR control. Static mode allows DSI to send one normal frame per skip frames based on DSI_LFR_SKIP_NUM autometically, and dynamic mode allows software to control when to send normal frame manually. 0: Disable 1: Static mode 2: Dynamic mode 3: Both

14011034 **DSI_LFR_STA** **DSI Low Frame Rate Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name								DSI_LFR_SKIP_STA			DSI_LFR_SKIP_CNT					
Type								RU			RU					
Reset								0			0	0	0	0	0	0

Bit(s)	Name	Description
8	DSI_LFR_SKIP_STA	**Low frame rate skip frame status** 0: Normal frame 1: Skip frame
5:0	DSI_LFR_SKIP_CNT	**Low frame rate skip frame counter** Shows current frame count of skip frames in static mode

14011050 **DSI_HSA_WC** **DSI Horizontal Sync Active Word Count Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					DSI_HSA_WC											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	DSI_HSA_WC	**Word count of horizontal sync active duration**

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Bit(s)	Name	Description
		Follow the program sequence and configure sync pulse mode.

14011054 **DSI_HBP_WC** **DSI Horizontal Back Porch Word Count Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DSI_HBP_WC											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	DSI_HBP_WC	**Word count of horizontal sync back porch duration** Follow the program sequence and configure all video mode.

14011058 **DSI_HFP_WC** **DSI Horizontal Front Porch Word Count Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DSI_HFP_WC											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	DSI_HFP_WC	**Word count of horizontal sync front porch duration** Follow the program sequence and configure all video mode.

1401105C **DSI_BLLP_WC** **DSI Horizontal Blanking or Low Power Mode Word Count Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DSI_BLLP_WC											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	DSI_BLLP_WC	**Word count of horizontal blanking or low power mode duration** Follow the program sequence and configure burst mode.

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14011060	DSI_CMDQ_CON	DSI Command Queue Control Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CMDQ_SIZE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	CMDQ_SIZE	**Number of commands in command queue** Range: 1 ~ 127

14011064	DSI_HSTX_CKLP_WC	DSI HSTX Clock Low-power Mode Word Count Register	00010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																HSTX_CKLP_WC_AUTO
Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HSTX_CKLP_WC															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
16	HSTX_CKLP_WC_AUTO	**Automatic calculation for HSTX_CKLP_WC**
15:2	HSTX_CKLP_WC	**Word count of non-continuous clock lane counter** Sets up HSTX clock low-power period when HSTX_CKLP_EN = 1. Refer to programming guide for details on the usage.

14011068	DSI_HSTX_CKLP_WC_AUTO_RESULT	DSI HSTX Clock Low-power Mode Automatic Calculation result	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HSTX_CKLP_WC_AUTO_RESULT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	HSTX_CKLP_WC_AUTO_RESULT	DSI HSTX Clock Low-power Mode Automatic Calculation result

14011074 **DSI_RX_DATA03** **DSI Receive Packet Data Byte 0 ~ 3 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BYTE3								BYTE2							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYTE1								BYTE0							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	BYTE3	RX read data buffer byte 3
23:16	BYTE2	RX read data buffer byte 2
15:8	BYTE1	RX read data buffer byte 1
7:0	BYTE0	RX read data buffer byte 0

14011078 **DSI_RX_DATA47** **DSI Receive Packet Data Byte 4 ~ 7 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BYTE7								BYTE6							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYTE5								BYTE4							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	BYTE7	RX read data buffer byte 7
23:16	BYTE6	RX read data buffer byte 6
15:8	BYTE5	RX read data buffer byte 5
7:0	BYTE4	RX read data buffer byte 4

1401107C **DSI_RX_DATA8B** **DSI Receive Packet Data Byte 8 ~ 11 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BYTEB								BYTEA							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYTE9								BYTE8							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:24	BYTEB	RX read data buffer byte 11
23:16	BYTEA	RX read data buffer byte 10
15:8	BYTE9	RX read data buffer byte 9
7:0	BYTE8	RX read data buffer byte 8

14011080 DSI_RX_DATAC DSI Receive Packet Data Byte 12 ~ 15 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BYTEF								BYTEE							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYTED								BYTEC							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	BYTEF	RX read data buffer byte 15
23:16	BYTEE	RX read data buffer byte 14
15:8	BYTED	RX read data buffer byte 13
7:0	BYTEC	RX read data buffer byte 12

14011084 DSI_RX_RACK DSI Read Data Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RACK_BYPASS	RACK
Type															RW	W1C
Reset															0	0

Bit(s)	Name	Description
1	RACK_BYPASS	**Enables RX read acknowledge bypass** Set this bit to enable to ignore RACK from SW and continue next commands 1: Does not check RACK 0: Check RACK
0	RACK	**Acknowledges RX read** When a read command is executed and read data are received completely, the LPRX_RD_RDY interrupt will be issued. After read from the RX_DATA buffer, set up this bit to continue to the next command. 1: Acknowledge 0: No effect

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14011088 **DSI_RX_TRIG_STA** **DSI Receiver Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_POINTER					RX_LPDT	DIRECTION	RX_ULPS	RX_TRIG_3	RX_TRIG_2	RX_TRIG_1	RX_TRIG_0
Type					RU					RU	RU	RU	RU	RU	RU	RU
Reset					0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
11:8	RX_POINTER	**RX data count**
6	RX_LPDT	**RX low power data transmission state**
5	DIRECTION	**Escape turnaround direction** Current bus direction of Data Lane 0. If set to 1, there will be reverse direction transmission on Data Lane0 in Low Power mode. Otherwise, it will be a forward direction transmission. 1: Reverse direction 0: Forward direction
4	RX_ULPS	**RX ULPS (Ultra-low power state)** Entry pattern is 00011110
3	RX_TRIG_3	**Reserved by DSI specification.** Entry pattern is 10100000
2	RX_TRIG_2	**Acknowledge.** Entry pattern is 00100001
1	RX_TRIG_1	**TE.** Entry pattern is 01011101
0	RX_TRIG_0	**Remote application reset.** Entry pattern is 01100010

14011090 **DSI_MEM_CONTI** **DSI Memory Continue Command Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DSI_RWMEM_CONTI															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DSI_RWMEM_CONTI	Read/Write memory continue command

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14011094 DSI_FRM_BC DSI Frame Byte Count Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												DSI_FRM_BC[20:16]				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DSI_FRM_BC[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	DSI_FRM_BC	**Frame buffer byte count** The total number of byte is expected to be read for type3 command.

14011098 DSI_V3D_CON DSI Vsync 3D Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								V3D_EN			V3D_LR	V3D_VSYNC	V3D_FMT		V3D_MODE	
Type								RW			RW	RW	RW		RW	
Reset								0			0	0	0	0	0	0

Bit(s)	Name	Description
8	V3D_EN	Enables 3D control payload to be present in video mode VSS packet
5	V3D_LR	3D left/right order
4	V3D_VSYNC	Enables the second VSYNC between images on the left and right
3:2	V3D_FMT	3D image format
1:0	V3D_MODE	3D mode on/off, display orientation

140110A0 DSI_TIME_CON0 DSI Timing Control 0 Register 00060080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SKEWCAL_PRD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ULPS_WAKEUP_PRD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SKEWCAL_PRD	**Skew calibration period** Cycle count for skew-calibration period defined in DPHY 1.2 spec to continuously send out calibration patterns.

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Bit(s)	Name	Description
		Total time = (SKEWCAL_PRD*1024*DSI clock cycle time) Default value: 45us under 130MHz DSI byte clock
15:0	ULPS_WAKEUP_PRD	**ULPS wakeup period** Cycle count for ultra-low power state (ULPS) wake-up during ULPS-exit sequence. Total wait time = (ULPS_WAKEUP_PRD*1024*DSI clock cycle time) Default value: 1ms under 130MHz DSI byte clock

140110A4 **DSI_TIME_CON1** **DSI Timing Control 1 Register** **00002000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TE_TIMEOUT_PRD															
Type	RW															
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TE_TIMEOUT_PRD	**TE time-out check period** Cycle count to check TE time-out and issue time-out interrupt when waiting for TE signal. Total wait time = (TE_TIMEOUT_PRD*16384*DSI clock cycle time) Default value: 1sec under 130MHz DSI byte clock

14011100 **DSI_PHY_LCPAT** **DSI PHY Lane Clock Pattern Register** **00000055**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									LC_HSTX_CK_PAT							
Type									RW							
Reset									0	1	0	1	0	1	0	1

Bit(s)	Name	Description
7:0	LC_HSTX_CK_PAT	**Clock lane HSTX clock pattern** Configure this field to generate HSTX clock pattern and change polarity. Default: Rising edge pulse first

14011104 **DSI_PHY_LCCON** **DSI PHY Lane Clock Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														LC_WAKEUP_EN	LC_ULPM_EN	LC_HSTX_EN
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	LC_WAKEUP_EN	**Enables clock lane wake-up** Make the clock lane wake-up from ultra-low power mode. Make sure DSI_EN = 1 when setting this register
1	LC_ULPM_EN	**Enables clock lane ULPS** Make the clock lane go to ultra-low power mode. Make sure DSI_EN = 1 when setup this register
0	LC_HSTX_EN	**Enables clock lane HS mode** Start clock lane high speed transmission.

14011108 **DSI_PHY_L0CON** **DSI PHY Lane 0 Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												L0_RX_FILTER_EN	LX_ULPM_AS_L0	L0_WAKEUP_EN	L0_ULPM_EN	L0_RM_TRIG_EN
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	L0_RX_FILTER_EN	**Enables data lane 0 RX glitch filter** If the MIPI RX signal from peripheral is not stable, set up this bit to filter the signal glitches
3	LX_ULPM_AS_L0	**Enables data lane 1/2/3 ULPS mode** Set up this bit to make data lane 1/2/3 enter ULPS accompanied by data lane 0.
2	L0_WAKEUP_EN	**Enables data lane 0 wake-up** Make the data lane 0 wake-up from ultra-low power mode.
1	L0_ULPM_EN	**Enables data lane 0 ULPS** Make the data lane 0 go to ultra-low power mode.
0	L0_RM_TRIG_EN	**Enables data lane 0 remote application trigger** Send application trigger to slave side.

1401110C **DSI_PHY_SYNCON** **DSI PHY Sync Control Register** **000000B8**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								HS_	HS_SKEWCAL_PAT							

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								DB_SYNC_EN								
Type								RW	RW							
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HS_SYNC_CODE2								HS_SYNC_CODE							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	0

Bit(s)	Name	Description
24	HS_DB_SYNC_EN	**Enables HSTX double-byte sync code** Set this bit to 1 if 16-bit sync code is to be sent. The LSB is HS_SYNC_CODE; the MSB is HS_SYNC_CODE2.
23:16	HS_SKEWCAL_PAT	**HSTX skew calibration pattern** Set up this bit to transmit continuous pattern code for skew calibration.
15:8	HS_SYNC_CODE2	**HSTX sync code 2** If a sync code with 16-bit length is sent, fill out this field.
7:0	HS_SYNC_CODE	**HSTX sync code** Sync code byte sent for high-speed transmission

14011110 DSI_PHY_TIMCON0 DSI PHY Timing Control 0 Register 14140A0A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DA_HS_TRAIL								DA_HS_ZERO							
Type	RW								RW							
Reset	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_HS_PREP								LPX							
Type	RW								RW							
Reset	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
31:24	DA_HS_TRAIL	Control for timing parameter: T_HS-Trail
23:16	DA_HS_ZERO	Control for timing parameter: T_HS-Zero
15:8	DA_HS_PREP	Control for timing parameter: T_HS-Prepare
7:0	LPX	Control for timing parameter: T_LPX

14011114 DSI_PHY_TIMCON1 DSI PHY Timing Control 1 Register 0E1A1632

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DA_HS_EXIT								TA_GET							
Type	RW								RW							
Reset	0	0	0	0	1	1	1	0	0	0	0	1	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TA_SURE								TA_GO							
Type	RW								RW							
Reset	0	0	0	1	0	1	1	0	0	0	1	1	0	0	1	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:24	DA_HS_EXIT	Control for timing parameter: T_HS-Exit for data lane
23:16	TA_GET	Control for timing parameter: T_TA-Get
15:8	TA_SURE	Control for timing parameter: T_TA-Sure
7:0	TA_GO	Control for timing parameter: T_TA-Go

14011118 **DSI_PHY_TIMCON2** **DSI PHY Timing Control 2 Register** **14140100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CLK_HS_TRAIL								CLK_HS_ZERO							
Type	RW								RW							
Reset	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_HS_SYNC								CONT_DET							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	CLK_HS_TRAIL	Control for timing parameter: T_CLK-Trail
23:16	CLK_HS_ZERO	Control for timing parameter: T_CLK-Zero
15:8	DA_HS_SYNC	Control for timing parameter: T_HS-Sync
7:0	CONT_DET	Control for contention detection cycle

1401111C **DSI_PHY_TIMCON3** **DSI PHY Timing Control 3 Register** **000E0E0A**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CLK_HS_EXIT							
Type									RW							
Reset									0	0	0	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_HS_POST								CLK_HS_PREP							
Type	RW								RW							
Reset	0	0	0	0	1	1	1	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
23:16	CLK_HS_EXIT	Control for timing parameter: T_HS-Exit for clock lane
15:8	CLK_HS_POST	Control for timing parameter: T_CLK-Post
7:0	CLK_HS_PREP	Control for timing parameter: T_CLK-Prepare

14011130 **DSI_VM_CMD_CON** **DSI Video Mode Command Packet Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CM_DATA_1								CM_DATA_0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CM_DATA_ID										TS_	TS_	TS_	TIM	LON	VM_

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											VFP _EN	VBP _EN	VSA _EN	E_S EL	G_P KT	CMD _EN
Type	RW										RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
31:24	CM_DATA_1	**Command packet data byte 1** If short packet, the byte will be used as DATA 1. If long packet, this registers should be 0 because word count should be less than 16 bytes.
23:16	CM_DATA_0	**Command packet data byte 0** If short packet, the byte will be used as DATA 0. If long packet, this registers should be used as Word Count 0 for long packet
15:8	CM_DATA_ID	**Command packet data ID** Note: The packet data ID should contain both data type and VC.
5	TS_VFP_EN	**Command packet is allowable in VFP period** 0: Disable 1: Enable
4	TS_VBP_EN	**Command packet is allowable in VBP period** 0: Disable 1: Enable
3	TS_VSA_EN	**Command packet is allowable in VSA period** 0: Disable 1: Enable
2	TIME_SEL	**Timing interval for transmission** Allowable timing interval for command transmission in BLLP period. Select RGB if the HBP interval length is shorter than long packet length to be sent. 0: HBP timing interval 1: RGB timing interval
1	LONG_PKT	**Command packet type** 0: Short packet 1: Long packet
0	VM_CMD_EN	**Enables video mode command packet transmission** 0: Disable 1: Enable

14011134 **DSI_VM_CMD_DATA0** **DSI Video Mode Command Packet Data Byte 0~3 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD	**Command packet word** Command packet data byte 0~3 of long packet for video mode transmission

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14011138	DSI_VM_CMD_DATA4	DSI Video Mode Command Packet Data Byte 4~7 Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD	**Command packet word** Command packet data byte 4~7 of long packet for video mode transmission

1401113C	DSI_VM_CMD_DATA8	DSI Video Mode Command Packet Data Byte 8~11 Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD	**Command packet word** Command packet data byte 8~11 of long packet for video mode transmission

14011140	DSI_VM_CMD_DATAC	DSI Video Mode Command Packet Data Byte 12~15 Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD	**Command packet word** Command packet data byte 12~15 of long packet for video mode transmission

14011144	DSI_CKSM_OUT	DSI Checksum Output	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	ACC_CHKSUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PKT_CHKSUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ACC_CHKSUM	**Accumulated packet checksum** Checksum value of sequentially accumulated packets for System Level Test (SLT)
15:0	PKT_CHKSUM	**Transmitted packet checksum** Checksum value of the last transmitted packet for System Level Test (SLT)

14011148 DSI_STATE_DBG0 DSI State Machine Debug 0 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												DPHY_HS_TX_STATE_C				
Type												RU				
Reset												0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DPHY_CTL_STATE_C								
Type								RU								
Reset								0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
20:16	DPHY_HS_TX_STATE_C	DSI DPHY clock lane HSTX state monitor
8:0	DPHY_CTL_STATE_C	DSI DPHY clock lane control state monitor

1401114C DSI_STATE_DBG1 DSI State Machine Debug 1 01010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DPHY_ESC_STATE_0											DPHY_HS_TX_STATE_0				
Type	RU											RU				
Reset	0	0	0	0	0	0	0	1				0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DPHY_CTL_STATE_0														
Type		RU														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:24	DPHY_ESC_STATE_0	DSI DPHY data lane 0 escape state monitor
20:16	DPHY_HS_TX_STATE_0	DSI DPHY data lane 0 HSTX state monitor
14:0	DPHY_CTL_STATE_0	DSI DPHY data lane 0 control state monitor

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14011150 DSI_STATE_DBG2 DSI State Machine Debug 2 01010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DPHY_TA_R2T_STATE								DPHY_TA_T2R_STATE				
Type				RU								RU				
Reset				0	0	0	0	1				0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							DPHY_RX_ESC_STATE									
Type							RU									
Reset							0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
28:24	DPHY_TA_R2T_STATE	DSI DPHY data lane 0 turnaround RX to TX state monitor
20:16	DPHY_TA_T2R_STATE	DSI DPHY data lane 0 turnaround TX to RX state monitor
9:0	DPHY_RX_ESC_STATE	DSI DPHY data lane 0 LPRX escape state monitor

14011154 DSI_STATE_DBG3 DSI State Machine Debug 3 01010101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DPHY_HS_TX_STATE_2								DPHY_CTL_STATE_2				
Type				RU								RU				
Reset				0	0	0	0	1				0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DPHY_HS_TX_STATE_1								DPHY_CTL_STATE_1				
Type				RU								RU				
Reset				0	0	0	0	1				0	0	0	0	1

Bit(s)	Name	Description
28:24	DPHY_HS_TX_STATE_2	DSI DPHY data lane 2 HSTX state monitor
20:16	DPHY_CTL_STATE_2	DSI DPHY data lane 2 control state monitor
12:8	DPHY_HS_TX_STATE_1	DSI DPHY data lane 1 HSTX state monitor
4:0	DPHY_CTL_STATE_1	DSI DPHY data lane 1 control state monitor

14011158 DSI_STATE_DBG4 DSI State Machine Debug 4 00000101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DPHY_HS_TX_STATE_3								DPHY_CTL_STATE_3				
Type				RU								RU				
Reset				0	0	0	0	1				0	0	0	0	1

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Bit(s)	Name	Description
12:8	DPHY_HS_TX_STATE_3	DSI DPHY data lane 3 HSTX state monitor
4:0	DPHY_CTL_STATE_3	DSI DPHY data lane 3 control state monitor

1401115C DSI_STATE_DBG5 DSI State Machine Debug 5 10000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WAKEUP_STATE															TIMER_BUSY
Type	RU															RU
Reset	0	0	0	1												0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TIMER_COUNTER															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	WAKEUP_STATE	DSI sleep-out state monitor
16	TIMER_BUSY	DSI sleep mode/TE time-out timer busy status
15:0	TIMER_COUNTER	DSI sleep mode/TE time-out timer counter

14011160 DSI_STATE_DBG6 DSI State Machine Debug 6 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										CMDQ_STATE						
Type										RU						
Reset										0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CMCTL_STATE														
Type		RU														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
22:16	CMDQ_STATE	DSI command queue state monitor
14:0	CMCTL_STATE	DSI command control state monitor

14011164 DSI_STATE_DBG7 DSI State Machine Debug 7 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	VSA_PERIOD	VBP_PERIOD	VACT_PERIOD	VFP_PERIOD		VMCTL_STATE										
Type	RU	RU	RU	RU		RU										
Reset	0	0	0	0		0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15	VSA_PERIOD	DSI video mode VSA indication
14	VBP_PERIOD	DSI video mode VBP indication
13	VACT_PERIOD	DSI video mode VACT indication
12	VFP_PERIOD	DSI video mode VFP indication
10:0	VMCTL_STATE	DSI video mode control state monitor

14011168 DSI_STATE_DBG8 DSI State Machine Debug 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			WORD_COUNTER													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	WORD_COUNTER	DSI packet word count monitor

1401116C DSI_STATE_DBG9 DSI State Machine Debug 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											LINE_COUNTER[21:16]					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LINE_COUNTER[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	LINE_COUNTER	DSI packet line count monitor

14011170 DSI_DEBUG_SEL DSI Debug Output Selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								CHKSUM_REC_EN				DEBUG_OUT_SEL				
Type								RW				RW				
Reset								0				0	0	0	0	0

Bit(s)	Name	Description
8	CHKSUM_REC_EN	**Enables checksum record** Set this bit to enable checksum record circuit to obtain PKT_CHKSUM and ACC_CHKSUM in DSI_CKSM_OUT register.
4:0	DEBUG_OUT_SEL	**Selects DSI debug out** This register selects which group of internal signal is sent to debug output port. It is only for hardware debug purpose and not described here.

14011174 **DSI_RESERVED** **Reserved Register** **FFF00000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DSI_RESERVED[31:16]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DSI_RESERVED[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DSI_RESERVED	DSI reserved register for HW usage

14011178 **DSI_BIST_PATTERN** **DSI Bist Pattern Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BIST_PATTERN[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIST_PATTERN[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BIST_PATTERN	DSI BIST test register for HW verification

1401117C **DSI_BIST_CON** **DSI Bist Control Register** **00200000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BIST_TIMIING							

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Type									RW							
Reset									0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					BIST_LANE_NUM					SELF_PAT_MODE		BIST_HS_FREE	BIST_SPECIFIED_PATTERN	BIST_FIX_PATTERN	BIST_ENABLE	BIST_MODE
Type					RW					RW		RW	RW	RW	RW	RW
Reset					0	0	0	0		0		0	0	0	0	0

Bit(s)	Name	Description
23:16	BIST_TIMIING	**BIST timing control for MIPI signal**
11:8	BIST_LANE_NUM	**BIST lane number** 4'b0000: Disable all lanes 4'b0001: Enable 1 lane 4'b0011: Enable 2 lanes 4'b0111: Enable 3 lanes 4'b1111: Enable 4 lanes
6	SELF_PAT_MODE	**Enables the self-pattern test mode to show built-in pattens according to configuration of BIST_PATTERN value** 0: Disable 1: Enable
4	BIST_HS_FREE	**Enables BIST free run test** 0: Normal mode 1: Free-run mode
3	BIST_SPECIFIED_PATTERN	**Enables BIST specified pattern** 0: Not specified pattern 1: Specified pattern
2	BIST_FIX_PATTERN	**Enables BIST fix pattern** 0: Not fix pattern 1: Fix pattern
1	BIST_ENABLE	**Start BIST mode** 0: No effect 1: Trigger
0	BIST_MODE	**Enables BIST mode** 0: Disable 1: Enable

14011180 **DSI_VM_CMD_DATA10** **DSI Video Mode Command Packet Data Byte 16~19 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD	**Command packet word**

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Bit(s)	Name	Description
		Command packet data byte 16~19 of long packet for video mode transmission

14011184 **DSI_VM_CMD_DATA14** **DSI Video Mode Command Packet Data Byte 20~23 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD	**Command packet word** Command packet data byte 20~23 of long packet for video mode transmission

14011188 **DSI_VM_CMD_DATA18** **DSI Video Mode Command Packet Data Byte 24~27 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD	**Command packet word** Command packet data byte 24~27 of long packet for video mode transmission

1401118C **DSI_VM_CMD_DATA1C** **DSI Video Mode Command Packet Data Byte 28~31 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD	**Command packet word** Command packet data byte 28~31 of long packet for video mode transmission

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14011200 ~140113FC	DSI_CMDQ[n] (n=0~127)	DSI Command Queue	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA_1								DATA_0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_ID								RESV		TE	CL	HS	BTA	TYPE	
Type	RW								RW		RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	DATA_1	**Data byte 1 of command**
23:16	DATA_0	**Data byte 0 of command**
15:8	DATA_ID	**Data ID of command**
7:6	RESV	**Reserved**
5	TE	**Enables internal or external TE** 0:Disable 1: Enable
4	CL	**Selects DCS byte** 0: 1-byte DCS 1: 2-byte DCS
3	HS	**Enables high-speed transmission** 0: LPTX transmission 1: HSTX transmission
2	BTA	**Enables BTA** 0: Disable 1: Enable
1:0	TYPE	**Command types** 0: Type-0 command 1: Type-1 command 2: Type-2 command 3: Type-3 command

6.21.4 Programming Guide

6.21.4.1 Clock Control

After enabling PLL clock from MIPI DPHY macro and CG cells in MMSYS, a primary module clock enable should be set to turn on for the entire design (see Table 6-8). To disable clock for DSI, unset it. For more details on MIPI DPHY PLL clock control, refer to the functional specification of MIPI TX Config module.

Table 6-8. Sequence to enable module clock

Step	Description	R/W	Register [bit]	Value
1	Enable primary module clock	W	DSI_COM_CON [1]	1

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6.21.4.2 DSI HS Clock Control

After enabling the module clock and properly setting up the related registers, it is necessary to enable the clock lane before starting high-speed data transmission by setting up the DSI_PHY_LCCON register. Please follow the steps shown in Table 6-9 to turn on the high-speed clock.

Table 6-9. Sequence to enable high-speed clock

Step	Description	R/W	Register [bit]	Value
1	Enable DSI high-speed clock	W	DSI_PHY_LCCON [0]	1

To disable high-speed clock, follow steps in Table 6-10. Sequence of exiting ultra-low power mode on clock lane Note that the high-speed clock should be turned off before ultra-low power mode.

Table 6-10. Sequence of exiting ultra-low power mode on clock lane

Step	Description	R/W	Register [bit]	Value
1	Disable DSI high-speed clock	W	DSI_PHY_LCCON [0]	0

6.21.4.3 DSI ULPS Enter Control

In cetain condition, the DISP subsys may be powered off after DSI entering the *ultra-low power state* (ULPS) to reduce more power consumption. ULPS is a protocol defined in MIPI spec and force LCM to enter standby scenario to save power. The sleep-in control in this module is shown in Table 6-11.

Table 6-11. Sequence of sleep-in control (entering ultra-low power mode)

Step	Description	R/W	Register [bit]	Value
1	Disable DSI high-speed clock	W	DSI_PHY_LCCON [0]	0
2	Data lane enter ultra-low power mode	W	DSI_PHY_LD0CON [1]	1
3	Clock lane enter ultra-low power mode	W	DSI_PHY_LCCON [1]	1

6.21.4.4 DSI ULPS Exit Control

To wake up DSI and LCM from ULPM, executing an "ULPS-exit" procedure defined by MIPI spec is required. This procedure performs a protocol to get DP/DN signals from LP-00 through LP-10 to LP-11, where the LP-10 period should not be less than 1ms. The procedure can be easily controlled by the DSI sleep-out sequence with an interrupt indication in Table 6-12. Note that ULPS_WAKEUP_PRD should be changed according to different MIPI frequency to make sure wake-up time is not less than 1ms.

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Table 6-12. Sequence of sleep-out control (exiting ultra-low power mode)

Step	Description	R/W	Register [bit]	Value
1	Enable sleep-out interrupt	W	DSI_INTEN [6]	1
2	Configure corresponding cycle counts for ULPS wakeup period according to current MIPI frequency (ex. 1Gbps)	W	DSI_TIME_CON0 [15:0]	0x80
3	Recover lane number (4-lane)	W	DSI_TXRX_CON [5:2]	0xF
4	Sleep-out start	W	DSI_START [2]	1
5	Issue interrupt and sleep-out done	R	DSI_INTSTA [6]	1
6	Clear interrupt	W	DSI_INTSTA [6]	1

6.21.4.5 DPHY Timing Control

All of the timing parameters defined in MIPI DPHY should be properly written in the DSI registers for correct timing control. The written value is based on the DSI internal clock cycle period which is related to DPHY PLL clock settings through MIPI TX Config engine.

For example, the timing parameter $T_{HS\text{-}PREPARE}$ is mandatory to be between 40ns+4*UI and 85ns +6*UI, where UI means time interval, equal to the duration of any HS state on clock lane. If the clock lane is set to 500MHz frequency, as well as bit-rate 1Gbps, the UI should be 1ns. In other words, the value of $T_{HS\text{-}PREPARE}$ must be between 44 ~ 91ns. The internal DSI clock is 4x divided by clock lane, as well as 125MHz. To satisfy $T_{HS\text{-}PREPARE}$, the register value DA_HS_PREP should be 6 ~ 11 (see Table 6-13).

Table 6-13. DPHY timing parameters register settings

	Timing specification	Absolute time for UI: 1ns	DA_HS_PREP value
$T_{HS\text{-}PREPARE}$	40ns+4*UI ~ 85ns +6*UI	44 ~ 91 ns	6 ~ 11

Table 6-14 lists the timing parameters which should be configured in the DSI registers. Note that for different bit-rate requirements, the UI values are various. For more precise timing control, select DPHY clock as fast as possible. However, the faster DPHY clock is set, the more the power waste. A suitable clock is beneficial to the optimization of system power consumption.

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Table 6-14. DPHY global operation timing parameter defined by MIPI spec

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{CLK-MISS}$	Detection time that the clock has stopped toggling			60	ns	1
$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	60 ns + 52*UI			ns	
$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8			UI	
$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS clock transmission	38		95	ns	
$T_{CLK-TERM-EN}$	Time to enable Clock Lane receiver line termination measured from when Dn crosses $V_{IL,MAX}$	Time for Dn to reach $V_{TERM-EN}$		38	ns	
$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60			ns	
$T_{CLK-PREPARE} + T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time for lead HS-0 drive period before starting Clock	300			ns	
$T_{D-TERM-EN}$	Time to enable Data Lane receiver line termination measured from when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35 ns + 4*UI		
T_{EOT}	Time from start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$ period to start of LP-11 state			105 ns + n*12*UI		3
$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100			ns	
$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40 ns + 4*UI		85 ns + 6*UI	ns	
$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	145 ns + 10*UI			ns	
$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40		55 ns + 4*UI	ns	
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60 ns + n*4*UI)			ns	2, 3
T_{INIT}	Initialization period (PHY might calibrate)	100			µs	
T_{LPX}	Length of any Low-Power state period	50			ns	4
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}/T_{LPX(SLAVE)}$ between Master and Slave side	2/3		3/2		
T_{TA-GET}	Time to drive LP-00 by new TX		5*T_{LPX}		ns	
T_{TA-GO}	Time to drive LP-00 after Turnaround Request		4*T_{LPX}		ns	
$T_{TA-SURE}$	Time-out before new TX side starts driving	T_{LPX}		2*T_{LPX}	ns	
T_{WAKEUP}	Recovery time from Ultra-Low Power State	1			ms	

The registers of timing parameters for data lanes and clock lane are illustrated in Figure 6-60 and Figure 6-61 respectively. The registers for BTA (Bus Turn-Around) timing are illustrated in Figure 6-62.

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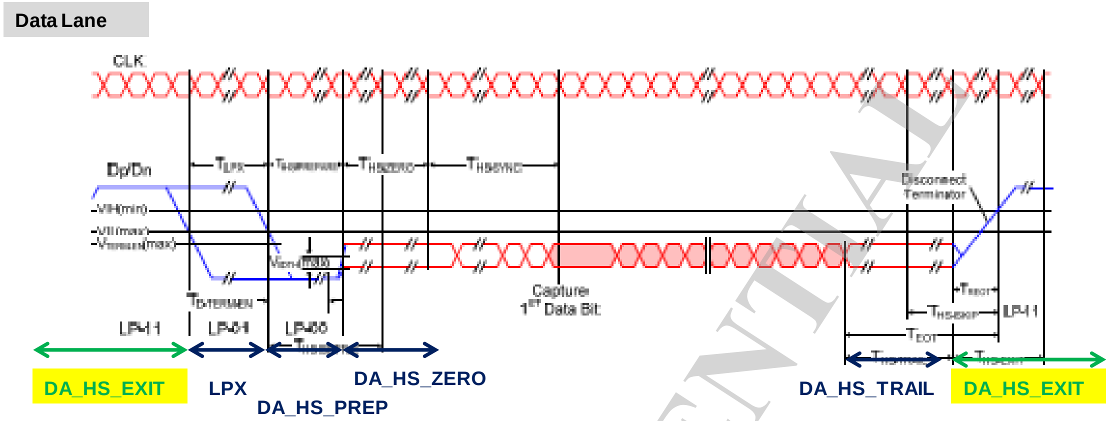

Figure 6-60.Registers for data lane timing parameters

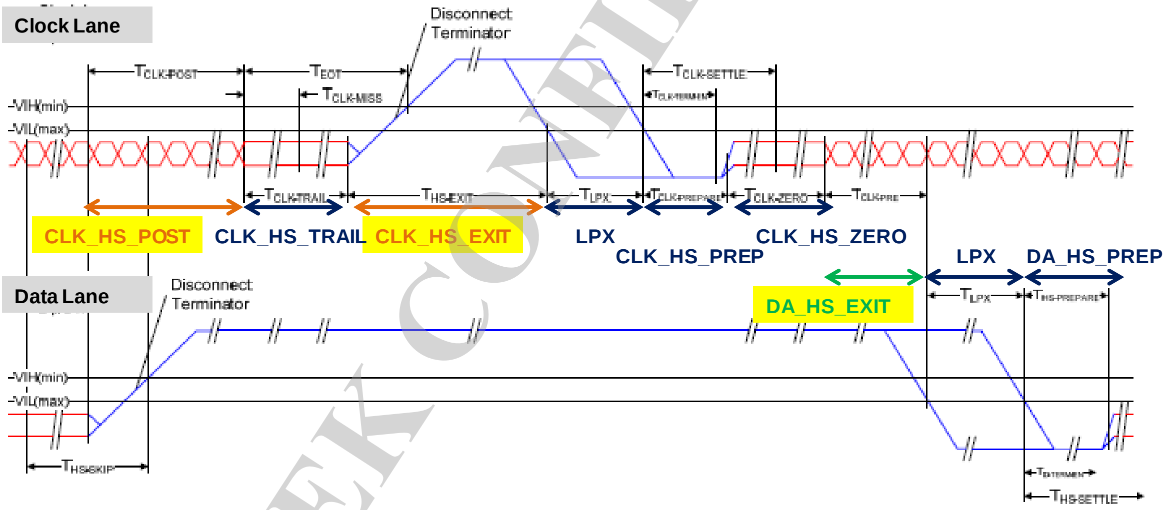

Figure 6-61. Registers for clock lane timing parameters

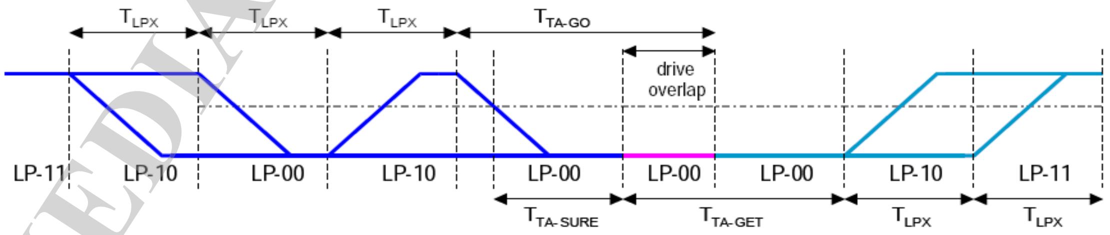

Figure 6-62. Register for BTA timing parameters

6.21.5 Command Mode

DSI supports command mode transmission through writing commands to a dedicated command queue. By configuring commands and triggering, the transmission can be executed sequentially.

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6.21.5.1 Command Queue

DSI has a dedicated command queue that are 32-bit wide and up to 128-entry deep, as shown in Figure 6-63. To simplify the settings for transmitting a packet in the command mode, the command queue is designed to categorize all possible transmission types and commands into four primary instructions and unifies all DSI specification commands into one or several 32-bit wide instructions. Figure 6-63 also illustrates a 32-bit instruction structure with the instruction format of CONFG byte.

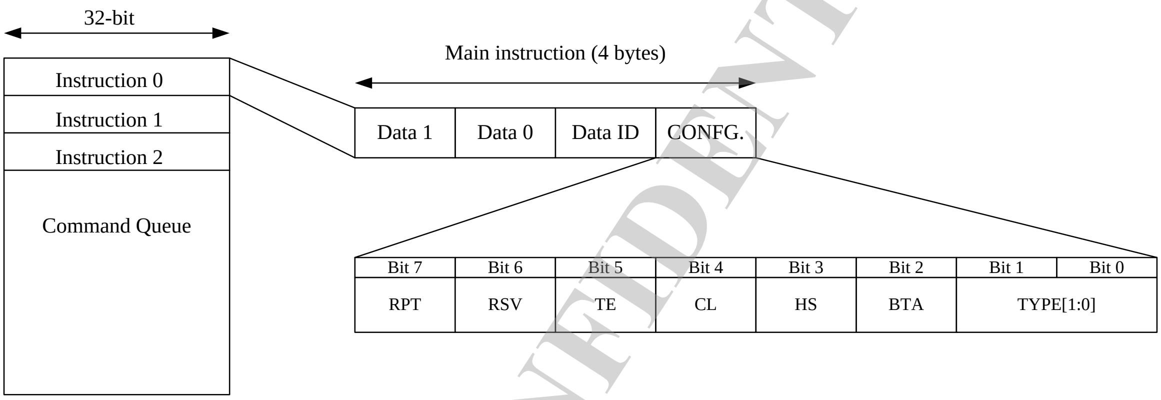

Figure 6-63. DSI command queue instruction format

Table 6-15 shows the descriptions of the CONFG byte to a instruction. For convenience's sake, virtual channel 0 is used for all packets in the following examples. Software programmers should take charge of the real virtual channel numbers to the slave devices.

Table 6-15. Config. field description of main instruction

	Value	Function	Description
Type[1:0]	00	-	Used for DSI short packet read/write command
	01	-	Used for DSI frame buffer write command (long packet)
	10	-	Used for DSI generic long packet write command
	11	-	Used for DSI frame buffer read command (short packet)
BTA	0	Off	Turns around the DSI link after the DSI command is transmitted
	1	On	
HS	0	Off	Enables HS Tx transmission for this packet; otherwise transmit packet via LP Tx
	1	On	
CL	0	8-bit	Selects command length for frame buffer read/write instruction. Only effective for type 1 and type 3 instructions.
	1	16-bt	
TE	0	Off	Enables TE request. Will only turn around the DSI link without any packet transmission
	1	On	
Resv	-	-	Reserved for further use
Resv	-	-	Reserved for further use

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6.21.5.2 Type-0 Instruction

Type-0 instruction is used to transmit short packets. Figure 6-64 lists the formats of type-0 instruction where (Data ID + Data 0 + Data 1) is constructed by a DSI short packet command (without ECC).

Byte 3	Byte 2	Byte 1	Byte 0
Data 1	Data 0	Data ID	CONFG.

Figure 6-64. Type-0 instruction format

Suppose we are to send "Turn On Peripheral" and "Color Mode On" commands which are transmitted via LP Tx and HS Tx respectively and request slave response after the second command finished, the descriptions can be translated into two 32-bit instructions and achieved by the steps illustrated in Table 6-16.

Table 6-16. Type-0 Tx example

Step	Description	R/W	Register [bit]	Value
1	Fill command queue entry-0	W	DSI_CMDQ_0	0x0000120C
2	Fill command queue entry-1	W	DSI_CMDQ_1	0x00003200
3	Set command count	W	DSI_CMDQ_CON	0x2
4	Start command	W	DSI_START [0]	0x1
5	Issue interrupt and receive slave response	R	DSI_INTSTA [0]	0x1
6	Clear interrupt status	W	DSI_INTSTA [0]	0x1
7	Read trigger status (Acknowledge)	R	DSI_RX_TRIG_STA [3:0]	0x4
8	Reponse read ack to module and go to next commends in queue	W	DSI_RX_RACK [0]	0x1
9	Issue interrupt and command done	R	DSI_INTSTA [1]	0x1
10	Clear interrupt status	W	DSI_INTSTA [1]	0x1

6.21.5.2.1 Type-1 Instruction

Type-1 command is used to write data into the frame buffer. As shown in Figure 6-65, there are 4 bytes constructing this type of instruction where mem_start_0 and mem_start_1 can be generic commands defined by slave vendors or DCS commands. mem_start_1 is optional, i.e. the memory start/continue command can be single-byte as DCS defines. To indicate whether the DSI controller sends mem_start_1 or not depends on the CL bit of the CONFG. byte. Since the length of frame butter to be updated is not a constant, this type of instruction may send several long packets to the slave. The payload data and length of each packet (excluding mem_start_0 and mem_start_1) is prepared by the RDMA controller which couples the output of image data path or layer overlay result to the DSI controller. For the first packet, mem_start_0 and mem_start_1 (if CL = 1) are used as the parameters to inform the slave that the host is starting to write the frame buffer. For the remaining packets, the register value MEM_CONTI[15:0] will be used as the parameters to inform the slave side to write these data following the last pixel of the previous packet. For more flexibility, mem_start_0,

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mem_start_1, MEM_CONTI[15:0] and CL are all programmable. However, it consumes only one entry of command queue.

The user needs to set up two registers to define the packet length and packet count for a frame-based type-1 transmission. Frame width in bytes should be set to DSI_PSCON, and frame height in lines should be set to DSI_VACT_NL, respectively. These two registers are used in both video and command mode frame data transmission.

Byte 3	Byte 2	Byte 1	Byte 0
Mem start 1 (optional)	Mem start 0	Data ID	CONFG.

Figure 6-65. Type-1 instruction format

Follow the example in Table 6-17 to write the frame buffer via DCS command in the HS Tx mode.

Table 6-17. Type-1 Tx example

Step	Description	R/W	Register [bit]	Value
1	Fill command queue entry-0	W	DSI_CMDQ_0	0x002C3909
2	Set command count	W	DSI_CMDQ_CON	0x1
3	Set memory continue command	W	DSI_MEM_CONTI [15:0]	0x3C
4	Start command	W	DSI_START [0]	0x1
5	Issue interrupt and command done	R	DSI_INTSTA [1]	0x1
6	Clear interrupt status	W	DSI_INTSTA [1]	0x1

6.21.5.2.2 Type-2 Instruction

Type-2 instruction is used to send a long packet. As shown in Figure 6-66, this type of main instruction requires several sub-instructions which do not have CONFIG. To send a type-2 command, the user needs to write a CONFIG with TYPE = 2 and packet header information (Data ID + 2 byte word count) to enrty 0, and a series of data bytes in size of word count to the following entries, excluding ECC and checksum. The bytes in following entries will be treated as long packet data instead of the next instruction until the word count size is reached. The command queue count should be set as the number of multiple entries used.

The type-2 command is sent in LPTX mode due to memory latency in reading sub-instruction data. Besides, type-2 command should be sent individually without the next instruction followed. For the 32-entry command queue, the maximum word count for long packet is 124 bytes.

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Byte 3	Byte 2	Byte 1	Byte 0
WC 1	WC 0	Data ID	CONFG.
Data 3	Data 2	Data 1	Data 0
		Data WC-1	Data WC-2

Figure 6-66. Type-2 instruction format

See Table 6-18 below for the example of sending 3 parameters (0x33, 0x22, 0x11) by a generic long packet command with 3-byte word count.

Table 6-18. Type-2 Tx example

Step	Description	R/W	Register [bit]	Value
1	Fill command queue entry-0 (data ID and word count)	W	DSI_CMDQ_0	0x00032902
2	Fill command queue entry-1 (parameters)	W	DSI_CMDQ_1	0x00112233
3	Set command count	W	DSI_CMDQ_CON	0x2
4	Start command	W	DSI_START [0]	0x1
5	Issue interrupt and command done	R	DSI_INTSTA [1]	0x1
6	Clear interrupt status	W	DSI_INTSTA [1]	0x1

Note that the RPT bit of CONFIG. is designed for this type of instruction. It is useful for the NULL packet or blanking packet. For example, if a null packet is to be sent, only the main instruction (entry-0 of command queue) will be needed, the following payload data will be sent as “0”.

6.21.5.2.3 Type-3 Instruction

Type-3 instruction is used for reading frame buffer. As shown in Figure 6-67, the format is the same as that of type-1. When this instruction is executed, the host will first send a short packet with memory start parameter given in byte 2 and byte 3 and automatically issue the next packet by memory continue parameters programmed in MEM_CONTI[15:0]. The number of total packets required to be sent depends on the FRM_BC and “maximum return packet size”. For example, if we are to read 1,024 bytes from the frame buffer in the slave, and the “maximum return packet size” is set to “4”, after the first short packet described in main instruction is sent, there will be another 255 short packets with memory continue parameters to be sent successively.

Byte 3	Byte 2	Byte 1	Byte 0
Men start 1 (optional)	Mem start 0	Data ID	CONFG.

Figure 6-67. Type-3 instruction format

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See Table 6-19 for the example of using type-3 instruction to perform the frame buffer read.

Table 6-19. Type-3 Tx example

Step	Description	R/W	Register [bit]	Value
1	Fill command queue entry-0	W	DSI_CMDQ_0	0x002E0603
2	Set command count	W	DSI_CMDQ_CON	0x1
3	Set memory read continue command	W	DSI_MEM_CONTI[15:0]	0x3E
4	Start command	W	DSI_START [0]	0x1
5	Issue interrupt and receive slave response	R	DSI_INTSTA [0]	0x1
6	Read receive data bytes	R	DSI_RX_DATA03	-
7	Clear interrupt status	W	DSI_INTSTA [0]	0x1
8	Reponse read ack to module and go to next commends in queue	W	DSI_RX_RACK [0]	0x1
9	Issue interrupt and command done	R	DSI_INTSTA [1]	0x1
10	Clear interrupt status	W	DSI_INTSTA [1]	0x1

6.21.5.2.4 Command Mode Status Debug Register

Sometimes an improper configuration settings to DSI, DISP paths and MUTEX may cause hanged issues on DSI because command mode control needs to wait for memory data from DMA in previous stages. As a result, a debugging register DSI_STATE_DBG6 is designed for users to observe internal states of DSI controller in order to reduce debugging efforts. Table 6-20 shows the status mapping to the register bit [14:0]. The user can check the on-hot bit to find incorrect settings.

Table 6-20. Command mode status in debugging register

Bit	Value	Description
0	0x0001	Idle (wait command)
1	0x0002	Reads command queue for packet header
2	0x0004	Sends type-0 command
3	0x0008	Waits for data from the previous module to send type-1 command
4	0x0010	Sends type-1 command
5	0x0020	Sends type-2 command
6	0x0040	Reads command queue for paket data
7	0x0080	Sends type-3 command
8	0x0100	Sends BTA
9	0x0200	Waits for RX-read data
10	0x0400	Waits for software RACK for RX-read data
11	0x0800	Waits for peripheral TE
12	0x1000	Gets TE signaling
13	0x2000	Waits for software RACK for peripheral TE
14	0x4000	Waits for external TE

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6.21.5.3 Video Mode

DSI supports video mode traffic sequences, including sync pulse mode, sync event mode and burst mode. To facilitate the translation of the parameters of packets, see the timing diagrams below for the corresponding register settings.

6.21.5.3.1 Sync-Pulse Mode

A non-burst sync-pulse mode enables the peripheral to accurately reconstruct the original video timing, including sync pulse widths. A timing diagram for sync-pulse mode is shown in Figure 6-68, which also shows registers mappings to lines of VSA/VBP/VACT/VFP periods

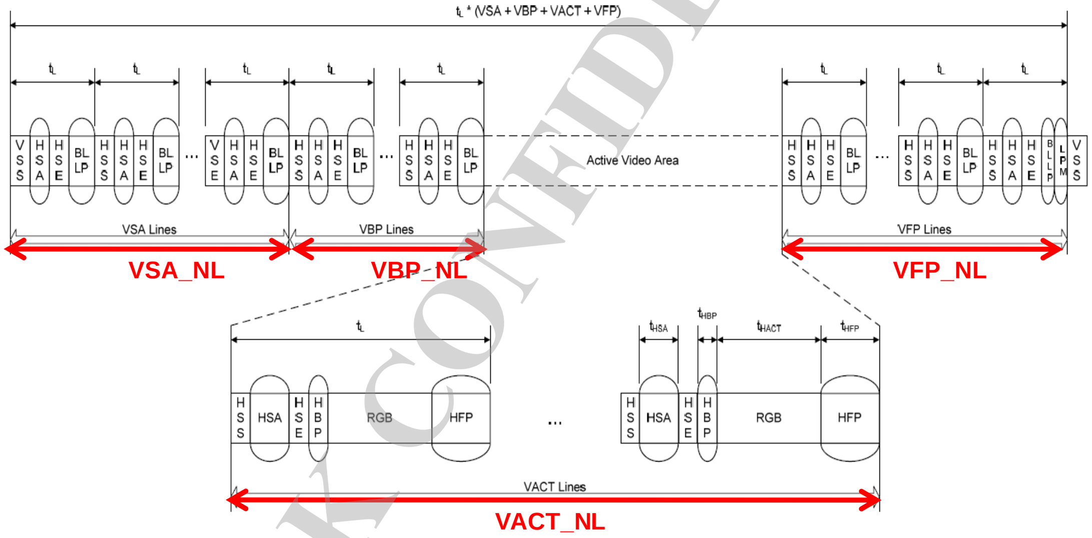

Figure 6-68. Non-burst transmission: sync-pulse mode

A detailed timing diagram for one line period is shown in Figure 6-69. In this diagram, the user must base on real timing parameters of HPW/HBP/HFP and pixel format to figure out the correct value to registers. In addition, a slight adjustment on HFP_WC should also be performed because it needs to leave some space time for HS preparation time due to non-continuous data lane transmission. The formulas for these registers are shown in Figure 6-70.

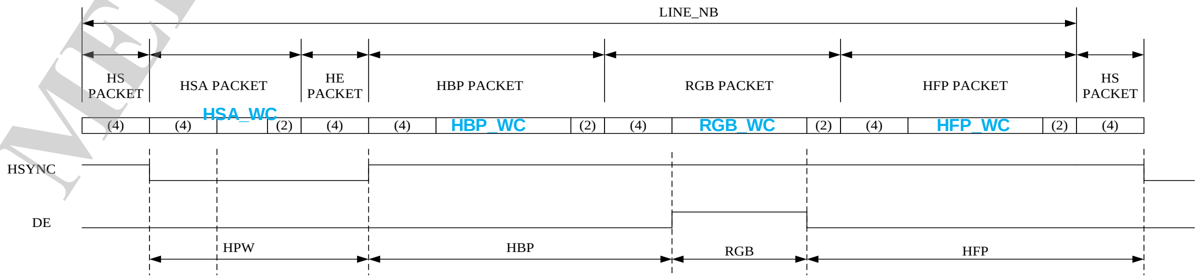

Figure 6-69. Sync-pulse mode line period

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- HSA_WC = HPW * BPP - 10
- HBP_WC = HBP * BPP - 10
- RGB_WC = active_pixel * BPP
- HFP_WC = HFP * BPP - 12 - data_init_cycle * lane_num
- data_init_cycle = T_hs-exit + T_lpx + T_hs-prep + T_hs-zero

Figure 6-70. Sync-pulse mode word-count parameters

6.21.5.3.2 Sync-Event Mode

A non-burst sync-event mode is similar to the pulse-sync mode, but accurate reconstruction of sync pulse widths is not required. Therefore, a single sync event is substituted. The timing diagram is shown in Figure 6-71.

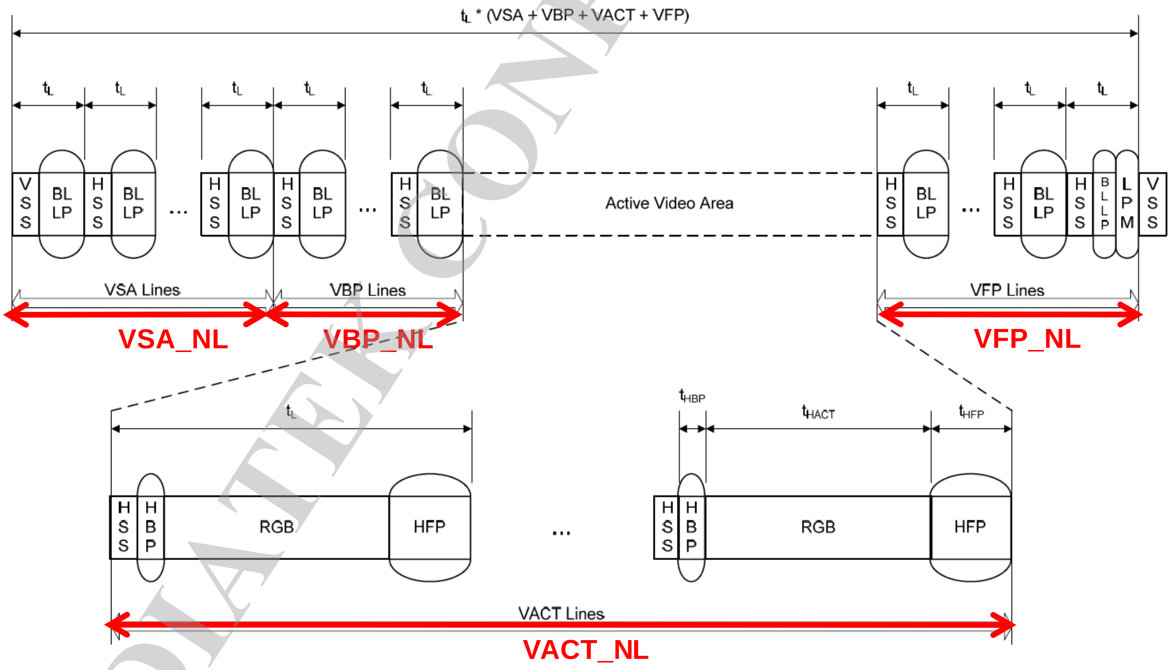

Figure 6-71. Non-burst transmission: Sync-event mode

A detailed timing diagram for one line period is shown in Figure 6-72, and the register settings of word count is listed in Figure 6-73.

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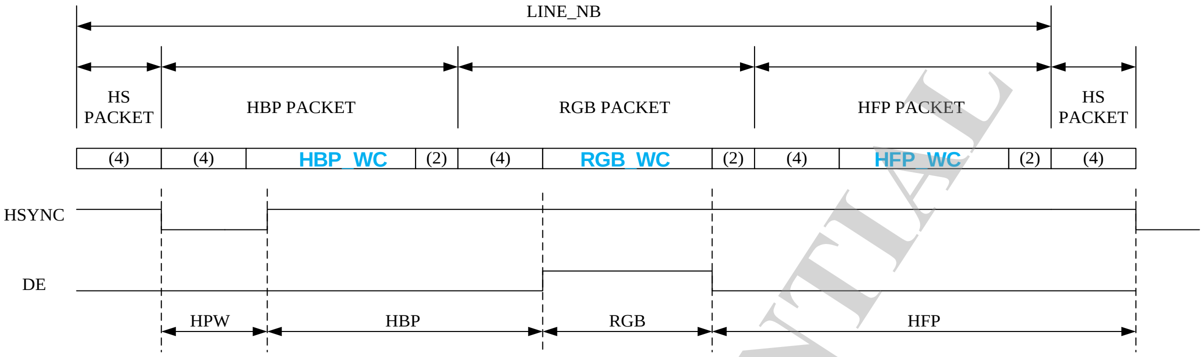

Figure 6-72. Sync-event mode line period

- HSA_WC = don't care
- HBP_WC = (HPW + HPW) * BPP - 10
- RGB_WC = active_pixel * BPP
- BLLP_WC = only set in Burst Mode
- HFP_WC = HFP * BPP - 12 - data_init_cycle * lane_num
- data_init_cycle = T_hs-exit + T_lpx + T_hs-prep + T_hs-zero

Figure 6-73. Sync-event mode word-count parameters

6.21.5.3.3 Burst Mode

The burst mode allows RGB pixel packets to be time-compressed, leaving more time in a scan line for LP mode to save power or for multiplexing other transmissions onto DSI link. The timing diagram is shown in Figure 6-71Figure 6-71.

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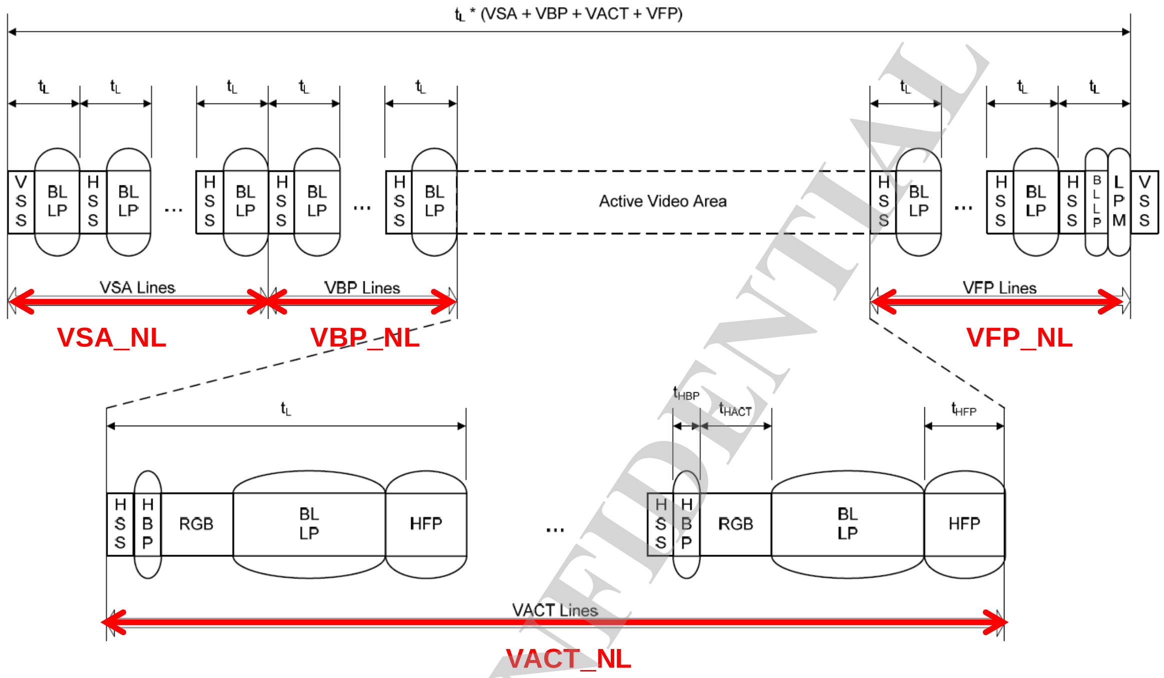

Figure 6-74. Burst mode transmission

Detailed timing diagram for one line period of burst mode is almost the same as sync-event mode shown in Figure 6-72 and Figure 6-73 except that the BLLC_WC register should be set.

6.21.5.4 Clock Lane Non-continuous Low-power Control

Clock lane non-continuous low-power control is supported in the version of DSI, which allows clock lane to return to idle state after a command transmission or during blanking packet period in the video mode. Figure 6-75 shows the blanking packet period distributed in a video mode transmission, where the host transfers blanking packets or back to idle state.

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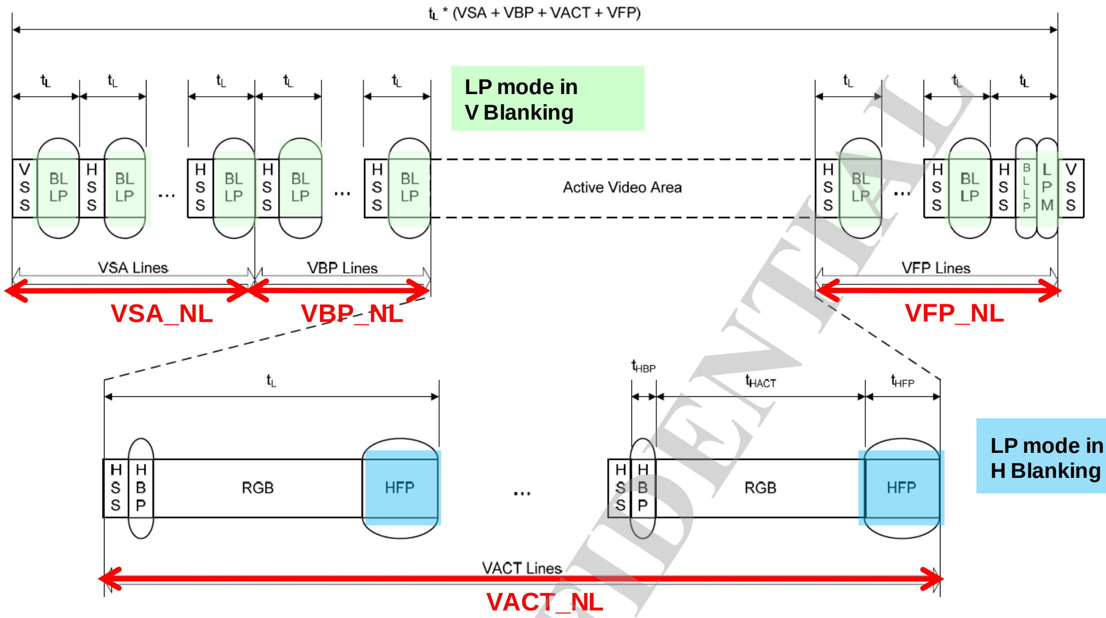

Figure 6-75. Blanking packet in video mode transmission

Figure 6-76 is the timing diagram of vertical blanking low-power control. This mechanism is through the register of DSI_HSTX_CKLP_WC, whose value is listed below. In most cases, vertical blanking power-saving is suggested. If the user would like to have more precise low-power control, the value set for VACT-line horizontal blanking low-power is acceptable. However, the timing should be calculated carefully from affecting the line period since the clock/data lanes need to take time back from idle state to high-speed mode before the next HS transmission.

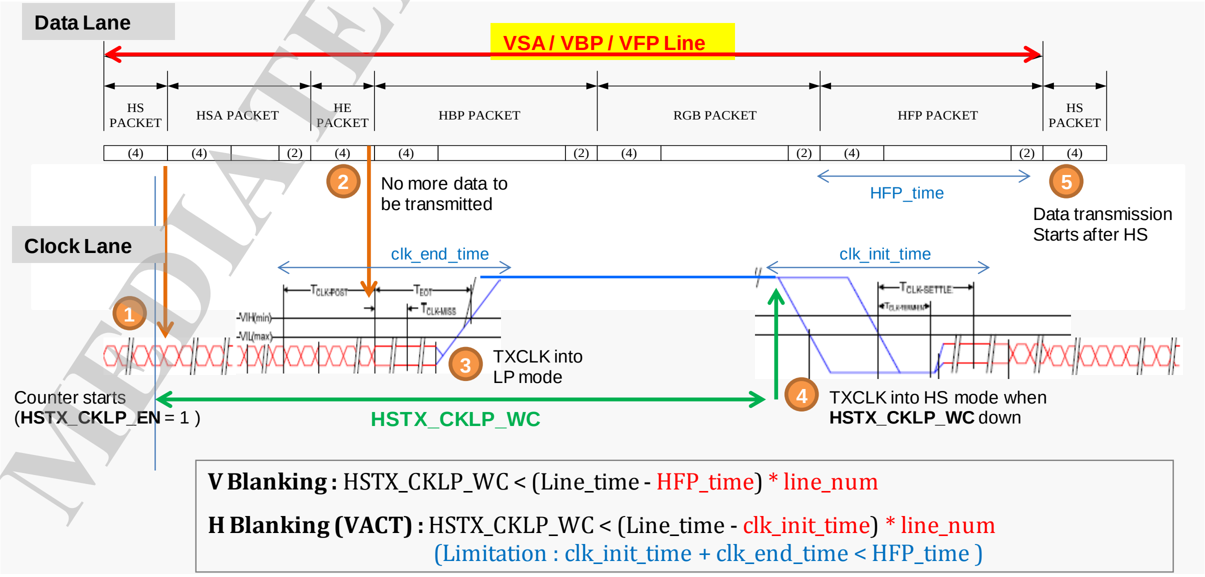

Figure 6-76. Low-power counter settings for video mode low-power control

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6.21.5.4.1 Auto-calculation for Non-continuous Clock Word Counter

Because the calculation of word counter to control non-continuous clock recover is complicated, to simplify this flow, an auto-calculation register is provided in this version of design. Users can set HSTX_CKLP_WC_AUTO in register DSI_HSTX_CKLP_WC to 1 to allow module to automatically figure out the required values instead of manually calculation. In this mode, the value of HSTX_CKLP_WC is ignored.

6.21.5.5 Peripheral TE Detection

6.21.5.5.1 TE Signaling

DSI is capable of receiving peripheral TE (Tearing Effect) signals via BTA process. Before starting to receive TE signals from the peripheral, make sure a DCS command of "set_tear_on" is sent and register configuration of TE is enabled in the peripheral to avoid TE hang issue. Table 6-21 is an example showing how to trigger TE commands by command queue.

Table 6-21. Example of TE signaling detection

Step	Description	R/W	Register [bit]	Value
1	Fill command queue : DCS "set_tear_on"	W	DSI_CMDQ_0	0x00351500
2	Fill command queue : get TE	W	DSI_CMDQ_1	0x00000020
3	Fill command queue : type-1 command	W	DSI_CMDQ_2	0x002C3909
4	Set command count	W	DSI_CMDQ_CON	0x3
5	Set memory write continue command	W	DSI_MEM_CONTI[15:0]	0x3C
6	Start command	W	DSI_START [0]	0x1
7	Issue interrupt and receive TE	R	DSI_INTSTA [2]	0x1
8	Read trigger status (TE)	R	DSI_RX_TRIG_STA [3:0]	0x2
9	Clear interrupt status	W	DSI_INTSTA [2]	0x1
10	Reponse read ack to module and go to next commends in queue	W	DSI_RX_RACK [0]	0x1
11	Issue interrupt and command done	R	DSI_INTSTA [1]	0x1
12	Clear interrupt status	W	DSI_INTSTA [1]	0x1

6.21.5.5.2 External TE Pin

In certain case we may use external TE pin instead of TE signals for some reasons. DSI supports such mechanism to issue external TE interrupt signals. Refer to the sequences shown in Table 6-22 for detailed control information.

Table 6-22. Example of external TE pin detection

Step	Description	R/W	Register [bit]	Value
1	Enable external TE interrupt	W	DSI_INTEN [4]	0x1
2	Enable external TE	W	DSI_TXRX_CON [10]	0x1

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Step	Description	R/W	Register [bit]	Value
3	Select external TE polarity (active-high)	W	DSI_TXRX_CON [9]	0x0
4	Issue interrupt and receive external TE	R	DSI_INTSTA [4]	0x1
5	Clear interrupt status	W	DSI_INTSTA [4]	0x1

6.21.5.6 Video Mode Extra Packet Transmission

DSI supports sending out an extra short/long packet during video mode transmission. This operation must use a set of special registers instead of the original command queue. The single extra packet is sent once and immediately when the user triggers the VM_CMD_START bit of register DSI_START. Refer to the registers with prefix of "DSI_VM_CMD" for more detailed descriptions.

6.21.5.6.1 Short Packet

To transmit an extra short packet in the video mode, follow the example illustrated in Table 6-23.

Table 6-23. Example of short packet transmission in video mode

Step	Description	R/W	Register [bit]	Value
1	Enable vm-cmd function	W	DSI_VM_CMD_CON [0]	0x1
2	Select short packet to be sent	W	DSI_VM_CMD_CON [1]	0x0
3	Enable sending period (VBP, VFP)	W	DSI_VM_CMD_CON [5:3]	0x6
4	Fill short packet ID and bytes 0~1	W	DSI_VM_CMD_CON [31:8]	0x001535
5	Enable vm-cmd done interrupt	W	DSI_INTEN [5]	0x1
6	Start vm-cmd transmission	W	DSI_START [16]	0x1
7	Issue interrupt and vm-cmd transmission done	R	DSI_INTSTA [5]	0x1
8	Clear interrupt status	W	DSI_INTSTA [5]	0x1

6.21.5.6.2 Long Packet

To transmit an extra long packet in the video mode, follow the example illustrated in Table 6-24.

Table 6-24. Example of long packet transmission in video mode

Step	Description	R/W	Register [bit]	Value
1	Enable vm-cmd function	W	DSI_VM_CMD_CON [0]	0x1
2	Select long packet to be sent	W	DSI_VM_CMD_CON [1]	0x1
3	Enable sending period (VSA, VBP, VFP)	W	DSI_VM_CMD_CON [5:3]	0x7
4	Fill long packet ID and word count	W	DSI_VM_CMD_CON [31:8]	0x000739
5	Fill long packet data byte 0~3	W	DSI_VM_CMD_DATA0	0x332211FF
6	Fill long packet data byte 4~6	W	DSI_VM_CMD_DATA1	0x00665544
7	Enable vm-cmd done interrupt	W	DSI_INTEN [5]	0x1
8	Start vm-cmd transmission	W	DSI_START [16]	0x1
9	Issue interrupt and vm-cmd transmission	R	DSI_INTSTA [5]	0x1

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Step	Description	R/W	Register [bit]	Value
	done			
10	Clear interrupt status	W	DSI_INTSTA [5]	0x1

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6.22 MIPI TX Configuration Module

6.22.1 Introduction

The MIPI TX configuration module, as well as MIPI_TX_Config described in the following sections, is used to control MIPI TX related registers for MIPI DPHY macro. This analog macro includes design of SDM PLL, bandgap, LDO core, lane control, GPI pads, output enable, etc. It provides MIPI DSI high-speed clock up to 1.5Gbps, as well as 768MHz and provides primary clocks to DSI module.

6.22.2 Features

The following functions of MIPI DPHY can be controlled by this module.

- Bandgap control
- LDO core power and configuration
- SDM PLL configuration
- SSC control
- Analog function related settings and status
- Output pads control and electronic features
- GPI pads control
- Software-control mode for each lanes
- Lane swap for clock and data lanes

6.22.3 Register Definition

Module name: mipi_tx_config Base address: (+14017000h)

Address	Name	Width	Register Function
14017000	DSI_CON	32	DSI Configuration Register
14017004	DSI_CLOCK_LANE	32	DSI Clock Lane Configuration Register
14017008	DSI_DATA_LANE_0	32	DSI Data Lane 0 Configuration Register
1401700C	DSI_DATA_LANE_1	32	DSI Data Lane 1 Configuration Register
14017010	DSI_DATA_LANE_2	32	DSI Data Lane 2 Configuration Register
14017014	DSI_DATA_LANE_3	32	DSI Data Lane 3 Configuration Register
14017040	DSI_TOP_CON	32	DSI Top Configuration Register
14017044	DSI_BG_CON	32	DSI BG Configuration Register
14017050	DSI_PLL_CON0	32	DSI PLL Configuration 0 Register
14017054	DSI_PLL_CON1	32	DSI PLL Configuration 1 Register
14017058	DSI_PLL_CON2	32	DSI PLL Configuration 2 Register
1401705C	DSI_PLL_CON3	32	DSI PLL Configuration 3 Register
14017060	DSI_PLL_CHG	32	DSI PLL Charge Register
14017064	DSI_PLL_TOP	32	DSI PLL TOP Configuration Register
14017068	DSI_PLL_PWR	32	DSI PLL Power Control Register

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Address	Name	Width	Register Function
14017070	DSI_RGS	32	DSI RGS Register
14017074	DSI_GPI_EN	32	DSI GPI Enable Register
14017078	DSI_GPI_PULL	32	DSI GPI Pull Register
1401707C	DSI_PHY_SEL	32	DSI MIPI TX PHY Lane Swap Selection
14017080	DSI_SW_CTRL_EN	32	DSI Software Control Enable Register
14017084	DSI_SW_CTRL_CON0	32	DSI Software Control Configuration Register 0
14017088	DSI_SW_CTRL_CON1	32	DSI Software Control Configuration Register 1
1401708C	DSI_SW_CTRL_CON2	32	DSI Software Control Configuration Register 0
14017090	DSI_DBG_CON	32	DSI Debug Control Register
14017094	DSI_DBG_OUT	32	DSI Debug Out Register
14017098	DSI_APB_ASYNC_STA	32	DSI APB Async Status Register

14017000 DSI_CON DSI Configuration Register 00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					RG_DSI_LPTX_CLMP_EN	RG_DSI_DSICLK_FREQ_SEL	RG_DSI_PHYCLK_SEL			RG_DSI_LD_IDX_SEL			RG_DSI_BCLK_SEL		RG_DSI_CKG_LDOOUT_EN	RG_DSI_LDOCORE_EN
Type					RW	RW	RW			RW			RW		RW	RW
Reset					0	1	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11		RG_DSI_LPTX_CLMP_EN	**DSI0_LPTX_CLMP_EN** 1'b0: Disable DC clamp 1'b1: Enable DC clamp
10		RG_DSI_DSICLK_FREQ_SEL	**Selects DSI DSICLK frequency** 1'b0: 2X of PHYCLK 1'b1: 1X of PHYCLK
9:8		RG_DSI_PHYCLK_SEL	**Selects DSI0 PHYCLK phase** 2'b00: Align with BCLK 2'b01: Align with BCLKQ 2'b10: Align with BCLKB 2'b11: Align with BCLKQB
6:4		RG_DSI_LD_IDX_SEL	**Selects DSI0 LD_IDX phase** 3'b000: 1/4T delay from CKQ 3'b001: 3/8T delay from CKQ etc.
3:2		RG_DSI_BCLK_SEL	**Selects DSI0 byteclk phase** 2'b00: Align with CK 2'b01: Align with CKQ

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Bit(s)	Mnemonic	Name	Description
			2'b10: Align with CKB 2'b11: Align with CKQB
1		RG_DSI_CKG_LDOOUT_EN	**Enables DSI0 CKG LDO output** 1'b0: Disable 1'b1: Enable
0		RG_DSI_LDOCORE_EN	**Enables DSI0 LDO core** 1'b0: Disable 1'b1: Enable

14017004 **DSI_CLOCK_LANE** **DSI Clock Lane Configuration Register** **00000802**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RG_DSI_LNTC_RT_CODE**					**RG_DSI_LNTC_LPCD_IMINUS**	**RG_DSI_LNTC_LPCD_IPLUS**	**RG_DSI_LNTC_LPTX_IMINUS**	**RG_DSI_LNTC_LPTX_IPLUS2**	**RG_DSI_LNTC_LPTX_IPLUS1**	**RG_DSI_LNTC_CKLANE_EN**	**RG_DSI_LNTC_LDOOUT_EN**
Type					RW					RW	RW	RW	RW	RW	RW	RW
Reset					1	0	0	0		0	0	0	0	0	1	0

Bit(s)	Mnemonic	Name	Description
11:8		RG_DSI_LNTC_RT_CODE	**DSI CK lane HS impedance control code** 4'b0000: Maximum impedance 4'b1111: Minimum impedance
6		RG_DSI_LNTC_LPCD_IMINUS	**Adjusts DSI CK lane LP driver current** 1'b0: Normal 1'b1: -10%
5		RG_DSI_LNTC_LPCD_IPLUS	**Adjusts DSI CK lane LP driver N current** 1'b0: Normal 1'b1: +10%
4		RG_DSI_LNTC_LPTX_IMINUS	**Adjusts DSI CK lane LP driver current** 1'b0: Normal 1'b1: -10%
3		RG_DSI_LNTC_LPTX_IPLUS2	**Adjusts DSI CK lane LP driver N current** 1'b0: Normal 1'b1: +10%
2		RG_DSI_LNTC_LPTX_IPLUS1	**Adjusts DSI CK lane LP driver P current** 1'b00: Normal 1'b01: +10%
1		RG_DSI_LNTC_CKLANE_EN	**Enables DSI CK lane as clock lane** 1'b0: Disable 1'b1: Enable
0		RG_DSI_LNTC_LDOOUT_EN	**Enables DSI CK lane LDO output** 1'b0: Disable 1'b1: Enable

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14017008 **DSI_DATA_LANE_0** **DSI Data Lane 0 Configuration Register** **00000800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_DSI_LNT0_RT_CODE					RG_DSI_LNT0_LPCD_IMINUS	RG_DSI_LNT0_LPCD_IPLUS	RG_DSI_LNT0_LPTX_IMINUS	RG_DSI_LNT0_LPTX_IPLUS2	RG_DSI_LNT0_LPTX_IPLUS1	RG_DSI_LNT0_CKLANE_EN	RG_DSI_LNT0_LDOOUT_EN
Type					RW					RW	RW	RW	RW	RW	RW	RW
Reset					1	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:8		RG_DSI_LNT0_RT_CODE	**DSI Lane 0 HS impedance control code** 4'b0000: Maximum impedance 4'b1111: Minimum impedance
6		RG_DSI_LNT0_LPCD_IMINUS	**Adjusts DSI Lane 0 LP driver current** 1'b0: Normal 1'b1: -10%
5		RG_DSI_LNT0_LPCD_IPLUS	**Adjusts DSI Lane 0 LP driver N current** 1'b0: Normal 1'b1: +10%
4		RG_DSI_LNT0_LPTX_IMINUS	**Adjusts DSI Lane 0 LP driver current** 1'b0: Normal 1'b1: -10%
3		RG_DSI_LNT0_LPTX_IPLUS2	**Adjusts DSI Lane 0 LP driver N current** 1'b0: Normal 1'b1: +10%
2		RG_DSI_LNT0_LPTX_IPLUS1	**Adjusts DSI Lane 0 LP driver P current** 1'b00: Normal 1'b01: +10%
1		RG_DSI_LNT0_CKLANE_EN	**Enables DSI Lane 0 as clock lane** 1'b0: Disable 1'b1: Enable
0		RG_DSI_LNT0_LDOOUT_EN	**Enables DSI Lane 0 LDO output** 1'b0: Disable 1'b1: Enable

1401700C **DSI_DATA_LANE_1** **DSI Data Lane 1 Configuration Register** **00000800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_DSI_LNT1_RT_CODE					RG_DSI_LNT	RG_DSI_LNT	RG_DSI_LNT	RG_DSI_LNT	RG_DSI_LNT1	RG_DSI_LNT	RG_DSI_LNT1

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										1_LPCD_IMINUS	1_LPCD_IPLUS	1_LPTX_IMINUS	1_LPTX_IPLUS2	_LPTX_IPLUS1	1_CKLANE_EN	_LDOOUT_EN
Type					RW					RW	RW	RW	RW	RW	RW	RW
Reset					1	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:8		RG_DSI_LNT1_RT_CODE	**DSI Lane 1 HS impedance control code** 4'b0000: Maximum impedance 4'b1111: Minimum impedance
6		RG_DSI_LNT1_LPCD_IMINUS	**Adjusts DSI Lane 1 LP driver current** 1'b0: Normal 1'b1: -10%
5		RG_DSI_LNT1_LPCD_IPLUS	**Adjusts DSI Lane 1 LP driver N current** 1'b0: Normal 1'b1: +10%
4		RG_DSI_LNT1_LPTX_IMINUS	**Adjusts DSI Lane 1 LP driver current** 1'b0: Normal 1'b1: -10%
3		RG_DSI_LNT1_LPTX_IPLUS2	**Adjusts DSI Lane 1 LP driver N current** 1'b0: Normal 1'b1: +10%
2		RG_DSI_LNT1_LPTX_IPLUS1	**Adjusts DSI Lane 1 LP driver P current** 1'b00: Normal 1'b01: +10%
1		RG_DSI_LNT1_CKLANE_EN	**Enables DSI Lane 1 as clock lane** 1'b0: Disable 1'b1: Enable
0		RG_DSI_LNT1_LDOOUT_EN	**Enables DSI Lane 1 LDO output** 1'b0: Disable 1'b1: Enable

14017010 **<u>DSI_DATA_LANE_2</u>** **DSI Data Lane 2 Configuration Register** **00000800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					RG_DSI_LNT2_RT_CODE					RG_DSI_LNT2_LPCD_IMINUS	RG_DSI_LNT2_LPCD_IPLUS	RG_DSI_LNT2_LPTX_IMINUS	RG_DSI_LNT2_LPTX_IPLUS2	RG_DSI_LNT2_LPTX_IPLUS1	RG_DSI_LNT2_CKLANE_EN	RG_DSI_LNT2_LDOOUT_EN
Type					RW					RW	RW	RW	RW	RW	RW	RW
Reset					1	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:8		RG_DSI_LNT2_RT_CODE	**DSI Lane 2 HS impedance control code** 4'b0000: Maximum impedance 4'b1111: Minimum impedance

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Bit(s)	Mnemonic	Name	Description
6		RG_DSI_LNT2_LPCD_IMINUS	**Adjusts DSI Lane 2 LP driver current** 1'b0: Normal 1'b1: -10%
5		RG_DSI_LNT2_LPCD_IPLUS	**Adjusts DSI Lane 2 LP driver N current** 1'b0: Normal 1'b1: +10%
4		RG_DSI_LNT2_LPTX_IMINUS	**Adjusts DSI Lane 2 LP driver current** 1'b0: Normal 1'b1: -10%
3		RG_DSI_LNT2_LPTX_IPLUS2	**Adjusts DSI Lane 2 LP driver N current** 1'b0: Normal 1'b1: +10%
2		RG_DSI_LNT2_LPTX_IPLUS1	**Adjusts DSI Lane 2 LP driver P current** 1'b00: Normal 1'b01: +10%
1		RG_DSI_LNT2_CKLANE_EN	**Enables DSI Lane 2 as clock lane** 1'b0: Disable 1'b1: Enable
0		RG_DSI_LNT2_LDOOUT_EN	**Enables DSI Lane 2 LDO output** 1'b0: Disable 1'b1: Enable

14017014 **DSI_DATA_LANE_3** **DSI Data Lane 3 Configuration Register** **00000800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_DSI_LNT3_RT_CODE					RG_DSI_LNT3_LPCD_IMINUS	RG_DSI_LNT3_LPCD_IPLUS	RG_DSI_LNT3_LPTX_IMINUS	RG_DSI_LNT3_LPTX_IPLUS2	RG_DSI_LNT3_LPTX_IPLUS1	RG_DSI_LNT3_CKLANE_EN	RG_DSI_LNT3_LDOOUT_EN
Type					RW					RW	RW	RW	RW	RW	RW	RW
Reset					1	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:8		RG_DSI_LNT3_RT_CODE	**DSI Lane 3 HS impedance control code** 4'b0000: Maximum impedance 4'b1111: Minimum impedance
6		RG_DSI_LNT3_LPCD_IMINUS	**Adjusts DSI Lane 3 LP driver current** 1'b0: Normal 1'b1: -10%
5		RG_DSI_LNT3_LPCD_IPLUS	**Adjusts DSI Lane 3 LP driver N current** 1'b0: Normal 1'b1: +10%
4		RG_DSI_LNT3_LPTX_IMINUS	**Adjusts DSI Lane 3 LP driver current** 1'b0: Normal 1'b1: -10%

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Bit(s)	Mnemonic	Name	Description
3		RG_DSI_LNT3_LPTX_IPLUS2	**Adjusts DSI Lane 3 LP driver N current** 1'b0: Normal 1'b1: +10%
2		RG_DSI_LNT3_LPTX_IPLUS1	**Adjusts DSI Lane 3 LP driver P current** 1'b00: Normal 1'b01: +10%
1		RG_DSI_LNT3_CKLANE_EN	**Enables DSI Lane 3 as clock lane** 1'b0: Disable 1'b1: Enable
0		RG_DSI_LNT3_LDOOUT_EN	**Enables DSI Lane 3 LDO output** 1'b0: Disable 1'b1: Enable

14017040 **DSI_TOP_CON** **DSI Top Configuration Register** **00000880**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_DSI_PRESERVE				RG_DSI_PAD_TIE_LOW_EN	RG_DSI_LNT_AIO_SEL			RG_DSI_LNT_IMP_CAL_CODE				RG_DSI_LNT_TESTMODE_EN	RG_DSI_LNT_IMP_CAL_EN	RG_DSI_LNT_HS_BIAS_EN	RG_DSI_LNT_INTR_EN
Type	RW				RW	RW			RW				RW	RW	RW	RW
Reset	0	0	0		1	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:13		RG_DSI_PRESERVE	**DSI preserved registers**
11		RG_DSI_PAD_TIE_LOW_EN	**Enables DSI 8 pads tie-low** 1'b0: Floating or depend on line driver 1'b1: Tie to AVSS18 ground
10:8		RG_DSI_LNT_AIO_SEL	**Selects DSI analog debugging mode output** 3'b000: Output VREF 0.2V 3'b001: Output VREF 0.32V 3'b010: Output VREF 0.4V 3'b011: Output VREF 0.72V 3'b100: Output VREF 0.86V 3'b101: Output VREF 1.2V 3'b110: Output VCCK09 3'b111: Output PLL_TST
7:4		RG_DSI_LNT_IMP_CAL_CODE	**DSI HS impedance calibration code** 4'b0000: Maximum impedance 4'b1111: Minimum impedance
3		RG_DSI_LNT_TESTMODE_EN	**Enables DSI analog debugging mode** 1'b0: Disable 1'b1: Enable
2		RG_DSI_LNT_IMP_CAL_EN	**Enables DSI HS impedance calibration** 1'b0: Disable

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Bit(s)	Mnemonic	Name	Description
			1'b1: Enable
1		RG_DSI_LNT_HS_BIAS_EN	**Enables DSI HS bias** 1'b0: Disable 1'b1: Enable
0		RG_DSI_LNT_INTR_EN	**Enables DSI HS bias internal R** 1'b0: Use external R 1'b1: Use internal R

14017044 DSI_BG_CON DSI BG Configuration Register 88492480

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_DSI_BG_R2_TRIM				RG_DSI_BG_R1_TRIM					RG_DSI_V02_SEL			RG_DSI_V032_SEL			RG_DSI_V04_SEL[2:2]
Type	RW				RW					RW			RW			RW
Reset	1	0	0	0	1	0	0	0		1	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_DSI_V04_SEL[1:0]		RG_DSI_V072_SEL			RG_DSI_V10_SEL			RG_DSI_V12_SEL			RG_DSI_BG_FAST_CHARGE	RG_DSI_BG_DIV		RG_DSI_BG_CKEN	RG_DSI_BG_CORE_EN
Type	RW		RW			RW			RW			RW	RW		RW	RW
Reset	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		RG_DSI_BG_R2_TRIM	**Trims DSI BGR R2** ORed with RG_CSI_BG_R2_TRIM[3:0] 4'b0000: Maximum resistance 4'b1000: Typical resistance 4'b1111: Minimum resistance
27:24		RG_DSI_BG_R1_TRIM	**Trims DSI BGR R1** ORed with RG_CSI_BG_R1_TRIM[3:0] 4'b0000: Maximum resistance 4'b1000: Typical resistance 4'b1111: Minimum resistance
22:20		RG_DSI_V02_SEL	**Selects 0.2V output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage
19:17		RG_DSI_V032_SEL	**Selects 0.32V output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage
16:14		RG_DSI_V04_SEL	**Selects 0.4V output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage
13:11		RG_DSI_V072_SEL	**Selects 0.72V output voltage** 3'b000: Minimum voltage

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Bit(s)	Mnemonic	Name	Description
			3'b100: Typical voltage 3'b111: Maximum voltage
10:8		RG_DSI_V10_SEL	**Selects AVDD10 output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage
7:5		RG_DSI_V12_SEL	**Selects 1.2V output voltage** 3'b0000: Minimum voltage 3'b0100: Typical voltage 3'b0111: Maximum voltage
4		RG_DSI_BG_FAST_CHARGE	**Enables BG bias low-pass filter fast charge** 1'b0: Disable; settling time 30us 1'b1: Enable; settling time 1us
3:2		RG_DSI_BG_DIV	**Controls BG chopper clock divisor** 2'b00: /2 2'b01: /4 2'b10: /8 2'b11: /16
1		RG_DSI_BG_CKEN	**Enables BG chopper clock** 1'b0: Disable 1'b1: Enable
0		RG_DSI_BG_CORE_EN	**Enables BG** OR with RG_CSI_BG_CORE_EN 1'b0: Power off 1'b1: Enable

14017050 **DSI_PLL_CON0** **DSI PLL Configuration 0 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**RG_DSI_MPPLL_VOD_EN**	**RG_DSI_MPPLL_MONREF_EN**	**RG_DSI_MPPLL_MONVC_EN**	**RG_DSI_MPPLL_POSDIV**			**RG_DSI_MPPLL_TXDIV1**		**RG_DSI_MPPLL_TXDIV0**		**RG_DSI_MPPLL_PREDIV**		**RG_DSI_MPPLL_PLL_EN**
Type				RW	RW	RW	RW			RW		RW		RW		RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12		RG_DSI_MPPLL_VOD_EN	**Enables MPPLL VOD** 1'b0: AVDD10 for PLL is not over-driven 10% to 1.15V for Vcore = 1.15V. 1'b1: AVDD10 for PLL is over-driven 10% to 1.15V for Vcore = 1.05V.
11		RG_DSI_MPPLL_MONREF_EN	**Enables monitor reference** 1'b0: Disable 1'b1: Enable
10		RG_DSI_MPPLL_MONVC_EN	**Enables monitor Vctrl** 1'b0: Disable

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Bit(s)	Mnemonic	Name	Description
			1'b1: Enable
9:7		RG_DSI_MPPLL_POSDIV	**PLL post divide ratio** 3'b000: /1 3'b001: /2 3'b010: /4 3'b011: /8 3'b100: /16 Others: Clock gating
6:5		RG_DSI_MPPLL_TXDIV1	**PLL0 VCO post-divider ratio** 2'b00: /1 2'b01: /2 2'b1X: /4
4:3		RG_DSI_MPPLL_TXDIV0	**PLL0 VCO post-divider ratio** 2'b00: /1 2'b01: /2 2'b1X: /4
2:1		RG_DSI_MPPLL_PREDIV	**Pre-divider ratio** 2'b00: /1 2'b01: /2 2'b1X: /4
0		RG_DSI_MPPLL_PLL_EN	**Enables PLL** 1'b0: Disable 1'b1: Enable

14017054 **DSI_PLL_CON1** **DSI PLL Configuration 1 Register** **00000003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_DSI_MPPLL_SDM_SSC_PRD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_DSI_MPPLL_SDM_SSC_EN	RG_DSI_MPPLL_SDM_SSC_PH_INIT	RG_DSI_MPPLL_SDM_FRA_EN
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Mnemonic	Name	Description
31:16		RG_DSI_MPPLL_SDM_SSC_PRD	**PLL SDM SSC period** 16'd0: Min. 16'd65536: Max. Counter triggered by reference 26MHz clock
2		RG_DSI_MPPLL_SDM_SSC_EN	**Enables PLL SDM SSC** 1'b0: Disable 1'b1: Enable
1		RG_DSI_MPPLL_SDM_SSC_PH_INIT	**Initializes PLL SDM SSC phase** 1'b0: Upward 1'b1: Downward

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Bit(s)	Mnemonic	Name	Description
0		RG_DSI_MPPLL_SDM_FRA_EN	**Enables PLL SDM fractional mode** 1'b0: Integer mode 1'b1: Fractional mode

14017058 **DSI_PLL_CON2** **DSI PLL Configuration 2 Register** **50000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_DSI_MPPLL_SDM_PCW[30:16]														
Type		RW														
Reset		1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_DSI_MPPLL_SDM_PCW[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		RG_DSI_MPPLL_SDM_PCW	**PLL feedback divide ratio** 7-bit integer + 24-bit fractional

1401705C **DSI_PLL_CON3** **DSI PLL Configuration 3 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_DSI_MPPLL_SDM_SSC_DELTA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_DSI_MPPLL_SDM_SSC_DELTA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		RG_DSI_MPPLL_SDM_SSC_DELTA	**PLL SDM SSC amplitude** 16'd0: Min. 16'd65536: Max.
15:0		RG_DSI_MPPLL_SDM_SSC_DELTA1	**PLL SDM SSC amplitude 1** 16'd0: Min. 16'd65536: Max.

14017060 **DSI_PLL_CHG** **DSI PLL Charge Register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_DSI_MPP

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																LL_SDM_PCW_CHG
Type																RW
Reset																1

Bit(s)	Mnemonic	Name	Description
0		RG_DSI_MPPLL_SDM_PCW_CHG	**PLL SDM feedback divide ratio update signal** Updates divide ratio at 0 to 1 falling edge and goes back to 1 after the registers are updated.

14017064 **DSI_PLL_TOP** **DSI PLL TOP Configuration Register** **00000020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_DSI_MPPLL_PRESERVE					RG_DSI_MPPLL_PLLOUT_EN	RG_DSI_MPPLL_S2QDIV		RG_DSI_MPPLL_TSTSEL		RG_DSI_MPPLL_TSTCK_EN	RG_DSI_MPPLL_TST_EN
Type					RW					RW	RW		RW		RW	RW
Reset					0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:7		RG_DSI_MPPLL_PRESERVE	**Preserved register for PLL**
6		RG_DSI_MPPLL_PLLOUT_EN	**Enables PLL output (to LVDS)** 1'b0: Disable 1'b1: Enable
5:4		RG_DSI_MPPLL_S2QDIV	**PLL quadrature phase output divide ratio** 2'b00: Disable 2'b01: /2 2'b1X: /4
3:2		RG_DSI_MPPLL_TSTSEL	**Selects test cicruit input**
1		RG_DSI_MPPLL_TSTCK_EN	**Enables test cicruit clock** 1'b0: Monitor VDC 1'b1: Monitor clock
0		RG_DSI_MPPLL_TST_EN	**Enables test circuit** 1'b0: Disable 1'b1: Enable

14017068 **DSI_PLL_PWR** **DSI PLL Power Control Register** **00000002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

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Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**AD_DSI_MPPLL_SDM_PWR_ACK**							**DA_DSI_MPPLL_SDM_ISO_EN**	**DA_DSI_MPPLL_SDM_PWR_ON**
Type								RU							RW	RW
Reset								0							1	0

Bit(s)	Mnemonic	Name	Description
8		AD_DSI_MPPLL_SDM_PWR_ACK	**Acknowledges PLL power-on** 1'b0: No effect 1'b1: Acknowledge power-on
1		DA_DSI_MPPLL_SDM_ISO_EN	**Enables PLL isolation** 1'b0: Disable 1'b1: Enable
0		DA_DSI_MPPLL_SDM_PWR_ON	**Controls PLL power-on** 1'b0: Power-off 1'b1: Power-on

14017070 DSI_RGS DSI RGS Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**RGS_DSI_LNT_IMP_CAL_OUTPUT**
Type																RU
Reset																0

Bit(s)	Mnemonic	Name	Description
0		RGS_DSI_LNT_IMP_CAL_OUTPUT	Watchdog action flag

14017074 DSI_GPI_EN DSI GPI Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_DSI_GPI_DRIVE_EN	RG_DSI_GPI_SMT_EN	RG_DSI_GPI9_EN	RG_DSI_GPI8_EN	RG_DSI_GPI7_EN	RG_DSI_GPI6_EN	RG_DSI_GPI5_EN	RG_DSI_GPI4_EN	RG_DSI_GPI3_EN	RG_DSI_GPI2_EN	RG_DSI_GPI1_EN	RG_DSI_GPI0_EN
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11		RG_DSI_GPI_DRIVE_EN	**Enables DSI GPI driving strength** 1'b0: Normal 1'b1: Enlarge
10		RG_DSI_GPI_SMT_EN	**Enables DSI GPI Schmitt** 1'b0: Disable 1'b1: Enable
9		RG_DSI_GPI9_EN	**Enables DSI GPI9, mux with PAD_TDN3** 1'b0:Disable 1'b1: Enable
8		RG_DSI_GPI8_EN	**Enables DSI GPI8, mux with PAD_TDP3** 1'b0:Disable 1'b1: Enable
7		RG_DSI_GPI7_EN	**Enables DSI GPI7, mux with PAD_TDN2** 1'b0:Disable 1'b1: Enable
6		RG_DSI_GPI6_EN	**Enables DSI GPI6, mux with PAD_TDP2** 1'b0:Disable 1'b1: Enable
5		RG_DSI_GPI5_EN	**Enables DSI GPI5, mux with PAD_TCN** 1'b0:Disable 1'b1: Enable
4		RG_DSI_GPI4_EN	**Enables DSI GPI4, mux with PAD_TCP** 1'b0:Disable 1'b1: Enable
3		RG_DSI_GPI3_EN	**Enables DSI GPI3, mux with PAD_TDN1** 1'b0:Disable 1'b1: Enable
2		RG_DSI_GPI2_EN	**Enables DSI GPI2, mux with PAD_TDP1** 1'b0:Disable 1'b1: Enable
1		RG_DSI_GPI1_EN	**Enables DSI GPI1, mux with PAD_TDN0** 1'b0:Disable 1'b1: Enable
0		RG_DSI_GPI0_EN	**Enables DSI GPI0, mux with PAD_TDP0** 1'b0:Disable 1'b1: Enable

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14017078 **DSI_GPI_PULL** **DSI GPI Pull Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							RG_DSI_	RG_DSI_	RG_DSI_	RG_DSI_	RG_DSI_	RG_DSI_	RG_DSI_	RG_DSI_	RG_DSI_	RG_DSI_

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							GPI9_PU	GPI8_PU	GPI7_PU	GPI6_PU	GPI5_PU	GPI4_PU	GPI3_PU	GPI2_PU	GPI1_PU	GPI0_PU
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_DSI_GPI9_PD	RG_DSI_GPI8_PD	RG_DSI_GPI7_PD	RG_DSI_GPI6_PD	RG_DSI_GPI5_PD	RG_DSI_GPI4_PD	RG_DSI_GPI3_PD	RG_DSI_GPI2_PD	RG_DSI_GPI1_PD	RG_DSI_GPI0_PD
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
25		RG_DSI_GPI9_PU	**DSI0 GPI9 pull-up** 1'b0: Disable 1'b1: Enable
24		RG_DSI_GPI8_PU	**DSI0 GPI8 pull-up** 1'b0: Disable 1'b1: Enable
23		RG_DSI_GPI7_PU	**DSI0 GPI7 pull-up** 1'b0: Disable 1'b1: Enable
22		RG_DSI_GPI6_PU	**DSI0 GPI6 pull-up** 1'b0: Disable 1'b1: Enable
21		RG_DSI_GPI5_PU	**DSI0 GPI5 pull-up** 1'b0: Disable 1'b1: Enable
20		RG_DSI_GPI4_PU	**DSI0 GPI4 pull-up** 1'b0: Disable 1'b1: Enable
19		RG_DSI_GPI3_PU	**DSI0 GPI3 pull-up** 1'b0: Disable 1'b1: Enable
18		RG_DSI_GPI2_PU	**DSI0 GPI2 pull-up** 1'b0: Disable 1'b1: Enable
17		RG_DSI_GPI1_PU	**DSI0 GPI1 pull-up** 1'b0: Disable 1'b1: Enable
16		RG_DSI_GPI0_PU	**DSI0 GPI0 pull-up** 1'b0: Disable 1'b1: Enable
9		RG_DSI_GPI9_PD	**DSI0 GPI9 pull-down** 1'b0: Disable 1'b1: Enable
8		RG_DSI_GPI8_PD	**DSI0 GPI8 pull-down** 1'b0: Disable 1'b1: Enable
7		RG_DSI_GPI7_PD	**DSI0 GPI7 pull-down** 1'b0: Disable 1'b1: Enable
6		RG_DSI_GPI6_PD	**DSI0 GPI6 pull-down** 1'b0: Disable 1'b1: Enable

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Bit(s)	Mnemonic	Name	Description
5		RG_DSI_GPI5_PD	**DSI0 GPI5 pull-down** 1'b0: Disable 1'b1: Enable
4		RG_DSI_GPI4_PD	**DSI0 GPI4 pull-down** 1'b0: Disable 1'b1: Enable
3		RG_DSI_GPI3_PD	**DSI0 GPI3 pull-down** 1'b0: Disable 1'b1: Enable
2		RG_DSI_GPI2_PD	**DSI0 GPI2 pull-down** 1'b0: Disable 1'b1: Enable
1		RG_DSI_GPI1_PD	**DSI0 GPI1 pull-down** 1'b0: Disable 1'b1: Enable
0		RG_DSI_GPI0_PD	**DSI0 GPI0 pull-down** 1'b0: Disable 1'b1: Enable

1401707C **DSI_PHY_SEL** **DSI MIPI TX PHY Lane Swap Selection** **00043210**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										MIPI_TX_LPRX_SEL				MIPI_TX_PHYC_SEL		
Type										RW				RW		
Reset										0	0	0		1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		MIPI_TX_PHY3_SEL				MIPI_TX_PHY2_SEL				MIPI_TX_PHY1_SEL				MIPI_TX_PHY0_SEL		
Type		RW				RW				RW				RW		
Reset		0	1	1		0	1	0		0	0	1		0	0	0

Bit(s)	Mnemonic	Name	Description
22:20		MIPI_TX_LPRX_SEL	**Selects MIPI TX PHY Lane RX**
18:16		MIPI_TX_PHYC_SEL	**Selects MIPI TX PHY Lane CK**
14:12		MIPI_TX_PHY3_SEL	**Selects MIPI TX PHY Lane 3**
10:8		MIPI_TX_PHY2_SEL	**Selects MIPI TX PHY Lane 2**
6:4		MIPI_TX_PHY1_SEL	**Selects MIPI TX PHY Lane 1**
2:0		MIPI_TX_PHY0_SEL	**Selects MIPI TX PHY Lane 0** 3'd0: DSI lane 0 3'd1: DSI lane 1 3'd2: DSI lane 2 3'd3: DSI lane 3 3'd4: DSI lane CK

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14017080	DSI_SW_CTRL_EN	DSI Software Control Enable Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MIPI_TX_SW_CTRL_EN
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0		MIPI_TX_SW_CTRL_EN	**Enables DSI software control** 1'b0: Disable 1'b1: Enable

14017084	DSI_SW_CTRL_CON0	DSI Software Control Configuration Register 0	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIPI_TX_SW_LNTC_HSTX_DATA								MIPI_TX_SW_LNTC_LPRX_EN	MIPI_TX_SW_LNTC_HSTX_RDY	MIPI_TX_SW_LNTC_HSTX_OE	MIPI_TX_SW_LNTC_HSTX_PRE_OE	MIPI_TX_SW_LNTC_LPTX_DN	MIPI_TX_SW_LNTC_LPTX_DP	MIPI_TX_SW_LNTC_LPTX_OE	MIPI_TX_SW_LNTC_LPTX_PRE_OE
Type	RW								RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8		MIPI_TX_SW_LNTC_HSTX_DATA	DSI CK Lane HSTX Data
7		MIPI_TX_SW_LNTC_LPRX_EN	DSI CK Lane LPRX Enable
6		MIPI_TX_SW_LNTC_HSTX_RDY	DSI CK Lane HSTX Ready
5		MIPI_TX_SW_LNTC_HSTX_OE	DSI CK Lane HSTX OE
4		MIPI_TX_SW_LNTC_HSTX_PRE_OE	DSI CK Lane HSTX Pre OE
3		MIPI_TX_SW_LNTC_LPTX_DN	DSI CK Lane LPTX DN

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Bit(s)	Mnemonic	Name	Description
2		MIPI_TX_SW_LNTC_LPTX_DP	DSI CK Lane LPTX DP
1		MIPI_TX_SW_LNTC_LPTX_OE	DSI CK Lane LPTX OE
0		MIPI_TX_SW_LNTC_LPTX_PRE_OE	DSI CK Lane LPTX Pre OE

14017088	DSI_SW_CTRL_CON1	DSI Software Control Configuration Register 1	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIPI_TX_SW_LNT3_LPRX_EN	MIPI_TX_SW_LNT3_HSTX_RDY	MIPI_TX_SW_LNT3_HSTX_OE	MIPI_TX_SW_LNT3_HSTX_PRE_OE	MIPI_TX_SW_LNT3_LPTX_DN	MIPI_TX_SW_LNT3_LPTX_DP	MIPI_TX_SW_LNT3_LPTX_OE	MIPI_TX_SW_LNT3_LPTX_PRE_OE	MIPI_TX_SW_LNT2_LPRX_EN	MIPI_TX_SW_LNT2_HSTX_RDY	MIPI_TX_SW_LNT2_HSTX_OE	MIPI_TX_SW_LNT2_HSTX_PRE_OE	MIPI_TX_SW_LNT2_LPTX_DN	MIPI_TX_SW_LNT2_LPTX_DP	MIPI_TX_SW_LNT2_LPTX_OE	MIPI_TX_SW_LNT2_LPTX_PRE_OE
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIPI_TX_SW_LNT1_LPRX_EN	MIPI_TX_SW_LNT1_HSTX_RDY	MIPI_TX_SW_LNT1_HSTX_OE	MIPI_TX_SW_LNT1_HSTX_PRE_OE	MIPI_TX_SW_LNT1_LPTX_DN	MIPI_TX_SW_LNT1_LPTX_DP	MIPI_TX_SW_LNT1_LPTX_OE	MIPI_TX_SW_LNT1_LPTX_PRE_OE	MIPI_TX_SW_LNT0_LPRX_EN	MIPI_TX_SW_LNT0_HSTX_RDY	MIPI_TX_SW_LNT0_HSTX_OE	MIPI_TX_SW_LNT0_HSTX_PRE_OE	MIPI_TX_SW_LNT0_LPTX_DN	MIPI_TX_SW_LNT0_LPTX_DP	MIPI_TX_SW_LNT0_LPTX_OE	MIPI_TX_SW_LNT0_LPTX_PRE_OE
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		MIPI_TX_SW_LNT3_LPRX_EN	DSI Data Lane 3 LPRX Enable
30		MIPI_TX_SW_LNT3_HSTX_RDY	DSI Data Lane 3 HSTX Ready
29		MIPI_TX_SW_LNT3_HSTX_OE	DSI Data Lane 3 HSTX OE
28		MIPI_TX_SW_LNT3_HSTX_PRE_OE	DSI Data Lane 3 HSTX Pre OE
27		MIPI_TX_SW_LNT3_LPTX_DN	DSI Data Lane 3 LPTX DN
26		MIPI_TX_SW_LNT3_LPTX_DP	DSI Data Lane 3 LPTX DP
25		MIPI_TX_SW_LNT3_LPTX_OE	DSI Data Lane 3 LPTX OE
24		MIPI_TX_SW_LNT3_LPTX_PRE_OE	DSI Data Lane 3 LPTX Pre OE
23		MIPI_TX_SW_L	DSI Data Lane 2 LPRX Enable

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Bit(s)	Mnemonic	Name	Description
		NT2_LPRX_EN	
22		MIPI_TX_SW_LNT2_HSTX_RDY	DSI Data Lane 2 HSTX Ready
21		MIPI_TX_SW_LNT2_HSTX_OE	DSI Data Lane 2 HSTX OE
20		MIPI_TX_SW_LNT2_HSTX_PRE_OE	DSI Data Lane 2 HSTX Pre OE
19		MIPI_TX_SW_LNT2_LPTX_DN	DSI Data Lane 2 LPTX DN
18		MIPI_TX_SW_LNT2_LPTX_DP	DSI Data Lane 2 LPTX DP
17		MIPI_TX_SW_LNT2_LPTX_OE	DSI Data Lane 2 LPTX OE
16		MIPI_TX_SW_LNT2_LPTX_PRE_OE	DSI Data Lane 2 LPTX Pre OE
15		MIPI_TX_SW_LNT1_LPRX_EN	DSI Data Lane 1 LPRX Enable
14		MIPI_TX_SW_LNT1_HSTX_RDY	DSI Data Lane 1 HSTX Ready
13		MIPI_TX_SW_LNT1_HSTX_OE	DSI Data Lane 1 HSTX OE
12		MIPI_TX_SW_LNT1_HSTX_PRE_OE	DSI Data Lane 1 HSTX Pre OE
11		MIPI_TX_SW_LNT1_LPTX_DN	DSI Data Lane 1 LPTX DN
10		MIPI_TX_SW_LNT1_LPTX_DP	DSI Data Lane 1 LPTX DP
9		MIPI_TX_SW_LNT1_LPTX_OE	DSI Data Lane 1 LPTX OE
8		MIPI_TX_SW_LNT1_LPTX_PRE_OE	DSI Data Lane 1 LPTX Pre OE
7		MIPI_TX_SW_LNT0_LPRX_EN	DSI Data Lane 0 LPRX Enable
6		MIPI_TX_SW_LNT0_HSTX_RDY	DSI Data Lane 0 HSTX Ready
5		MIPI_TX_SW_LNT0_HSTX_OE	DSI Data Lane 0 HSTX OE
4		MIPI_TX_SW_LNT0_HSTX_PRE_OE	DSI Data Lane 0 HSTX Pre OE
3		MIPI_TX_SW_LNT0_LPTX_DN	DSI Data Lane 0 LPTX DN
2		MIPI_TX_SW_LNT0_LPTX_DP	DSI Data Lane 0 LPTX DP
1		MIPI_TX_SW_LNT0_LPTX_OE	DSI Data Lane 0 LPTX OE
0		MIPI_TX_SW_LNT0_LPTX_PRE_OE	DSI Data Lane 0 LPTX Pre OE

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1401708C **DSI_SW_CTRL_CON2** **DSI Software Control Configuration Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MIPI_TX_SW_LNTD_HSTX_DATA							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		MIPI_TX_SW_LNTD_HSTX_DATA	DSI Data Lane 0~3 HSTX Data

14017090 **DSI_DBG_CON** **DSI Debug Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MIPI_TX_TST_CK_OUT_SEL	MIPI_TX_TST_CK_OUT_EN	MIPI_TX_APB_ASYNC_CNT_EN	MIPI_TX_GPIO_MODE_EN	MIPI_TX_DBG_OUT_EN	MIPI_TX_DBG_SEL			
Type								RW	RW	RW	RW	RW	RW			
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8		MIPI_TX_TST_CK_OUT_SEL	Selects MIPI clocks to frequency meter
7		MIPI_TX_TST_CK_OUT_EN	Enables MIPI clock output to frequency meter
6		MIPI_TX_APB_ASYNC_CNT_EN	Enables APB async RX debugging counter
5		MIPI_TX_GPIO_MODE_EN	Enables GPIO of MIPI TX pads
4		MIPI_TX_DBG_OUT_EN	Enables debugging output of MIPI probe bus
3:0		MIPI_TX_DBG_SEL	Selects debug mux of MIPI debugging bus

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14017094 **DSI_DBG_OUT** **DSI Debug Out Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIPI_TX_DBG_OUT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIPI_TX_DBG_OUT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MIPI_TX_DBG_OUT	MIPI debug bus out status

14017098 **DSI_APB_ASYNC_STA** **DSI APB Async Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						MIPI_TX_APB_ASYNC_ERR_ADDR										MIPI_TX_APB_ASYNC_ERR
Type						RO										RO
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
10:1		MIPI_TX_APB_ASYNC_ERR_ADDR	MIPI APB async error address
0		MIPI_TX_APB_ASYNC_ERR	MIPI APB async error status

6.22.4 Programming Guide

6.22.4.1 MIPI PLL Initial Sequence

Figure 6-77 illustrates the waveform of the initial sequence to enable power of MIPI DPHY macro and initialize MIPI PLL. The user should follow the steps described in Table 6-23 to perform waveform behavior for MIPI DPHY control. In this example, 520MHz clock is set.

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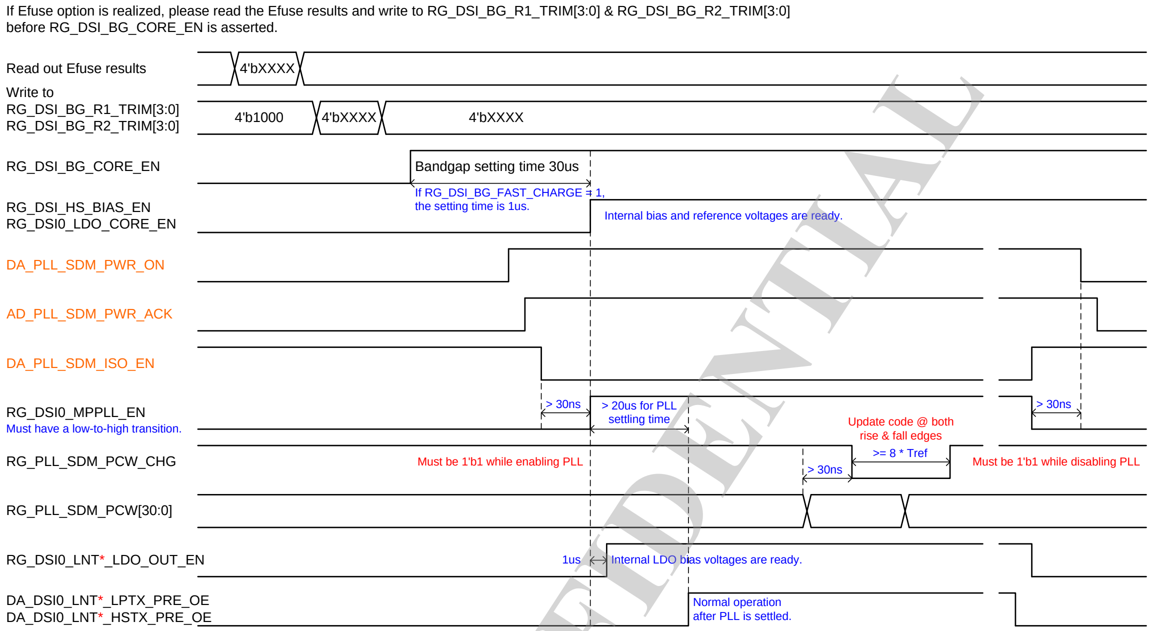

Figure 6-77. Initial waveform of MIPI PLL

Table 6-25. MIPI PLL initial sequence

Step	Description	R/W	Register [bit]	Value
1	Enable 26MHz reference clock	W	AP_PLL_CON0 [6] (0x10209000)	1
2	Enable BG core power and clock	W	DSI_BG_CON [1:0]	3
3	Wait for 30 us	-		
4	Enable HS bias	W	DSI_TOP_CON [1]	1
5	Enable LDO core power and CKG	W	DSI_CON [1:0]	3
6	Enable PLL power	W	DSI_PLL_PWR [0]	1
7	Disable PLL isolation	W	DSI_PLL_PWR [1]	0
8	Set divider control for PLL (no division)	W	DSI_PLL_CON0 [9:1]	0
9	Set SSC control for PLL (no SSC)	W	DSI_PLL_CON1	1
10	Set PLL frequency (512MHz)	W	DSI_PLL_CON2	0x50000000
11	Enable clock lane	W	DSI_CLOCK_LANE [0]	1
12	Enable data lane 0	W	DSI_DATA_LANE_0 [0]	1
13	Enable data lane 1	W	DSI_DATA_LANE_1 [0]	1
14	Enable data lane 2	W	DSI_DATA_LANE_2 [0]	1
15	Enable data lane 3	W	DSI_DATA_LANE_3 [0]	1
16	Enable PLL	W	DSI_PLL_CON0 [0]	1
17	Wait for 20 us	-		
18	Disable pad tie low	W	DSI_TOP_CON [11]	0

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6.22.4.2 MIPI PLL De-initial Sequence

For power-off of MIPI PLL for sleep-in or suspend purpose, follow the steps listed in Table 6-26. Be sure to make all registers to default settings to avoid unexpected power consumption.

Table 6-26. MIPI PLL de-initial sequence

Step	Description	R/W	Register [bit]	Value
1	Disable PLL	W	DSI_PLL_CON0 [0]	0
2	Enable pad tie low	W	DSI_TOP_CON [11]	1
3	Disable clock lane	W	DSI_CLOCK_LANE [0]	0
4	Disable data lane 0	W	DSI_DATA_LANE_0 [0]	0
5	Disable data lane 1	W	DSI_DATA_LANE_1 [0]	0
6	Disable data lane 2	W	DSI_DATA_LANE_2 [0]	0
7	Disable data lane 3 (if it exists)	W	DSI_DATA_LANE_3 [0]	0
8	Enable PLL isolation	W	DSI_PLL_PWR [1]	1
9	Disable PLL power	W	DSI_PLL_PWR [0]	0
10	Disable HS bias	W	DSI_TOP_CON [1]	0
11	Disable LDO core power and CG	W	DSI_CON [1:0]	0
12	Disable BG core power and clock	W	DSI_BG_CON [1:0]	0
13	Reset divider control for PLL	W	DSI_PLL_CON0 [9:1]	0
14	Reset SSC control for PLL	W	DSI_PLL_CON1	0
15	Reset PLL frequency (default value)	W	DSI_PLL_CON2	0x50000000
16	Disable 26MHz reference clock	W	AP_PLL_CON0 [6] (0x10209000)	0

6.22.4.3 Suspend/Resume Control

If the system enters suspend mode, DSI module should be operated to enter the ultra-low power state (ULPS) before execution of the sequence shown in Table 6-26. When the system needs to resume from suspend mode, the sequence shown in Table 6-23 should be performed first followed by the ULPS-exit procedure to return the normal output status.

6.22.5 Software Control Mode

The software control mode allows user control output DP/DN pads directly. It is usually used for test or signal measurement. To enable output signals, it needs to setup PRE_OE and OE bits under this mode. Table 6-27 is an example of software control mode operation which sets all output pads to low voltage.

Table 6-27. Software control mode example

Step	Description	R/W	Register [bit]	Value
1	Set up clock lane PRE_OE/OE signal	W	DSI_SW_CTRL_CON0 [1:0]	0x3
2	Set up Data Lane 0 PRE_OE/OE signal	W	DSI_SW_CTRL_CON0 [8:7]	0x3

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Step	Description	R/W	Register [bit]	Value
3	Set up Data Lane 1 PRE_OE/OE signal	W	DSI_SW_CTRL_CON0 [15:14]	0x3
4	Set up Data Lane 2 PRE_OE/OE signal	W	DSI_SW_CTRL_CON0 [21:20]	0x3
5	Set up Data Lane 3 PRE_OE/OE signal	W	DSI_SW_CTRL_CON0 [27:26]	0x3
6	Enable software control mode	W	DSI_SW_CTRL_EN	1

6.22.5.1 MIPI PLL SSC

MIPI PLL supports SSC (Spread-Spectrum Control) with fractional précised frequency multiplication. To enable SSC function, the user needs to set up the SSC_EN bit of register DSI_PLL_CON1 and other proper settings. Table 6-28 is an example of initial sequence with SSC for 0 ~ -4% and frequency of 208MHz.

Table 6-28. MIPI PLL initial sequence with SSC enable

Step	Description	R/W	Register [bit]	Value
1	Enable BG core power and clock	W	DSI_BG_CON [1:0]	3
2	Wait for 30 us	-		
3	Enable HS bias	W	DSI_TOP_CON [1]	1
4	Enable LDO core power and CG	W	DSI_CON [1:0]	3
5	Enable PLL power	W	DSI_PLL_PWR [0]	1
6	Disable PLL isolation	W	DSI_PLL_PWR [1]	0
7	Set up TXDIV0 divider (divided by 2)	W	DSI_PLL_CON0 [4:3]	1
8	Set up SSC fraction enable	W	DSI_PLL_CON1 [0]	1
9	Set up SSC phase initial (downward)	W	DSI_PLL_CON1 [1]	1
10	Set up SSC period	W	DSI_PLL_CON1 [31:16]	0x01B1
11	Set up PLL frequency	W	DSI_PLL_CON2	0x40000000
12	Set up SSC amplitude	W	DSI_PLL_CON3	0x07900790
13	Enable clock lane	W	DSI_CLOCK_LANE [0]	1
14	Enable Data Lane 0	W	DSI_DATA_LANE_0 [0]	1
15	Enable Data Lane 1	W	DSI_DATA_LANE_1 [0]	1
16	Enable Data Lane 2	W	DSI_DATA_LANE_2 [0]	1
17	Enable Data Lane 3	W	DSI_DATA_LANE_3 [0]	1
18	Enable PLL	W	DSI_PLL_CON0 [0]	1
19	Wait for 20 us	-		
20	Enable SSC	W	DSI_PLL_CON1 [2]	1
21	Disable pad tie low	W	DSI_TOP_CON [11]	0

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6.23 JPEG Encoder

6.23.1 Introduction

The hardware JPEG encoder implements the baseline mode of Standard ISO/IEC 10918-1. After initialization by software, the hardware JPEG encoder can generate the entire compressed file. Figure 6-78 shows the procedure of the JPEG encoder. The YUV pixel data are retrieved from the memory and grouped into 8x8 blocks. YUV422 one plane and YUV420 two plane formats are supported. When encoding, the first thing to do is turning the pixel data into the frequency domain using FDCT. After the quantization is done, the quantized DCT coefficients are encoded by RLE and VLC. Then the bitstream of JPEG file is generated.

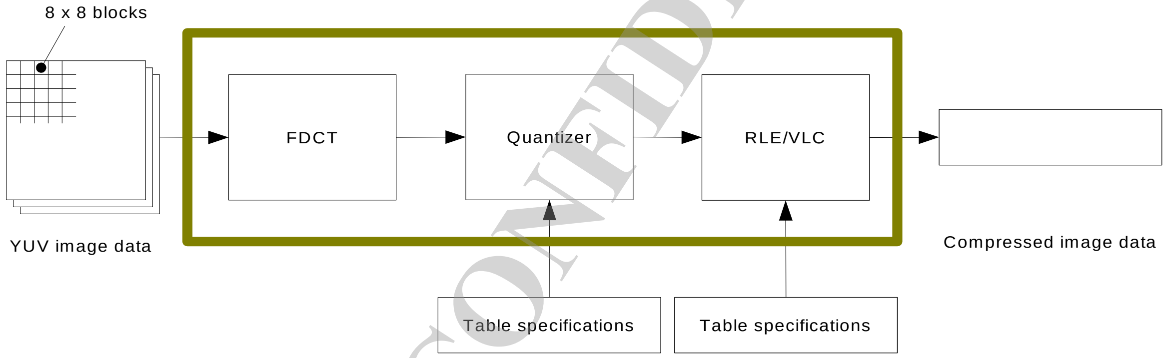

Figure 6-78. Procedure of JPEG encoder

6.23.2 Features

The JPEG encoder supports YUV 422 and 420 formats for color pictures. With software assistance and suitable destination memory address setting; JFIF/EXIF JPEG format can also be supported. For hardware reduction, it uses standard DC and AC Huffman tables for both luminance and chrominance components. To adjust the picture compression ratio and picture quality, there are 15 levels of quantization that can be programmed.

6.23.2.1 Software Reset Mechanism

To avoid problem occurred with wrong SMI protocol, the software should do reset based on the following procedure.

1. The EN bit in JPGENC_CTL should be set to 0.
2. The software polls the GMC_IDLE bit in JPGENC_DEBUG_INFO0.

Only when the GMC_IDLE bit is 1 can the RSTB bit in JPGENC_RST be set to 0 to do the reset scheme. Be sure to follow this procedure to do software reset.

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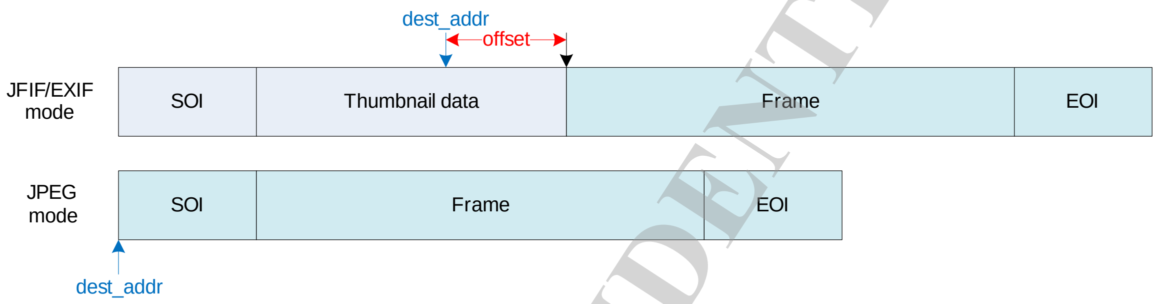
6.23.2.2 Byte Offset Address Setting

To align SMI bus bitwidth, the buffer address should be 16-bytes aligned. However, to reduce software bitstream copy and concatenate effort, software can program a byte offset setting (from 0~15 bytes) to offset the start position of bitstream written out by hardware. The illustration of this feature is as the following.



- Example: If SOI starts at 0x0000,
  - JFIF/EXIF mode: SOI+thumbnail data length = 50 bytes
    - dest_addr = 0x0030
      offset = 0x0002

6.23.3 DRAM Buffer Requirement

- Source frame buffer
  - YUV422:
    - One frame buffer
    - Buffer size
      - {[(width_y*2) + 127]/128}*128*[(height_y + 7)/8]*8
  - YUV420: Two frame buffers
    - Two frame buffers
    - Buffer size
      - Y: [(width_y + 127)/128]*128*[(height_y + 15)/16]*16
      - UV: [(width_y + 127)/128]*128*[(height_y + 7)/8]*8
- Bitstream buffer
  - One buffer
  - Buffer size (suggested)
    - YUV422: width_y* height_y * 2
    - YUV420: width_y* height_y * 1.5
    - Must be multiple of 128 bytes.

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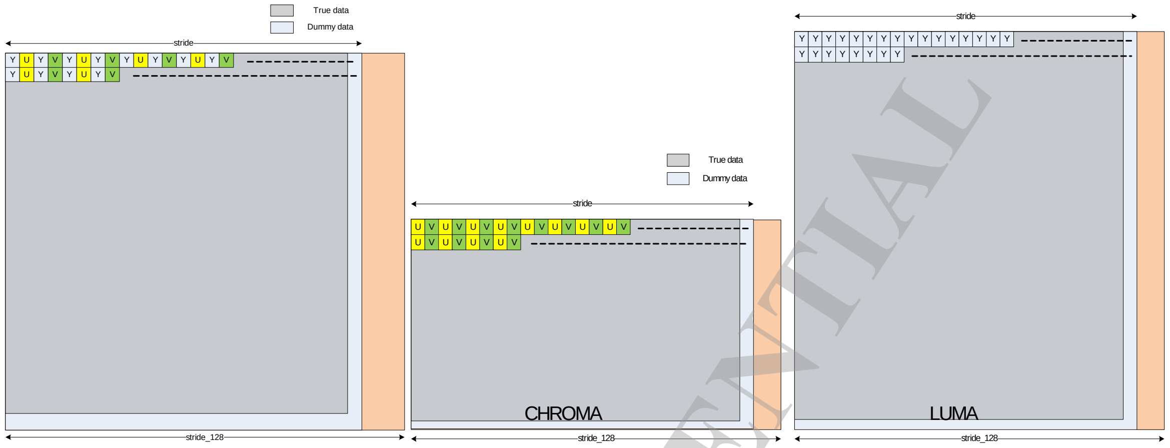

Figure 6-79. Memory footprint of source frame buffer

6.23.4 Register Definition

Module name: jpgenc Base address: (+17003000h)

Address	Name	Width	Register Function
17003100	JPGENC_RSTB	32	JPEG Encoder Reset Register
17003104	JPGENC_CTRL	32	JPEG Encoder Control Register
17003108	JPGENC_QUALITY	32	JPEG Encoder Quality Setting Register
1700310C	JPGENC_BLK_NUM	32	JPEG Encoder Total Block Number Register
17003110	JPGENC_BLK_CNT	32	JPEG Encoder Current Block Count Register
1700311C	JPGENC_INT_STS	32	JPEG Encoder Interrupt Status Register
17003120	JPGENC_DST_ADDR0	32	JPEG Encoder Destination Address 0 Register
17003124	JPGENC_DMA_ADDR0	32	JPEG Encoder Write Address 0 Register
17003128	JPGENC_STALL_ADDR0	32	JPEG Encoder Stall Address 0 Register
17003138	JPGENC_OFFSET_ADDR	32	JPEG Encoder Offset Address Register
1700313C	JPGENC_CURR_DMA_ADDR	32	JPEG Encoder Current Write Address Register
17003150	JPGENC_RST_MCU_NUM	32	JPEG Encoder Restart MCU Number Register
17003154	JPGENC_IMG_SIZE	32	JPEG Encoder Image Size Register
17003160	JPGENC_DEBUG_INFO0	32	JPEG Encoder Debug Information 0 Register
17003164	JPGENC_DEBUG_INFO1	32	JPEG Encoder Debug Information 1 Register
17003168	JPGENC_TOTAL_CYCLE	32	JPEG Encoder Performance Counter Register
1700316C	JPGENC_BYTE_OFFSET_MASK	32	JPEG Encoder Destination Address Offset Mask Register

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Address	Name	Width	Register Function
17003170	JPGENC_SRC_LUMA_ADDR	32	JPEG Encoder Luma Source Data Base Address Register
17003174	JPGENC_SRC_CHROMA_ADDR	32	JPEG Encoder Chroma Source Data Base Address Rregister
17003178	JPGENC_STRIDE	32	JPEG Encoder Memory Stride Register
1700317C	JPGENC_IMG_STRIDE	32	JPEG Encoder Image Stride Width Register
17003200	JPGENC_RDMA_CHKSUM	32	JPEG Encoder RDMA Checksum
17003204	JPGENC_BSDMA_CHKSUM	32	JPEG Encoder BSDMA Checksum
17003300	JPGENC_DCM_CTRL	32	JPEG Encoder DCM Control Register
17003318	JPGENC_ULTRA_THRES	32	JPEG Encoder Ultra Threshold Control Register
1700331C	JPGENC_LATENCY_THRES	32	JPEG Encoder Latency Threshold Control Register
17003400	JPGENC_IRQ_EN	32	JPEG Encoder IRQ Enable Control Register

17003100 **JPGENC_RSTB** **JPEG Encoder Reset Register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RSTB
Type																RW
Reset																1

Bit(s)	Name	Description
0	RSTB	**Resets JPEG encoder's active-low** 0: Reset mode 1: Normal mode After the JPEG encoder is reset, the RSTB bit should be re-assigned to 1. *Note: Reset the JPEG encoder before encoding each new image.* *If it is required to reset the encoder during encoding, follow the soft reset mechanism. Hard reset may cause unexpected SMI behavior.*

17003104 **JPGENC_CTRL** **JPEG Encoder Control Register** **00000004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				ULTRA_CTRL												
Type				RW												
Reset				0	0	0	0									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RST_MARK					JPG	YUV		INT_EN		EN

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Type						RW					RW	RW		RW		RW
Reset						0					0	0	0	1		0

Bit(s)	Name	Description
28:25	ULTRA_CTRL	**Controls JPEG SMI port ultra option enabling** Set to 1 to enable the corresponding option. bit[27]: RDMA GULTRA bit[26]: RDMA GPREULTRA bit]25]: BSDMA GULTRA bit[24]: BSDMA GPREULTRA
10	RST_MARK	**Restarts interval encoding process enabling** 0: Disable 1: Enable JPEG encoder inserts restart marker based on JPGENC_RST_MCU_NUM; JPGENC_RST_MCU_NUM must be given one value that is bigger than 0.
5	JPG	**JPEG or JFIF/EXIF** 0: JPEG mode 1: JFIF/EXIF If JFIF/EXIF format is enabled, the JPEG encoder will not write out SOI marker (starting from 0xffd8) but write out from DQT maker (starting from 0xffdb). Software program can fill the JFIF/EXIF content above the DQT marker to finish one JFIF/EXIF JPEG file.
4:3	YUV	**YUV format** 0: YUV422 (YUYV) 1: YUV422 (YVYU) 2: YUV420 (NV12) 3: YUV420 (NV21)
2	INT_EN	**Enables interrupt** 0: Disable 1: Enable
0	EN	**Triggers signal to enable JPEG encoder** This bit is cleared by hardware after encoding is done. For software reset, this bit should be set to 0 first.

17003108 **JPGENC_QUALITY** **JPEG Encoder Quality Setting Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**QT**			**QUALITY**	
Type												RW			RW	
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:2	QT	**Quantization table setting for frame 1** Only works in continuous shooting mode. 00: High quality table 01: Good quality table 10: Fair quality table 11: Low quality table
1:0	QUALITY	**Quantization level setting for frame 1** Only works in continuous shooting mode.

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Bit(s)	Name	Description
		00: Low; only for high and good quality quantization table 01: Fair 10: Good 11: High

1700310C **JPGENC_BLK_NUM** **JPEG Encoder Total Block Number Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						BLK_NUM[26:16]										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BLK_NUM[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	BLK_NUM	**Total 8x8 block number** Min value: 4. (Image with block number less than 4 cannot be encoded, which is the hardware limitation) *Note: The dummy 8x8 block must be considered in BLK_NUM. For example, a 162x128 YUV420 JPEG file, the block number setting should be 527.*

17003110 **JPGENC_BLK_CNT** **JPEG Encoder Current Block Count Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RD_RLE					BLK_CNT[26:16]										
Type	RW					RO										
Reset	0					0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BLK_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RD_RLE	**Read RLE current 8x8 block count control** 0: FDCT current block count 1: RLE current block count
26:0	BLK_CNT	**Current encoded 8x8 block number**

1700311C **JPGENC_INT_STS** **JPEG Encoder Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												ERR			STA	ENC

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												OR			LL	ODE_DONE
Type												RW			RW	RW
Reset												0			0	0

Bit(s)	Name	Description
4	ERROR	**Shows if codec selection is accessed by video encoder when JPGENC is working**
1	STALL	**Stall interrupt** Indicates that encoding operation is reaching the memory bound configured by software and entering stall condition. Set this bit to 0 after reading and reset hardware to start another encoding process.
0	ENCODE_DONE	**Done interrupt** Indicates that encoding operation is done. Set to 0 after reading.

17003120 **JPGENC_DST_ADDR0** **JPEG Encoder Destination Address 0 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEST_ADDR0[27:12]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEST_ADDR0[11:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	DEST_ADDR0	**JPEG encoder destination address setting 0** Must be 16-byte aligned.

17003124 **JPGENC_DMA_ADDR0** **JPEG Encoder Write Address 0 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA_ADDR0[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_ADDR0[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DMA_ADDR0	**JPEG encoder current written address setting 0** This address information will be updated after every one burst write command is finished.

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17003128 **JPGENC_STALL_ADDR0** **JPEG Encoder Stall Address 0 Register** **000000F0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STALL_ADDR0[27:12]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STALL_ADDR0[11:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	1	1	1				

Bit(s)	Name	Description
31:4	STALL_ADDR0	**JPEG encoder stall address setting 0** The stall address must be 16-byte aligned and should be set to bigger than the actual upper bound by one burst command (128 bytes). Whenever the stall address is reached, the JPEG encoder stalls and issues an interrupt to software. The software can discard the incomplete file by simply resetting the JPEG encoder to cancel the encoding operation. It is also essential that the value of JPGENC_STALL_ADDR should be bigger than JPGENC_DEST_ADDR by at least 624 bytes to guarantee the header of the JPEG file can be completely written into memory. *Note: JPG_ENC_STALL_ADDR should not be set to smaller than JPG_ENC_DEST_ADDR; otherwise stall condition will occur.*

17003138 **JPGENC_OFFSET_ADDR** **JPEG Encoder Offset Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFFSET_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
15:4	OFFSET_ADDR	**JPEG encoder offset address** This address must be 16-byte aligned. OFFSET_ADDR should be set to 0 if this function is not needed. *Note: OFFSET_ADDR is set before starting encoding process only to offset the destination address for the application such as EXIF mode.*

1700313C **JPGENC_CURR_DMA_ADDR** **JPEG Encoder Current Write Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CURR_DMA_ADDR[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CURR_DMA_ADDR[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	CURR_DMA_ADDR	Current DMA address during encoding

17003150 **JPGENC_RST_MCU_NUM** **JPEG Encoder Restart MCU Number Register** **00000004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RST_MCU_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
15:0	RST_MCU_NUM	**JPEG encoder restart interval** If the marker restart feature is enabled, the JPEG encoder will insert one re-start marker when this defined MCU number is encoded. For example, if you are to insert one re-start marker every N MCUs, RST_MCU_MUN must be programmed as N. *Note: The setting of RST_MCU_NUM should be bigger than 0 if restart marker insertion is enabled.*

17003154 **JPGENC_IMG_SIZE** **JPEG Encoder Image Size Register** **0A200798**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	XSIZE															
Type	RW															
Reset	0	0	0	0	1	0	1	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	YSIZE															
Type	RW															
Reset	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0	0

Bit(s)	Name	Description
31:16	XSIZE	Width of the current image
15:0	YSIZE	Height of the current image

17003160 **JPGENC_DEBUG_INFO0** **JPEG Encoder Debug Information 0 Register** **00022000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							PXL_VLD	DMA_REQ							VLC_EPY	END_IMG
Type							RO	RO							RO	RO
Reset							0	0							1	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**GMC_IDLE**	**HEAD**								**GREQ**	**ENC_STATE**			
Type			RO	RO								RO	RO			
Reset			1	0								0	0	0	0	0

Bit(s)	Name	Description
25	PXL_VLD	**Date valid indicator from JPEG DMA** 0: Idle 1: Valid
24	DMA_REQ	**Request status between JPEG encoder and JPEG DMA** 0: Idle 1: Active
17	VLC_EPY	**Empty status of VLC buffer** 0: Not empty 1: Empty
16	END_IMG	**Frame ending indicator** 0: Not in frame ending 1: Process the last block data of current frame
13	GMC_IDLE	**Status of GMC port for JPEG encoder** 0: Active 1: Idle
12	HEAD	**Header generation indicator** 0: JPEG encoder does not generate header stream. 1: JPEG encoder generates header stream.
4	GREQ	**Memory access status** 0: Active 1: Idle
3:0	ENC_STATE	**FSM status of JPEG encoder** 0: IDLE 1: INIT 2: START_HEADER 3: HEADER_GEN 4: WAIT_FST_FDCT 5: TRANS_COEFF 6: WAIT_RLE 7: WAIT_FDCT 8: WAIT_DONE 9: WAIT_ENC_DONE 10: WAIT_FST_FDCT_RDY 11: STOP_BLK 12: WAIT_TO_IDLE

17003164 **JPGENC_DEBUG_INFO1** **JPEG Encoder Debug Information 1 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RLE_CYCLE_CNT[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RLE_CYCLE_CNT[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	RLE_CYCLE_CNT	Process cycle of Huffman encoding

17003168 **JPGENC_TOTAL_CYCLE** **JPEG Encoder Performance Counter Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TOTAL_CYCLE[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOTAL_CYCLE[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TOTAL_CYCLE	Total cycle count of JPEG encoder

1700316C **JPGENC_BYTE_OFFSET_MASK** **JPEG Encoder Destination Address Offset Mask Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYTE_OFFSET_MASK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BYTE_OFFSET_MASK	0: No offset 1~15: Offset byte from the 16-byte aligned destination address setting Actual destination address = Destination address +offset address + destination address offset mask Bit 4 ~ 15 are reserved for future use.

17003170 **JPGENC_SRC_LUMA_ADDR** **JPEG Encoder Luma Source Data Base Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LUMA_BASE[27:12]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_BASE[11:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:4	LUMA_BASE	**LUMA source data base address** YUV422: Memory base address of image data YUV420: Memory base address of luma image data

17003174 JPGENC_SRC_CHROMA_ADDR JPEG Encoder Chroma Source Data Base Address Rregister 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHROMA_BASE[27:12]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHROMA_BASE[11:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	CHROMA_BASE	**CHROMA source data base address** YUV422: Not used YUV420: Memory base address of chroma image data

17003178 JPGENC_STRIDE JPEG Encoder Memory Stride Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STRIDE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
15:4	STRIDE	**JPEG encoder memory stride register** Must be 128-byte aligned.

1700317C JPGENC_IMG_STRIDE JPEG Encoder Image Stride Width Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STRIDE_IMG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

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Bit(s)	Name	Description
15:4	STRIDE_IMG	**JPEG encoder image stride register** Must be MCU alignment. For YUV422, it is 32-byte aligned. For YUV420, it is 16-byte aligned.

17003200 **JPGENC_RDMA_CHKSUM** **JPEG Encoder RDMA Checksum** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA_CHKSUM[31:16]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA_CHKSUM[15:0]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	RDMA_CHKSUM	Checksum

17003204 **JPGENC_BSDMA_CHKSUM** **JPEG Encoder BSDMA Checksum** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BSDMA_CHKSUM[31:16]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSDMA_CHKSUM[15:0]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	BSDMA_CHKSUM	Checksum

17003300 **JPGENC_DCM_CTRL** **JPEG Encoder DCM Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																STATUS
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DISABLE
Type																RW
Reset																0

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Bit(s)	Name	Description
16	STATUS	**0: JPGENC clock is off.** 1: JPGENC clock is on.
0	DISABLE	**0: Enable JPGENC DCM (default)** 1: Disable JPGENC DCM

17003318 JPGENC_ULTRA_THRES JPEG Encoder Ultra Threshold Control Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA_ULTRA_THRES								RDMA_PREULTRA_THRES							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSDMA_ULTRA_THRES								BSDMA_PREULTRA_THRES							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	RDMA_ULTRA_THRES	**Sets up RDMA gultra threshold** Useful if the corresponding ultra enabling bit is set.
23:16	RDMA_PREULTRA_THRES	**Sets up RDMA gpreultra threshold** Useful if the corresponding preultra enabling bit is set.
15:8	BSDMA_ULTRA_THRES	**Sets up BSDMA gultra threshold** Useful if the corresponding ultra enabling bit is set.
7:0	BSDMA_PREULTRA_THRES	**Sets up BSDMA gpreultra threshold** Useful if the corresponding preultra enabling bit is set.

1700331C JPGENC_LATENCY_THRES JPEG Encoder Latency Threshold Control Register 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA_LATENCY_EN	BSDMA_LATENCY_EN														
Type	RW	RW														
Reset	0	0														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA_LATENCY_THRES								BSDMA_LATENCY_THRES							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31	RDMA_LATENCY_EN	Set to 1 to enable RDMA latency request control
30	BSDMA_LATENCY_EN	Set to 1 to enable BSDMA latency requset control
15:8	RDMA_LATENCY_	Sets up RDMA latency threshold

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Bit(s)	Name	Description
	THRES	
7:0	BSDMA_LATENCY_THRES	Sets up BSDMA latency threshold

17003400 JPGENC_IRQ_EN JPEG Encoder IRQ Enable Control Register 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CMDQ_EN															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														IRQ_EN		
Type														WO		
Reset														1	1	1

Bit(s)	Name	Description
31	CMDQ_EN	**Set to 1 to enable frame done signal to command queue**
2:0	IRQ_EN	**Set to 1 to enable each IRQ status** bit[0]: Error bit[1]: Stall bit[2]: Encoding done When command queue is used, set bit[2] to 0.

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6.24 JPEG Decoder

6.24.1 Introduction

At present most images must be stored as JPEG format compressed files. In order to display this kind of files and boost image processing performance, the hardware JPEG decoder is developed. The JPEG decoder is designed to decode baseline JPEG file with general YUV sampling combinations. (Note that the progressive decoding is NOT supported in the hardware decoder).

To obtain the best speed performance, the JPEG decoder handles all portions of JPEG files except for the 17-byte SOF marker. The software only needs to program related control registers based on the SOF marker and wait for an interrupt coming from the hardware. Figure 6-80 is the basic JPEG file structure and the start address that JPEG decoder needs. The information of DQT and DHT table is included in the JPEG file, which should be parsed by the JPEG decoder and stored in the memory.

Taking into consideration the limited size of memories, the hardware decoder also supports breakpoints insertion in huge JPEG files. Breakpoints insertion allows software to load partial JPEG file from the external flash into the internal memory if the JPEG file is too large to sit internally at a time.

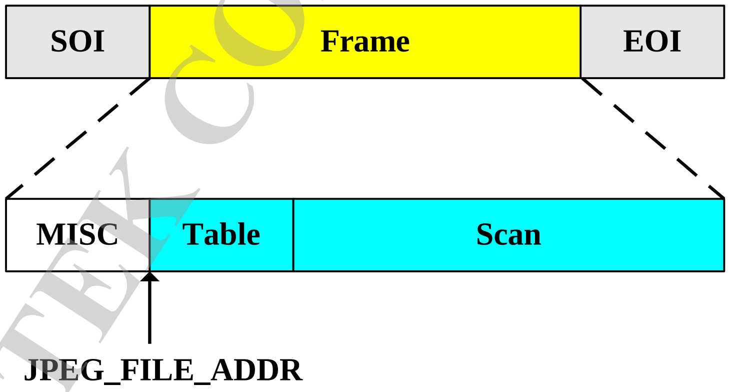

Figure 6-80. Basic structure of JPEG files

6.24.2 Features

The sleep controller receives commands from system software and controls the built-in power management unit to cut off the power supply of the external clock source. The power of external clock source can be resumed by several events predefined by users. These events are issued by:

- Baseline JPEG decoding (no progressive decoding, no restart marker decoding, bypassed to software solution)
- Sampling format limitation: See Figure 6-81.
- Hardware table parsing (SW handles SOF parsing.)
- Supports file breakpoint
- 1/2/4/8 block resize (some limitation due to format conversion; see 6.24.2.3 “Block Resizing”)
- Supports MCU rows pause/resume

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- Error handling by bitstream overflow detection
  The supported input sampling format of JPEG decoder is illustrated in Figure 1-2

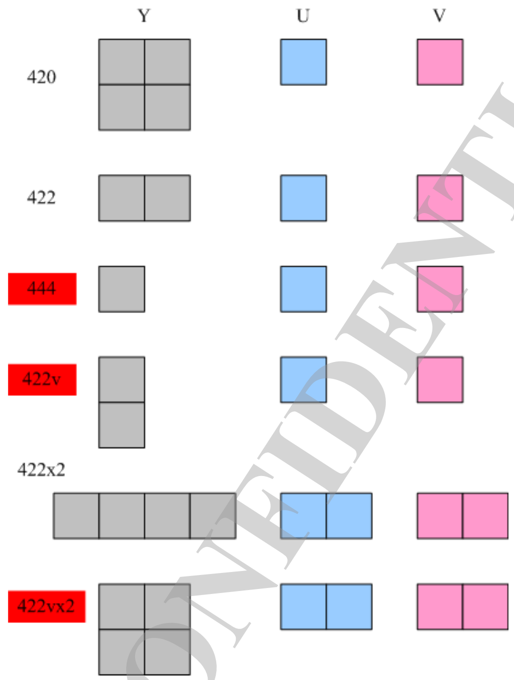

Figure 6-81. Supported sampling format of input JPEG file

For input sampling format that is not supported by the hardware, software solutions are adopted.

6.24.2.1 Software Reset Mechanism

To avoid unexpected memory access behavior, the soft reset scheme is also developed for JPEG decoder (same procedure as JPEG encoder). First, assert the soft reset bit in JPGDEC_RESET. Then hardware issues a done interrupt when its state is not busy. Software de-asserts the soft reset bit and clears the interrupt status. Finally, assert the hard reset bit in JPGDEC_RESET to do the reset process.

To reset JPEG decoder and GDMA in the direct couple mode, perform soft reset mechanism to JPEG decoder and reset JPEG decoder first. Then perform GDMA soft reset mechanism to reset GDMA.

6.24.2.2 Operation Modes

6.24.2.2.1 Normal Mode (Full Frame Mode)

In normal mode, JPEG decoder will output full frame to DRAM. Next, ISP/MDP takes over to resize and do image processing. For software usage, one set of frame buffer should be allocated to JPEG decoder and set up the corresponding configuration to trigger hardware for decoding. JPEG decoder will return interrupt when full frame is decoded.

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6.24.2.2.2 Pause/Resume Mode

In pause/resume mode, JPEG decoder outputs multiple MCU rows to DRAM based on software configuration and pause. JPEG decoder returns interrupt when the assigned MCU rows are decoded. The next configuration and trigger resume JPEG decoder, and the following MCU rows are outputted correspondingly. For software usage, one set of MCU rows buffer should be allocated to JPEG decoder. When JPEG decoder finishes the assigned MCU rows and pause, software should do the next configuration and trigger hardware until full frame is decoded. JPEG decoder will return interrupt when full frame is decoded.

6.24.2.3 Block Resizing

To save memory usage for JPEG image with extreme large size, block level resizing is supported by JPEG decoder. Simple 1/2, 1/4, 1/8 block level resize using 2-tap bilinear filter is adopted.

Since sampling format conversion is needed for JPEG decoder. Resize limitation exists for some source formats (e.g. for YUV444 input, only 1/4 resize can be performed).

		Config			
src format	dst format (3/1-plane)	Y_rsz	UV_h_rsz	UV_v_rsz	Limitation on real rsz
420	420	real_rsz	real_rsz	real_rsz	No
422	422	real_rsz	real_rsz	real_rsz	No
444	422	real_rsz	1+real_rsz	real_rsz	~ 1/4
422v	420	real_rsz	1+real_rsz	real_rsz	~ 1/4
422 x 2	422	real_rsz	real_rsz	real_rsz	No
422v x 2	420	real_rsz	1+real_rsz	real_rsz	~ 1/4

6.24.2.4 Error Handling Mechanism

Error handling is first performed in software header parsing stage. If the header is corrupted, software should not pass such file to hardware decoder. In hardware decoding stage, only part of error detection is supported (no error concealment capability). Several types of detection are supported, including invalid Huffman entry and block overflow. One flag will be raised when such error is detected and error interrupt will be issued. Hardware stops when 0xffd9 is encountered or the file size count is reached. If software is to stop JPEG decoder when error is detected, use the soft reset scheme.

6.24.3 DRAM Buffer Requirement

For JPEG decoder, two types of buffers should be allocated by software, bitstream buffer and decoded frame buffer.

The bitstream buffer is used to store the jpeg file bitstream. The start address should be 16-byte aligned, and the address position should be the first marker segment (such as DQT or DHT) after all

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the APP markers are skipped. The break point address can be set based on the limited memory size. The related control register is JPEG_FILE_ADDR and JPEG_FILE_BRP. The allocated bitstream buffer size should be multiple of 128 bytes.

The decoded frame buffer is separate 3-plane planar format and the supported color format is YUV422, YUV420 and grayscale Figure 6-82 is an example of the decoded frame buffer.

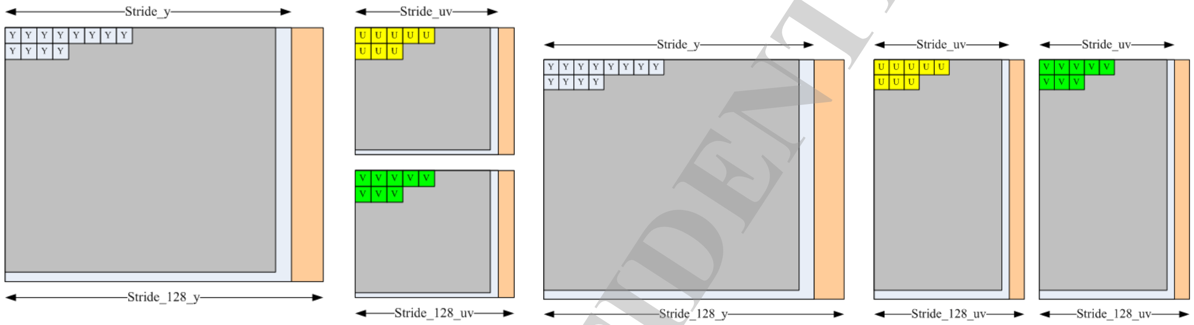

Figure 6-82. Memory footprint of source frame buffer

- Bitstream buffer
  - One buffer
  - Buffer size: Depends on available memory buffer
    - **Must be multiple of 128 bytes**
    - Loading as many as possible for better decoding performance is recommended.
    - Supports breakpoint feature
- Destination frame buffer
  - YUV422:
    - Three frame buffers
    - Buffer size
      - Y: [(width_y + 127)/128)]***128***[(height_y + 7)/8)]*8
      - U: [(width_u + 127)/128]***128***[(height_y + 7)/8]*8
      - V: [(width_v + 127)/128]***128***[(height_y + 7)/8)]*8
  - YUV420:
    - Three frame buffers
    - Buffer size
      - Y: [(width_y + 127)/128]***128***[(height_y + 15)/16]*16
      - U: [(width_u + 127)/128]***128***[(height_y + 7)/8]*8
      - V: [(width_v + 127)/128]***128***[(height_y + 7)/8]*8

6.24.4 Register Definition

Module name: jpgdec Base address: (+17004000h)

Address	Name	Width	Register Function
17004090	**JPGDEC_RESET**	32	JPEG Decoder Reset Register
170040F8	**JPGDEC_BRZ_F**	32	JPEG Decode Block Resize Factor

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Address	Name	Width	Register Function
	ACTOR		
170040FC	JPGDEC_DU_NUM	32	JPEG Decode DU Number for Each Component
1700412C	JPGDEC_DCT_DEBUG	32	JPEG Decoder Debug Register
17004130	JPGDEC_CHKSUM0	32	JPEG Decoder Checksum 0
17004134	JPGDEC_CHKSUM1	32	JPEG Decoder Checksum 1
17004140	JPGDEC_DEST_ADDR0_Y	32	JPEG Decode Y Base Address
17004144	JPGDEC_DEST_ADDR0_U	32	JPEG Decode U Base Address
17004148	JPGDEC_DEST_ADDR0_V	32	JPEG Decode V Base Address
1700414C	JPGDEC_DEST_ADDR1_Y	32	JPEG Decode Y Base Address
17004150	JPGDEC_DEST_ADDR1_U	32	JPEG Decode U Base Address
17004154	JPGDEC_DEST_ADDR1_V	32	JPEG Decode V Base Address
17004158	JPGDEC_STRIDE_Y	32	JPEG Decode Y Plane Memory Stride
1700415C	JPGDEC_STRIDE_UV	32	JPEG Decode U or V Plane Nemory Stride
17004160	JPGDEC_IMG_STRIDE_Y	32	JPEG Decode Y Plane Image Stride
17004164	JPGDEC_IMG_STRIDE_UV	32	JPEG Decode U or V Plane Image Stride
1700416C	JPGDEC_WDMA_CTRL	32	JPEG Decoder WDMA Control
17004170	JPGDEC_PAUSE_MCU_NUM	32	JPEG Decoder Pause MCU Index
1700417C	JPGDEC_OPERATION_MODE	32	JPEG Decoder Operation Mode
17004180	JPGDEC_DEBUG0	32	JPEG Decoder Debug Register
17004184	JPGDEC_DEBUG1	32	JPEG Decoder Debug Register
17004188	JPGDEC_DEBUG2	32	JPEG Decoder Debug Register
1700418C	JPGDEC_DEBUG3	32	JPEG Decoder Debug Register
17004200	JPGDEC_FILE_ADDR	32	JPEG Decoder File Address Register
1700420C	JPGDEC_COMP_ID	32	JPEG Decoder Component ID Register
17004210	JPGDEC_TOTAL_MCU_NUM	32	JPEG Decoder Total MCU Number Register
17004224	JPGDEC_COMP0_DATA_UNIT_NUM	32	JPEG Decoder Component 0's Data Unit Number Register
1700423C	JPGDEC_DU_CTRL	32	JPEG Decoder Control Register
17004240	JPGDEC_TRIG	32	JPEG Decoder Trigger Register

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Address	Name	Width	Register Function
17004248	JPGDEC_FILE_BRP	32	JPEG Decoder Breakpoint Address Register
1700424C	JPGDEC_FILE_TOTAL_SIZE	32	JPEG Decoder File Size Register
17004270	JPGDEC_QT_ID	32	JPEG Decoder Quantization Table ID Register
17004274	JPGDEC_INTERRUPT_STATUS	32	JPEG Decoder Interrupt Status Register
17004278	JPGDEC_STATUS	32	JPEG Decoder FSM Status Register
17004294	JPGDEC_MCU_CNT	32	JPEG VLD Decoded MCU Count Register
17004300	JPGDEC_DCM_CTRL	32	JPEG Decoder DCM Control Register
17004304	JPGDEC_SMI_DEBUG0	32	JPEG Decoder Debug Register
17004308	JPGDEC_SMI_DEBUG1	32	JPEG Decoder Debug Register
1700430C	JPGDEC_SMI_DEBUG2	32	JPEG Decoder Debug Register
17004310	JPGDEC_SMI_DEBUG3	32	JPEG Decoder Debug Register
17004318	JPGDEC_ULTRA_THRES	32	JPEG Decoder Ultra Threshold Control Register
1700431C	JPGDEC_IRQ_EN	32	JPEG Decoder IRQ Enable Control Register

17004090 JPGDEC_RESET JPEG Decoder Reset Register 00000010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RSTB				
Type												RW				
Reset												1				

Bit(s)	Name	Description
4	RSTB	**JPEG decoder's active-low reset (write only)** 0: Reset mode 1: Normal mode After the JPEG decoder is reset, the RSTB bit should be re-assigned to 1. *Note: Reset the JPEG decoder before decoding each new image.* *If it is required to reset the decoder during decoding, follow the soft reset mechanism. Hard reset may cause unexpected SMI behavior.*

170040F8 JPGDEC_BRZ_FACTOR JPEG Decode Block Resize Factor 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

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Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			BRZ_FACTOR_UV_V				BRZ_FACTOR_UV_H				BRZ_FACTOR_Y_V				BRZ_FACTOR_Y_H	
Type			RW				RW				RW				RW	
Reset			0	0			0	0			0	0			0	0

Bit(s)	Name	Description
13:12	BRZ_FACTOR_UV_V	**Vertical block resize factor for chroma** 2'b00: No resize 2'b01: 1/2 resize horizontally and vertically 2'b10: 1/4 resize horizontally and vertically 2'b11: 1/8 resize horizontally and vertically
9:8	BRZ_FACTOR_UV_H	**Horizontal block resize factor for chroma** 2'b00: No resize 2'b01: 1/2 resize horizontally and vertically 2'b10: 1/4 resize horizontally and vertically 2'b11: 1/8 resize horizontally and vertically
5:4	BRZ_FACTOR_Y_V	**Vertical block resize factor for luma** 2'b00: No resize 2'b01: 1/2 resize horizontally and vertically 2'b10: 1/4 resize horizontally and vertically 2'b11: 1/8 resize horizontally and vertically
1:0	BRZ_FACTOR_Y_H	**Horizontal block resize factor for luma** 2'b00: No resize 2'b01: 1/2 resize horizontally and vertically 2'b10: 1/4 resize horizontally and vertically 2'b11: 1/8 resize horizontally and vertically

170040FC **JPGDEC_DU_NUM** **JPEG Decode DU Number for Each Component** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					H_SAMP_0		V_SAMP_0		H_SAMP_1		V_SAMP_1		H_SAMP_2		V_SAMP_2	
Type					RW		RW		RW		RW		RW		RW	
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:10	H_SAMP_0	**Horizontal sampling factor of the 1st component, Y** 2'b00: Sampling factor = 1 2'b01: Sampling factor = 2 2'b10: Invalid 2'b11: Sampling factor = 4
9:8	V_SAMP_0	**Vertical sampling factor of the 1st component, Y.** 2'b00: Sampling factor = 1 2'b01: Sampling factor = 2 2'b10: Invalid 2'b11: Sampling factor = 4
7:6	H_SAMP_1	**Horizontal sampling factor of the 2nd component, U** 2'b00: Sampling factor = 1

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Bit(s)	Name	Description
		2'b01: Sampling factor = 2 2'b10: Invalid 2'b11: Sampling factor = 4
5:4	V_SAMP_1	**Vertical sampling factor of the 2nd component, U** 2'b00: Sampling factor = 1 2'b01: Sampling factor = 2 2'b10: Invalid 2'b11: Sampling factor = 4
3:2	H_SAMP_2	**Horizontal sampling factor of the 3rd component, V** 2'b00: Sampling factor = 1 2'b01: Sampling factor = 2 2'b10: Invalid 2'b11: Sampling factor = 4
1:0	V_SAMP_2	**Vertical sampling factor of the 3rd component, V** 2'b00: Sampling factor = 1 2'b01: Sampling factor = 2 2'b10: Invalid 2'b11: Sampling factor = 4

1700412C JPGDEC_DCT_DEBUG JPEG Decoder Debug Register 00000013

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																ERROR
Type																RO
Reset																0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name						STATUS0							STATUS1			
Type						RO							RO			
Reset						0	0	0	0	0	0	1	0	0	1	1

Bit(s)	Name	Description
16	ERROR	Indicates if there is VLD error
10:4	STATUS0	DCT core status
3:0	STATUS1	DCT buffer status

17004130 JPGDEC_CHKSUM0 JPEG Decoder Checksum 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKSUM[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CHKSUM[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CHKSUM	BSDMA checksum register

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17004134 **JPGDEC_CHKSUM1** **JPEG Decoder Checksum 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKSUM[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKSUM[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CHKSUM	WDMA checksum register

17004140 **JPGDEC_DEST_ADDR0_Y** **JPEG Decode Y Base Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEST_ADDR0_Y[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEST_ADDR0_Y[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEST_ADDR0_Y	**The first base address of Y component** Should be 16-byte aligned.

17004144 **JPGDEC_DEST_ADDR0_U** **JPEG Decode U Base Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEST_ADDR0_U[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEST_ADDR0_U[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEST_ADDR0_U	**The first base address of U component** Should be 16-byte aligned.

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17004148	JPGDEC_DEST_ADDR0_V	JPEG Decode V Base Address	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEST_ADDR0_V[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEST_ADDR0_V[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEST_ADDR0_V	**The first base address of V component** Should be 16-byte aligned.

1700414C	JPGDEC_DEST_ADDR1_Y	JPEG Decode Y Base Address	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEST_ADDR1_Y[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEST_ADDR1_Y[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEST_ADDR1_Y	**The second base address of Y component** Should be 16-byte aligned. Only used for JPGDEC/GDMA direct couple mode.

17004150	JPGDEC_DEST_ADDR1_U	JPEG Decode U Base Address	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEST_ADDR1_U[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEST_ADDR1_U[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEST_ADDR1_U	**The second base address of U component** Should be 16-byte aligned. Only used for JPGDEC/GDMA direct couple mode.

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17004154 JPGDEC_DEST_ADDR1_V JPEG Decode V Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEST_ADDR1_V[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEST_ADDR1_V[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEST_ADDR1_V	**The second base address of V component** Should be 16-byte aligned. Only used for JPGDEC/GDMA direct couple mode.

17004158 JPGDEC_STRIDE_Y JPEG Decode Y Plane Memory Stride 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				STRIDE_Y												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	STRIDE_Y	**Memory stride of Y component** Should be 16-byte aligned. Larger than Image_stride_Y = (image_width_Y+15)/16*16. *Note: Only useful in GDMA direct couple mode. Must set to be equal to image stride in other modes.*

1700415C JPGDEC_STRIDE_UV JPEG Decode U or V Plane Nemory Stride 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				STRIDE_UV												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	STRIDE_UV	**Memory stride of U and V component** Should be 16-byte aligned. Larger than Image_stride_UV = (image_width_UV+15)/16*16.

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Bit(s)	Name	Description
		Note: Only useful in GDMA direct couple mode. Must set to be equal to image stride in other modes.

17004160 **JPGDEC_IMG_STRIDE_Y** **JPEG Decode Y Plane Image Stride** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				IMG_STRIDE_Y												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	IMG_STRIDE_Y	**Image stride of Y component** Should be 16-bytes aligned. Image_stride_Y = (image_width_Y+15)/16 * 16.

17004164 **JPGDEC_IMG_STRIDE_UV** **JPEG Decode U or V Plane Image Stride** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				IMG_STRIDE_UV												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	IMG_STRIDE_UV	**Image stride of U and V component** Should be 16-bytes aligned. Image_stride_UV = (image_width_UV+15)/16 * 16.

1700416C **JPGDEC_WDMA_CTRL** **JPEG Decoder WDMA Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									NUM_MCU_PER_GROUP							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		NUM_GROUP_MCU							NUM_MCU_LAST_GROUP							
Type		RW							RW							
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
23:16	NUM_MCU_PER_GROUP	**Sets up the number of MCU in each MCU group except for that of last MCU group for write DMA control** NUM_MCU_PER_GROUP = 128/(Y pixel width in one MCU) -1 The Y pixel number in one MCU corresponds to that after format conversion and resizing.
14:8	NUM_GROUP_MCU	**Sets up the number of MCU group for write DMA control.** NUM_GROUP_MCU = (number of MCU per MCU row + number of MCU per MCU group -1/number of MCU per MCU group) -1
7:0	NUM_MCU_LAST_GROUP	**Sets up the number of MCU in last MCU group for write DMA control** NUM_MCU_LAST_GROUP = (Y pixel width in last MCU group)/(Y pixel width in one MCU) - 1. Here the Y pixel number in one MCU corresponds to that after format conversion and resizing.

17004170 **JPGDEC_PAUSE_MCU_NUM** **JPEG Decoder Pause MCU Index** **03FFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							**PAUSE_MCU_NUM[25:16]**									
Type							RW									
Reset							1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**PAUSE_MCU_NUM[15:0]**															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
25:0	PAUSE_MCU_NUM	**Sets up pause MCU index for pause/resume mode** If stop MCU index is N in this pause/resume interaction, set this value to N-1, and N must be the MCU index of MCU row end.

1700417C **JPGDEC_OPERATION_MODE** **JPEG Decoder Operation Mode** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**ULTRA_CTRL**											**ERR_DET_DISABLE**
Type					RW											RW
Reset					0	0	0	0								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**RST_INVALID_SKIP**							**OP_MODE**	
Type								RW							RW	
Reset								0							0	0

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Bit(s)	Name	Description
27:24	ULTRA_CTRL	**Controls JPEG SMI port ultra option enabling** Set to 1 to enable corresponding option. bit[27]: WDMA GULTRA bit[26]: WDMA GPREULTRA bit]25]: BSDMA GULTRA bit[24]: BSDMA GPREULTRA
16	ERR_DET_DISABLE	**Disables error detection feature** Set to 0 to disable error detection.
8	RST_INVALID_SKIP	**Skip invalid restart marker detection** Set to 1 to skip invalid restart marker detection if necessary.
1:0	OP_MODE	**Sets up JPEG decoder operation mode** 2'b00: Normal mode (full frame mode) 2'b01: Direct couple mode 2'b10: Pause/resume mode 2'b11: Reserved

17004180 JPGDEC_DEBUG0 JPEG Decoder Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				JPGDEC_READY0				JPGDEC_READY1				GDMA_BUSY0				GDMA_BUSY1
Type				RO				RO				RO				RO
Reset				0				0				0				0

Bit(s)	Name	Description
12	JPGDEC_READY0	Debugging information for direct couple mode
8	JPGDEC_READY1	Debugging information for direct couple mode
4	GDMA_BUSY0	Debugging information for direct couple mode
0	GDMA_BUSY1	Debugging information for direct couple mode

17004184 JPGDEC_DEBUG1 JPEG Decoder Debug Register 00000080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GWRSP_CNT_INT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name			GWRSP_CNT_INT_OVERFLOW		WDMA_DEBUG				WDMA_BUFFER_STATE				WDMA_MAIN_STATE			
Type			RO		RO				RO				RO			
Reset			0	0	0	0	0	0	1	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:16	GWRSP_CNT_INT	JPEG decoder debugging information
13:12	GWRSP_CNT_INT_OVERFLOW	JPEG decoder debugging information
11:8	WDMA_DEBUG	JPEG decoder debugging information
7:4	WDMA_BUFFER_STATE	JPEG decoder debugging information
3:0	WDMA_MAIN_STATE	JPEG decoder debugging information

17004188 **JPGDEC_DEBUG2** **JPEG Decoder Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GWRSP_CNT_SMI[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GWRSP_CNT_SMI[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	GWRSP_CNT_SMI	JPEG decoder debugging information

1700418C **JPGDEC_DEBUG3** **JPEG Decoder Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				EARLY_EOI				INVALID_RST				INVALID_CODE				BLK_OVERFLOW
Type				RO				RO				RO				RO
Reset				0				0				0				0

Bit(s)	Name	Description
12	EARLY_EOI	Debugging information for error detection
8	INVALID_RST	Debugging information for error detection
4	INVALID_CODE	Debugging information for error detection
0	BLK_OVERFLOW	Debugging information for error detection

17004200 **JPGDEC_FILE_ADDR** **JPEG Decoder File Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	FILE_ADDR[27:12]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FILE_ADDR[11:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	FILE_ADDR	**JPEG file starting address** This address must be 16-byte aligned. This register's content will be changed by hardware if JPEG decoder is started. The contents represent the address read. It is suggested the starting address be set to the location of DQT marker (0xffdb) at the beginning of decoding one JPEG file. Some dummy data (0xff) can be inserted before the JPEG file to help meet the limitation of 16-byte alignment. When enabling the function of breakpoint, one JPEG file can be divided into several sections and loaded to the memory for decoding individually. In every end of a section, the software needs to re-program this file address to the start address of the next file section. Any dummy data are not allowed to be inserted in the file content. *Note: Due to DCM implementation, this register can be read only if DCM is disabled.*

1700420C **JPGDEC_COMP_ID** **JPEG Decoder Component ID Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COMP0_ID								COMP1_ID							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMP2_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Name	Description
31:24	COMP0_ID	**1st component (Y) ID extracted from SOF marker** *Note: This register should be written before read; otherwise, the return value will be meaningless.*
23:16	COMP1_ID	**2nd component (U) ID extracted from SOF marker** *Note: This register should be written before read; otherwise, the return value will be meaningless.*
15:8	COMP2_ID	**3rd component (V) ID extracted from SOF marker** *Note: This register should be written before read; otherwise, the return value will be meaningless.*

17004210 **JPGDEC_TOTAL_MCU_NUM** **JPEG Decoder Total MCU Number Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TOTAL_MCU_NUM[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	TOTAL_MCU_NUM[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TOTAL_MCU_NUM	**Total MCU number to be decoded** If the MCU number is N, program (N-1) into this register. *Note: This register should be written before read; otherwise, the return value will be meaningless.*

17004224 JPGDEC_COMP0_DATA_UNIT_NUM JPEG Decoder Component 0's Data Unit Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COMP0_DATA_UNIT_NUM[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMP0_DATA_UNIT_NUM[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	COMP0_DATA_UNIT_NUM	**Component 0 data unit count** Only effective in grayscale mode. Contains the 8x8 data unit number of the first component in non-interleaved scans. If the data unit number is N, program (N-1) into this register. *Note: This register MUST be written before read; otherwise, the return value will be meaningless*

1700423C JPGDEC_DU_CTRL JPEG Decoder Control Register 3FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GRAY	GMC_EN	DU_9			DU_8			DU_7			DU_6			DU_5[2:1]	
Type	RW	RW	RW			RW			RW			RW			RW	
Reset	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DU_5[0:0]	DU_4			DU_3			DU_2			DU_1			DU_0		
Type	RW	RW			RW			RW			RW			RW		
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31	GRAY	**Grayscale mode indicator** 0: Not grayscale 1: Grayscale
30	GMC_EN	**Enables signal for GMC activity** Should be set to 1 before trigger JPEG decoder 0: Disable

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Bit(s)	Name	Description
		1: Enable *Note: Due to DCM implementation, this register can be read only if DCM is disabled.*
29:27	DU_9	**10th data unit component category in a MCU** 3'b100: Data unit is Y component 3'b101: Data unit is U component 3'b110: Data unit is V component 3'b111: Not used in current frame Other: Invalid *Note: Due to DCM implementation, this register can be read only when DCM is disabled.*
26:24	DU_8	**9th data unit component category in a MCU** 3'b100: Data unit is Y component 3'b101: Data unit is U component 3'b110: Data unit is V component 3'b111: Not used in current frame other: Invalid *Note: Due to DCM implementation, this register can be read only when DCM is disabled.*
23:21	DU_7	**8th data unit component category in a MCU** 3'b100: Data unit is Y component 3'b101: Data unit is U component 3'b110: Data unit is V component 3'b111: Not used in current frame Other: Invalid *Note: Due to DCM implementation, this register can be read only when DCM is disabled.*
20:18	DU_6	**7th data unit component category in a MCU** 3'b100: Data unit is Y component 3'b101: Data unit is U component 3'b110: Data unit is V component 3'b111: Not used in current frame Other: Invalid *Note: Due to DCM implementation, this register can be read only when DCM is disabled.*
17:15	DU_5	**6th data unit component category in a MCU** 3'b100: Data unit is Y component 3'b101: Data unit is U component 3'b110: Data unit is V component 3'b111: Not used in current frame Other: Invalid *Note: Due to DCM implementation, this register can be read only when DCM is disabled.*
14:12	DU_4	**5th data unit component category in a MCU** 3'b100: Data unit is Y component 3'b101: Data unit is U component 3'b110: Data unit is V component 3'b111: Not used in current frame Other: Invalid *Note: Due to DCM implementation, this register can be read only when DCM is disabled.*
11:9	DU_3	**4th data unit component category in a MCU** 3'b100: Data unit is Y component 3'b101: Data unit is U component 3'b110: Data unit is V component 3'b111: Not used in current frame Other: Invalid *Note: Due to DCM implementation, this register can be read only when DCM is disabled.*

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Bit(s)	Name	Description
8:6	DU_2	**3rd data unit component category in a MCU** 3'b100: Data unit is Y component 3'b101: Data unit is U component 3'b110: Data unit is V component 3'b111: Not used in current frame Other: Invalid *Note: Due to DCM implementation, this register can be read only when DCM is disabled.*
5:3	DU_1	**2nd data unit component category in a MCU** 3'b100: Data unit is Y component 3'b101: Data unit is U component 3'b110: Data unit is V component 3'b111: Not used in current frame Other: Invalid *Note: Due to DCM implementation, this register can be read only when DCM is disabled.*
2:0	DU_0	**1st data unit component category in a MCU** 3'b100: Data unit is Y component 3'b101: Data unit is U component 3'b110: Data unit is V component 3'b111: Not used in current frame Other: Invalid *Note: Due to DCM implementation, this register can be read only when DCM is disabled.*

17004240 JPGDEC_TRIG JPEG Decoder Trigger Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TRIG
Type																WO
Reset																0

Bit(s)	Name	Description
0	TRIG	Write to start JPEG decoder.

17004248 JPGDEC_FILE_BRP JPEG Decoder Breakpoint Address Register FFFFFFFC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	JPEG_FILE_BRP_ADDR[29:14]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	JPEG_FILE_BRP_ADDR[13:0]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1		

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:2	JPEG_FILE_BRP_ADDR	**JPGDEC_FILE_BRP stands for 16-byte aligned breakpoint address that hardware will stall once the breakpoint address is encountered.** The data in the current breakpoint address will not be parsed for decoding. This control register provides a solution for software to swap internal memory content with the external memory in case the JPEG source file is too big for the internal memory to store at a time. A breakpoint interrupt will be fired when the hardware DMA address hits the breakpoint address. The software can refill the residue bitstream and follow the procedure below to restart the JPEG decoder. 1. Write new breakpoint address to JPGDEC_FILE_BRP register. 2. Write new destination address to JPEG_DEC_FILE_ADDR register. 3. Write JPG_DEC_TRIG register to trigger the decoder.

1700424C	**JPGDEC_FILE_TOTAL_SIZE**	**JPEG Decoder File Size Register**	**FFFFFFFC**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**JPEG_FILE_TOTAL_SIZE[29:14]**															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**JPEG_FILE_TOTAL_SIZE[13:0]**															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1		

Bit(s)	Name	Description
31:2	JPEG_FILE_TOTAL_SIZE	**Size slightly larger than the JPEG source file size in bytes for error file detection** The hardware will fire a file overflow interrupt and stall if this size of bitstream has been read in. *Note: The total size of file must be a multiple of 128 (including initial dummy data). If the total size is not divisible by 128, increase the size value until it is.*

17004270	**JPGDEC_QT_ID**	**JPEG Decoder Quantization Table ID Register**	**00000011**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**COMP0_QT_ID**				**COMP1_QT_ID**				**COMP2_QT_ID**			
Type					RW				RW				RW			
Reset					0	0	0	0	0	0	0	1	0	0	0	1

Bit(s)	Name	Description
11:8	COMP0_QT_ID	Quantization table ID of Y component directly extracted from SOF marker
7:4	COMP1_QT_ID	Quantization table ID of U component directly extracted from SOF marker
3:0	COMP2_QT_ID	Quantization table ID of V component directly extracted from SOF marker

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17004274	JPGDEC_INTERRUPT_STATUS	JPEG Decoder Interrupt Status Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ_TYPE															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											ERR_IRQ	PAUSE_IRQ		OVFL_IRQ	BRP_IRQ	EOF_IRQ
Type											RW	RW		RW	RW	RW
Reset											0	0		0	0	0

Bit(s)	Name	Description
31	IRQ_TYPE	**IRQ type** 0: Write-clear mode 1: Read-clear mode (If read-clear mode is enabled, this bit should always be set to 1.)
5	ERR_IRQ	**Set to 1 by error interrupt; write 1 to clear interrupt signal (write-clear mode).**
4	PAUSE_IRQ	**Set to 1 by pause interrupt; write 1 to clear interrupt signal (write-clear mode).**
2	OVFL_IRQ	**Set to 1 by file overflow interrupt; write 1 to clear interrupt signal (write-clear mode).**
1	BRP_IRQ	**Set to 1 by breakpoint interrupt; write 1 to clear interrupt signal (write-clear mode).**
0	EOF_IRQ	**Set to 1 by end of file interrupt; write 1 to clear interrupt signal (write-clear mode).**

17004278	JPGDEC_STATUS	JPEG Decoder FSM Status Register	88011000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GREQ_EN	FOS	BRPS	EOFS	GMC_IDLE	JPEG_DEC_STATE			HUFF_DEC_STATE					MARKER_PARSER_STATE		
Type	RO	RO	RO	RO	RO	RO			RO					RO		
Reset	1	0	0	0	1	0	0	0	0	0	0	0		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SOS_PARSER_STATE						DHT_PARSER_STATE				DQT_PARSER_STATE		DATA_UNIT_STATE			
Type	RO						RO				RO		RO			
Reset	0	0	0	1			0	0			0	0	0	0	0	0

Bit(s)	Name	Description
31	GREQ_EN	**Indicator for greq port**
30	FOS	**Set to 1 in overflow condition**
29	BRPS	**Set to 1 in breakpoint condition**
28	EOFS	**Set to 1 in EOI condition**
27	GMC_IDLE	**Status of GMC port for JPEG decoder**

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Bit(s)	Name	Description
		0: Active 1: Idle
26:24	JPEG_DEC_STATE	**State of JPEG decoder** 0: IDLE 1: DMA_LOAD 2: MARKER_PARSER 3: HUFFMAN_DECODE 4: RST_SRCH 5: RELOAD_PROGR_COEFF 6: WAIT_FOR_IDCT
23:20	HUFF_DEC_STATE	**State of huffman decoding** 0: IDLE 1: RELOAD_SCAN_START_ADDR 2: RELOAD_EOB_RUN 3: BYPASS_DATA 4: RELOAD_CTRL 5: READ_COEFF 6: HUFF_ADDR_LOGICAL 7: HUFF_ADDR_PHYSICAL 8: EOB_RUN_GEN 9: AMP_CAL A: WAIT_COEFF B: SAVE_SCAN_START_ADDR C: SAVE_EOB_RUN D: SAVE_CTRL E: WAIT_FOR_IDCT
18:16	MARKER_PARSER_STATE	**State of marker parser** 1: SRCH_0xFF 2: MARKER_TYPE_IDEN 3: MARKER_LEN_HIGH 4: MARKER_LEN_LOW 5: MARKER_MISC_INFO_DEC
15:12	SOS_PARSER_STATE	**State of SOS parser** 1: NS 2: COMP_SPEC 3: SS_FIELD 4: SE_FIELD 5: AH_AL_FIELD
9:8	DHT_PARSER_STATE	**State of DHT parser** 0: TC_TH 1:HUFF_SYM_LENGTH 2: HUFF_VAL_COLLECT 3: WRITE_HUFF_VAL
5:4	DQT_PARSER_STATE	**State of DQT parser** 0: PQ_TQ 1: READ_COEFF 2: PROGR_COEFF 3: WRITE_COEFF
3:0	DATA_UNIT_STATE	**State of process data unit** 0: DU0 1: DU1 2: DU2 3: DU3 4: DU4 5: DU5 6: DU6 7: DU7 8: DU8 9: DU9

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17004294 **JPGDEC_MCU_CNT** **JPEG VLD Decoded MCU Count Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												MCU_CNT[20:16]				
Type												RO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MCU_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	MCU_CNT	MCU counts decoded by VLD

17004300 **JPGDEC_DCM_CTRL** **JPEG Decoder DCM Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																STATUS
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DISABLE
Type																RW
Reset																0

Bit(s)	Name	Description
16	STATUS	0: JPGDEC clock is off. 1: JPGDEC clock is on.
0	DISABLE	0: Enable JPGDEC DCM (default) 1: Disable JPGDEC DCM

17004304 **JPGDEC_SMI_DEBUG0** **JPEG Decoder Debug Register** **10000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG0[31:16]															
Type	RO															
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG0[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG0	JPEG decoder debugging information

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17004308 **JPGDEC_SMI_DEBUG1** **JPEG Decoder Debug Register** **10000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG1[31:16]															
Type	RO															
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG1[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG1	JPEG decoder debugging information

1700430C **JPGDEC_SMI_DEBUG2** **JPEG Decoder Debug Register** **02300000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG2[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG2[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG2	JPEG decoder debugging information

17004310 **JPGDEC_SMI_DEBUG3** **JPEG Decoder Debug Register** **00040000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG3[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG3[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG3	JPEG decoder debugging information

17004318 **JPGDEC_ULTRA_THRES** **JPEG Decoder Ultra Threshold Control Register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_ULTRA_THRES								WDMA_PREULTRA_THRES							
Type	RW								RW							

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Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSDMA_ULTRA_THRES								BSDMA_PREULTRA_THRES							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	WDMA_ULTRA_THRES	**Sets up WDMA gultra threshold** Useful if the corresponding ultra enabling bit is set.
23:16	WDMA_PREULTRA_THRES	**Sets up WDMA gpreultra threshold** Useful if the corresponding preultra enabling bit is set.
15:8	BSDMA_ULTRA_THRES	**Sets up BSDMA gultra threshold** Useful if the corresponding ultra enabling bit is set.
7:0	BSDMA_PREULTRA_THRES	**Sets up BSDMA gpreultra threshold** Useful if the corresponding preultra enabling bit is set.

1700431C **JPGDEC_IRQ_EN** **JPEG Decoder IRQ Enable Control Register** **0000003F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CMDQ_EN															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											IRQ_INT_EN					
Type											RW					
Reset											1	1	1	1	1	1

Bit(s)	Name	Description
31	CMDQ_EN	**Set to 0 to disable command queue frame done**
5:0	IRQ_INT_EN	**Enables IRQ** bit[5]: Enable error detection interrupt bit[4]: Enable decoding paused interrupt bit[2]: Enable overflow interrupt bit[1]: Enable break point interrupt bit[0]: Enable EOF interrupt *Note: When command queue is not used, set all IRQ enable to 1. When command queue is used, set error detection/overflow/breakpoint to 1 and others to 0.*

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6.25 Video Decoder

6.25.1 Introduction

MediaTek Video Decoder (VDEC) in project MT6735 supports multi-standard video compression format, which greatly reduces the CPU loading and achieves high performance video decompression.

The video standard supported by VDEC includes:

- MPEG1/2
- H.264 CBP/MP/HP
- MPEG4 ASP
- DIVX3/DIVX4/DIVX5/DIVX6/DIVX HD/XVID
- Sorenson H.263, H.263
- De-Blocking Filter for MPEG2, H.263
- H.264 decoder Constraint Baseline Profile/Main/High Profile

VDEC supports full-HD 30fps under the limitation of picture size > full-HD, (i.e. does not support picture width > 1920 or picture height > 1088).

6.25.2 Block Diagram

The architecture and core blocks of VDEC are shown in Figure 6-83, including the following parts: Entropy Decoder, IS/IQ/IT, MV Calculation, Intra Prediction, Motion Compensation and De-blocking Filter. The input to VDEC is a compressed video bitstream. After the decoding process, the reconstructed video will be sent to the display stage.

6.25.2.1 Interface

The interface of VDEC is shown in Figure 6-84. Related modules include SMI interface, APB interface and handshaking bus between VDEC and CDP. The output format supported by VDEC is:

- NV12_BLK (Video block mode), 420 format block mode, 2 plane (UV)
- NV12_BLK_FCM (Video field compact mode), 420 format block mode, 2 plane (UV)

VDEC use DRAM as bitstream input, working buffer, reference buffer and output, and DRAM access process is achieved by using SMI interface. 7 sets of SMI interface with 128 bits read/write are used including MC/PP/PP_WRAP/AVC_MV/PRED_RD/PRED_WR/VLD. In addition, all ports are EMI ports, i.e. no SYSRAM required.

Register settings are passed to VDEC by APB interface. There are 1 set of APB interface.

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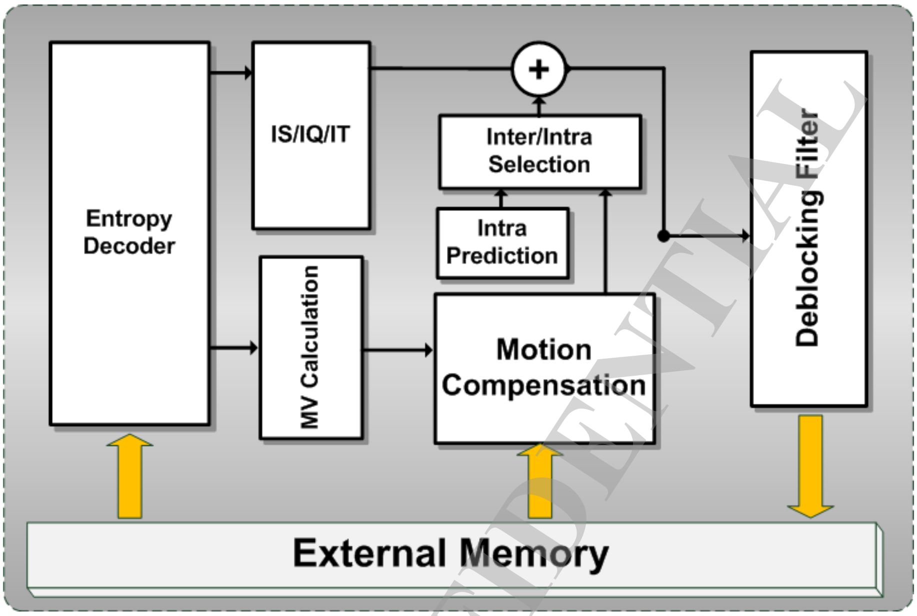

Figure 6-83. Block diagram of video decoder

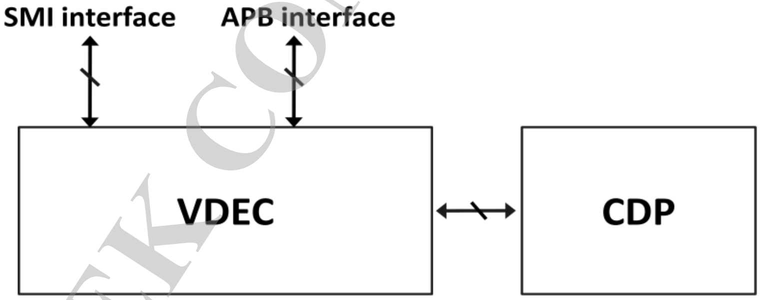

Figure 6-84. Interface of VDEC

6.25.3 Programming Guide

This section defines the recommended programming procedure for using VDEC to perform video decompression correctly. Moreover, this section also introduces common functions and settings, that is, these functions do not change under different video coding standards.

6.25.3.1 Base Settings

This section describes useful settings before programming VDEC, including clocks and base address of VDEC.

6.25.3.1.1 Clocks

Two clocks are required for VDEC.

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- smi_clk: 300MHz
- vdec_clk: 273MHz

For more details, see the CKGEN register map.

6.25.3.1.2 VDEC Register Base Address

Base address of each sub-module is described in Table 6-29.

Table 6-29. VDEC base address

CS	BASE (hex)	HW cs	comment
VDEC_MISC	0x16020000	cs_vdec_dv	Legacy naming is DV_BASE
VLD	0x16021000	cs_vdec_vld	
VLD_TOP	0x16021800	cs_vdec_vld	Partial bank of VLD_BASE, i.e. (VLD | 0x800)
MC	0x16022000	cs_vdec_mc	
AVC_VLD	0x16023000	cs_avc_vld	
AVC_MV	0x16024000	cs_avc_mv	
PP	0x16025000	cs_vdec_pp	
VDEC_GCON	0x16000000		VDEC global control registers
SMI_LARB1	0x16010000		SMI Larb1 control registers

6.25.3.2 VDEC Hardware Architecture

Figure 6-85 is the hardware architecture; Figure 6-86 is the detail architecture of VLD. It is essential to know the architecture of VLD because most common settings are related to this module.

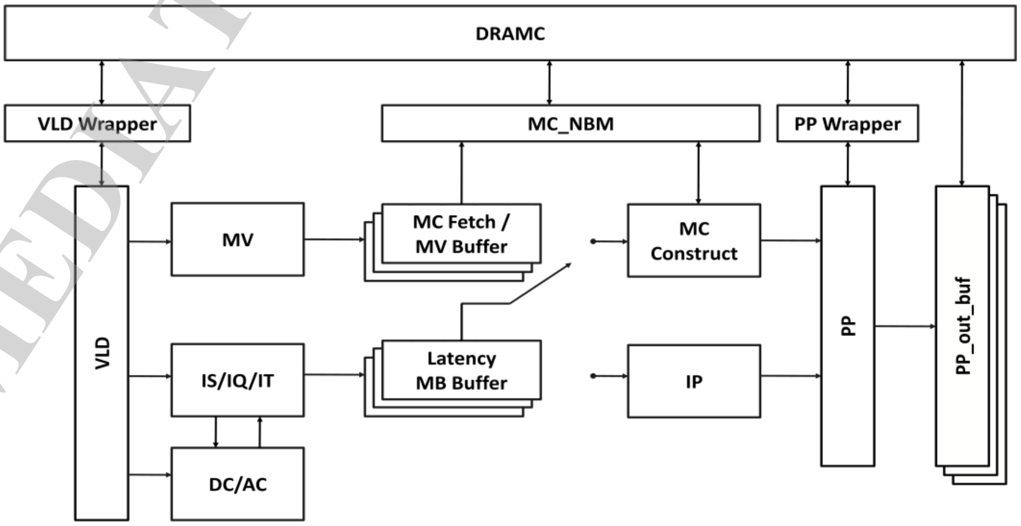

Figure 6-85. VDEC hardware architecture

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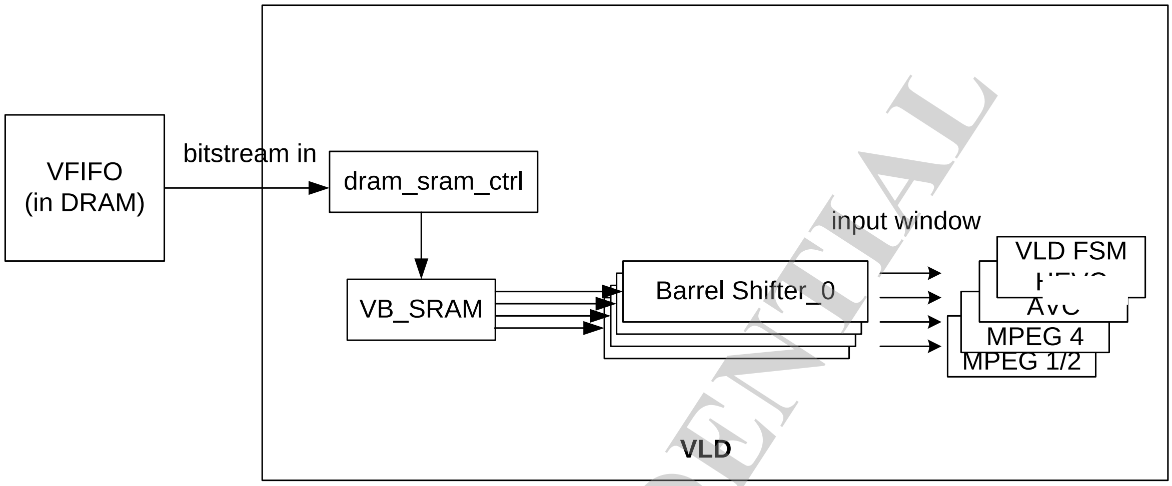

Figure 6-86. VLD hardware architecture

6.25.3.3 Firmware Hardware Partition

Figure 6-87 shows a typical decoding flow with FW/HW partition. SW takes charge of the frame level setting, including syntax decoded from frame header and proper DRAM buffer allocation, and triggers HW to decode the bitstream. An interrupt signal will be sent to CPU when HW finishes decoding a frame and FW can reset HW and program settings for the next frame if necessary. Details of FW decoding are described in section 6.25.3.4.

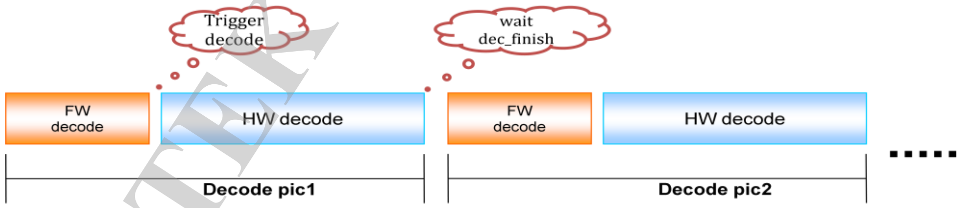

Figure 6-87. VDEC decoding flow

6.25.3.4 FW Decoding Flow

This section describes our recommended step-by-step FW setup flow. Each step should be followed to ensure a correct decoding process.

1. Soft reset
   a. Issue reset vld_reg_66[0] = 1.
   b. Turn on VDEC related clocks.
   c. Release soft reset vld_reg_66[0] = 0.
2. Initial Bitstream DMAs and Barrel-Shifters.
3. Decode frame layer syntax.
4. Maintain DPB buffer.

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5. HW registers setting
    a. SQT setting
    b. MV setting
    c. MC setting
    d. De-blocking (PP) setting
    e. VLD setting
6. Trigger HW decoding.
7. Wait for decoding picture to finish via VDEC interrupt (HW auto turns off VDEC related clocks).

6.25.3.4.1 Software Reset and Power Control Flow

Figure 6-88 is the software reset and power control flow. Details of each step are described in the following sections.

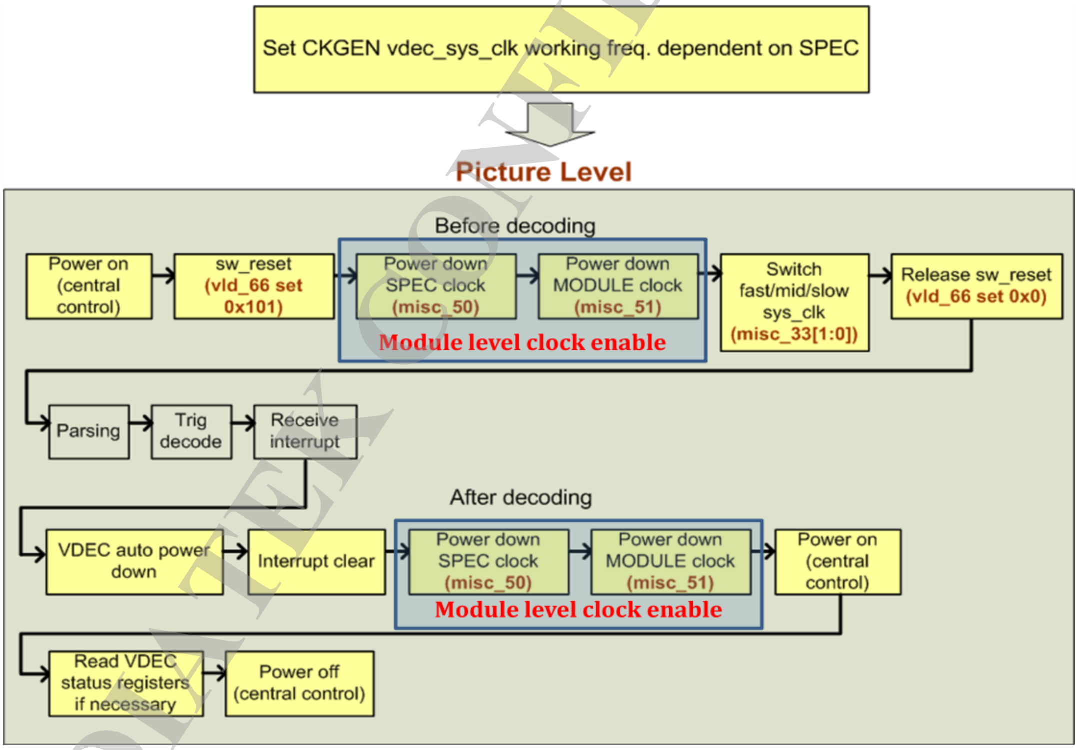

Figure 6-88. Software reset and power control

- ✓ Power on (central control)
    - Set VDEC_GCON reg 0 bit[0] (vdec subsys clock enable) = 1.
    - Enable global clocks of VDEC (DRAM clock, vdec_sys clock, bus clock).
- ✓ VDEC auto power-down
    - Auto turn off DRAM clock, vdec_sys clock.
    - Auto set pdn_con_spec (vdec_misc_reg 50) = 32'hffffffff.
    - Auto set pdn_con_module (vdec_misc_reg 51) = 32'hffffffff.
- ✓ Interrupt clear
    - No interrupt clear from CPU

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- Use internal VDEC RISC clear int
  - VDEC_MISC reg 41
    - Bit [0] (risc_clr_int_mode) always set to 1
    - Bit [4] (risc_int_clr): Internal VDEC RISC clear int

✓ Power off (central control)
  - Set VDEC_GCON reg 0 bit[0] (vdec subsys clock enable) = 0

6.25.3.4.2 Turn off VDEC Auto Power Down

FW can turn off VDEC auto power down by disabling the setting of "auto turn off dram clk, vdec sys clock" and disabling "Auto set pdn_con_spec = 32'hffffffff & Auto set pdn_con_module = 32'hffffffff".

Related register settings are:

- Disable "Auto turn off dram clock, vdec_sys clock"
  - Set VDEC_GCON reg 6 bit[0] = 1
- Disable "Auto set pdn_con_spec = 32'hffffffff & Auto set pdn_con_module = 32'hffffffff"
  - Set VDEC_MISC reg 59 bit[0] = 1

The decoding process will change after FW turns off VDEC auto power-down control. The difference is shown Figure 6-89.

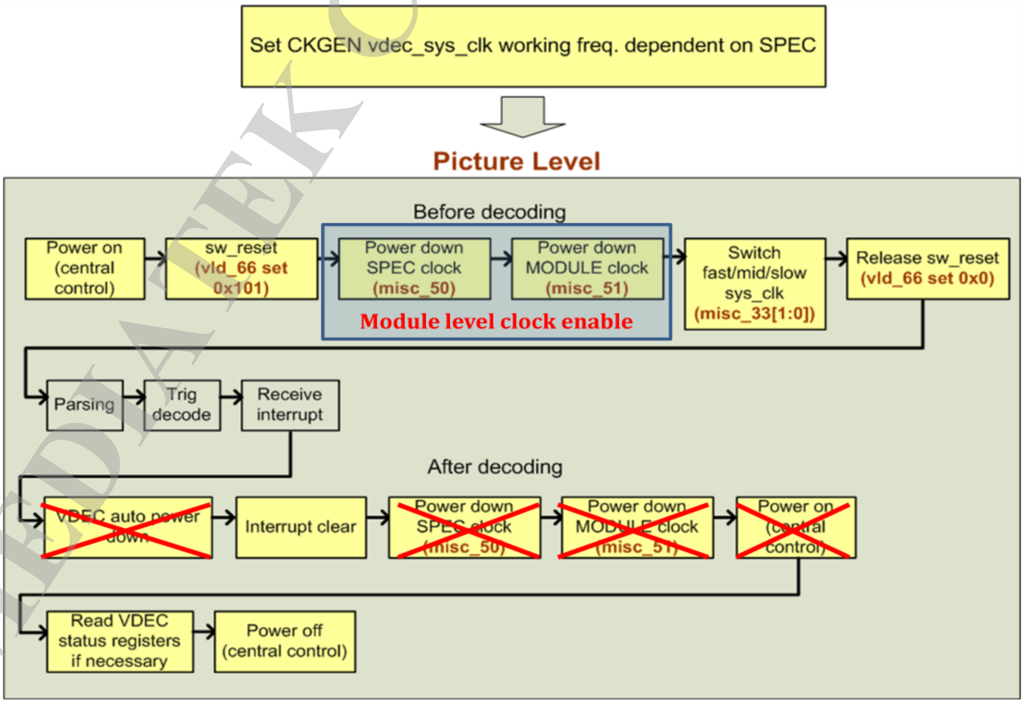

Figure 6-89. Software reset and power control (turn off VDEC auto power down)

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6.25.3.4.3 Other Relative Registers for Power Control

FW can disable "Auto turn off dram clock, vdec_sys clock" when dec_error occurs by setting VDEC_GCON reg 6 bit[4] = 1.In addition, when dec_error occurs, there is **always no** "Auto set pdn_con_spec = 32'hffffffff & Auto set pdn_con_module = 32'hffffffff".

6.25.3.4.4 Clock and Power Down Setting

a. Enable global clocks of VDEC (DRAM clock, vdec_sys clock, bus clock).
   i. Set VDEC_GCON reg 0 bit[0] (vdec subsys clock enable) = 1.
b. Enable SRAMs of SMI/VDEC.
   i. ***SLEEP_IFR_PWR_CON = (***SLEEP_IFR_PWR_CON&0xffff00ff);
   ii. ***SLEEP_VDE_PWR_CON = (***SLEEP_IFR_PWR_CON&0xffff00ff);
c. Set up clock gating for each standard and modules.
   i. Software reset: Set VLD reg 66 = 0x101.
   ii. Set up **pdn_con_spec** & **pdn_con_module** setting for different specs.
      1. **pdn_con_spec (VDEC_MISC reg 50 (0xC8))**
         A) **pdn_con_module (VDEC_MISC reg 51 (0xCC))**
   iii. Set up vdec_sys_clk_sel for different specs:
      1. **vdec_sys_clk_sel (VDEC_MISC reg 33(0x84))**
   iv. Release software reset: reset VLD reg 66 = 0x0

VDEC system clock frequent, as well as Module level power down control, depend on different specs. Details are described in Table 6-30.

Table 6-30. Power down control and clock selection

SPEC	VDEC_MISC reg 50 (0xC8) pdn_con_spec (set 1: turn off clock)	VDEC_MISC reg 51 (0xCC) pdn_con_module (set 1: turn off clock)	VDEC_MISC reg 33(0x84) vdec_sys_clk_sel (0 = Slow; 1 = Mid; 2 = Fast)
MPEG1_2	0x1FE	0x7F6A_15FD (w/o DBK) 0x7F6A_151D (w DBK)	0x1 (mid)
MPEG4	0x1FD	0x7F6A_11E8 (w/o DBK) 0x7F6A_1108 (w DBK)	0x1 (mid)
H.264/MVC	0x1F7	0x53E2_0180	0x2 (fast)

6.25.3.4.5 Interrupt Clear

In MT6735, there is no interrupt clear from CPU, i.e. interrupt clear should be achieved by FW setting up internal VDEC RISC. To perform interrupt clear, set up the following:

VDEC_MISC reg 41
- Bit [0] (risc_clr_int_mode) always set to 1
- Bit [4] (risc_int_clr): Internal VDEC RISC clear int

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6.25.3.5 Initial Bitstream DMAs and Barrel-Shifters

Before triggering HW VDEC to decode a picture, load bitstream from DRAM to VDEC internal memory and set up correct read location of bitstream. These steps are known as the initial fetch and initial barrel-shifters. The concept is described in Figure 6-90, and the flow chart is in Figure 6-91.

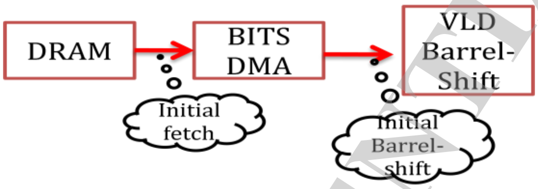

Figure 6-90. Initial fetch and initial Barrel-shift

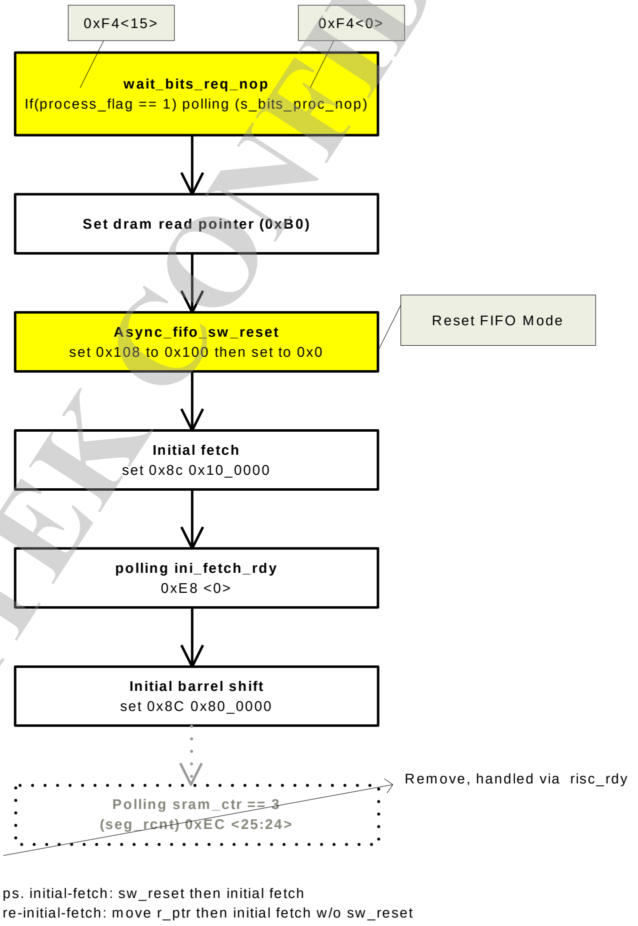

Figure 6-91. Flow chart of initial fetch and initial Barrel-shift

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6.25.3.5.1 Bitstream FIFO (vb SRAM)

After initial fetch, the bitstream will be loaded in to bitstream FIFO (vb SRAM). When the amount of empty data is less than the threshold, the engine will auto fetch bitstream from DRAM to bitstream FIFO (see Figure 6-92).

- Read pointer of bitstream buffer: vb_sram_ra (0x0EC VB_SRAM_RA<4:0>)
- Write pointer of bitstream buffer: vb_sram_wa (0x0EC VB_SRAM_WA<12:8>)
- Read counter for each 128-bit data: seg_rcnt (0x0EC SEG_RCNT<25:24>)

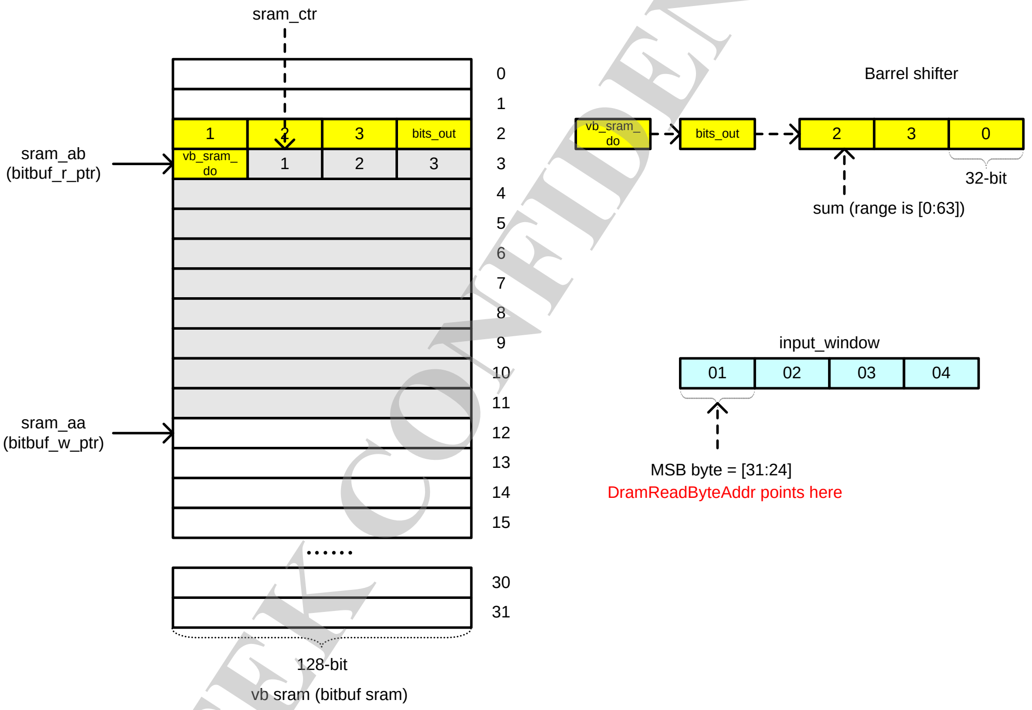

Figure 6-92. Block diagram of bitstream buffer and barrel shifter

When vb_sram_ra points to row 3 and seg_rcnt value is 1, the barrel shifter content is {row2{2}, row2{3}, row3{0}}.

6.25.3.5.2 Barrel Shifter

The barrel shifter has 3*32 bits. The sum is the read pointer of barrel shifter, i.e. the start address of input window. Figure 6-93 is the block diagram.

- Read pointer of barrel shifter: Sum (0x114 BSSR<5:0>); range [0, 63]
- Input window (0x0F0 BIW(#60) <31:0>)

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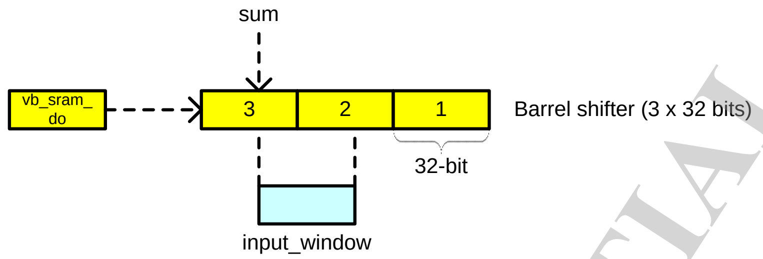

Figure 6-93. Block diagram of barrel shifter and input window

VDEC also provides checksum register for debugging. By checking the values of these registers with simulation result, you can confirm whether the above process is correct. The location of checksum registers are listed in Table 6-31.

Table 6-31. Checksum register

Spec	Base	Reg offset
BITS_DMA		
MPEG-2	**VLD**	**69 (0x114) bit [5:0]**
H.264/MVC	**AVC_VLD**	**33 (0xa4) bit [21:16]**

6.25.3.6 VDEC Output Format

VDEC supports two types of output formats:

- 16*32 Progressive Mode (NV12_BLK)
  - Original block mode (default)
- 16*32 Field Compact Mode (NV12_BLK_FCM)
  - PP, set PP reg 15 bit[28] = 0
  - MC, set MC reg 584 bit[24] = 0

The difference between progressive mode and field compact mode is shown in Figure 6-94. Besides MPEG2, MPEG4 and VP6, it is recommended that the output results are written to DRAM by PP for better efficiency.

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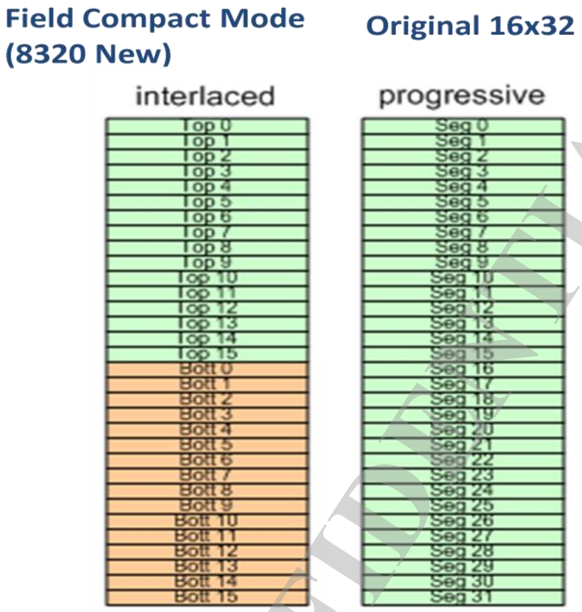

Figure 6-94. Field compact mode and progressive mode

6.25.3.7 VDEC Break Function

This section describes the correct steps for FW to break VDEC before finishing decoding a picture.

1. Set up vdec_break.
   - Set VDEC_MISC reg 64 Bit [0] (vdec_break) = 1'b1
2. Monitor status vdec_break_ok
   - VDEC_MISC reg 65 Bit [0]: vdec_break_ok_0
   - VDEC_MISC reg 65 Bit [4]: vdec_break_ok_1
   - Monitor until both vdec_break_ok _0 = 1 && vdec_break_ok_1= 1
3. Software reset
   - VLD reg 66 Bit [0]: vdec_sw_rst
   - Set vdec_sw_rst = 1 then reset vdec_sw_rst = 0
4. Turn off the clocks.
5. Finish.

6.25.4 VDEC Register Map

6.25.4.1 VDEC_GLOBAL_CON

Module name: vdec_global_con Base address: (+16000000h)

Address	Name	Width	Register Function
16000000	**VDEC_CKEN_SET**	32	Enable VDEC Clock (Power On) Register (CG Off)
16000004	**VDEC_CKEN_CL**	32	Disable VDEC Clock (Power Down) Register (CG On)

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Address	Name	Width	Register Function
	R		
16000008	SMI_LARB1_CK EN_SET	32	Enable SMI Clock (Power On) Register (CG Off)
1600000C	SMI_LARB1_CK EN_CLR	32	Disable SMI Clock (Power Down) Register (CG On)
16000010	VDEC_RESETB_CON	32	VDEC Reset Register
16000014	SMI_LARB1_RE STB_CON	32	SMI_LARB Reset Register
16000018	VDEC_DCM_CO N	32	VDEC DCM Off While Decoding Error
1600001C	VDEC_SRAM_C FG	32	VDEC SRAM DELSEL Configuration Register
16000020	VDEC_ROM_CF G	32	VDEC ROM Configuration Register
16000028	VDEC_MBIST_MODE_CFG0	32	VDEC Core MBIST Mode Control Register
1600002C	VDEC_MBIST_R ESETB_CFG	32	VDEC Core MBIST Reset Control Register
16000030	VDEC_MBIST_D EBUG_CFG	32	VDEC Core MBIST Debug Control Register
16000034	VDEC_MBIST_H OLDB_CFG0	32	VDEC Core MBIST holdb Control Register
16000038	VDEC_MBIST_B ACKGROUND	32	VDEC Core MBIST Background Control Register
1600003C	VDEC_MBIST_D ONE_CFG0	32	VDEC Core MBIST Done Monitor
16000040	VDEC_MBIST_F AIL_0	32	VDEC Core MBIST Done Failure Status Monitor 0
16000044	VDEC_MBIST_F AIL_1	32	VDEC Core MBIST Done Failure Status Monitor 1
16000048	VDEC_MBIST_MODE_CFG1	32	VDEC Core MBIST Mode Control Register
1600004C	VDEC_MBIST_H OLDB_CFG1	32	VDEC Core MBIST holdb Control Register
16000050	VDEC_MBIST_D ONE_CFG1	32	VDEC Core MBIST Done Monitor
16000058	VDEC_MBIST_B SEL_2	32	BSEL Value for #02 VDEC Core MBIST Controller
16000060	VDEC_MBIST_B SEL_4	32	BSEL Value for #04 VDEC Core MBIST Controller
16000064	VDEC_MBIST_B SEL_5	32	BSEL Value for #05 VDEC Core MBIST Controller
16000068	VDEC_MBIST_B SEL_6	32	BSEL Value for #06 VDEC Core MBIST Controller
1600006C	VDEC_MBIST_B SEL_7	32	BSEL Value for #07 VDEC Core MBIST Controller
16000070	VDEC_MBIST_B SEL_8	32	BSEL Value for #08 VDEC Core MBIST Controller
16000074	VDEC_MBIST_B SEL_9	32	BSEL Value for #09 VDEC Core MBIST Controller
16000080	VDEC_MBIST_B SEL_12	32	BSEL Value for #12 VDEC Core MBIST Controller
16000084	VDEC_MBIST_B SEL_13	32	BSEL Value for #13 VDEC Core MBIST Controller

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Address	Name	Width	Register Function
16000088	VDEC_MBIST_BSEL_14	32	BSEL Value for #14 VDEC Core MBIST Controller
1600008C	VDEC_MBIST_BSEL_15	32	BSEL Value for #15 VDEC Core MBIST Controller
16000090	VDEC_MBIST_BSEL_16	32	BSEL Value for #16 VDEC Core MBIST Controller
16000094	VDEC_MBIST_BSEL_17	32	BSEL Value for #17 VDEC Core MBIST Controller
16000098	VDEC_MBIST_BSEL_18	32	BSEL Value for #18 VDEC Core MBIST Controller
160000AC	VDEC_MBIST_BSEL_23	32	BSEL Value for #23 VDEC Core MBIST Controller
160000B0	VDEC_MBIST_BSEL_24	32	BSEL Value for #23 VDEC Core MBIST Controller
160000F0	MBIST_SCAN_OUT_SEL	32	Selects Control of MBIST Scan Out Pin
160000F4	MBIST_FAIL_SEL	32	Selects Control of MBIST Fail Pin

16000000 **VDEC_CKEN_SET** **Enable VDEC Clock (Power On) Register (CG Off)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								VDEC_CKEN_ENG				VDEC_ACTIVE				VDEC_CKEN_CFG
Type								RO				RO				WO
Reset								0				0				0

Bit(s)	Name	Description
8	VDEC_CKEN_ENG	0: Disable VDEC clock 1: Enable VDEC clock
4	VDEC_ACTIVE	
0	VDEC_CKEN_CFG	0: No effect 1: Enable VDEC clock

16000004 **VDEC_CKEN_CLR** **Disable VDEC Clock (Power Down) Register (CG On)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								VDEC_CKEN_EN				VDEC_ACTIVE_CL				VDEC_PDN_CFG

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								G				R				
Type								RO				RO				WO
Reset								0				0				0

Bit(s)	Name	Description
8	VDEC_CKEN_ENG	0: Disable VDEC clock 1: Enable VDEC clock
4	VDEC_ACTIVE_CLR	
0	VDEC_PDN_CFG	0: No effect 1: Disable VDEC clock

16000008 **SMI_LARB1_CKEN_SET** **Enable SMI Clock (Power On) Register (CG Off)** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name																SMI_LARB1_CKEN_CFG
Type																RW
Reset																1

Bit(s)	Name	Description
0	SMI_LARB1_CKEN_CFG	0: No effect 1: Enable VDEC clock

1600000C **SMI_LARB1_CKEN_CLR** **Disable SMI Clock (Power Down) Register (CG On)** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name																SMI_LARB1_PDN_CFG
Type																RW
Reset																1

Bit(s)	Name	Description
0	SMI_LARB1_PDN_CFG	0: No effect 1: Disable VDEC clock

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16000010 **VDEC_RESETB_CON** **VDEC Reset Register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**VDEC_RSTB**
Type																RW
Reset																1

Bit(s)	Name	Description
0	VDEC_RSTB	0: Reset the entire VDEC system (incl. MBIST registers) (Reset is low active. Be sure to set it back to 1 for VDEC sub-system to work again.) 1: No effect

16000014 **SMI_LARB1_RESTB_CON** **SMI_LARB Reset Register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**SMI_LARB1_RSTB**
Type																RW
Reset																1

Bit(s)	Name	Description
0	SMI_LARB1_RSTB	0: Reset smi_larb1 1: No effect

16000018 **VDEC_DCM_CON** **VDEC DCM Off While Decoding Error** **00000010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**VDEC_ERR_DCM OFF**				**HW_DCM OFF**
Type												RW				RW
Reset												1				0

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Bit(s)	Name	Description
4	VDEC_ERR_DCMOFF	0: DCM on (auto power_off after receiving interrupt) 1: DCM off (disable auto power_off)
0	HW_DCMOFF	0: DCM on (auto power_off after receiving interrupt) 1: DCM off (disable auto power_off)

1600001C **VDEC_SRAM_CFG** **VDEC SRAM DELSEL Configuration Register** **000AA5A5**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													t_rvt_b256m1_delsel		t_lvt_b256m1_delsel	
Type													RW		RW	
Reset													1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s_rvt_b512m4_delsel				s_rvt_b256m2_s_delsel				s_rvt_b256m2_l_delsel				s_lvt_b64m4_delsel			
Type	RW				RW				RW				RW			
Reset	1	0	1	0	0	1	0	1	1	0	1	0	0	1	0	1

Bit(s)	Name	Description
19:18	t_rvt_b256m1_delsel	SRAM configuration: TP_B256M1_DELSEL
17:16	t_lvt_b256m1_delsel	SRAM configuration: TP_B256M1_DELSEL
15:12	s_rvt_b512m4_delsel	SRAM configuration: SP_B512M4_DELSEL
11:8	s_rvt_b256m2_s_delsel	SRAM configuration: SP_B256M2_DELSEL
7:4	s_rvt_b256m2_l_delsel	SRAM configuration: SP_B256M2_DELSEL
3:0	s_lvt_b64m4_delsel	SRAM configuration: SP_B64M4_DELSEL

16000020 **VDEC_ROM_CFG** **VDEC ROM Configuration Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ROM_4K_SEL[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ROM_4K_SEL[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ROM_4K_SEL	ROM configuration: ROM_4K_DELSEL

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16000028 **VDEC_MBIST_MODE_CFG0** **VDEC Core MBIST Mode Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VBSTMOD0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VBSTMOD0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VBSTMOD0	MBIST mode pin control for VDEC core

1600002C **VDEC_MBIST_RESETB_CFG** **VDEC Core MBIST Reset Control Register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																VBSTRSTB
Type																RW
Reset																1

Bit(s)	Name	Description
0	VBSTRSTB	MBIST reset_b pin control for VDEC core

16000030 **VDEC_MBIST_DEBUG_CFG** **VDEC Core MBIST Debug Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																VBSTDBG
Type																RW
Reset																0

Bit(s)	Name	Description
0	VBSTDBG	MBIST debug pin control for VDEC core

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16000034	VDEC_MBIST_HOLDB_CFG0	VDEC Core MBIST holdb Control Register	FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VBSTHLD0[31:16]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VBSTHLD0[15:0]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	VBSTHLD0	MBIST holdb pin control for VDEC core

16000038	VDEC_MBIST_BACKGROUND	VDEC Core MBIST Background Control Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														VBSTBGD		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	VBSTBGD	MBIST background pin control for VDEC core

1600003C	VDEC_MBIST_DONE_CFG0	VDEC Core MBIST Done Monitor	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VBSTDONO0[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VBSTDONO0[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VBSTDONO0	MBIST done pin monitor for VDEC core

16000040	VDEC_MBIST_FAIL_0	VDEC Core MBIST Done Failure Status Monitor 0	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	**VBSTFAL0[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**VBSTFAL0[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VBSTFAL0	MBIST fail pin [31:0] monitor for VDEC core

16000044 **VDEC_MBIST_FAIL_1** **VDEC Core MBIST Done Failure Status Monitor 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**VBSTFAL1[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**VBSTFAL1[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VBSTFAL1	MBIST fail pin [63:32] monitor for VDEC core

16000048 **VDEC_MBIST_MODE_CFG1** **VDEC Core MBIST Mode Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**VBSTMOD1**				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	VBSTMOD1	MBIST mode pin control for VDEC core

1600004C **VDEC_MBIST_HOLDB_CFG1** **VDEC Core MBIST holdb Control Register** **0000001F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**VBSTHLD1**				

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Type												RW				
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:0	VBSTHLD1	MBIST holdb pin control for VDEC core

16000050 VDEC_MBIST_DONE_CFG1 VDEC Core MBIST Done Monitor 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**VBSTDON1**				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	VBSTDON1	MBIST done pin monitor for VDEC core

16000058 VDEC_MBIST_BSEL_2 BSEL Value for #02 VDEC Core MBIST Controller 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**VBSTBSEL2**															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	VBSTBSEL2	MBIST bsel pin control for VDEC core MBIST module: [2]

16000060 VDEC_MBIST_BSEL_4 BSEL Value for #04 VDEC Core MBIST Controller 00000FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**VBSTBSEL4**											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
11:0	VBSTBSEL4	MBIST bsel pin control for VDEC core MBIST module: [4]

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16000064 VDEC_MBIST_BSEL_5 BSEL Value for #05 VDEC Core MBIST Controller 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														VBSTBSEL5		
Type														RW		
Reset														1	1	1

Bit(s)	Name	Description
2:0	VBSTBSEL5	MBIST bsel pin control for VDEC core MBIST module: [5]

16000068 VDEC_MBIST_BSEL_6 BSEL Value for #06 VDEC Core MBIST Controller 0000007F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										VBSTBSEL6						
Type										RW						
Reset										1	1	1	1	1	1	1

Bit(s)	Name	Description
6:0	VBSTBSEL6	MBIST bsel pin control for VDEC core MBIST module: [6]

1600006C VDEC_MBIST_BSEL_7 BSEL Value for #07 VDEC Core MBIST Controller 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													VBSTBSEL7			
Type													RW			
Reset													1	1	1	1

Bit(s)	Name	Description
3:0	VBSTBSEL7	MBIST bsel pin control for VDEC core MBIST module: [7]

16000070 VDEC_MBIST_BSEL_8 BSEL Value for #08 VDEC Core MBIST Controller 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									VBSTBSEL8							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	VBSTBSEL8	MBIST bsel pin control for VDEC core MBIST module: [8]

16000074 **VDEC_MBIST_BSEL_9** **BSEL Value for #09 VDEC Core MBIST Controller** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									VBSTBSEL9							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	VBSTBSEL9	MBIST bsel pin control for VDEC core MBIST module: [9]

16000080 **VDEC_MBIST_BSEL_12** **BSEL Value for #12 VDEC Core MBIST Controller** **00000007**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														VBSTBSEL12		
Type														RW		
Reset														1	1	1

Bit(s)	Name	Description
2:0	VBSTBSEL12	MBIST bsel pin control for VDEC core MBIST module: [12]

16000084 **VDEC_MBIST_BSEL_13** **BSEL Value for #13 VDEC Core MBIST Controller** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													VBSTBSEL13			
Type													RW			
Reset													1	1	1	1

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Bit(s)	Name	Description
3:0	VBSTBSEL13	MBIST bsel pin control for VDEC core MBIST module: [13]

16000088 VDEC_MBIST_BSEL_14 BSEL Value for #14 VDEC Core MBIST Controller 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									VBSTBSEL14							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	VBSTBSEL14	MBIST bsel pin control for VDEC core MBIST module: [14]

1600008C VDEC_MBIST_BSEL_15 BSEL Value for #15 VDEC Core MBIST Controller 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VBSTBSEL15															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	VBSTBSEL15	MBIST bsel pin control for VDEC core MBIST module: [15]

16000090 VDEC_MBIST_BSEL_16 BSEL Value for #16 VDEC Core MBIST Controller 0000007F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										VBSTBSEL16						
Type										RW						
Reset										1	1	1	1	1	1	1

Bit(s)	Name	Description
6:0	VBSTBSEL16	MBIST bsel pin control for VDEC core MBIST module: [16]

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16000094 **VDEC_MBIST_BSEL_17** **BSEL Value for #17 VDEC Core MBIST Controller** **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VBSTBSEL17															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	VBSTBSEL17	MBIST bsel pin control for VDEC core MBIST module: [17]

16000098 **VDEC_MBIST_BSEL_18** **BSEL Value for #18 VDEC Core MBIST Controller** **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VBSTBSEL18															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	VBSTBSEL18	MBIST bsel pin control for VDEC core MBIST module: [18]

160000AC **VDEC_MBIST_BSEL_23** **BSEL Value for #23 VDEC Core MBIST Controller** **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LBSTBSEL23															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	LBSTBSEL23	MBIST bsel pin control for VDEC core MBIST module: [23]

160000B0 **VDEC_MBIST_BSEL_24** **BSEL Value for #23 VDEC Core MBIST Controller** **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LBSTBSEL24															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	LBSTBSEL24	MBIST bsel pin control for VDEC core MBIST module: [24]

160000F0 **MBIST_SCAN_OUT_SEL** **Selects Control of MBIST Scan Out Pin** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SOSEL						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	SOSEL	**Selects sub-system debug output port [0] for all MBIST scan out pins: 23 to 1** 0: vld_bus_int_unit 1: vld_avc__cabac_context 2: vb_mbist 3: vb2_mbist 4: pp_sram_y 5: pp_sram_c 6: pp_out_buf 7: mv_pre_fetch_buf 8: mv_out_buf 9: mc_nbm 10: mc_nbm_map 11: lat_wp_buf 12: lat_coef_buf 13: ds_mix_vld 14: ds_mix_deblocking 15: mc_qiu 16: mc_ibuf 17: mc_hiu

160000F4 **MBIST_FAIL_SEL** **Selects Control of MBIST Fail Pin** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										FALSEL						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
6:0	FALSEL	Selects sub-system debug output port [1] for all MBIST fail pins: 34 to 1

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6.26 H.264 Video Encoder

6.26.1 Introduction

This design is main stream H.264 video encoder. It is capable of encoding 1080P video at 30 frames per second (FPS) with promising superior video quality. This IP supports various encoding methods that satisfy basic requirements of easy software controllability. Furthermore, with advanced encoding technology, it brings astonishing high quality and low memory bandwidth requirements. It also considers the usage of portable devices and provides several power saving capabilities.

6.26.2 Features

The supported video codec and their capability are listed in the table below.

Table 6-32. Main features

H.264 encoder	Profile	High
	Level	4.1
	Speed	**1080p@30fps**

The video encoder takes DRAM as input, output and working buffer. It reads input frame buffers, executes video encoding and writes encoded bitstream to the output buffer. The driver software maintains all buffers and assigns proper values to the video encoder to allow the hardware to work correctly. Figure 6-95 shows the procedure of the video encoder. YUV420 two plane scan-line (NV12/NV21), YUV420 three plane scan-line (YV12/I420) or MTK block formats are supported.

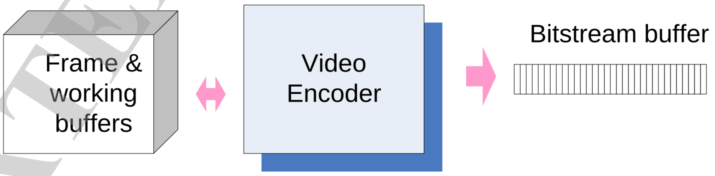

Figure 6-95. Procedure of video encoder

6.26.3 Block Diagram

Figure 6-96 is the brief IP architecture and local on-chip-bus architecture. The interface for controlling it is consisted of ARM APB bus and MediaTek proprietary SMI bus. It reports hardware event through interrupts or software polling. In addition, it adopts several SMI ports and one APB port. The video encoder is configured by software through the APB interface. As the register is configured, the sequencer will send the corresponding control signals to trigger sub-modules. DMA will acquire and store back the image data and bitstream from and to memory according to the configured address. ME will conduct motion estimation to decide motion vector for later encoding. MC will conduct motion compensation to give predicted pixel values. TQ will conduct transform and quantization operation and write reconstructed pixels to DB and quantized transformed coefficient to

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EC. DB will conduct de-blocking operation and allow the DMA to store back the processed frame as the next frame's reference frame. EC will conduct entropy encoding, and the coding can be variable length code, context based arithmetic code or context based variable length code. The encoded bitstream will be written to memory by DMA.

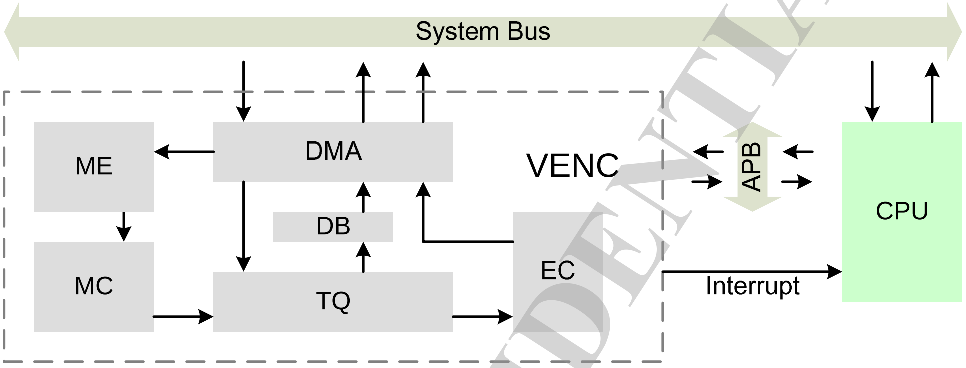

Figure 6-96. Block diagram of video encoder

6.26.4 Register Definition

Module name: VENC Base address: (+17002000h)

Address	Name	Width	Register Function
17002094	VENC_CLK_CG_CTRL	32	VENC_CLK_CG_CTRL
170020EC	VENC_CE	32	VIDEO_CE
170020F4	VENC_CLK_DCM_CTRL	32	VIDEO_CLK_DCM_CTRL

17002094 VENC_CLK_CG_CTRL VIDEO_CLK_CG_CTRL FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CLK_CG_CTRL[31:16]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_CG_CTRL[15:0]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	CLK_CG_CTRL	**Uses 1-bit to enable VENC internal gated clock mechanism** 1'b0: Disable gated clock (all clock sources will work at all time) 1'b1: Sequencer will turn off specific clock when the corresponding engine is not under operation.

170020EC VENC_CE VIDEO_CE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CE
Type																RW
Reset																0

Bit(s)	Name	Description
0	CE	**Enables VENC chip** 1'b1: All VENC internal registers can be written and operated. 1'b0: VENC is stall and no data can be read from local bus decoder except for MMR.

170020F4 **VENC_CLK_DCM_CTRL** **VIDEO_CLK_DCM_CTRL** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DCM_STATUS															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CLK_DCM_CTRL
Type																RW
Reset																1

Bit(s)	Name	Description
31	DCM_STATUS	**Uses 1-bit to show VENC DCM status** 1'b0: Disable DCM management (all clock sources will work at all time) 1'b1: Sequencer will turn off internal VENC clock when frame encoding is finished
0	CLK_DCM_CTRL	**Uses 1-bit to enable VENC DCM mechanism** 1'b0: Disable DCM management (all clock sources will work at all time) 1'b1: Sequencer will turn off internal VENC clock when frame encoding is finished.

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6.27 MFG

6.27.1 Introduction

MFG contains Mali-T720 MP2 GPU and clock/reset control logic. The Mali-T720 series of GPUs process extremely complicated graphics and perform general processing tasks assigned by the main application processor. This diagram shows the main components and interface of MFG.

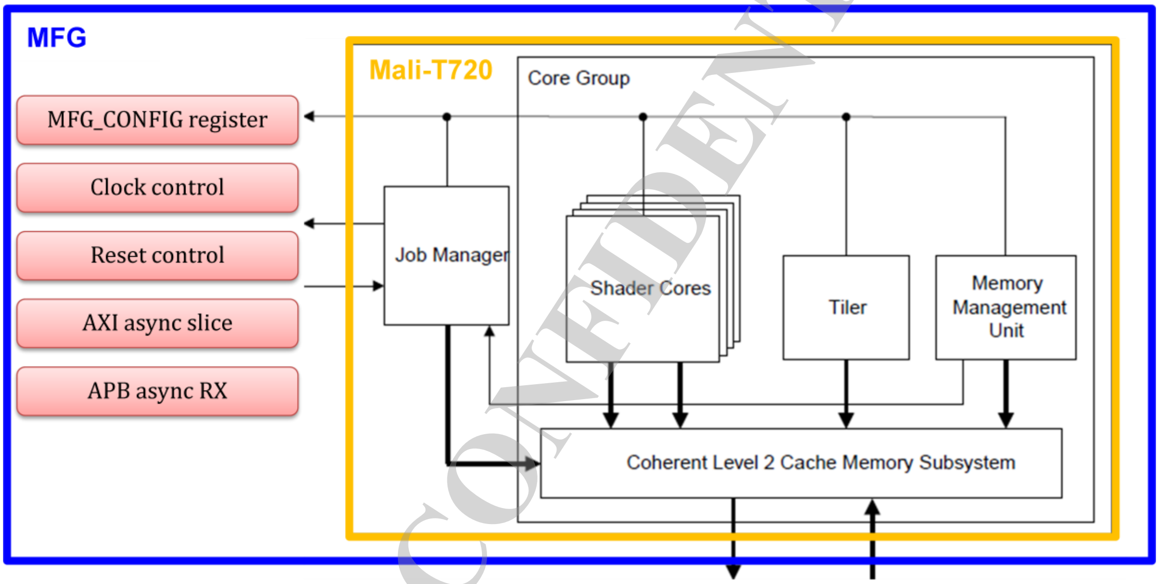

Figure 6-97. Block diagram and interface of MFG

6.27.2 Features

The Mali-T720 MP2 GPU includes the following features:

- A rich API feature set with high-performance support for both shader-based and fixed-function graphics APIs. These API graphics industry standards are:
  - *OpenGL ES 1.1 Specification* at *Khronos*
  - *OpenGL ES 2.0 Specification* at *Khronos*
  - *OpenGL ES 3.0 Specification* at *Khronos*
  - *OpenCL 1.0 Specification* at *Khronos*
  - *OpenCL 1.1 Specification* at *Khronos*
  - *OpenCL 1.2 Specification* at *Khronos*
  - *DirectX 9 Specification*
- Anti-aliasing capabilities
- An effective core for *General Purpose computing on GPU* (GPGPU) applications
- Image quality using double-precision FP64, and anti-aliasing
- Bus protocol
  - 128-bit AXI bus with up to 32 outstanding
  - 32-bit APB bus

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- Level-2 cache
  - 128KB
  - 4-way set associative
- Performance
  - Triangle rate 100M Tri/sec
  - Fill rate 900M Pixels/sec
  - Shader rate 15.3 GFLOPS

6.27.3 Register Definition

Module name: MFG_TOP Base address: (+13000000h)

Address	Name	Width	Register Function
13000000	MFG_CG_CON	32	MFG Clock Gating Register
13000004	MFG_CG_SET	32	MFG Clock Gating Set Register
13000008	MFG_CG_CLR	32	MFG Clock Gating Clear Register
1300000C	MFG_RESET	32	MFG Reset Register
13000010	MFG_DCM_CON_0	32	MFG DCM Control Register 0
13000018	MFG_APB_DEBUG	32	MFG APB Debug Register
1300001C	MFG_ASYNC_CON	32	MFG ASYNC_SEL Register
13000020	MFG_SRAM_DELSEL_00	32	MFG_SRAM_DELSEL_00
13000024	MFG_SRAM_DELSEL_01	32	MFG_SRAM_DELSEL_01
13000028	MFG_SRAM_DELSEL_02	32	MFG_SRAM_DELSEL_02
1300002C	MFG_SRAM_DELSEL_03	32	MFG_SRAM_DELSEL_03
130000A0	MFG_MBIST_MODE	32	MFG MBIST Mode Control Register 0
130000A4	MFG_MBIST_MODE_1	32	MFG MBIST Mode Control Register 1
130000A8	MFG_MBIST_DBG_CON	32	MFG MBIST Debug Register
130000AC	MFG_MBIST_BG	32	MFG MBIST Background Register
130000B0	MFG_GLOBAL_CON	32	MFG Global Control Register
130000B4	MFG_MBIST_HOLDB	32	MFG MBIST Holdb Control Register
130000C0	MFG_MBIST_BSEL_0	32	MFG MBIST BSEL Register 0
130000D0	MFG_MBIST_DONE_0	32	MFG MBIST Done Register 0
130000D4	MFG_MBIST_DONE_1	32	MFG MBIST Done Register 1
13000100	MFG_MBIST_FAIL_0	32	MFG MBIST Fail Register 0
13000104	MFG_MBIST_FAIL_1	32	MFG MBIST Fail Register 1

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Address	Name	Width	Register Function
13000108	MFG_MBIST_FAIL_2	32	MFG MBIST Fail Register 2
1300010C	MFG_MBIST_FAIL_3	32	MFG MBIST Fail Register 3
13000110	MFG_MBIST_FAIL_4	32	MFG MBIST Fail Register 4
13000114	MFG_MBIST_FAIL_5	32	MFG MBIST Fail Register 5
13000124	MFG_MBIST_DONE_FAIL	32	MFG MBIST Done and Fail Register
13000130	MFG_TIMESTAMP	32	MFG IP Timestamp Register
13000134	MFG_BARRIER_DISABLE	32	MFG IP Barrier Disable Register
13000180	MFG_DEBUG_SEL	32	MFG Debug Select Register
13000184	MFG_DEBUG_A	32	MFG Debug Register A
13000188	MFG_DEBUG_B	32	MFG Debug Register B
130001A0	MFG_AXI0_CRC_0	32	MFG_AXI0_CRC_0
130001A4	MFG_AXI0_CRC_1	32	MFG_AXI0_CRC_1
130001A8	MFG_AXI0_CRC_2	32	MFG_AXI0_CRC_2
130001AC	MFG_AXI0_CRC_3	32	MFG_AXI0_CRC_3

13000000 MFG_CG_CON MFG Clock Gating Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name																BG3D_PDN
Type																RU
Reset																0

Bit(s)	Mnemonic	Name	Description
0		BG3D_PDN	**Controls 3D core clock gating** 0: Turn on 3D core clock 1: Turn off 3D core clock

13000004 MFG_CG_SET MFG Clock Gating Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BG3D_SET
Type																WO
Reset																0

Bit(s)	Mnemonic	Name	Description
0		BG3D_SET	Turns off 3D core clock

13000008 **MFG_CG_CLR** **MFG Clock Gating Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BG3D_CLR
Type																WO
Reset																0

Bit(s)	Mnemonic	Name	Description
0		BG3D_CLR	Turns on 3D core clock

1300000C **MFG_RESET** **MFG Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															AXI_RESET	G3D_RESET
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1		AXI_RESET	Resets 3D software
0		G3D_RESET	Resets AXI async

13000010 **MFG_DCM_CON_0** **MFG DCM Control Register 0** **0000C03F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															BG3D_DCM_ALL	BG3D_ASYNC_F

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															_IDLE_OPT	REE_RUN
Type															RW	RW
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BG3D_DCM_EN	BG3D_DBC_EN	BG3D_FSEL							BG3D_DBC_CNT						
Type	RW	RW	RW							RW						
Reset	1	1	0	0	0	0	0	0		0	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
17		BG3D_DCM_ALL_IDLE_OPT	**Option for DCM all idle**
16		BG3D_ASYNC_FREE_RUN	**Forces AXI async interface to turn on**
15		BG3D_DCM_EN	**Enables core clock DCM**
14		BG3D_DBC_EN	**Enables core clock debounce DCM**
13:8		BG3D_FSEL	**Selects core clock frequency** 100000: Divide by 1 010000: Divide by 2 001000: Divide by 4 000100: Divide by 8 000010: Divide by 16 000001: Divide by 32 000000: Divide by 64
6:0		BG3D_DBC_CNT	**Debounce counter**

13000018 **MFG_APB_DEBUG** **MFG APB Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERR_ADDR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERR_TIMEOUT															ERR_FLAG_EN
Type	RU															RW
Reset	0															0

Bit(s)	Mnemonic	Name	Description
31:16		ERR_ADDR	APR error address
15		ERR_TIMEOUT	APB error timeout occurs.
0		ERR_FLAG_EN	Enables APB error flag

1300001C **MFG_ASYNC_CON** **MFG ASYNC_SEL Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																MEM_REG_AR_FCTRL_EN
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			MEM_DEPTH_VALUE										MEM_SLV_SEL		MEM_MST_SEL	
Type			RW										RW		RW	
Reset			0	0	0	0	0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description
16		MEM_REG_AR_FCTRL_EN	**Enables AXI async IP FCTRL**
13:8		MEM_DEPTH_VALUE	**AXI async IP depth value**
3:2		MEM_SLV_SEL	**Selects async-FIFO depth** 00: Sync delay 1T 01: Sync delay 2T 10: Sync delay 3T 11: Sync delay 3T
1:0		MEM_MST_SEL	**Selects async-FIFO depth** 00: Sync delay 1T 01: Sync delay 2T 10: Sync delay 3T 11: Sync delay 3T

13000020 **MFG_SRAM_DELSEL_00** **MFG_SRAM_DELSEL_00** **00000002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															MFG_SRAM_DELSEL_GLOBAL	
Type															RW	
Reset															1	0

Bit(s)	Mnemonic	Name	Description
1:0		MFG_SRAM_DELSEL_GLOBAL	MFG_SRAM_DELSEL for Mali Global

13000024 **MFG_SRAM_DELSEL_01** **MFG_SRAM_DELSEL_01** **000025A5**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**MFG_SRAM_DELSEL_CG**													
Type			RW													
Reset			1	0	0	1	0	1	1	0	1	0	0	1	0	1

Bit(s)	Mnemonic	Name	Description
13:0		MFG_SRAM_DELSEL_CG	MFG_SRAM_DELSEL for Mali Core Group

13000028 **MFG_SRAM_DELSEL_02** **MFG_SRAM_DELSEL_02** **000002A5**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**MFG_SRAM_DELSEL_SC0**									
Type							RW									
Reset							1	0	1	0	1	0	0	1	0	1

Bit(s)	Mnemonic	Name	Description
9:0		MFG_SRAM_DELSEL_SC0	MFG_SRAM_DELSEL for Mali Shader Core0

1300002C **MFG_SRAM_DELSEL_03** **MFG_SRAM_DELSEL_03** **000002A5**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**MFG_SRAM_DELSEL_SC1**									
Type							RW									
Reset							1	0	1	0	1	0	0	1	0	1

Bit(s)	Mnemonic	Name	Description
9:0		MFG_SRAM_DELSEL_SC1	MFG_SRAM_DELSEL for Mali Shader Core1 (not exist in Denali2)

130000A0 **MFG_MBIST_MODE** **MFG MBIST Mode Control Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MBIST_**	**MBIST_MODE_0**							**MBIST_MODE[23:16]**							

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	RST B															
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MBIST_MODE[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		MBIST_RSTB	Resets MBIST
30:24		MBIST_MODE_0	MBIST mode 0 enable for Mali SRAM (not exist in Denali2)
23:0		MBIST_MODE	MBIST mode enable for Mali SRAM

130000A4 MFG_MBIST_MODE_1 MFG MBIST Mode Control Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**MBIST_MODE_1**				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		MBIST_MODE_1	MBIST mode 1 enable for Mali SRAM (not exist in Denali2)

130000A8 MFG_MBIST_DBG_CON MFG MBIST Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											**MBIST_DONE_SEL**					
Type											RW					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**MBIST_FAIL_SEL**											**MBIST_DBG_EN**
Type					RW											RW
Reset					0	0	0	0	0	0	0	0				0

Bit(s)	Mnemonic	Name	Description
21:16		MBIST_DONE_SEL	**Selects MBIST done bus** When this register is set to i, MBIST_DONE_MUX = MBIST_DONE[i] will output to DEBUG.
11:4		MBIST_FAIL_SEL	**Selects MBIST fail bus** When this register is set to i, MBIST_FAIL_MUX = MBIST_FAIL[i] will output to DEBUG.
0		MBIST_DBG_EN	**Enables MBIST debugging for SRAM with diagnosis circuit**

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130000AC **MFG_MBIST_BG** **MFG MBIST Background Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														MBIST_BG		
Type														RW		
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2:0		MBIST_BG	Selects MBIST background

130000B0 **MFG_GLOBAL_CON** **MFG Global Control Register** **00000003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PSEL_M_GLOBAL_CON_OPT	PSEL_S_GLOBAL_CON_OPT
Type															RW	RW
Reset															1	1

Bit(s)	Mnemonic	Name	Description
1		PSEL_M_GLOBAL_CON_OPT	Option for master PSEL Global control
0		PSEL_S_GLOBAL_CON_OPT	Option for slave PSEL Global control

130000B4 **MFG_MBIST_HOLDB** **MFG MBIST Holdb Control Register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MBSIT_HOLDB_CON
Type																RW
Reset																1

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Bit(s)	Mnemonic	Name	Description
0		MBSIT_HOLDB_CON	MBIST holdb register 1 for Mali SRAM

130000C0 **MFG_MBIST_BSEL_0** **MFG MBIST BSEL Register 0** **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MBIST_BSEL_0															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
15:0		MBIST_BSEL_0	MFG MBIST BSEL register for Mali SRAM

130000D0 **MFG_MBIST_DONE_0** **MFG MBIST Done Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MBIST_DONE_SC1_0								MBIST_DONE_SC0[11:4]							
Type	RU								RU							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MBIST_DONE_SC0[3:0]				MBIST_DONE_CG											MBIST_DONE_GLOBAL
Type	RU				RU											RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		MBIST_DONE_SC1_0	MBIST done 0 for Mali Shader Core1 (not exist in Denali2)
23:12		MBIST_DONE_SC0	MBIST done 0 for Mali Shader Core0
11:1		MBIST_DONE_CG	MBIST done 0 for Mali core group
0		MBIST_DONE_GLOBAL	MBIST done 0 for Mali global

130000D4 **MFG_MBIST_DONE_1** **MFG MBIST Done Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

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Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**MBIST_DONE_SC1_1**			
Type													RU			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0		MBIST_DONE_SC1_1	MBIST done 1 for Mali Shader Core1 (not exist in Denali2)

13000100 **MFG_MBIST_FAIL_0** **MFG MBIST Fail Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MBIST_FAIL_CG_0[29:14]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MBIST_FAIL_CG_0[13:0]**														**MBIST_FAIL_GLOBAL**	
Type	RU														RU	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:2		MBIST_FAIL_CG_0	MBIST fail 0 for Mali core group
1:0		MBIST_FAIL_GLOBAL	MBIST fail 0 for Mali global

13000104 **MFG_MBIST_FAIL_1** **MFG MBIST Fail Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MBIST_FAIL_SC0_0**							**MBIST_FAIL_CG_1[24:16]**								
Type	RU							RU								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MBIST_FAIL_CG_1[15:0]**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25		MBIST_FAIL_SC0_0	MBIST fail 0 for Mali Shader Core0
24:0		MBIST_FAIL_CG_1	MBIST fail 1 for Mali core group

13000108 **MFG_MBIST_FAIL_2** **MFG MBIST Fail Register 2** **00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MBSIT_FAIL_SC0_1[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MBSIT_FAIL_SC0_1[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MBSIT_FAIL_SC0_1	MBIST fail 1 for Mali Shader Core0

1300010C **MFG_MBIST_FAIL_3** **MFG MBIST Fail Register 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MBIST_FAIL_SC1_0										MBIST_FAIL_SC0_2[21:16]					
Type	RU										RU					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MBIST_FAIL_SC0_2[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:22		MBIST_FAIL_SC1_0	MBIST fail 0 for Mali Shader Core1 (not exist in Denali2)
21:0		MBIST_FAIL_SC0_2	MBIST fail 2 for Mali Shader Core0

13000110 **MFG_MBIST_FAIL_4** **MFG MBIST Fail Register 4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MBIST_FAIL_SC1_1[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MBIST_FAIL_SC1_1[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MBIST_FAIL_SC1_1	MBIST fail 1 for Mali Shader Core1 (not exist in Denali2)

13000114 **MFG_MBIST_FAIL_5** **MFG MBIST Fail Register 5** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														MBIST_FAIL_SC		

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														1_2[18:16]		
Type														RU		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MBIST_FAIL_SC1_2[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
18:0		MBIST_FAIL_SC1_2	MBIST fail 2 for Mali Shader Core1 (not exist in Denali2)

13000124 MFG_MBIST_DONE_FAIL MFG MBIST Done and Fail Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															MFG_MBIST_FAIL_OR_ALL_X	MFG_MBIST_DONE_AND_ALL_X1
Type															RU	RU
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1		MFG_MBIST_FAIL_OR_ALL_X	MBIST FAIL is OR'ed to one signal
0		MFG_MBIST_DONE_AND_ALL_X1	MBIST DONE is AND'ed to one signal

13000130 MFG_TIMESTAMP MFG IP Timestamp Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TOP_TSVALUEB_EN
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
0		TOP_TSVALUEB_EN	Enables Mali timestamp

13000134 **MFG_BARRIERDISABLE** **MFG IP Barrier Disable Register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MALI_T760_BARRIERDISABLE
Type																RW
Reset																1

Bit(s)	Mnemonic	Name	Description
0		MALI_T760_BARRIERDISABLE	Disables ACE barrier

13000180 **MFG_DEBUG_SEL** **MFG Debug Select Register** **00000108**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MFG_CRC_CLR				MFG_DEBUG_SEL				
Type								RW				RW				
Reset								1				0	1	0	0	0

Bit(s)	Mnemonic	Name	Description
8		MFG_CRC_CLR	**Clears GPU CRC**
4:0		MFG_DEBUG_SEL	**Selects MFG debugging signals** 5'h0: MBIST 5'h1: IRQ 5'h3: MISC

13000184 **MFG_DEBUG_A** **MFG Debug Register A** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_DEBUG_A[31:16]															

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Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_DEBUG_A[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_DEBUG_A	MFG DEBUG OUT signals

13000188 **MFG_DEBUG_B** **MFG Debug Register B** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_DEBUG_B[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_DEBUG_B[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_DEBUG_B	Reserved

130001A0 **MFG_AXI0_CRC_0** **MFG_AXI0_CRC_0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_AXI0_CRC_0[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_AXI0_CRC_0[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_AXI0_CRC_0	

130001A4 **MFG_AXI0_CRC_1** **MFG_AXI0_CRC_1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_AXI0_CRC_1[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_AXI0_CRC_1[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31:0		MFG_AXI0_CRC_1	

130001A8 **MFG_AXI0_CRC_2** **MFG_AXI0_CRC_2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_AXI0_CRC_2[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_AXI0_CRC_2[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_AXI0_CRC_2	

130001AC **MFG_AXI0_CRC_3** **MFG_AXI0_CRC_3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_AXI0_CRC_3[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_AXI0_CRC_3[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_AXI0_CRC_3	

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6.28 Multimedia Memory Management Unit (M4U)

6.28.1 Introduction

In the smart phone system, the multimedia (MM) engine usually requires a certain amount of contiguous memory region. In order to avoid memory fragmentation, the Operating System (OS) needs to perform memory copy to align the requested ranges with one another. However, excessive memory copy may greatly degrade the system performance. For some performance-critical engines, a common method to guarantee sufficient memory available for them is to statically reserve the physical memory. This solution is straightforward but expensive since a large amount memory is reserved for a certain engine without sharing with others.

The Multimedia Memory Management Unit (M4U), which is also referred to as the IOMMU, is therefore designed to solve the fragmentation problem by paging the memory space and to reduce the cost of static memory reservation. Each page has an identical size of 4KB and can inherently be self-aligned without needing any memory copies. This means the system performance will be enhanced a lot due to exempting memory copies. With the unit of 4KB, the chance of occurring internal fragmentation is acceptable in our system and moreover the virtual memory efficiency is much better than that of using a larger unit of page size, e.g. 1MB. Therefore, with a smaller unit of page size, there will be ample page numbers available in the system. The engines will have even more chances to obtain the pages from the OS.

The major function of the M4U is to translate a virtual address into a physical one by performing page table look-up. As a result, the memory space of the MM engines is virtualized and contiguously seen by the MM engines. Along with the page table managed by the OS, there is no longer need to statically reserve any physical memory for the MM engines on system-up. The physical memory can be allocated dynamically in the unit of 4KB by the OS. From the system cost of view, the physical memory size is greatly reduced.

Since all the MM engines can use the M4U to perform address translation, M4U plays a critical role in MM performance, especially for hard real-time MM engines. The translation look-aside buffer (TLB), a major component in the M4U, caches the page numbers to accelerate the translation process. Besides, M4U performs auto-prefetching function to further lower the impact of page table walk caused by cache compulsory misses as well. In addition, a non-blocking TLB interface is designed to support miss-under-miss capability to achieve high performance translation.

6.28.2 Features

- One-level address translation with 4KB page size
- Two-level TLB structure (main TLB and prefetch TLB):
  - Level 1 is used to cache the most recently used pages.
  - Level 2 performs table walk when TLB miss and auto-prefetching when TLB hit
  - Entry number: 48
- Entry lock in the main TLB for critical pages
- Supports TLB range invalidation and full range invalidation to free TLB entries

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- Supports range sequential single-entry and multi-entry mode to minimize the entry usage
  - 16 sequential ranges available
- Supports range wrap mode in prefetch TLB for better address prediction
  - 4 wrap ranges available
- Each master port can be programmed to use M4U or not.
- Supports TrustZone security
- Supports high-performance bus prioritization for transactions with different priority levels

Descriptor format				
31:12	11:4	3	2	1:0
Page number	Reserved	Non-secure	Sharable	Access type

Figure 6-98. Descriptor attributes

In Figure 6-98, bit[3]:NS is used to differentiate secure and non-secure memory region for TrustZone security support. bit[2]:sharable is used to indicate if the coherence access with the CPU caches is required or not. bit[1:0]:should be 2'b10 for a valid 4KB page.

6.28.3 Block Diagram

In the system architecture, M4U is placed between the Smart Multimedia Interface (SMI) and the External Memory Interface (EMI) (see Figure 6-99). In Figure 6-99, M4U is shared by all MM engines and performs virtual to physical address translation for MM engines.

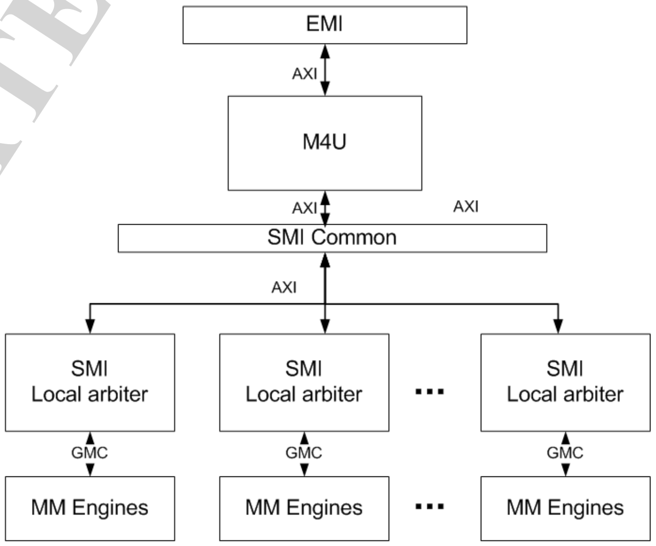

Figure 6-99. MM bus architecture

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When a virtual address comes from the master port, M4U will perform page table look-up to translate the virtual address into a physical one. main_tlb and pre_fetch_tlb in (see Figure 6-100) are two levels of caches for the page table. They are used to accelerate the translation process. If a page number is a miss in tlbs, prefetch_tlb will perform "table walk" to obtain the page number in the DRAM. prefetch_tlb contains auto-prefetching logic as well to increase the cache hit-rate. The non-blocking TLB interface is designed to support miss-under-miss capability to achieve high performance translation.

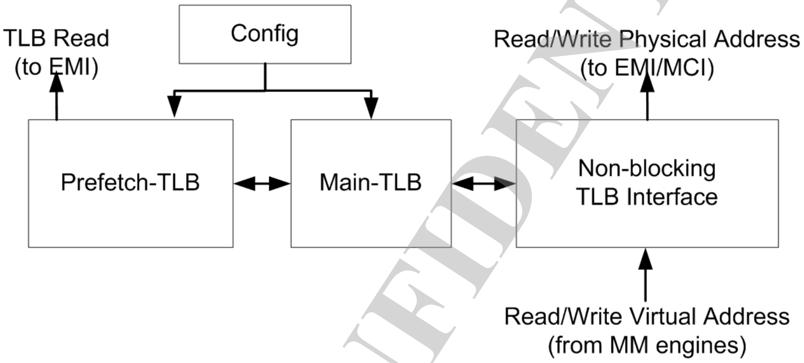

Figure 6-100. Block diagram of M4U

In Figure 6-100, M4U has a non-blocking interface to support miss-under-miss behavior and TLBs to cache the recently used pages.

6.28.4 Register Definition

Address	Name	Width	Register function
10205000	MMU_PT_BASE_ADDR	32	**MMU page rable base address** MMU page table base address in DRAM
10205004	MMU_PT_BASE_ADDR_SEC	32	**Secure MMU page table base address** MMU page table base address in DRAM
10205220	MMU_INT_CONTROL	32	**MMU interrupt control** Controls MMU interrupts.
10205224	MMU_FAULT_ST	32	**MMU interrupt status** Shows the status of the interrupts.
102055C0	MMU_INVALIDATE	32	**MMU invalidation enable** Triggers range or whole TLB invalidation.
102055C4	MMU_INVLD_START_A	32	**MMU range invalidation start address** Start address of range invalidation
102055C8	MMU_INVLD_END_A	32	**MMU range invalidation end address** End address of range invalidation
102055CC	MMU_INVALIDATE_SEC	32	**Secure MMU invalidation enable** Triggers range or full TLB invalidation.
102055D0	MMU_INVLD_START_A_SEC	32	**Secure MMU range invalidation start address** Start address of range invalidation

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Address	Name	Width	Register function
102055D4	MMU_INVLD_END_A_SEC	32	**Secure MMU range invalidation end address** End address of range invalidation
102055D8	MMU_INV_SEL	32	**MMU_INV_SEL** The selected TLB to be invalidated in the non-secure world.
102055DC	MMU_INV_SEL_SEC	32	**Secure MMU_INV_SEL** The selected TLB to be invalidated in the secure world.
102055F0	MMU_DCM	32	**MMU DCM control** Controls MMU DCM.

10205000 **MMU_PT_BASE_ADDR** **MMU Page Table Base Adderss** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
31:16	BADDR	BASE_ADDR	**Base address of page table** Alignment requirement: Size of page table Example: The 4MB page table size is needed for 4GB VA space. Therefore, 4MB alignment is required.

10205004 **MMU_PT_BASE_ADDR_SEC** **Secure MMU Page Table Base Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
31:16	BADDR	BASE_ADDR_SEC	**Base address of page table** Alignment requirement: Size of page table Example: The 4MB page table size is needed for 4GB VA space. Therefore, 4MB alignment is required.

10205220 **MMU_INT_CONTROL** **MMU Interrupt Control** **00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				MMUWEA1					MMUWSA2							
Type				Other					RW							
Reset				0					0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12	**MMUWEA1**	MMU_INT_CLR	**Clears interrupt** Write 1 to clear all interrupts in MMU.
7:0	**MMUWSA2**	MMU_INT_EN	**Interrupt enabling bits for MMU** [0]: Enable translation fault interrupt [1]: Enable TLB multi-hit interrupt [2]: Enable invalid physical address interrupt [3]: Enable entry replacement fault interrupt [4]: Enable table walk fault interrupt [5]: Enable TLB miss fault interrupt (while table walk logic is disabled) [6]: Enable pre-fetch DMA FIFO overflow interrupt [7]: Enable miss DMA FIFO overflow interrupt

10205224 **MMU_FAULT_ST** **MMU Interrupt Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MMUWEA2							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**MMUWEA2**	MMU_INT_STATUS	**Interrupt status** [0]: Translation fault [1]: TLB multi-hit fault [2]: Invalid physical address fault [3]: Entry replacement fault [4]: Table walk fault [5]: TLB miss fault (while table walk logic is disabled) [6]: Pre-fetch DMA FIFO overflow [7]: Miss DMA FIFO overflow

102055C0 **MMU_INVALIDATE** **MMU Invalidation Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FULL_INVLD	RANGE_INVLD
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1		FULL_INVLD	**Invalidates whole TLB entries** 0: No effect 1: Invalidate whole TLB entries
0		RANGE_INVLD	**Range Invalidation specified by RANGE_IVD_START_ADDR and RANGE_IVD_END_ADDR** 0: No effect 1: Invalidation address from RANGE_IVD_START_ADDR to RANGE_IVD_END_ADDR

102055C4 MMU_INVLD_START_A MMU Range Invalidation Start Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RIVDSA[19:4]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RIVDSA[3:0]															
Type	RW															
Reset	0	0	0	0												

Bit(s)	Mnemonic	Name	Description
31:12	**RIVDSA**	RANGE_IVD_START_ADDR	**Start address of range invalidation or auto-prefetch** The TLB entries with value that is bigger than or equal to the start address will be invalidated.

102055C8 MMU_INVLD_END_A MMU Range Invalidation End Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RIVDEA[19:4]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RIVDEA[3:0]															
Type	RW															
Reset	0	0	0	0												

Bit(s)	Mnemonic	Name	Description
31:12	**RIVDEA**	RANGE_IVD_END_ADDR	**End address of range invalidation or auto-prefetch** The TLB entries with value that is smaller than or equal to the end address will be invalidated.

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102055CC **MMU_INVALIDATE_SEC** **Secure MMU Invalidation Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**RANGE_INVLD_SEC**
Type																Other
Reset																0

Bit(s)	Mnemonic	Name	Description
0		RANGE_INVLD_SEC	**Range invalidation specified by RANGE_IVD_START_ADDR_SEC and RANGE_IVD_END_ADDR_SEC** 0: No effect 1: Invalidation address from RANGE_IVD_START_ADDR_SEC to RANGE_IVD_END_ADDR_SEC

102055D0 **MMU_INVLD_START_A_SEC** **Secure MMU Range Invalidation Start Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RIVDSA[19:4]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RIVDSA[3:0]**															
Type	RW															
Reset	0	0	0	0												

Bit(s)	Mnemonic	Name	Description
31:12	RIVDSA	RANGE_IVD_START_ADDR_SEC	**Start address of range invalidation or auto-prefetch** The TLB entries with value that is bigger than or equal to the start address will be invalidated.

102055D4 **MMU_INVLD_END_A_SEC** **Secure MMU Range Invalidation End Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RIVDEA[19:4]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RIVDEA[3:0]**															
Type	RW															
Reset	0	0	0	0												

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Bit(s)	Mnemonic	Name	Description
31:12	RIVDEA	RANGE_IVD_END_ADDR_SEC	**End address of range invalidation auto-prefetch** The TLB entries with value that is smaller than or equal to the end address will be invalidated.

102055D8 **MMU_INV_SEL** **MMU_INV_SEL** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												PREFETCH_EN			INVLD_EN1	INVLD_EN0
Type												Other			RW	RW
Reset												0			0	0

Bit(s)	Mnemonic	Name	Description
4		PREFETCH_EN	**Enables pre-fill L2** 1'b0: Normal operation 1'b1: Prefetch operation
1		INVLD_EN1	**L2 range invalidation and invalidate_all L2 selection bit** 0: Disable invalidation function 1: Enable invalidation function
0		INVLD_EN0	**MMU0 range invalidation and invalidation all TLB selection bit** 0: Disable invalidation function 1: Enable invalidation function

102055DC **MMU_INV_SEL_SEC** **SECURE MMU_INV_SEL** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												PREFETCH_EN_SEC			INVLD_EN1_SEC	INVLD_EN0_SEC
Type												Other			RW	RW
Reset												0			0	0

Bit(s)	Mnemonic	Name	Description
4		PREFETCH_EN_SEC	**Enables secure pre-fill L2** 1'b0: Normal operation 1'b1: Prefetch operation
1		INVLD_EN1_SEC	**L2 range invalidation and invalidation all TLB selection bit** 0: Disable invalidation function 1: Enable invalidation function

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Bit(s)	Mnemonic	Name	Description
0		INVLD_EN0_SEC	**MMU0 range invalidation and invalidation all TLB selection bit** 0: Disable invalidation function 1: Enable invalidation function

102055F0 **MMU_DCM** **MMU DCM Control** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MMU_DCM
Type																RW
Reset																1

Bit(s)	Mnemonic	Name	Description
0		MMU_DCM	**MMU DCM control** 1'b0: Clock will be always on. 1'b1: Clock will be gated when idle.

6.28.5 Programming Guide

1. Enable M4U for the corresponding ports (refer to the SMI_LARB/SMI_COMMON functional spec).
2. Request for a page table from the OS for the working address space.
3. Confirm the memory access behavior of each master.
4. Program the registers based on the master's memory-access behavior, e.g. set up the range sequential single-entry for the scan-line based masters then the range sequential multiple-entry and wrap mode for the rotators.
5. Set the pre-fetch distance to either "forward" or "backward" direction for the ports (default: forward 1).
6. Set up the page table base address.
7. Launch the engines.

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7 Analog Baseband

7.1 AP Mixedsys

7.1.1 Block Diagram

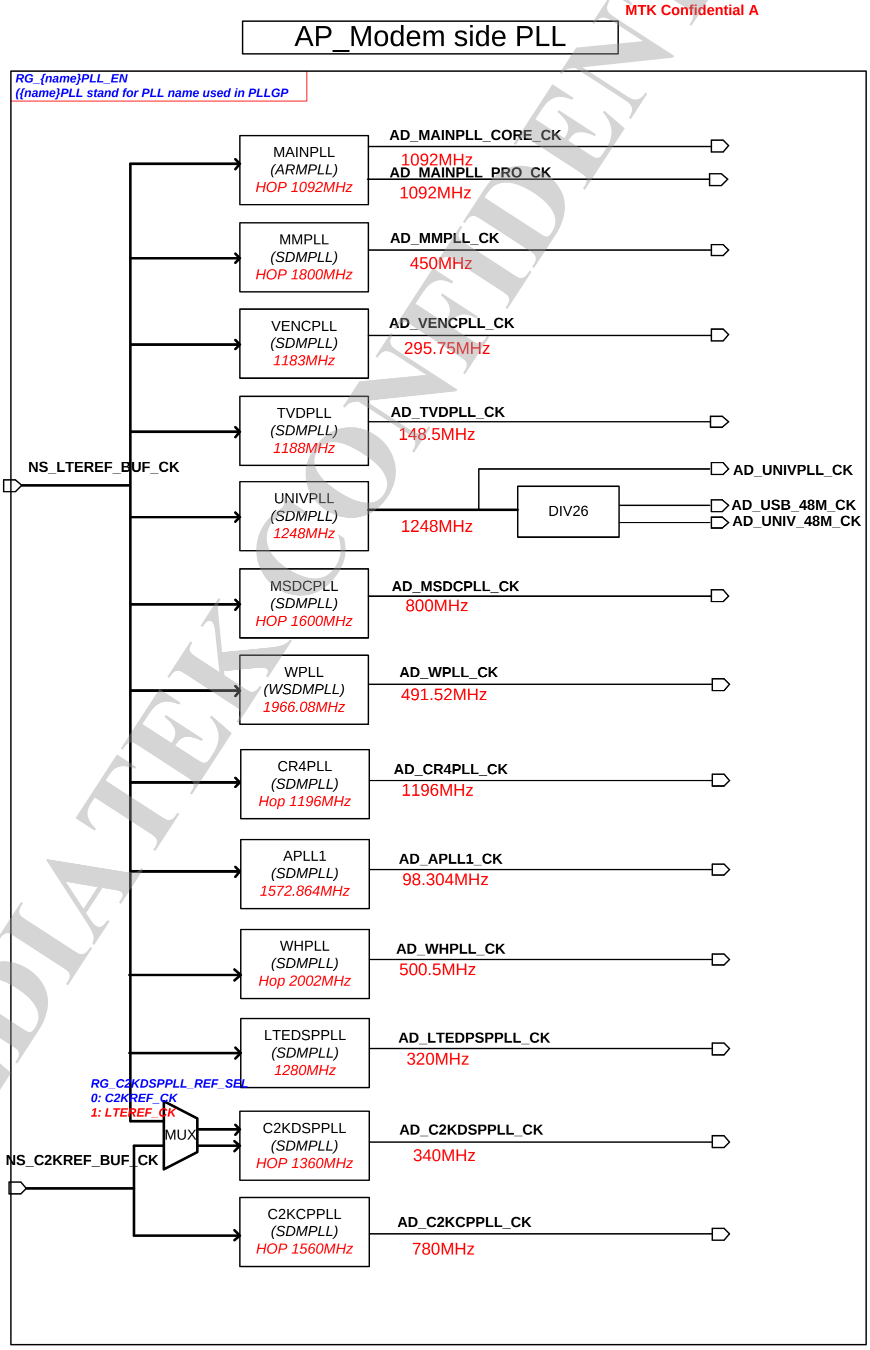

Figure 7-1. PLL block diagram

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7.1.2 Register Definition

Module name: APMIXEDSYS Base address: (+10209000h)

Address	Name	Width	Register Function
10209000	AP_PLL_CON0	32	AP PLL Control Register 0
10209004	AP_PLL_CON1	32	AP PLL Control Register 1
10209008	AP_PLL_CON2	32	AP PLL Control Register 2
1020900C	AP_PLL_CON3	32	AP PLL Control Register 3
10209010	AP_PLL_CON4	32	AP PLL Control Register 4
10209014	AP_PLL_CON5	32	AP PLL Control Register 5
10209040	PLL_TEST_CON0	32	PLL Test Control Register 0
10209044	PLL_TEST_CON1	32	PLL Test Control Register 1
10209200	ARMPLL_CON0	32	ARMPLL Control Register 0
10209204	ARMPLL_CON1	32	ARMPLL Control Register 1
1020920C	ARMPLL_PWR_CON0	32	ARMPLL Power Control Register 0
10209210	MAINPLL_CON0	32	MAINPLL Control Register 0
10209214	MAINPLL_CON1	32	MAINPLL Control Register 1
1020921C	MAINPLL_PWR_CON0	32	MAINPLL Power Control Register 0
10209220	UNIVPLL_CON0	32	UNIVPLL Control Register 0
10209224	UNIVPLL_CON1	32	UNIVPLL Control Register 1
1020922C	UNIVPLL_PWR_CON0	32	UNIVPLL Power Control Register 0
10209230	MMPLL_CON0	32	MMPLL Control Register 0
10209234	MMPLL_CON1	32	MMPLL Control Register 1
1020923C	MMPLL_PWR_CON0	32	MMPLL Power Control Register 0
10209240	MSDCPLL_CON0	32	MSDCPLL Control Register 0
10209244	MSDCPLL_CON1	32	MSDCPLL Control Register 1
1020924C	MSDCPLL_PWR_CON0	32	MSDCPLL Power Control Register 0
10209250	VENCPLL_CON0	32	VENCPLL Control Register 0
10209254	VENCPLL_CON1	32	VENCPLL Control Register 1
1020925C	VENCPLL_PWR_CON0	32	VENCPLL Power Control Register 0
10209260	TVDPLL_CON0	32	TVDPLL Control Register 0
10209264	TVDPLL_CON1	32	TVDPLL Control Register 1
1020926C	TVDPLL_PWR_CON0	32	TVDPLL Power Control Register 0
10209270	APLL1_CON0	32	APLL1 Control Register 0
10209274	APLL1_CON1	32	APLL1 Control Register 1
10209278	APLL1_CON2	32	APLL1 Control Register 2
10209280	APLL1_PWR_CON0	32	APLL1 Power Control Register 0
10209284	APLL2_CON0	32	APLL2 Control Register 0
10209288	APLL2_CON1	32	APLL2 Control Register 1
1020928C	APLL2_CON2	32	APLL2 Control Register 2
10209294	APLL2_PWR_CON0	32	APLL2 Power Control Register 0

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Address	Name	Width	Register Function
10209400	AP_AUXADC_CON0	32	AUXADC Control Register 0
10209404	AP_AUXADC_CON1	32	AUXADC Control Register 1
10209600	TS_CON0	32	Thermal Sensor Control Register 0
10209604	TS_CON1	32	Thermal Sensor Control Register 1

10209000 AP_PLL_CON0 AP PLL Control Register 0 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name													CLKSQ2_LPF_EN	CLKSQ2_EN	CLKSQ1_LPF_EN	CLKSQ1_EN
Type													RW	RW	RW	RW
Reset													0	0	0	1

Bit(s)	Mnemonic	Name	Description
3	CLKSQ2_LPF_EN	CLKSQ2_LPF_EN	Enables clock square2 low-pass filter
2	CLKSQ2_EN	CLKSQ2_EN	Enables clock square2
1	CLKSQ1_LPF_EN	CLKSQ1_LPF_EN	Enables clock square1 low-pass filter
0	CLKSQ1_EN	CLKSQ1_EN	Enables clock square1

10209004 AP_PLL_CON1 AP PLL Control Register 1 00040100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												CLKSQ2_HYS_SEL				
Type												RW				
Reset												0	0	1		
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name		CLKSQ2_MON_EN				CLKSQ1_HYS_SEL						CLKSQ1_MON_EN				
Type		RW				RW						RW				
Reset		0				0	0	1				0				

Bit(s)	Mnemonic	Name	Description
20:18	CLKSQ2_HYS_SEL	CLKSQ2_HYS_SEL	**Selects clock square hysteresis level**
14	CLKSQ2_MON_EN	CLKSQ2_MON_EN	**Enables clock square monitor** 0: Disable 1: Enable
10:8	CLKSQ1_H	CLKSQ1_HYS_SEL	**Selects clock square hysteresis level**

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Bit(s)	Mnemonic	Name	Description
	YS_SEL		
4	**CLKSQ1_MON_EN**	CLKSQ1_MON_EN	**Enables clock square monitor** 0: Disable 1: Enable

10209008 **AP_PLL_CON 2** **AP PLL Control Register 2** **00000A0E**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**APC2_SEL**	**APC1_SEL**	**C2KDSPPLL_REF_SEL**				**WHPLL_PS_CG_EN**		**MDPLL2_SEL**	**MDPLL2_CG_EN**	**WHPLL_SEL**
Type						RW	RW	RW				RW		RW	RW	RW
Reset						0	1	0				0	1	1	1	0

Bit(s)	Mnemonic	Name	Description
10		APC2_SEL	**APC2 switch for C2K and MD1** 0: MD3 (C2K) 1: MD1
9		APC1_SEL	**APC1 switch for C2K and MD1** 0: MD3 (C2K) 1: MD1
8		C2KDSPPLL_REF_SEL	**Selects C2KDSPPLL reference CLK** 0: C2KREF_CK 1: LTEREF_CK
4:3		WHPLL_PS_CG_EN	**[3]: For AD_WHPLL_CK_to_md1** [4]: For AD_WHPLL_CK_to_ap 0: Mask ck 1: Does not mask ck
2		MDPLL2_SEL	0: mdpll2 ctrl by MD1 1: mdpll2 ctrl by C2K
1		MDPLL2_CG_EN	0: Mask mdpll2 ck 1: Does not mask mdpll2 ck
0		WHPLL_SEL	0: whpll ctrl by MD1 1: whpll ctrl by AP

1020900C **AP_PLL_CON 3** **AP PLL Control Register 3** **0007777F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														**UNIVDIV_RSTB_SEL**	**MAINDIV_RSTB_SEL**	**VENCDIV_RSTB_SEL**
Type														RW	RW	RW
Reset														1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**UNIV**	**MAIN**	**ARM**		**UNIV**	**MAIN**	**ARM**		**UNIV**	**MAIN**	**ARM**	**CLKS**	**CLKS**	**CLKS**	**CLKS**

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		PLL_EN_SEL	PLL_EN_SEL	PLL_EN_SEL		PLL_ISO_SEL	PLL_ISO_SEL	PLL_ISO_SEL		PLL_PWR_SEL	PLL_PWR_SEL	PLL_PWR_SEL	Q2_LPF_EN_SEL	Q2_EN_SEL	Q1_LPF_EN_SEL	Q1_EN_SEL
Type		RW	RW	RW		RW	RW	RW		RW	RW	RW	RW	RW	RW	RW
Reset		1	1	1		1	1	1		1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
18	**UNIVDIV_RSTB_SEL**	UNIVDIV_RSTB_SEL	**Selects UNIVPLL DIV_RSTB control** 0: Sleep control 1: Register control
17	**MAINDIV_RSTB_SEL**	MAINDIV_RSTB_SEL	**Selects MAINPLL DIV_RSTB control** 0: Sleep control 1: Register control
16	**VENCDIV_RSTB_SEL**	VENCDIV_RSTB_SEL	**Selects VENCPLL DIV_RSTB control** 0: Sleep control 1: Register control
14	**UNIVPLL_EN_SEL**	UNIVPLL_EN_SEL	**Selects UNIVPLL enable control** 0: Sleep control 1: Register control
13	**MAINPLL_EN_SEL**	MAINPLL_EN_SEL	**Selects MAINPLL enable control** 0: Sleep control 1: Register control
12	**ARMPLL_EN_SEL**	ARMPLL_EN_SEL	**Selects ARMPLL enable control** 0: Sleep control 1: Register control
10	**UNIVPLL_ISO_SEL**	UNIVPLL_ISO_SEL	**Selects UNIVPLL ISO_EN control** 0: Sleep control 1: Register control
9	**MAINPLL_ISO_SEL**	MAINPLL_ISO_SEL	**Selects MAINPLL ISO_EN control** 0: Sleep control 1: Register control
8	**ARMPLL_ISO_SEL**	ARMPLL_ISO_SEL	**Selects ARMPLL ISO_EN control** 0: Sleep control 1: Register control
6	**UNIVPLL_PWR_SEL**	UNIVPLL_PWR_SEL	**Selects UNIVPLL PWR_ON control** 0: Sleep control 1: Register control
5	**MAINPLL_PWR_SEL**	MAINPLL_PWR_SEL	**Selects MAINPLL PWR_ON control** 0: Sleep control 1: Register control
4	**ARMPLL_PWR_SEL**	ARMPLL_PWR_SEL	**Selects ARMPLL PWR_ON control** 0: Sleep control 1: Register control
3	**CLKSQ2_LPF_EN_SEL**	CLKSQ2_LPF_EN_SEL	**Selects CLKSQ2 LPF_EN control** 0: Sleep control 1: Register control
2	**CLKSQ2_EN_SEL**	CLKSQ2_EN_SEL	**Selects CLKSQ2 enable control** 0: Sleep control 1: Register control
1	**CLKSQ1_LPF_EN_SEL**	CLKSQ1_LPF_EN_SEL	**Selects CLKSQ1 LPF_EN control** 0: Sleep control 1: Register control
0	**CLKSQ1_E**	CLKSQ1_EN_SEL	**Selects CLKSQ1 enable control**

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Bit(s)	Mnemonic	Name	Description
	N_SEL		0: Sleep control 1: Register control

10209010 **AP_PLL_CON4** **AP PLL Control Register 4** **00000007**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						UNIVPLL_OUT_OFF	MAINPLL_OUT_OFF	ARMPLL_OUT_OFF						UNIVPLL_OUT_OFF_SEL	MAINPLL_OUT_OFF_SEL	ARMPLL_OUT_OFF_SEL
Type						RW	RW	RW						RW	RW	RW
Reset						0	0	0						1	1	1

Bit(s)	Mnemonic	Name	Description
10	UNIVPLL_OUT_OFF	UNIVPLL_OUT_OFF	**Controls UNIVPLL CG register**
9	MAINPLL_OUT_OFF	MAINPLL_OUT_OFF	**Controls MAINPLL CG register**
8	ARMPLL_OUT_OFF	ARMPLL_OUT_OFF	**Controls ARMPLL CG register**
2	UNIVPLL_OUT_OFF_SEL	UNIVPLL_OUT_OFF_SEL	**Selects UNIVPLL CG control** 0: Sleep control 1: Register control
1	MAINPLL_OUT_OFF_SEL	MAINPLL_OUT_OFF_SEL	**Selects MAINPLL CG control** 0: Sleep control 1: Register control
0	ARMPLL_OUT_OFF_SEL	ARMPLL_OUT_OFF_SEL	**Selects ARMPLL CG control** 0: Sleep control 1: Register control

10209014 **AP_PLL_CON5** **AP PLL Control Register 5** **000000FC**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										MDPLL2_FS26M_CK	MDPLL1_ARM26M_CK_EN	MDPLL1_MEM26M_CK_EN	MDPLL1_MIPI26M_CK_EN	MDPLL1_FS26M_CK_EN	APLL2_TUNER_EN	APLL1_TUNER_EN
Type										RW	RW	RW	RW	RW	RW	RW
Reset										1	1	1	1	1	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
6		MDPLL2_FS26M_CK	Enables MDPLL2 FS 26MHz clock source
5		MDPLL1_ARM26M_CK_EN	Enables ARM 26MHz clock source
4		MDPLL1_MEM26M_CK_EN	Enables MEM 26MHz clock source
3		MDPLL1_MIPI26M_CK_EN	Enables MIPI 26MHz clock source
2		MDPLL1_FS26M_CK_EN	Enables FS 26MHz clock source
1		APLL2_TUNER_EN	Enable APLL2 tuning function
0		APLL1_TUNER_EN	Enable APLL1 tuning function

10209040 **PLL_TEST_CON0** **PLL Test Control Register 0** **FF000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PLLGP_RESERVE															
Type	RW															
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name		PLLGP_LTEREF_MON_CK_EN	PLLGP_C2KREF_MON_CK_EN		PLLGP_MONREF_EN	PLLGP_LVROD_EN	PLLGP_TST_SEL		PLLGP_TSTMUX				PLLGP_TSTOD_EN	PLLGP_A2DCK_EN	PLLGP_TSTCK_EN	PLLGP_TST_EN
Type		RW	RW		RW	RW	RW		RW				RW	RW	RW	RW
Reset		0	0		0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16	**PLLGP_RESERVE**	PLLGP_RESERVE	
14	**PLLGP_LTEREF_MON_CK_EN**	PLLGP_LTEREF_MON_CK_EN	Enables REF_CK monitor
13	**PLLGP_C2KREF_MON_CK_EN**	PLLGP_C2KREF_MON_CK_EN	Enables REF_CK monitor
11	**PLLGP_MONREF_EN**	PLLGP_MONREF_EN	Enables FBK clock testing mode
10	**PLLGP_LVROD_EN**	PLLGP_LVROD_EN	Overdrive open drain LDO
9:8	**PLLGP_TST_SEL**	PLLGP_TST_SEL	Selects test mux
7:4	**PLLGP_TSTMUX**	PLLGP_TSTMUX	Selects test mux
3	**PLLGP_TSTOD_EN**	PLLGP_TSTOD_EN	Enables open drain
2	**PLLGP_A2DCK_EN**	PLLGP_A2DCK_EN	Enables frequency meter path

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Bit(s)	Mnemonic	Name	Description
1	**PLLGP_TSTCK_EN**	PLLGP_TSTCK_EN	Enables PLL output clock testing mode
0	**PLLGP_TST_EN**	PLLGP_TST_EN	Enables testing mode

10209044 **PLL_TEST_CON1** **PLL Test Control Register 1** **FF000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ARMPLL_TOP_RESERVE															
Type	RW															
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name			ARMPLL_TOP_REF_MON_CK_EN		ARMPLL_TOP_MONREF_EN	ARMPLL_TOP_LVROD_EN	ARMPLL_TOP_TST_SEL		ARMPLL_TOP_TSTMUX				ARMPLL_TOP_TSTOD_EN	ARMPLL_TOP_A2DCK_EN	ARMPLL_TOP_TSTCK_EN	ARMPLL_TOP_TST_EN
Type			RW		RW	RW	RW		RW				RW	RW	RW	RW
Reset			0		0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16	**ARMPLL_TOP_RESERVE**	ARMPLL_TOP_RESERVE	
13	**ARMPLL_TOP_REF_MON_CK_EN**	ARMPLL_TOP_REF_MON_CK_EN	Enables REF_CK monitor
11	**ARMPLL_TOP_MONREF_EN**	ARMPLL_TOP_MONREF_EN	Enables REF_CK monitor
10	**ARMPLL_TOP_LVROD_EN**	ARMPLL_TOP_LVROD_EN	Overdrive open drain LDO
9:8	**ARMPLL_TOP_TST_SEL**	ARMPLL_TOP_TST_SEL	Selects test mux
7:4	**ARMPLL_TOP_TSTMUX**	ARMPLL_TOP_TSTMUX	Selects test mux
3	**ARMPLL_TOP_TSTOD_EN**	ARMPLL_TOP_TSTOD_EN	Enables open drain
2	**ARMPLL_TOP_A2DCK_EN**	ARMPLL_TOP_A2DCK_EN	Enables frequency meter path
1	**ARMPLL_TOP_TSTCK_EN**	ARMPLL_TOP_TSTCK_EN	Enables PLL output clock testing mode
0	**ARMPLL_TOP_TST_EN**	ARMPLL_TOP_TST_EN	Enables testing mode

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10209200 **ARMPLL_CON0** **ARMPLL Control Register 0** **00000100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**ARMPLL_SDM_FRA_EN**								**ARMPLL_EN**
Type								RW								RW
Reset								1								0

Bit(s)	Mnemonic	Name	Description
8	**ARMPLL_SDM_FRA_EN**	ARMPLL_SDM_FRA_EN	**Enables SDMPLL fractional mode** 0: Integer mode 1: Fractional mode
0	**ARMPLL_EN**	ARMPLL_EN	**Enables PLL**

10209204 **ARMPLL_CON1** **ARMPLL Control Register 1** **800C8000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**ARMPLL_SDM_PCW_CHG**					**ARMPLL_POSDIV**						**ARMPLL_SDM_PCW[20:16]**				
Type	RW					RW						RW				
Reset	1					0	0	0				0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ARMPLL_SDM_PCW[15:0]**															
Type	RW															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**ARMPLL_SDM_PCW_CHG**	ARMPLL_SDM_PCW_CHG	**Feedback divide ratio update signal**
26:24	**ARMPLL_POSDIV**	ARMPLL_POSDIV	**Post divide ratio** 000: /1 001: /2 010: /4 011: /8 100: /16
20:0	**ARMPLL_SDM_PCW**	ARMPLL_SDM_PCW	**Feedback divide ratio**

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1020920C **ARMPLL_PWR_CON0** **ARMPLL Power Control Register 0** **00000002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ARMPLL_SDM_PWR_ACK															
Type	RO															
Reset	0															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name															ARMPLL_SDM_ISO_EN	ARMPLL_SDM_PWR_ON
Type															RW	RW
Reset															1	0

Bit(s)	Mnemonic	Name	Description
31	ARMPLL_SDM_PWR_ACK	ARMPLL_SDM_PWR_ACK	ARMPLL power ack
1	ARMPLL_SDM_ISO_EN	ARMPLL_SDM_ISO_EN	Enables ARMPLL ISO
0	ARMPLL_SDM_PWR_ON	ARMPLL_SDM_PWR_ON	ARMPLL power-on

10209210 **MAINPLL_CON0** **MAINPLL Control Register 0** **F0000100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAINPLL_DIV2_EN	MAINPLL_DIV3_EN	MAINPLL_DIV5_EN	MAINPLL_DIV7_EN				MAINPLL_DIV_RSTB								
Type	RW	RW	RW	RW				RW								
Reset	1	1	1	1				0								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name								MAINPLL_SDM_FRA_EN								MAINPLL_EN
Type								RW								RW
Reset								1								0

Bit(s)	Mnemonic	Name	Description
31	MAINPLL_DIV2_EN	MAINPLL_DIV2_EN	**Enables MAINPLL DIV2**
30	MAINPLL_DIV3_EN	MAINPLL_DIV3_EN	**Enables MAINPLL DIV3**
29	MAINPLL_DIV5_EN	MAINPLL_DIV5_EN	**Enables MAINPLL DIV5**

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Bit(s)	Mnemonic	Name	Description
28	**MAINPLL_DIV7_EN**	MAINPLL_DIV7_EN	**Enables MAINPLL DIV7**
24	**MAINPLL_DIV_RSTB**	MAINPLL_DIV_RSTB	**PLL divider reset bar** 0: Reset 1: Enable
8	**MAINPLL_SDM_FRA_EN**	MAINPLL_SDM_FRA_EN	**Enables SDMPLL fractional mode** 0: Integer mode 1: Fractional mode
0	**MAINPLL_EN**	MAINPLL_EN	**Enables PLL**

10209214 **MAINPLL_CON1** **MAINPLL Control Register 1** **800A8000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAINPLL_SDM_PCW_CHG					MAINPLL_POSDIV						MAINPLL_SDM_PCW[20:16]				
Type	RW					RW						RW				
Reset	1					0	0	0				0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAINPLL_SDM_PCW[15:0]															
Type	RW															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**MAINPLL_SDM_PCW_CHG**	MAINPLL_SDM_PCW_CHG	**Feedback divide ratio update signal**
26:24	**MAINPLL_POSDIV**	MAINPLL_POSDIV	**Post divide ratio** 000: /1 001: /2 010: /4 011: /8 100: /16
20:0	**MAINPLL_SDM_PCW**	MAINPLL_SDM_PCW	**Feedback divide ratio**

1020921C **MAINPLL_PWR_CON0** **MAINPLL Power Control Register 0** **00000002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAINPLL_SDM_PWR_ACK															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															MAIN	MAIN

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Bit																
															PLL_SDM_ISO_EN	PLL_SDM_PWR_ON
Type															RW	RW
Reset															1	0

Bit(s)	Mnemonic	Name	Description
31	**MAINPLL_SDM_PWR_ACK**	MAINPLL_SDM_PWR_ACK	MAINPLL power ack
1	**MAINPLL_SDM_ISO_EN**	MAINPLL_SDM_ISO_EN	Enables MAINPLL ISO
0	**MAINPLL_SDM_PWR_ON**	MAINPLL_SDM_PWR_ON	MAINPLL power-on

10209220 **UNIVPLL_CON0** **UNIVPLL Control Register 0** **FC000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	UNIVPLL_DIV2_EN	UNIVPLL_DIV3_EN	UNIVPLL_DIV5_EN	UNIVPLL_DIV7_EN	UNIV48M_EN	USB48M_EN		UNIVPLL_DIV_RSTB								
Type	RW	RW	RW	RW	RW	RW		RW								
Reset	1	1	1	1	1	1		0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								UNIVPLL_SDM_FRA_EN								UNIVPLL_EN
Type								RW								RW
Reset								0								0

Bit(s)	Mnemonic	Name	Description
31	**UNIVPLL_DIV2_EN**	UNIVPLL_DIV2_EN	**Enables UNIVPLL DIV2**
30	**UNIVPLL_DIV3_EN**	UNIVPLL_DIV3_EN	**Enables UNIVPLL DIV3**
29	**UNIVPLL_DIV5_EN**	UNIVPLL_DIV5_EN	**Enables UNIVPLL DIV5**
28	**UNIVPLL_DIV7_EN**	UNIVPLL_DIV7_EN	**Enables UNIVPLL DIV7**
27	**UNIV48M_EN**	UNIV48M_EN	**Enables UNIV 48M clock**
26	**USB48M_EN**	USB48M_EN	**Enables USB 48M clock**
24	**UNIVPLL_DIV_RSTB**	UNIVPLL_DIV_RSTB	**PLL divider reset bar** 0: Reset 1: Enable
8	**UNIVPLL_SDM_FRA_EN**	UNIVPLL_SDM_FRA_EN	**Enables SDMPLL fractional mode** 0: Integer mode 1: Fractional mode

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Bit(s)	Mnemonic	Name	Description
0	UNIVPLL_EN	UNIVPLL_EN	**Enables PLL**

10209224 UNIVPLL_CON1 UNIVPLL Control Register 1 800C0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	UNIVPLL_SDM_PCW_CHG					UNIVPLL_POSDIV						UNIVPLL_SDM_PCW[6:2]				
Type	RW					RW						RW				
Reset	1					0	0	0				0	1	1	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	UNIVPLL_SDM_PCW[1:0]															
Type	RW															
Reset	0	0														

Bit(s)	Mnemonic	Name	Description
31	UNIVPLL_SDM_PCW_CHG	UNIVPLL_SDM_PCW_CHG	**Feedback divide ratio update signal**
26:24	UNIVPLL_POSDIV	UNIVPLL_POSDIV	**Post divide ratio** 000: /1 001: /2 010: /4 011: /8 100: /16
20:14	UNIVPLL_SDM_PCW	UNIVPLL_SDM_PCW	**Feedback divide ratio**

1020922C UNIVPLL_PWR_CON0 UNIVPLL Power Control Register 0 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	UNIVPLL_SDM_PWR_ACK															
Type	RO															
Reset	0															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name															UNIVPLL_SDM_ISO_EN	UNIVPLL_SDM_PWR_ON
Type															RW	RW
Reset															1	0

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Bit(s)	Mnemonic	Name	Description
31	**UNIVPLL_SDM_PWR_ACK**	UNIVPLL_SDM_PWR_ACK	UNIVPLL power ack
1	**UNIVPLL_SDM_ISO_EN**	UNIVPLL_SDM_ISO_EN	Enables UNIVPLL ISO
0	**UNIVPLL_SDM_PWR_ON**	UNIVPLL_SDM_PWR_ON	UNIVPLL power-on

10209230 **MMPLL_CON0** **MMPLL Control Register 0** **00000100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MMPLL_SDM_FRA_EN								MMPLL_EN
Type								RW								RW
Reset								1								0

Bit(s)	Mnemonic	Name	Description
8	**MMPLL_SDM_FRA_EN**	MMPLL_SDM_FRA_EN	**Enables SDMPLL fractional mode** 0: Integer mode 1: Fractional mode
0	**MMPLL_EN**	MMPLL_EN	**Enables PLL**

10209234 **MMPLL_CON1** **MMPLL Control Register 1** **82114EC5**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMPLL_SDM_PCW_CHG					MMPLL_POSDIV						MMPLL_SDM_PCW[20:16]				
Type	RW					RW						RW				
Reset	1					0	1	0				1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MMPLL_SDM_PCW[15:0]															
Type	RW															
Reset	0	1	0	0	1	1	1	0	1	1	0	0	0	1	0	1

Bit(s)	Mnemonic	Name	Description
31	**MMPLL_SDM_PCW_CHG**	MMPLL_SDM_PCW_CHG	**Feedback divide ratio update signal**
26:24	**MMPLL_P**	MMPLL_POSDIV	**Post divide ratio**

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Bit(s)	Mnemonic	Name	Description
	OSDIV		000: /1 001: /2 010: /4 011: /8 100: /16
20:0	**MMPLL_SDM_PCW**	MMPLL_SDM_PCW	**Feedback divide ratio**

1020923C **MMPLL_PWR_CON0** **MMPLL Power Control Register 0** **00000002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMPLL_SDM_PWR_ACK															
Type	RO															
Reset	0															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name															MMPLL_SDM_ISO_EN	MMPLL_SDM_PWR_ON
Type															RW	RW
Reset															1	0

Bit(s)	Mnemonic	Name	Description
31	**MMPLL_SDM_PWR_ACK**	MMPLL_SDM_PWR_ACK	MMPLL power ack
1	**MMPLL_SDM_ISO_EN**	MMPLL_SDM_ISO_EN	Enables MMPLL ISO
0	**MMPLL_SDM_PWR_ON**	MMPLL_SDM_PWR_ON	MMPLL power-on

10209240 **MSDCPLL_CON0** **MSDCPLL Control Register 0** **00000100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name								MSDCPLL_SDM_FRA_EN								MSDCPLL_EN
Type								RW								RW
Reset								1								0

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Bit(s)	Mnemonic	Name	Description
8	MSDCPLL_SDM_FRA_EN	MSDCPLL_SDM_FRA_EN	**Enables SDMPLL fractional mode** 0: Integer mode 1: Fractional mode
0	MSDCPLL_EN	MSDCPLL_EN	**Enables PLL**

10209244 **MSDCPLL_CON1** **MSDCPLL Control Register 1** **810F6276**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MSDCPLL_SDM_PCW_CHG					MSDCPLL_POSDIV						MSDCPLL_SDM_PCW[20:16]				
Type	RW					RW						RW				
Reset	1					0	0	1				0	1	1	1	1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDCPLL_SDM_PCW[15:0]															
Type	RW															
Reset	0	1	1	0	0	0	1	0	0	1	1	1	0	1	1	0

Bit(s)	Mnemonic	Name	Description
31	MSDCPLL_SDM_PCW_CHG	MSDCPLL_SDM_PCW_CHG	**Feedback divide ratio update signal**
26:24	MSDCPLL_POSDIV	MSDCPLL_POSDIV	**Post divide ratio** 000: /1 001: /2 010: /4 011: /8 100: /16
20:0	MSDCPLL_SDM_PCW	MSDCPLL_SDM_PCW	**Feedback divide ratio**

1020924C **MSDCPLL_PWR_CON0** **MSDCPLL Power Control Register 0** **00000002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MSDCPLL_SDM_PWR_ACK															
Type	RO															
Reset	0															

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															MSDCPLL_SDM_ISO_EN	MSDCPLL_SDM_PWR_ON
Type															RW	RW
Reset															1	0

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Bit(s)	Mnemonic	Name	Description
31	MSDCPLL_SDM_PWR_ACK	MSDCPLL_SDM_PWR_ACK	**MSDCPLL power ack**
1	MSDCPLL_SDM_ISO_EN	MSDCPLL_SDM_ISO_EN	**Enables MSDCPLL ISO**
0	MSDCPLL_SDM_PWR_ON	MSDCPLL_SDM_PWR_ON	**MSDCPLL power-on**

10209250 VENCPLL_CON0 VENCPLL Control Register 0 F0000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VENCPLL_DIV2_EN	VENCPLL_DIV3_EN	VENCPLL_DIV5_EN	VENCPLL_DIV7_EN				VENCPLL_DIV_RSTB	VENCPLL_CKOUT_ON							
Type	RW	RW	RW	RW				RW	RW							
Reset	1	1	1	1				0	0							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name								VENCPLL_SDM_FRA_EN								VENCPLL_EN
Type								RW								RW
Reset								1								0

Bit(s)	Mnemonic	Name	Description
31	VENCPLL_DIV2_EN	VENCPLL_DIV2_EN	**Enables VENCPLL DIV2**
30	VENCPLL_DIV3_EN	VENCPLL_DIV3_EN	**Enables VENCPLL DIV3**
29	VENCPLL_DIV5_EN	VENCPLL_DIV5_EN	**Enables VENCPLL DIV5**
28	VENCPLL_DIV7_EN	VENCPLL_DIV7_EN	**Enables VENCPLL DIV7**
24	VENCPLL_DIV_RSTB	VENCPLL_DIV_RSTB	**PLL divider reset bar** 0: Reset 1: Enable
23	VENCPLL_CKOUT_ON	VENCPLL_CKOUT_ON	0: Disable 1: Enable
8		VENCPLL_SDM_FRA_EN	**Enables SDMPLL fractional mode** 0: Integer mode 1: Fractional mode
0		VENCPLL_EN	**Enables PLL**

10209254 VENCPLL_CO VENCPLL Control Register 1 820B6000

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N1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VENCPLL_SDM_PCW_CHG					VENCPLL_POSDIV						VENCPLL_SDM_PCW[20:16]				
Type	RW					RW						RW				
Reset	1					0	1	0				0	1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VENCPLL_SDM_PCW[15:0]															
Type	RW															
Reset	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		VENCPLL_SDM_PCW_CHG	**Feedback divide ratio update signal**
26:24		VENCPLL_POSDIV	**Post divide ratio** 000: /1 001: /2 010: /4 011: /8 100: /16 Others: Clock gating
20:0		VENCPLL_SDM_PCW	**Feedback divide ratio**

1020925C **VENCPLL_PWR_CON0** **VENCPLL Power Control Register 0** **00000002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VENCPLL_SDM_PWR_ACK															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															VENCPLL_SDM_ISO_EN	VENCPLL_SDM_PWR_ON
Type															RW	RW
Reset															1	0

Bit(s)	Mnemonic	Name	Description
31		VENCPLL_SDM_PWR_ACK	VENCPLL power ack
1		VENCPLL_SDM_ISO_EN	Enables VENCPLL ISO
0		VENCPLL_SDM_PWR_ON	VENCPLL power-on

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10209260 **TVDPLL_CON0** **TVDPLL Control Register 0** **00000100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TVDPLL_SDM_FRA_EN								TVDPLL_EN
Type								RW								RW
Reset								1								0

Bit(s)	Mnemonic	Name	Description
8	**TVDPLL_SDM_FRA_EN**	TVDPLL_SDM_FRA_EN	**Enables SDMPLL fractional mode** 0: Integer mode 1: Fractional mode
0	**TVDPLL_EN**	TVDPLL_EN	**Enables PLL**

10209264 **TVDPLL_CON1** **TVDPLL Control Register 1** **830B6C4F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TVDPLL_SDM_PCW_CHG					TVDPLL_POSDIV						TVDPLL_SDM_PCW[20:16]				
Type	RW					RW						RW				
Reset	1					0	1	1				0	1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TVDPLL_SDM_PCW[15:0]															
Type	RW															
Reset	0	1	1	0	1	1	0	0	0	1	0	0	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**TVDPLL_SDM_PCW_CHG**	TVDPLL_SDM_PCW_CHG	**Feedback divide ratio update signal**
26:24	**TVDPLL_POSDIV**	TVDPLL_POSDIV	**Post divide ratio** 000: /1 001: /2 010: /4 011: /8 100: /16
20:0	**TVDPLL_SDM_PCW**	TVDPLL_SDM_PCW	**Feedback divide ratio**

1020926C **TVDPLL_PWR** **TVDPLL Power Control Register 0** **00000002**

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_CON0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**TVDPLL_SDM_PWR_ACK**															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**TVDPLL_SDM_ISO_EN**	**TVDPLL_SDM_PWR_ON**
Type															RW	RW
Reset															1	0

Bit(s)	Mnemonic	Name	Description
31	**TVDPLL_SDM_PWR_ACK**	TVDPLL_SDM_PWR_ACK	TVDPLL power ack
1	**TVDPLL_SDM_ISO_EN**	TVDPLL_SDM_ISO_EN	Enables TVDPLL ISO
0	**TVDPLL_SDM_PWR_ON**	TVDPLL_SDM_PWR_ON	TVDPLL power-on

10209270 APLL1_CON0 APLL1 Control Register 0 00000140

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**APLL1_SDM_FRA_EN**		**APLL1_POSDIV**						**APLL1_EN**
Type								RW		RW						RW
Reset								1		1	0	0				0

Bit(s)	Mnemonic	Name	Description
8		APLL1_SDM_FRA_EN	**Enables SDMPLL fractional mode** 0: Integer mode 1: Fractional mode
6:4		APLL1_POSDIV	**Post divide ratio** 000: /1 001: /2 010: /4 011: /8 100: /16
0		APLL1_EN	**Enables PLL**

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10209274 APLL1_CON1 APLL1 Control Register 1 BC7EA932

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	APLL1_SDM_PCW_CHG	APLL1_SDM_PCW[30:16]														
Type	RW	RW														
Reset	1	0	1	1	1	1	0	0	0	1	1	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	APLL1_SDM_PCW[15:0]															
Type	RW															
Reset	1	0	1	0	1	0	0	1	0	0	1	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
31		APLL1_SDM_PCW_CHG	Feedback divide ratio update signal
30:0		APLL1_SDM_PCW	Feedback divide ratio

10209278 APLL1_CON2 APLL1 Control Register 2 3C7EA932

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		APLL1_TUNER_SDM_PCW[30:16]														
Type		RW														
Reset		0	1	1	1	1	0	0	0	1	1	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	APLL1_TUNER_SDM_PCW[15:0]															
Type	RW															
Reset	1	0	1	0	1	0	0	1	0	0	1	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
30:0		APLL1_TUNER_SDM_PCW	Feedback divide ratio

10209280 APLL1_PWR_CON0 APLL1 Power Control Register 0 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	APLL1_SDM_PWR_ACK															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															APLL1_SDM_ISO_EN	APLL1_SDM_PWR_ON
Type															RW	RW
Reset															1	0

Bit(s)	Mnemonic	Name	Description
31		APLL1_SDM_PWR	APLL1 power ack

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Bit(s)	Mnemonic	Name	Description
		_ACK	
1		APLL1_SDM_ISO_EN	Enables APLL1 ISO
0		APLL1_SDM_PWR_ON	APLL1 power-on

10209284 APLL2_CON0 APLL2 Control Register 0 00000140

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name								APLL2_SDM_FRA_EN		APLL2_POSDIV						APLL2_EN
Type								RW		RW						RW
Reset								1		1	0	0				0

Bit(s)	Mnemonic	Name	Description
8		APLL2_SDM_FRA_EN	**Enables SDMPLL fractional mode** 0: Integer mode 1: Fractional mode
6:4		APLL2_POSDIV	**Post divide ratio** 000: /1 001: /2 010: /4 011: /8 100: /16
0		APLL2_EN	**Enables PLL**

10209288 APLL2_CON1 APLL2 Control Register 1 B7945EA6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	APLL2_SDM_PCW_CHG	APLL2_SDM_PCW[30:16]														
Type	RW	RW														
Reset	1	0	1	1	0	1	1	1	1	0	0	1	0	1	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	APLL2_SDM_PCW[15:0]															
Type	RW															
Reset	0	1	0	1	1	1	1	0	1	0	1	0	0	1	1	0

Bit(s)	Mnemonic	Name	Description
31		APLL2_SDM_PCW_CHG	Feedback divide ratio update signal
30:0		APLL2_SDM_PCW	Feedback divide ratio

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1020928C APLL2_CON2 APLL2 Control Register 2 37945EA6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		APLL2_TUNER_SDM_PCW[30:16]														
Type		RW														
Reset		0	1	1	0	1	1	1	1	0	0	1	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	APLL2_TUNER_SDM_PCW[15:0]															
Type	RW															
Reset	0	1	0	1	1	1	1	0	1	0	1	0	0	1	1	0

Bit(s)	Mnemonic	Name	Description
30:0		APLL2_TUNER_SDM_PCW	Feedback divide ratio

10209294 APLL2_PWR_CON0 APLL2 Power Control Register 0 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	APLL2_SDM_PWR_ACK															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															APLL2_SDM_ISO_EN	APLL2_SDM_PWR_ON
Type															RW	RW
Reset															1	0

Bit(s)	Mnemonic	Name	Description
31		APLL2_SDM_PWR_ACK	APLL2 power ack
1		APLL2_SDM_ISO_EN	Enables APLL2 ISO
0		APLL2_SDM_PWR_ON	APLL2 power-on

10209400 AP_AUXADC_CON0 AUXADC Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AUXADC_RSV															
Type	RW															
Reset	0	0	0	0	0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												AUXADC_FS	AUXADC_CALI			
Type												RW	RW			
Reset												0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31:24	**AUXADC_RSV**	AUXADC_RSV	**Reserved**
4	**AUXADC_FS**	AUXADC_FS	
3:0	**AUXADC_CALI**	AUXADC_CALI	**ADC core bias current calibration** 0000: 1X 0001: 1.25X 0010: 1.5X 0011: 1.75X 0100: 2X 1000: 1X 1001: 0.8X 1010: 0.67X 1011: 0.57X 1100: 0.5X

10209404 **AP_AUXADC_CON1** **AUXADC Control Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		AUXIN2_SMT	AUXIN1_SMT	AUXIN0_SMT		AUXIN2_PD	AUXIN1_PD	AUXIN0_PD		AUXIN2_PU	AUXIN1_PU	AUXIN0_PU		AUXIN2_GEN	AUXIN1_GEN	AUXIN0_GEN
Type		RW	RW	RW		RW	RW	RW		RW	RW	RW		RW	RW	RW
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
14	**AUXIN2_SMT**	AUXIN2_SMT	
13	**AUXIN1_SMT**	AUXIN1_SMT	
12	**AUXIN0_SMT**	AUXIN0_SMT	
10	**AUXIN2_PD**	AUXIN2_PD	
9	**AUXIN1_PD**	AUXIN1_PD	
8	**AUXIN0_PD**	AUXIN0_PD	
6	**AUXIN2_PU**	AUXIN2_PU	
5	**AUXIN1_PU**	AUXIN1_PU	
4	**AUXIN0_PU**	AUXIN0_PU	
2	**AUXIN2_GEN**	AUXIN2_GEN	
1	**AUXIN1_GEN**	AUXIN1_GEN	
0	**AUXIN0_GEN**	AUXIN0_GEN	

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Bit(s)	Mnemonic	Name	Description
	EN		

10209600 TS_CON0 Thermal Sensor Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BGR_RSV								BGR_TCTRL							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BGR_CTRL				BGR_RSEL							BGR_UGB	BGR_BUFIN	BGR_FSETUP	BGR_UNCHOP_PH	BGR_UNCHOP
Type	RW				RW							RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**BGR_RSV**	BGR_RSV	**RG_BGR_RSV[7:1]: Reserved register** RG_BGR_RSV[0]: Enable VBGR output to PAD_TESTIIN 0: Disable 1: Enable
23:16	**BGR_TCTRL**	BGR_TCTRL	**BGR_TCTRL[1:0]: BGR Replica VBE TSensor chopping control** 00: Unchop, PH = 0 01: Unchop, PH = 1 10: Chop 11: Disable The current for VBE TSensor is also as the reference of calibrating VBE TSensor for 00/01/10 mode. By setting RG_BGR_CTRL[3]=1 and RG_BGR_TCTRL[1:0]=11,the current source of calibrating VBE can be applied externally (drawn from PD_TESTIIN). BGR_TCTRL[3:2]: PAD_TSOUT output selection 00: Disable TSOUT 01: IPTAT_OUT (for VBE calibration) 10: VBE_MCU 11: VBE_ABB RG_BGR_TCTRL[7:4]: IPTAT VBE TSensor current selection 0000: 100000000 for 1I calibrating VBE 0001: 010000000 for 1I calibrating VBE 0010: 001000000 for 1I calibrating VBE 0011: 000100000 for 1I calibrating VBE 0100: 000010000 for 1I calibrating VBE 0101: 000001000 for 1I calibrating VBE 0110: 000000100 for 1I calibrating VBE 0111: 000000010 for 1I calibrating VBE 1000: 000000001 for 1I calibrating VBE 1001: 111000000 for 3I calibrating VBE 1010: 000111000 for 3I calibrating VBE 1011: 000000111 for 3I calibrating VBE 1100: 111111111 for 9I calibrating VBE
15:12	**BGR_CTRL**	BGR_CTRL	**RG_BGR_CTRL[2:0]: BGR resistor selection for denomerator** RG_BGR_CTRL[3]: Enable test current input 0: Disable test current 1: Enable test current. In this mode, PAD_TESTIIN is used for

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Bit(s)	Mnemonic	Name	Description
			applying calibrating VBE TSensor current. (see RG_BGR_TCTRL[1:0].)
11:8	**BGR_RSEL**	BGR_RSEL	**Selects BGR resistor for numerator**
4	**BGR_UGB**	BGR_UGB	**BGR VBUFFER force unity gain mode** 0: Disable 1: Enable
3	**BGR_BUFIN**	BGR_BUFIN	**BGR VBUFFER external input mode** 0: Disable 1: Enable
2	**BGR_FSETUP**	BGR_FSETUP	**BGR fast setup control** 0: Disable resistor in low pass filter, speed up settling 1: Enable low pass filter
1	**BGR_UNCHOP_PH**	BGR_UNCHOP_PH	**Selects BGR unchop mode phase**
0	**BGR_UNCHOP**	BGR_UNCHOP	**BGR unchop mode** 0: Chop 1: Unchop

10209604 TS_CON1 Thermal Sensor Control Register 1 00000030

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name											TS2AUXADC			VBE_SEL		
Type											RW			RW		
Reset											1	1		0	0	0

Bit(s)	Mnemonic	Name	Description
5:4	**TS2AUXADC**	TS2AUXADC	**Enables output buffer and selects TS output to AUXADC** 00: Buffer on, TSMCU to AUXADC 01: Buffer on, TSABB to AUXADC 10: Buffer on, VBGR to AUXADC 11: Buffer off
2:0	**VBE_SEL**	VBE_SEL	**Selects VBE**

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